MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS
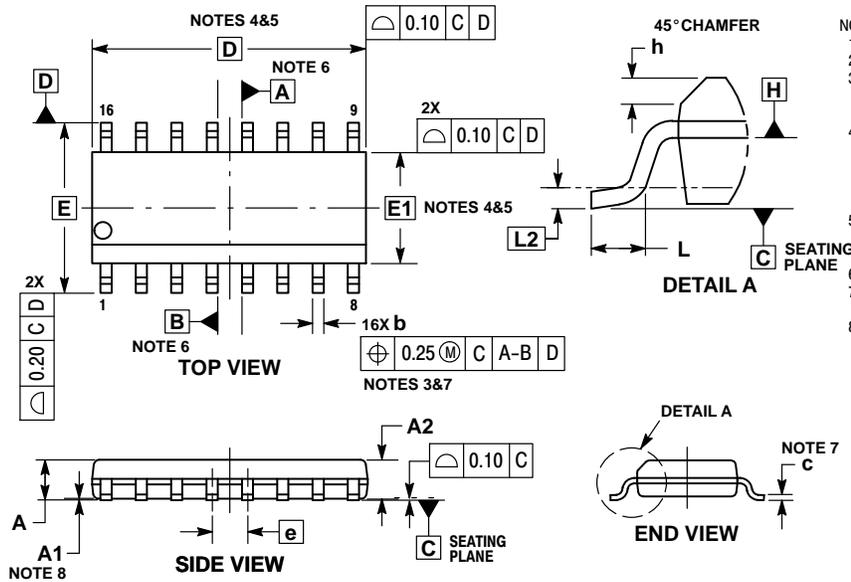
ON Semiconductor®

SOIC−16
CASE 751BA
ISSUE A

SCALE 1:1

DATE 18 MAY 2015

TOP VIEW

NOTES 4&5

$\boxed{\triangle\ 0.10\ \text{C}\ \text{D}}$

NOTE 6

2X $\boxed{\triangle\ 0.10\ \text{C}\ \text{D}}$

E1 NOTES 4&5

2X $\boxed{0.20\ \text{C}\ \text{D}}$

NOTE 6

16X b

$\boxed{\oplus\ 0.25\ \text{Ⓜ}\ \text{C}\ \text{A-B}\ \text{D}}$

NOTES 3&7

SIDE VIEW

$\boxed{\triangle\ 0.10\ \text{C}}$

A2

e

C SEATING PLANE

A

A1 NOTE 8

45° CHAMFER

h

H

L2

L

C SEATING PLANE

DETAIL A

DETAIL A

NOTE 7

c

END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.004 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006 mm PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.010 mm PER SIDE.
5. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOT-TOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTER-MOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM H.
7. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25 FROM THE LEAD TIP.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

| DIM	MILLIMETERS	
	MIN	MAX
A	---	1.75
A1	0.10	0.25
A2	1.25	---
b	0.31	0.51
c	0.10	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
h	0.25	0.41
L	0.40	1.27
L2	0.25 BSC	

RECOMMENDED SOLDERING FOOTPRINT*

16X 0.76

16X 1.52

7.00

1.27 PITCH
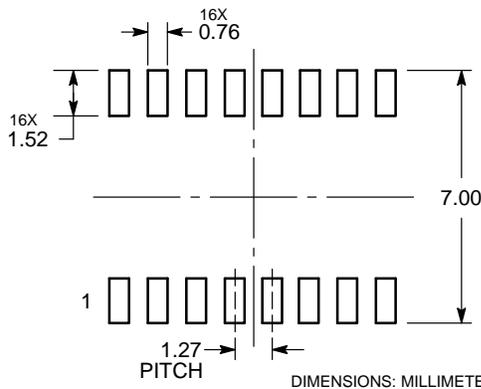
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXXXXXXXX
AWLYWWG
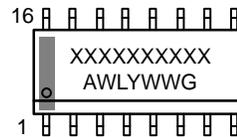
XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G", may or not be present.

DOCUMENT NUMBER:	98AON34919E	
STATUS:	ON SEMICONDUCTOR STANDARD	
REFERENCE:		
DESCRIPTION:	SOIC−16	PAGE 1 OF 2

Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.

ISSUE	REVISION	DATE
O	RELEASED FOR PRODUCTION FROM POD #6000209 TO ON SEMICONDUCTOR. REQ. BY B. BERGMAN.	19 SEP 2008
A	REDREW DRAWING TO JEDEC STANDARDS AND ADDED SOLDER FOOTPRINT. REQ. BY F. KOLANKO.	18 MAY 2015