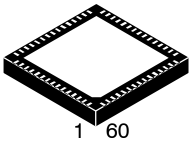
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

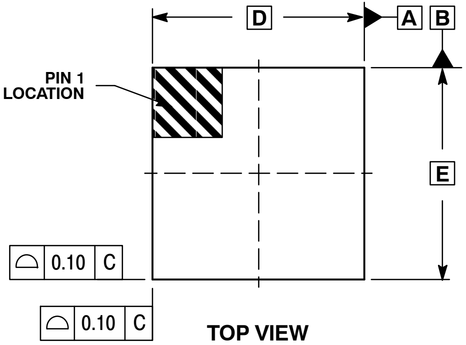
ON Semiconductor®

QFN60 7x7, 0.4P
CASE 485BB−01
ISSUE A

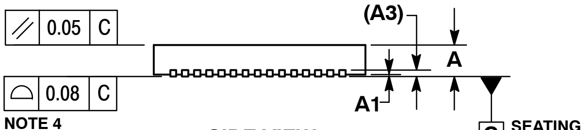
DATE 07 DEC 2009



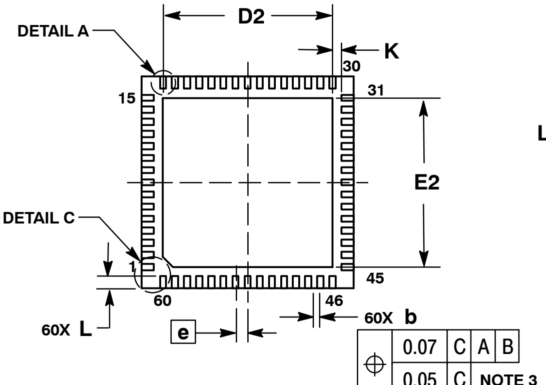
SCALE 2:1



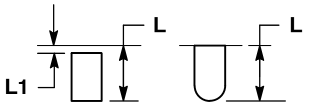
TOP VIEW



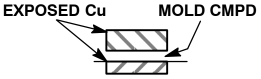
SIDE VIEW



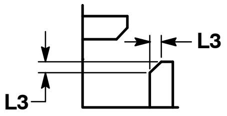
BOTTOM VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTIONS

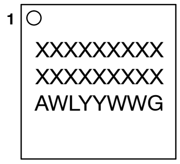


DETAIL C
ALTERNATE CORNER LEAD CONSTRUCTION

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED ABETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	7.00 BSC	
D2	5.50	5.70
E	7.00 BSC	
E2	5.50	5.70
e	0.40 BSC	
K	0.30 REF	
L	0.30	0.50
L1	---	0.15
L3	0.10 REF	

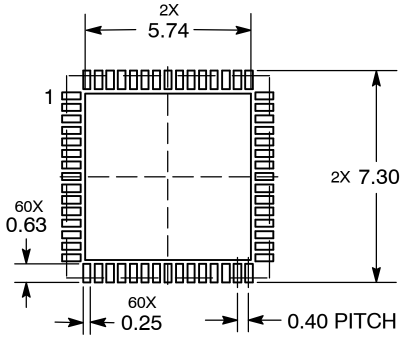
GENERIC MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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NEW STANDARD:		
DESCRIPTION:	**QFN60 7X7, 0.40P**	**PAGE 1 OF 2**

ON Semiconductor®	**DOCUMENT NUMBER:** **98AON45860E** **PAGE 2 OF 2**

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O	RELEASED FOR PRODUCTION. REQ. D. SHORT.	29 OCT 2009
A	ADDED DETAIL C FOR CHAMFERED LEADS. REQ. D. SHORT.	07 DEC 2009

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