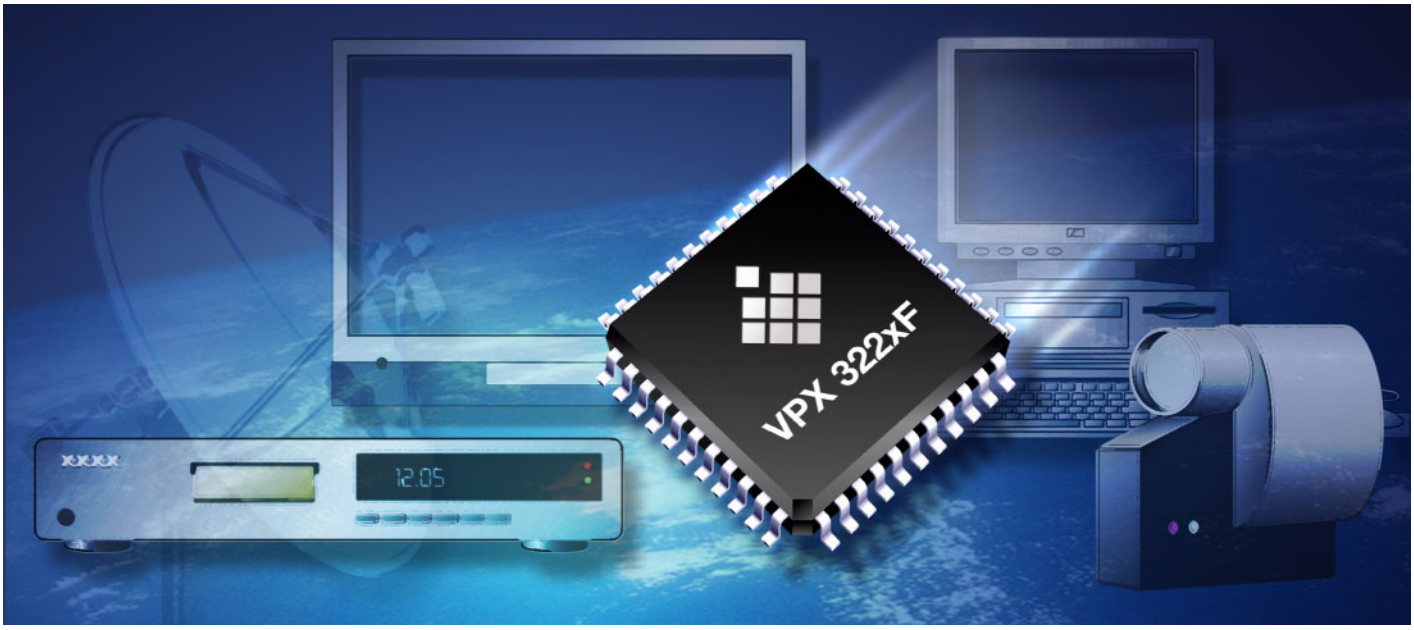
MULTIMEDIA

MICRONAS

# VPX 322xF

Feb/2003




# VPX 322xF
# Video Pixel Decoder

The Video Pixel Decoder VPX 322xF is the fourth generation of full-feature video acquisition IC for consumer video and multimedia applications. All of the processing units necessary to convert an analog video signal into a digital component stream have been integrated onto a single 44- or 64-pin IC. Additionally, the VPX 322xF provides text slicing for Intercast, Teletext, and Closed Caption. An adaptive 4H comb filter allows improved Y/C separation. In addition to the VPX 3226F, the VPX 3228F provides an analog component video interface. All chips are pin-compatible to the VPX 322xE.

## New Features
(compared to VPX 322xE)

- Analog $YP_rP_b$ input (VPX 3228F only)
- Additional access of closed caption and CGMS data via $I^2C$
- Full Macrovision 7.01 detection
- New small-outline package (64-PQFN)

## Video Decoding

- High-performance adaptive 4H comb filter Y/C separator with adjustable vertical peaking
- Multistandard color decoding:
  - NTSC-M, NTSC-443
  - PAL-BDGHI, PAL-M, PAL-N, PAL-60
  - SECAM, S-VHS
- Video ADCs with clamping and automatic gain control (AGC)
- Seven analog inputs with integrated selector for the following sources:
  - 4×composite video (CVBS), or
  - 2×CVBS and 2×Y/C (S-VHS), or
  - 2×CVBS, 1×Y/C and 1×$YP_rP_b$

  (Some inputs are available only in the 64-pin version.)
- Decoding and detection of Macrovision 7.01 protected video

## Video Processing

- Hue, brightness, contrast, and saturation control
- Dual-window cropping and scaling
- Horizontal resizing between 32 and 864 pixels/line
- Vertical resizing by line dropping
- High-quality anti-aliasing filter
- Scaling controlled peaking and coring

## Video Interfacing

- Digital $YC_rC_b$ 4:2:2 format
- ITU-R 601/656 compliant output format
- Square pixel format (640/768 pixels/line)
- 8-bit or 16-bit synchronous output mode
- 13.5 MHz/16-bit and 27 MHz/8-bit output rate
- VBI bypass and raw ADC data output

## Data Broadcast Support

- High-performance hardware data slicing
- Multistandard data slicer
  - NABTS, WST
  - CAPTION (1×, 2×), CGMS, VPS, WSS, Antiope
- Full support for
  - Teletext, Intercast
  - WebTV for Windows, EPG services
- Programmable to new standards via $I^2C$
- VBI and Full-field mode
- Data insertion into video stream
- Simultaneous acquisition of Teletext, VPS, WSS, and Caption

# VPX 322xF

Feb/2003

## Miscellaneous

- 44-pin PMQFP and 64-pin PMQFP/ PQFN packages
- Reduced power consumption of about 500 mW
- $I^2C$ serial control, two different device addresses
- On-chip clock generation, single crystal
- Eight user-programmable I/O pins

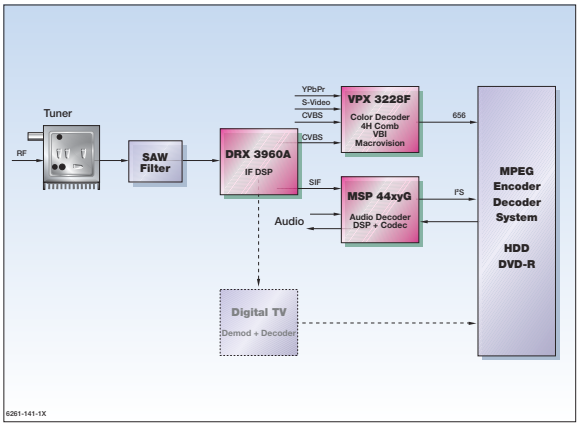



**Fig. 1:** Typical application

## System Architecture

The block diagram illustrates the signal flow through the VPX 322xF. The analog front-end performs input selection, clamping, AGC, and A/D conversion allowing CVBS, S-VHS and $YP_rP_b$ input. The color decoder separates the luma and chroma signals, demodulates the chroma and filters the luminance. The video processing stage resizes the $YP_rP_b$ samples, adjusts the contrast and brightness, and interpolates the chroma. The text slicer extracts lines with text information and delivers decoded data bytes to the video interface.

The VPX 322xF is register compatible to the VPX 322xE family. Please note, that in the 44-pin versions VIN1 cannot alternatively be used as CIN.

For further information please contact multimedia@micronas.com.

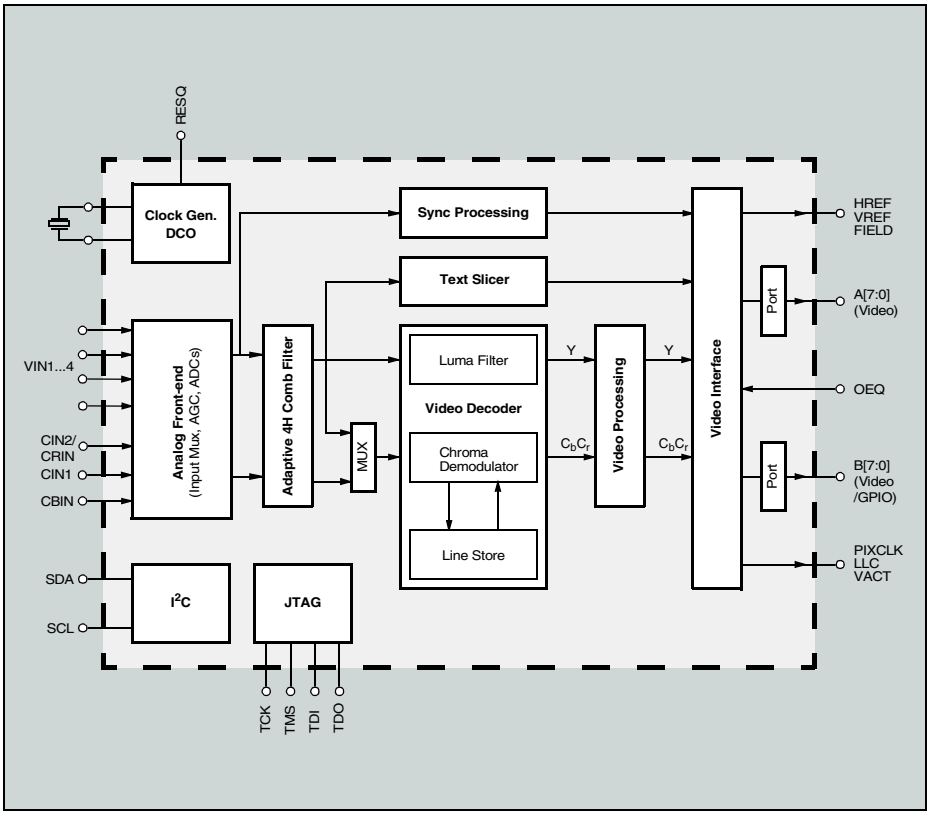



**Fig. 2:** Block diagram of the VPX 322xF

All information and data contained in this product information are without any commitment, are not to be considered as an offer for conclusion of a contract, nor shall they be construed as to create any liability. Product or development sample availability and delivery are exclusively subject to our respective order confirmation form. By this publication, Micronas GmbH does not assume responsibility for patent infringements or other rights of third parties which may result from its use.

No part of this publication may be reproduced, photocopied, stored on a retrieval system, or transmitted without the express written consent of Micronas GmbH.

Edition Feb. 20, 2003; Order No. 6251-607-1PI

Micronas GmbH · Hans-Bunte-Strasse 19 · D-79108 Freiburg (Germany) · P.O. Box 840 · D-79008 Freiburg (Germany)
Tel. +49-761-517-0 · Fax +49-761-517-2174 · E-mail: docservice@micronas.com · www.micronas.com