

**VPS12**

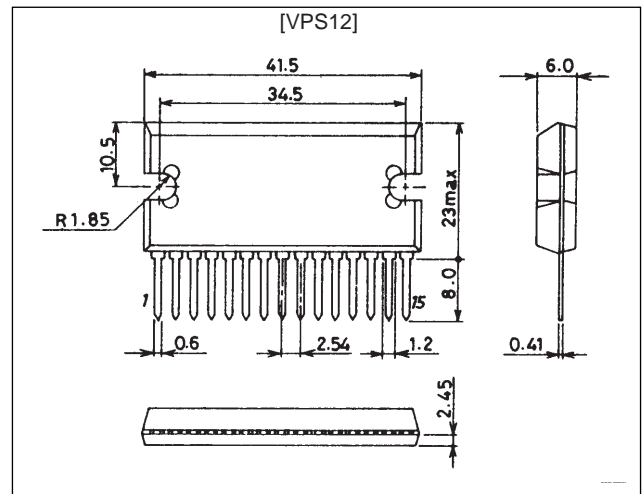
CRT Display Video Output Amplifier: High-Voltage, Wideband Amplifier

Features

- High output voltage and wide bandwidth: optimal for use in color monitors in the f_H (horizontal deflection frequency) = 90-kHz class ($f = 120 \text{ MHz} -3 \text{ dB at } V_{\text{OUT}} = 40 \text{ V}_{\text{p-p}}$)
- Package: Molded 15-pin SIP package housing 3 channels in a single package

Package Dimensions

unit: mm

2127A

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{\text{CC max}}$		90	V
	$V_{\text{BB max}}$		15	V
Allowable power dissipation	$P_d \text{ max}$	At $T_c = 25^\circ\text{C}$ with an ideal heat sink	25	W
Maximum junction temperature	$T_j \text{ max}$		150	$^\circ\text{C}$
Maximum case temperature	$T_c \text{ max}$		100	$^\circ\text{C}$
Storage temperature	T_{stg}		-20 to +110	$^\circ\text{C}$

Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		80	V
	V_{BB}		10	V

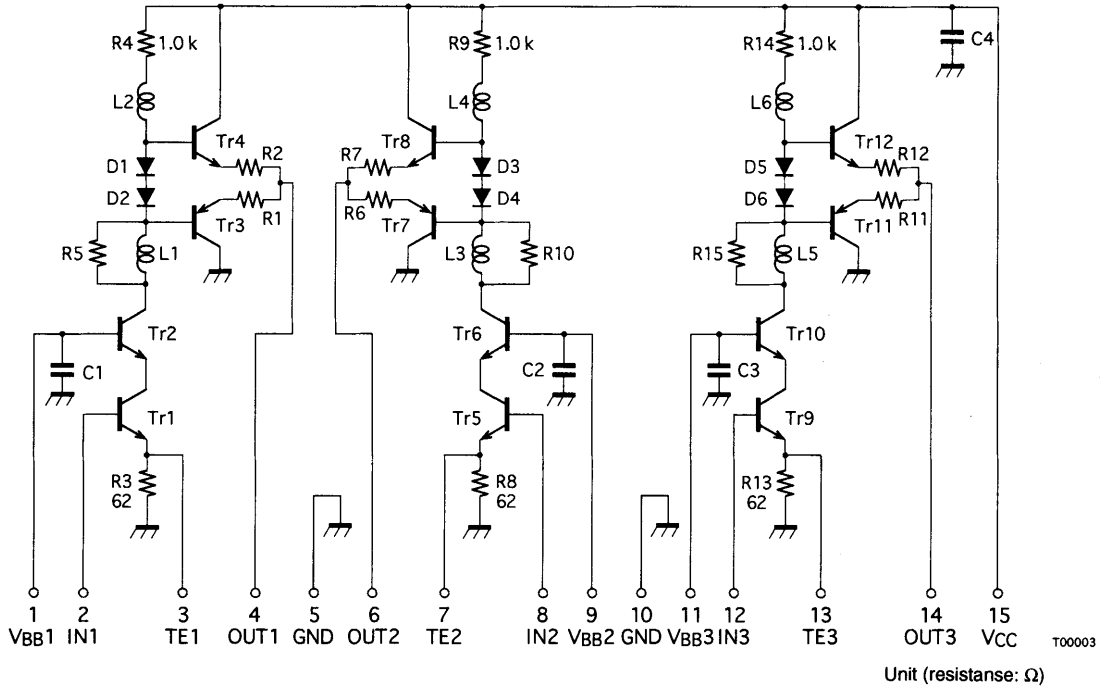
Electrical Characteristics at $T_a = 25^\circ\text{C}$ (for a single channel)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Frequency band (-3 dB)	f_c	$V_{\text{CC}} = 80 \text{ V}$, $V_{\text{BB}} = 10 \text{ V}$, $C_L = 10 \text{ pF}$ $V_{\text{IN}} (\text{DC}) = 3.2 \text{ V}$, $V_{\text{OUT}} (\text{p-p}) = 40 \text{ V}$		120		MHz
Pulse response	t_r	$V_{\text{CC}} = 80 \text{ V}$, $V_{\text{BB}} = 10 \text{ V}$, $C_L = 10 \text{ pF}$		4.2		ns
	t_f	$V_{\text{IN}} (\text{DC}) = 3.2 \text{ V}$, $V_{\text{OUT}} (\text{p-p}) = 40 \text{ V}$		3.2		ns
Voltage gain	VG (DC)		13	15	17	Times
Current drain	$I_{\text{CC}} (1)$	$V_{\text{CC}} = 80 \text{ V}$, $V_{\text{BB}} = 10 \text{ V}$, $V_{\text{IN}} (\text{DC}) = 2.9 \text{ V}$, $f = 10 \text{ MHz clock}$, $C_L = 10 \text{ pF}$, $V_{\text{OUT}} (\text{p-p}) = 40 \text{ V}$		45		mA
	$I_{\text{CC}} (2)$	$V_{\text{CC}} = 80 \text{ V}$, $V_{\text{BB}} = 10 \text{ V}$, $V_{\text{IN}} (\text{DC}) = 2.9 \text{ V}$, $f = 120 \text{ MHz clock}$, $C_L = 10 \text{ pF}$, $V_{\text{OUT}} (\text{p-p}) = 40 \text{ V}$		70		mA

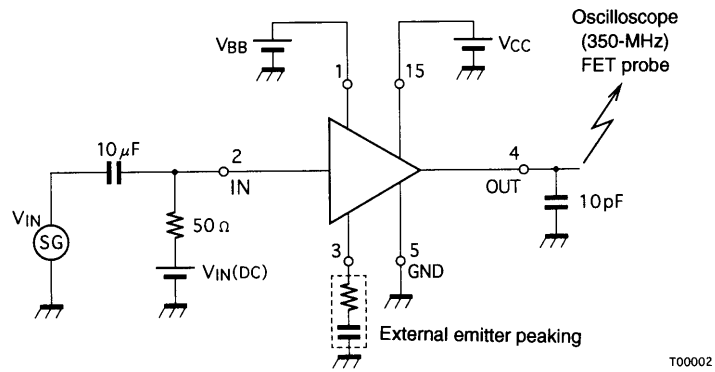
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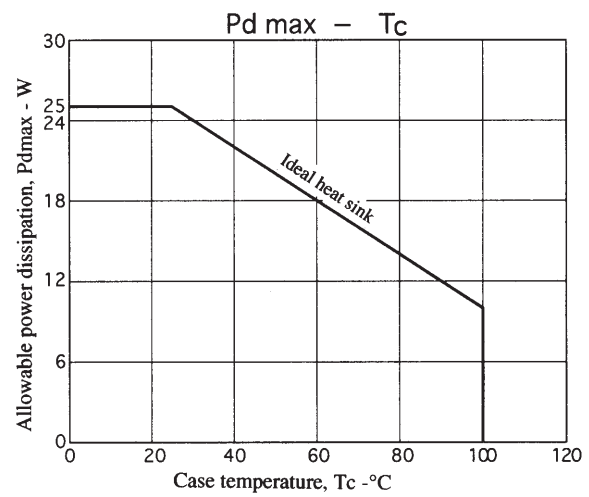
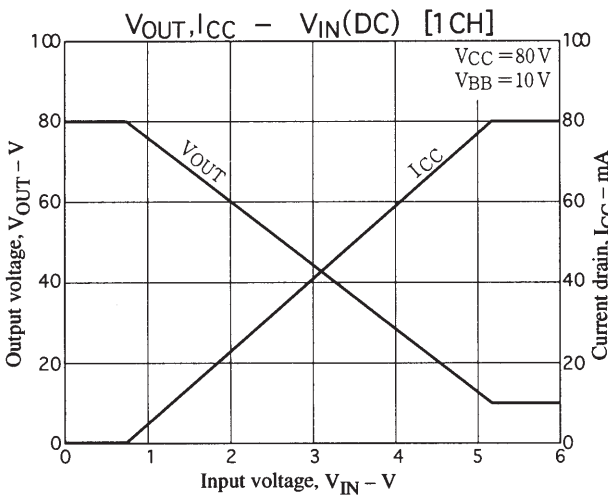
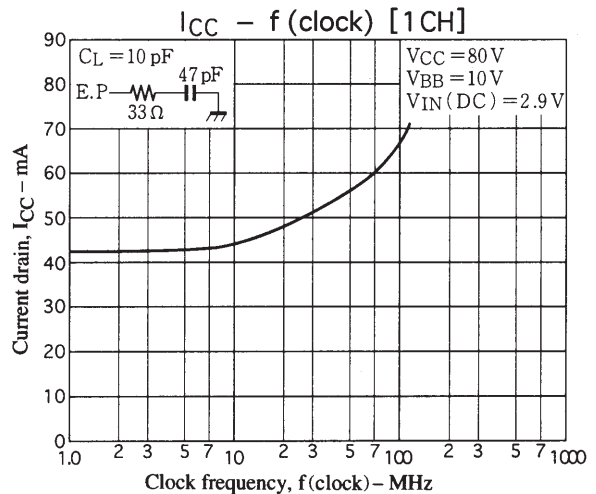
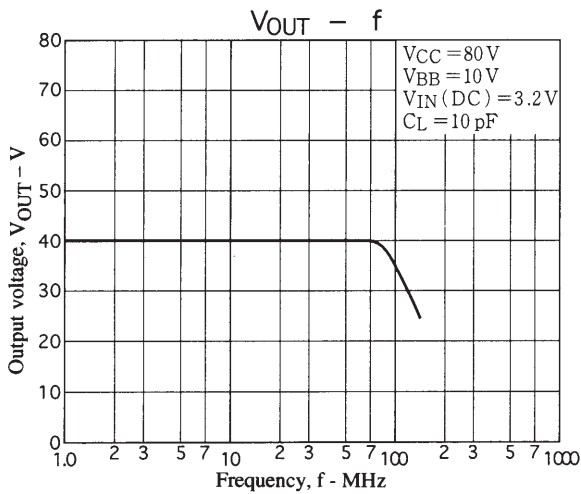
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Internal Equivalent Circuit



Test Circuit (for testing a single channel)





Thermal Design

Since the VPS12 has the three-channel configuration shown in the circuit diagram on page 2, we first consider a single channel. The chip temperatures of the transistors during operation can be determined from the following formula:

$$T_j = (T_{ri}) = \theta_{j-c} (T_{ri}) \times P_c (T_{ri}) + \Delta T_c + T_a \text{ (}^\circ\text{C)} \dots\dots\dots(1)$$

$\theta_{j-c} (T_{ri})$: Thermal resistances of the transistor chips themselves

$P_c (T_{ri})$: Collector loss of the transistors

ΔT_c : Increase in case temperature

T_a : Ambient temperature

The $\theta_{j-c} (T_{ri})$ for the individual transistors is:

$$\theta_{j-c}(Tr1) \text{ to } (Tr4) = 35^\circ\text{C/W} \dots\dots\dots(2)$$

Although the loss in each transistor in the video pack changes with frequency and thus are not identical, assuming a maximum frequency of 120 MHz (clock), the transistor with the largest loss is Tr3 in the emitter-follower stage. From the Pd-f(clock) figure it can be seen that this loss is 22% of the total loss. Thus:

$$P_c (EF \text{ stage})_{f=120 \text{ MHz}} = P_d (1ch)_{f=120 \text{ MHz}} \times 0.22 \text{ [W]} \dots\dots\dots(3)$$

Select a θ_h for the heat sink so that the junction temperature (T_j) of this transistor does not exceed 150°C. Equation (4) gives the relationship between θ_h and ΔT_c .

$$\Delta T_c = P_d (TOTAL) \times \theta_h \dots\dots\dots(4)$$

The required θ_h can be calculated from this equation and equation (1).

VPS12 Thermal Design Example

Conditions: $f_V = 120$ MHz (clock) in an $f_H = 85$ -kHz class monitor
 $V_{CC} = 80$ V, $V_{BB} = 10$ V, $V_{OUT} = 40$ Vp-p ($C_L = 10$ pF)

Consider using this monitor at $T_a = 60^\circ\text{C}$ and operating it at a maximum frequency of $f = 120$ MHz (clock).

As was mentioned previously, the chip with the largest loss is Tr3 in the emitter-follower stage. Deriving that value from the figures below and equation (3) gives:

$$P_c (\text{EF stage}) = 5.8 \times 0.22 \approx 1.3 \text{ [W]} \dots\dots\dots(5)$$

Next, applying the value of θ_{j-c} to equation (5) shows ΔT_j to be as follows:

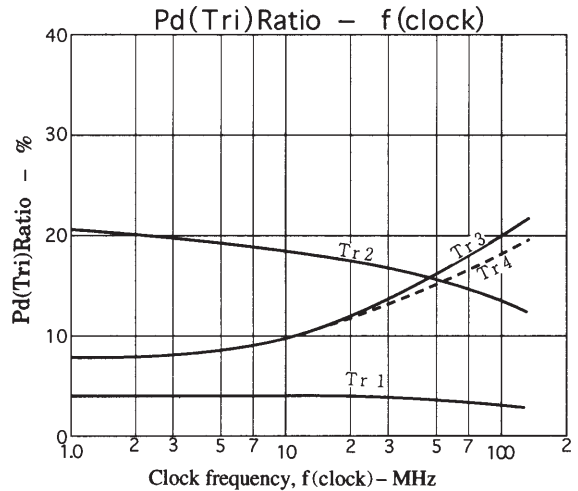
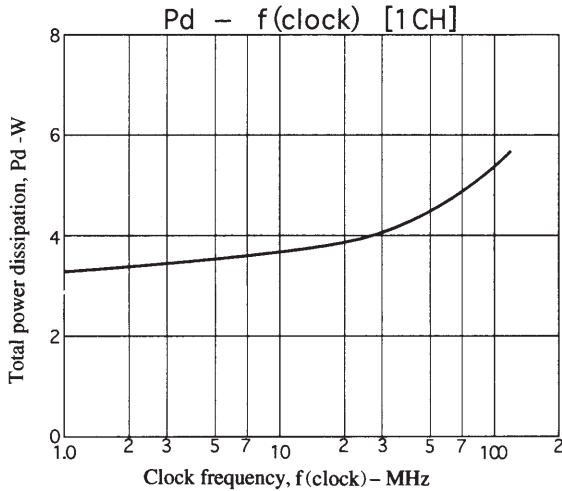
$$\Delta T_j = 1.3 \times 35 = 45.5 \text{ [}^\circ\text{C]}$$

Here, ΔT_j is less than 50°C , and in the thermal design we only have to assure that T_c is less than 100°C . That is, we must set θ_h so that T_c is less than 100°C when $P_d (\text{TOTAL}) = P_d (\text{one channel}) \times 3$.

$$\text{Here, } \Delta T_c \text{ will be } \Delta T_c = 100 - 60 = 40^\circ\text{C}$$

$$\text{Since } \theta_h = \Delta T_c \div P_d (\text{TOTAL}) = 40 \div (5.8 \times 3) = 2.3, \text{ then } \theta_h = 2.3 \text{ }^\circ\text{C/W.}$$

In an actual system, it may be possible to use a heat sink smaller than the one required for the value calculated above due to the actual ambient temperature and other operating conditions. Actual designs should be optimized to match those conditions using the data presented above.



V_{CC} (V)	V_{BB} (V)	V_{OUT} (V)	V_O (center)
80	10	40	45

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