Ordering number : EN5309A

Wideband Output Module (Video Pack)

VPS12

CRT Display Video Output Amplifier: High-Voltage, Wideband Amplifier

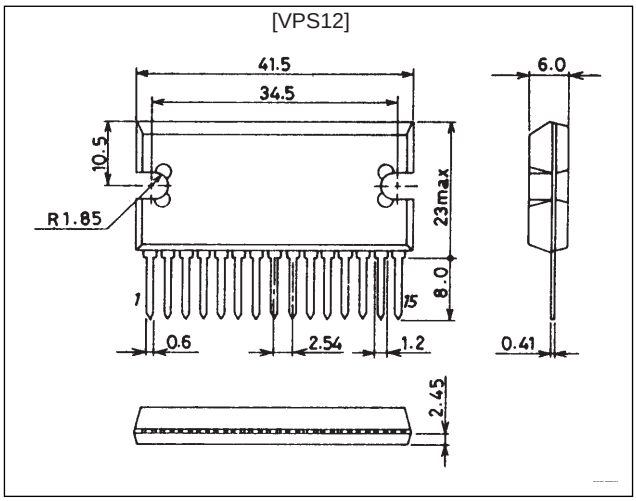
Features

- High output voltage and wide bandwidth: optimal for use in color monitors in the f_H (horizontal deflection frequency) = 90-kHz class
  (f = 120 MHz –3 dB at V_{OUT} = 40 Vp-p)
- Package: Molded 15-pin SIP package housing 3 channels in a single package

Package Dimensions

unit: mm

2127A



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		90	V
	V_{BB} max		15	V
Allowable power dissipation	Pd max	At Tc = 25°C with an ideal heat sink	25	W
Maximum junction temperature	Tj max		150	°C
Maximum case temperature	Tc max		100	°C
Storage temperature	Tstg		–20 to +110	°C

Operating Conditions at Ta = 25°C

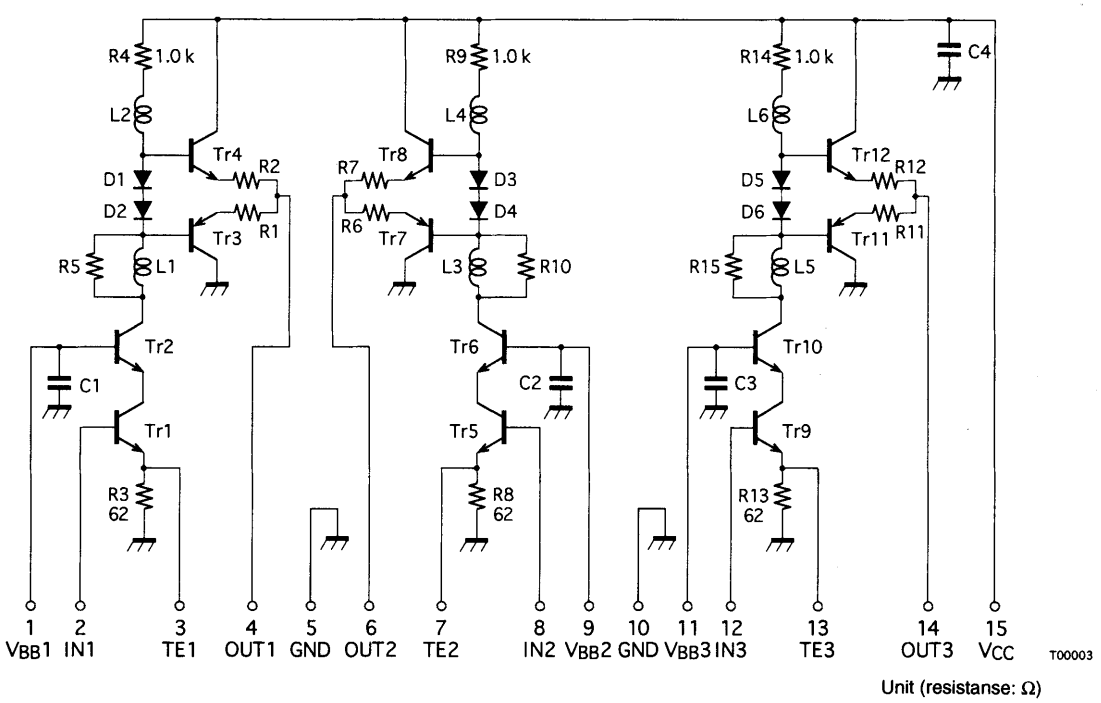
Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		80	V
	V_{BB}		10	V

Electrical Characteristics at Ta = 25°C (for a single channel)

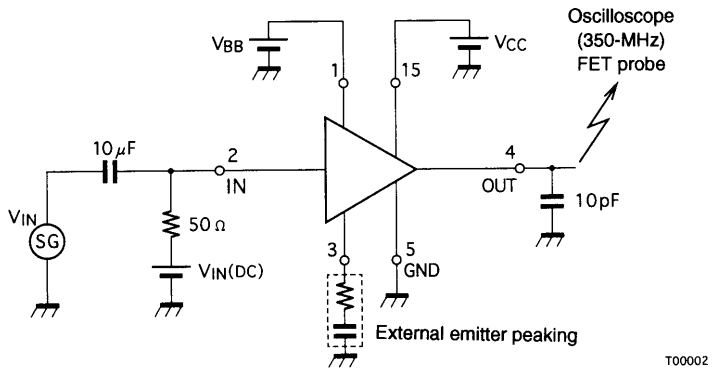
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Frequency band (–3 dB)	f_c	V_{CC} = 80 V, V_{BB} = 10 V, C_L = 10 pF V_{IN} (DC) = 3.2 V, V_{OUT} (p-p) = 40 V		120		MHz
Pulse response	t_r	V_{CC} = 80 V, V_{BB} = 10 V, C_L = 10 pF		4.2		ns
	t_f	V_{IN} (DC) = 3.2 V, V_{OUT} (p-p) = 40 V		3.2		ns
Voltage gain	VG (DC)		13	15	17	Times
Current drain	I_{CC} (1)	V_{CC} = 80 V, V_{BB} = 10 V, V_{IN} (DC) = 2.9 V, f = 10 MHz clock, C_L = 10 pF, V_{OUT} (p-p) = 40 V		45		mA
	I_{CC} (2)	V_{CC} = 80 V, V_{BB} = 10 V, V_{IN} (DC) = 2.9 V, f = 120 MHz clock, C_L = 10 pF, V_{OUT} (p-p) = 40 V		70		mA

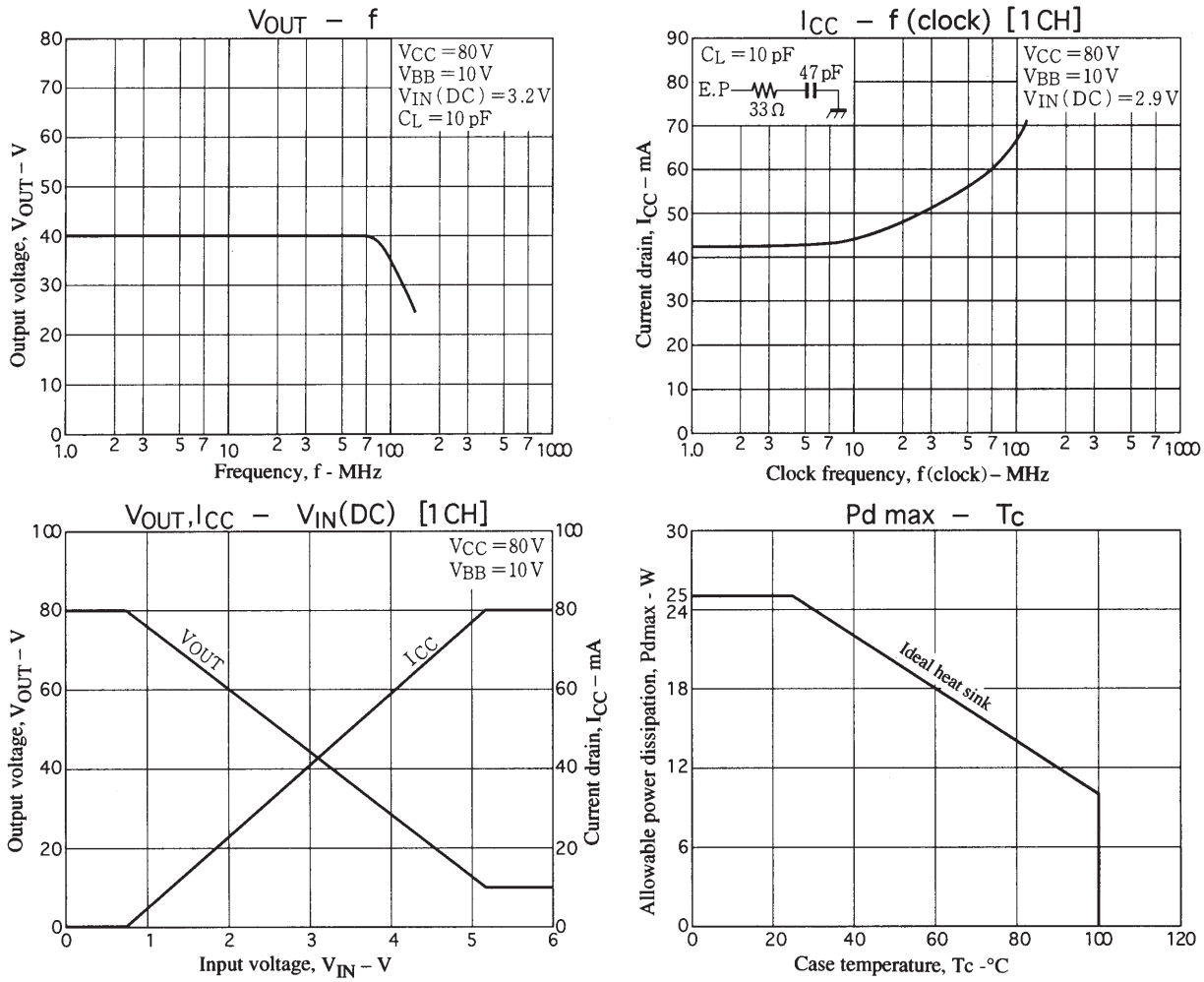
SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

Internal Equivalent Circuit



Test Circuit (for testing a single channel)





Thermal Design

Since the VPS12 has the three-channel configuration shown in the circuit diagram on page 2, we first consider a single channel. The chip temperatures of the transistors during operation can be determined from the following formula:

$$Tj = (Tri) = \theta j\text{-}c\ (Tri) \times Pc\ (Tri) + \Delta Tc + Ta\ (°C) \quad \text{.....(1)}$$

θj-c (Tri): Thermal resistances of the transistor chips themselves
Pc (Tri): Collector loss of the transistors
ΔTc: Increase in case temperature
Ta: Ambient temperature

The θj-c (Tri) for the individual transistors is:

$$\theta j\text{-}c(Tr1) \text{ to } (Tr4) = 35°C/W \quad \text{.....(2)}$$

Although the loss in each transistor in the video pack changes with frequency and thus are not identical, assuming a maximum frequency of 120 MHz (clock), the transistor with the largest loss is Tr3 in the emitter-follower stage. From the Pd-f(clock) figure it can be seen that this loss is 22% of the total loss. Thus:

$$Pc\ (EF\ stage)_{f = 120\ MHz} = Pd\ (1ch)_{f = 120\ MHz} \times 0.22\ [W] \quad \text{.....(3)}$$

Select a θh for the heat sink so that the junction temperature (Tj) of this transistor does not exceed 150°C. Equation (4) gives the relationship between θh and ΔTc.

$$\Delta Tc = Pd\ (TOTAL) \times \theta h \quad \text{.....(4)}$$

The required θh can be calculated from this equation and equation (1).

VPS12 Thermal Design Example

Conditions: f_V = 120 MHz (clock) in an f_H = 85-kHz class monitor
V_{CC} = 80 V, V_{BB} = 10 V, V_{OUT} = 40 Vp-p (C_L = 10 pF)

Consider using this monitor at Ta = 60°C and operating it at a maximum frequency of f = 120 MHz (clock).

As was mentioned previously, the chip with the largest loss is Tr3 in the emitter-follower stage. Deriving that value from the figures below and equation (3) gives:

$$Pc \text{ (EF stage)} = 5.8 \times 0.22 \approx 1.3 \text{ [W]} \quad \text{.....(5)}$$

Next, applying the value of θj-c to equation (5) shows ΔTj to be as follows:

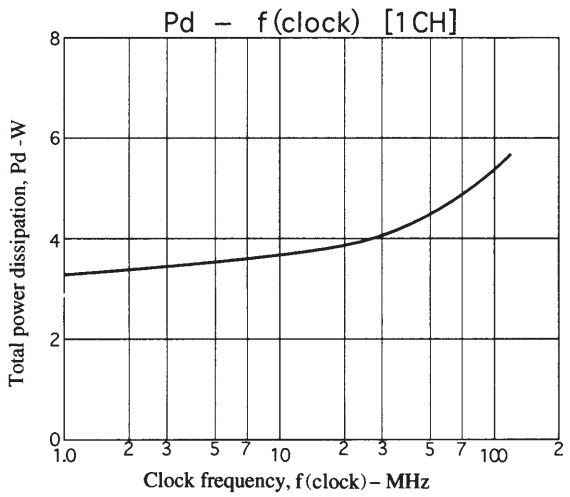
$$\Delta Tj = 1.3 \times 35 = 45.5 \text{ [°C]}$$

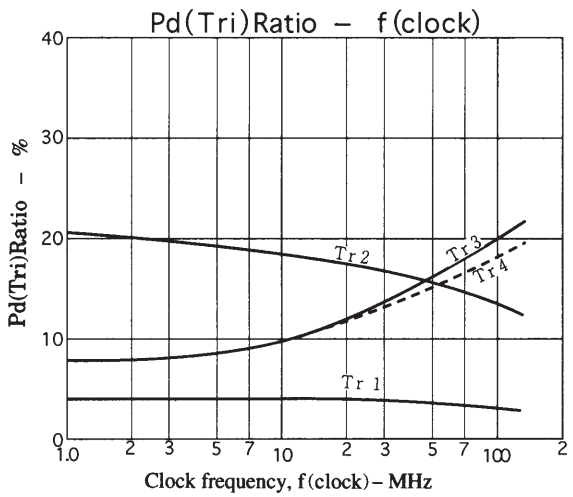
Here, ΔTj is less than 50°C, and in the thermal design we only have to assure that Tc is less than 100°C. That is, we must set θh so that Tc is less than 100°C when Pd (TOTAL) = Pd (one channel) × 3.

Here, ΔTc will be ΔTc = 100 – 60 = 40°C

Since θh = ΔTc ÷ Pd (TOTAL) = 40 ÷ (5.8 × 3) = 2.3, then θh = 2.3 °C/W.

In an actual system, it may be possible to use a heat sink smaller than the one required for the value calculated above due to the actual ambient temperature and other operating conditions. Actual designs should be optimized to match those conditions using the data presented above.





V_{CC} (V)	V_{BB} (V)	V_{OUT} (V)	V_O (center)
80	10	40	45