DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD98503

NETWORK CONTROLLER

The μPD98503 is a high performance controller which can perform TCP/IP and USB protocol stacks or other application system related software. It includes high performance MIPS™ based 64-bit RISC processor VR4120A™ CPU core, Ethernet™ controller, USB controller block, general purpose input/output functions and a memory/system-bus interface.

Detailed function descriptions are provided in the following user's manual. Be sure to read the manual before designing.
μPD98503 User's Manual: S15906E

FEATURES

- Includes high performance MIPS based 64-bit RISC processor VR4120A
- Can perform RTOS and network middleware (M/W) on the chip
- Includes interface for PROM and flash ROM used for storing boot program
- Includes 10/100 Mbps Ethernet controllers compliant to IEEE802.3, IEEE802.3u and IEEE802.3x
- Can directly connect external Ethernet PHY device through 3.3-V MII interface
- Includes USB full speed function controller compliant to USB specification 1.1
- Supports operation conforming to the USB Communication Device Class Specification
- Can directly connect 64-Mbit and 128-Mbit SDRAM as external memory
- Includes boundary scan function (JTAG) compliant to IEEE 1149.1
- Includes UART and Micro Wire™ interface
- Includes 2-channel general purpose timers
- Includes 16 general purpose input/output pins
- Using advanced CMOS technology
- Supply voltage : 3.3 V (I/O) / 2.5 V (Core)
- Package 256-pin Tape-BGA

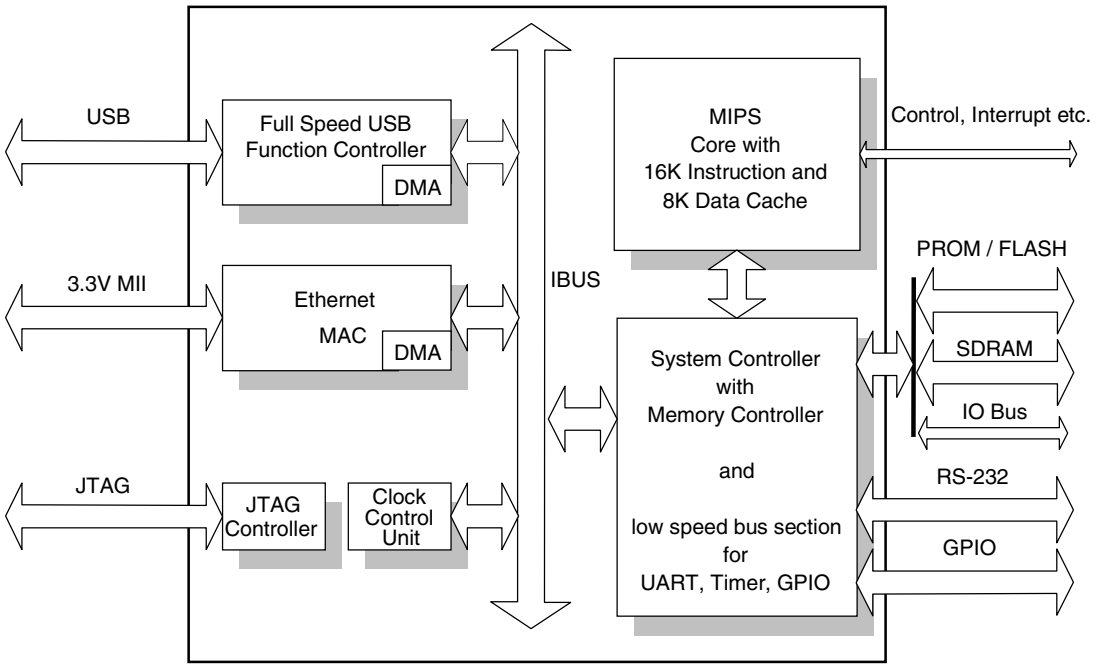
ORDERING INFORMATION

Part Number	Package
μPD98503N7-B6	256-pin tape BGA (heat spreader type) (27 × 27)

Document No. S15894EJ2V0DS00 (2nd edition)
Date Published November 2002 NS CP (K)
Printed in Japan

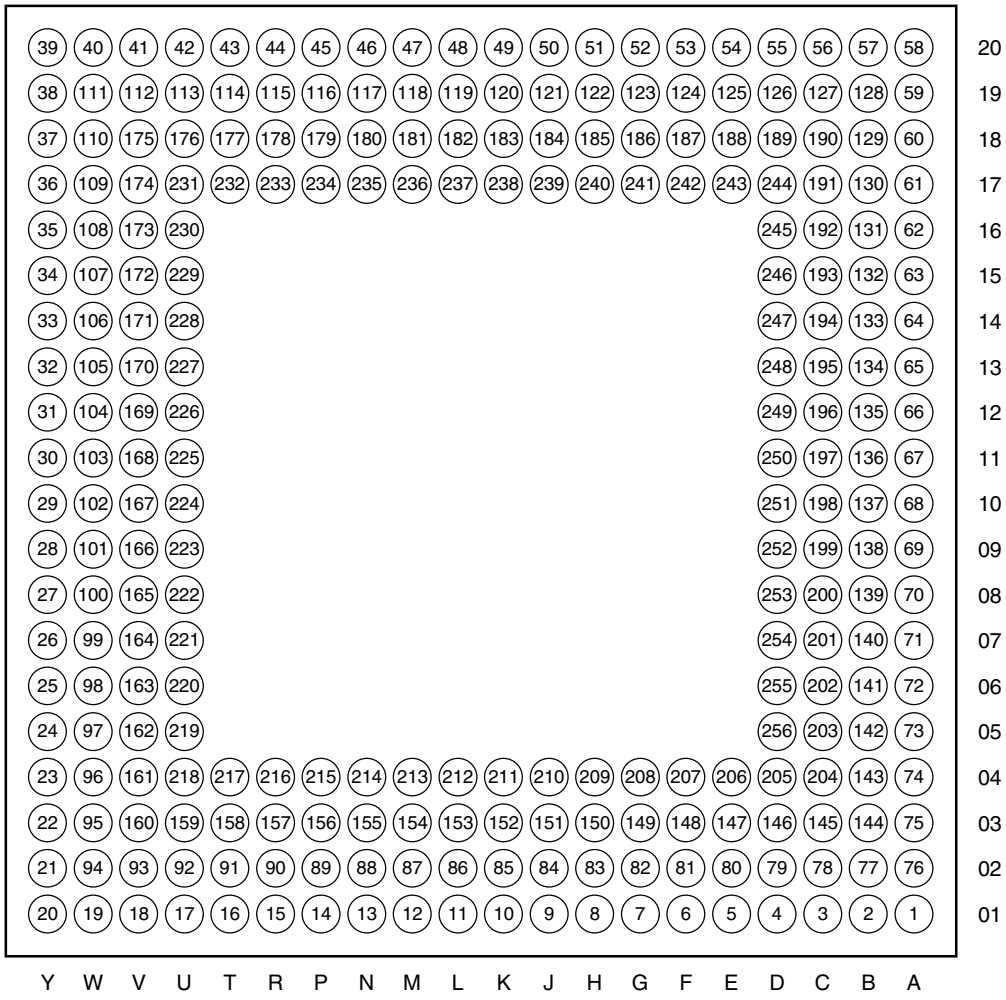
The mark ★ shows major revised points.

BLOCK DIAGRAM



PIN CONFIGURATION (Bottom View)

- **256-pin tape BGA (heat spread type) (27 × 27)**
  μPD98503N7-B6



Pin Name

(1/2)

Address No.	Pin No.	Pin Name	Address No.	Pin No.	Pin Name	Address No.	Pin No.	Pin Name	Address No.	Pin No.	Pin Name
A01	1	IC-PUpR	C06	202	GPIO2	F03	148	IC-PDn	L20	48	SDCAS_B
A02	76	IC-Open	C07	201	IVDD	F04	207	IC-Open	M01	12	IC-PDn
A03	75	ENDCEN	C08	200	GND	F17	242	SMA19	M02	87	IC-PDn
A04	74	RMSL0	C09	199	GPIO10	F18	187	SMA20	M03	154	IVDD
A05	73	GPIO0	C10	198	IVDD	F19	124	SRMOE_B	M04	213	GND
A06	72	GPIO4	C11	197	EXINT_B	F20	53	SRMCS_B	M17	236	GND
A07	71	GPIO6	C12	196	GND	G01	7	IC-PDn	M18	181	SMD2
A08	70	GPIO8	C13	195	URDSR_B	G02	82	IC-PDn	M19	118	SMD1
A09	69	EXNMI_B	C14	194	IVDD	G03	149	IVDD	M20	47	SMD0
A10	68	GPIO13	C15	193	URSDI	G04	208	GND	N01	13	GND
A11	67	GPIO14	C16	192	SMA4	G17	241	GND	N02	88	MIMD
A12	66	MWDI	C17	191	SMA6	G18	186	IVDD	N03	155	MIRD0
A13	65	MWDO	C18	190	IVDD	G19	123	SEXCS0_B	N04	214	EVDD
A14	64	URDCD_B	C19	127	SMA12	G20	52	SEXCS1_B	N17	235	EVDD
A15	63	URDTR_B	C20	56	SMA14	H01	8	GND	N18	180	SMD5
A16	62	SMA1	D01	4	GND	H02	83	IVDD	N19	117	SMD4
A17	61	SMA3	D02	79	IC-Open	H03	150	GND	N20	46	SMD3
A18	60	SMA5	D03	146	IC-Open	H04	209	EVDD	P01	14	MIRD1
A19	59	SMA8	D04	205	GND	H17	240	EVDD	P02	89	MIRD2
A20	58	SMA9	D05	256	EVDD	H18	185	GND	P03	156	IVDD
B01	2	IC-PUpR	D06	255	GPIO1	H19	122	SEXCS2_B	P04	215	GND
B02	77	IC-PUpR	D07	254	GND	H20	51	SDCS_B	P17	234	GND
B03	144	IC-PDnR	D08	253	EVDD	J01	9	IC-PDn	P18	179	IVDD
B04	143	IC-PDn	D09	252	GPIO9	J02	84	IC-PDn	P19	116	SMD7
B05	142	RMSL1	D10	251	GND	J03	151	IC-Open	P20	45	SMD6
B06	141	GPIO3	D11	250	EVDD	J04	210	IC-Open	R01	15	MIRD3
B07	140	GPIO5	D12	249	MWSK	J17	239	SDCKE1	R02	90	MIRER
B08	139	GPIO7	D13	248	URRTS_B	J18	184	SDRAS_B	R03	157	MIRDV
B09	138	GPIO11	D14	247	GND	J19	121	SDCKE0	R04	216	MITD0
B10	137	GPIO12	D15	246	SMA0	J20	50	SDCLK0	R17	233	SMD11
B11	136	GPIO15	D16	245	EVDD	K01	10	IC-PDn	R18	178	SMD10
B12	135	MWCS	D17	244	GND	K02	85	IC-PDn	R19	115	SMD9
B13	134	URCTS_B	D18	189	SMA13	K03	152	GND	R20	44	SMD8
B14	133	URCLK	D19	126	SMA15	K04	211	IVDD	T01	16	MITD1
B15	132	URSDO	D20	55	SMA16	K17	238	GND	T02	91	MITD2
B16	131	SMA2	E01	5	GND	K18	183	IVDD	T03	158	MICRS
B17	130	GND	E02	80	IVDD	K19	120	SDCLK1	T04	217	GND
B18	129	SMA7	E03	147	IC-Open	K20	49	GND	T17	232	EVDD
B19	128	SMA10	E04	206	IC-Open	L01	11	IC-PUp	T18	177	SMD14
B20	57	SMA11	E17	243	EVDD	L02	86	IC-PDn	T19	114	SMD12
C01	3	IC-Open	E18	188	GND	L03	153	IVDD	T20	43	GND
C02	78	IC-PUpR	E19	125	SMA17	L04	212	GND	U01	17	MITD3
C03	145	IVDD	E20	54	SMA18	L17	237	SDWE_B	U02	92	MIRCLK
C04	204	GND	F01	6	IC-PDn	L18	182	IC-PDn	U03	159	IC-PDn
C05	203	BIG	F02	81	IC-PDn	L19	119	EVDD	U04	218	GND

(2/2)

Address No.	Pin No.	Pin Name	Address No.	Pin No.	Pin Name	Address No.	Pin No.	Pin Name	Address No.	Pin No.	Pin Name
U05	219	JDO	V04	161	JCK	W03	95	GND	Y02	21	IC-Open
U06	220	IC-PUp	V05	162	EVDD	W04	96	JDI	Y03	22	JMS
U07	221	GND	V06	163	IC-PUp	W05	97	RST_B	Y04	23	JRSTB_B
U08	222	IC-Open	V07	164	IVDD	W06	98	CLKSL	Y05	24	IC-PUp
U09	223	PSDVD	V08	165	PSDGND	W07	99	SCLK	Y06	25	IC-PDn
U10	224	PUDGND	V09	166	PUDVD	W08	100	PSAGND	Y07	26	PSTBY
U11	225	GND	V10	167	IC-PDn	W09	101	PUAVD	Y08	27	PSAVD
U12	226	EVDD	V11	168	IVDD	W10	102	PUSTBY	Y09	28	PUAGND
U13	227	GND	V12	169	USBDM	W11	103	IC-PDn	Y10	29	IC-Open
U14	228	GND	V13	170	IVDD	W12	104	USBDP	Y11	30	USBCLK
U15	229	SMD30	V14	171	IVDD	W13	105	IC-Open	Y12	31	EVDD
U16	230	EVDD	V15	172	SMD31	W14	106	IC-PDn	Y13	32	IC-Open
U17	231	GND	V16	173	SMD27	W15	107	IC-PDn	Y14	33	IC-Open
U18	176	SMD17	V17	174	SMD24	W16	108	GND	Y15	34	IC-PDn
U19	113	SMD15	V18	175	IVDD	W17	109	SMD26	Y16	35	SMD29
U20	42	SMD13	V19	112	SMD18	W18	110	SMD23	Y17	36	SMD28
V01	18	MITCLK	V20	41	SMD16	W19	111	SMD21	Y18	37	SMD25
V02	93	MICOL	W01	19	MITER	W20	40	SMD19	Y19	38	SMD22
V03	160	IVDD	W02	94	MITE	Y01	20	MIMCLK	Y20	39	SMD20

Remarks1. Special pin name description:

IC-PDn: Pull Down
IC-PDnR: Pull Down with Resistor
IC-PUp: Pull Up
IC-PUpR: Pull Up with Resistor
IC-Open: Test output shall be left open

2. In this document, XXX_B stands for active low pin.

CONTENTS

1. PIN FUNCTIONS

Symbol of I/O column indicates following status in this section.

- I : Input
- O : Output
- I/O : Bidirection
- I/OZ : Bidirection (Include Hi-Z state)
- I/OD : Bidirection (Open drain output)
- OZ : Output (Include Hi-Z state)
- OD : Output (Open drain)

1.1 Power Supply

Pin Name	Address No.	Pin No.	I/O	Active Level	Function
GND	B17, C04, C08, C12, D01, D04, D07, D10, D14, D17, E01, E18, G04, G17, H01, H03, H18, K03, K17, K20, L04, M04, M17, N01, P04, P17, T04, T20, U04, U07, U11, U13, U14, U17, W03, W16	130, 204, 200, 196, 4, 205, 254, 251, 247, 244, 5, 188, 208, 241, 8, 150, 185, 152, 238, 49, 212, 213, 236, 13, 215, 234, 217, 43, 218, 221, 225, 227, 228, 231, 95, 108			GND (0 V)
IVDD	C03, C07, C10, C14, C18, E02, G03, G18, H02, K04, K18, L03, M03, P03, P18, V03, V07, V11, V13, V14, V18	145, 201, 198, 194, 190, 80, 149, 186, 83, 211, 183, 153, 154, 156, 179, 160, 164, 168, 170, 171, 175			Internal logic core power supply (+2.5 V)
EVDD	D05, D08, D11, D16, E17, H04, H17, L19, N04, N17, T17, U12, U16, V05, Y12	256, 253, 250, 245, 243, 209, 240, 119, 214, 235, 232, 226, 230, 162, 31			External (I/O) power supply (+3.3 V)

1.2 System PLL Power Supply

Pin Name	Address No.	Pin No.	I/O	Active Level	Function
PSAGND	W08	100			Analog ground (0 V)
PSAVD	Y08	27			Analog power supply (+2.5 V)
PSDGND	V08	165			Digital ground (0 V)
PSDVD	U09	223			Digital power supply (+2.5 V)

Remark The power supply pins of the System PLL shall be blocked with capacitors separately as closed to the device as possible.

1.3 USB PLL Power Supply

Pin Name	Address No.	Pin No.	I/O	Active Level	Function
PUAGND	Y09	28			Analog ground (0 V)
PUAVD	W09	101			Analog power supply (+2.5 V)
PUDGND	U10	224			Digital ground (0 V)
PUDVD	V09	166			Digital power supply (+2.5 V)

Remark The power supply pins of the USB PLL shall be blocked with capacitors separately as closed to the device as possible.

1.4 System Control Interface

Pin Name	Address No.	Pin No.	I/O	Active Level	Function
SCLK	W07	99	I		System clock (33 MHz)
CLKSL	W06	98	I		Clock select for VR4120A and SDRAM (L: 100 MHz/H: 66 MHz)
PSTBY	Y07	26	I	H	System PLL standby mode control (L: active, H: standby)
PUSTBY	W10	102	I	H	USB PLL standby mode control (L: active, H: standby)
BIG	C05	203	I	H	VR4120A big endian mode
ENDCEN	A03	75	I		Endian conversion enable
EXINT_B	C11	197	I	L	External interrupt
EXNMI_B	A09	69	I	L	External non-maskable interrupt
RST_B	W05	97	I	L	System reset
★ RMSL0, RMSL1	A04, B05	74, 142	I		ROM access bus width (RMSL1/0 = L/L: 32 bits, L/H: 16 bits, H/L: 8 bits)

1.5 Memory Interface

Pin Name	Address No.	Pin No.	I/O	Active Level	Function
SDCLK0, SDCLK1	J20, K19	50, 120	O		SDRAM Clock
SDCKE0, SDCKE1	J19, J17	121, 239	O	H	SDRAM Clock Enable
SDCS_B	H20	51	O	L	SDRAM Chip select
SDRAS_B	J18	184	O	L	SDRAM Row address strobe
SDCAS_B	L20	48	O	L	SDRAM Column address strobe
SDWE_B	L17	237	O	L	SDRAM/PROM/FLASH write enable
SRMCS_B	F20	53	O	L	PROM/FLASH chip select
SRMOE_B	F19	124	O	L	PROM/FLASH output enable
SEXCS0_B - SEXCS2_B	G19, G20, H19	123, 52, 122	O	L	Extended Chip Select
SMA0 - SMA20	D15, A16, B16, A17, C16, A18, C17, B18, A19, A20, B19, B20, C19, D18, C20, D19, D20, E19, E20, F17, F18	246, 62, 131, 61, 192, 60, 191, 129, 59, 58, 128, 57, 127, 189, 56, 126, 55, 125, 54, 242, 187	O		System Bus Address
SMD0 - SMD31	M20, M19, M18, N20, N19, N18, P20, P19, R20, R19, R18, R17, T19, U20, T18, U19, V20, U18, V19, W20, Y20, W19, Y19, W18, V17, Y18, W17, V16, Y17, Y16, U15, V15	47, 118, 181, 46, 117, 180, 45, 116, 44, 115, 178, 233, 114, 42, 177, 113, 41, 176, 112, 40, 39, 111, 38, 110, 174, 37, 109, 173, 36, 35, 229, 172	I/O		System Bus data

1.6 Ethernet Interface

Pin Name	Address No.	Pin No.	I/O	Active Level	Function
MIRCLK	U02	92	I		MII - Receive clock (2.5 MHz/25 MHz)
MIMCLK	Y01	20	O		MII - management clock
MIMD	N02	88	I/O		MII - management
MICOL	V02	93	I		MII - Collision
MICRS	T03	158	I		MII - carrier Sense
MIRDV	R03	157	I		MII - Receive data valid
MIRER	R02	90	I		MII - Receive error
MIRD0 - MIRD3	N03, P01, P02, R01	155, 14, 89, 15	I		MII - Receive data
MITCLK	V01	18	I		MII - Transmit clock (2.5 MHz/25 MHz)
MITE	W02	94	O		MII - Transmit enable
MITER	W01	19	O		MII - Transmit error
MITD0 - MITD3	R04, T01, T02, U01	216, 16, 91, 17	O		MII - Transmit data

1.7 UART and Micro Wire Interface

Pin Name	Address No.	Pin No.	I/O	Active Level	Function
URCLK	B14	133	I		UART external Clock (18.432 MHz)
URSDO	B15	132	O		UART serial data output
URSDI	C15	193	I		UART serial data input
URDTR_B	A15	63	O	L	UART data terminal ready
URRTS_B	D13	248	O	L	UART data request to send
URCTS_B	B13	134	I	L	UART clear to send
URDCD_B	A14	64	I	L	UART data carrier detect
URDSR_B	C13	195	I	L	UART data set ready
MWDI	A12	66	I		Micro Wire data in
MWSK	D12	249	O		Micro Wire sampling clock out
MWCS	B12	135	O		Micro Wire chip select
MWDO	A13	65	O		Micro Wire data out

1.8 USB Interface

Pin Name	Address No.	Pin No.	I/O	Active Level	Function
USBCLK	Y11	30	I		External USB clock (12 MHz)
USBDM	V12	169	I/O		USB data (–)
USBDP	W12	104	I/O		USB data (+)

1.9 Parallel Port Interface

Pin Name	Address No.	Pin No.	I/O	Active Level	Function
GPIO0 - GPIO15	A05, D06, C06, B06, A06, B07, A07, B08, A08, D09, C09, B09, B10, A10, A11, B11	73, 255, 202, 141, 72, 140, 71, 139, 70, 252, 199, 138, 137, 68, 67, 136	I/O		General Purpose Input/Output

1.10 Boundary Scan Interface

Pin Name	Address No.	Pin No.	I/O	Active Level	Function
JCK	V04	161	I		B-SCAN clock
JDI	W04	96	I		B-SCAN input-data
JDO	U05	219	OZ		B-SCAN output-data
JMS	Y03	22	I		B-SCAN mode select
JRSTB_B	Y04	23	I	L	B-SCAN reset

Remark In general all above specified functional pins (and no kind of power supply pins) are included in the boundary scan chain, with the following exceptions: USBDM, USBDP, SDCLK0, SDCLK1
Beside the above specified functional pins, the scan chain includes some of the non-specified test-pins.
The boundary scan device part number is 0503 (hex).

1.11 I.C. - Open

Pin Name	Address No.	Pin No.	I/O	Active Level	Function
IC-Open	A02, C01, D02, D03, E03, E04, F04, J03, J04, U08, W13, Y02, Y10, Y13, Y14	76, 3, 79, 146, 147, 206, 207, 151, 210, 222, 105, 21, 29, 32, 33	O		Test output pins which must be left unconnected

1.12 I.C. - Pull Down

Pin Name	Address No.	Pin No.	I/O	Active Level	Function
IC-PDn	B04, F01, F02, F03, G01, G02, J01, J02, K01, K02, L02, L18, M01, M02, U03, V10, W11, W14, W15, Y06, Y15	143, 6, 81, 148, 7, 82, 9, 84, 10, 85, 86, 182, 12, 87, 159, 167, 103, 106, 107, 25, 34	I		Test input pins which shall be connected to GND

1.13 I.C. - Pull Down with Resistor (50 kΩ)

Pin Name	Address No.	Pin No.	I/O	Active Level	Function
IC-PDnR	B03	144	I/O		Test inputs which shall be connected externally to GND through a resistor

1.14 I.C. - Pull Up

Pin Name	Address No.	Pin No.	I/O	Active Level	Function
IC-PUp	L01, U06, V06, Y05	11, 220, 163, 24	I		Test input pins shall be connected to EVDD

1.15 I.C. - Pull Up with Resistor (50 kΩ)

Pin Name	Address No.	Pin No.	I/O	Active Level	Function
IC-PUpR	A01, B01, B02, C02	1, 2, 77, 78	I/O		Test inputs which shall be connected externally to EVDD through a resistor

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	IV_{DD}	Internal logic core	–0.5 to +3.6	V
	EV_{DD}	I/O buffer	–0.5 to +4.6	V
Input/output voltage	V_{I1}/V_{O1}	LVTTL-level pin	–0.5 to +4.6	V
	V_{I2}/V_{O2}	LVTTL-level MII pin	–0.5 to +4.6	V
	V_{I3}/V_{O3}	USB I/O buffer	–0.5 to +4.6	V
Output current	I_{O1}	LVTTL-level pin, I_{OL} = 9 mA	30	mA
	I_{O2}	LVTTL-level MII pin	30	mA
	I_{O3}	USB I/O buffer, I_{OL} = 18 mA	55	mA
Storage temperature	T_{stg}		–60 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	IV_{DD}		2.3	2.5	2.7	V
	EV_{DD}		3.0	3.3	3.6	V
Low level input voltage	V_{IL1}	LVTTL-level pin	0		0.8	V
	V_{IL2}	LVTTL-level MII pin	0		0.8	V
	V_{IL3}	USB I/O buffer, refer to **(9) USB Interface Parameter** (Single-end operation)			0.8	V
High level input voltage	V_{IH1}	LVTTL-level pin	2.0			V
	V_{IH2}	LVTTL-level MII pin	2.0			V
	V_{IH3}	USB I/O buffer, refer to **(9) USB Interface Parameter** (Single-end operation)	2.0			V
USB differential input voltage	V_{IDF}	USB I/O buffer, refer to **(9) USB Interface Parameter** (Differential operation)	0.2			V
Operating ambient temperature	T_A		0		70	°C

DC Characteristics (IV_{DD} = 2.5 ± 0.2 V, EV_{DD} = 3.3 ± 0.3 V, T_A = 0 to +70°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply current	II_{DD}				550	mA
Supply current	EI_{DD}				100	mA
Input leakage current	I_{LI1}	V_I = EV_{DD} or GND			±10	μA
	I_{LI2}	V_I = EV_{DD} (pin group A)			±1440	μA
	I_{LI3}	V_I = GND (pin group B)			±180	μA
Off state output current	I_{OZ}	V_O = EV_{DD} or GND			±10	μA
Low level output voltage	V_{OL1}	LVTTL-level pin, I_{OL} = 9 mA			0.4	V
★	V_{OL2}	LVTTL-level MII pin, I_{OL} = 9 mA			0.4	V
	V_{OL3}	USB I/O buffer, refer to **(9) USB Interface Parameter**			0.3	V
High level output voltage	V_{OH1}	LVTTL-level pin, I_{OH} = 9 mA	2.4			V
★	V_{OH2}	LVTTL-level MII pin, I_{OH} = 9 mA	2.4			V
	V_{OH3}	USB I/O buffer, refer to **(9) USB Interface Parameter**	2.8		EV_{DD}	V

Capacitance (T_A = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_I	f_C = 1 MHz,	4		8	pF
Output Capacitance	C_O	Unmeasured pins returned to 0 V	4		8	pF
I/O Capacitance	C_{IO}		4		8	pF

Pin Classifications

Caution I/O pins are listed twice - in the input and in the output section !

Input pins

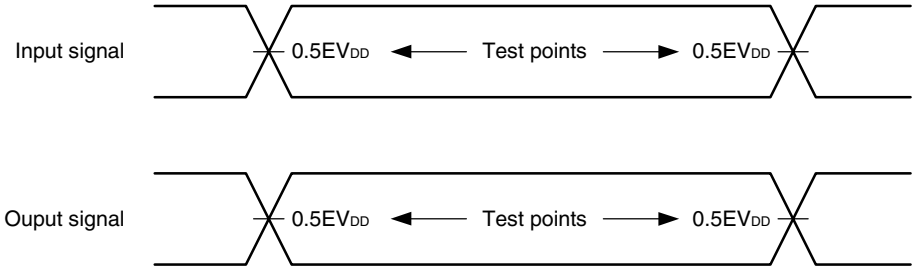
Category		Application Pins	Number of Pins
LVTTL-level pin	V_{I1}, V_{IL1}/V_{IH1}	SCLK, CLKSL, PSTBY, PUSTBY, BIG, ENDCEN, EXINT_B, EXNMI_B, RST_B, RMSL[1:0], SMD[31:0], USBCLK, URCLK, URSDI, MWDI, URCTS_B, URDCD_B, URDSR_B, GPIO[15:0], JCK, JDI, JMS, JRSTB_B	70
LVTTL-level MII pin	V_{I2}, V_{IL2}/V_{IH2}	MIRCLK, MIMD, MICOL, MICRS, MIRDV, MIRER, MIRD[3:0], MITCLK	11
USB I/O buffer	V_{I3}, V_{IL3}/V_{IH3}, V_{IDF}	USBDP, USBDM	2
Pin group A	I_{L2}	IC-PUp (Pin No. 2, 11, 24, 163, 220)	5
Pin group B	I_{L3}	IC-PDn (Pin No. 159)	1

Output pins

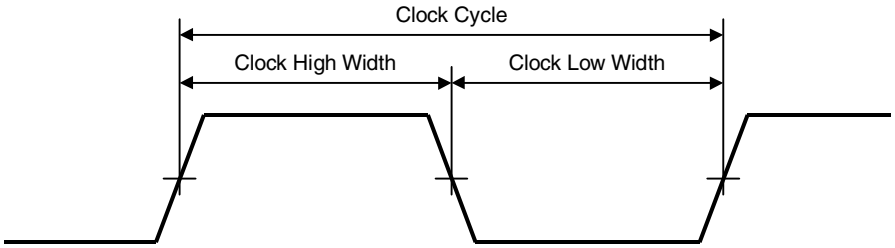
Category			Application Pins	Number of Pins
LVTTL-level pin	I_{O1}	V_{O1}, V_{OL1}/V_{OH1}	SDCLK0, SDCLK1, SDCKE0, SDCKE1, SDCS_B, SDRAS_B, SDCAS_B, SDWE_B, SRMCS_B, SRMOE_B, SEXCS0_B, SEXCS1_B, SEXCS2_B, SMA[20:0], SMD[31:0], URSDO, URDTR_B, URRTS_B, MWSK, MWCS, MWDO, GPIO[15:0], JDO	89
LVTTL-level MII pin	I_{O2}	V_{O2}, V_{OL2}/V_{OH2}	MIMCLK, MIMD, MITE, MITER, MITD[3:0]	8
USB I/O buffer	I_{O3}	V_{O3}, V_{OL3}/V_{OH3}	USBDP, USBDM	2

AC Characteristics (IV_{DD} = 2.5 ± 0.2 V, EV_{DD} = 3.3 ± 0.3 V, T_A = 0 to +70 °C)

(1) AC Test Waveform



(2) Clock Parameter



(2)-1 Clock Input

	Parameter	Symbol	Conditions	MIN.	MAX.	Unit
	SCLK Input Cycle	t_{CYSCK}		30.00	33.00	ns
	SCLK Input High Width	t_{WHSCK}		0.4 × t_{CYSCK}	0.6 × t_{CYSCK}	ns
	SCLK Input Low Width	t_{WLSCK}		0.4 × t_{CYSCK}	0.6 × t_{CYSCK}	ns
	MITCLK Input Cycle	t_{CYMTK}		40.00	400.00	ns
	MITCLK Input High Width	t_{WHMTK}		0.4 × t_{CYMTK}	0.6 × t_{CYMTK}	ns
	MITCLK Input Low Width	t_{WLMTK}		0.4 × t_{CYMTK}	0.6 × t_{CYMTK}	ns
	MIRCLK Input Cycle	t_{CYMRK}		40.00	400.00	ns
	MIRCLK Input High Width	t_{WHMRK}		0.4 × t_{CYMRK}	0.6 × t_{CYMRK}	ns
	MIRCLK Input Low Width	t_{WLMRK}		0.4 × t_{CYMRK}	0.6 × t_{CYMRK}	ns
	USBCLK Input Cycle	t_{CYUBK}		83.12	84.54	ns
	USBCLK Input High Width	t_{WHUBK}		0.4 × t_{CYUBK}	0.6 × t_{CYUBK}	ns
	USBCLK Input Low Width	t_{WLUBK}		0.4 × t_{CYUBK}	0.6 × t_{CYUBK}	ns
★	URCLK Input Cycle	t_{CYURK}		54.25	55.55	ns
★	URCLK Input High Width	t_{WHURK}		0.4 × t_{CYURK}	0.6 × t_{CYURK}	ns
★	URCLK Input Low Width	t_{WLURK}		0.4 × t_{CYURK}	0.6 × t_{CYURK}	ns
	JCK Input Cycle	t_{CYJCK}		100.00	1000.00	ns
	JCK Input High Width	t_{WHJCK}		0.4 × t_{CYJCK}	0.6 × t_{CYJCK}	ns
	JCK Input Low Width	t_{WLJCK}		0.4 × t_{CYJCK}	0.6 × t_{CYJCK}	ns

Remarks 1. For SCLK, USBCLK, usage of a 100 ppm oscillator circuit is recommended.
For MITCLK/MIRCLK the required stability normally depends on the used Ethernet PHY.
In many cases 100 ppm oscillators are recommended.

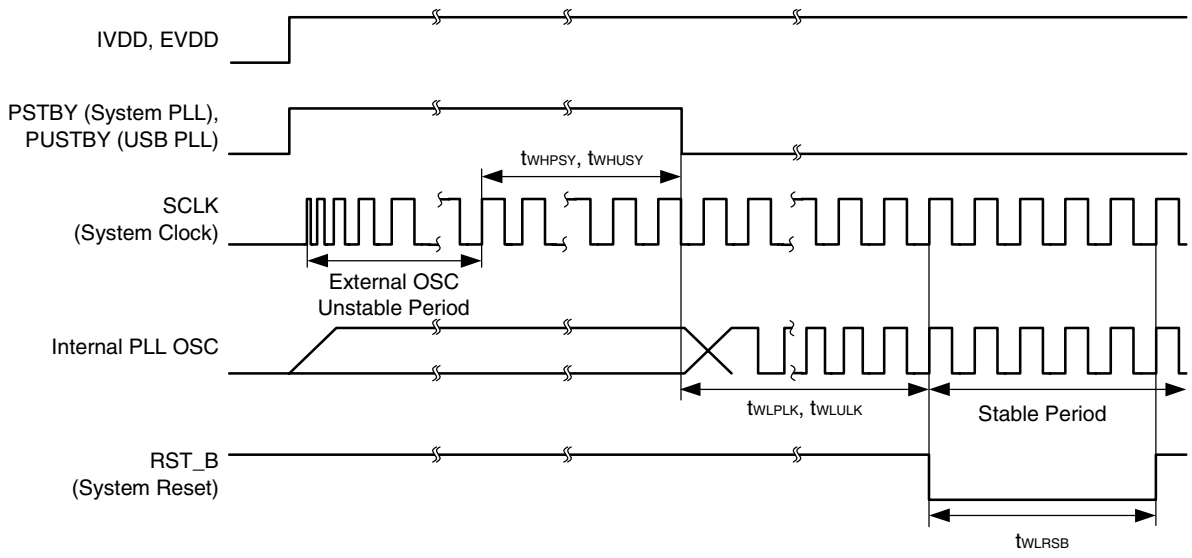
2. The PLL clock input signals (USBCLK and SCLK) shall be derived from a dedicated driving device to ensure short rise and fall times. Normally the clock signals shall not be passed through a resistor.

(2)-2 Clock Output

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SDCLK0 Output Cycle	t_{CYSK0}	Load 30 pF	10.00	15.00	ns
SDCLK0 Output High Width	t_{WHSK0}	Load 30 pF	0.4 × t_{CYSK0}	0.6 × t_{CYSK0}	ns
SDCLK0 Output Low Width	t_{WLSK0}	Load 30 pF	0.4 × t_{CYSK0}	0.6 × t_{CYSK0}	ns
SDCLK1 Output Cycle	t_{CYSK1}	Load 30 pF	10.00	15.00	ns
SDCLK1 Output High Width	t_{WHSK1}	Load 30 pF	0.4 × t_{CYSK1}	0.6 × t_{CYSK1}	ns
SDCLK1 Output Low Width	t_{WLSK1}	Load 30 pF	0.4 × t_{CYSK1}	0.6 × t_{CYSK1}	ns
MIMCLK Output Cycle	t_{CYMCK}	Load 50 pF	420.00		ns
MIMCLK Output High Width	t_{WHMCK}	Load 50 pF	0.4 × t_{CYMCK}		ns
MIMCLK Output Low Width	t_{WLMCK}	Load 50 pF	0.4 × t_{CYMCK}		ns

Remark The value $t_{CYSDCLK}$ which is referenced later on in this document refers to the cycle time of the signals SDCLK0/1 defined in above table.

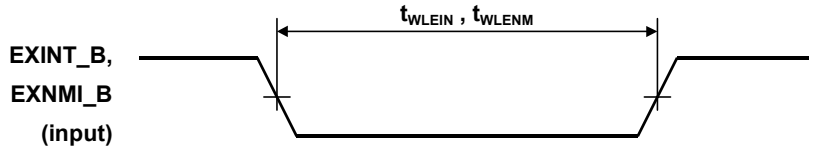
(3) Reset, PLL Parameter



	Parameter	Symbol	Conditions	MIN.	MAX.	Unit
★	RST_B Input Low Level Width	t_{WLRSB}		6 × t_{CYSCK}	4000 **Note**	ns
★	PSTBY Hold High Level Width	t_{WHPSY}		1		μs
★	PSTBY Lookup Time	t_{WLPLK}	Load 50 pF	1000		μs
★	PUSTBY Hold High Level Width	t_{WHUSY}		1		μs
★	PUSTBY Lookup Time	t_{WLULK}	Load 50 pF	1000		μs

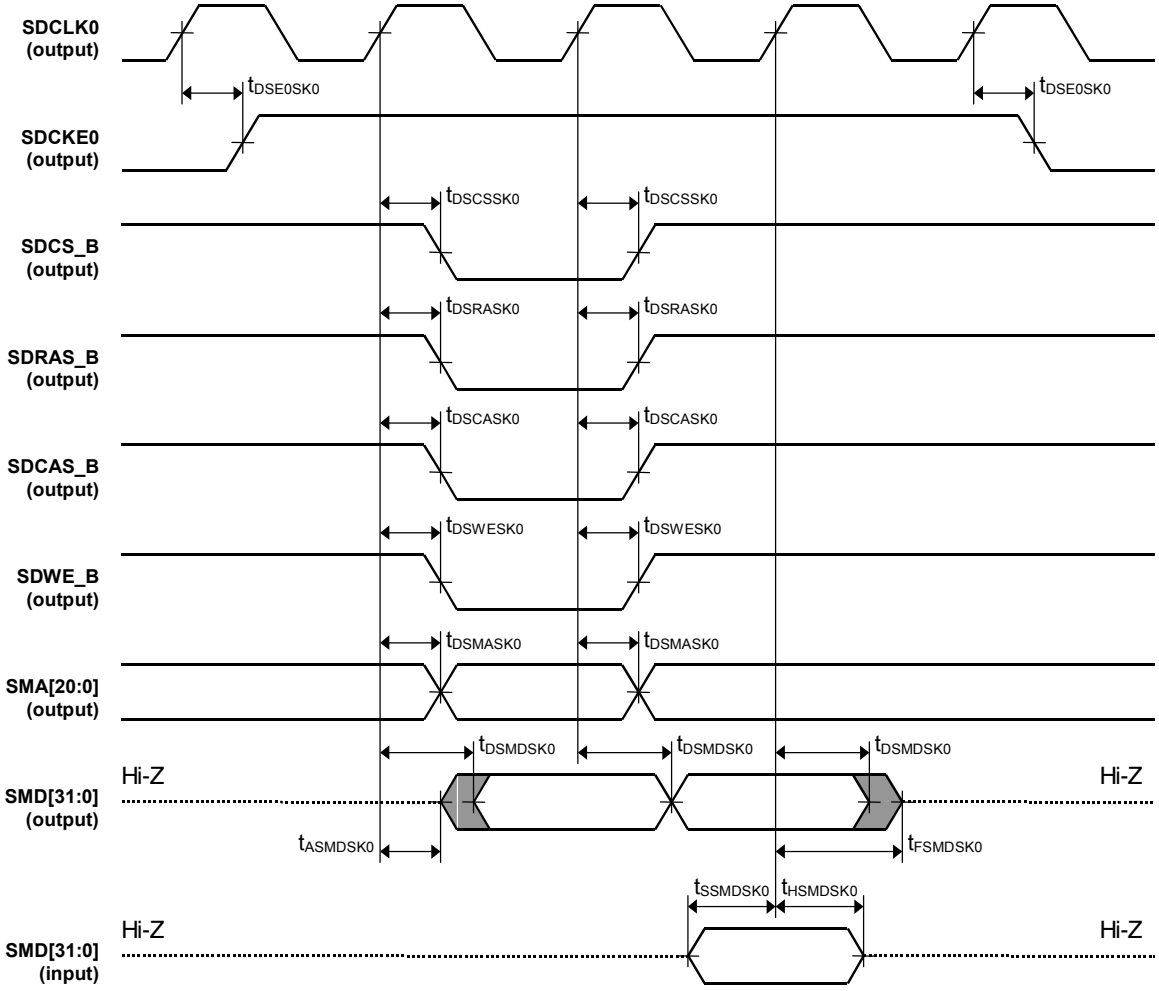
Note If RST_B is applied longer, operation of the μPD98503 will start anyhow. Therefore it shall be made sure, that other logic is also out of RESET state after 4 μs, even if RST_B is applied for longer period.

(4) Interrupt Interface Parameter

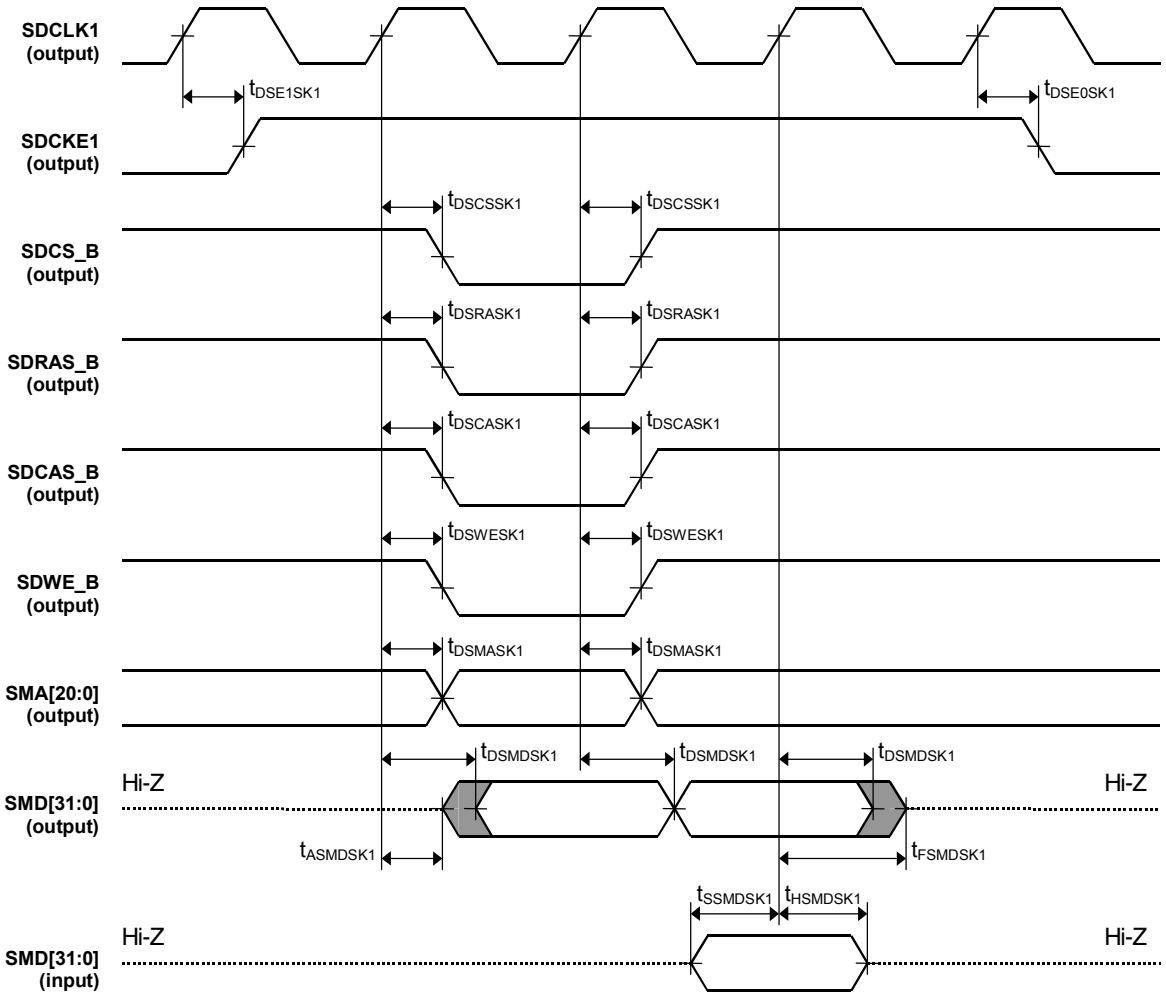


Parameter	Symbol	Conditions	MIN.	MAX.	Unit
EXINT_B Input Low Width	t_{WLEIN}		$4 \times t_{CYSK0/1}$		ns
EXNMI_B Input Low Width	t_{WLENM}		$4 \times t_{CYSK0/1}$		ns

(5) System Bus - SDRAM interface parameter



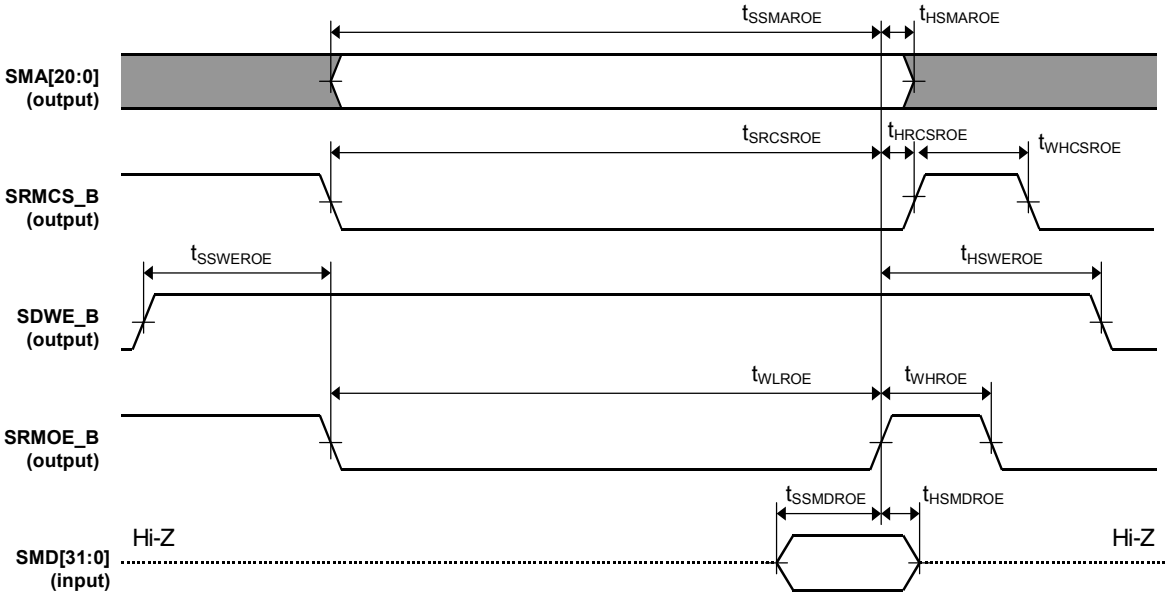
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SDCKE0 Output Delay from SDCLK0	$t_{DSE0SK0}$	Load 30 pF	1.00	8.00	ns
SDCS_B Output Delay from SDCLK0	$t_{DSCSSK0}$	Load 30 pF	1.00	8.00	ns
SDRAS_B Output Delay from SDCLK0	$t_{DSRASK0}$	Load 30 pF	1.00	8.00	ns
SDCAS_B Output Delay from SDCLK0	$t_{DSCASK0}$	Load 30 pF	1.00	8.00	ns
SDWE_B Output Delay from SDCLK0	$t_{DSWESK0}$	Load 30 pF	1.00	8.00	ns
SMA[20:0] Output Delay from SDCLK0	$t_{DSMASK0}$	Load 30 pF	1.00	8.00	ns
SMD[31:0] Output Floating to Active Delay from SDCLK0	$t_{ASMDSK0}$	Load 30 pF	1.00		ns
SMD[31:0] Output Delay from SDCLK0	$t_{DSMDSK0}$	Load 30 pF	1.00	8.00	ns
SMD[31:0] Output Active to Floating Delay from SDCLK0	$t_{FSMDSK0}$	Load 30 pF		8.00	ns
SMD[31:0] Input Setup to SDCLK0	$t_{SSMDSK0}$		4.00		ns
★ SMD[31:0] Input Hold from SDCLK0	$t_{HSMDSK0}$		1.50		ns



Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SDCKE1 Output Delay from SDCLK1	$t_{DSE1SK1}$	Load 30 pF	1.00	8.00	ns
SDCS_B Output Delay from SDCLK1	$t_{DSCSSK1}$	Load 30 pF	1.00	8.00	ns
SDRAS_B Output Delay from SDCLK1	$t_{DSRASK1}$	Load 30 pF	1.00	8.00	ns
SDCAS_B Output Delay from SDCLK1	$t_{DSCASK1}$	Load 30 pF	1.00	8.00	ns
SDWE_B Output Delay from SDCLK1	$t_{DSWESK1}$	Load 30 pF	1.00	8.00	ns
SMA[20:0] Output Delay from SDCLK1	$t_{DSMASK1}$	Load 30 pF	1.00	8.00	ns
SMD[31:0] Output Floating to Active Delay from SDCLK1	$t_{ASMDSK1}$	Load 30 pF	1.00		ns
SMD[31:0] Output Delay from SDCLK1	$t_{DSMDSK1}$	Load 30 pF	1.00	8.00	ns
SMD[31:0] Output Active to Floating Delay from SDCLK1	$t_{FSMDSK1}$	Load 30 pF		8.00	ns
SMD[31:0] Input Setup to SDCLK1	$t_{SSMDSK1}$		4.00		ns
★ SMD[31:0] Input Hold from SDCLK1	$t_{HSMDSK1}$		1.50		ns

(6) System Bus - Flash ROM Interface Parameter

<Read Cycle>



Parameter	Symbol	Condition		MIN.	MAX.	Unit
SMA[20:0] Setup to SRMOE_B	$t_{SSMAROE}$	Load 30 pF		(FAT+1) × $t_{CYSDCLK}$ – 3		ns
SMA[20:0] Hold from SRMOE_B	$t_{HSMAROE}$	Load 30 pF		1 × $t_{CYSDCLK}$ – 3		ns
SRMCS_B Setup to SRMOE_B	$t_{SRCSROE}$	Load 30 pF		(FAT+1) × $t_{CYSDCLK}$ – 2		ns
SRMCS_B Hold from SRMOE_B	$t_{HRCSROE}$	Load 30 pF		–1		ns
SRMCS_B High Pulse Width	$t_{WHCSROE}$	Load 30 pF	**Note 1**	1 × $t_{CYSDCLK}$ – 2		ns
			Note 2	7 × $t_{CYSDCLK}$ – 2		ns
SDWE_B Setup Time to SRMOE_B	$t_{SSWEROE}$	Load 30 pF		2 × $t_{CYSDCLK}$ – 3		ns
★ SDWE_B Hold Time from SRMOE_B	$t_{HSWEROE}$	Load 30 pF		4 × $t_{CYSDCLK}$ – 2		ns
SRMOE_B Low Pulse Width	t_{WLROE}	Load 30 pF		(FAT+1) × $t_{CYSDCLK}$ – 2		ns
SRMOE_B High Pulse Width	t_{WHROE}	Load 30 pF	**Note 1**	1 × $t_{CYSDCLK}$ – 2		ns
			Note 2	7 × $t_{CYSDCLK}$ – 2		ns
SMD[31:0] Setup to SRMOE_B	$t_{SSMDROE}$			11		ns
SMD[31:0] Hold from SRMOE_B	$t_{HSMDROE}$			–1		ns

Notes 1. In case of burst transfers

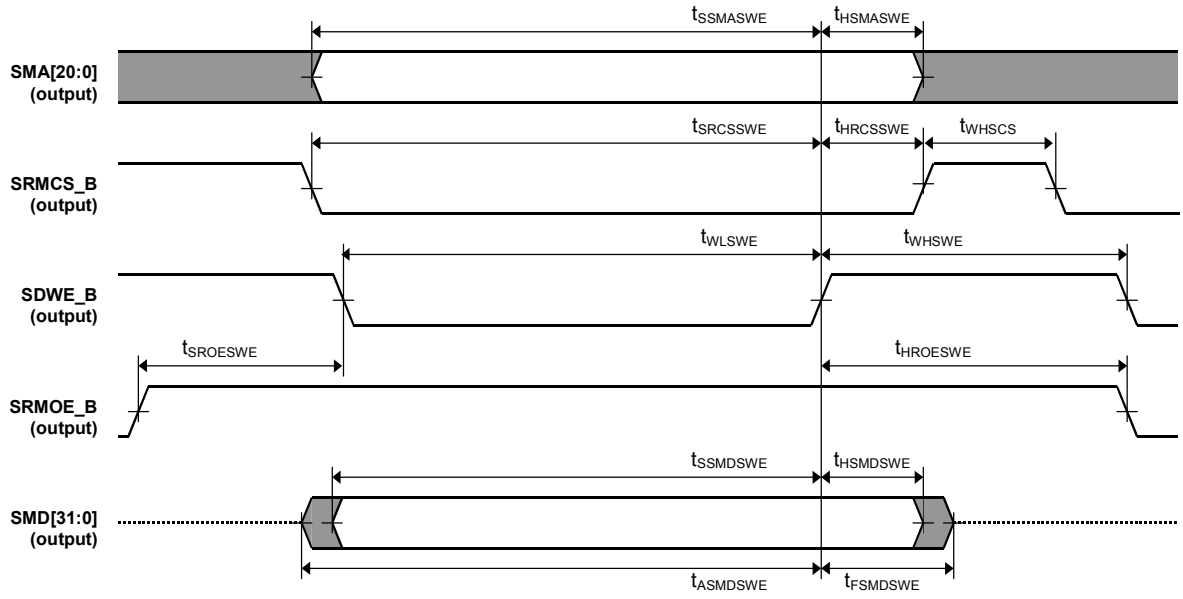
2. In case of subsequent non-burst single word transfers (only possible for 32-bit bus width)

Remarks 1. FAT timing parameter and bus width selection is equivalent for Flash ROM (SRMCS_B area) and IO Bus (SEXCS[2:0]_B area) access.

2. FAT is programmed in register RMATR according the following table.

RMATR[2:0]	FAT
000	18
001	4
010	6
011	8
100	10
101	12
110	14
111	16

<Write Cycle>



	Parameter	Symbol	Condition		MIN.	MAX.	Unit
	SMA[20:0] Setup to SDWE_B	$t_{SSMASWE}$	Load 30 pF		FAT × $t_{CYSDCLK}$ – 2		ns
	SMA[20:0] Hold from SDWE_B	$t_{HSMASWE}$	Load 30 pF		2 × $t_{CYSDCLK}$ – 4		ns
	SRMCS_B Setup to SDWE_B	$t_{SRCSSWE}$	Load 30 pF		FAT × $t_{CYSDCLK}$ – 2		ns
	SRMCS_B Hold from SDWE_B	$t_{HRCSSWE}$	Load 30 pF		1 × $t_{CYSDCLK}$ – 4		ns
	SDMCS_B High Pulse Width	t_{WHSCS}	Load 30 pF		1 × $t_{CYSDCLK}$ – 2 **Note 1**		ns
★	SRMOE_B Setup Time to SDWE_B	$t_{SROESWE}$	Load 30 pF		4 × $t_{CYSDCLK}$ – 2		ns
	SRMOE_B Hold Time from SDWE_B	$t_{HROESWE}$	Load 30 pF		2 × $t_{CYSDCLK}$ – 3		ns
	SDWE_B Low Pulse Width	t_{WLSWE}	Load 30 pF		(FAT–1) × $t_{CYSDCLK}$ – 2		ns
	SDWE_B High Pulse Width	t_{WHSWE}	Load 30 pF	**Note 2**	3 × $t_{CYSDCLK}$ – 2		ns
				Note 3	6 × $t_{CYSDCLK}$ – 2		
	SMD[31:0] Setup to SDWE_B	$t_{SSMDSWE}$	Load 30 pF		FAT × $t_{CYSDCLK}$ – 3		ns
★	SMD[31:0] Hold from SDWE_B	$t_{HSMDSWE}$	Load 30 pF		1 × $t_{CYSDCLK}$ – 5		ns
★	SMD[31:0] Output Hi-Z to Valid Delay	$t_{ASMDSWE}$	Load 30 pF			FAT × $t_{CYSDCLK}$ + 2	ns
★	SMD[31:0] Output Valid to Hi-Z Delay	$t_{FSMDSWE}$	Load 30 pF			1 × $t_{CYSDCLK}$ + 3	ns

Notes 1. To extend this short timing, it is recommended to insert a read access to the RMMDR register after a bus write access, which is directly followed by a bus read access cycle.

2. In case of burst transfers

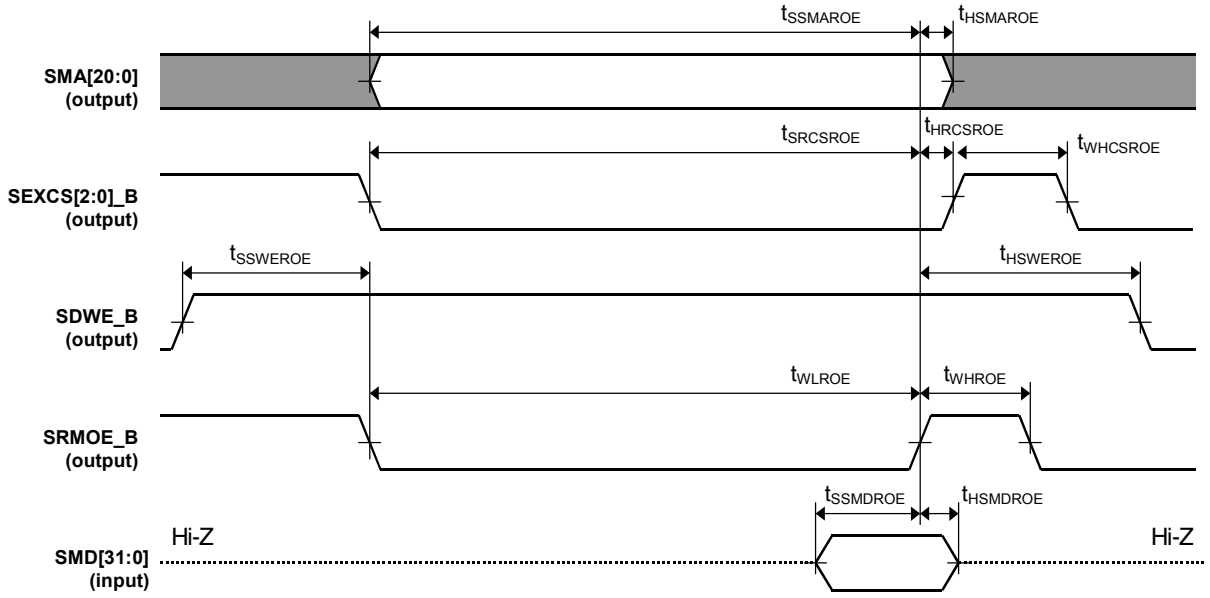
3. In case of subsequent non-burst single word transfers (only possible for 32-bit bus width)

Remark FAT is programmed in register RMATR according the following table.

RMATR[2:0]	FAT
000	18
001	4
010	6
011	8
100	10
101	12
110	14
111	16

(7) System Bus - Extended Chip Select Interface Parameter

<Read Cycle>



Parameter	Symbol	Condition		MIN.	MAX.	Unit
SMA[20:0] Setup to SRMOE_B	$t_{SSMAROE}$	Load 30 pF		(FAT+1) × $t_{CYSDCLK}$ – 3		ns
SMA[20:0] Hold from SRMOE_B	$t_{HSMAROE}$	Load 30 pF		1 × $t_{CYSDCLK}$ – 3		ns
SEXCS[2:0]_B Setup to SRMOE_B	$t_{SRCSROE}$	Load 30 pF		(FAT+1) × $t_{CYSDCLK}$ – 2		ns
SEXCS[2:0]_B Hold from SRMOE_B	$t_{HRCSROE}$	Load 30 pF		–1		ns
SEXCS[2:0]_B High Pulse Width	$t_{WHCSROE}$	Load 30 pF	**Note 1**	1 × $t_{CYSDCLK}$ – 2		ns
			Note 2	7 × $t_{CYSDCLK}$ – 2		ns
SDWE_B Setup Time to SRMOE_B	$t_{SSWEROE}$	Load 30 pF		2 × $t_{CYSDCLK}$ – 3		ns
★ SDWE_B Hold Time from SRMOE_B	$t_{HSWEROE}$	Load 30 pF		4 × $t_{CYSDCLK}$ – 2		ns
SRMOE_B Low Pulse Width	t_{WLROE}	Load 30 pF		(FAT+1) × $t_{CYSDCLK}$ – 2		ns
SRMOE_B High Pulse Width	t_{WHROE}	Load 30 pF	**Note 1**	1 × $t_{CYSDCLK}$ – 2		ns
			Note 2	7 × $t_{CYSDCLK}$ – 2		ns
SMD[31:0] Setup to SRMOE_B	$t_{SSMDROE}$			11		ns
SMD[31:0] Hold from SRMOE_B	$t_{HSMDROE}$			–1		ns

Notes 1. In case of burst transfers

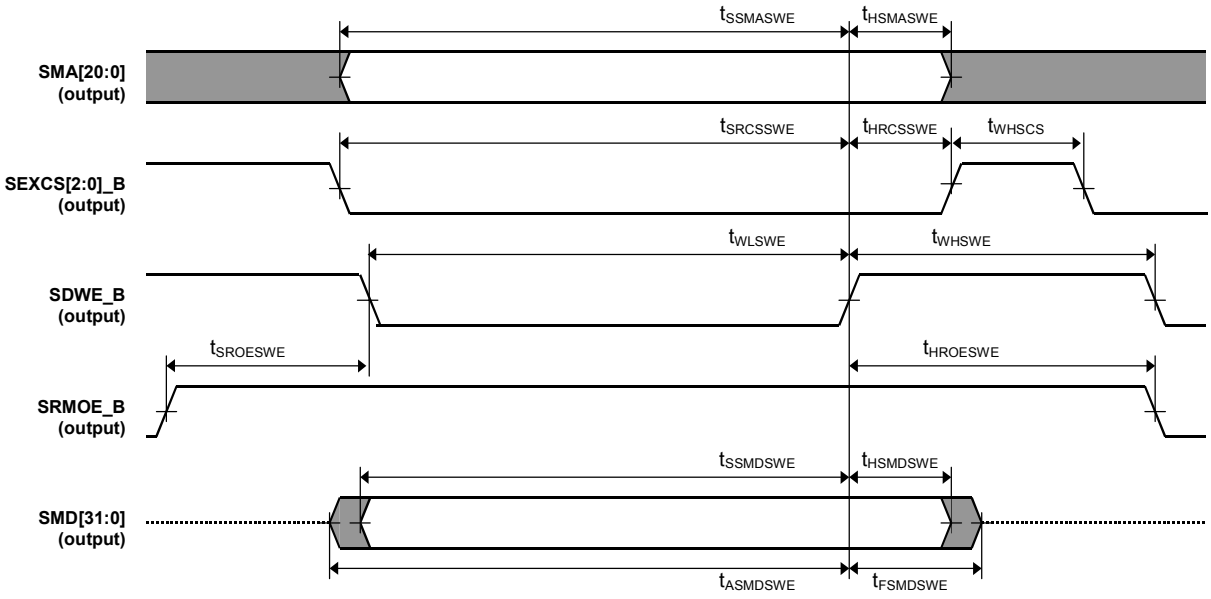
2. In case of subsequent non-burst single word transfers (only possible for 32-bit bus width)

Remarks 1. FAT timing parameter and bus width selection is equivalent for Flash ROM (SRMCS_B area) and IO Bus (SEXCS[2:0]_B area) access.

2. FAT is programmed in register RMATR according the following table.

RMATR[2:0]	FAT
000	18
001	4
010	6
011	8
100	10
101	12
110	14
111	16

<Write Cycle>



	Parameter	Symbol	Condition		MIN.	MAX.	Unit
	SMA[20:0] Setup to SDWE_B	$t_{SSMASWE}$	Load 30 pF		FAT × $t_{CYSDCLK}$ – 2		ns
	SMA[20:0] Hold from SDWE_B	$t_{HSMASWE}$	Load 30 pF		2 × $t_{CYSDCLK}$ – 4		ns
	SEXCS[2:0]_B Setup to SDWE_B	$t_{SRCSSWE}$	Load 30 pF		FAT × $t_{CYSDCLK}$ – 2		ns
★	SEXCS[2:0]_B Hold from SDWE_B	$t_{HRCSSWE}$	Load 30 pF		1 × $t_{CYSDCLK}$ – 4		ns
	SEXCS[2:0]_B High Pulse Width	t_{WHSCS}	Load 30 pF		1 × $t_{CYSDCLK}$ – 2 Note 1		ns
★	SRMOE_B Setup Time to SDWE_B	$t_{SROESWE}$	Load 30 pF		4 × $t_{CYSDCLK}$ – 2		ns
	SRMOE_B Hold Time from SDWE_B	$t_{HROESWE}$	Load 30 pF		2 × $t_{CYSDCLK}$ – 3		ns
	SDWE_B Low Pulse Width	t_{WLSWE}	Load 30 pF		(FAT–1) × $t_{CYSDCLK}$ – 2		ns
	SDWE_B High Pulse Width	t_{WHSWE}	Load 30 pF	**Note 2**	3 × $t_{CYSDCLK}$ – 2		ns
				Note 3	6 × $t_{CYSDCLK}$ – 2		ns
	SMD[31:0] Setup to SDWE_B	$t_{SSMDSWE}$	Load 30 pF		FAT × $t_{CYSDCLK}$ – 3		ns
★	SMD[31:0] Hold from SDWE_B	$t_{HSMDSWE}$	Load 30 pF		1 × $t_{CYSDCLK}$ – 5		ns
★	SMD[31:0] Output Hi-Z to Valid Delay	$t_{ASMDSWE}$	Load 30 pF			FAT × $t_{CYSDCLK}$ + 2	ns
★	SMD[31:0] Output Valid to Hi-Z Delay	$t_{FSMDSWE}$	Load 30 pF			1 × $t_{CYSDCLK}$ + 3	ns

Notes 1. To extend this short timing, it is recommended to insert a read access to the RMMDR register after a bus write access, which is directly followed by a bus read access cycle.

2. In case of burst transfers

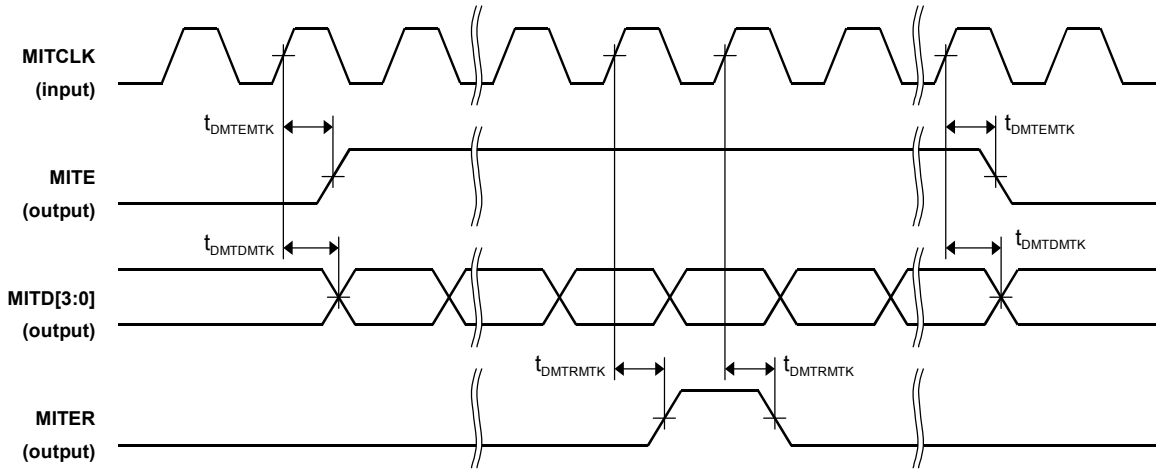
3. In case of subsequent non-burst single word transfers (only possible for 32-bit bus width)

Remark FAT is programmed in register RMATR according the following table.

RMATR[2:0]	FAT
000	18
001	4
010	6
011	8
100	10
101	12
110	14
111	16

(8) Ethernet Interface Parameter

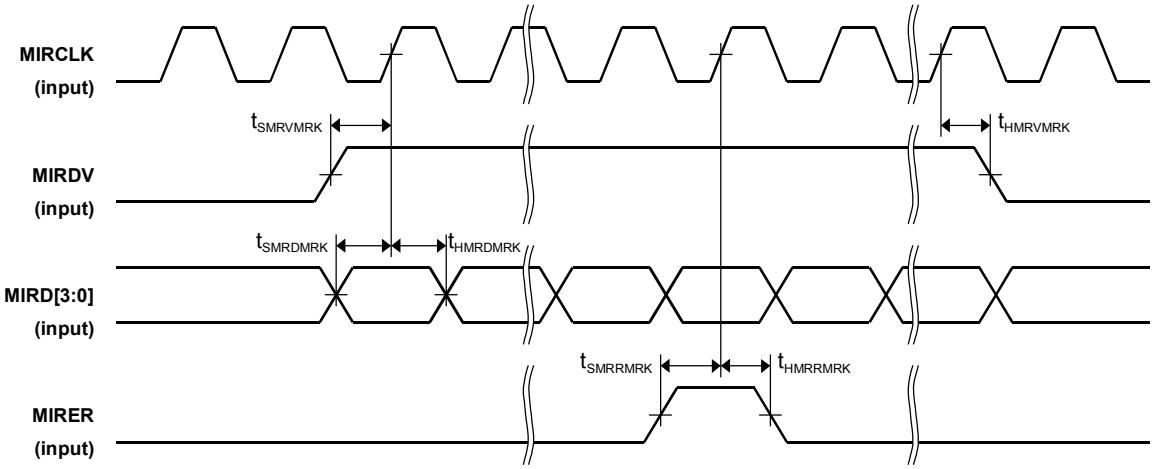
<MII Data Transmission>



Parameter	Symbol	Conditions	MIN.	MAX.	Unit
MITE Output Delay	$t_{DMTEMTK}$	Load 50 pF	0	20 Note	ns
MITD[3:0] Output Delay	$t_{DMTDMTK}$	Load 50 pF	0	20 Note	ns
MITER Output Delay	$t_{DMTRMTK}$	Load 50 pF	0	20 Note	ns

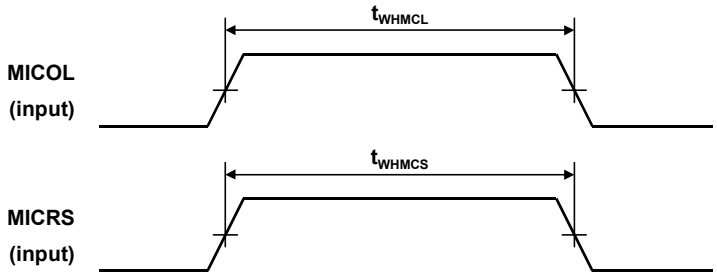
Note In MII Spec., Maximum output delay is specified as 25 ns.

<MII Data Reception>



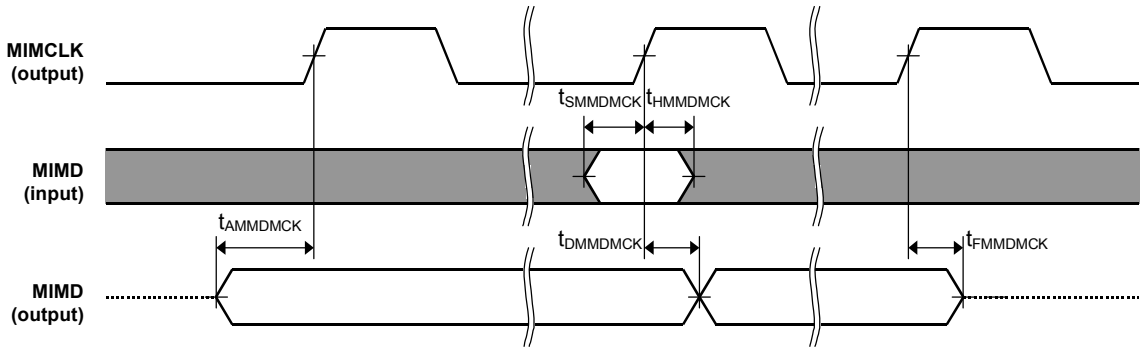
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
MIRDV Setup Time	$t_{SMRVMRK}$		10		ns
MIRDV Hold Time	$t_{HMRVMRK}$		10		ns
MIRD[3:0] Setup Time	$t_{SMRDMRK}$		10		ns
MIRD[3:0] Hold Time	$t_{HMRDMRK}$		10		ns
MIRER Setup Time	$t_{SMRRMRK}$		10		ns
MIRER Hold Time	$t_{HMRRMRK}$		10		ns

<MII Interface Signals>



Parameter	Symbol	Conditions	MIN.	MAX.	Unit
MICOL High Pulse Width	t_{WHMCL}		$2 \times t_{CYMTK}$		ns
MICRS High Pulse Width	t_{WHMCS}		$2 \times t_{CYMTK}$		ns

<MII Management Interface>

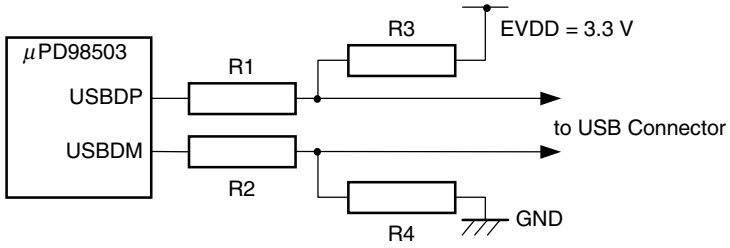


	Parameter	Symbol	Condition	MIN.	MAX.	Unit
	MIMD Setup to MIMCLK	$t_{SMMDMCK}$		30		ns
	MIMD Hold from MIMCLK	$t_{HMMDMCK}$		0		ns
★	MIMD Active Delay from MIMCLK	$t_{AMMDMCK}$	Load 50 pF	10		ns
	MIMD Output Delay from MIMCLK	$t_{DMMDMCK}$	Load 50 pF	10	20	ns
★	MIMD Floating Delay from MIMCLK	$t_{FMMDMCK}$	Load 50 pF		20	ns

(9) USB Interface Parameter

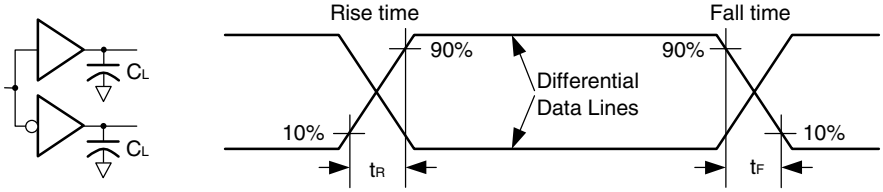
External Circuitry

The USB line output signals (refer to **chapter 1.8 USB interface**) need 4 external resistors to adjust the output impedance (R1 and R2 = 22 Ω each), to code the full speed USB mode (R3 = 1.5 kΩ) and to protect the output driver of the USBDM pin (R4 = 51 kΩ). The following figure shows a typical connection diagram.

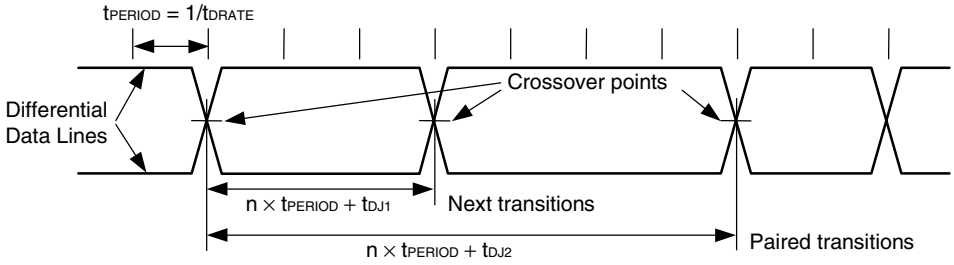


Parameter: USBDM, USBDP

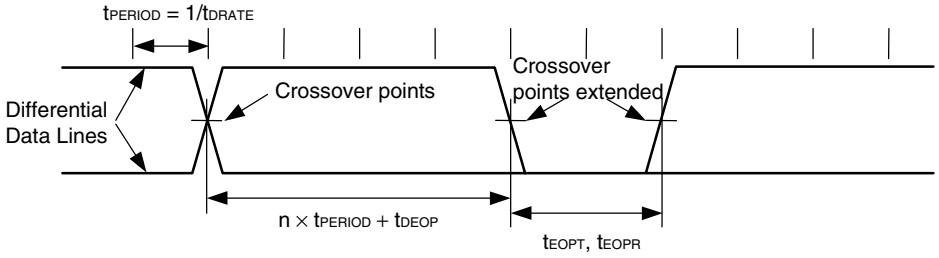
<Data Signal Rise and Fall>



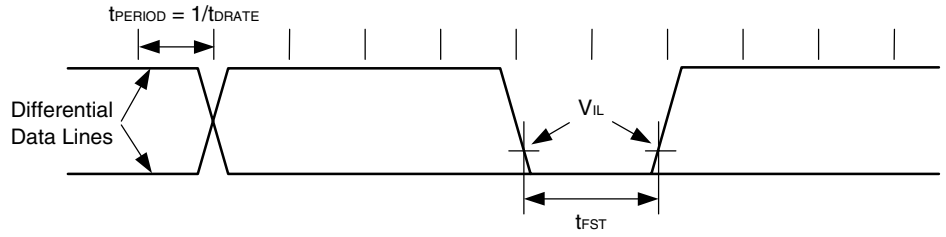
<Differential Data Jitter>



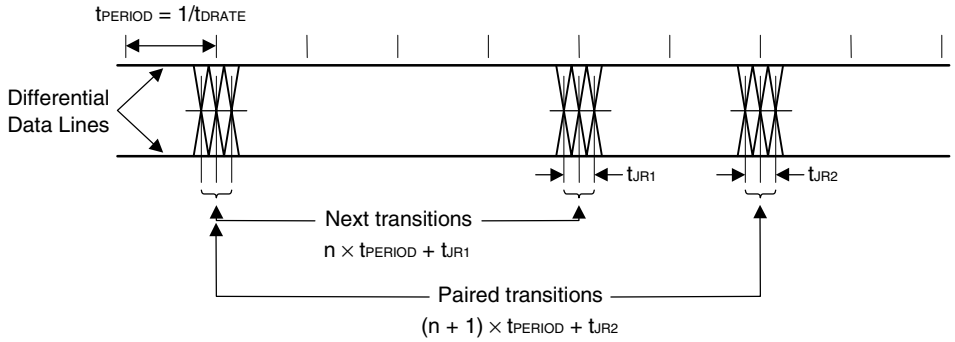
<Differential-to-EOP Transition Skew and EOP Width>



<Differential Transition Interval Width>

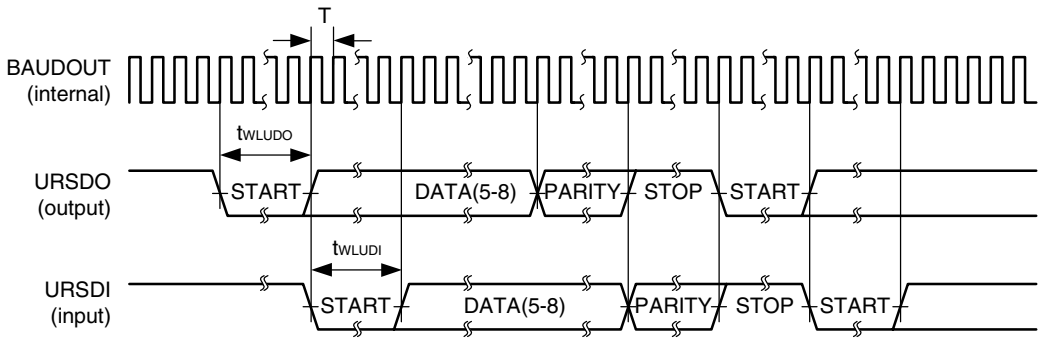


<Receiver Jitter Tolerance>



	Parameter	Symbol	Condition	MIN.	MAX.	Unit
★	Rise Time	t_R		0.4	20	ns
★	Fall Time	t_F		0.4	20	ns
	Differential Rise and Fall Time Matching	t_{FRFM}	t_R/t_F	90	111.11	%
	Full-speed Data Rate	t_{DRATE}		11.9700	12.0300	Mbps
	Source Jitter Total (including frequency tolerance):					ns
	To Next Transition	t_{DJ1}		−3.5	+3.5	
	For Paired Transitions	t_{DJ2}		−4	+4	
	Source Jitter for Differential Transition to SE0 Transition	t_{DEOP}		−2	+5	ns
	Receiver Jitter:					ns
	To Next Transition	t_{JR1}		−18.5	+18.5	
	For Paired Transitions	t_{JR2}		−9	+9	
	Source SE0 interval of EOP	t_{EOPT}		160	175	ns
	Receiver SE0 interval of EOP	t_{EOPR}		82		ns
	Width of SE0 interval during differential transition	t_{FST}			14	ns

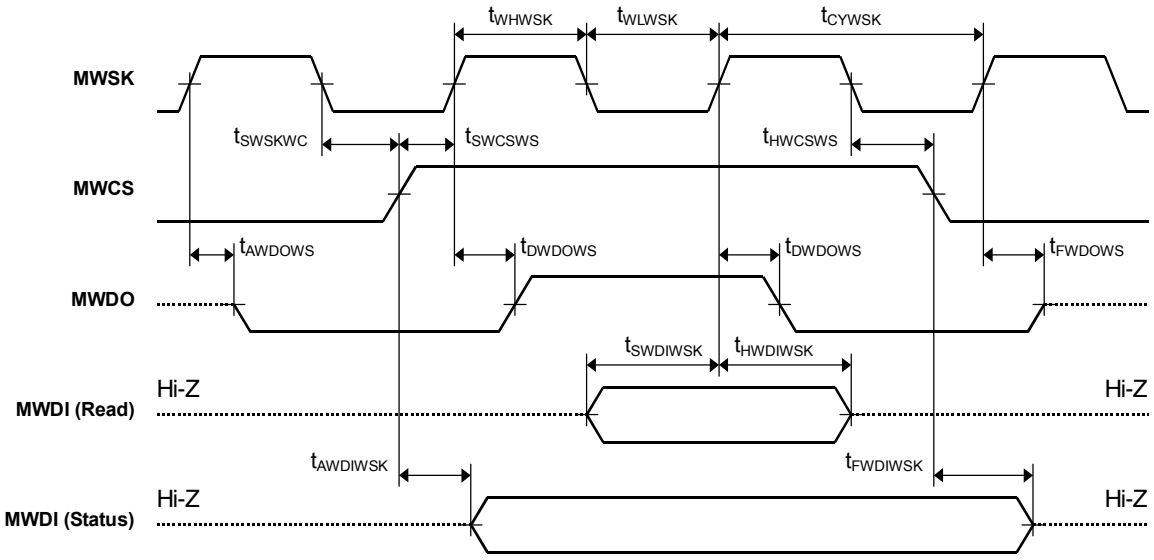
(10) UART Interface Parameter



Remark The BAUDOUT is equal to the 16X of transmisson baud rate (1/T = 16 × Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

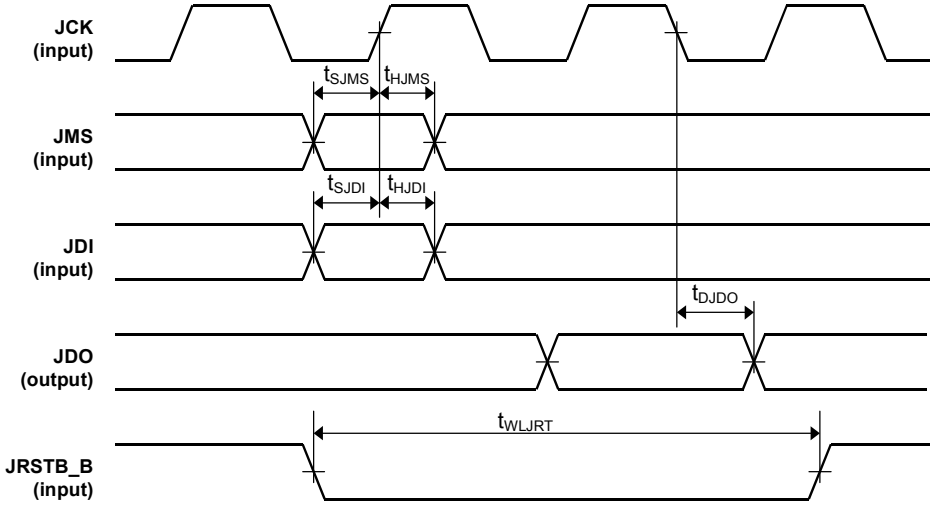
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
URCLK input frequency	f_{CYUCK}			18.432	MHz
URSDO low level width	t_{WLUDO}		16 × T		ns
URSDI low level width	t_{WLUDI}		16 × T		ns

(11) Micro Wire Interface Parameter



Parameter	Symbol	Conditions	MIN.	MAX.	Unit
MWSK Clock Frequency	t_{CYWSK}	Load 50 pF	400 × t_{CYSK0}		ns
MWSK High Time	t_{WHWSK}	Load 50 pF	190 × t_{CYSK0}		ns
MWSK Low Time	t_{WLWSK}	Load 50 pF	190 × t_{CYSK0}		ns
MWSK Setup to MWCS	$t_{SWSKWCS}$	Load 50 pF	90 × t_{CYSK0}		ns
MWCS Setup to MWSK	$t_{SWCSWSK}$	Load 50 pF	90 × t_{CYSK0}		ns
MWCS Hold from MWSK	$t_{HWCSWSK}$	Load 50 pF	90 × t_{CYSK0}		ns
MWDO Output Active to Floating Delay from MWSK	$t_{AWDOWSK}$	Load 50 pF	190 × t_{CYSK0}		ns
MWDO Output Delay from MWSK	$t_{DWDOWSK}$	Load 50 pF	190 × t_{CYSK0}		ns
MWDO Output Floating to Active Delay from MWSK	$t_{FWDOWSK}$	Load 50 pF	190 × t_{CYSK0}		ns
MWDI Setup to MWSK	$t_{SWDIWSK}$		10 × t_{CYSK0}		ns
MWDI Hold from MWSK	$t_{HWDIWSK}$		10 × t_{CYSK0}		ns
MWCS to Status Time from MWSK	$t_{AWDIWSK}$			100 × t_{CYSK0}	ns
MWCS to MWDO in 3-State	$t_{FWDIWSK}$			40 × t_{CYSK0}	ns

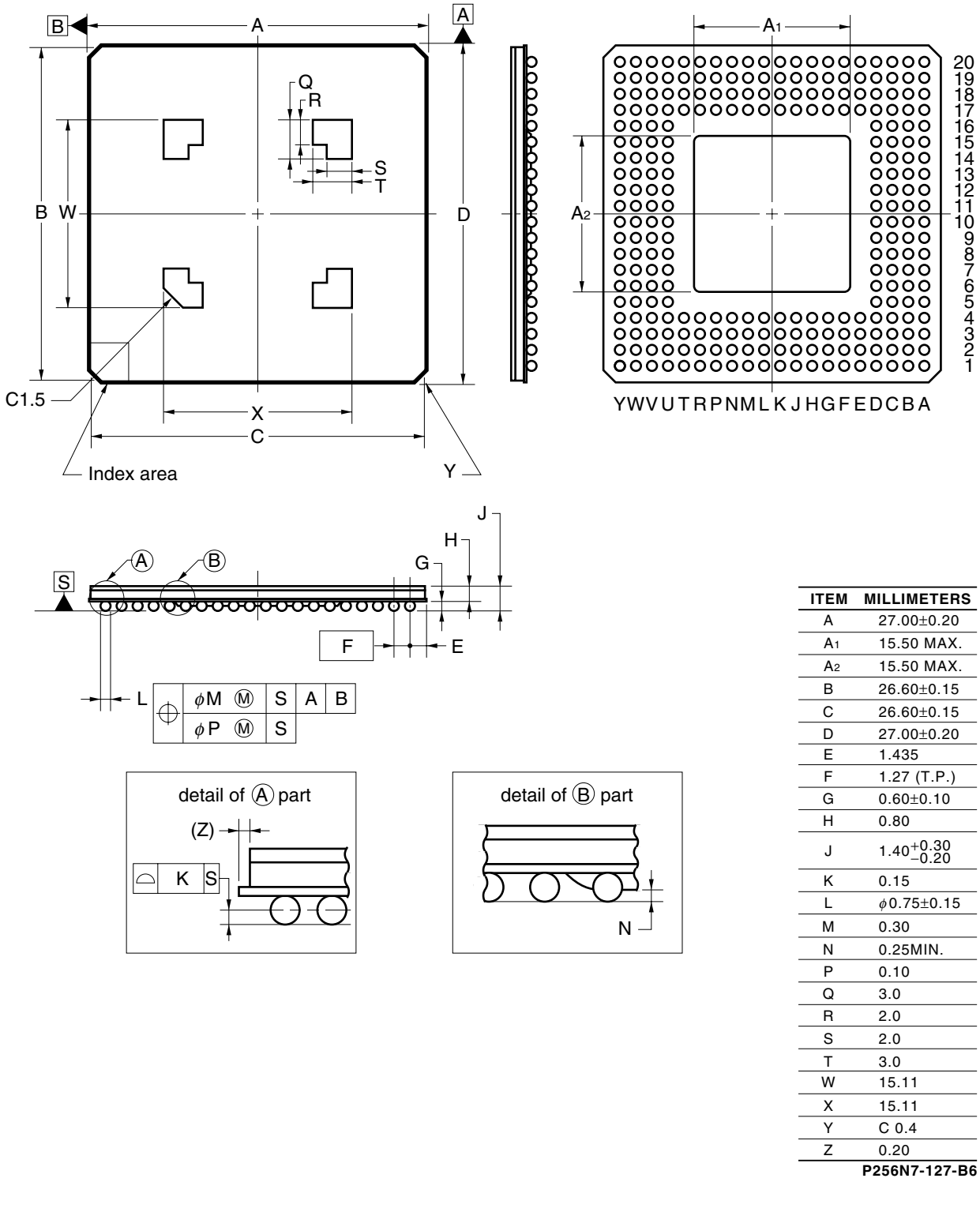
(12) JTAG Boundary-Scan



	Parameter	Symbol	Conditions	MIN.	MAX.	Unit
	JMS Setup Time	t_{SJMS}		10		ns
	JMS Hold Time	t_{HJMS}		10		ns
	JDI Setup Time	t_{SJDI}		10		ns
★	JDI Hold Time	t_{HJDI}		12		ns
	JDO Output Delay	t_{DJDO}	Load 50 pF		20	ns
	JRSTB_B Low Pulse Width	t_{WLJRT}		$5 \times t_{CYJCK}$		ns

3. PACKAGE DRAWING

256-PIN TAPE BGA (HEAT SPREADER TYPE) (27x27)



ITEM	MILLIMETERS
A	27.00±0.20
A_1	15.50 MAX.
A_2	15.50 MAX.
B	26.60±0.15
C	26.60±0.15
D	27.00±0.20
E	1.435
F	1.27 (T.P.)
G	0.60±0.10
H	0.80
J	$1.40^{+0.30}_{-0.20}$
K	0.15
L	φ0.75±0.15
M	0.30
N	0.25MIN.
P	0.10
Q	3.0
R	2.0
S	2.0
T	3.0
W	15.11
X	15.11
Y	C 0.4
Z	0.20

P256N7-127-B6

4. RECOMMENDED SOLDERING CONDITIONS

The μPD98503 should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC Electronics sales representative.

Table 4-1. Surface Mounting Type Soldering Conditions

• μPD98503N7-B6: 256-pin tape BGA (heat spreader type) (27 × 27)

Method	Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher), Count: three times or less, Exposure limit: 7 days Note (after that, prebake at 125°C for 10 hours)	IR35-107-3
VPS	Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher), Count: three times or less, Exposure limit: 7 days Note (after that, prebake at 125°C for 10 hours)	VP15-107-3

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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