NEC

MOS INTEGRATED CIRCUIT

μPD98501

NETWORK CONTROLLER

The μPD98501 is a high performance controller which can perform the protocol conversion between IP packets and ATM cells, which is especially suitable for ADSL modem. It includes high performance MIPS™ based 64-bit RISC processor VR4120A™ CPU core, ATM cell processor, Ethernet™ controller, USB controller block, UTOPIA2 interface and SDRAM interface.

Detailed function descriptions are provided in the following user's manual. Be sure to read the manual before designing.
μPD98501 User's Manual: S14767E

FEATURES

- Includes high performance MIPS based 64-bit RISC processor VR4120A
- Can perform RTOS and network middleware (M/W) on the chip
- Includes interface for PROM and flash ROM used for storing boot program
- Includes 32-bit RISC controller, as ATM cell processor
- Software SAR processing by RISC controller affords flexibility for specification update
- Supports CBR/VBR/UBR service classes
- Includes 2-channel 10/100 Mbps Ethernet controllers compliant to IEEE802.3, IEEE802.3u and IEEE802.3x
- Can directly connect external Ethernet PHY device through 3.3-V MII interface
- Includes USB full speed function controller compliant to USB specification 1.1
- Supports operation conforming to the USB Communication Device Class Specification
- Can directly connect 64M-bit and 128M-bit SDRAM as external memory
- Includes 8-bit 33 MHz UTOPIA level 2 interface compliant to ATM Forum af-phy-0039
- Includes boundary scan function (JTAG) compliant to IEEE 1149.1
- Includes Micro Wire™ interface
- Includes 2-channel general purpose timers
- Using advanced CMOS technology
- Power supply voltage: 3.3 V (I/O), 2.5 V (Core)
- Package 352-pin T-BGA

ORDERING INFORMATION

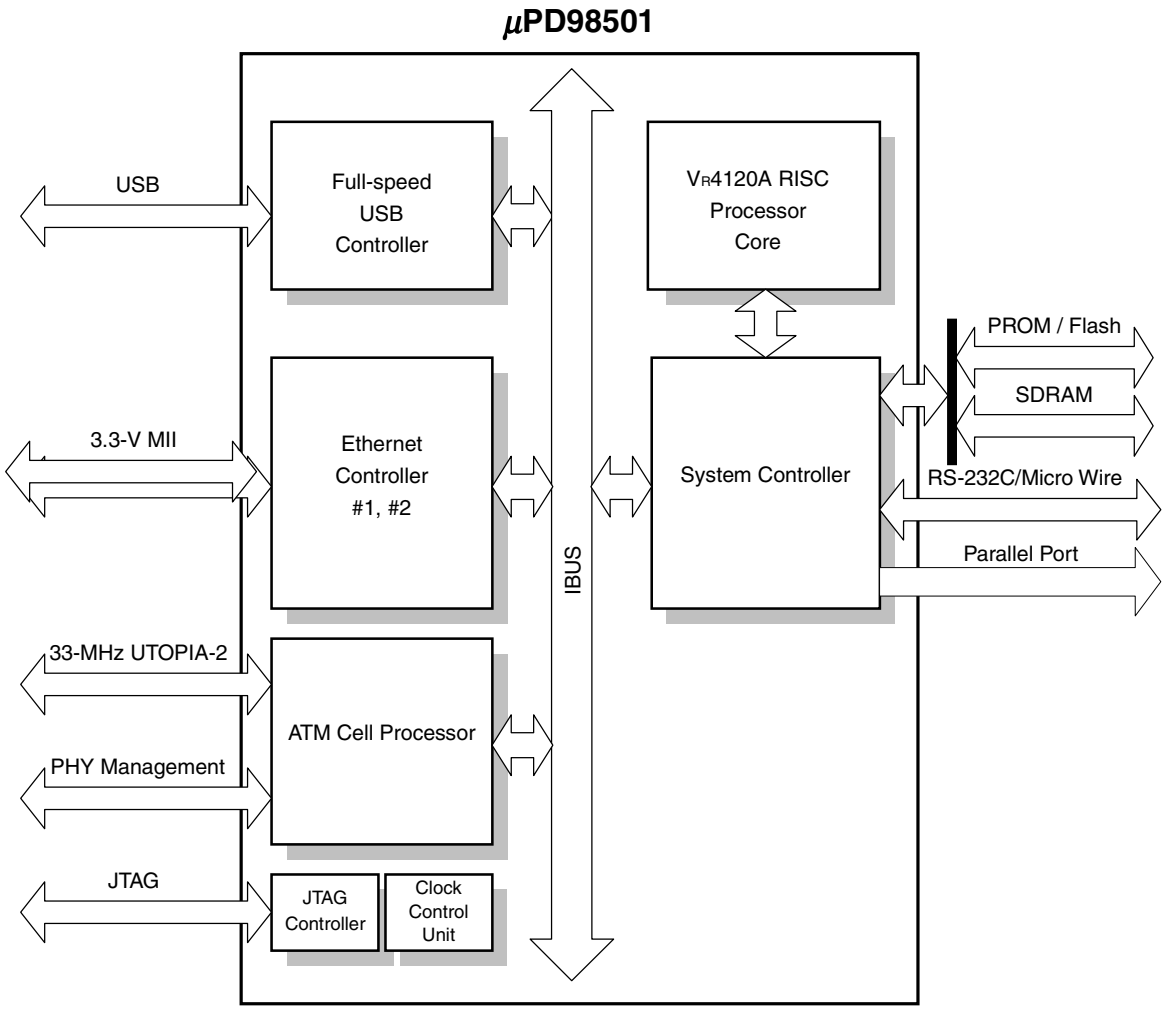
Part Number	Package
μPD98501N7-F6	352-pin tape BGA (heat spreader type) (35 × 35)

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

Document No. S14828EJ5V0DS00 (5th edition)
Date Published August 2002 NS CP (K)
Printed in Japan

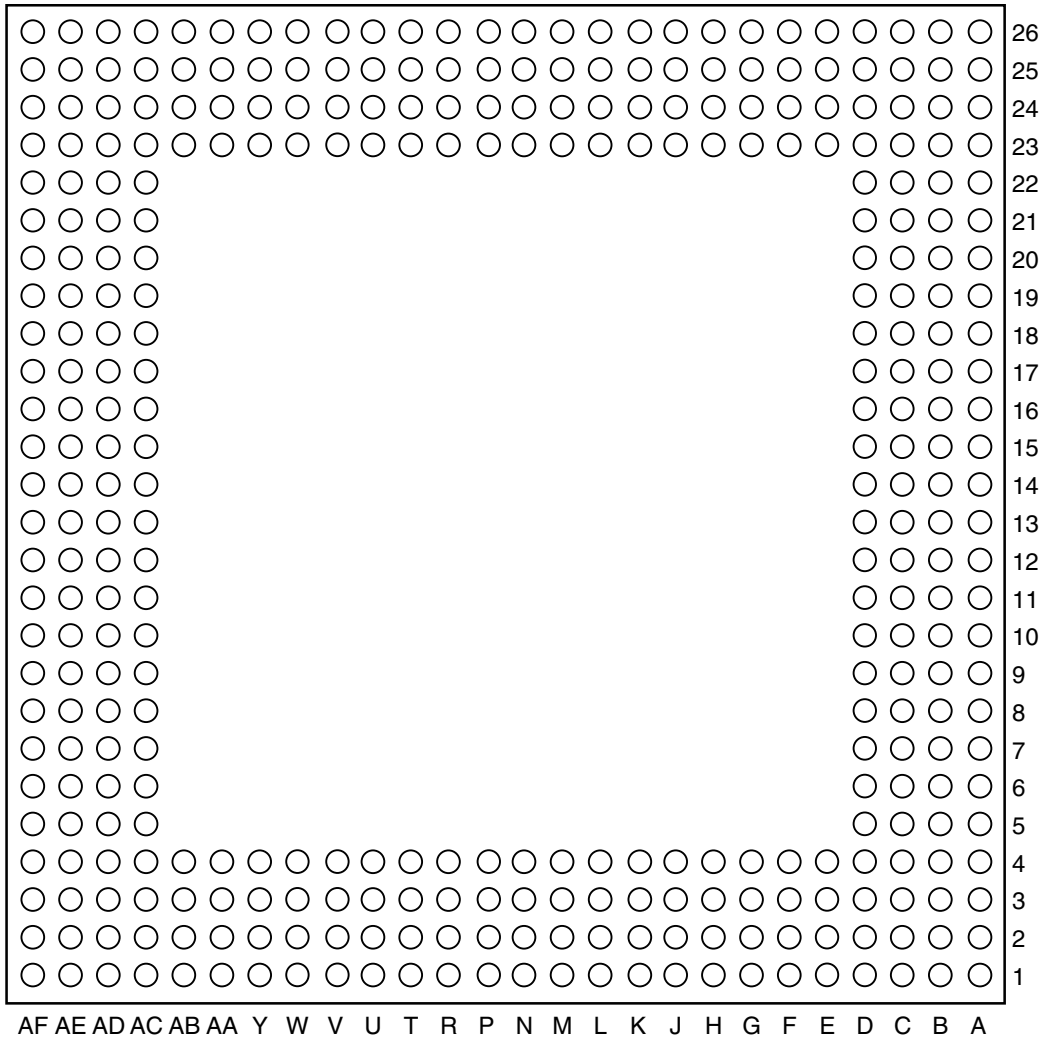
The mark ★ shows major revised points.

BLOCK DIAGRAM



PIN CONFIGURATION (Bottom View)

- **352-pin tape BGA (head spreader type) (35 × 35)**
  μPD98501N7-F6



Pin Name

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A01	IC-Open	C01	SCLK	E01	EVDD	L23	UMD0	V01	SMA6
A02	IVDD	C02	CLKSL	E02	PSDVD	L24	IC-PUp	V02	SMA5
A03	GND	C03	IC-PDn	E03	PSAGND	L25	GND	V03	IVDD
A04	PUAGND	C04	PUMD_B	E04	GND	L26	IVDD	V04	GND
A05	GND	C05	PUAVD	E23	IVDD	M01	SMD16	V23	MI2RD1
A06	EVDD	C06	IC-PDn	E24	UMAD4	M02	SMD17	V24	MI2RD0
A07	EVDD	C07	IC-PDn	E25	UMAD2	M03	IVDD	V25	MI2MD
A08	IC-PUpR	C08	USBDP	E26	EVDD	M04	GND	V26	MI2RDV
A09	IC-Open	C09	IC-PDnR	F01	SRMCS_B	M23	IC-PUpR	W01	SMA4
A10	IVDD	C10	IVDD	F02	SRMOE_B	M24	IC-PUpR	W02	SMA3
A11	IVDD	C11	UDRCLV	F03	PSTBY	M25	IC-PUpR	W03	GND
A12	EVDD	C12	UDRD6	F04	PSMD_B	M26	IC-PUpR	W04	SMA2
A13	UDRD1	C13	UDRD3	F23	UMAD1	N01	SMA19	W23	IVDD
A14	IVDD	C14	UDRD0	F24	UMAD0	N02	SMA20	W24	MI2MCLK
A15	UDRAD3	C15	UDRCLK	F25	IC-PUpR	N03	GND	W25	MI2RD3
A16	UDRAD0	C16	GND	F26	IC-PUpR	N04	EVDD	W26	MI2RD2
A17	UDTE_B	C17	UDTAD4	G01	SMD30	N23	IC-PUpR	Y01	SMA1
A18	UDTAD3	C18	UDTAD1	G02	SMD31	N24	IC-PUpR	Y02	EVDD
A19	GND	C19	UDTD7	G03	IVDD	N25	IC-PUpR	Y03	SMA0
A20	UDTD5	C20	UDTD4	G04	GND	N26	IC-PUpR	Y04	SDCKE1
A21	UDTCLK	C21	IVDD	G23	IC-PUpR	P01	SMA18	Y23	GND
A22	UMRST_B	C22	UMRDY_B	G24	IC-PUpR	P02	SMA17	Y24	IC-PDnR
A23	UDTD0	C23	UMRD_B	G25	IC-PUpR	P03	SMA16	Y25	IC-PDnR
A24	UMINT_B	C24	EVDD	G26	IC-PUpR	P04	SMA15	Y26	GND
A25	UMAD11	C25	UMAD7	H01	SMD27	P23	MI2TD1	AA01	IVDD
A26	UMMD	C26	GND	H02	GND	P24	MI2TD0	AA02	GND
B01	IC-PDn	D01	PSAVD	H03	SMD28	P25	IVDD	AA03	SDCLK1
B02	IC-Open	D02	PSDGND	H04	SMD29	P26	GND	AA04	SDCS_B
B03	IC-Open	D03	GND	H23	IC-PUpR	R01	SMA14	AA23	EVDD
B04	PUDVD	D04	IC-PDn	H24	IC-PUpR	R02	EVDD	AA24	MITD1
B05	PUDGND	D05	USBCLK	H25	UMD7	R03	SMA13	AA25	MITD0
B06	PUSTBY	D06	IC-PDn	H26	GND	R04	SMA12	AA26	IVDD
B07	GND	D07	IC-Open	J01	IVDD	R23	MI2TCLK	AB01	SDRAS_B
B08	EVDD	D08	USBDM	J02	GND	R24	MI2COL	AB02	SDCAS_B
B09	IC-Open	D09	IC-PDnR	J03	SMD25	R25	MI2TD3	AB03	EVDD
B10	GND	D10	GND	J04	SMD26	R26	MI2TD2	AB04	SDCLK0
B11	UDRSC	D11	UDRE_B	J23	IVDD	T01	SMA11	AB23	GND
B12	UDRD5	D12	UDRD7	J24	UMD6	T02	IVDD	AB24	MICRS
B13	UDRD2	D13	UDRD4	J25	UMD5	T03	GND	AB25	MITD3
B14	GND	D14	UDRAD4	J26	UMD4	T04	SMA10	AB26	MITD2
B15	UDRAD2	D15	UDRAD1	K01	SMD22	T23	MI2TER	AC01	SDWE_B
B16	IVDD	D16	UDTCLV	K02	SMD23	T24	MI2CRS	AC02	SDCKE0
B17	UDTSC	D17	EVDD	K03	EVDD	T25	IVDD	AC03	SMD15
B18	UDTAD2	D18	IVDD	K04	SMD24	T26	GND	AC04	SMD10
B19	UDTAD0	D19	UDTD6	K23	UMD3	U01	SMA9	AC05	SMD6
B20	EVDD	D20	UDTD3	K24	EVDD	U02	SMA8	AC06	EVDD
B21	UDTD2	D21	GND	K25	UMD2	U03	SMA7	AC07	SMD1
B22	UDTD1	D22	GND	K26	UMD1	U04	EVDD	AC08	EXNMI_B
B23	UMSL_B	D23	UMAD10	L01	SMD18	U23	MI2TE	AC09	POM5
B24	UMWR_B	D24	UMAD6	L02	SMD19	U24	MI2RCLK	AC10	POM2
B25	UMAD9	D25	UMAD5	L03	SMD20	U25	EVDD	AC11	POM0
B26	UMAD8	D26	UMAD3	L04	SMD21	U26	MI2RER	AC12	URSDI

Pin No.	Pin Name
AC13	EVDD
AC14	IC-Open
AC15	EVDD
AC16	GND
AC17	IC-PUpR
AC18	JRSTB_B
AC19	JDO
AC20	IC-PDn
AC21	ROMSEL0
AC22	MIRD2
AC23	GND
AC24	MITER
AC25	MITCLK
AC26	MICOL
AD01	GND
AD02	SMD11
AD03	SMD14
AD04	SMD8
AD05	GND
AD06	SMD4
AD07	IVDD
AD08	EXINT_B
AD09	POM7

Pin No.	Pin Name
AD10	IVDD
AD11	URCLK
AD12	URDSR_B/MWDO
AD13	URRTS_B/MWDI
AD14	IVDD
AD15	IC-Open
AD16	IC-PDn
AD17	IC-Open
AD18	IC-Open
AD19	JMS
AD20	EVDD
AD21	ROMSEL1
AD22	MIMCLK
AD23	MIRD0
AD24	MIMD
AD25	MIRER
AD26	IVDD
AE01	IVDD
AE02	GND
AE03	EVDD
AE04	SMD9
AE05	SMD3
AE06	SMD2

Pin No.	Pin Name
AE07	GND
AE08	ENDCEN
AE09	POM6
AE10	POM3
AE11	GND
AE12	URDCD_B/MWCS
AE13	URDTR_B
AE14	GND
AE15	IC-Open
AE16	IC-PUpR
AE17	IC-PUpR
AE18	BIG
AE19	IVDD
AE20	JCK
AE21	IC-PDn
AE22	IC-PDn
AE23	MIRD3
AE24	IVDD
AE25	MIRCLK
AE26	MITE
AF01	GND
AF02	SMD13
AF03	SMD12

Pin No.	Pin Name
AF04	SMD5
AF05	SMD7
AF06	SMD0
AF07	RST_B
AF08	EVDD
AF09	POM4
AF10	POM1
AF11	IVDD
AF12	URCTS_B/MWSK
AF13	URSDO
AF14	IC-PDn
AF15	IC-Open
AF16	IC-Open
AF17	IVDD
AF18	IC-PUpR
AF19	GND
AF20	JDI
AF21	SSEL
AF22	IC-PDn
AF23	GND
AF24	MIRD1
AF25	GND
AF26	MIRDV

Special pin name description:

IC-PDn: Pull Down

IC-PDnR: Pull Down with Resistor

IC-PUp: Pull Up

IC-PUpR: Pull Up with Resistor

Remark In this document, XXX_B stands for active low pin.

CONTENTS

1. PIN FUNCTIONS

Symbol of I/O column indicates following status in this section.

I :Input
O :Output
I/O :Bidirection
I/OZ :Bidirection (Include Hi-Z state)
I/OD :Bidirection (Open drain output)
OZ :Output (Include Hi-Z state)
OD :Output (Open drain)

1.1 Power Supply

Pin Name	Pin No.	I/O	Active Level	Function
GND	A03, A05, AB23, AC16, AC23, AD01, AE02, AE07, AE14, AF01, AF19, AF23, C16, C26, D10, D21, D22, E04, G04, H02, H26, P26, T03, T26, W03, Y23, Y26, A19, AA02, AD05, AE11, AF25, B07, B10, B14, D03, J02, L25, M04, N03, V04			GND (0 V)
IVDD	A02, A10, A14, AA01, AA26, AD14, AE24, AF11, B16, D18, E23, J01, J23, L26, M03, P25, V03, A11, AD07, AD10, AD26, AE01, AE19, AF17, C10, C21, G03, T02, T25, W23			Internal logic core power supply (+2.5 V)
EVDD	A07, A12, AA23, AB03, AC06, AC13, AC15, AD20, AE03, AF08, B08, B20, C24, E01, E26, K24, N04, R02, U04, U25, Y02, A06, D17, K03			External (I/O) power supply (+3.3 V)

1.2 System PLL Power Supply

Pin Name	Pin No.	I/O	Active Level	Function
PSAGND	E03			Analog ground (0 V)
PSAVD	D01			Analog power supply (+2.5 V)
PSDGND	D02			Digital ground (0 V)
PSDVD	E02			Digital power supply (+2.5 V)

1.3 USB PLL Power Supply

Pin Name	Pin No.	I/O	Active Level	Function
PUAGND	A04			Analog ground (0 V)
PUAVD	C05			Analog power supply (+2.5 V)
PUDGND	B05			Digital ground (0 V)
PUDVD	B04			Digital power supply (+2.5 V)

1.4 System Control Interface

Pin Name	Pin No.	I/O	Active Level	Function
SCLK	C01	I		System clock (33 MHz)
CLKSL	C02	I		Clock select (L: 100 MHz/H: 66 MHz) for VR4120A and SDRAM
PSMD_B	F04	I	L	System PLL mode control input (L: normal, H: through) Note
PSTBY	F03	I	H	System PLL standby mode control input (L: active, H: standby)
PUMD_B	C04	I	L	USB PLL mode control (L: normal, H: through) Note
PUSTBY	B06	I	H	USB PLL standby mode control (L: active, H: standby)
BIG	AE18	I	H	VR4120A big endian mode
ENDCEN	AE08	I		Endian conversion enable
EXINT_B	AD08	I	L	External interrupt
EXNMI_B	AC08	I	L	External non-maskable interrupt
RST_B	AF07	I	L	System reset
ROMSEL0, ROMSEL1	AC21, AD21	I		ROM access bus width (ROMSEL1/0 = L/L: 32-bit, L/H: 16-bit, H/L: 8-bit)
SSEL	AF21	I		UART/Micro Wire Select (L: UART, H: Micro Wire)

Note PSMD_B and PUMD_B pins shall be connected to GND.

1.5 Memory Interface

Pin Name	Pin No.	I/O	Active Level	Function
SDCLK0, SDCLK1	AB04, AA03	O		SDRAM clock
SDCKE0, SDCKE1	AC02, Y04	O	H	SDRAM clock enable
SDCS_B	AA04	O	L	SDRAM chip select
SDRAS_B	AB01	O	L	SDRAM row address strobe
SDCAS_B	AB02	O	L	SDRAM column address strobe
SDWE_B	AC01	O	L	SDRAM/PROM/FLASH write enable
SRMCS_B	F01	O	L	PROM/FLASH chip select
SRMOE_B	F02	O	L	PROM/FLASH output enable
SMA0 - SMA20	Y03, Y01, W04, W02, W01, V02, V01, U03, U02, U01, T04, T01, R04, R03, R01, P04, P03, P02, P01, N01, N02	O		Memory address
SMD0-SMD31	AF06, AC07, AE06, AE05, AD06, AF04, AC05, AF05, AD04, AE04, AC04, AD02, AF03, AF02, AD03, AC03, M01, M02, L01, L02, L03, L04, K01, K02, K04, J03, J04, H01, H03, H04, G01, G02	I/O		Memory data

1.6 ATM Interface

(1) UTOPIA management interface

Pin Name	Pin No.	I/O	Active Level	Function
UMMD	A26	O		Management mode select
UMINT_B	A24	I	L	Interrupt from PHY
UMRD_B	C23	O	L	Management read enable
UMRDY_B	C22	I	L	Management data ready
UMRST_B	A22	O	L	PHY reset
UMSL_B	B23	O	L	PHY select
UMWR_B	B24	O	L	Management write enable
UMAD0 - UMAD11	F24, F23, E25, D26, E24, D25, D24, C25, B26, B25, D23, A25	O		PHY address
UMD0 - UMD7	L23, K26, K25, K23, J26, J25, J24, H25	I/O		Management data

(2) UTOPIA data interface

Pin Name	Pin No.	I/O	Active Level	Function
UDRCLK	C15	O		Receive clock
UDRCLV	C11	I	H	Receive cell available
UDRE_B	D11	O	L	Receive enable
UDRSC	B11	I	H	Receive cell start
UDRAD0 - UDRAD4	A16, D15, B15, A15, D14	O		Receive PHY address
UDRD0 - UDRD7	C14, A13, B13, C13, D13, B12, C12, D12	I		Receive data
UDTCLK	A21	O		Transmit clock
UDTCLV	D16	I	H	Transmit Cell Available
UDTE_B	A17	O	L	Transmit enable
UDTSC	B17	O	H	Transmit Cell start position
UDTAD0 - UDTAD4	B19, C18, B18, A18, C17	O		Transmit PHY address
UDTD0 - UDTD7	A23, B22, B21, D20, C20, A20, D19, C19	O		Transmit data

1.7 Ethernet Interface

(1) Ethernet interface (Channel 1)

Pin Name	Pin No.	I/O	Active Level	Function
MIRCLK	AE25	I		MII - Receive clock (2.5 MHz/25 MHz)
MIMCLK	AD22	O		MII - Management clock
MIMD	AD24	I/O		MII – Management data
MICOL	AC26	I		MII - Collision
MICRS	AB24	I		MII - Carrier sense
MIRDV	AF26	I		MII - Receive data valid
MIRER	AD25	I		MII - Receive error
MIRD0 - MIRD3	AD23, AF24, AC22, AE23	I		MII - Receive data
MITCLK	AC25	I		MII - Transmit clock (2.5 MHz/25 MHz)
MITE	AE26	O		MII - Transmit enable
MITER	AC24	O		MII - Transmit error
MITD0 - MITD3	AA25, AA24, AB26, AB25	O		MII - Transmit data

(2) Ethernet interface (Channel 2)

Pin Name	Pin No.	I/O	Active Level	Function
MI2RCLK	U24	I		MII - Receive clock (2.5 MHz/25 MHz)
MI2MCLK	W24	O		MII - Management clock
MI2MD	V25	I/O		MII - Management data
MI2COL	R24	I		MII - Collision
MI2CRS	T24	I		MII - Carrier sense
MI2RDV	V26	I		MII - Receive data valid
MI2RER	U26	I		MII - Receive error
MI2RD0 - MI2RD3	V24, V23, W26, W25	I		MII - Receive data
MI2TCLK	R23	I		MII - Transmit clock (2.5 MHz/25 MHz)
MI2TE	U23	O		MII - Transmit enable
MI2TER	T23	O		MII - Transmit error
MI2TD0 - MI2TD3	P24, P23, R26, R25	O		MII - Transmit data

1.8 USB Interface

Pin Name	Pin No.	I/O	Active Level	Function
USBCLK	D05	I		External USB clock (12 MHz)
USBDM	D08	I/O		USB data (–)
USBDP	C08	I/O		USB data (+)

1.9 UART/Micro Wire Interface

Pin Name	Pin No.	I/O	Active Level	Function
URCLK	AD11	I		UART external clock (18.432 MHz)
URSDO	AF13	O		UART serial data output
URSDI	AC12	I		UART serial data input
URDTR_B	AE13	O	L	UART data terminal ready
URRTS_B	AD13	O	L	UART data request to send
/MWDI		I		Micro Wire data in
URCTS_B	AF12	I	L	UART clear to send
/MWSK		O		Micro Wire sampling clock out
URDCD_B	AE12	I	L	UART data carrier detect
/MWCS		O		Micro Wire chip select
URDSR_B	AD12	I	L	UART data set ready
/MWDO		O		Micro Wire data out

Remark For the function multiplexed pins (AD13, AF12, AE12, AD12), function is determined as follows.

SSEL = L: UART operation mode

SSEL = H: Micro Wire operation mode

1.10 Parallel Port Interface

Pin Name	Pin No.	I/O	Active Level	Function
POM0 - POM7	AC11, AF10, AC10, AE10, AF09, AC09, AE09, AD09	O		Parallel port signal output

1.11 Boundary Scan Interface

Pin Name	Pin No.	I/O	Active Level	Function
JCK	AE20	I		B-SCAN clock
JDI	AF20	I		B-SCAN input-data
JDO	AC19	OZ		B-SCAN output-data
JMS	AD19	I		B-SCAN mode select
JRSTB_B	AC18	I	L	B-SCAN reset

1.12 I.C. - Open

Pin Name	Pin No.	I/O	Active Level	Function
IC-Open	A09, B09, A01, B02, D07, B03, AC14, AD15, AD17, AD18, AE15, AF15, AF16	O		Leave open

1.13 I.C. - Pull Down

Pin Name	Pin No.	I/O	Active Level	Function
IC-PDn	AF22, C03, B01, D04, C06, D06, C07, AE21, AC20, AD16, AE22, AF14	I		Connect to GND

1.14 I.C. - Pull Down with Resistor

Pin Name	Pin No.	I/O	Active Level	Function
IC-PDnR	C09, D09, Y24, Y25	I/O		Connect to GND via pull-down resistor

1.15 I.C. - Pull Up

Pin Name	Pin No.	I/O	Active Level	Function
IC-PUp	L24	I		Connect to EVDD

1.16 I.C. - Pull Up with Resistor

Pin Name	Pin No.	I/O	Active Level	Function
IC-PUpR	A08, H24, H23, G26, G25, G24, G23, F26, F25, N26, N25, N24, N23, M26, M25, M23, M24, AC17, AE16, AE17, AF18	I/O		Connect to EVDD via pull-up resistor

2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	IV_{DD}	Internal logic core	−0.5 to +3.6	V
	EV_{DD}	I/O buffer	−0.5 to +4.6	V
Input/output voltage	V_{I1}/V_{O1}	LVTTL-level pin	−0.5 to +4.6	V
	V_{I2}/V_{O2}	USB I/O buffer	−0.5 to +4.6	V
Output current	I_{O1}	LVTTL-level pin, I_{OL} = 9 mA	30	mA
	I_{O2}	USB I/O buffer, I_{OL} = 18 mA	55	mA
Storage temperature	T_{stg}		−60 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	IV_{DD}		2.35	2.5	2.65	V
	EV_{DD}		3.15	3.3	3.45	V
Low level input voltage	V_{IL1}	LVTTL-level pin	0		0.8	V
	V_{IL2}	USB I/O/ buffer, refer to **(9) USB Interface Parameter** (Single-end operation)			0.8	V
High level input voltage	V_{IH1}	LVTTL-level pin	2.0			V
	V_{IH2}	USB I/O/ buffer, refer to **(9) USB Interface Parameter** (Single-end operation)	2.0			V
USB differential input voltage	V_{IDF}	USB I/O buffer, refer to **(9) USB Interface Parameter** (Differential operation)	0.2			V
Operating ambient temperature	T_A		0		70	°C

DC Characteristics (IV_{DD} = 2.5 ± 0.15 V, EV_{DD} = 3.3 ± 0.15 V, T_A = 0 to +70 °C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★ Supply current	I_{IDD}				1100	mA
	E_{IDD}				200	mA
Input leakage current	I_{LI}	V_I = EV_{DD} or GND			±10	μA
Off state output current	I_{OZ}	V_O = EV_{DD} or GND			±10	μA
Low level output voltage	V_{OL1}	LVTTL-level pin, I_{OL} = 9 mA			0.4	V
	V_{OL2}	USB I/O buffer, refer to **(9) USB Interface Parameter**			0.3	V
High level output voltage	V_{OH1}	LVTTL-level pin, I_{OH}= 9mA	2.4			V
	V_{OH2}	USB I/O buffer, refer to **(9) USB Interface Parameter**	2.8		EV_{DD}	V

Capacitance (T_A = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_I	f_C = 1 MHz,	4		8	pF
Output Capacitance	C_O	Unmeasured pins returned to 0 V	4		8	pF
I/O Capacitance	C_{IO}		4		8	pF

Pin Classifications

Input pins

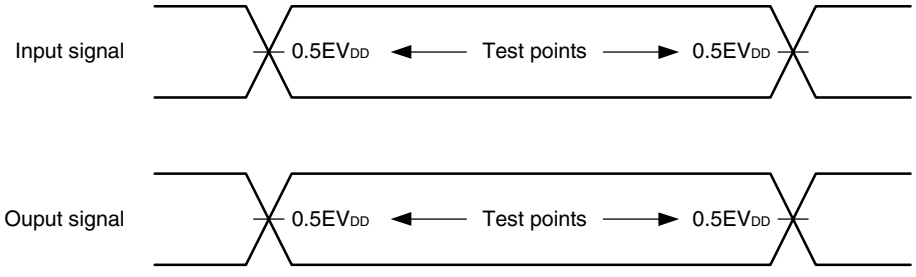
Category		Application Pins	Number of Pins
LVTTL-level pin	V_{I1}, V_{IL1}/V_{IH1}	BIG, CLKSL, ENDCEN, EXINT_B, EXNMI_B, JCK, JDI, JMS, JRSTB_B, MI2COL, MI2CRS, MI2MD, MI2RCLK, MI2RD[3:0], MI2RDV, MI2RER, MI2TCLK, MICOL, MICRS, MIMD, MIRCLK, MIRD[3:0], MIRDV, MIRER, MITCLK, MWDI, PSMD_B, PSTBY, PUMD_B, PUSTBY, ROMSEL[1:0], RST_B, SCLK, SMD[31:0], SSEL, UDRCLV, UDRD[7:0], UDRSC, UDTCLV, UMD[7:0], UMINT_B, UMRDY_B, URCLK, URCTS_B, URDCD_B, URDSR_B, URSDI, USBCLK	100
USB I/O buffer	V_{I2}, V_{IL2}/V_{IH2}, V_{IDF}	USBDP, USBDM	2

Output pins

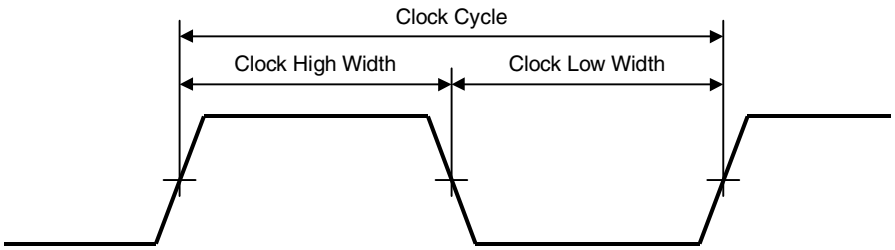
Category			Application Pins	Number of Pins
LVTTL-level pin	I_{O1}	V_{O1}, V_{OL1}/V_{OH1}	JDO, MI2MCLK, MI2MD, MI2TD[3:0], MI2TE, MI2TER, MIMCLK, MIMD, MITD[3:0], MITE, MITER, MWCS, MWDO, MWSK, POM[7:0], SDCAS_B, SDCKE0, SDCKE1, SDCLK0, SDCLK1, SDCS_B, SDRAS_B, SDWE_B, SMA[20:0], SMD[31:0], SRMCS_B, SRMOE_B, UDRAD[4:0], UDRCLK, UDRE_B, UDTAD[4:0], UDTCLK, UDTD[7:0], UDTE_B, UDTSC, UMAD[11:0], UMD[7:0], UMMD, UMRD_B, UMRST_B, UMSL_B, UMWR_B, URDTR_B, URRTS_B, URSDO	142
USB I/O buffer	I_{O2}	V_{O2}, V_{OL2}/V_{OH2}	USBDP, USBDM	2

AC Characteristics (IV_{DD} = 2.5 ± 0.15 V, EV_{DD} = 3.3 ± 0.15 V, T_A = 0 to +70 °C)

(1) AC Test Waveform



(2) Clock parameter



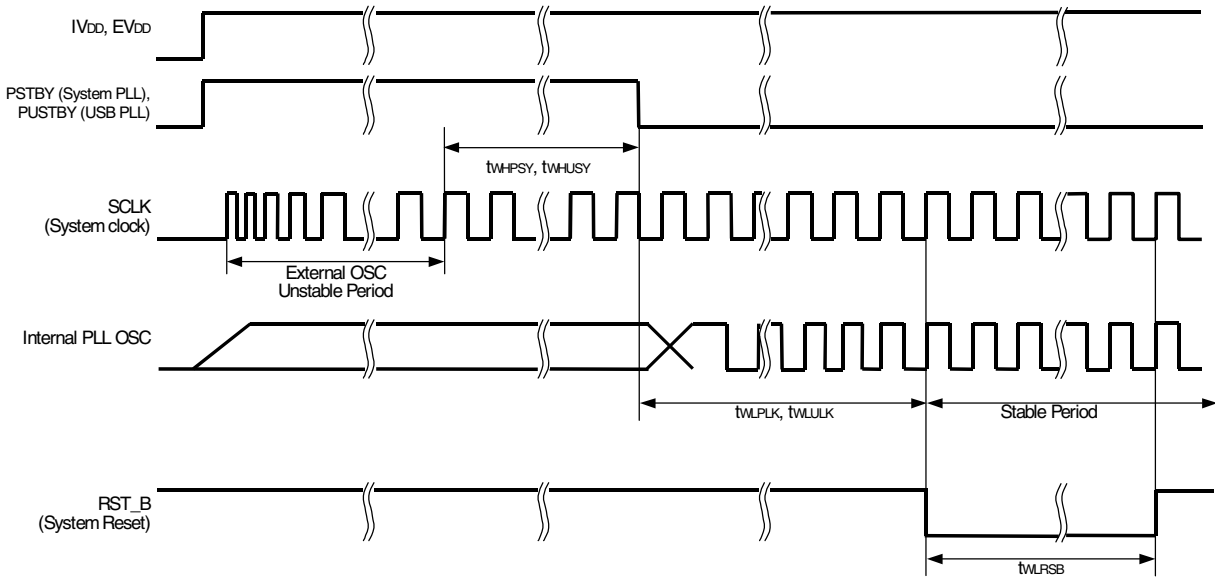
(2)-1 Clock input

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLK input cycle	t_{CYSCK}		30.0	40.0	ns
SCLK input high level width	t_{WHSCK}		0.4 × t_{CYSCK}	0.6 × t_{CYSCK}	ns
SCLK input low level width	t_{WLSCK}		0.4 × t_{CYSCK}	0.6 × t_{CYSCK}	ns
MITCLK input cycle	t_{CYMTK}		40.0	400.0	ns
MITCLK input high level width	t_{WHMTK}		0.4 × t_{CYMTK}	0.6 × t_{CYMTK}	ns
MITCLK input low level width	t_{WLMTK}		0.4 × t_{CYMTK}	0.6 × t_{CYMTK}	ns
MIRCLK input cycle	t_{CYMRK}		40.0	400.0	ns
MIRCLK input high level width	t_{WHMRK}		0.4 × t_{CYMRK}	0.6 × t_{CYMRK}	ns
MIRCLK input low level width	t_{WLMRK}		0.4 × t_{CYMRK}	0.6 × t_{CYMRK}	ns
MI2TCLK input cycle	t_{CY2TK}		40.0	400.0	ns
MI2TCLK input high level width	t_{WH2TK}		0.4 × t_{CY2TK}	0.6 × t_{CY2TK}	ns
MI2TCLK input low level width	t_{WL2TK}		0.4 × t_{CY2TK}	0.6 × t_{CY2TK}	ns
MI2RCLK input cycle	t_{CY2RK}		40.0	400.0	ns
MI2RCLK input high level width	t_{WH2RK}		0.4 × t_{CY2RK}	0.6 × t_{CY2RK}	ns
MI2RCLK input low level width	t_{WL2RK}		0.4 × t_{CY2RK}	0.6 × t_{CY2RK}	ns
USBCLK input cycle	t_{CYUBK}		83.1	84.6	ns
USBCLK input high level width	t_{WHUBK}		0.4 × t_{CYUBK}	0.6 × t_{CYUBK}	ns
USBCLK input low level width	t_{WLUBK}		0.4 × t_{CYUBK}	0.6 × t_{CYUBK}	ns
JCK input cycle	t_{CYJCK}		100.0	1000.0	ns
JCK input high level width	t_{WHJCK}		0.4 × t_{CYJCK}	0.6 × t_{CYJCK}	ns
JCK input low level width	t_{WLJCK}		0.4 × t_{CYJCK}	0.6 × t_{CYJCK}	ns

(2)-2 Clock output

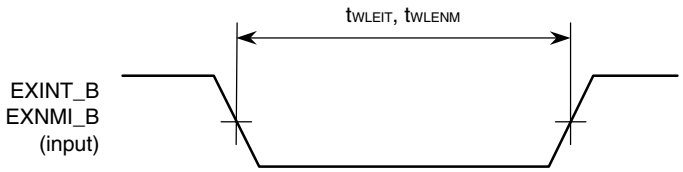
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SDCLK0 output cycle	t_{CYSK0}	Load 10 pF	10.0	15.0	ns
SDCLK0 output high level width	t_{WHSK0}	Load 10 pF	0.4 × t_{CYSK0}	0.6 × t_{CYSK0}	ns
SDCLK0 output low level width	t_{WLSK0}	Load 10 pF	0.4 × t_{CYSK0}	0.6 × t_{CYSK0}	ns
SDCLK1 output cycle	t_{CYSK1}	Load 10 pF	10.0	15.0	ns
SDCLK1 output high level width	t_{WHSK1}	Load 10 pF	0.4 × t_{CYSK1}	0.6 × t_{CYSK1}	ns
SDCLK1 output low level width	t_{WLSK1}	Load 10 pF	0.4 × t_{CYSK1}	0.6 × t_{CYSK1}	ns
UDTCLK output cycle	t_{CYUTK}	Load 50 pF	30.0		ns
UDTCLK output high level width	t_{WHUTK}	Load 50 pF	0.4 × t_{CYUTK}		ns
UDTCLK output low level width	t_{WLUTK}	Load 50 pF	0.4 × t_{CYUTK}		ns
UDRCLK output cycle	t_{CYURK}	Load 50 pF	30.0		ns
UDRCLK output high level width	t_{WHURK}	Load 50 pF	0.4 × t_{CYURK}		ns
UDRCLK output low level width	t_{WLURK}	Load 50 pF	0.4 × t_{CYURK}		ns
MIMCLK output cycle	t_{CYMCK}	Load 50 pF	420.0		ns
MIMCLK output high level width	t_{WHMCK}	Load 50 pF	0.4 × t_{CYMCK}		ns
MIMCLK output low level width	t_{WLMCK}	Load 50 pF	0.4 × t_{CYMCK}		ns
MI2MCLK output cycle	t_{CYM2K}	Load 50 pF	420.0		ns
MI2MCLK output high level width	t_{WHM2K}	Load 50 pF	0.4 × t_{CYM2K}		ns
MI2MCLK output low level width	t_{WLM2K}	Load 50 pF	0.4 × t_{CYM2K}		ns

(3) Reset, PLL parameter



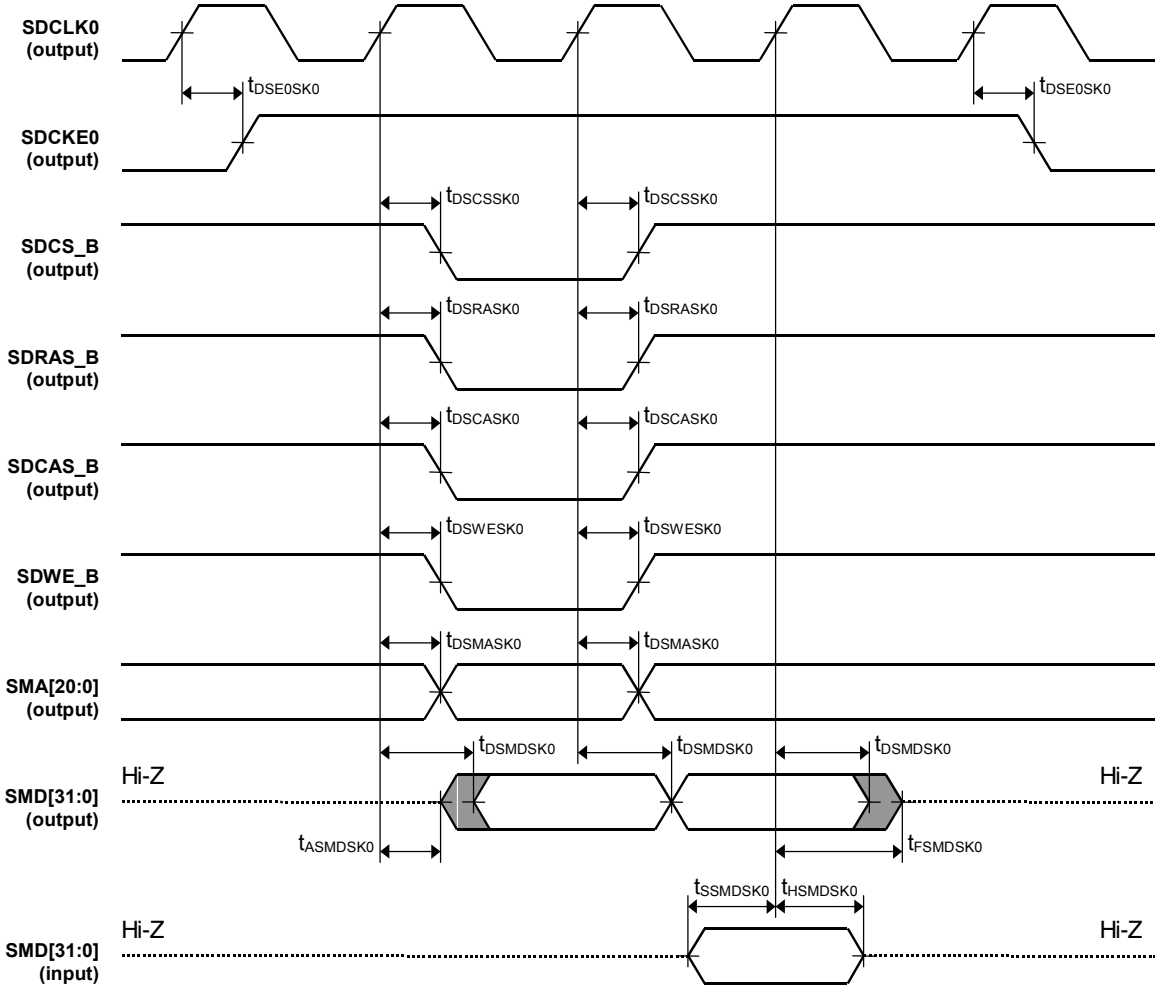
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
RST_B input low level width	t_{WLRSB}		6.0 × t_{CYSCK}		ns
PSTBY hold high level width	t_{WHPSY}		1		μs
PSTBY lookup time	t_{WLPLK}	Load 50 pF	1000		μs
PUSTBY hold high level width	t_{WHUSY}		1		μs
PUSTBY lookup time	t_{WLULK}	Load 50 pF	1000		μs

(4) Interrupt interface parameter

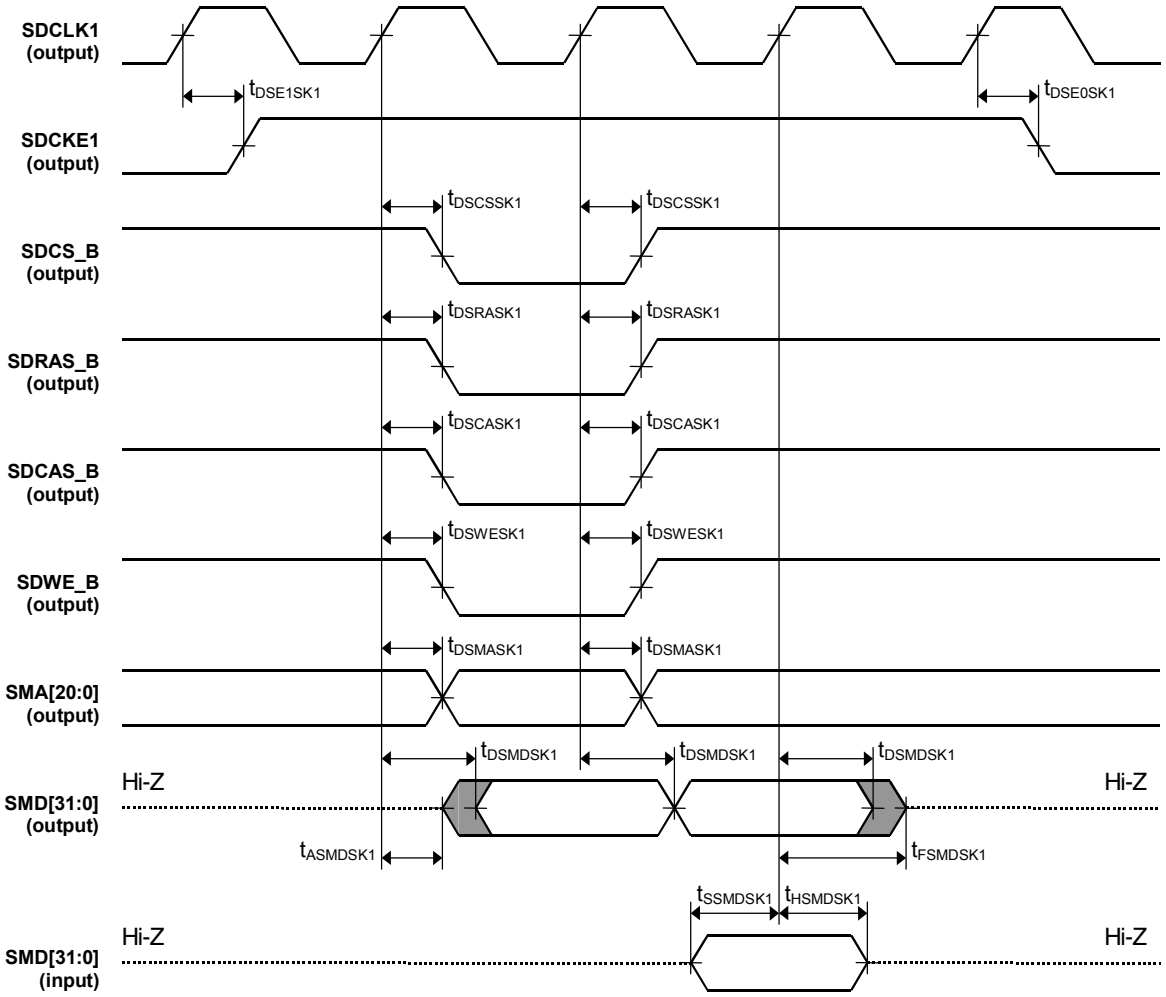


Parameter	Symbol	Conditions	MIN.	MAX.	Unit
EXINT_B input low level width	t_{WLEIN}		4.0 × t_{CYSK0}		ns
EXNMI_B input low level width	t_{WLENM}		4.0 × t_{CYSK0}		ns

(5) SDRAM interface parameter



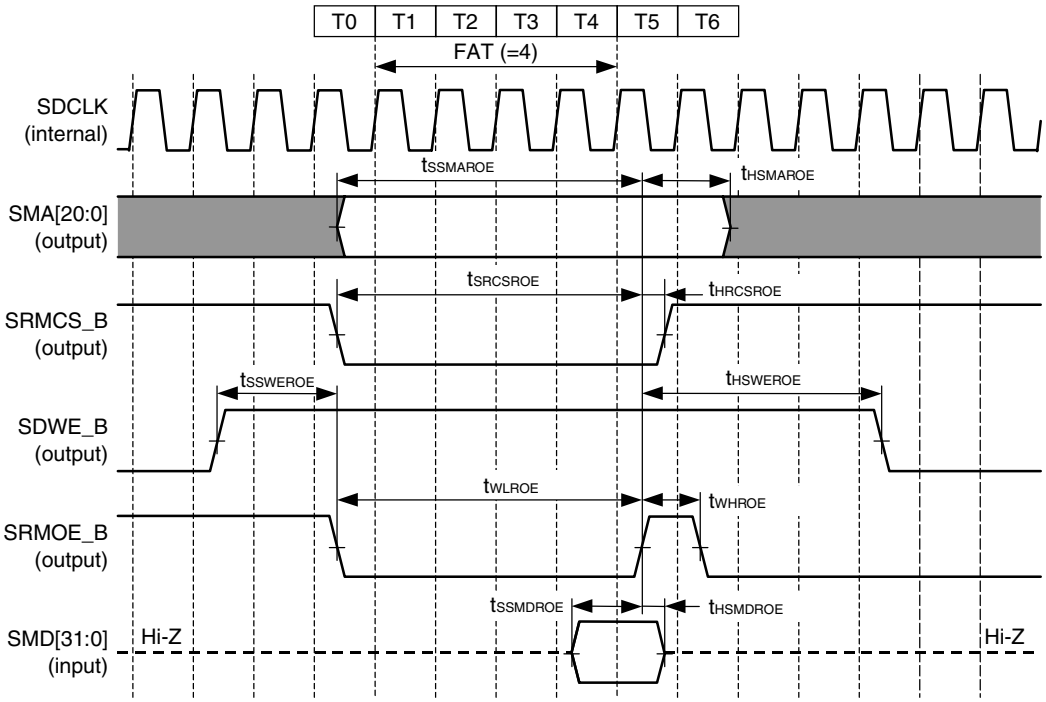
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SDCKE0 output delay from SDCLK0	$t_{DSE0SK0}$	Load 30 pF	1.0	7.5	ns
SDCS_B output delay from SDCLK0	$t_{DSCSSK0}$	Load 30 pF	1.0	7.5	ns
SDRAS_B output delay from SDCLK0	$t_{DSRASK0}$	Load 30 pF	1.0	7.5	ns
SDCAS_B output delay from SDCLK0	$t_{DSCASK0}$	Load 30 pF	1.0	7.5	ns
SDWE_B output delay from SDCLK0	$t_{DSWESK0}$	Load 50 pF	1.0	7.5	ns
SMA[20:0] output delay from SDCLK0	$t_{DSMASK0}$	Load 50 pF	1.0	7.5	ns
SMD[31:0] output floating to active delay from SDCLK0	$t_{ASMDSK0}$	Load 50 pF	1.0		ns
SMD[31:0] output delay from SDCLK0	$t_{DSMDSK0}$	Load 50 pF	1.0	7.5	ns
SMD[31:0] output active to floating delay from SDCLK0	$t_{FSMDSK0}$	Load 50 pF		7.5	ns
SMD[31:0] input setup to SDCLK0	$t_{SSMDSK0}$		4.0		ns
SMD[31:0] input hold from SDCLK0	$t_{HSMDSK0}$		1.0		ns



Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SDCKE1 output delay from SDCLK1	$t_{DSE1SK1}$	Load 30 pF	1.0	7.5	ns
SDCS_B output delay from SDCLK1	$t_{DSCSSK1}$	Load 30 pF	1.0	7.5	ns
SDRAS_B output delay from SDCLK1	$t_{DSRASK1}$	Load 30 pF	1.0	7.5	ns
SDCAS_B output delay from SDCLK1	$t_{DSCASK1}$	Load 30 pF	1.0	7.5	ns
SDWE_B output delay from SDCLK1	$t_{DSWESK1}$	Load 50 pF	1.0	7.5	ns
SMA[20:0] output delay from SDCLK1	$t_{DSMASK1}$	Load 50 pF	1.0	7.5	ns
SMD[31:0] output floating to active delay from SDCLK1	$t_{ASMDSK1}$	Load 50 pF	1.0		ns
SMD[31:0] output delay from SDCLK1	$t_{DSMDSK1}$	Load 50 pF	1.0	7.5	ns
SMD[31:0] output active to floating delay from SDCLK1	$t_{FSMDSK1}$	Load 50 pF		7.5	ns
SMD[31:0] input setup to SDCLK1	$t_{SSMDSK1}$		4.0		ns
SMD[31:0] input hold from SDCLK1	$t_{HSMDSK1}$		1.0		ns

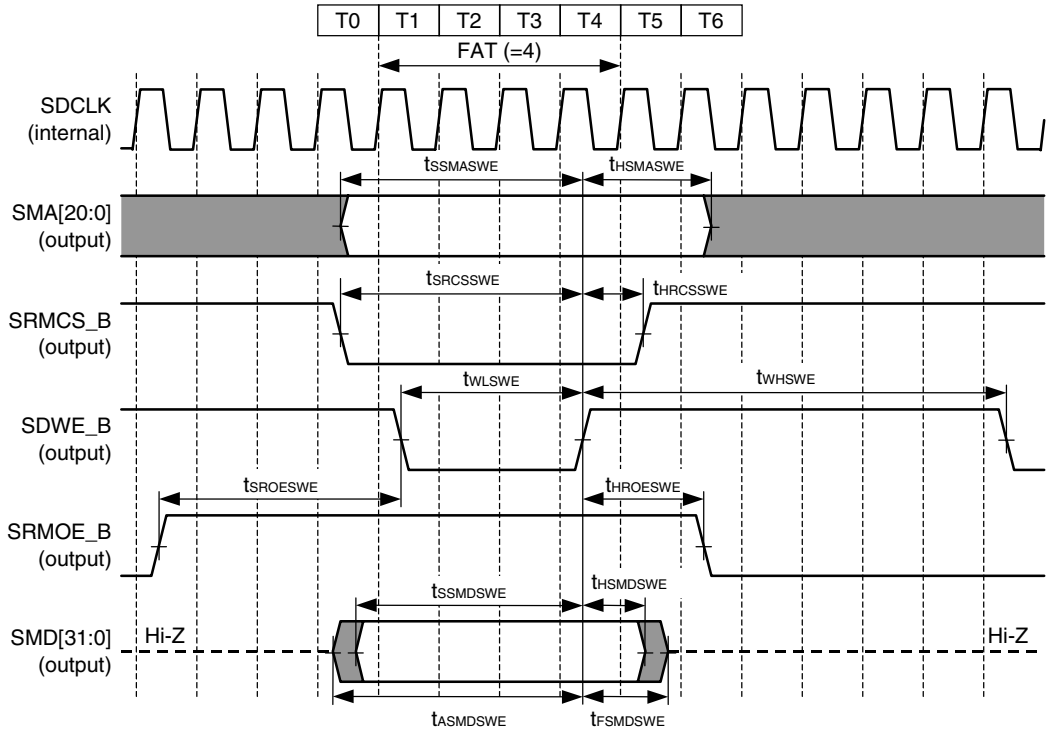
(6) Flash ROM interface parameter

<Read cycle>



	Parameter	Symbol	Condition	MIN.	MAX.	Unit
★	SMA[20:0] setup to SRMOE_B	$t_{SSMAROE}$	Load 50 pF	$5.0 \times t_{CYSK0} - 8.0$		ns
★	SMA[20:0] hold from SRMOE_B	$t_{HSMAROE}$	Load 50 pF	$1.0 \times t_{CYSK0} - 8.0$		ns
★	SRMCS_B setup to SRMOE_B	$t_{SRCSROE}$	Load 50 pF	$5.0 \times t_{CYSK0} - 8.0$		ns
	SRMCS_B hold from SRMOE_B	$t_{HRCSROE}$	Load 50 pF		5.0	ns
★	SDWE_B setup time to SRMOE_B	$t_{SSWEROE}$	Load 50 pF	$2.0 \times t_{CYSK0} - 8.0$		ns
★	SDWE_B hold time from SRMOE_B	$t_{HSWEROE}$	Load 50 pF	$4.0 \times t_{CYSK0} - 8.0$		ns
★	SRMOE_B low level pulse width	t_{WLROE}	Load 50 pF	$5.0 \times t_{CYSK0} - 8.0$		ns
★	SRMOE_B high level pulse width	t_{WHROE}	Load 50 pF	$1.0 \times t_{CYSK0} - 8.0$		ns
	SMD[31:0] setup to SRMOE_B	$t_{SSMDROE}$		10.0		ns
	SMD[31:0] hold from SRMOE_B	$t_{HSMDROE}$		0		ns

<Write cycle>

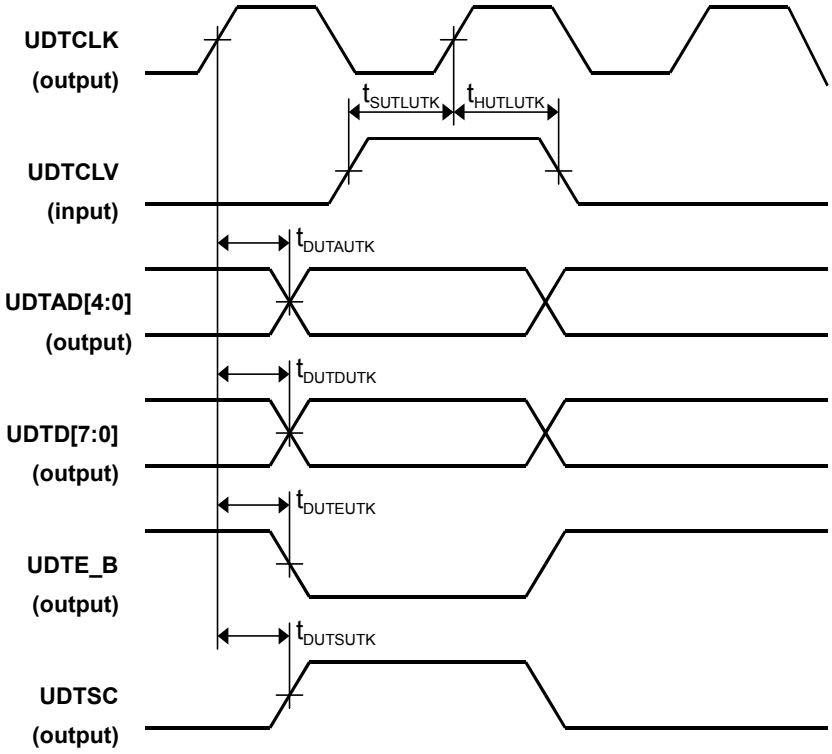


	Parameter	Symbol	Condition	MIN.	MAX.	Unit
★	SMA[20:0] setup to SDWE_B	$t_{SSMASWE}$	Load 50 pF	$4.0 \times t_{CYSK0} - 8.0$		ns
★	SMA[20:0] hold from SDWE_B	$t_{HSMASWE}$	Load 50 pF	$2.0 \times t_{CYSK0} - 8.0$		ns
★	SRMCS_B setup to SDWE_B	$t_{SRCSSWE}$	Load 50 pF	$4.0 \times t_{CYSK0} - 8.0$		ns
★	SRMCS_B hold from SDWE_B	$t_{HRCSSWE}$	Load 50 pF	$1.0 \times t_{CYSK0} - 8.0$		ns
★	SRMOE_B setup time to SDWE_B	$t_{SROESWE}$	Load 50 pF	$4.0 \times t_{CYSK0} - 8.0$		ns
★	SRMOE_B hold time from SDWE_B	$t_{HROESWE}$	Load 50 pF	$2.0 \times t_{CYSK0} - 8.0$		ns
★	SDWE_B low level pulse width	t_{WLSWE}	Load 50 pF	$3.0 \times t_{CYSK0} - 8.0$		ns
★	SDWE_B high level pulse width	t_{WHSWE}	Load 50 pF	$7.0 \times t_{CYSK0} - 8.0$		ns
★	SMD[31:0] setup to SDWE_B	$t_{SSMDSWE}$	Load 50 pF	$4.0 \times t_{CYSK0} - 8.0$		ns
★	SMD[31:0] hold from SDWE_B	$t_{HSMDSWE}$	Load 50 pF		$1.0 \times t_{CYSK0} + 8.0$	ns
★	SMD[31:0] output floating to active delay from SDWE_B	$t_{ASMDSWE}$	Load 50 pF	$4.0 \times t_{CYSK0} - 8.0$		ns
★	SMD[31:0] output active to floating delay from SDWE_B	$t_{FSMDSWE}$	Load 50 pF		$1.0 \times t_{CYSK0} + 8.0$	ns

(7) ATM interface parameter

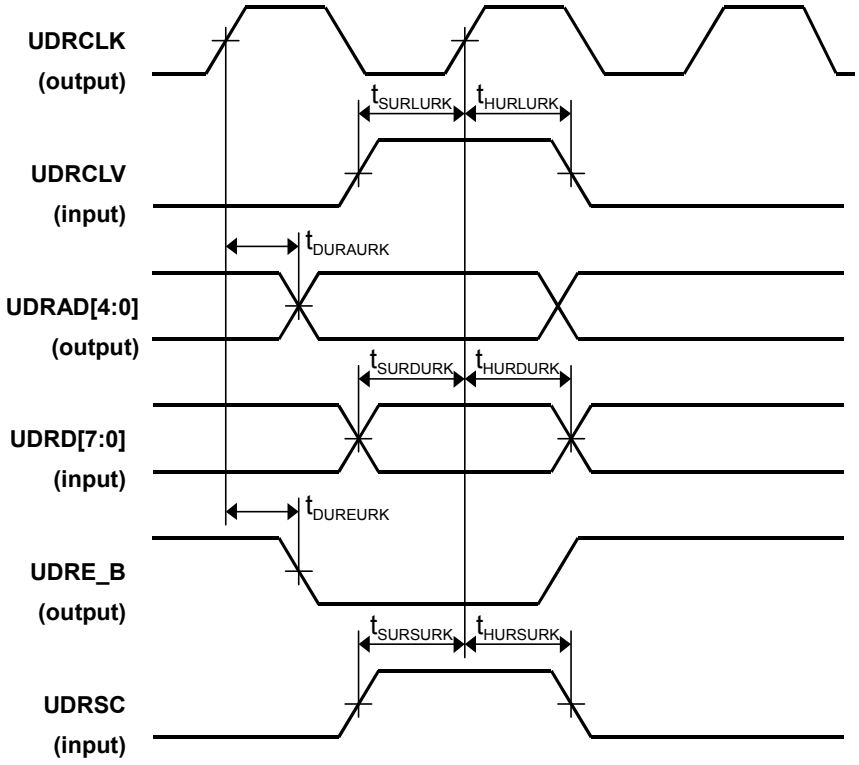
(7)-1 UTOPIA2 interface

<Data transmission>



Parameter	Symbol	Conditions	MIN.	MAX.	Unit
UDTCLV setup time to UDTCLK	$t_{SUTLUTK}$		8.0		ns
UDTCLV hold time from UDTCLK	$t_{HUTLUTK}$		1.0		ns
UDTAD[4:0] output delay from UDTCLK	$t_{DUTAUTK}$	Load 50 pF	1.0	15.0	ns
UDTD[7:0] output delay from UDTCLK	$t_{DUTDUTK}$	Load 50 pF	1.0	15.0	ns
UDTE_B output delay from UDTCLK	$t_{DUTEUTK}$	Load 50 pF	1.0	15.0	ns
UDTSC output delay from UDTCLK	$t_{DUTSUTK}$	Load 50 pF	1.0	15.0	ns

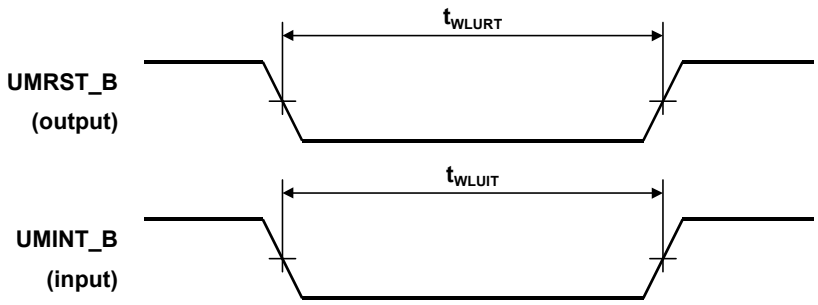
<Data reception>



Parameter	Symbol	Conditions	MIN.	MAX.	Unit
UDRCLV setup time to UDRCLK	$t_{SURLURK}$		8.0		ns
UDRCLV hold time from UDRCLK	$t_{HURLURK}$		1.0		ns
UDRAD[4:0] output delay from UDRCLK	$t_{DURAURK}$	Load 50 pF	1.0	15.0	ns
UDRD[7:0] setup to from UDRCLK	$t_{SURDURK}$		8.0		ns
UDRD[7:0] hold time from UDRCLK	$t_{HURDURK}$		1.0		ns
UDRE_B output delay from UDRCLK	$t_{DUREURK}$	Load 50 pF	1.0	15.0	ns
UDRSC setup time to UDRCLK	$t_{SURSURK}$		8.0		ns
UDRSC hold time from UDRCLK	$t_{HURSURK}$		1.0		ns

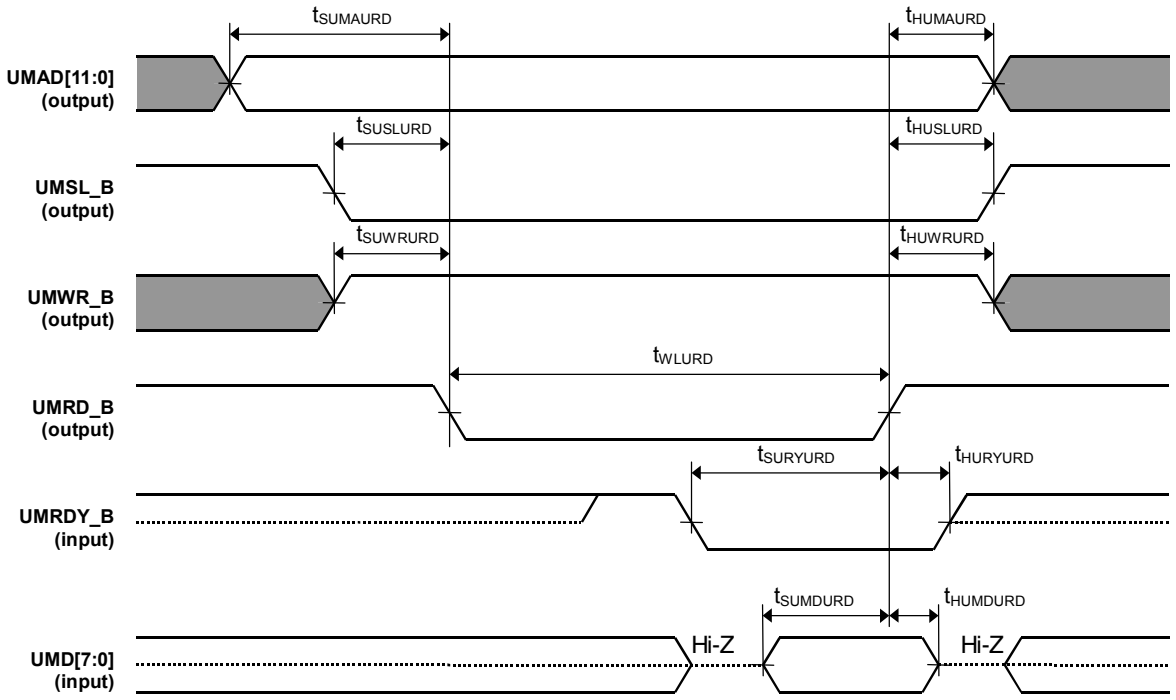
(7)-2 UTOPIA management interface

<Interface signals>



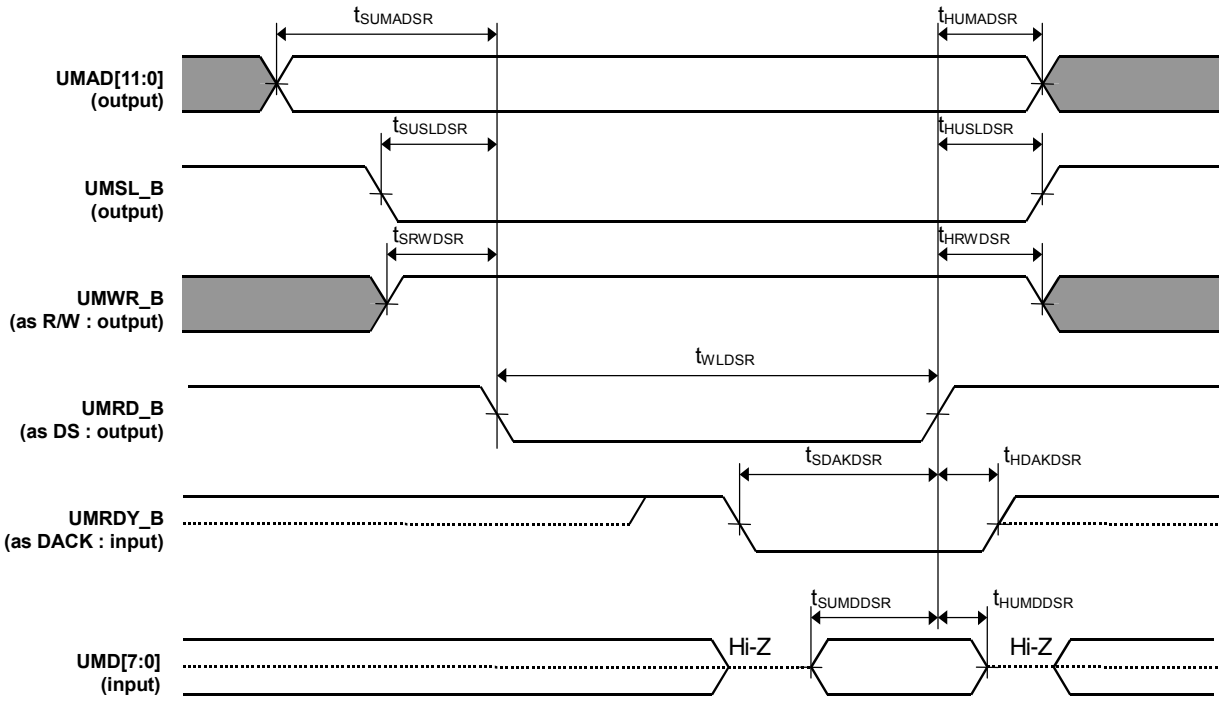
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
UMRST_B low level pulse width	t_{WLURT}		3.0 × t_{CYSCK}		ns
UMINT_B low level pulse width	t_{WLUIT}		3.0 × t_{CYSCK}		ns

<Read cycle : Intel mode>



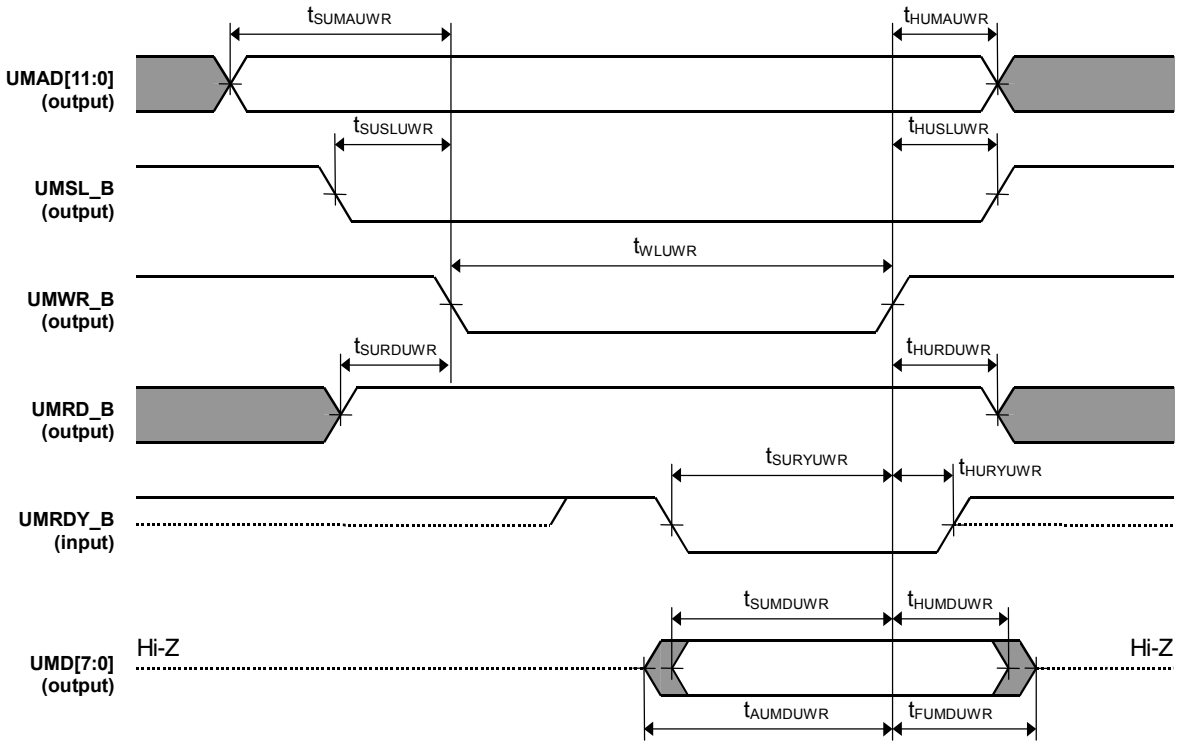
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
UMAD[11:0] setup to UMRD_B	$t_{SUMAURD}$	Load 50 pF	10		ns
UMAD[11:0] hold from UMRD_B	$t_{HUMAURD}$	Load 50 pF	4		ns
UMSL_B setup to UMRD_B	$t_{SUSLURD}$	Load 50 pF	5		ns
UMSL_B hold from UMRD_B	$t_{HUSLURD}$	Load 50 pF	0		ns
UMWR_B setup to UMRD_B	$t_{SUWRURD}$	Load 50 pF	5		ns
UMWR_B hold from UMRD_B	$t_{HUWRURD}$	Load 50 pF	0		ns
UMRD_B low level pulse width	t_{WLURD}	Load 50 pF	50		ns
UMRDY_B setup to UMRD_B	$t_{SURYURD}$		25		ns
UMRDY_B hold from UMRD_B	$t_{HURYURD}$		10		ns
UMD[7:0] setup to UMRD_B	$t_{SUMDURD}$		15		ns
UMD[7:0] hold from UMRD_B	$t_{HUMDURD}$		15		ns

<Read cycle : Motorola mode>



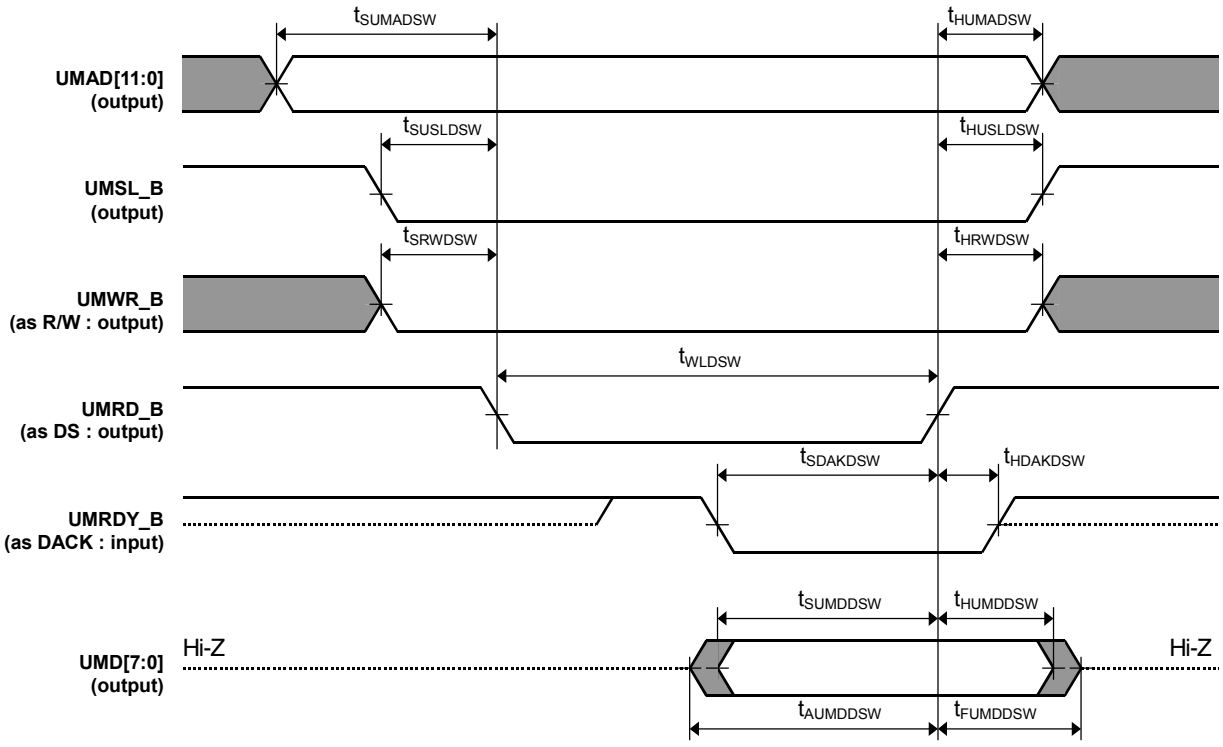
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
UMAD[11:0] setup to DS	$t_{SUMADSR}$	Load 50 pF	10		ns
UMAD[11:0] hold from DS	$t_{HUMADSR}$	Load 50 pF	4		ns
UMSL_B setup to DS	$t_{SUSLDSR}$	Load 50 pF	5		ns
UMSL_B hold from DS	$t_{HUSLDSR}$	Load 50 pF	0		ns
R/W setup to DS	t_{SRWDSR}	Load 50 pF	5		ns
R/W hold from DS	t_{HRWDSR}	Load 50 pF	0		ns
DS low level pulse width	t_{WLDSR}	Load 50 pF	50		ns
DACK setup to DS	$t_{SDAKDSR}$		25		ns
DACK hold from DS	$t_{HDAKDSR}$		10		ns
UMD[7:0] setup to DS	$t_{SUMDDSR}$		15		ns
UMD[7:0] hold from DS	$t_{HUMDDSR}$		15		ns

<Write cycle : Intel mode>



Parameter	Symbol	Conditions	MIN.	MAX.	Unit
UMAD[11:0] setup to UMWR_B	$t_{SUMAUWR}$	Load 50 pF	10		ns
UMAD[11:0] hold from UMWR_B	$t_{HUMAUWR}$	Load 50 pF	4		ns
UMSL_B setup to UMWR_B	$t_{SUSLUWR}$	Load 50 pF	5		ns
UMSL_B hold from UMWR_B	$t_{HUSLUWR}$	Load 50 pF	0		ns
UMRD_B setup to UMWR_B	$t_{SURDUWR}$	Load 50 pF	5		ns
UMRD_B hold from UMWR_B	$t_{HURDUWR}$	Load 50 pF	0		ns
UMWR_B low level pulse width	t_{WLUWR}	Load 50 pF	50		ns
UMRDY_B setup to UMWR_B	$t_{SURYUWR}$		25		ns
UMRDY_B hold from UMWR_B	$t_{HURYUWR}$		10		ns
UMD[7:0] setup to UMWR_B	$t_{SUMDUWR}$		15		ns
UMD[7:0] hold from UMWR_B	$t_{HUMDUWR}$		4		ns
UMD[7:0] active time to UMWR_B	$t_{AUMDUWR}$	Load 50 pF	15		ns
UMD[7:0] floating time from UMWR_B	$t_{FUMDUWR}$	Load 50 pF	4		ns

<Write cycle : Motorola mode>

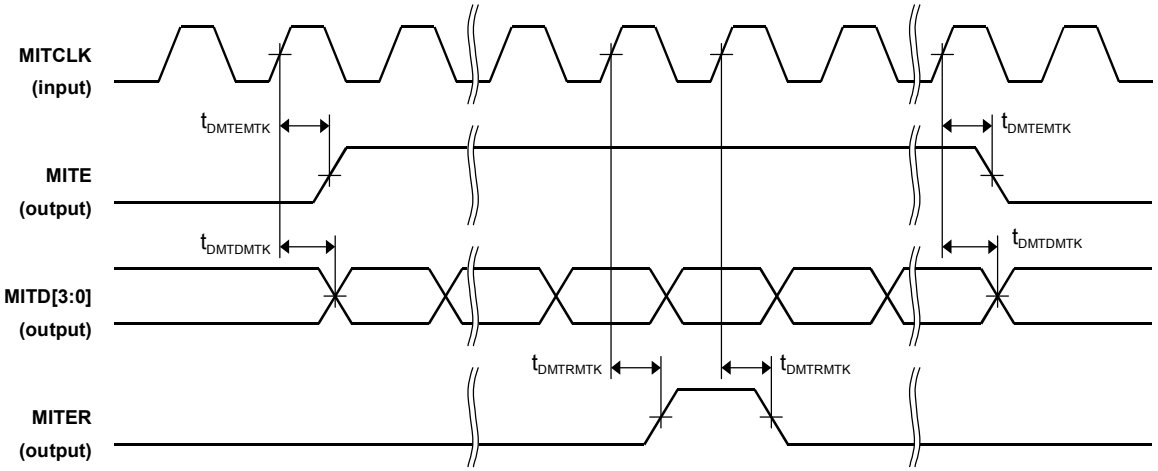


Parameter	Symbol	Conditions	MIN.	MAX.	Unit
UMAD[11:0] setup to DS	$t_{SUMADSW}$	Load 50 pF	10		ns
UMAD[11:0] hold from DS	$t_{HUMADSW}$	Load 50 pF	4		ns
UMSL_B setup to DS	$t_{SUSLDSW}$	Load 50 pF	5		ns
UMSL_B hold from DS	$t_{HUSLDSW}$	Load 50 pF	0		ns
R/W setup to DS	t_{SRWDSW}	Load 50 pF	5		ns
R/W hold from DS	t_{HRWDSW}	Load 50 pF	0		ns
DS low level pulse width	t_{WLDSW}	Load 50 pF	50		ns
DACK setup to DS	$t_{SDAKDSW}$		25		ns
DACK hold from DS	$t_{HDAKDSW}$		10		ns
UMD[7:0] setup to DS	$t_{SUMDDSW}$		15		ns
UMD[7:0] hold from DS	$t_{HUMDDSW}$		4		ns
UMD[7:0] active time to DS	$t_{AUMDDSW}$	Load 50 pF	15		ns
UMD[7:0] floating time from DS	$t_{FUMDDSW}$	Load 50 pF	4		ns

(8) Ethernet interface parameter

(8)-1 Ethernet 1

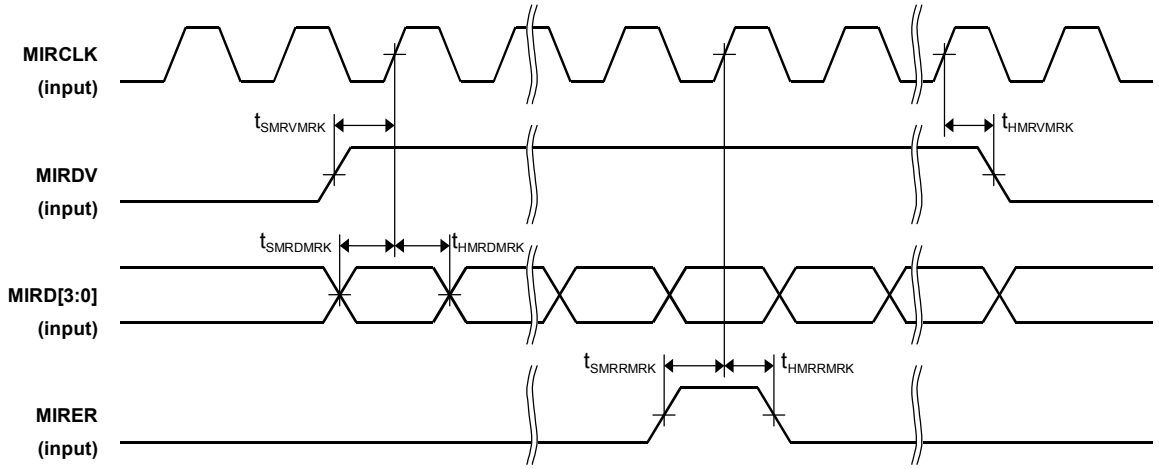
<MII data transmission>



Parameter	Symbol	Conditions	MIN.	MAX.	Unit
MITE output delay from MITCLK	$t_{DMTEMTK}$	Load 50 pF	0	20 Note	ns
MITD[3:0] output delay from MITCLK	$t_{DMTDMTK}$	Load 50 pF	0	20 Note	ns
MITER output delay from MITCLK	$t_{DMTRMTK}$	Load 50 pF	0	20 Note	ns

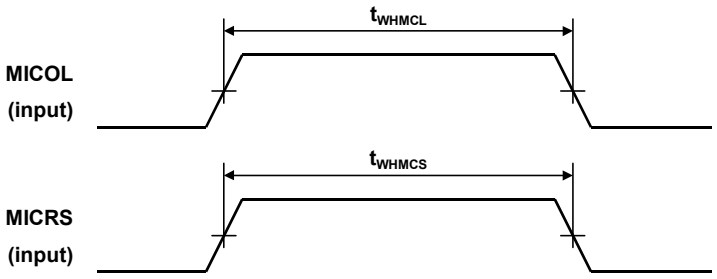
Note In MII Spec., Maximum output delay is specified as 25 ns

<MII data reception>



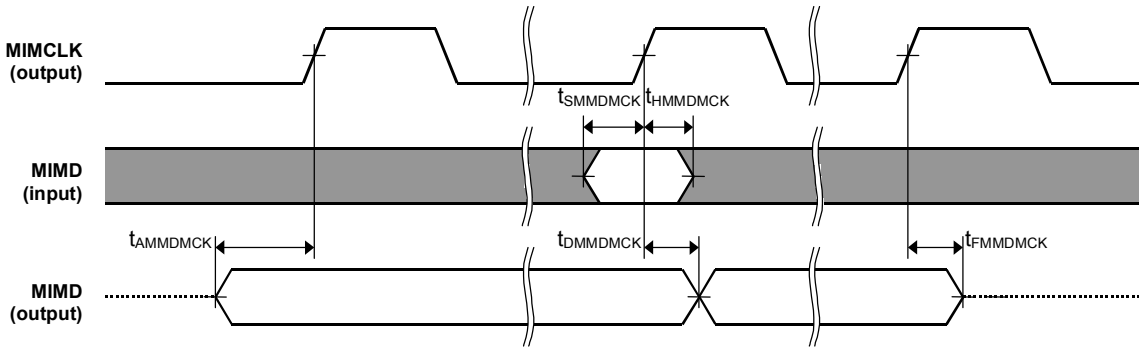
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
MIRDV setup time to MIRCLK	$t_{SMRVMRK}$		10		ns
MIRDV hold time from MIRCLK	$t_{HMRVMRK}$		10		ns
MIRD[3:0] setup time to MIRCLK	$t_{SMRDMRK}$		10		ns
MIRD[3:0] hold time from MIRCLK	$t_{HMRDMRK}$		10		ns
MIRER setup time to MIRCLK	$t_{SMRRMRK}$		10		ns
MIRER hold time from MIRCLK	$t_{HMRRMRK}$		10		ns

<MII interface signals>



Parameter	Symbol	Conditions	MIN.	MAX.	Unit
MICOL high level pulse width	t_{WHMCL}		2.0 × t_{CYMTK}		ns
MICRS high level pulse width	t_{WHMCS}		2.0 × t_{CYMTK}		ns

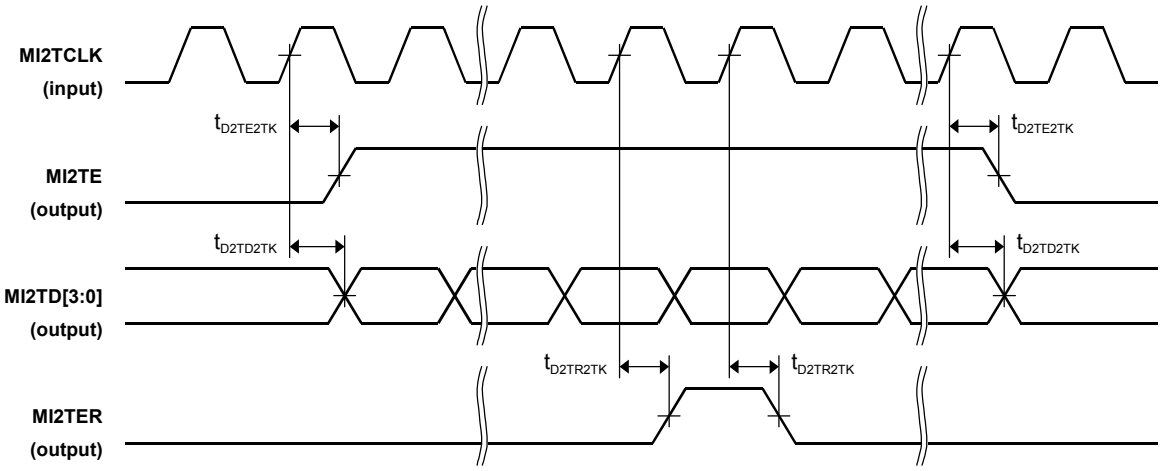
<MII management interface>



Parameter	Symbol	Condition	MIN.	MAX.	Unit
MIMD setup to MIMCLK	$t_{SMMDMCK}$		20		ns
MIMD hold from MIMCLK	$t_{HMMDMCK}$		0		ns
MIMD active delay from MIMCLK	$t_{AMMDMCK}$	Load 50 pF	10		ns
MIMD output delay from MIMCLK	$t_{DMMDMCK}$	Load 50 pF	10	20	ns
MIMD floating delay from MIMCLK	$t_{FMMDMCK}$	Load 50 pF	10		ns

(8)-2 Ethernet 2

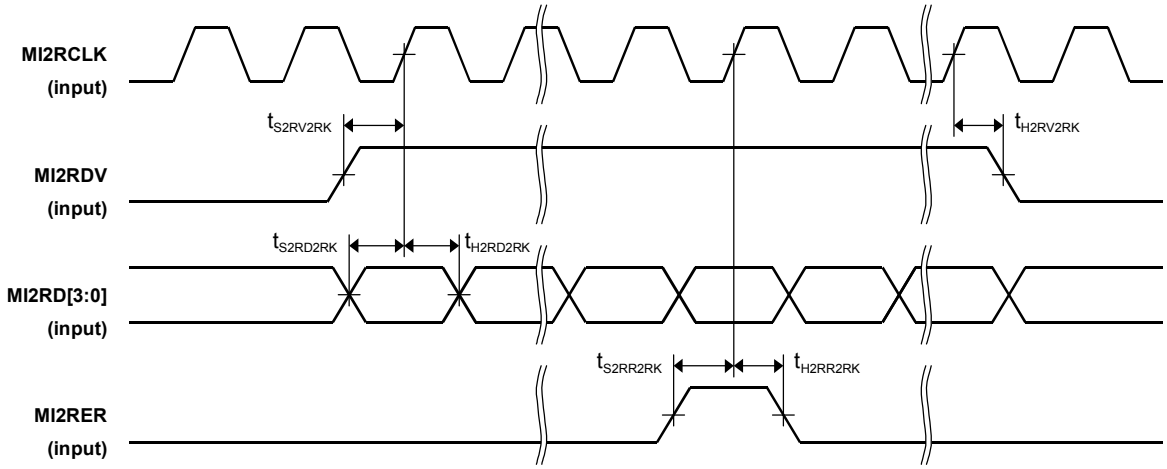
<MII data transmission>



Parameter	Symbol	Conditions	MIN.	MAX.	Unit
MI2TE output delay from MI2TCLK	$t_{D2TE2TK}$	Load 50 pF	0	20 Note	ns
MI2TD[3:0] output delay from MI2TCLK	$t_{D2TD2TK}$	Load 50 pF	0	20 Note	ns
MI2TER output delay from MI2TCLK	$t_{D2TR2TK}$	Load 50 pF	0	20 Note	ns

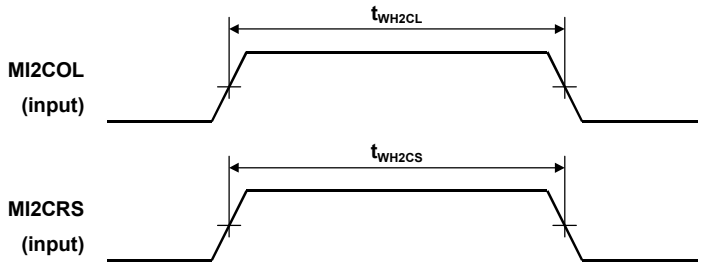
Note In MII Spec., Maximum output delay is specified as 25 ns

<MII data reception>



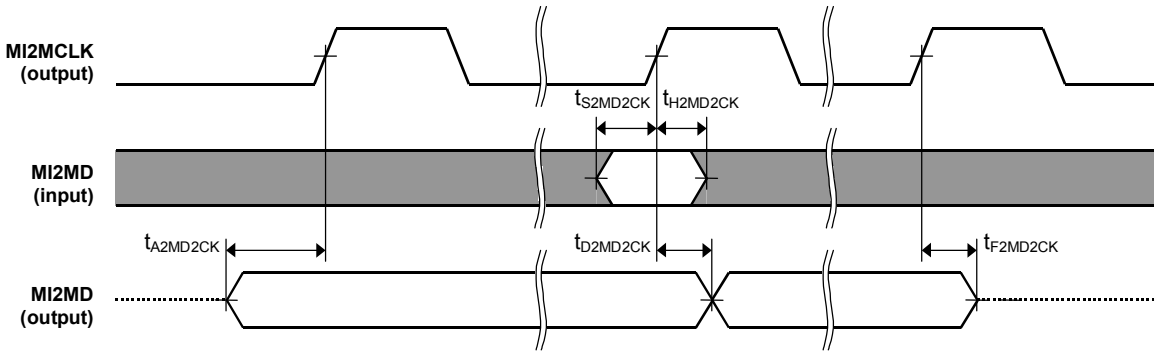
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
MI2RDV setup time to MI2RCLK	$t_{S2RV2RK}$		10		ns
MI2RDV hold time from MI2RCLK	$t_{H2RV2RK}$		10		ns
MI2RD[3:0] setup time to MI2RCLK	$t_{S2RD2RK}$		10		ns
MI2RD[3:0] hold time from MI2RCLK	$t_{H2RD2RK}$		10		ns
MI2RER setup time to MI2RCLK	$t_{S2RR2RK}$		10		ns
MI2RER hold time from MI2RCLK	$t_{H2RR2RK}$		10		ns

<MII interface signals>



Parameter	Symbol	Conditions	MIN.	MAX.	Unit
MI2COL high level pulse width	t_{WH2CL}		2.0 × t_{CY2TK}		ns
MI2CRS high level pulse width	t_{WH2CS}		2.0 × t_{CY2TK}		ns

<MII management interface>

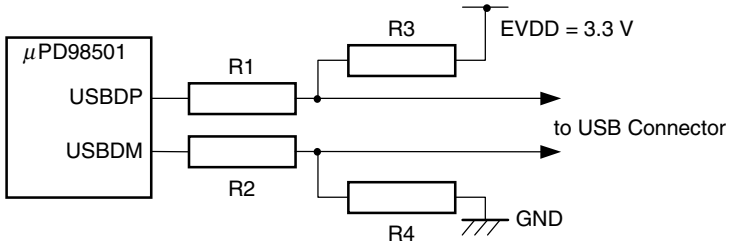


Parameter	Symbol	Condition	MIN.	MAX.	Unit
MI2MD setup to MI2MCLK	$t_{S2MD2CK}$		20		ns
MI2MD hold from MI2MCLK	$t_{H2MD2CK}$		0		ns
MI2MD active delay from MI2MCLK	$t_{A2MD2CK}$	Load 50 pF	10		ns
MI2MD output delay from MI2MCLK	$t_{D2MD2CK}$	Load 50 pF	10	20	ns
MI2MD floating delay from MI2MCLK	$t_{F2MD2CK}$	Load 50 pF	10		ns

(9) USB interface parameter

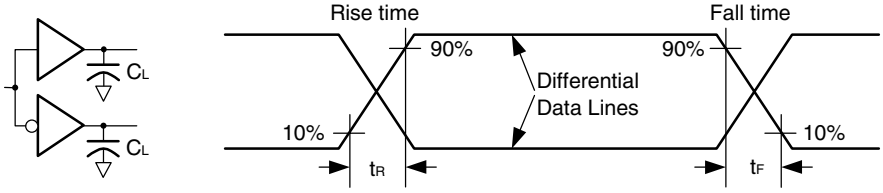
External Circuitry

The USB line I/O signals (refer to **chapter 1.8 USB interface**) need 4 external resistors to adjust the output impedance (R1 and R2 = 22 Ω each), to code the full speed USB mode (R3 = 1.5 kΩ) and to protect the output driver of the USBDM pin (R4 = 51 kΩ). The following figure shows a typical connection diagram.

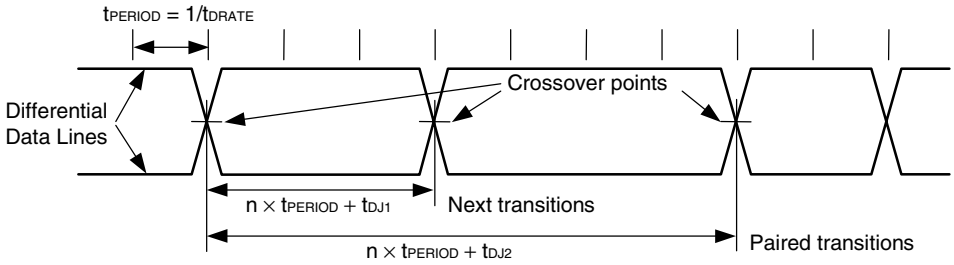


Parameter: USBDM, USBDP

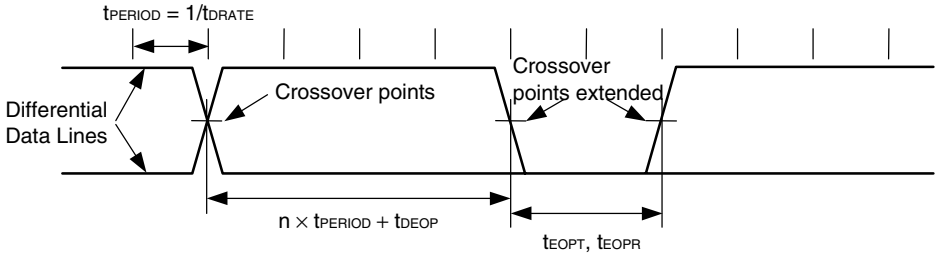
<Data signal rise and fall>



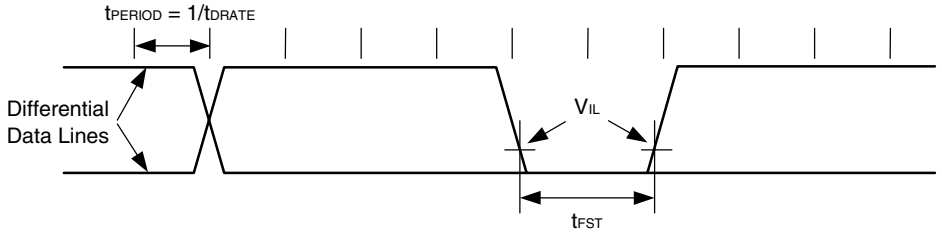
<Differential data jitter>



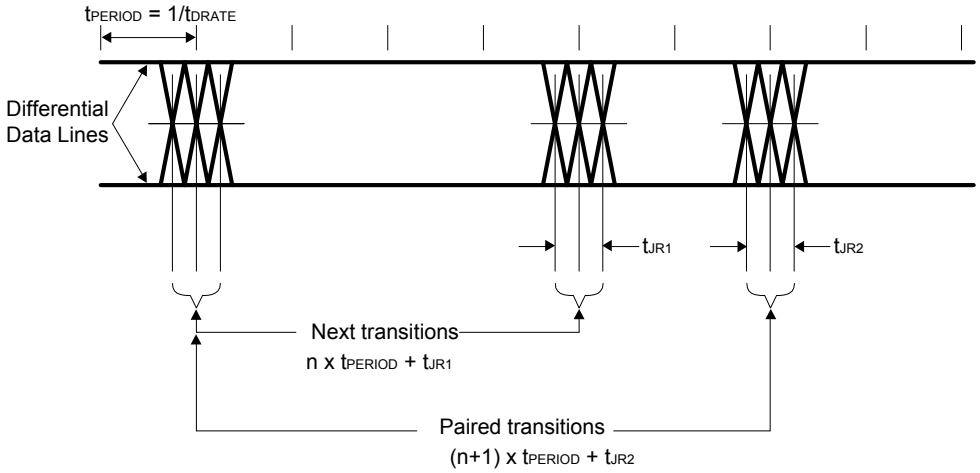
<Differential-to-EOP transition skew and EOP width>



<Differential transition interval width>

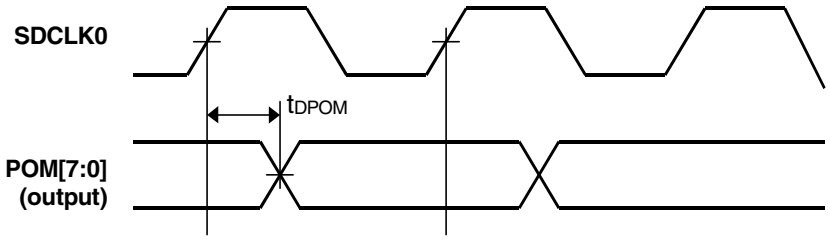


<Receiver jitter tolerance>



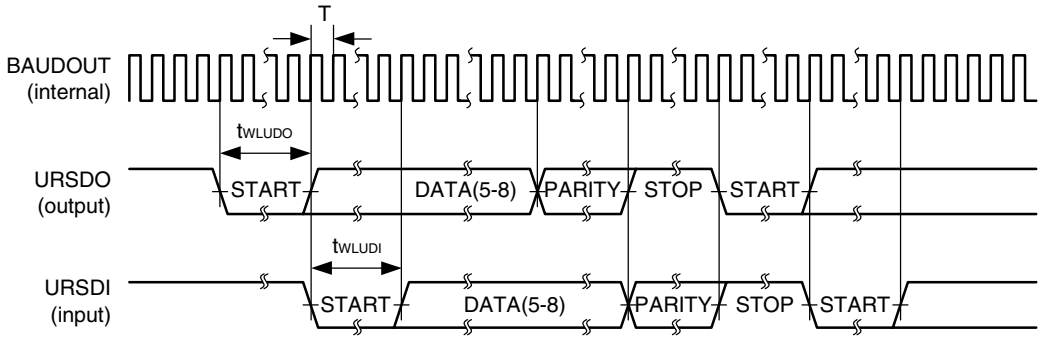
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Rise time	t_R	Load 50 pF	1.0	20.0	ns
Fall time	t_F	Load 50 pF	1.0	20.0	ns
Differential rise and fall time matching	t_{FRFM}	t_R/t_F	90.0	111.1	%
Full-speed data rate	t_{DRATE}		11.97	12.13	Mbps
Source jitter total (including frequency tolerance):					ns
To next transition	t_{DJ1}		−3.5	+3.5	
For paired transitions	t_{DJ2}		−4.0	+4.0	
Source jitter for differential transition to SE0 transition	t_{DEOP}		−2.0	+5.0	ns
Receiver jitter:					ns
To next transition	t_{JR1}		−18.5	+18.5	
For paired transitions	t_{JR2}		−9.0	+9.0	
Source SE0 interval of EOP	t_{EOPT}		160.0	175.0	ns
Receiver SE0 interval of EOP	t_{EOPR}		82.0		ns
Width of SE0 interval during differential transition	t_{FST}			14.0	ns

(10) Parallel port interface parameter



Parameter	Symbol	Conditions	MIN.	MAX.	Unit
POM[7:0] output delay	t_{DPOM}	Load 50 pF	0.0	8.0	ns

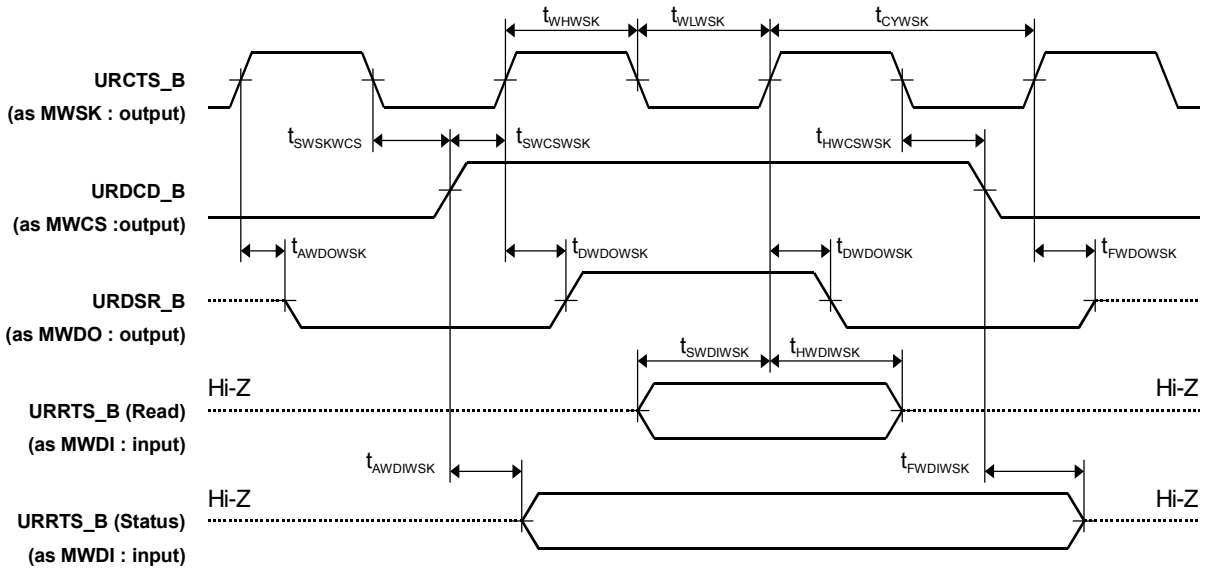
(11) UART interface parameter



Remark The BAUDOUT is equal to the 16X of transmisson baud rate (1/T = 16 × Baud Rate). Customize Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of baud rate generator.

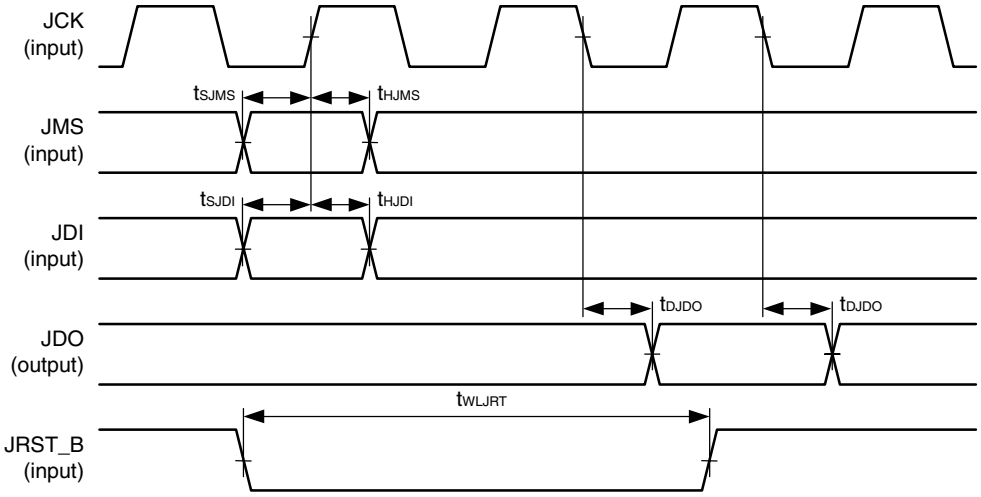
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
URCLK input frequency	f_{CYUCK}			18.432	MHz
URSDO low level width	t_{WLUDO}		16 × T		ns
URSDI low level width	t_{WLUDI}		16 × T		ns

(12) Micro Wire interface parameter



Parameter	Symbol	Conditions	MIN.	MAX.	Unit
MWSK clock cycle	t_{CYWSK}	Load 50 pF	400 × t_{CYSK0}		ns
MWSK high time	t_{WHWSK}	Load 50 pF	190 × t_{CYSK0}		ns
MWSK low time	t_{WLWSK}	Load 50 pF	190 × t_{CYSK0}		ns
MWSK setup to MWSK	$t_{SWSKWCS}$	Load 50 pF	90 × t_{CYSK0}		ns
MWCS setup to MWSK	$t_{SWCSWSK}$	Load 50 pF	90 × t_{CYSK0}		ns
MWCS hold from MWSK	$t_{HWCSWSK}$	Load 50 pF	90 × t_{CYSK0}		ns
MWDO output active to floating delay from MWSK	$t_{AWDOWSK}$	Load 50 pF	190 × t_{CYSK0}		ns
MWDO output delay from MWSK	$t_{DWDOWSK}$	Load 50 pF	190 × t_{CYSK0}		ns
MWDO output floating to active delay from MWSK	$t_{FWDOWSK}$	Load 50 pF	190 × t_{CYSK0}		ns
MWDI setup to MWSK	$t_{SWDIWSK}$		10 × t_{CYSK0}		ns
MWDI hold from MWSK	$t_{HWDIWSK}$		10 × t_{CYSK0}		ns
MWCS to status time from MWSK	$t_{AWDIWSK}$			100 × t_{CYSK0}	ns
MWCS to MWDO in 3-state	$t_{FWDIWSK}$			40 × t_{CYSK0}	ns

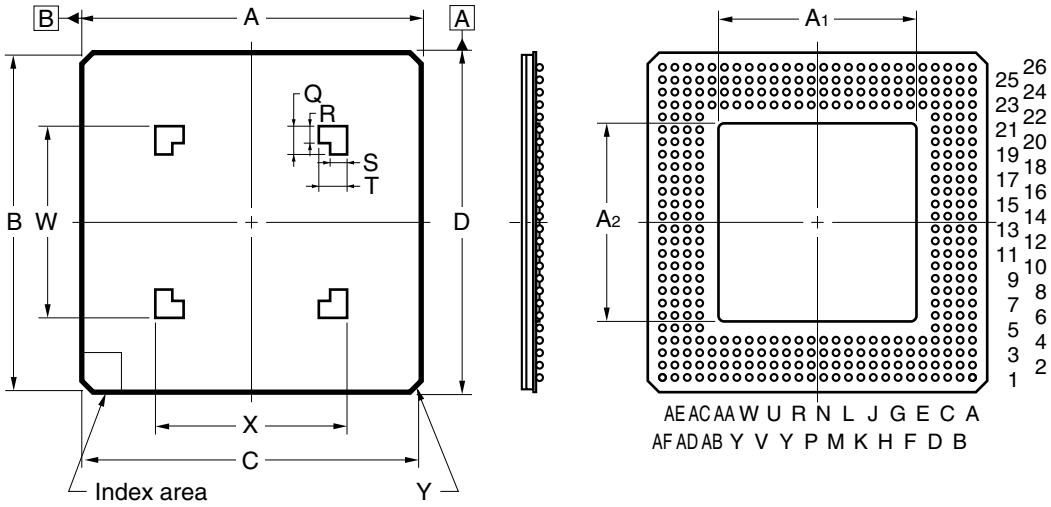
(13) JTAG boundary-scan

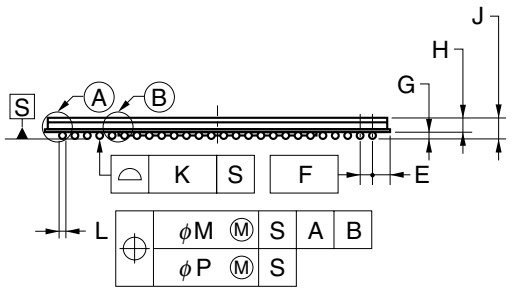


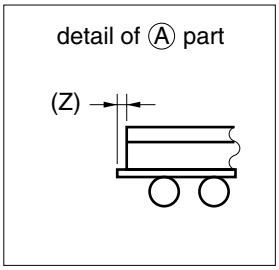
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
JMS Setup Time	t_{SJMS}		15		ns
JMS Hold Time	t_{HJMS}		15		ns
JDI Setup Time	t_{SJDI}		15		ns
JDI Hold Time	t_{HJDI}		15		ns
JDO Output Delay	t_{DJDO}	Load 50 pF		25	ns
JRSTB_B Low Pulse Width	t_{WLJRT}		$5 \times t_{CYJCK}$		ns

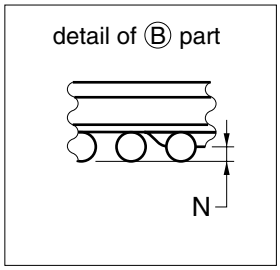
3. PACKAGE DRAWING

352-PIN TAPE BGA (HEAT SPREADER TYPE) (35x35)









ITEM	MILLIMETERS
A	35.00±0.20
A_1	23.00 MAX.
A_2	23.00 MAX.
B	34.60±0.15
C	34.60±0.15
D	35.00±0.20
E	1.625
F	1.27 (T.P.)
G	0.60±0.10
H	$0.80^{+0.20}_{-0.10}$
J	$1.40^{+0.30}_{-0.20}$
K	0.15
L	φ 0.75±0.15
M	0.30
N	0.25 MIN.
P	0.10
Q	3.0
R	2.0
S	2.0
T	3.0
W	20.19
X	20.19
Y	C0.4
Z	0.20

S352N7-127-F6-2

4. RECOMMENDED SOLDERING CONDITIONS

The μPD98501 should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 4-1. Surface Mounting Type Soldering Conditions

μPD98501N7-F6: 352-pin tape BGA (heat spreader type) (35 × 35)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher), Count: three times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-107-3
VPS	Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher), Count: three times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-107-3

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

VR4120A is a trademark of NEC Corporation.

Micro Wire is a trademark of National Semiconductor Corp.

Ethernet is a trademark of Xerox Corp.

MIPS is a trademark of MIPS Technologies, Inc.