NEC

MOS INTEGRATED CIRCUIT

μPD98433

10/100/1000 Mbps Ethernet™ Controller

The μPD98433 is a 10/100/1000 Mbps Ethernet controller with eight-port internal Media Access Control (MAC) function that complies with the IEEE Standard 802.3 1998 Edition.

Each port is provided with a 6 KB internal memory as transmit/receive FIFO.

★ The FIFO bus interface, which is used as the interface with the host systems, is a high-speed (125 MHz operation) bus interface that supports both 128-bit transmission and reception.

Since a statistic counter is included to support RMON/SNMP for each port, the μPD98433 is ideally suited for application such as LAN switches and routers.

Detailed function descriptions are provided in the following user's manual. Be sure to read this manual before designing.

μPD98433 User's Manual: S15212E

FEATURES

- 8-port 10/100/1000 Mbps on-chip MAC compliant with IEEE Standard 802.3 1998 Edition
- Interface with physical layer device can be selected from TBI, GMII, and MII
- On-chip 6 KB receive FIFO and 6 KB transmit FIFO for each port
- ★ On-chip high-speed FIFO data bus of 128 bits × 125 MHz per transmit or receive
- On-chip data bus of 32 bits × 62.5 MHz as a CPU bus
- Full-duplex operation (for 10/100/1000 Mbps operation) or half-duplex operation (for 10/100 Mbps operation) is possible
- Compatible with IEEE Standard 802.3 1998 Edition flow control
- Compatible with IEEE Standard 802.3 1998 Edition 8B10B PCS Encoder/Decoder
- Compatible with IEEE Standard 802.3 1998 Edition Chapter 37 Auto-Negotiation
- Filtering that responds to address types can be established
- Provides statistical information for supporting RMON/SNMP
- On-chip functions including VLAN frame detection function, low power function, and others
- JTAG support
- 0.25 μm CMOS process 2.5 V, 3.3 V dual system power supply

ORDERING INFORMATION

Part Number	Package
μPD98433S9-K6	756-pin plastic BGA (C/D advanced type) (45 × 45)

Remark This document uses xxx# as the active low representation (pin/signal name followed by #).

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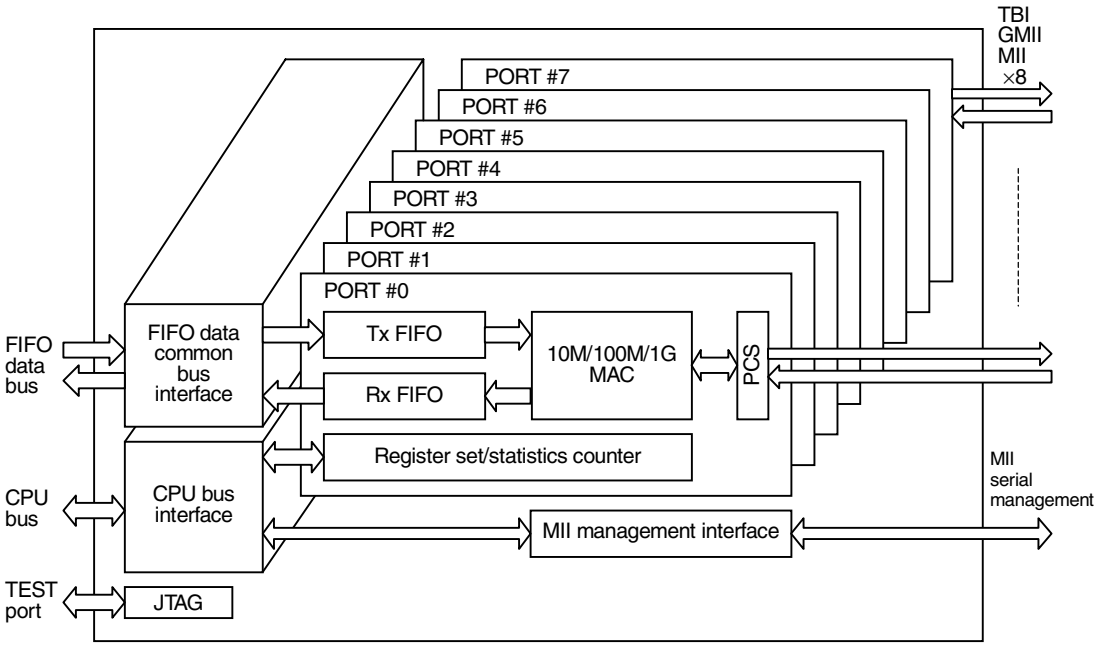
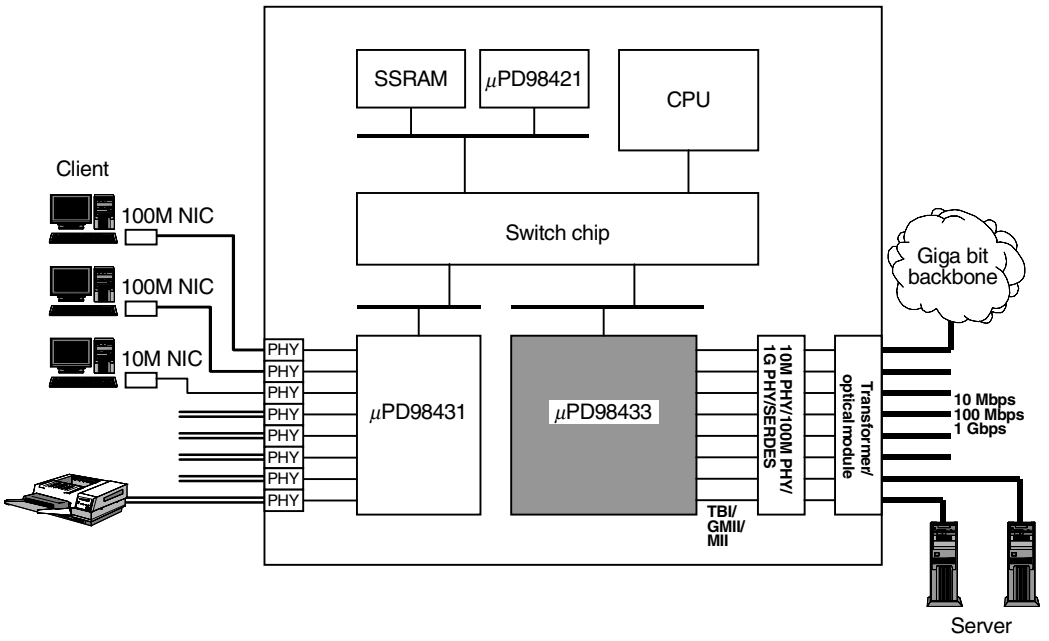
The mark ★ shows major revised points.

BLOCK DIAGRAM



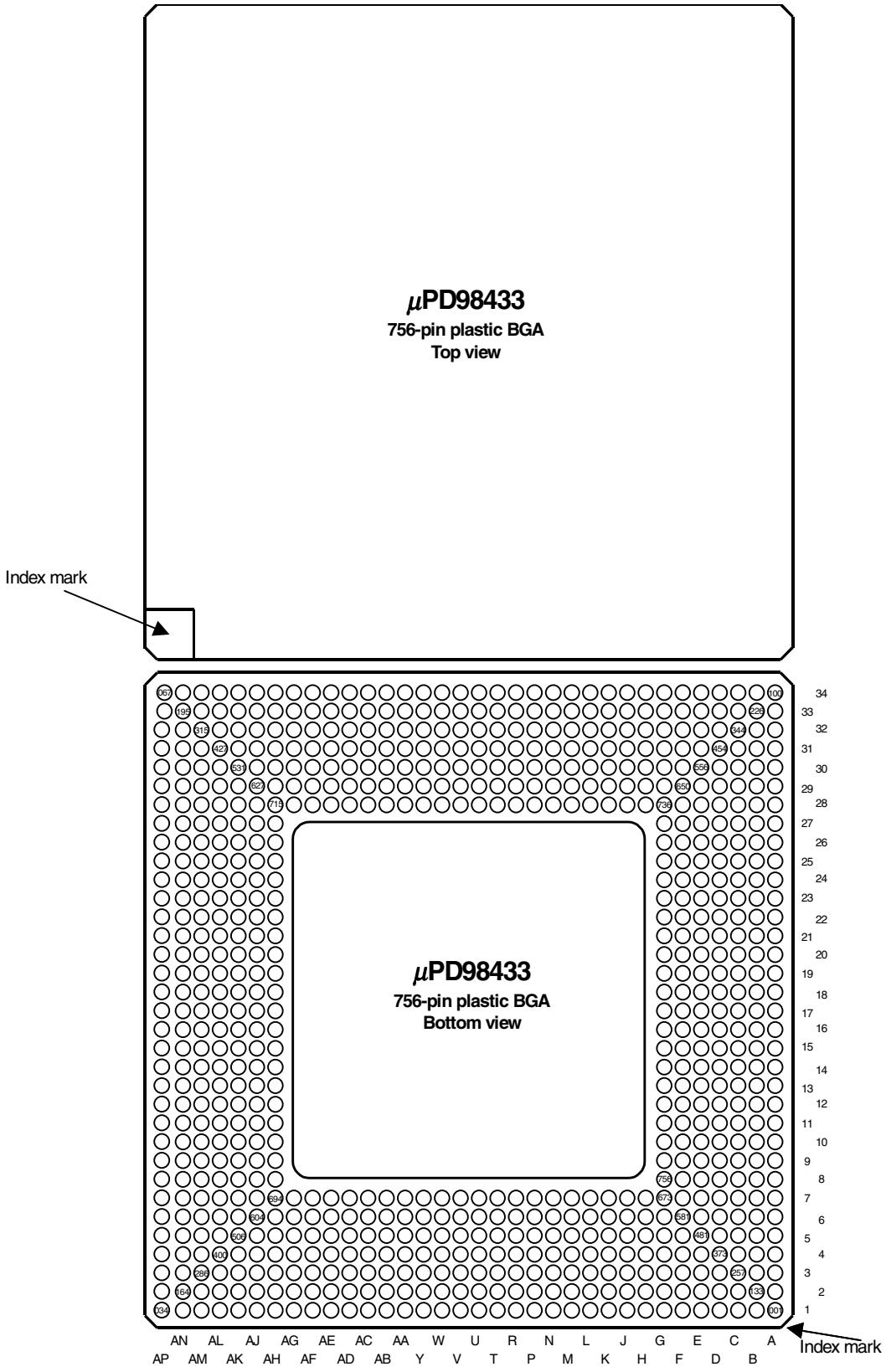
SYSTEM CONFIGURATION EXAMPLE



PIN CONFIGURATION

- **756-Pin Plastic BGA (C/D Advanced Type) (45 × 45)**

μPD98433S9-K6



PIN NAMES

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Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1 (A1)	GND	51 (AP18)	RXFDQ0	101 (A33)	GND	151 (Y2)	TXD24
2 (B1)	GND	52 (AP19)	RXFCK	102 (A32)	GND	152 (AA2)	TX_ER2
3 (C1)	GND	53 (AP20)	VDD	103 (A31)	TXFBA3	153 (AB2)	COL2
4 (D1)	FC7	54 (AP21)	RXFD74	104 (A30)	TXFBA0	154 (AC2)	RXD26
5 (E1)	TXFD4	55 (AP22)	RXFD80	105 (A29)	VDD	155 (AD2)	RXD23
6 (F1)	VDD	56 (AP23)	RXFD86	106 (A28)	TXFD114	156 (AE2)	RXD20
7 (G1)	TXD06	57 (AP24)	RXFD92	107 (A27)	TXFD108	157 (AF2)	TX_ER3
8 (H1)	EWRAP0	58 (AP25)	RXFD97	108 (A26)	VDDQ	158 (AG2)	LINK3#
9 (J1)	VDDQ	59 (AP26)	VDDQ	109 (A25)	TXFD97	159 (AH2)	RX_DV3
10 (K1)	TXD10	60 (AP27)	RXFD108	110 (A24)	TXFD92	160 (AJ2)	RXD34
11 (L1)	TXD12	61 (AP28)	RXFD114	111 (A23)	TXFD86	161 (AK2)	RXD32
12 (M1)	TXD15	62 (AP29)	VDD	112 (A22)	TXFD80	162 (AL2)	RXFD3
13 (N1)	EWRAP1	63 (AP30)	TMS	113 (A21)	TXFD74	163 (AM2)	GND
14 (P1)	RX_CLK11	64 (AP31)	TEST3	114 (A20)	VDD	164 (AN2)	GND
15 (R1)	VDD	65 (AP32)	GND	115 (A19)	TXFCK	165 (AN3)	GND
16 (T1)	CRS1	66 (AP33)	GND	116 (A18)	TXFDQ0	166 (AN4)	RXETH2
17 (U1)	HD4	67 (AP34)	GND	117 (A17)	TXFD62	167 (AN5)	RXFPT0
18 (V1)	HA2	68 (AN34)	GND	118 (A16)	TXFD56	168 (AN6)	RXFPT2
19 (W1)	HA8	69 (AM34)	GND	119 (A15)	VDD	169 (AN7)	RXFD6
20 (Y1)	VDD	70 (AL34)	RXD40	120 (A14)	TXFD45	170 (AN8)	RXFD12
21 (AA1)	GTX_CLK2	71 (AK34)	RXD43	121 (A13)	TXFD39	171 (AN9)	RXFD17
22 (AB1)	RX_CLK20	72 (AJ34)	VDD	122 (A12)	TXFD33	172 (AN10)	RXFD23
23 (AC1)	RXD25	73 (AH34)	COL4	123 (A11)	TXFD28	173 (AN11)	RXFD29
24 (AD1)	RXD22	74 (AG34)	TX_ER4	124 (A10)	TXFD22	174 (AN12)	RXFD34
25 (AE1)	CRS2	75 (AF34)	VDDQ	125 (A9)	VDDQ	175 (AN13)	RXFD40
26 (AF1)	VDDQ	76 (AE34)	CRS5	126 (A8)	TXFD11	176 (AN14)	RXFD46
27 (AG1)	COL3	77 (AD34)	RXD55	127 (A7)	TXFD5	177 (AN15)	RXFD51
28 (AH1)	RXD37	78 (AC34)	RX_CLK50	128 (A6)	VDD	178 (AN16)	RXFD57
29 (AJ1)	VDD	79 (AB34)	GTX_CLK5	129 (A5)	TXFEN#	179 (AN17)	RXFD63
30 (AK1)	RXFD4	80 (AA34)	TXD54	130 (A4)	FC1	180 (AN18)	RXFDQ1
31 (AL1)	RXETH7	81 (Y34)	VDD	131 (A3)	GND	181 (AN19)	RXFD64
32 (AM1)	GND	82 (W34)	HD12	132 (A2)	GND	182 (AN20)	RXFD69
33 (AN1)	GND	83 (V34)	HD18	133 (B2)	GND	183 (AN21)	RXFD75
34 (AP1)	GND	84 (U34)	HD24	134 (C2)	GND	184 (AN22)	RXFD81
35 (AP2)	GND	85 (T34)	HD30	135 (D2)	TXFD3	185 (AN23)	RXFD87
36 (AP3)	GND	86 (R34)	VDD	136 (E2)	TXD01	186 (AN24)	RXFD93
37 (AP4)	RXETH1	87 (P34)	RX_DV6	137 (F2)	TXD03	187 (AN25)	RXFD98
38 (AP5)	RXFEN#	88 (N34)	LINK6#	138 (G2)	TXD07	188 (AN26)	RXFD103
39 (AP6)	VDD	89 (M34)	TXD67	139 (H2)	TX_CLK0	189 (AN27)	RXFD109
40 (AP7)	RXFD5	90 (L34)	TXD63	140 (J2)	RX_ER0	190 (AN28)	RXFD115
41 (AP8)	RXFD11	91 (K34)	TXD60	141 (K2)	TXD11	191 (AN29)	RXFD120
42 (AP9)	VDDQ	92 (J34)	VDDQ	142 (L2)	TXD13	192 (AN30)	TCK
43 (AP10)	RXFD22	93 (H34)	LINK7#	143 (M2)	TXD16	193 (AN31)	TDO
44 (AP11)	RXFD28	94 (G34)	TX_EN7	144 (N2)	TX_CLK1	194 (AN32)	GND
45 (AP12)	RXFD33	95 (F34)	VDD	145 (P2)	RX_ER1	195 (AN33)	GND
46 (AP13)	RXFD39	96 (E34)	TXD72	146 (R2)	RXD14	196 (AM33)	GND
47 (AP14)	RXFD45	97 (D34)	TXD70	147 (T2)	HRW	197 (AL33)	CRS4
48 (AP15)	VDD	98 (C34)	GND	148 (U2)	HD5	198 (AK33)	RXD42
49 (AP16)	RXFD56	99 (B34)	GND	149 (V2)	HA3	199 (AJ33)	RXD46
50 (AP17)	RXFD62	100 (A34)	GND	150 (W2)	HA9	200 (AH33)	RX_CLK40

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Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
201 (AG33)	GTX_CLK4	251 (B8)	TXFD12	301 (AM18)	RXFDQ2	351 (C25)	TXFD99
202 (AF33)	TXD44	252 (B7)	TXFD6	302 (AM19)	RXFD65	352 (C24)	TXFD94
203 (AE33)	RXD50	253 (B6)	TXFPT2	303 (AM20)	RXFD70	353 (C23)	TXFD88
204 (AD33)	RXD54	254 (B5)	TXFPT0	304 (AM21)	RXFD76	354 (C22)	TXFD82
205 (AC33)	RX_CLK51	255 (B4)	FC2	305 (AM22)	RXFD82	355 (C21)	TXFD76
206 (AB33)	EWRAP5	256 (B3)	GND	306 (AM23)	RXFD88	356 (C20)	TXFD70
207 (AA33)	TXD55	257 (C3)	GND	307 (AM24)	RXFD94	357 (C19)	TXFD65
208 (Y33)	HD6	258 (D3)	FC0	308 (AM25)	RXFD99	358 (C18)	TXFDQ2
209 (W33)	HD11	259 (E3)	TXD02	309 (AM26)	RXFD104	359 (C17)	TEST5
210 (V33)	HD17	260 (F3)	TXD04	310 (AM27)	RXFD110	360 (C16)	TXFD58
211 (U33)	HD23	261 (G3)	TX_EN0	311 (AM28)	RXFD116	361 (C15)	TXFD52
212 (T33)	HD29	262 (H3)	LINK0#	312 (AM29)	RXFD121	362 (C14)	TXFD47
213 (R33)	RXD62	263 (J3)	RX_DV0	313 (AM30)	TDI	363 (C13)	TXFD41
214 (P33)	RXD67	264 (K3)	RXD04	314 (AM31)	TRST#	364 (C12)	TXFD35
215 (N33)	COL6	265 (L3)	TXD14	315 (AM32)	GND	365 (C11)	TXFD30
216 (M33)	TX_EN6	266 (M3)	TXD17	316 (AL32)	RXFCKOUT	366 (C10)	TXFD24
217 (L33)	TXD64	267 (N3)	LINK1#	317 (AK32)	RXD41	367 (C9)	TXFD18
218 (K33)	TXD61	268 (P3)	RX_DV1	318 (AJ32)	RXD45	368 (C8)	TXFD13
219 (J33)	RXD77	269 (R3)	RXD13	319 (AH32)	RX_CLK41	369 (C7)	TXFD7
220 (H33)	COL7	270 (T3)	HD0	320 (AG32)	EWRAP4	370 (C6)	TXFD0
221 (G33)	TX_ER7	271 (U3)	HACK#	321 (AF32)	TXD45	371 (C5)	TXFPT1
222 (F33)	TXD75	272 (V3)	HA4	322 (AE32)	RXD51	372 (C4)	FC3
223 (E33)	TXD73	273 (W3)	HA10	323 (AD32)	RXD53	373 (D4)	VDD
224 (D33)	TXD71	274 (Y3)	TXD23	324 (AC32)	RX_ER5	374 (E4)	FC4
225 (C33)	GND	275 (AA3)	TX_EN2	325 (AB32)	TX_CLK5	375 (F4)	TXD05
226 (B33)	GND	276 (AB3)	LINK2#	326 (AA32)	TXD56	376 (G4)	TX_ER0
227 (B32)	GND	277 (AC3)	RXD27	327 (Y32)	TXD53	377 (H4)	COL0
228 (B31)	TXFBA4	278 (AD3)	RXD24	328 (W32)	HD10	378 (J4)	RXD07
229 (B30)	TXFBA1	279 (AE3)	RXD21	329 (V32)	HD16	379 (K4)	RXD03
230 (B29)	TXFD120	280 (AF3)	TX_EN3	330 (U32)	HD22	380 (L4)	VDD
231 (B28)	TXFD115	281 (AG3)	TX_CLK3	331 (T32)	HD28	381 (M4)	TX_EN1
232 (B27)	TXFD109	282 (AH3)	RX_ER3	332 (R32)	RXD61	382 (N4)	GND
233 (B26)	TXFD103	283 (AJ3)	RXD35	333 (P32)	RXD66	383 (P4)	RXD17
234 (B25)	TXFD98	284 (AK3)	RXD33	334 (N32)	RX_CLK60	384 (R4)	RXD12
235 (B24)	TXFD93	285 (AL3)	RXETH0	335 (M32)	TX_ER6	385 (T4)	HD1
236 (B23)	TXFD87	286 (AM3)	GND	336 (L32)	TXD65	386 (U4)	HCLK
237 (B22)	TXFD81	287 (AM4)	RXETH3	337 (K32)	CRS7	387 (V4)	HA5
238 (B21)	TXFD75	288 (AM5)	RXFPT1	338 (J32)	RXD76	388 (W4)	HCS#
239 (B20)	TXFD69	289 (AM6)	RXFD0	339 (H32)	RX_CLK70	389 (Y4)	TXD22
240 (B19)	TXFD64	290 (AM7)	RXFD7	340 (G32)	GTX_CLK7	390 (AA4)	TXD27
241 (B18)	TXFDQ1	291 (AM8)	RXFD13	341 (F32)	TXD76	391 (AB4)	GND
242 (B17)	TXFD63	292 (AM9)	RXFD18	342 (E32)	TXD74	392 (AC4)	RX_DV2
243 (B16)	TXFD57	293 (AM10)	RXFD24	343 (D32)	TXFBA7	393 (AD4)	VDD
244 (B15)	TXFD51	294 (AM11)	RXFD30	344 (C32)	GND	394 (AE4)	TXD34
245 (B14)	TXFD46	295 (AM12)	RXFD35	345 (C31)	TXFBA6	395 (AF4)	TXD37
246 (B13)	TXFD40	296 (AM13)	RXFD41	346 (C30)	TXFBA2	396 (AG4)	VDD
247 (B12)	TXFD34	297 (AM14)	RXFD47	347 (C29)	TXFD121	397 (AH4)	RX_CLK31
248 (B11)	TXFD29	298 (AM15)	RXFD52	348 (C28)	TXFD116	398 (AJ4)	RXD36
249 (B10)	TXFD23	299 (AM16)	RXFD58	349 (C27)	TXFD110	399 (AK4)	RXETH4
250 (B9)	TXFD17	300 (AM17)	RXABT	350 (C26)	TXFD104	400 (AL4)	VDD

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Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
401 (AL5)	RXETH5	451 (G31)	VDD	501 (AE5)	TXD33	551 (K30)	RXD71
402 (AL6)	RXFD1	452 (F31)	TXD77	502 (AF5)	TXD36	552 (J30)	RXD74
403 (AL7)	RXFD8	453 (E31)	TXFBA5	503 (AG5)	EWRAP3	553 (H30)	RX_ER7
404 (AL8)	RXFD14	454 (D31)	VDD	504 (AH5)	RX_CLK30	554 (G30)	EWRAP7
405 (AL9)	RXFD19	455 (D30)	TXFD125	505 (AJ5)	CRS3	555 (F30)	TXFD127
406 (AL10)	RXFD25	456 (D29)	TXFD122	506 (AK5)	RXETH6	556 (E30)	TXFD126
407 (AL11)	VDD	457 (D28)	TXFD117	507 (AK6)	RXFD2	557 (E29)	TXFD123
408 (AL12)	RXFD36	458 (D27)	TXFD111	508 (AK7)	RXFD9	558 (E28)	TXFD118
409 (AL13)	RXFD42	459 (D26)	TXFD105	509 (AK8)	RXFD15	559 (E27)	TXFD112
410 (AL14)	RXFD48	460 (D25)	TXFD100	510 (AK9)	RXFD20	560 (E26)	TXFD106
411 (AL15)	RXFD53	461 (D24)	VDD	511 (AK10)	RXFD26	561 (E25)	TXFD101
412 (AL16)	RXFD59	462 (D23)	TXFD89	512 (AK11)	RXFD31	562 (E24)	TXFD95
413 (AL17)	SKIP	463 (D22)	TXFD83	513 (AK12)	RXFD37	563 (E23)	TXFD90
414 (AL18)	RXFDQ3	464 (D21)	TXFD77	514 (AK13)	RXFD43	564 (E22)	TXFD84
415 (AL19)	RXFD66	465 (D20)	TXFD71	515 (AK14)	RXFD49	565 (E21)	TXFD78
416 (AL20)	RXFD71	466 (D19)	TXFD66	516 (AK15)	RXFD54	566 (E20)	TXFD72
417 (AL21)	RXFD77	467 (D18)	TXFDQ3	517 (AK16)	RXFD60	567 (E19)	TXFD67
418 (AL22)	RXFD83	468 (D17)	TEST1	518 (AK17)	PASS	568 (E18)	TXFDQ4
419 (AL23)	RXFD89	469 (D16)	TXFD59	519 (AK18)	RXFDQ4	569 (E17)	TEST0
420 (AL24)	VDD	470 (D15)	TXFD53	520 (AK19)	RXFD67	570 (E16)	TXFD60
421 (AL25)	RXFD100	471 (D14)	TXFD48	521 (AK20)	RXFD72	571 (E15)	TXFD54
422 (AL26)	RXFD105	472 (D13)	TXFD42	522 (AK21)	RXFD78	572 (E14)	TXFD49
423 (AL27)	RXFD111	473 (D12)	TXFD36	523 (AK22)	RXFD84	573 (E13)	TXFD43
424 (AL28)	RXFD117	474 (D11)	VDD	524 (AK23)	RXFD90	574 (E12)	TXFD37
425 (AL29)	RXFD122	475 (D10)	TXFD25	525 (AK24)	RXFD95	575 (E11)	TXFD31
426 (AL30)	RXFD125	476 (D9)	TXFD19	526 (AK25)	RXFD101	576 (E10)	TXFD26
427 (AL31)	VDD	477 (D8)	TXFD14	527 (AK26)	RXFD106	577 (E9)	TXFD20
428 (AK31)	TEST4	478 (D7)	TXFD8	528 (AK27)	RXFD112	578 (E8)	TXFD15
429 (AJ31)	RXD44	479 (D6)	TXFD1	529 (AK28)	RXFD118	579 (E7)	TXFD9
430 (AH31)	RX_ER4	480 (D5)	FC5	530 (AK29)	RXFD123	580 (E6)	TXFD2
431 (AG31)	VDD	481 (E5)	FC6	531 (AK30)	RXFD126	581 (F6)	MDC
432 (AF31)	TXD46	482 (F5)	MDIO	532 (AJ30)	RXFD127	582 (G6)	TXD00
433 (AE31)	RXD52	483 (G5)	GTX_CLK0	533 (AH30)	RX_DV4	583 (H6)	RX_CLK01
434 (AD31)	VDD	484 (H5)	RX_CLK00	534 (AG30)	TX_CLK4	584 (J6)	RXD05
435 (AC31)	RX_DV5	485 (J5)	RXD06	535 (AF30)	TXD47	585 (K6)	RXD01
436 (AB31)	GND	486 (K5)	RXD02	536 (AE30)	TXD42	586 (L6)	CRS0
437 (AA31)	TXD57	487 (L5)	RXD00	537 (AD30)	TXD41	587 (M6)	GTX_CLK1
438 (Y31)	TXD52	488 (M5)	TX_ER1	538 (AC30)	RXD57	588 (N6)	RX_CLK10
439 (W31)	HD9	489 (N5)	COL1	539 (AB30)	LINK5#	589 (P6)	RXD15
440 (V31)	HD15	490 (P5)	RXD16	540 (AA30)	TX_EN5	590 (R6)	RXD10
441 (U31)	HD21	491 (R5)	RXD11	541 (Y30)	TXD51	591 (T6)	HD3
442 (T31)	HD27	492 (T5)	HD2	542 (W30)	HD8	592 (U6)	HA1
443 (R31)	RXD60	493 (U5)	HA0	543 (V30)	HD14	593 (V6)	HA7
444 (P31)	RXD65	494 (V5)	HA6	544 (U30)	HD20	594 (W6)	RESET#
445 (N31)	GND	495 (W5)	INT#	545 (T30)	HD26	595 (Y6)	TXD20
446 (M31)	GTX_CLK6	496 (Y5)	TXD21	546 (R30)	CRS6	596 (AA6)	TXD25
★ 447 (L31)	GTX_REF_CLK	497 (AA5)	TXD26	547 (P30)	RXD64	597 (AB6)	EWRAP2
448 (K31)	RXD72	498 (AB5)	TX_CLK2	548 (N30)	RX_CLK61	598 (AC6)	RX_CLK21
449 (J31)	RXD75	499 (AC5)	RX_ER2	549 (M30)	EWRAP6	599 (AD6)	TXD30
450 (H31)	RX_CLK71	500 (AD5)	TXD31	550 (L30)	TXD66	600 (AE6)	TXD32

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Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
601 (AF6)	TXD35	651 (F28)	TXFD119	701 (AH14)	VDDQ	751 (G13)	GND
602 (AG6)	GTX_CLK3	652 (F27)	TXFD113	702 (AH15)	GND	752 (G12)	VDD
603 (AH6)	RXD31	653 (F26)	TXFD107	703 (AH16)	VDD	753 (G11)	GND
604 (AJ6)	RXD30	654 (F25)	TXFD102	704 (AH17)	GND	754 (G10)	VDDQ
605 (AJ7)	RXFD10	655 (F24)	TXFD96	705 (AH18)	GND	755 (G9)	GND
606 (AJ8)	RXFD16	656 (F23)	TXFD91	706 (AH19)	VDD	756 (G8)	VDD
607 (AJ9)	RXFD21	657 (F22)	TXFD85	707 (AH20)	GND		
608 (AJ10)	RXFD27	658 (F21)	TXFD79	708 (AH21)	VDDQ		
609 (AJ11)	RXFD32	659 (F20)	TXFD73	709 (AH22)	GND		
610 (AJ12)	RXFD38	660 (F19)	TXFD68	710 (AH23)	VDD		
611 (AJ13)	RXFD44	661 (F18)	TXPAR	711 (AH24)	GND		
612 (AJ14)	RXFD50	662 (F17)	TEST2	712 (AH25)	VDDQ		
613 (AJ15)	RXFD55	663 (F16)	TXFD61	713 (AH26)	GND		
614 (AJ16)	RXFD61	664 (F15)	TXFD55	714 (AH27)	VDD		
615 (AJ17)	RXFA	665 (F14)	TXFD50	715 (AH28)	GND		
616 (AJ18)	RXPAR	666 (F13)	TXFD44	716 (AG28)	VDD		
617 (AJ19)	RXFD68	667 (F12)	TXFD38	717 (AF28)	GND		
618 (AJ20)	RXFD73	668 (F11)	TXFD32	718 (AE28)	VDDQ		
619 (AJ21)	RXFD79	669 (F10)	TXFD27	719 (AD28)	GND		
620 (AJ22)	RXFD85	670 (F9)	TXFD21	720 (AC28)	VDD		
621 (AJ23)	RXFD91	671 (F8)	TXFD16	721 (AB28)	GND		
622 (AJ24)	RXFD96	672 (F7)	TXFD10	722 (AA28)	VDDQ		
623 (AJ25)	RXFD102	673 (G7)	GND	723 (Y28)	GND		
624 (AJ26)	RXFD107	674 (H7)	VDD	724 (W28)	VDD		
625 (AJ27)	RXFD113	675 (J7)	GND	725 (V28)	VDDQ		
626 (AJ28)	RXFD119	676 (K7)	VDDQ	726 (U28)	GND		
627 (AJ29)	RXFD124	677 (L7)	GND	727 (T28)	VDD		
628 (AH29)	RXD47	678 (M7)	VDD	728 (R28)	GND		
629 (AG29)	LINK4#	679 (N7)	GND	729 (P28)	VDDQ		
630 (AF29)	TX_EN4	680 (P7)	VDDQ	730 (N28)	GND		
631 (AE29)	TXD43	681 (R7)	GND	731 (M28)	VDD		
632 (AD29)	TXD40	682 (T7)	VDD	732 (L28)	GND		
633 (AC29)	RXD56	683 (U7)	GND	733 (K28)	VDDQ		
634 (AB29)	COL5	684 (V7)	VDDQ	734 (J28)	GND		
635 (AA29)	TX_ER5	685 (W7)	VDD	735 (H28)	VDD		
636 (Y29)	TXD50	686 (Y7)	GND	736 (G28)	GND		
637 (W29)	HD7	687 (AA7)	VDDQ	737 (G27)	VDD		
638 (V29)	HD13	688 (AB7)	GND	738 (G26)	GND		
639 (U29)	HD19	689 (AC7)	VDD	739 (G25)	VDDQ		
640 (T29)	HD25	690 (AD7)	GND	740 (G24)	GND		
641 (R29)	HD31	691 (AE7)	VDDQ	741 (G23)	VDD		
642 (P29)	RXD63	692 (AF7)	GND	742 (G22)	GND		
643 (N29)	RX_ER6	693 (AG7)	VDD	743 (G21)	VDDQ		
644 (M29)	TX_CLK6	694 (AH7)	GND	744 (G20)	GND		
645 (L29)	TXD62	695 (AH8)	VDD	745 (G19)	VDD		
646 (K29)	RXD70	696 (AH9)	GND	746 (G18)	GND		
647 (J29)	RXD73	697 (AH10)	VDDQ	747 (G17)	GND		
648 (H29)	RX_DV7	698 (AH11)	GND	748 (G16)	VDD		
649 (G29)	TX_CLK7	699 (AH12)	VDD	749 (G15)	GND		
650 (F29)	TXFD124	700 (AH13)	GND	750 (G14)	VDDQ		

1. PIN FUNCTIONS

(1) Register interface

Pin Name	Pin No.	I/O	Function
HCS#	388	Input	Chip select When this signal is low level, registers within the chip can be accessed.
HRW	147	Input	Host read/write This is used when the host system accesses the register bus. A read access is executed when high level is input to this pin; a write access is executed when a low level is input.
HA[10:0]	273, 150, 19, 593, 494, 387, 272, 149, 18, 592, 493	Input	Register address When accessing a register within the μPD98433, addresses needed to select the port and register for access are given to HA[10:0]. The μPD98433 has a 32-bit wide register for each port. HA[10:8] specifies the port and HA[7:0] specifies the register address. The relationship between HA[10:8] and port numbers is as follows. Port 0 → HA[10:8] = 000B Port 1 → HA[10:8] = 001B Port 2 → HA[10:8] = 010B Port 3 → HA[10:8] = 011B Port 4 → HA[10:8] = 100B Port 5 → HA[10:8] = 101B Port 6 → HA[10:8] = 110B Port 7 → HA[10:8] = 111B
HD[31:0]	641, 85, 212, 331, 442, 545, 640, 84, 211, 330, 441, 544, 639, 83, 210, 329, 440, 543, 638, 82, 209, 328, 439, 542, 637, 208, 148, 17, 591, 492, 385, 270	I/O 3 states	Register data This is a bi-directional data bus for accessing on-chip registers of the μPD98433.
INT#	459	Output Open-drain	Interrupt signal This is an interrupt request signal. It becomes low level when an interrupt occurs. When an interrupt has occurred, this maintains low level until every interrupt status is cleared.
RESET#	594	Input	Hardware reset This is an asynchronous reset signal. Immediately after a hardware reset, all registers are set to default values and every FIFO and every counter is cleared.
HACK#	271	Output 3 states	Register data acknowledge On a register read operation, this shows that data at HD[31:0] is valid. When this signal is low level, data that was read exists at HD[31:0]. On a register write operation, this shows that the write operation completed.
HCLK	386	Input	Register interface clock This is synchronization clock input for register access. Its maximum frequency is 62.5 MHz.

(2) FIFO interface

(1/3)

Pin Name	Pin No.	I/O	Function
RXFCK	52	Input	Receive FIFO bus clock This is the reference clock for RXFCKOUT output. Its maximum frequency is 125 MHz. Give it the same frequency as TXFCK.
RXFCKOUT	316	Output	Receive FIFO bus clock output A copy of RXFCK is output. The FIFO bus performs receive operations in synchronization with RXFCKOUT.
TXFCK	115	Input	Transmit FIFO bus clock The FIFO bus performs transmit operations in synchronization with TXFCK. The maximum frequency is 125 MHz. Give this the same frequency as RXFCK.
RXFEN#	38	Input	FIFO bus receive enable When this signal becomes low level, the receive FIFO bus interface is enabled and it becomes possible to read from the receive FIFO.
TXFEN#	129	Input	FIFO bus transmit enable When this signal becomes low level, the transmit FIFO bus interface is enabled and it becomes possible to write to the transmit FIFO.
RXFPT[2:0]	168, 288, 167	Output 3 states	Receive port number On a receive FIFO read access, this shows the port number where receive data is output. The relationship between RXFPT[2:0] and port numbers is shown below. Port 0 → RXFPT[2:0] = 000B Port 1 → RXFPT[2:0] = 001B Port 2 → RXFPT[2:0] = 010B Port 3 → RXFPT[2:0] = 011B Port 4 → RXFPT[2:0] = 100B Port 5 → RXFPT[2:0] = 101B Port 6 → RXFPT[2:0] = 110B Port 7 → RXFPT[2:0] = 111B
TXFPT[2:0]	253, 371, 254	Input	Transmit port number On a transmit FIFO write access, this shows the port number of the transmit FIFO to which to write transmit data. The relationship between TXFPT[2:0] and port numbers is shown below. Port 0 → TXFPT[2:0] = 000B Port 1 → TXFPT[2:0] = 001B Port 2 → TXFPT[2:0] = 010B Port 3 → TXFPT[2:0] = 011B Port 4 → TXFPT[2:0] = 100B Port 5 → TXFPT[2:0] = 101B Port 6 → TXFPT[2:0] = 110B Port 7 → TXFPT[2:0] = 111B

(2/3)

Pin Name	Pin No.	I/O	Function
TXFD[127:0]	555, 556, 455, 650, 557, 456, 347, 230, 651, 558, 457, 348, 231, 106, 652, 559, 458, 349, 232, 107, 653, 560, 459, 350, 233, 654, 561, 460, 351, 234, 109, 655, 562, 352, 235, 110, 656, 563, 462, 353, 236, 111, 657, 564, 463, 354, 237, 112, 658, 565, 464, 355, 238, 113, 659, 566, 465, 356, 239, 660, 567, 466, 357, 240, 242, 117, 663, 570, 469, 360, 243, 118, 664, 571, 470, 361, 244, 665, 572, 471, 362, 245, 120, 666, 573, 472, 363, 246, 121, 667, 574, 473, 364, 247, 122, 668, 575, 365, 248, 123, 669, 576, 475, 366, 249, 124, 670, 577, 476, 367, 250, 671, 578, 477, 368, 251, 126, 672, 579, 478, 369, 252, 127, 5, 135, 580, 479, 370	Input	Transmit FIFO data bus This provides the 128-bit wide data bus of the transmit FIFO bus interface.
RXFD[127:0]	532, 531, 426 ,627, 530, 425, 312, 191, 626, 529, 424, 311, 190, 61, 625, 528, 423, 310, 189, 60, 624, 527, 422, 309, 188, 623, 526, 421, 308, 187, 58, 622, 525, 307, 186, 57, 621, 524, 419, 306, 185, 56, 620, 523, 418, 305, 184, 55, 619, 522, 417, 304, 183, 54, 618, 521, 416, 303, 182, 617, 520, 415, 302, 181, 179, 50, 614, 517, 412, 299, 178, 49, 613, 516, 411, 298, 177, 612, 515, 410, 297, 176, 47, 611, 514, 409, 296, 175, 46, 610, 513, 408, 295, 174, 45, 609, 512, 294, 173, 44, 608, 511, 406, 293, 172, 43, 607, 510, 405, 292, 171, 606, 509, 404, 291, 170, 41, 605, 508, 403, 290, 169, 40, 30, 162, 507, 402, 289	Output 3 states	Receive FIFO data bus This provides the 128-bit wide data bus of the receive FIFO bus interface.

(3/3)

Pin Name	Pin No.	I/O	Function
RXFDQ[4:0]	519, 414, 301, 180, 51	Output 3 states	Receive data attributes This shows the attributes of receive data that is on the FIFO bus. On a read access of the receive FIFO, it outputs the attributes of receive data that was output at RXFD[127:0]. See **Table 3-2** in the **μPD98433 User's Manual (S15212E)** for the output patterns of RXFDQ[4:0]
TXFDQ[4:0]	568, 467, 358, 241, 116	Input	Transmit data attributes This shows the attributes of transmit data that is on the FIFO bus. On a write access to the transmit FIFO, it inputs the attributes of transmit data that was placed at TXFD[127:0]. See **Table 3-1** in the **μPD98433 User's Manual (S15212E)** for the input patterns of TXFDQ[4:0].
TXFBA[7:0]	343, 345, 453, 228, 103, 346, 229, 104	Output 3 states	Transmit FIFO buffer available When this signal is high level, it shows that the space within the transmit FIFO for writing transmit data is empty. This signal becomes low level if the amount of data in the transmit FIFO exceeds the value set in the TFWMH field of the TFIC1 register. A TXFBA signal is established for each port and TXFBA[n] indicates the TXFBA signal of port n. Output is asynchronous.
RXFA	615	Output 3 states	Receive frame available When this signal is high level, it shows that at least 1 packet of a receive data stream that can be transferred to the host system has been prepared and placed in the port shown by RXFPT or that data stored in the FIFO exceeds the threshold value set in the THRX field of the RFIC3 register.
PASS	518	Input	Receive frame pass On a read access from the receive FIFO, this is the signal that is input to begin the transfer of receive data of the port that currently is on the FIFO bus.
SKIP	413	Input	Receive frame skip On a read access from the receive FIFO, this signal is input to skip the port that currently is on the FIFO bus and read from the next port.
FC[7:0]	4, 481, 480, 374, 372, 255, 130, 258	Input	Flow control frame generation This signal designates the transmission of flow control packets by port. Besides using register settings for automatically generating them, flow control packet transmission can be designated directly using this pin.
RXPAR	616	Output 3 states	Receive parity bit This shows the parity with 128-bit receive data. Even or odd parity can be selected according to the register setting.
TXPAR	661	Input	Transmit parity bit This shows the parity with 128-bit transmit data. Even or odd parity can be selected according to the register setting.
RXABT	300	Input	Receive abort This signal designates removing receive FIFO data from within the receive FIFO before output to the receive FIFO interface.
RXETH[7:0]	31, 506, 401, 399, 287, 166, 37, 285	Output	Receive FIFO status display For each port, this signal is asserted when receive FIFO data exceeds a threshold (RXETH field of RFIC3 register).

(3) Physical layer interface

(1/5)

Pin Name	Pin No.	I/O	Function
TX_CLK[7:0]	649, 644, 325, 534, 281, 498, 144, 139	Input	MII transmit clock This transmit clock input is needed in order to output transmit data to the PHY device connected to each port. Each of TXD7[3:0] to TXD0[3:0], which is the transmit data from each port, and TXEN[7:0], which shows that transmit data at TXD is valid, are output by port in synchronization with this clock. In MII mode, a 2.5 MHz clock is input on 10 Mbps operation and a 25 MHz clock on 100 Mbps operation. In this mode, TXD and TXEN are output in synchronization with the rise of TX_CLK. In GMII or TBI mode, fix TX_CLK to high level or low level. For unused ports, fix TX_CLK to high level or low level.
★ GTX_CLK[7:0]	340, 446, 79, 201, 602, 21, 587, 483	Output	Transmit clock for 1000M This transmit clock is output with the transmit data to the PHY device connected to each port. Each of TXD7[3:0] to TXD0[3:0], which is the transmit data from each port, and TXEN[7:0], which shows that transmit data at TXD is valid, are output by port in synchronization with this clock. In GMII mode, this functions as GTX_CLK. In TBI mode, it functions as PMA_TX_CLK.
★ GTX_REF_CLK	447	Input	Transmit reference clock This reference clock is used for the internal operation and GTX_CLK[7:0] production. Always give the clock that the frequency is 125 MHz.
TXD0[7:0]	138, 7, 375, 260, 137, 259, 136, 582	Output	Transmit data (Port 0) This is transmit data output for the PHY device of port 0. In MII mode, the lower 4 bits are used to output a nibble (4 bits) of transmit data in synchronization with the rising edge of TX_CLK0. In GMII or TBI mode, this outputs 8-bit wide transmit data in synchronization with the rising edge of GTX_CLK0.
TXD1[7:0]	266, 143, 12, 265, 142, 11, 141, 10	Output	Transmit data (Port 1) This is transmit data output for the PHY device of port 1. In MII mode, the lower 4 bits are used to output a nibble (4 bits) of transmit data in synchronization with the rising edge of TX_CLK1. In GMII or TBI mode, this outputs 8-bit wide transmit data in synchronization with the rising edge of GTX_CLK1.
TXD2[7:0]	390, 497, 596, 151, 274, 389, 496, 595	Output	Transmit data (Port 2) This is transmit data output for the PHY device of port 2. In MII mode, the lower 4 bits are used to output a nibble (4 bits) of transmit data in synchronization with the rising edge of TX_CLK2. In GMII or TBI mode, this outputs 8-bit wide transmit data in synchronization with the rising edge of GTX_CLK2.
TXD3[7:0]	395, 502, 601, 394, 501, 600, 500, 599	Output	Transmit data (Port 3) This is transmit data output for the PHY device of port 3. In MII mode, the lower 4 bits are used to output a nibble (4 bits) of transmit data in synchronization with the rising edge of TX_CLK3. In GMII or TBI mode, this outputs 8-bit wide transmit data in synchronization with the rising edge of GTX_CLK3.

(2/5)

Pin Name	Pin No.	I/O	Function
TXD4[7:0]	535, 432, 321, 202, 631, 536, 537, 632	Output	Transmit data (Port 4) This is transmit data output for the PHY device of port 4. In MII mode, the lower 4 bits are used to output a nibble (4 bits) of transmit data in synchronization with the rising edge of TX_CLK4. In GMII or TBI mode, this outputs 8-bit wide transmit data in synchronization with the rising edge of GTX_CLK4.
TXD5[7:0]	437, 326, 207, 80, 327, 438, 541, 636	Output	Transmit data (Port 5) This is transmit data output for the PHY device of port 5. In MII mode, the lower 4 bits are used to output a nibble (4 bits) of transmit data in synchronization with the rising edge of TX_CLK5. In GMII or TBI mode, this outputs 8-bit wide transmit data in synchronization with the rising edge of GTX_CLK5.
TXD6[7:0]	89, 550, 336, 217, 90, 645, 218, 91	Output	Transmit data (Port 6) This is transmit data output for the PHY device of port 6. In MII mode, the lower 4 bits are used to output a nibble (4 bits) of transmit data in synchronization with the rising edge of TX_CLK6. In GMII or TBI mode, this outputs 8-bit wide transmit data in synchronization with the rising edge of GTX_CLK6.
TXD7[7:0]	452, 341, 222, 342, 223, 96, 224, 97	Output	Transmit data (Port 7) This is transmit data output for the PHY device of port 7. In MII mode, the lower 4 bits are used to output a nibble (4 bits) of transmit data in synchronization with the rising edge of TX_CLK7. In GMII or TBI mode, this outputs 8-bit wide transmit data in synchronization with the rising edge of GTX_CLK7.
TX_EN[7:0]	94, 216, 540, 630, 280, 275, 381, 261	Output	Transmit enable/transmit data bit 8 The function of this signal differs depending on the operation mode. (1) In GMII or MII mode This signal shows whether or not transmit data (TXD) is valid for each port. It is high level from the first data showing the preamble until the last data of a transmit frame is output. (2) In TBI mode This functions as bit 8 of the transmit data of each port (TX[8]).
TX_ER[7:0]	221, 335, 635, 74, 157, 152, 488, 376	Output	MII transmit error/transmit data bit 9 The function of this signal differs depending on the operation mode. (1) In GMII or MII mode This signal shows that an error occurred in the μPD98433. (2) In TBI mode This functions as bit 9 of the transmit data of each port (TX[9]).
RX_CLK[7:0]0	339, 334, 78, 200, 504, 22, 588, 484	Input	Receive clock This is receive clock input given by a PHY device. Each of RXD7[7:0] to RXD0[7:0], which is the receive data from each port, and RX_DV[7:0], which shows that receive data at RXD is valid, are output in synchronization with this clock. In TBI mode, this is a 62.5 MHz clock input pin. In this case, input RX_CLKn0 and RX_CLKn1 in an inverse phase relation. In TBI mode single phase use, this is 125 MHz clock input. In GMII or MII mode, a 125 MHz clock is input on 1000 Mbps operation, a 25 MHz clock on 100 Mbps operation, and a 2.5 MHz clock on 10 Mbps operation. For unused ports, fix RX_CLKn0 to high level or low level.

(3/5)

Pin Name	Pin No.	I/O	Function
RX_CLK[7:0]1	450, 548, 205, 319, 397, 598, 14, 583	Input	Receive clock To input a 62.5 MHz clock in TBI mode, input the clock in inverse phase to RX_CLK[7:0]0.
RXD0[7:0]	378, 485, 584, 264, 379, 486, 585, 487	Input	Receive data (Port 0) This is receive data input from the PHY device of port 0. In MII mode, the lower 4 bits are used to input a nibble (4 bits) of receive data on the rising edge of RX_CLK0. In GMII mode, this inputs 8-bit wide receive data on the rising edge of RX_CLK00. In TBI mode, it inputs 8-bit wide receive data on the rising edges of RXCLK00 and RX_CLK01.
RXD1[7:0]	383, 490, 589, 146, 269, 384, 491, 590	Input	Receive data (Port 1) This is receive data input from the PHY device of port 1. In MII mode, the lower 4 bits are used to input a nibble (4 bits) of receive data on the rising edge of RX_CLK1. In GMII mode, this inputs 8-bit wide receive data on the rising edge of RX_CLK10. In TBI mode, it inputs 8-bit wide receive data on the rising edges of RX_CLK10 and RX_CLK11.
RXD2[7:0]	277, 154, 23, 278, 155, 24, 279, 156	Input	Receive data (Port 2) This is receive data input from the PHY device of port 2. In MII mode, the lower 4 bits are used to input a nibble (4 bits) of receive data on the rising edge of RX_CLK2. In GMII mode, this inputs 8-bit wide receive data on the rising edge of RX_CLK20. In TBI mode, it inputs 8-bit wide receive data on the rising edges of RX_CLK20 and RX_CLK21.
RXD3[7:0]	28, 398, 283, 160, 284, 161, 603, 604	Input	Receive data (Port 3) This is receive data input from the PHY device of port 3. In MII mode, the lower 4 bits are used to input a nibble (4 bits) of receive data on the rising edge of RX_CLK3. In GMII mode, this inputs 8-bit wide receive data on the rising edge of RX_CLK30. In TBI mode, it inputs 8-bit wide receive data on the rising edges of RX_CLK30 and RX_CLK31.
RXD4[7:0]	628, 199, 318, 429, 71, 198, 317, 70	Input	Receive data (Port 4) This is receive data input from the PHY device of port 4. In MII mode, the lower 4 bits are used to input a nibble (4 bits) of receive data on the rising edge of RX_CLK4. In GMII mode, this inputs 8-bit wide receive data on the rising edge of RX_CLK40. In TBI mode, it inputs 8-bit wide receive data on the rising edges of RX_CLK40 and RX_CLK41.

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Pin Name	Pin No.	I/O	Function
RXD5[7:0]	538, 633, 77, 204, 323, 433, 322, 203	Input	Receive data (Port 5) This is receive data input from the PHY device of port 5. In MII mode, the lower 4 bits are used to input a nibble (4 bits) of receive data on the rising edge of RX_CLK5. In GMII mode, this inputs 8-bit wide receive data on the rising edge of RX_CLK50. In TBI mode, it inputs 8-bit wide receive data on the rising edges of RX_CLK50 and RX_CLK51.
RXD6[7:0]	214, 333, 444, 547, 642, 213, 332, 443	Input	Receive data (Port 6) This is receive data input from the PHY device of port 6. In MII mode, the lower 4 bits are used to input a nibble (4 bits) of receive data on the rising edge of RX_CLK6. In GMII mode, this inputs 8-bit wide receive data on the rising edge of RX_CLK60. In TBI mode, it inputs 8-bit wide receive data on the rising edges of RX_CLK60 and RX_CLK61.
RXD7[7:0]	219, 338, 449, 552, 647, 448, 551, 646	Input	Receive data (Port 7) This is receive data input from the PHY device of port 7. In MII mode, the lower 4 bits are used to input a nibble (4 bits) of receive data on the rising edge of RX_CLK7. In GMII mode, this inputs 8-bit wide receive data on the rising edge of RX_CLK70. In TBI mode, it inputs 8-bit wide receive data on the rising edges of RX_CLK70 and RX_CLK71.
RX_DV[7:0]	648, 87, 435, 533, 159, 392, 268, 263	Input	Receive data valid/receive data bit 8 The function of this signal differs depending on the operation mode. (1) In GMII or MII mode When this signal is high level, it shows that data at RXD is valid for each port. (2) In TBI mode This functions as bit 8 of the receive data of each port (RX[8]). For unused ports, fix RX_DV to low level.
RX_ER[7:0]	553, 643, 324, 430, 282, 499, 145, 140	Input	Receive error/receive data bit 9 The function of this signal differs depending on the operation mode. (1) In GMII or MII mode This is an input signal for detecting errors that occurred on a PHY device while receiving at each port. (2) In TBI mode This functions as bit 9 of the receive data of each port (RX[9]). For unused ports, fix RX_ER to low level.
CRS[7:0]	337, 546, 76, 197, 505, 25, 16, 586	Input	Carrier sense/SIGDET The function of this signal differs depending on the operation mode. (1) In GMII or MII mode This is the carrier sense signal input from the PHY device connected to each port. (2) In TBI mode This functions as SIGDET of each port. For unused ports, fix CRS to low level.

(5/5)

Pin Name	Pin No.	I/O	Function
MDC	581	Output	MII management clock This is the MII serial management data transfer clock.
COL[7:0]	220, 215, 634, 73, 27, 153, 489, 377	Input	Collision This is collision signal input detected by the PHY device connected to each port. For unused ports, fix COL to low level. This is not used in TBI mode.
MDIO	482	I/O 3 states	MII management data This is a bi-directional MII serial management data signal.
EWRAP[7:0]	554, 549, 206, 320, 503, 597, 13, 8	Output	Loopback designation This signal designates realization of a loopback configuration for the physical layer device on which an externally connected TBI is implemented for each port. It is the signal for designating switching the data flow within a physical layer device to a loop configuration.
★ LINK[7:0]#	93, 88, 539, 629, 158, 276, 267, 262	Output Open-drain	LED pins These are pins for LEDs that show that a link has been established in TBI mode for each port. Output is asynchronous.

(4) JTAG pins (This function can be supported upon customer request)

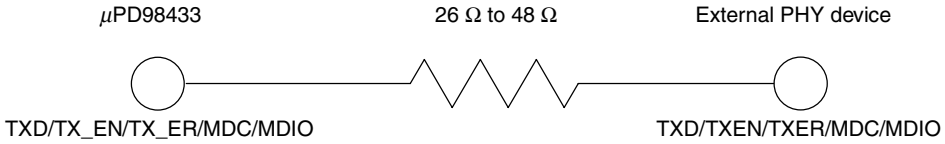
Pin Name	Pin No.	I/O	Function
TMS	63	Input	JTAG test mode select This signal controls a boundary scan state machine. The pin is not pulled up internally.
TDI	313	Input	JTAG test data input This signal is the serial data input for a boundary scan. The pin is not pulled up internally.
TDO	193	Output 3 states	JTAG test data output This signal is the serial data output for a boundary scan.
TCK	192	Input	JTAG test clock This is clock input that is used to synchronize test data I/O. The pin is not pulled up internally.
TRST#	314	Input	JTAG reset When this signal is made low level, a boundary scan operation is reset. This must be high level during a boundary scan operation. It is low level on a normal operation. The pin is not pulled up internally.

(5) Test pins and power supply pins

Pin Name	Pin No.	I/O	Function
VDD	756, 752, 748, 745, 741, 737, 735, 731, 727, 724, 720, 716, 714, 710, 706, 703, 699, 695, 693, 689, 685, 682, 678, 674, 474, 461, 454, 451, 434, 431, 427, 420, 407, 400, 396, 393, 380, 373, 128, 119, 114, 105, 95, 86, 81, 72, 62, 53, 48, 39, 29, 20, 15, 6	–	Power supply (+2.5 V)
GND	755, 753, 751, 749, 747, 746, 744, 742, 740, 738, 736, 734, 732, 730, 728, 726, 723, 721, 719, 717, 715, 713, 711, 709, 707, 705, 704, 702, 700, 698, 696, 694, 692, 690, 688, 686, 683, 681, 679, 677, 675, 673, 445, 436, 391, 382, 344, 315, 286, 257, 256, 227 to 225, 196 to 194, 165 to 163, 134 to 131, 102 to 98, 69 to 65, 36 to 32, 3 to 1	–	Ground (0 V)
VDDQ	754, 750, 743, 739, 733, 729, 725, 722, 718, 712, 708, 701, 697, 691, 687, 684, 680, 676, 125, 108, 92, 75, 59 ,42, 26, 9	–	Power supply for I/O buffer for physical layer interface This is the power supply for the I/O buffer used for the physical layer interface. Supply 3.3 V.
TEST[3, 1, 0]	64, 468, 569	Output	Test pins These are pins for device test. They are not used in normal operation.
TEST[5, 4, 2]	359, 428, 662	Input	Test pins These are pins for device test. Always fix these pins to low level.

(6) μPD98433 MII output signal pin connection

To connect a PHY device to the MII output signals (TXD, TX_EN, TX_ER, MDC, MDIO), connect a 26 Ω to 48 Ω series resistor to each MII output signal to make the drive capacity conform with the IEEE802.3 standard.



2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}		−0.5 to +3.6	V
Power supply voltage for physical layer interface	V_{DDQ}		−0.5 to +4.6	V
I/O voltage	V_{IO}		−0.5 to +3.6	V
I/O voltage for physical layer interface	V_{IOQ}		−0.5 to +4.6	V
Maximum power consumption	P_{MAX}		TBD	W
Operating ambient temperature	T_A		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	Power supply voltage	V_{DD}		2.375	2.500	2.625	V
★	Power supply voltage for physical layer interface	V_{DDQ}		3.135	3.300	3.465	V
	Operating ambient temperature	T_A		0		+70	°C

DC Characteristics (T_A = 0 to +70°C, V_{DD} = +2.5 V ±5%) (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LI}		−10		+10	μA
Off-state current	I_{OZ}		−10		+10	μA
Operating current	I_{DD}		TBD		TBD	mA
Input voltage, low	V_{IL}	Register interface FIFO interface	0		0.7	V
		MII interface	0		0.8	V
		GMII interface	0		0.9	V
		TBI interface	0		0.8	V
		JTAG signal	0		0.7	V
Input voltage, high	V_{IH}	Register interface FIFO interface	1.7		V_{DD}	V
★		MII interface	2.0		V_{DDQ}	V
★		GMII interface	1.7		V_{DDQ}	V
★		TBI interface	2.0		V_{DDQ}	V
		JTAG signal	1.7		V_{DD}	V

(2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, low	V_{OL}	Register interface FIFO interface (I_{OL} = 6 mA, I_{OL} = 12 mA only for RXFCKOUT)	0		0.4	V
		MII interface (I_{OL} = 4 mA)	0		0.4	V
		GMII interface (I_{OL} = 1 mA)	0		0.5	V
		TBI interface (I_{OL} = 1 mA)	0		0.6	V
		JTAG signal (I_{OL} = 6 mA)	0		0.4	V
Output voltage, high	V_{OH}	Register interface FIFO interface (I_{OH} = –6 mA, I_{OH} = –12 mA only for RXFCKOUT)	1.7		V_{DD}	V
		MII interface (I_{OH} = –4 mA)	2.4		V_{DDQ}	V
		GMII interface (I_{OH} = –1 mA)	2.1		V_{DDQ}	V
		TBI interface (I_{OH} = –0.4 mA)	2.2		V_{DDQ}	V
		JTAGT signal (I_{OH} = –6 mA)	1.7		V_{DD}	V

Capacitance (T_A = 25°C, f_C = 1 MHz)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	V_I = 0 V	TBD		TBD	pF
I/O capacitance	C_{IO}	V_{IO} = 0 V	TBD		TBD	pF

AC Characteristics (T_A = 0 to +70°C, V_{DD} = +2.5 V ±5%)

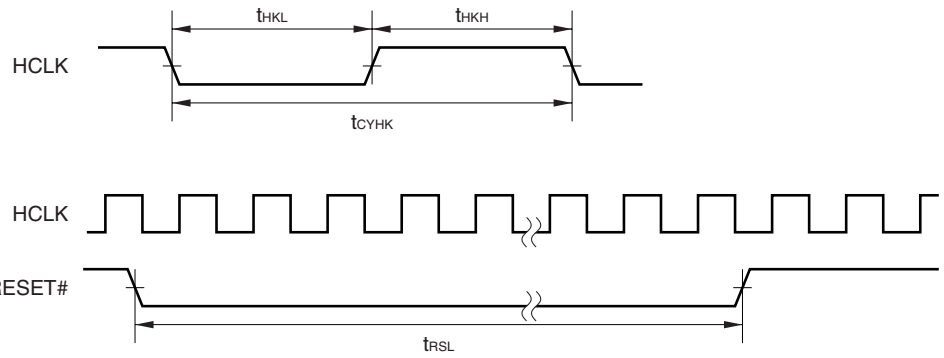
AC test conditions

- Load conditions: 15 pF (MII interface)
  10 pF (GMII interface)
  5 pF (TBI interface)
  15 pF (Other than above)
- Input pulse level: 0.4 V to 2.4 V (MII, GMII, TBI interface)
  0.3 V to 2.1 V (Other than above)
- ★ Measurement reference level: (V_{DDQ} – 5 %)/2 V (MII, GMII, TBI interface)
  (V_{DD} – 5 %)/2 V (Other than above)

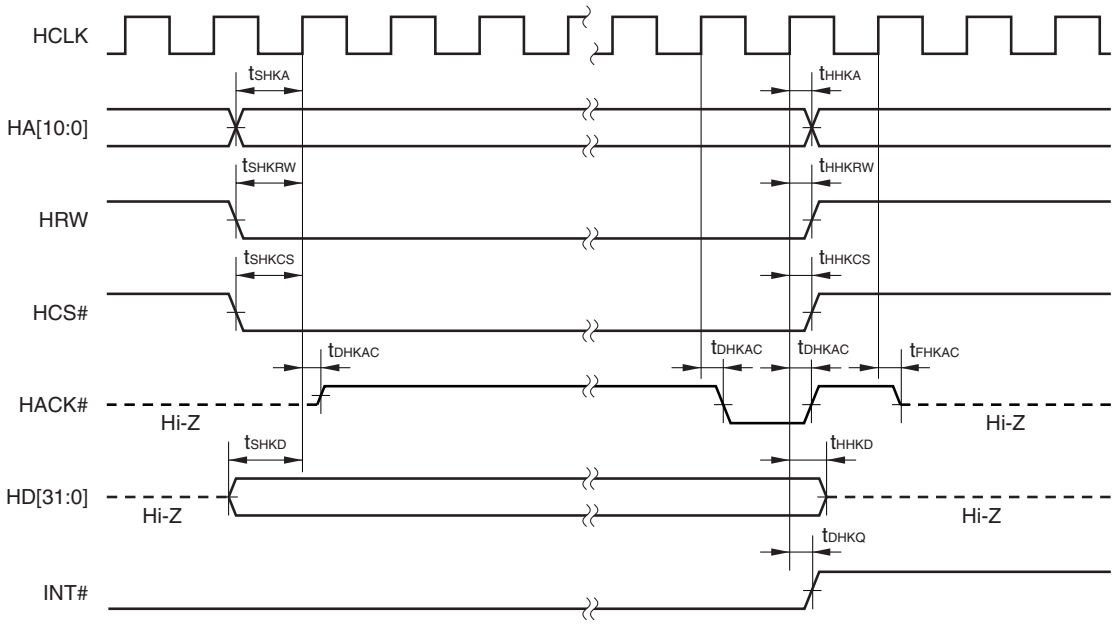
Register Bus Interface Timing

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
HCLK clock width	t_{CYHK}		16			ns
HCLK low-level width	t_{HKL}		7			ns
HCLK high-level width	t_{HKH}		7			ns
RESET# pulse width	t_{RSL}		16t_{CYHK}			ns
HA[10:0] setup time	t_{SHKA}		5			ns
HA[10:0] hold time	t_{HHKA}		5			ns
HRW setup time	t_{SHKRW}		5			ns
HRW hold time	t_{HHKRW}		5			ns
HSC# setup time	t_{SHKCS}		5			ns
HCS# hold time	t_{HHKCS}		5			ns
HACK# output delay time	t_{DHKAC}		0		7	ns
HACK# float time	t_{FHKAC}		0		7	ns
HD[31:0] output delay time	t_{DHKD}		0		7	ns
HD[31:0] setup time	t_{SHKD}		5			ns
HD[31:0] hold time	t_{HHKD}		5			ns
HD[31:0] float time	t_{FHKD}		0		7	ns
INT# output delay time	t_{DHKQ}		TBD		TBD	μs

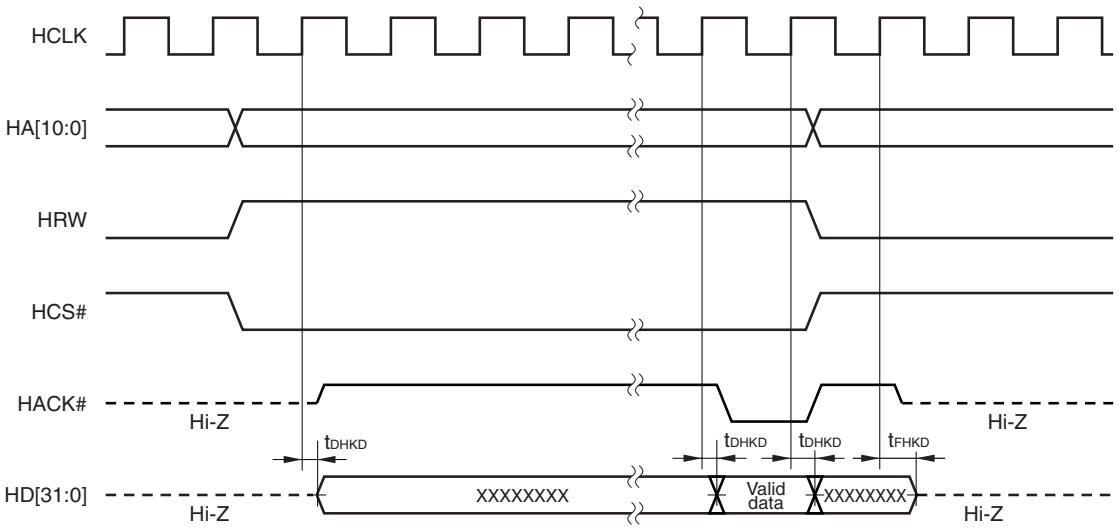
(1) HCLK timing



(2) Register bus interface write timing



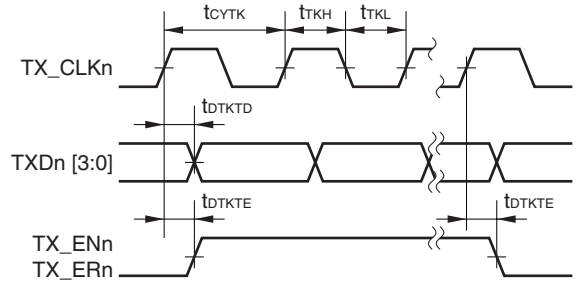
(3) Register bus interface read timing



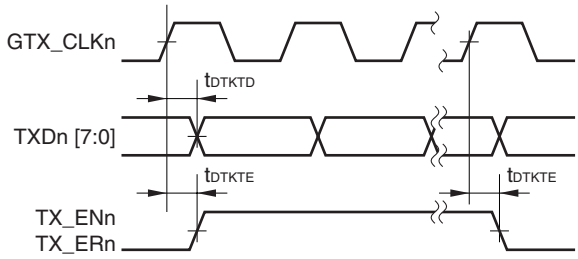
Ethernet Transmit Interface Timing

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	TXDn[7:0] delay time	t_{DTKTD}	C_L = 20 pF, MII mode			20.0	ns
			C_L = 20 pF, GMII mode	1.0		4.5	ns
			C_L = 20 pF, TBI mode	1.0		4.5	ns
	TX_ENn, TX_ERn delay time	t_{DTKTE}	C_L = 20 pF, MII mode			20.0	ns
			C_L = 20 pF, GMII mode	1.0		4.5	ns
			C_L = 20 pF, TBI mode	1.0		4.5	ns
	TX_CLKn clock width	t_{CYTK}	10M MII mode	400 – 100ppm	400	400 + 100ppm	ns
			100M MII mode	40 – 100ppm	40	40 + 100ppm	ns
★	TX_CLKn high-level width	t_{TKH}	10M MII mode	160	200	240	ns
			100M MII mode	16	20	24	ns
★	TX_CLKn low-level width	t_{TKL}	10M MII mode	160	200	240	ns
			100M MII mode	16	20	24	ns
★	GTX_REF_CLK clock width	t_{CYGTK}	GMII mode	8 – 100ppm	8	8 + 100ppm	ns
			TBI mode	8 – 100ppm	8	8 + 100ppm	ns
★	GTX_REF_CLK high-level width	t_{TGKH}		3.4		4.6	ns
★	GTX_REF_CLK low-level width	t_{TGKL}		3.4		4.6	ns

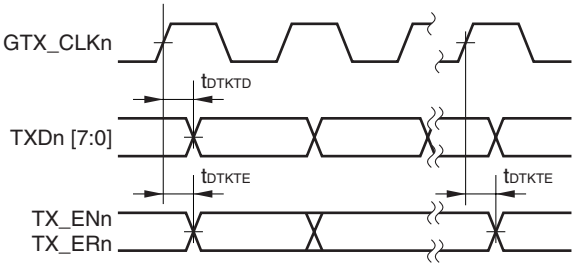
(a) MII mode



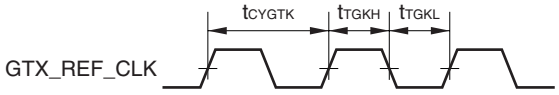
(b) GMII mode



(c) TBI mode



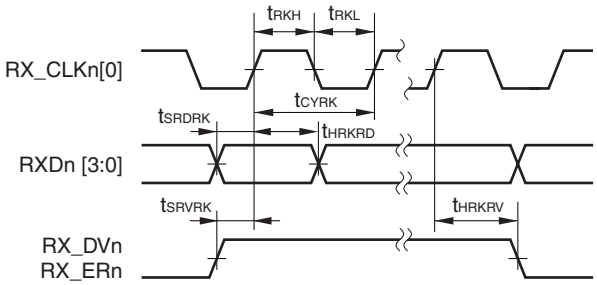
★ (d) GTX_REF_CLK



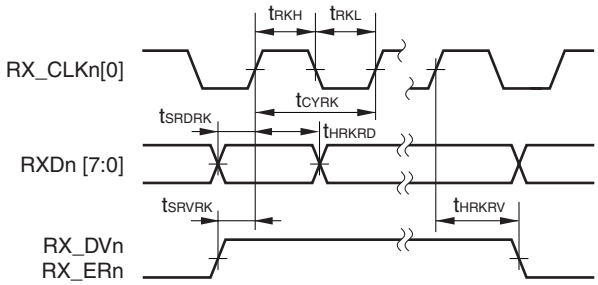
Ethernet Receive Interface Timing

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	RXDn[7:0] setup time	t_{SRDRK}	MII mode	10			ns
			GMII mode	2.0			ns
			TBI mode (including RX_DVn, RX_ERn)	2.5			ns
	RXDn[7:0] hold time	t_{HRKRD}	MII mode	10			ns
			GMII mode	0.0			ns
			TBI mode (including RX_DVn, RX_ERn)	1.5			ns
	Receive signal setup time	t_{SRVRK}	MII mode	10			ns
			GMII mode	2.0			ns
	Receive signal hold time	t_{HRKRV}	MII mode	10			ns
			GMII mode	0.0			ns
	RX_CLKn[0] clock width	t_{CYRK}	10M MII mode	400 – 100ppm	400	400 + 100ppm	ns
			100M MII mode	40 – 100ppm	40	40 + 100ppm	ns
			GMII mode	8 – 100ppm	8	8 + 100ppm	ns
			TBI mode	16 – 100ppm	16	16 + 100ppm	ns
	RX_CLKn[0] high-level width	t_{RKH}	10M MII mode	160	200		ns
			100M MII mode	16	20		ns
★			GMII mode	3.4	4		ns
			TBI mode	6.4		9.6	ns
	RX_CLKn[0] low-level width	t_{RKL}	10M MII mode	160	200		ns
			100M MII mode	16	20		ns
★			GMII mode	3.4	4		ns
			TBI mode	6.4		9.6	ns
★	RX_CLKn[1] clock width	t_{CYRK}	TBI mode	16 – 100ppm	16	16 + 100ppm	ns
★	RX_CLKn[1] high-level width	t_{RKH}	TBI mode	6.4		9.6	ns
★	RX_CLKn[1] low-level width	t_{RKL}	TBI mode	6.4		9.6	ns
	RX_CLKn[1] clock skew	t_{DRKRK}		7.5		8.5	ns

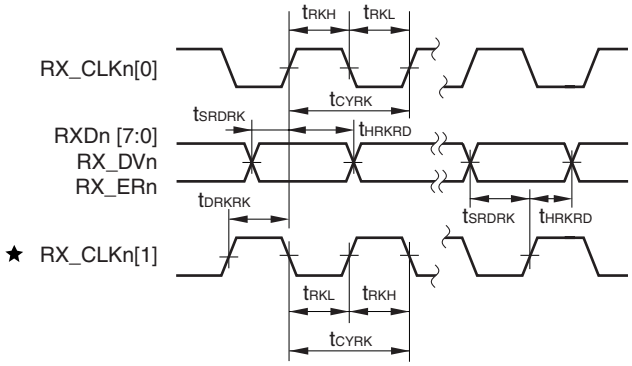
(a) MII mode



(b) GMII mode

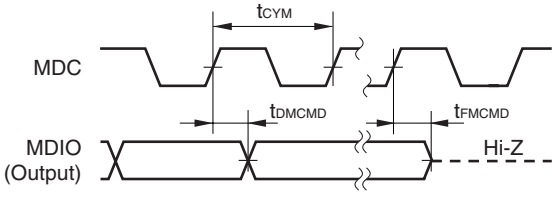


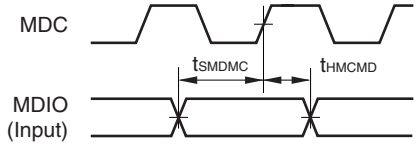
(c) TBI mode



MII Management Interface Timing

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
MDC cycle	t_{CYM}		400		1,080	ns
MDIO delay time	t_{DMCMD}		10		TBD	ns
MDIO float time	t_{FMCMD}		10		TBD	ns
MDIO setup time	t_{SMDMC}		100			ns
MDIO hold time	t_{HMCMD}		0			ns



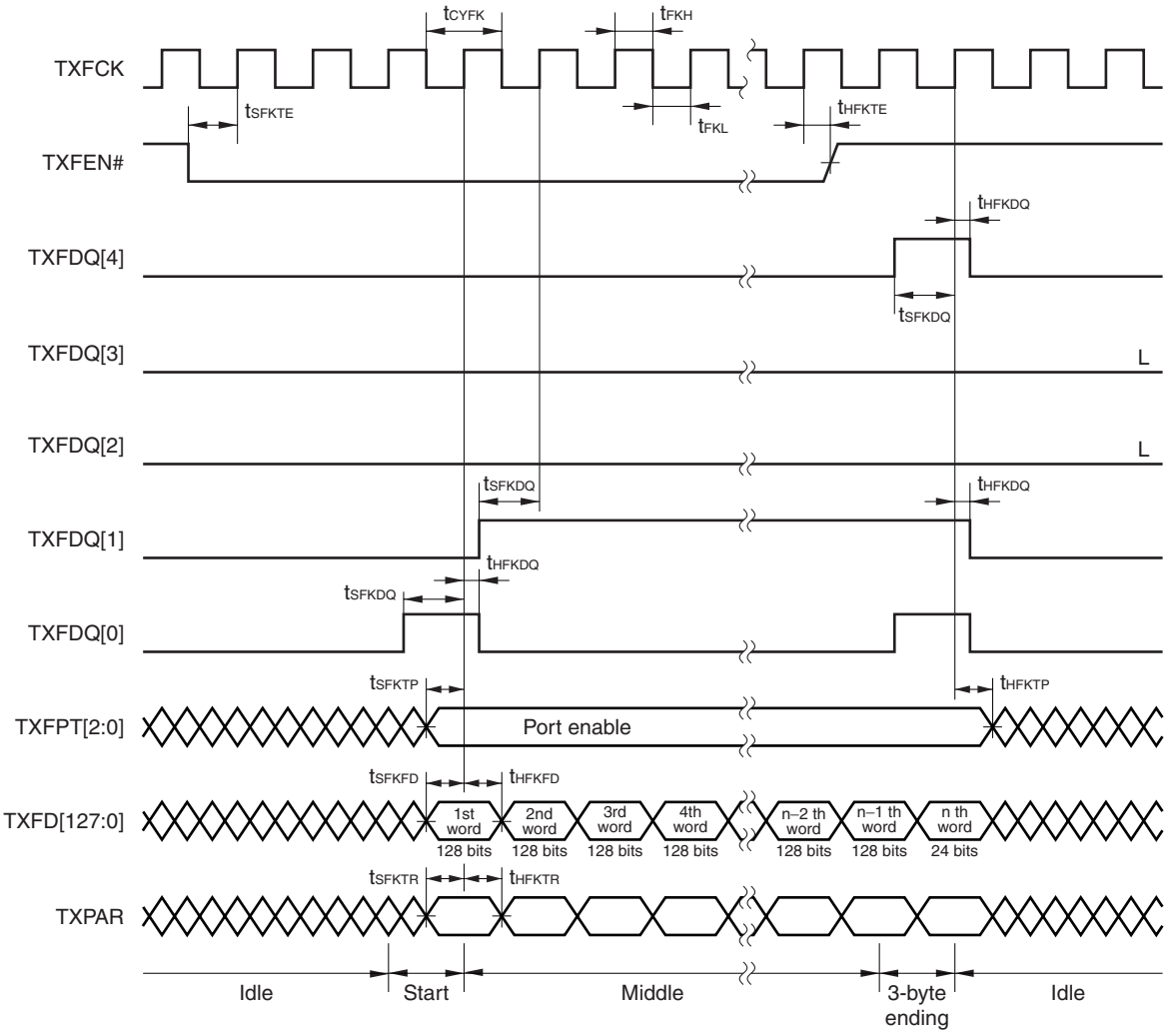


FIFO Bus Interface Write Timing

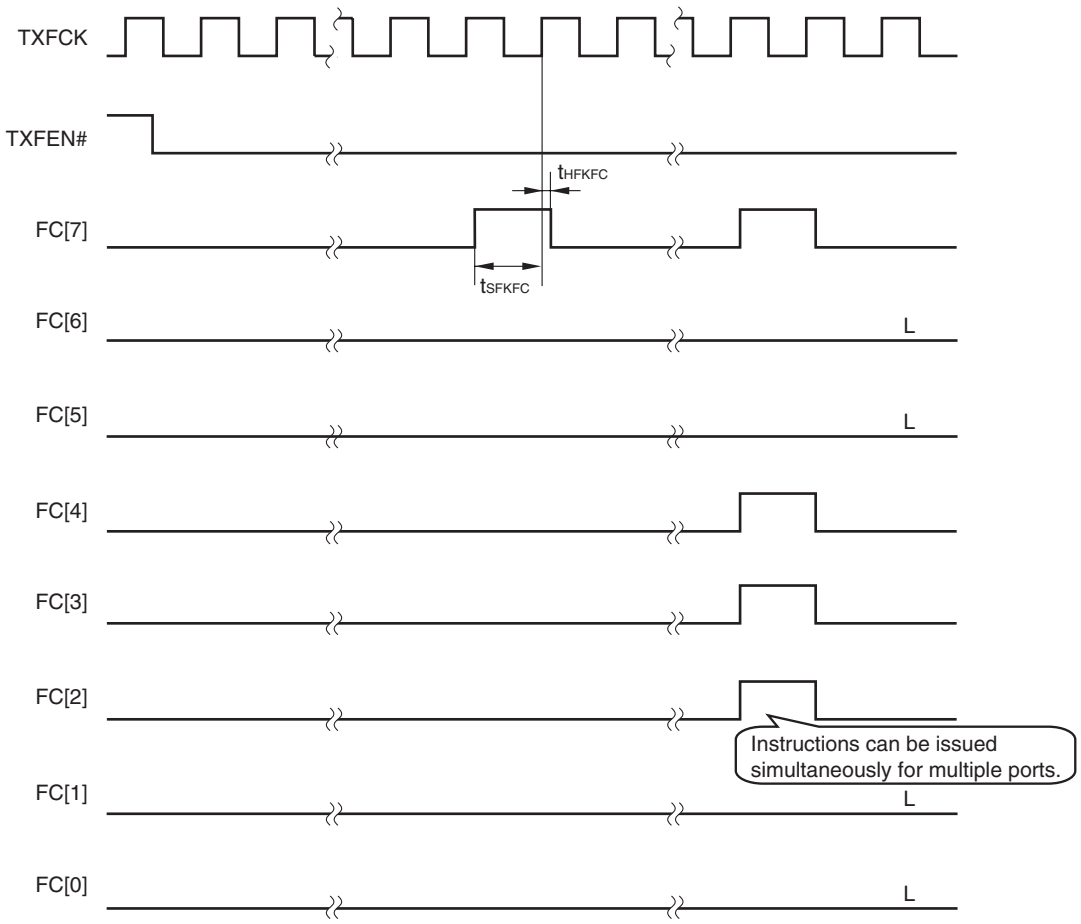
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★ TXFCK clock width	t_{CYFK}		8			ns
TXFCK high-level width	t_{FKH}		3.5			ns
TXFCK low-level width	t_{FKL}		3.5			ns
TXFEN# setup time	t_{SFKTE}		2.5			ns
TXFEN# hold time	t_{HFKTE}		2.5			ns
TXFDQ[4:0] setup time	t_{SFKDQ}		2.5			ns
TXFDQ[4:0] hold time	t_{HFKDQ}		2.5			ns
TXFPT[2:0] setup time	t_{SFKTP}		2.5			ns
TXFPT[2:0] hold time	t_{HFKTP}		2.5			ns
TXFD[127:0] setup time	t_{SFKFD}		2.5			ns
TXFD[127:0] hold time	t_{HFKFD}		2.5			ns
TXPAR setup time	t_{SFKTR}		2.5			ns
TXPAR hold time	t_{HFKTR}		2.5			ns
FC[N] setup time	t_{SFKFC}		2.5			ns
FC[N] hold time	t_{HFKFC}		2.5			ns

Remark FC[N]: N = 0 to 7

(1) FIFO bus interface write timing



(2) Flow control output instruction timing

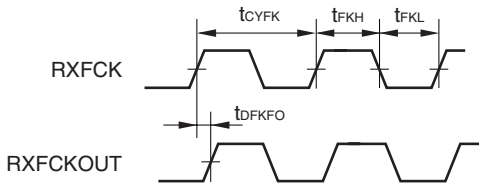


Remark FC[N]: N = 0 to 7

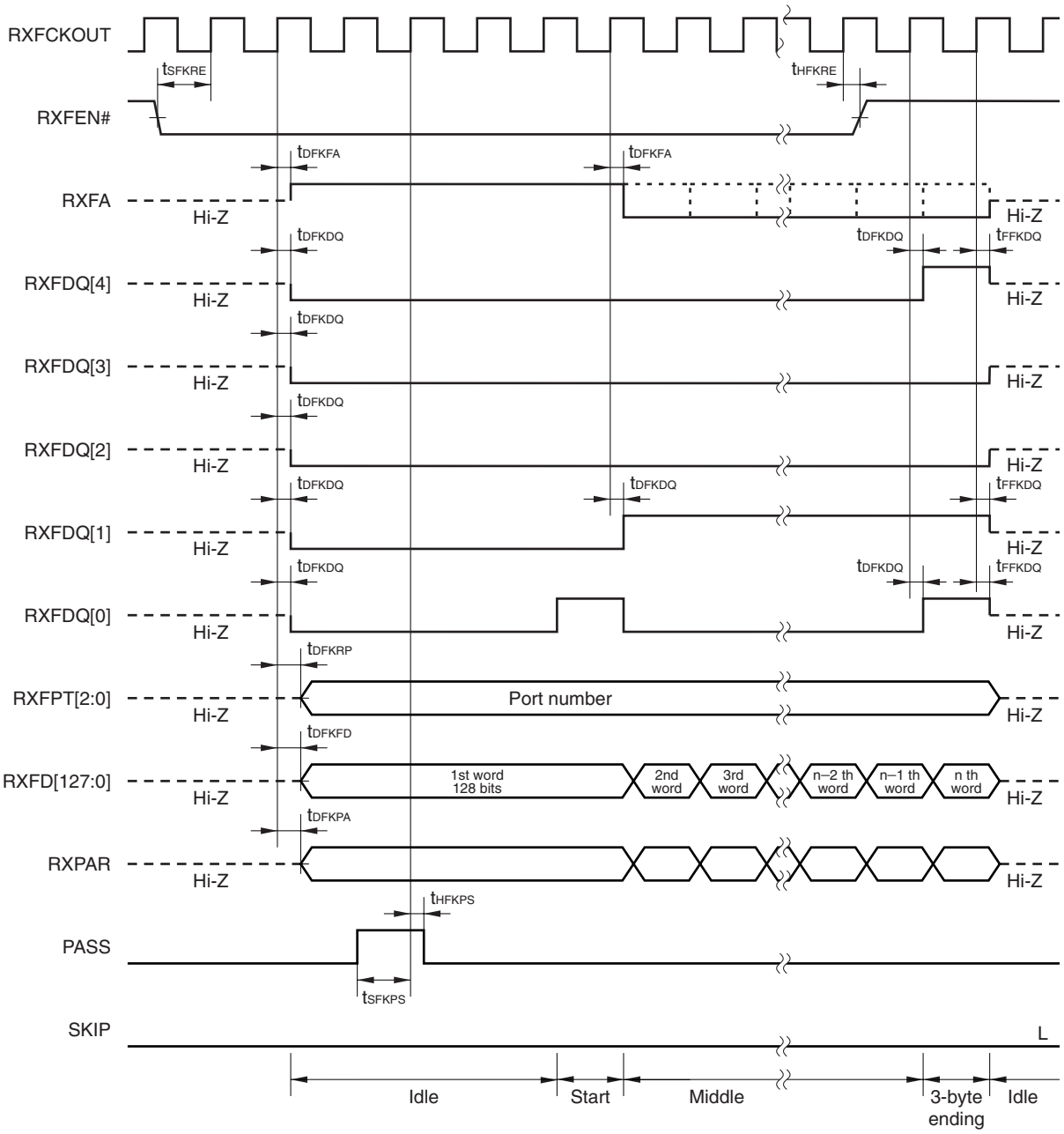
FIFO Bus Interface Read Timing

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★ RXFCK clock width	t_{CYFK}		8			ns
RXFCK high-level width	t_{FKH}		3.5			ns
RXFCK low-level width	t_{FKL}		3.5			ns
RXFCKOUT output delay time	t_{DFKFO}		TBD		TBD	ns
RXFEN# setup time	t_{SFKRE}		2.5			ns
RXFEN# hold time	t_{HFKRE}		2.5			ns
RXFA output delay time	t_{DFKFA}		0		4.5	ns
RXFDQ[4:0] output delay time	t_{DFKDQ}		0		4.5	ns
RXFDQ[4:0] float time	t_{FFKDQ}		0		4.5	ns
RXFPT[2:0] output delay time	t_{DFKRP}		0		4.5	ns
RXFD[127:0] output delay time	t_{DFKFD}		0		4.5	ns
RXPAR output delay time	t_{DFKPA}		0		4.5	ns
PASS setup time	t_{SFKPS}		2.5			ns
PASS hold time	t_{HFKPS}		2.5			ns
SKIP setup time	t_{SFKSP}		2.5			ns
SKIP hold time	t_{HFKSP}		2.5			ns
RXABT setup time	t_{SFKAB}		2.5			ns
RXABT hold time	t_{HFKAB}		2.5			ns

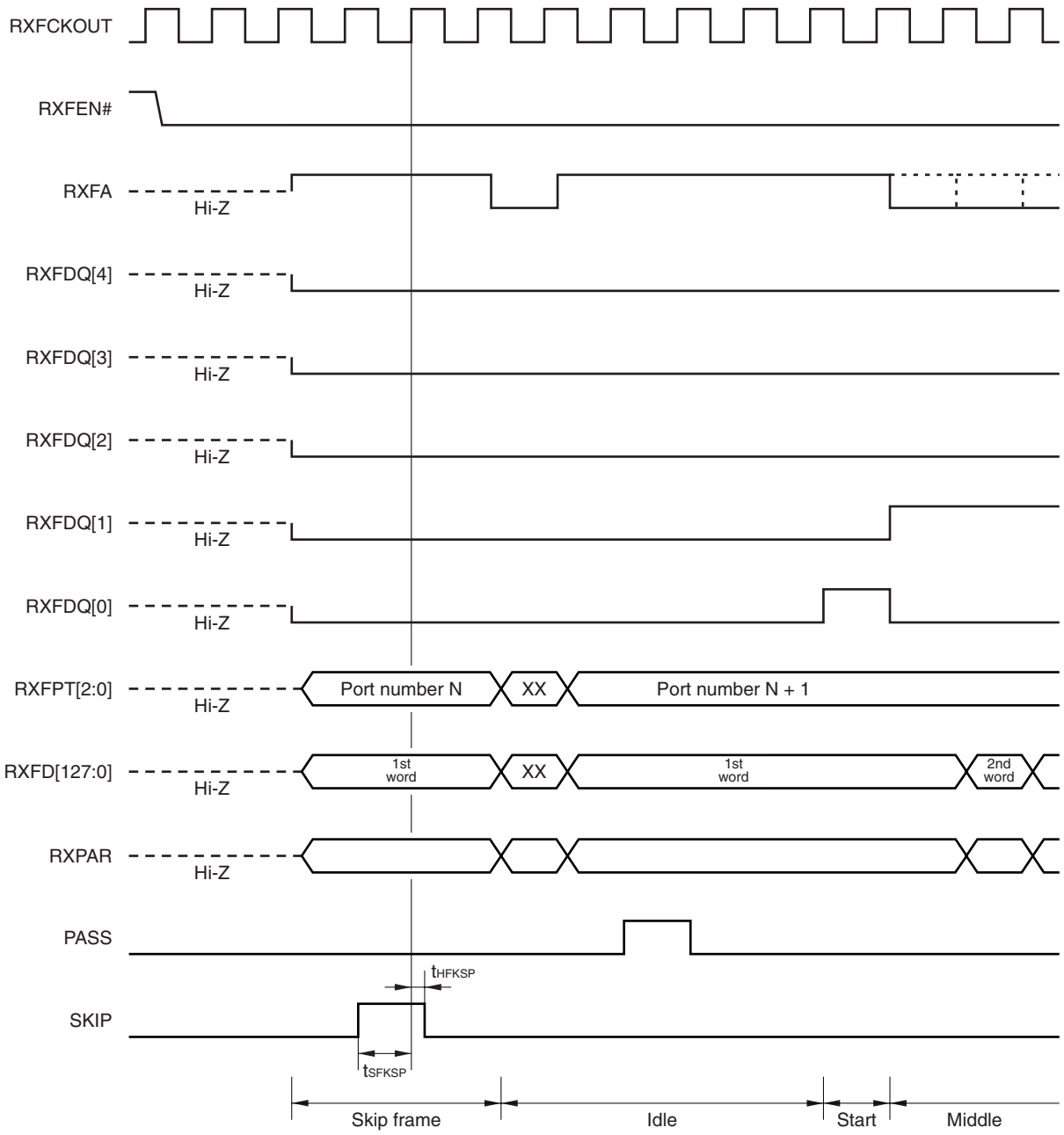
(1) Clock timing



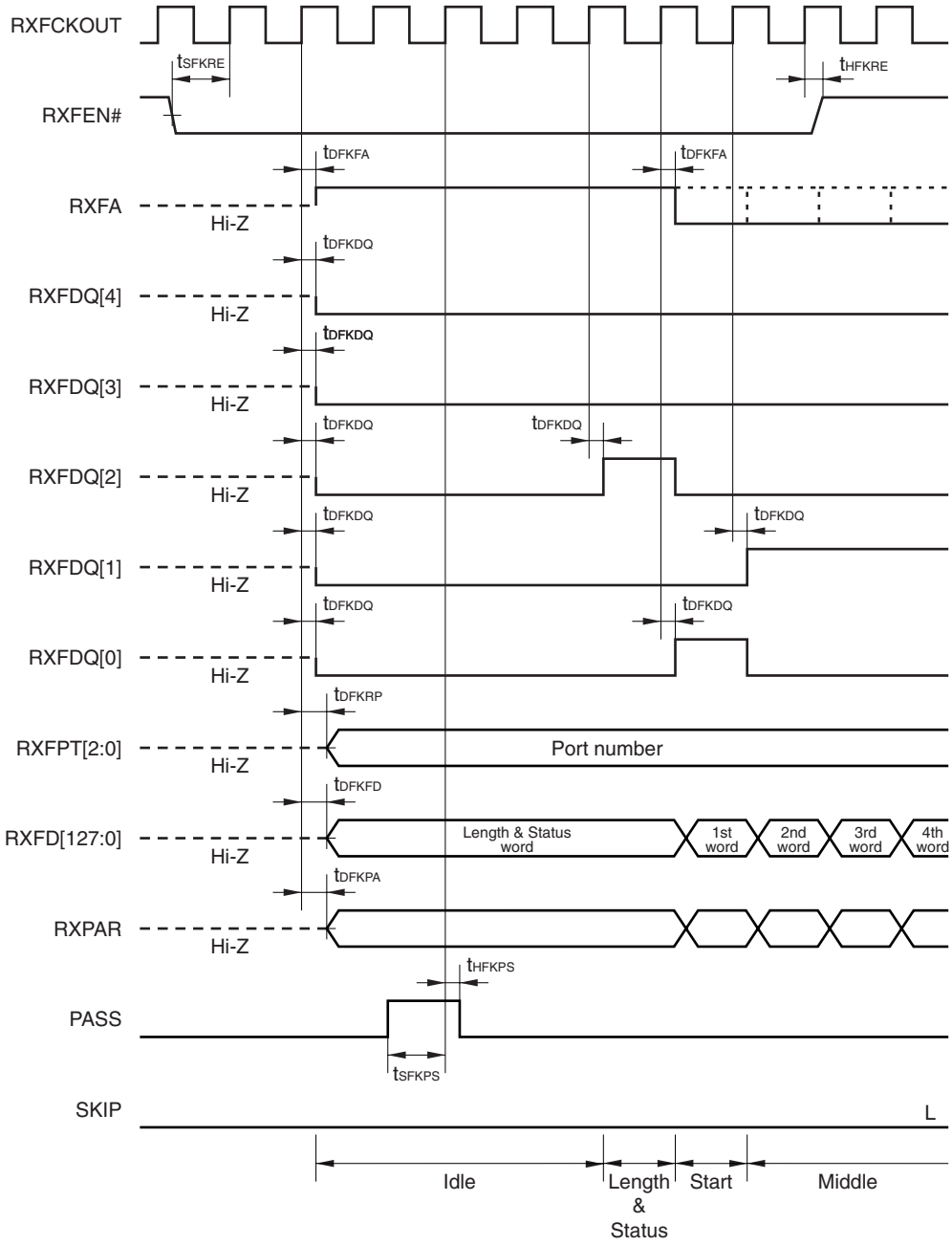
(2) FIFO bus interface read timing 1



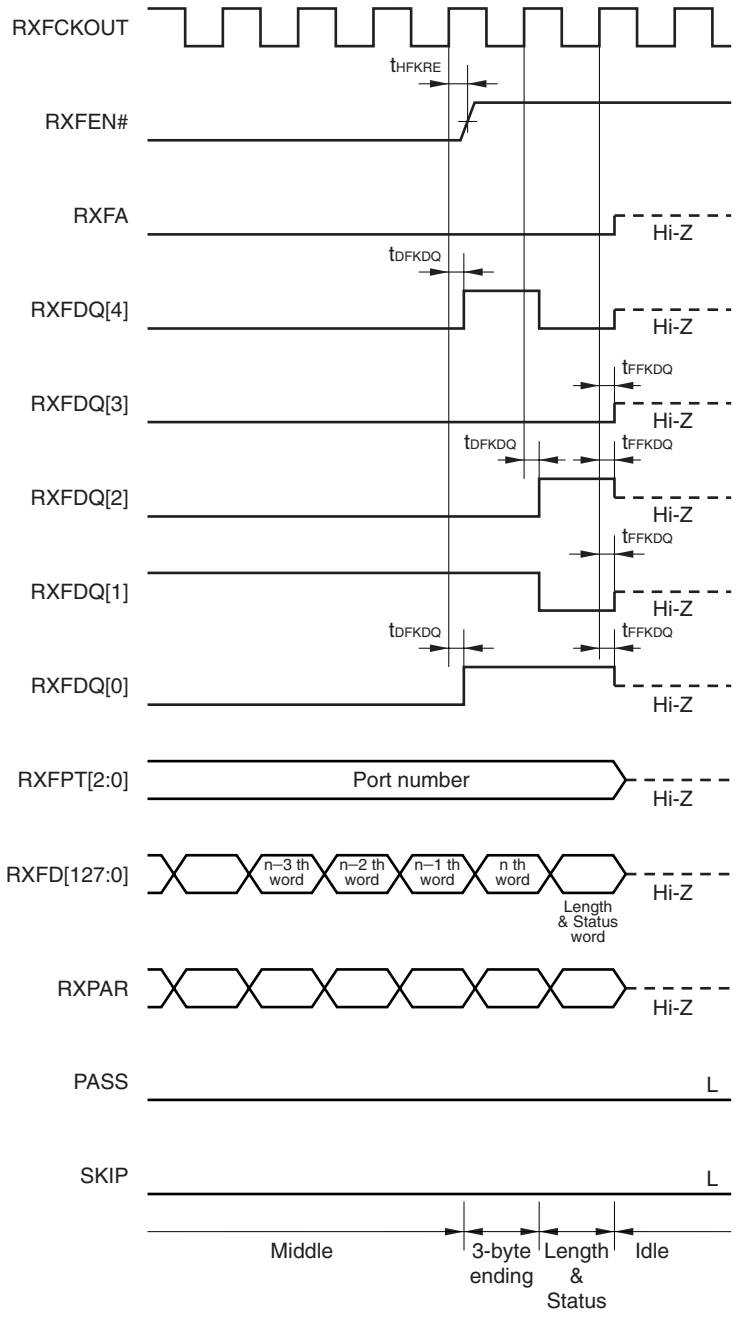
(3) FIFO bus interface read timing (when SKIP is input) 2



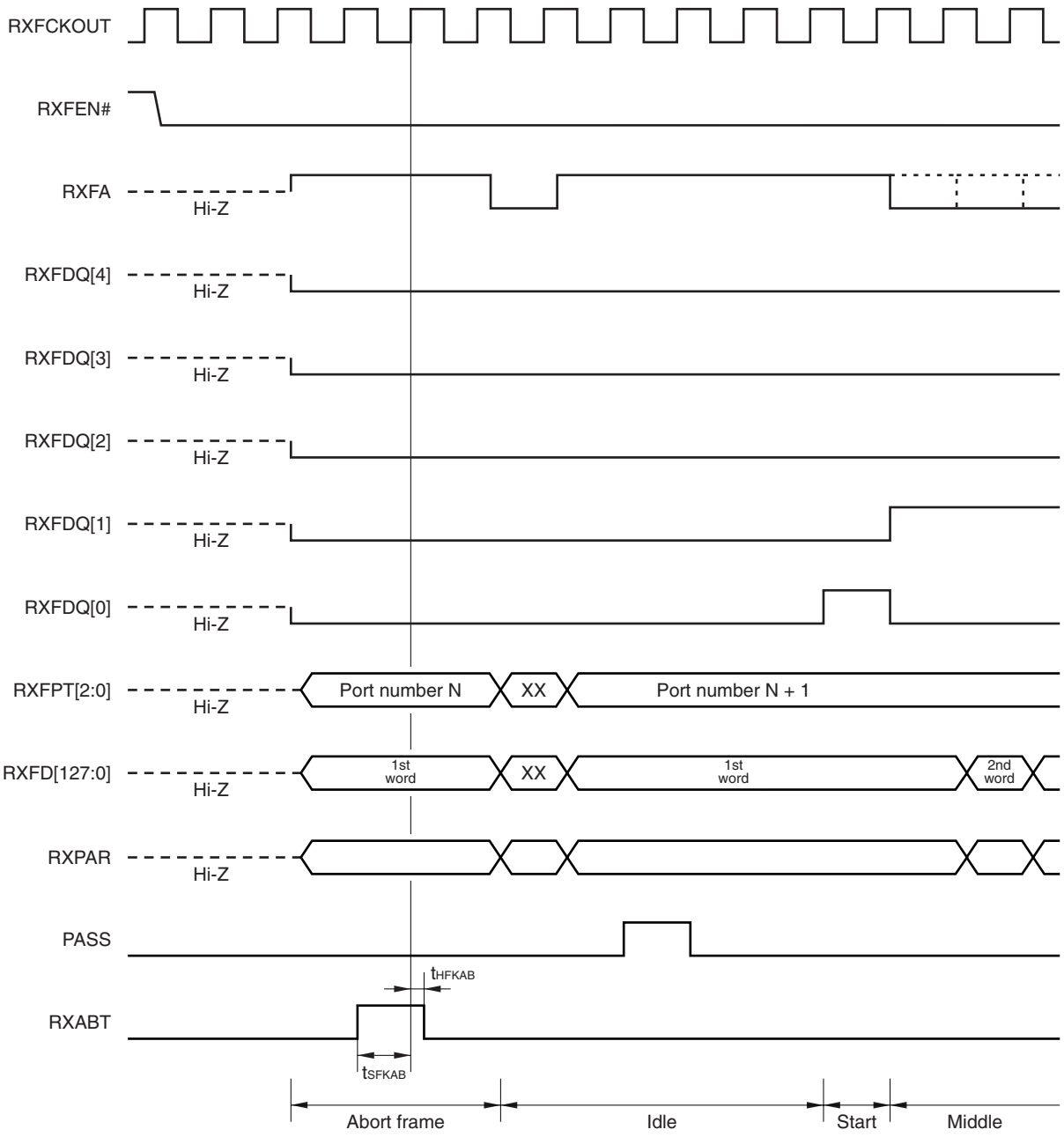
(4) FIFO bus interface read timing (when Status & RBYT are added at beginning) 3



(5) FIFO bus interface read timing (when Status & RBYT are added at end) 4

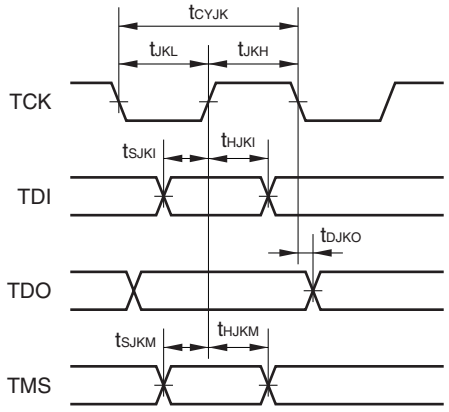


(6) RXABT signal input timing



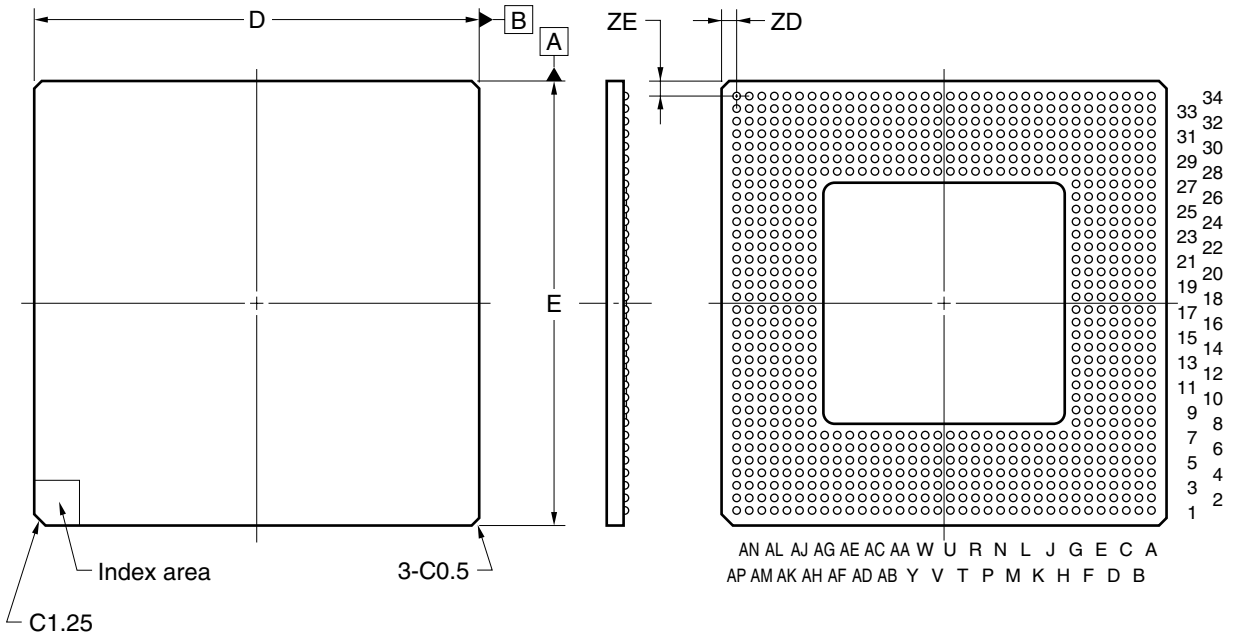
Boundary Scan (JTAG) Timing

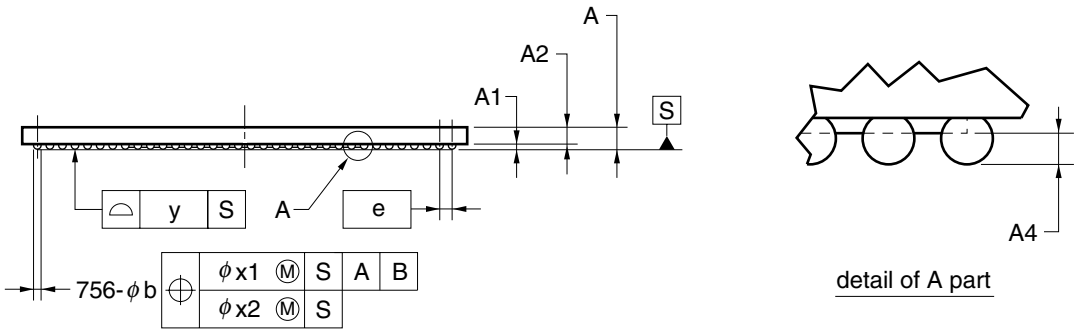
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TCK clock width	t_{CYJK}		100			ns
TCK low-level width	t_{JKL}		50			ns
TCK high-level width	t_{JKH}		50			ns
TDI setup time	t_{SJKI}		10			ns
TDI hold time	t_{HJKI}		10			ns
TDO output delay time	t_{DJKO}				20	ns
TMS setup time	t_{SJKM}		10			ns
TMS hold time	t_{HJKM}		10			ns



3. PACKAGE DRAWING

756-PIN PLASTIC BGA (CAVITY DOWN ADVANCED TYPE) (45x45)





ITEM	MILLIMETERS
D	45.00±0.20
E	45.00±0.20
e	1.27
A	2.50±0.30
A1	0.60±0.10
A2	1.90
A4	0.25 MIN.
b	0.75±0.15
x1	0.30
x2	0.15
y	0.20
ZD	1.545
ZE	1.545

P756S9-127-K6-1

4. RECOMMENDED SOLDERING CONDITIONS

The μPD98433 should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Surface Mount Type

μPD98433S9-K6: 756-pin plastic BGA (C/D advanced type) (45 × 45)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 20 hours)	IR30-203-3

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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