NEC

MOS INTEGRATED CIRCUIT

μPD98421

HIGH-SPEED ADDRESS SEARCH ENGINE

DESCRIPTION

The μPD98421 is a CAM (Content Addressable Memory) with a capacity of 64 bits × 8192 entries. Equipped with three types of search modes, this memory can search data at high speeds. One of these search modes, Longest Prefix Match mode, can mask data in entry units and output the address with the longest match in the search data. This function is effective for searching IP addresses of Layer 3.

FEATURES

- 64 bits × 8K entries
- High-speed synchronous operation. Maximum operating frequency: 33 MHz (normal mode)/50 MHz (FF mode)
- Mask register masking any bit of 64-bit search data
- Three search modes supported for high-speed searching.
  - Full Match mode: 30 ns (at 33 MHz)
  - Full Match with Mask mode: 30 ns
  - Longest Prefix Match mode: 60 ns
- Number of entries can be expanded by connecting multiple μPD98421s.
- Can read/write data by high-speed synchronous operation (memory operation).
- Supply voltage: 3.3 V ± 0.15 V
- 240-pin plastic FBGA

ORDERING INFORMATION

Part Number	Package
μPD98421F1-GA1	240-pin plastic FBGA (16 × 16)

Remark In this document, active-low pins are expressed as xxx_B (_B suffixed to a pin name).

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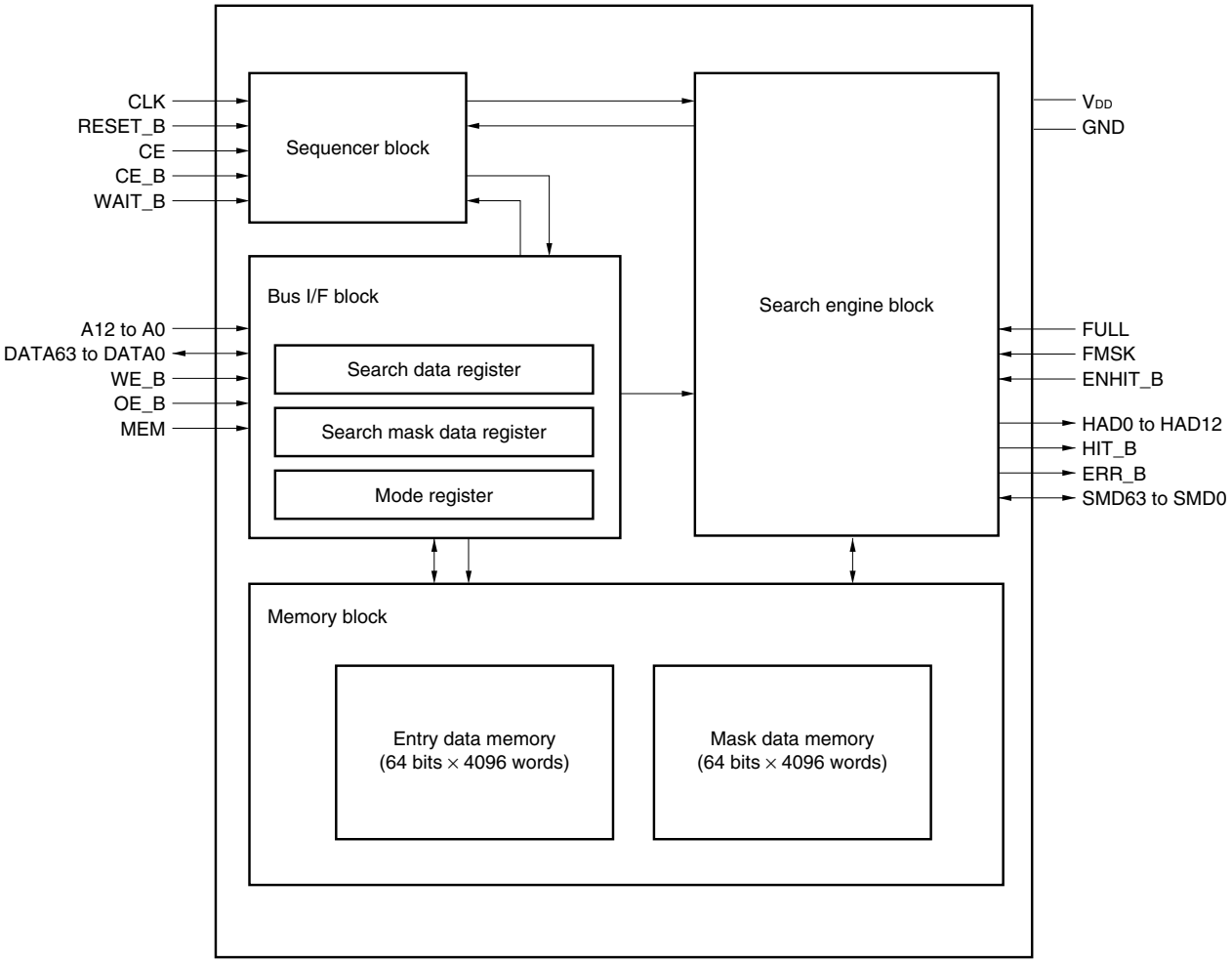
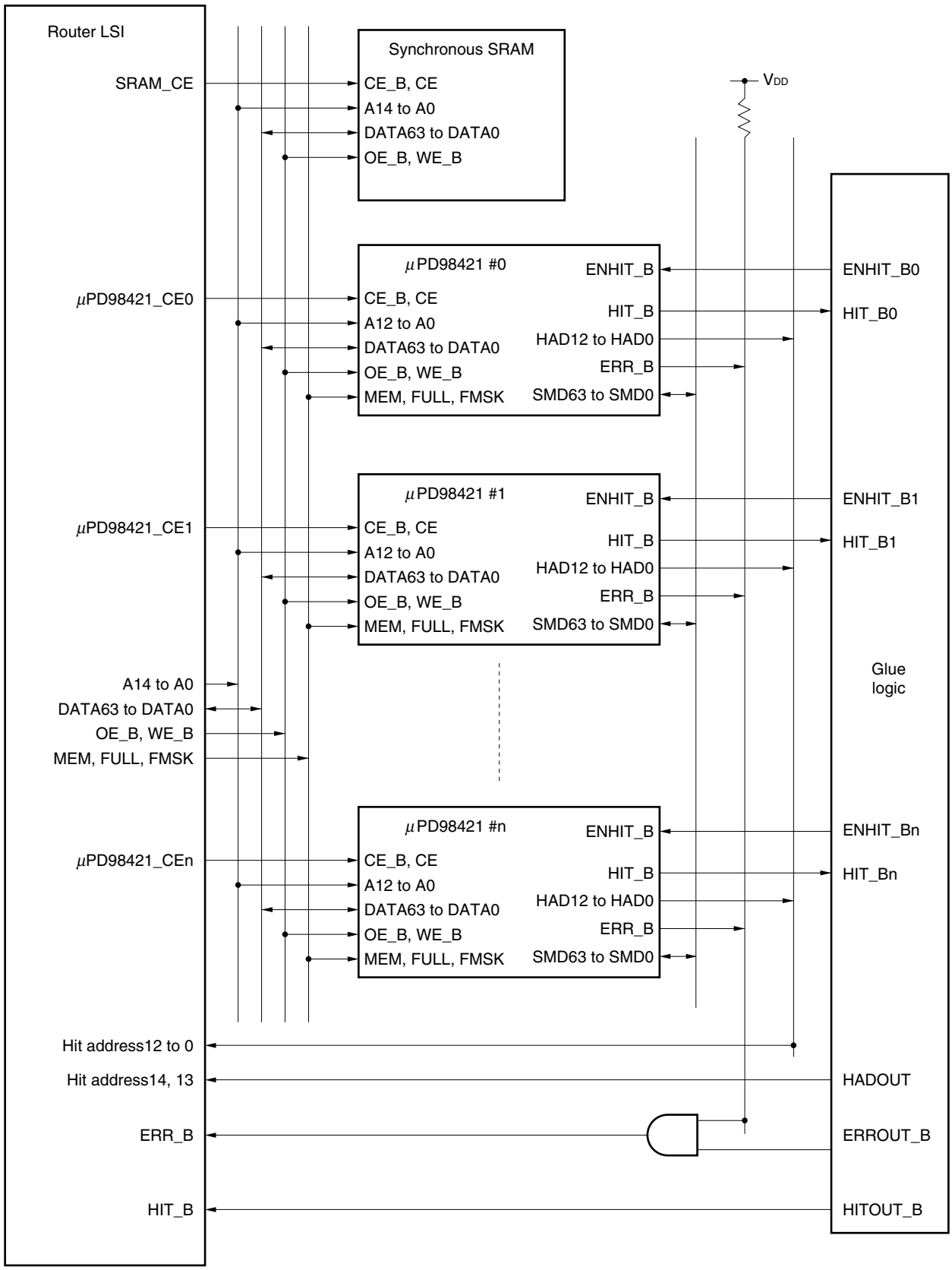
The mark ★ shows major revised points.

BLOCK DIAGRAM

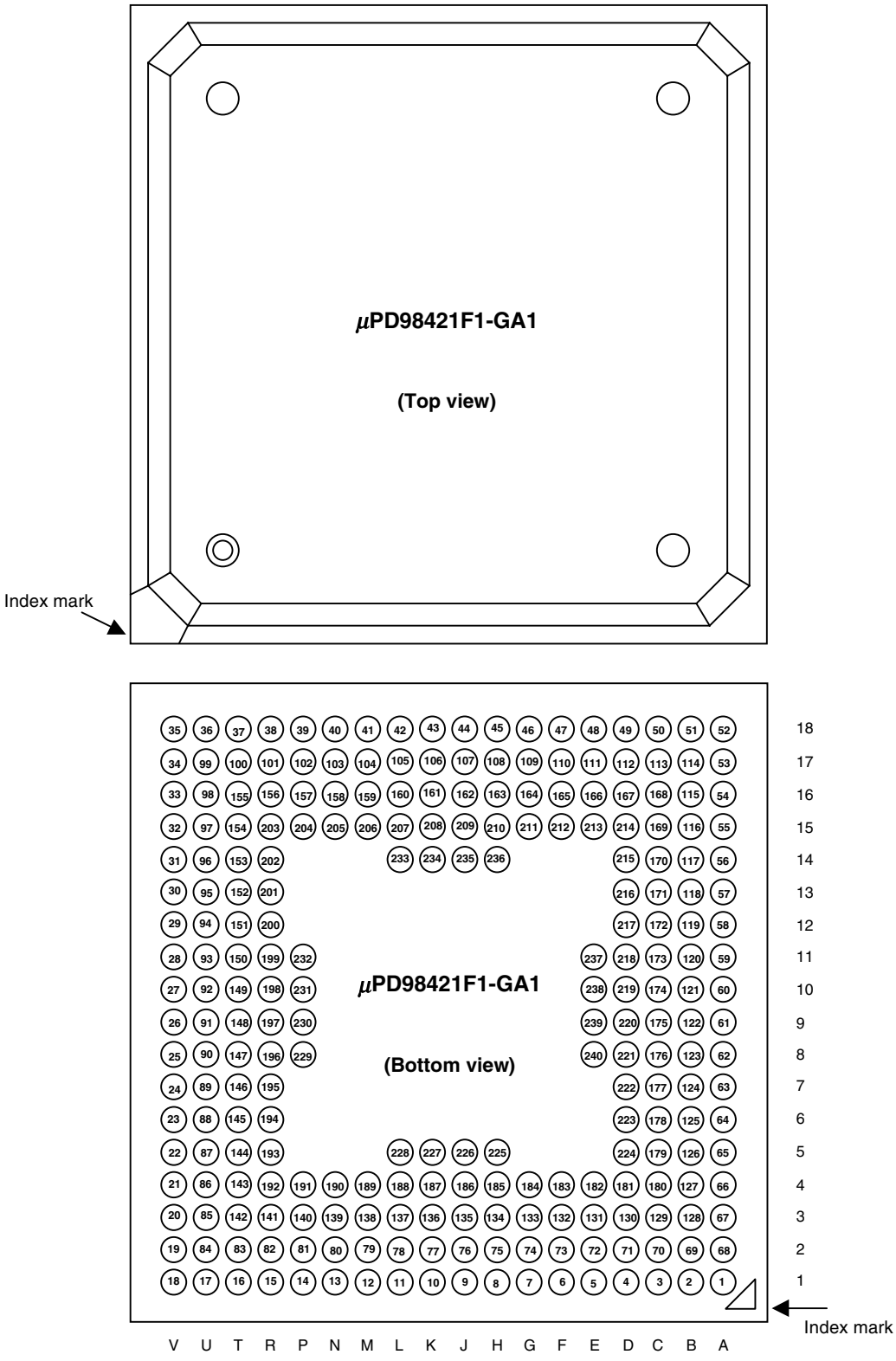


SYSTEM CONFIGURATION EXAMPLE



PIN CONFIGURATION

- **240-pin plastic FBGA (16 × 16)**



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1 (A1)	L	49 (D18)	DATA23	97 (U15)	GND	145 (T6)	GND	193 (R5)	DATA38
2 (B1)	L	50 (C18)	SMD22	98 (U16)	A3	146 (T7)	GND	194 (R6)	DATA40
3 (C1)	I.C.	51 (B18)	DATA21	99 (U17)	V_{DD}	147 (T8)	SMD36	195 (R7)	SMD38
4 (D1)	DATA63	52 (A18)	SMD20	100 (T17)	A1	148 (T9)	DATA34	196 (R8)	DATA35
5 (E1)	GND	53 (A17)	V_{DD}	101 (R17)	HAD12	149 (T10)	DATA32	197 (R9)	GND
6 (F1)	DATA60	54 (A16)	DATA18	102 (P17)	GND	150 (T11)	WE_B	198 (R10)	SMD32
7 (G1)	SMD59	55 (A15)	DATA17	103 (N17)	HAD6	151 (T12)	MEM	199 (R11)	OE_B
8 (H1)	DATA57	56 (A14)	GND	104 (M17)	HAD3	152 (T13)	GND	200 (R12)	CE_B
9 (J1)	V_{DD}	57 (A13)	SMD15	105 (L17)	GND	153 (T14)	A9	201 (R13)	A12
10 (K1)	SMD55	58 (A12)	SMD13	106 (K17)	ENHIT_B	154 (T15)	A6	202 (R14)	A8
11 (L1)	SMD53	59 (A11)	V_{DD}	107 (J17)	SMD30	155 (T16)	A4	203 (R15)	A0
12 (M1)	GND	60 (A10)	SMD10	108 (H17)	DATA28	156 (R16)	HAD11	204 (P15)	GND
13 (N1)	SMD50	61 (A9)	SMD9	109 (G17)	DATA26	157 (P16)	HAD9	205 (N15)	V_{DD}
14 (P1)	DATA48	62 (A8)	DATA7	110 (F17)	DATA25	158 (N16)	HAD7	206 (M15)	HAD4
15 (R1)	GND	63 (A7)	GND	111 (E17)	GND	159 (M16)	HAD2	207 (L15)	HIT_B
16 (T1)	DATA46	64 (A6)	SMD4	112 (D17)	GND	160 (L16)	V_{DD}	208 (K15)	SMD31
17 (U1)	DATA45	65 (A5)	SMD3	113 (C17)	DATA20	161 (K16)	RESET_B	209 (J15)	V_{DD}
18 (V1)	SMD44	66 (A4)	GND	114 (B17)	GND	162 (J16)	GND	210 (H15)	GND
19 (V2)	GND	67 (A3)	DATA0	115 (B16)	DATA19	163 (H16)	SMD28	211 (G15)	V_{DD}
20 (V3)	DATA42	68 (A2)	V_{DD}	116 (B15)	SMD18	164 (G16)	SMD26	212 (F15)	SMD24
21 (V4)	GND	69 (B2)	GND	117 (B14)	DATA16	165 (F16)	SMD25	213 (E15)	DATA22
22 (V5)	SMD40	70 (C2)	I.C.	118 (B13)	DATA15	166 (E16)	SMD23	214 (D15)	SMD19
23 (V6)	SMD39	71 (D2)	V_{DD}	119 (B12)	GND	167 (D16)	V_{DD}	215 (D14)	DATA14
24 (V7)	DATA37	72 (E2)	DATA62	120 (B11)	SMD12	168 (C16)	SMD21	216 (D13)	SMD16
25 (V8)	GND	73 (F2)	SMD61	121 (B10)	SMD11	169 (C15)	GND	217 (D12)	SMD14
26 (V9)	SMD34	74 (G2)	GND	122 (B9)	DATA8	170 (C14)	SMD17	218 (D11)	DATA11
27 (V10)	DATA33	75 (H2)	SMD58	123 (B8)	SMD7	171 (C13)	V_{DD}	219 (D10)	DATA9
28 (V11)	CLK	76 (J2)	DATA56	124 (B7)	SMD5	172 (C12)	DATA13	220 (D9)	GND
29 (V12)	WAIT_B	77 (K2)	DATA54	125 (B6)	V_{DD}	173 (C11)	GND	221 (D8)	SMD6
30 (V13)	CE	78 (L2)	DATA52	126 (B5)	SMD2	174 (C10)	DATA10	222 (D7)	GND
31 (V14)	N.C.	79 (M2)	SMD51	127 (B4)	SMD0	175 (C9)	SMD8	223 (D6)	DATA2
32 (V15)	A10	80 (N2)	DATA49	128 (B3)	L	176 (C8)	DATA6	224 (D5)	SMD1
33 (V16)	A7	81 (P2)	V_{DD}	129 (C3)	L	177 (C7)	DATA4	225 (H5)	DATA58
34 (V17)	A5	82 (R2)	SMD46	130 (D3)	GND	178 (C6)	DATA3	226 (J5)	GND
35 (V18)	A2	83 (T2)	DATA44	131 (E3)	SMD63	179 (C5)	DATA1	227 (K5)	DATA53
36 (U18)	GND	84 (U2)	V_{DD}	132 (F3)	DATA61	180 (C4)	GND	228 (L5)	DATA51
37 (T18)	N.C.	85 (U3)	DATA43	133 (G3)	DATA59	181 (D4)	L	229 (P8)	SMD37
38 (R18)	HAD10	86 (U4)	SMD42	134 (H3)	GND	182 (E4)	SMD60	230 (P9)	V_{DD}
39 (P18)	HAD8	87 (U5)	SMD41	135 (J3)	SMD56	183 (F4)	SMD62	231 (P10)	GND
40 (N18)	HAD5	88 (U6)	DATA39	136 (K3)	SMD54	184 (G4)	V_{DD}	232 (P11)	FULL
41 (M18)	HAD1	89 (U7)	V_{DD}	137 (L3)	SMD52	185 (H4)	SMD57	233 (L14)	HAD0
42 (L18)	ERR_B	90 (U8)	DATA36	138 (M3)	DATA50	186 (J4)	DATA55	234 (K14)	DATA31
43 (K18)	GND	91 (U9)	SMD35	139 (N3)	SMD49	187 (K4)	GND	235 (J14)	DATA29
44 (J18)	DATA30	92 (U10)	SMD33	140 (P3)	DATA47	188 (L4)	V_{DD}	236 (H14)	SMD27
45 (H18)	SMD29	93 (U11)	GND	141 (R3)	GND	189 (M4)	GND	237 (E11)	DATA12
46 (G18)	DATA27	94 (U12)	FMSK	142 (T3)	SMD45	190 (N4)	SMD48	238 (E10)	GND
47 (F18)	GND	95 (U13)	V_{DD}	143 (T4)	V_{DD}	191 (P4)	SMD47	239 (E9)	V_{DD}
48 (E18)	DATA24	96 (U14)	A11	144 (T5)	DATA41	192 (R4)	SMD43	240 (E8)	DATA5

Remarks 1. Figures in parentheses indicate the coordinates in the pin configuration.

2. I.C.: Internal Connection

L: Fixed at low level

N.C.: No Connection

PIN NAMES

A12 to A0:	Address
CE, CE_B:	Chip Select
CLK:	Clock
DATA63 to DATA0:	Data
ENHIT_B:	Enable Hit
ERR_B:	Error
FMSK:	Full Match Mask Mode
FULL:	Full Match Mode
GND:	Ground
HAD12 to HAD0:	Hit Address
HIT_B:	Hit
MEM:	Memory
OE_B:	Output Enable
RESET_B:	Reset
SMD63 to SMD0:	Search Mask Data
V_{DD}:	Supply Voltage
WAIT_B:	Wait
WE_B:	Write Enable

CONTENTS

1. PIN FUNCTIONS

Pin Name	Pin No.	I/O	Description
CLK	28	Input	Clock. System clock input pin. Inputs a clock of up to 33 MHz (normal mode)/50 MHz (FF mode).
WAIT_B	29	Input	Wait. Wait input pin. Asserted active at low level. If the WAIT_B signal is active at the rising edge of CLK, the μPD98421 is placed in a wait status for the duration of 1 CLK cycle from the next rising of CLK. In wait status, all the pins retain the status immediately before the wait status was set. However, output control by CE, CE_B, and ENHIT_B is valid.
CE_B	200	Input	Chip select. Asserted active at low level. When the CE signal and CE_B signal of a chip are asserted active at the same time, the chip is selected. DATA, HAD, ERR_B, and SMD of the unselected chip enter a high-impedance state.
CE	30	Input	Chip select. Asserted active at low level. When the CE signal and CE_B signal of a chip are asserted active at the same time, the chip is selected. DATA, HAD, ERR_B, and SMD of the unselected chip enter a high-impedance state.
A12 to A0	201, 96, 32, 153, 202, 33, 154, 34, 155, 98, 35, 100, 203	Input	Address. A12 to A0 are 13-bit address signals. Signals input to A12 through A8 are ignored in the I/O access mode.
DATA63 to DATA0	4, 72, 132, 6, 133, 225, 8, 76, 186, 77, 227, 78, 228, 138, 80, 14, 140, 16, 17, 83, 85, 20, 144, 194, 88, 193, 24, 90, 196, 148, 27, 149, 234, 44, 235, 108, 46, 109, 110, 48, 49, 213, 51, 113, 115, 54, 55, 117, 118, 215, 172, 237, 218, 174, 219, 122, 62, 176, 240, 177, 178, 223, 179, 67	I/O	Data. DATA63 to DATA0 are data bus signals that input/output 64-bit data to/from the internal memory and registers.
WE_B	150	Input	Write enable. Enables writing to DATA63 to DATA0. When the WE_B signal is active, DATA63 to DATA0 enter a high-impedance state.
OE_B	199	Input	Output enable. Enables output of data from DATA63 to DATA0.

Pin Name	Pin No.	I/O	Description
MEM	151	Input	Memory. Specifies access right to memory/register. When the MEM signal is high, the μPD98421 performs the same operations as an SRAM (refer to **3. FUNCTIONAL DESCRIPTION**). When this signal is low, the internal registers can be accessed for input/output. MEM Access function 1 Memory access 0 I/O access
FULL	232	Input	Full Match Mode. Sets a search mode with the MEM and FMSK signals (refer to **3. FUNCTIONAL DESCRIPTION**).
FMSK	94	Input	Full Match with Mask mode. Sets a search mode with the MEM and FULL signals (refer to 3. FUNCTIONAL DESCRIPTION).
HAD12 to HAD0	101, 156, 38, 157, 39, 158, 103, 40, 206, 104, 159, 41, 233	Output 3 state (Internal pull-up)	Hit address. HAD12 through HAD0 output a matched valid address if the HIT_B signal goes low and ERR_B goes high during a search operation. If ERR_B is asserted active (low level), HAD output is invalid. HAD12 is meaningless except in the Full Match mode. These pins are internally pulled up.
HIT_B	207	Output	Hit. Data is searched after it is written to the search data register during a search operation. HIT_B is a low-active signal that indicates that data matching the search data has been found. 0: Match data found, 1: Match data not found
ERR_B	42	Output (Open drain)	Error. This signal goes low if two or more sets of entry data having the same mask data are found during a search operation. Because this is an open-drain signal, pull it up. This signal is inactive (high-impedance) during a memory operation.
ENHIT_B	106	Input	Enable hit. This signal controls output of the HAD12 to HAD0 and ERR_B signals. ENHIT_B HAD[12:0] ERR_B 1 Hi-Z Hi-Z 0 Output enabled
SMD63 to SMD0	131, 183, 73, 182, 7, 75, 185, 135, 10, 136, 11, 137, 79, 13, 139, 190, 191, 82, 142, 18, 192, 86, 87, 22, 23, 195, 229, 147, 91, 26, 92, 198, 208, 107, 45, 163, 236, 164, 165, 212, 166, 50, 168, 52, 214, 116, 170, 216, 57, 217, 58, 120, 121, 60, 61, 175, 123, 221, 124, 64, 65, 126, 224, 127	I/O (Internal pull-up)	Search mask data. The SMD63 to SMD0 signals are used for temporary I/O with other μPD98421s in the Longest Prefix Match mode. Connect each of these pins to the corresponding pin of the other μPD98421s.

Pin Name	Pin No.	I/O	Description
RESET_B	161	Input	Reset. When this signal is set to low, the chip is initialized. Only the internal sequencer and mode register are initialized; the memory area is not cleared. Be sure to create an external circuit in which RESET_B becomes low level after power application. In addition, input at least 2 CLK or more NOP commands continuously after releasing reset.
VDD	9, 53, 59, 68, 71, 81, 84, 89, 95, 99, 125, 143, 160, 167, 171, 184, 188, 205, 209, 211, 230, 239	–	3.3 V power supply
GND	5, 12, 15, 19, 21, 25, 36, 43, 47, 56, 63, 66, 69, 74, 93, 97, 102, 105, 111, 112, 114, 119, 130, 134, 141, 145, 146, 152, 162, 169, 173, 180, 187, 189, 197, 204, 210, 220, 222, 226, 231, 238	–	Ground
N.C.	31, 37	–	No connection. Leave open.
I.C.	3, 70	–	Internally connected. Leave open.
L	1, 2, 128, 129, 181	–	Always fix these pins at low level.

2. MEMORY/REGISTER CONFIGURATION

2.1 Memory Configuration

The μPD98421 has a memory area of 64 bits × 8192 entries. Two types of memory configurations can be selected in accordance with the search mode. For this selection, no special setting of the chip is necessary. The μPD98421 can also be used as a synchronous SRAM.

2.1.1 Full Match mode

64 bits × 8192 entries: Entry data

In the Full Match mode, all the 8192 entries are used as a data area.

Table 2-1. Memory Mapping in Full Match Mode

Address	Contents
0000h	Entry data
0001h	Entry data
:	:
0FFFh	Entry data
1000h	Entry data
:	:
1FFEh	Entry data
1FFFh	Entry data

2.1.2 Full Match with Mask/Longest Prefix Match mode

64 bits × 4096 entries: Entry data
64 bits × 4096 entries: Entry mask data

In the Full Match with Mask and Longest Prefix Match modes, 4096 entries at addresses 0000h to 0FFFh are used as a data area, and addresses 1000h to 1FFFh are used as a mask data area.

The mask data at 1000h to 1FFFh mask each of the corresponding entry data as shown in Table 2-2. If a bit of the mask data is 0, the corresponding bit of the entry data is ignored during the search.

The mask data must be successively masked, starting from the LSB, in the Longest Prefix Match mode.

Example FFFF0000 → Correct, FF00F000 → Incorrect

Table 2-2. Memory Mapping in Full Match with Mask/Longest Prefix Match Modes

Address	Contents
0000h	Entry data
0001h	Entry data
:	:
0FFFh	Entry data
1000h	Mask data of 0000h
:	:
1FFEh	Mask data of 0FFEh
1FFFh	Mask data of 0FFFh

2.2 Register Configuration

The μPD98421 allocates the internal registers to 256 words of I/O addresses. Each register is 64 bits long. Address signal lines A0 through A7 are used to specify an I/O address to access a register. A8 through A12 are not used. When a register is accessed, the MEM signal line is made low. To write data to the register, the WE_B pin is asserted active; to read data from the register, the OE_B pin is asserted active. Data can be written to a register in 1 clock cycle in both the normal and FF modes (except a search operation by writing data to the search data register).

When a register is read in the normal mode, the read data is output 1 clock cycle after the I/O address has been input. In the FF mode, the read data is output 2 clock cycles after address input. For the details of the normal and FF modes, refer to **2.2.3 Mode register**.

Table 2-3. Internal Registers

I/O Address	Register
00h	Search data register
01h	Mask data register
02h	Mode register
03h	Reserved (do not access this register.)
04h	NOP register
05 to FFh	Reserved (do not access this register.)

2.2.1 Search data register

The search data is stored in this register. When 64-bit search data is written to the search data register, the μPD98421 starts a search operation.

The search data register is not initialized even when the chip is reset.

2.2.2 Mask data register

The mask data register stores a value to mask the search data stored in the search data register. Store a valid value in this register before a value is written to the search data register.

If a bit of the mask data register is 0, the corresponding bit of the search data register is masked and ignored. The masking specified by this register is valid for all entries in all the search modes.

The mask data register is not initialized even when the chip is reset. When the bit width of all entries is less than 64 bits, it is recommended to mask unused bits using this function (to reduce the current consumption of the chip).

However, do not mask bit 63.

2.2.3 Mode register

The mode register selects the search timing mode (normal/FF mode) of the μPD98421 and controls the operations of the μPD98421 without using the FULL, FMSK, and WAIT_B signal lines. This register is initialized to 0 after the chip has been reset.

63 6	5	4	3	2	1	0
reserved	ff	full	fmsk	wait_b2	wait_b1	enbl

enbl — Validates or invalidates the full, fmsk, wait_b2, and wait_b1 bits of the mode register.
- 0: Invalidates full, fmsk, wait_b2, and wait_b1 bits, and validates the FULL, FMSK, and WAIT_B signal lines.
- 1: Validates full, fmsk, wait_b2, and wait_b1 bits, and invalidates the FULL, FMSK, and WAIT_B signal lines.

wait_b1 — Specifies whether a wait cycle is inserted after the first clock.
- 0: Inserts 1 wait cycle after a search operation. In the Longest Prefix Match mode, one wait cycle is inserted between the first search clock and second search clock.
- 1: No operation

wait_b2 — Specifies whether a wait cycle is inserted after the second clock.
- 0: Inserts one wait cycle after the second search clock in the Longest Prefix Match mode.
- 1: No operation

full, fmsk — Selects a search mode ([full, fmsk] = [xx]).
- 00: Longest Prefix Match mode
- 01: Reserved
- 10: Full Match mode
- 11: Full Match with Mask mode

ff — Selects a search timing mode (normal or FF mode).
- 0: Normal mode.
  The hit address is output one clock after data has been input in the Full Match or Full Match with Mask mode at up to 33 MHz. In the Longest Prefix Match mode, the hit address is output two clocks after data has been input.
- 1: FF mode
  The hit address is output two clocks after data has been input in the Full Match or Full Match with Mask mode at up to 50 MHz. In the Longest Prefix Match mode, the hit address is output four clocks after data has been input.

reserved — Reserved

bit 64 to bit 6 — Do not access these bits.

Remark Do not execute another operation immediately after write access to the mode register or mask data register. Be sure to perform NOP (write the NOP register) for the duration of at least 1 clock before executing the another operation.

2.2.4 NOP register

When data is written to the NOP register, the μPD98421 is in a no-operation status, in which it performs nothing. Keep the μPD98421 in this status when no operations such as search memory access are being performed. An undefined value is read from the NOP register if it is read.

3. FUNCTIONAL DESCRIPTION

The μPD98421 can select an operation mode for memory operation and search operation by using combinations of the MEM, FULL, and FMSK signals, or combinations of the full and fmsk bits.

Table 3-1. Operation Modes

MEM	FULL	FMSK	Function
1	×	×	Memory operation
0	1	0	Full Match mode
0	1	1	Full Match with Mask mode
0	0	0	Longest Prefix Match mode
0	0	1	None (setting prohibited)

3.1 Memory Operation

The μPD98421 can read or write 64-bit data from or to an internal memory cell during operation, like a synchronous SRAM.

During memory operation, the MEM pin is set to high. When data is written, the WE_B signal is asserted active; when data is read, the OE_B signal is asserted active.

Data can be written within 1 clock in both the normal and FF modes. When data is read, the read data is output 1 clock after address input in the normal mode. In the FF mode, the read data is output 2 clocks after address input. Note, however, that outputting the read data can be delayed by inserting a WAIT cycle.

3.2 Search Operation

A search operation is started when a search mode is set and the search data is written to the search data register. A search mode can be set by setting the MEM, FULL, and FMSK signal lines in the search mode (refer to **Table 3-1**) or by using the mode register (refer to **2.2.3 Mode register**).

3.2.1 Full Match mode

In the Full Match mode, data that completely matches is searched. In this mode, entry data of 8K entries and one mask register can be used.

To search data in the Full Match mode, set the signal lines as shown in Table 3-1 (or set the mode register), and write the search data to the search data register.

The value of the search data register is masked by the value of the mask data register and compared with the 64-bit value of 8K words of memory cells. The bit of the search data register corresponding to a bit of the mask data register that is set to 0 is not used for comparison.

One clock after the search data has been written to the search data register in the normal mode (in the FF mode, two clocks after), the HIT_B signal is asserted active. The address of the match data is output to HAD12 to HAD0 if ENHIT_B is set to 0. If two or more match data items are found during the search operation, ERR_B goes low, and the output to HAD12 to HAD0 is invalid.

The timing to output the hit address can be delayed by inserting WAIT_B. When the ENHIT_B signal is set to 1, ERR_B and HAD12 to HAD0 enter a high-impedance state.

Example To search the data in Table 3-2 from the data shown in Table 3-3 in the Full Match mode (for the sake of convenience, 64-bit values are indicated in hexadecimal form in units of 8 bits).

Because bits 40 to 47 and 8 to 15 of the mask data register in Table 3-2 are 0, the data of the corresponding bits of the search register (44 and 77) is not compared when the data of memory cells is compared.

Bits 40 to 47 (ABh) and 8 to 15 (78h) of the data stored in 0003h are different from the values of the search data register, but this is ignored depending on the mask data register setting. All the other bits match the values of the search data register. This data is match data, and address 0003h is the match address.

Table 3-2. Example of Search Data

Search Data Register	Mask Data Register
11.22.33.44.55.66.77.88	FF.FF.00.FF.FF.FF.00.FF

Table 3-3. Example of Data

Address	Data
0000h	FF.FF.FF.FF.FF.FF.FF.FF.
0001h	11.11.22.33.44.55.66.77
0002h	11.22.33.44.55.66.77.99
0003h	11.22.AB.44.55.66.77.88
:	:

3.2.2 Full Match with Mask mode

In the Full Match with Mask mode, data can be masked in entry units, and the data that completely matches is searched. In this mode, 4K entry data can be used, and the mask register is valid.

To use the Full Match with Mask mode, set the signal line as shown in Table 3-1 (or set the mode register), and write the search data to the search data register.

Write the mask data that masks the search data to the mask data register. This must be completed before the search data is written to the search data register.

Each bit of the search data register is compared or ignored, depending on the value of the bit of the mask data register at the same bit position.

A bit of the mask data register that is set to 1 is compared with the corresponding bit of the search data register; a bit of the mask register that is reset to 0 is not compared with the corresponding bit of the search data register but ignored.

The search data is compared with a 64-bit value of 4K words of memory cells.

The data of memory cells at addresses 0000h to 0FFFh are masked by the data of memory cells at 1000h to 1FFFh.

If a match data is found, one clock after the search data was written to the search data register in the normal mode (two clocks after in the FF mode), the HIT signal is asserted active. The address of the match data is output to HAD12 to HAD0 if ENHIT_B is set to 0.

The timing to output the hit address can be delayed by inserting WAIT_B.

Example To search data in Table 3-4 from data in Table 3-5

The value of the search data register is ignored when bits 24 to 31 and 8 to 15 are searched from the value of the mask data register.

Data of 0000h is masked by the mask of 1000h and is not compared when bits 48 to 63 are searched. In this way, the data of 0001h is the match data because of the relationship between each data and mask. The match address is 0001h.

The value of 1003h is exactly the same as the value of the search data register, but it is not used as the match data because this area is used as the mask data area in the Full Match with Mask mode.

Table 3-4. Example of Search Data

Search Data Register	Mask Data Register
11.22.33.44.55.66.77.88	FF.FF.FF.FF.00.FF.00.FF

Table 3-5. Example of Data

Address	Data	Address	Mask
0000h	11.22.33.44.55.66.77.BB	1000h	00.00.FF.FF.FF.FF.FF.FF.
0001h	11.22.AA.44.55.66.77.88	1001h	FF.FF.00.FF.FF.FF.FF.FF
0002h	CC.22.33.44.55.66.77.88	1002h	FF.FF.FF.FF.FF.FF.00.00
0003h	99.AA.BB.CC.DD.EE.FF.00	1003h	11.22.33.44.55.66.77.88
:	:	:	:

3.2.3 Longest Prefix Match mode

The Longest Prefix Match mode can search the data with the longest match in the search data, by means of masking in entry units. The 4K-word area of addresses 0000h to 0FFFh is used as an entry data area, and 1000h to 1FFFh are used as a mask data area corresponding to the entry data. In the Longest Prefix Match mode, contiguous bits, starting from the least significant bit, must be masked as the mask data (refer to **2.1.2 Full Match with Mask/Longest Prefix Match mode**). The mask data register is valid, and the masking set by this register is valid for all the entries. The contiguous bits of the mask data register must be also masked, starting from the least significant bit. To connect two or more μPD98421 chips, the values of the mask data registers of all the chips must be the same.

Searching in the Longest Prefix Match mode is started by setting the signal lines as shown in Table 3-1 (or setting the mode register) and writing the search data to the search data register. Two clocks after the search has been started in the normal mode (four clocks after in the FF mode), the HIT_B pin is asserted active. The address of the match data is output to the HAD12 to HAD0 pins if ENHIT_B is set to 0.

The timing to output the hit address can be delayed by inserting WAIT_B.

If two or more match data are found during the search operation, the ERR_B pin goes low, and the output to the HAD12 to HAD0 pins is invalid. If no match data is found, both the HIT_B and ERR_B pins go high.

The mask data that masks search data is written to the mask data register. This must be completed before the search data is written to the search data register.

The search data is compared with a 64-bit value of 4K words of memory cells.

The data of the memory cells at addresses 0000h to 0FFFh is masked by the data of memory cells at addresses 1000h to 1FFFh.

Unlike the other two modes, the data of a memory cell having a bit string with the longest successive match in the search data, starting from the MSB, is the match data.

Example 1 To search with only one chip

The data shown in Table 3-6 is searched from the data of the memory cells shown in Table 3-7.

The value of the mask data register is masked after a value has been written to the search data register. Because all the bits of the mask data are 1, all the bits of the search data register are compared when searched.

The data stored to each memory cell is compared in the same manner as in the Full Match with Mask mode.

Of the matching data, that which has the longest number of bits that match is the final match data. In this example, it is the data of 0001h.

Table 3-6. Example of Search Data

Search Data Register	Mask Data Register
11.22.33.44.55.66.77.88	FF.FF.FF.FF.FF.FF.FF.FF

Table 3-7. Example of Data

Address	Data	Address	Mask
0000h	11.22.33.44.00.00.00.00	1000h	FF.FF.FF.FF.00.00.00.00
0001h	11.22.33.44.55.66.77.00	1001h	FF.FF.FF.FF.FF.FF.FF.00
0002h	11.22.33.44.55.00.00.00	1002h	FF.FF.FF.FF.FF.00.00.00
0003h	11.22.33.44.55.66.77.AA	1003h	FF.FF.FF.FF.FF.FF.00.00
:	:	:	:

Even when two or more μPD98421 chips are connected, the data with the longest match in the search data can be searched from all the μPD98421s. This can be done by connecting the SMD63 to SMD0 pins of all the chips.

When two or more chips are connected, make sure that the values of the mask data registers of all the chips are the same.

Example 2 To search with two or more chips

Data in Table 3-8 is searched from the data of the memory cells shown in Tables 3-9 to 3-11. These tables show different μPD98421 chips.

When searching is started, 0001h of chip 1, 0002h of chip 2, and 0001h of chip 3 match as the match addresses. In this case, 0002h of chip 2 in Table 3-10 has the shortest mask bit. Therefore, the data of 0002h of chip 2 is the match data. At this time, only the HIT_B pin of chip 2 goes low; the HIT_B pins of chips 1 and 3 go high.

Table 3-8. Search Data

Search Data Register	Mask Data Register
6E.13.01.22.5F.C2.77.E8	FF.FF.FF.FF.FF.FF.FF.FF

Table 3-9. Memory Cells of Chip 1

Address	Data	Address	Mask
0000h	11.22.33.44.55.00.00.00	1000h	FF.FF.FF.FF.FF.00.00.00
0001h	6E.13.01.22.5F.C2.77.00	1001h	FF.FF.FF.FF.FF.FF.00.00
0002h	6E.13.01.22.00.00.00.00	1002h	FF.FF.FF.FF.00.00.00.00
0003h	6F.FF.FF.FF.FF.00.00.00	1003h	FF.FF.FF.FF.FF.00.00.00
:	:	:	:

Table 3-10. Memory Cells of Chip 2

Address	Data	Address	Mask
0000h	11.22.33.44.00.00.00	1000h	FF.FF.FF.FF.00.00.00.00
0001h	6E.13.01.22.5F.C2.00.00	1001h	FF.FF.FF.FF.FF.FF.00.00
0002h	6E.13.01.22.5F.C2.77.00	1002h	FF.FF.FF.FF.FF.FF.FF.00
0003h	6D.FF.FE.EF.FF.FF.00.00	1003h	FF.FF.FF.FF.FF.FF.00.00
:	:	:	:

Table 3-11. Memory Cells of Chip 3

Address	Data	Address	Mask
0000h	6E.13.01.22.5F.C2.AA.00	1000h	FF.FF.FF.FF.FF.FF.FF.00
0001h	6E.13.01.22.5F.C2.00.00	1001h	FF.FF.FF.FF.FF.FF.00.00
0002h	6E.13.01.22.5F.BF.00.00	1002h	FF.FF.FF.FF.FF.FF.00.00
0003h	6E.13.01.22.61.01.00.00	1003h	FF.FF.FF.FF.FF.FF.00.00
:	:	:	:

3.2.4 Other points to be noted

- Do not change the mode by using the MEM, FULL, and FMSK pins in a mode that operates with two or more clock cycles. Similarly, do not change A12 to A0.

  Remark Modes that operate with two or more clock cycles
  In normal mode: Longest Prefix Match mode
  In FF mode: Memory/register read, Full Match mode, Full Match with Mask mode, and Longest Prefix Match mode

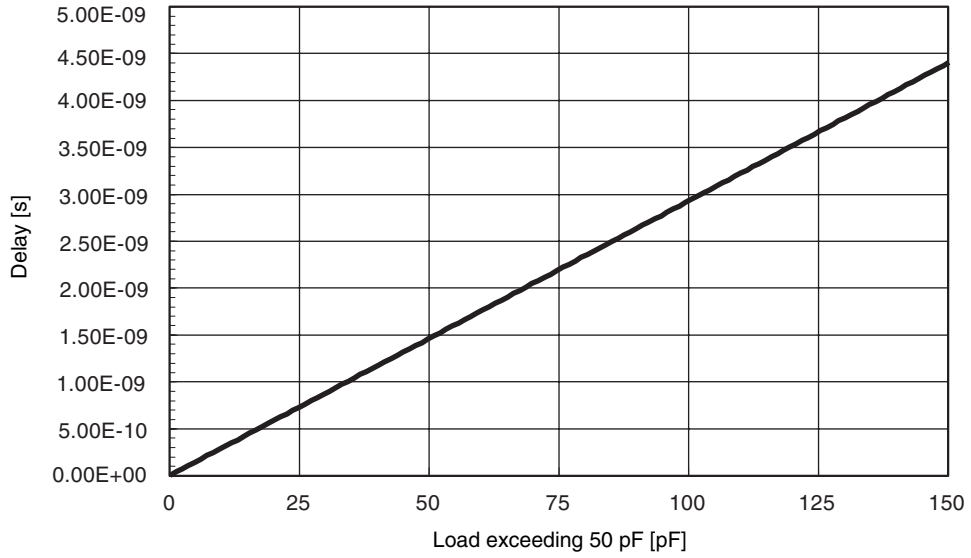
- Write to the NOP register for one or more clocks when changing the operation and the search mode.
- Create an external circuit in which RESET_B becomes low after power application.
- After releasing reset, input at least 2 CLK or more NOP commands continuously.
- When a search operation is stopped temporarily using CE (CE_B) during a continuous search operation, almost the same power is consumed as during a search operation. In this case, shift into no-operation mode by writing to the NOP register or inserting a wait.
- When performing a continuous search operation in the normal mode, make the total search frequency 66% or below.

- Cautions when connecting multiple μPD98421s

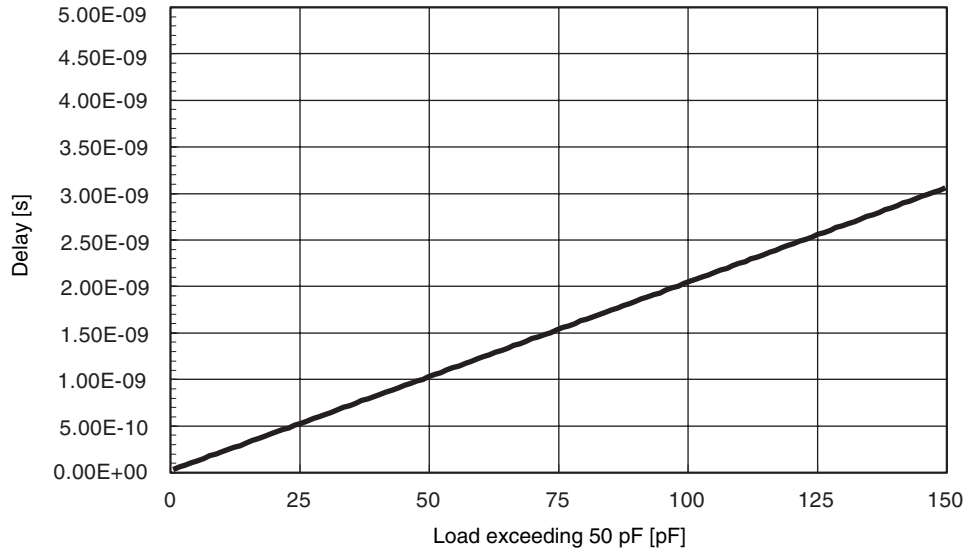
  The output load capacitance in the AC characteristics described later is 50 pF, so if the load capacitance exceeds 50 pF through the connection of multiple devices, the delay amount shown in the figure below must be added as an output delay.

  Reference this delay value when designing external circuits. The delay value in the figure is only that of the output buffer. Note also that the level at which output of the delay value is determined is V_{IH} (2.0 V) for the rising delay and V_{IL} (0.8 V) for the falling delay.

Output Buffer Load Dependence (typ.) @ Rising Delay



Output Buffer Load Dependence (typ.) @ Falling Delay



4. ELECTRICAL SPECIFICATIONS

All the rated values below are when the μPD98421 is cooled at a wind velocity of 2 m/s.

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}		–0.5 to +4.6	V
Input voltage	V_I		–0.5 to +V_{DD} + 0.5	V
I/O voltage	V_{IO}		–0.5 to +V_{DD} + 0.5	V
Operating ambient temperature	T_A		0 to 70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		3.15	3.3	3.45	V
Input voltage, high	V_{IH1}	Other than CLK, RESET_B	2.0		V_{DD}	V
	V_{IH2}	CLK, RESET_B	2.4		V_{DD}	V
Input voltage, low	V_{IL1}	Other than CLK, RESET_B	0		0.8	V
	V_{IL2}	CLK, RESET_B	0		0.4	V
Operating ambient temperature	T_A	Cooled at a wind velocity of 2 m/s or more	0		70	°C

DC Characteristics (T_A = 0 to +70°C, V_{DD} = 3.3 V ±0.15 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH}	I_{OH} = –4.0 mA	2.4			V
Output voltage, low	V_{OL}	I_{OL} = 8.0 mA			0.4	V
Operating current	I_{DD} Note	f_{clk} = 33 MHz (normal mode)			1150	mA
		f_{clk} = 50 MHz (FF mode)			1150	mA
Input leakage current	I_{LI}	V_I = 0 V to V_{DD}			±10	μA
Output leakage current	I_{LO}	V_{IO} = 0 V to V_{DD} Output: not selected			±10	μA
Pull-up resistance (HAD and SMD pins)	R_{PU}	V_I = 0 V	25	50	150	kΩ

Note When performing a continuous search operation in the normal mode, make the total search frequency 66% or below.

Capacitance

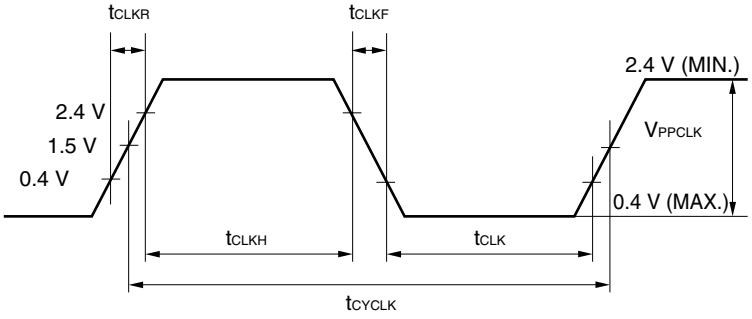
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V, f = 1 MHz			10	pF
Output capacitance	C_{OUT}	V_{IN} = 0 V, f = 1 MHz			10	pF
I/O capacitance	$C_{I/O}$	V_{IN} = 0 V, f = 1 MHz			10	pF

AC Characteristics (T_A = 0 to 70°C, V_{DD} = 3.3 V ±0.15 V)

All the values below are at an output load capacitance of 50 pF.

CLK input

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CLK cycle time	t_{CYCLK}	Normal mode	30		125	ns
		FF mode	20		125	ns
CLK high-level width	t_{CLKH}	Normal mode	13			ns
		FF mode	9			ns
CLK low-level width	t_{CLKL}	Normal mode	13			ns
		FF mode	9			ns
CLK rise time	t_{CLKR}				3	ns
CLK fall time	t_{CLKF}				3	ns



RESET input

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RESET_B low-level width	t_{WRSTL}		$t_{CYCLK} \times 2$			ns

CE and CE_B operations

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CE ↑ → DATA valid time	$t_{DCEDATA}$				10	ns
CE_B ↓ → DATA valid time						
CE ↑ → HAD valid time	t_{DCEHAD}				10	ns
CE_B ↓ → HAD valid time						
CE ↑ → ERR_B valid time	t_{DCEERR}				10	ns
CE_B ↓ → ERR_B valid time						
CE ↑ → SMD valid time	t_{DCESMD}				10	ns
CE_B ↓ → SMD valid time						
CE ↓ → DATA float time	$t_{FCEDATA}$				10	ns
CE_B ↑ → DATA float time						
CE ↓ → HAD float time	t_{FCEHAD}				10	ns
CE_B ↑ → HAD float time						
CE ↓ → ERR_B float time	t_{FCEERR}				10	ns
CE_B ↑ → ERR_B float time						
CE ↓ → SMD float time	t_{FCESMD}				10	ns
CE_B ↑ → SMD float time						

Search/memory operations (1/2)

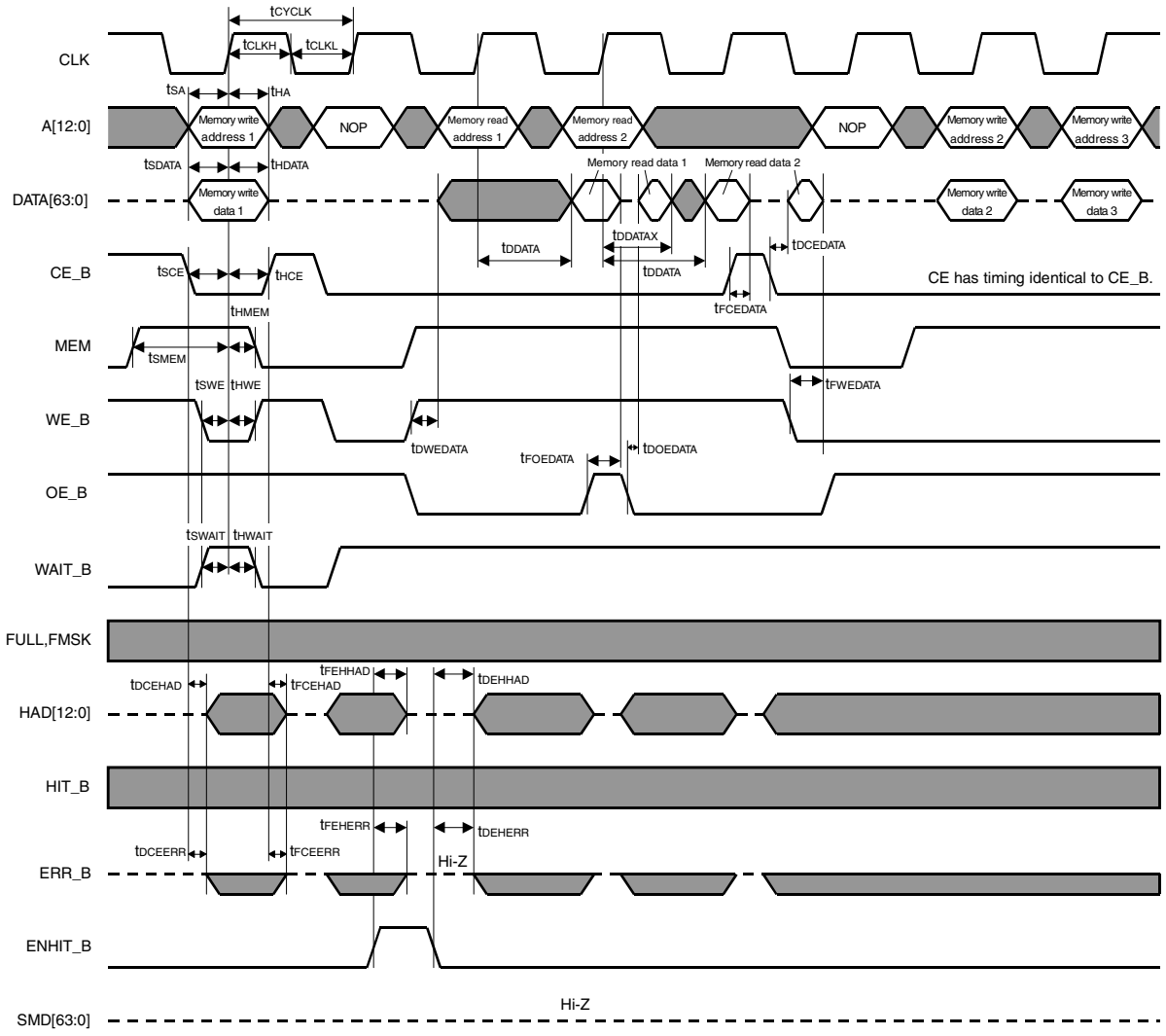
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time	t_{SA}		4			ns
Address hold time	t_{HA}		4			ns
Data setup time	t_{SDATA}		4			ns
Data hold time	t_{HDATA}		4			ns
CE, CE_B setup time	t_{SCE}		4			ns
CE, CE_B hold time	t_{HCE}		3			ns
MEM setup time	t_{SMEM}		3			ns
MEM hold time	t_{HMEM}		3			ns
WE_B setup time	t_{SWE}		3			ns
WE_B hold time	t_{DWE}		3			ns
WAIT_B setup time	t_{SWAIT}		3			ns
WAIT_B hold time	t_{HWAIT}		3			ns
FULL, FMSK setup time	t_{SMODE}		4			ns
FULL, FMSK hold time	t_{HMODE}		3			ns
Delay time from CLK ↑ to DATA	t_{DDATA}	Normal mode			26	ns
		FF mode			10	ns
CLK ↑ → DATA invalid time	t_{DDATAX}	Normal mode	4			ns
WE_B ↑ → DATA valid time	$t_{DWEDATA}$				10	ns
WE_B ↓ → DATA float time	$t_{FWEDATA}$				10	ns
OE_B ↓ → DATA valid time	$t_{DOEDATA}$				10	ns
OE_B ↑ → DATA float time	$t_{FOEDATA}$				10	ns
ENHIT_B ↓ → HAD valid time	t_{DEHHAD}				10	ns
ENHIT_B ↑ → HAD float time	t_{FEHHAD}				10	ns
ENHIT_B ↓ → ERR_B valid time	t_{DEHERR}				10	ns
ENHIT_B ↑ → ERR_B float time	t_{FEHERR}				10	ns
CLK ↑ → HAD valid time	t_{DHAD}	Normal mode			26	ns
		FF mode			10	ns
CLK ↑ → HAD float time	t_{FHAD}	Normal mode			26	ns
		FF mode			10	ns
CLK ↑ → HAD invalid time	t_{DHADX}		5			ns
CLK ↑ → HIT_B delay time	t_{DHIT}	Normal mode			26	ns
		FF mode			10	ns
CLK ↑ → HIT_B invalid time	t_{DHITX}		5			ns
CLK ↑ → ERR_B valid time	t_{DERR}	Normal mode			26	ns
		FF mode			10	ns
CLK ↑ → ERR_B float time	t_{FERR}	Normal mode			26	ns
		FF mode			10	ns
CLK ↑ → ERR_B invalid time	t_{DERRX}		5			ns
SMD setup time	t_{SSMD}		2			ns

Search/memory operations (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SMD hold time	t_{HSMD}		3			ns
CLK ↑ → SMD low-level valid time	t_{DSMDL1} Note	Normal mode			26	ns
		FF mode			10	ns
CLK ↓ → SMD low-level valid time	t_{DSMDL2} Note	Normal mode			12	ns
CLK ↓ → SMD high-level valid time	t_{DSMDH1}	Normal mode	2		13	ns
CLK ↑ → SMD high-level valid time	t_{DSMDH2}	FF mode	2		10	ns
CLK ↑ → SMD float time	t_{FSMD}		2		10	ns

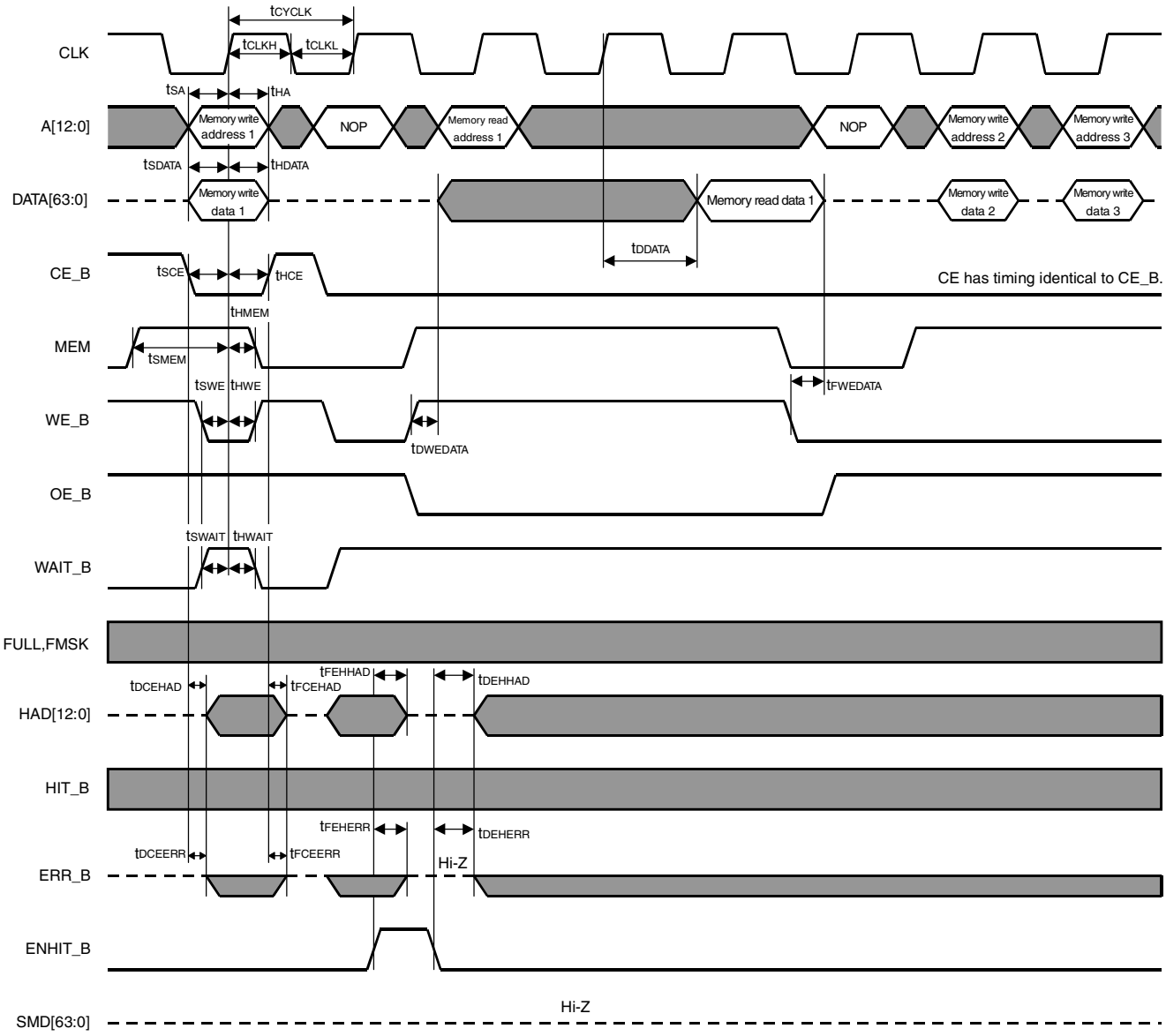
Note The SMD low-level valid time satisfies either the t_{DSMDL1} or t_{DSMDL2} value.

(1) Memory access (normal mode)



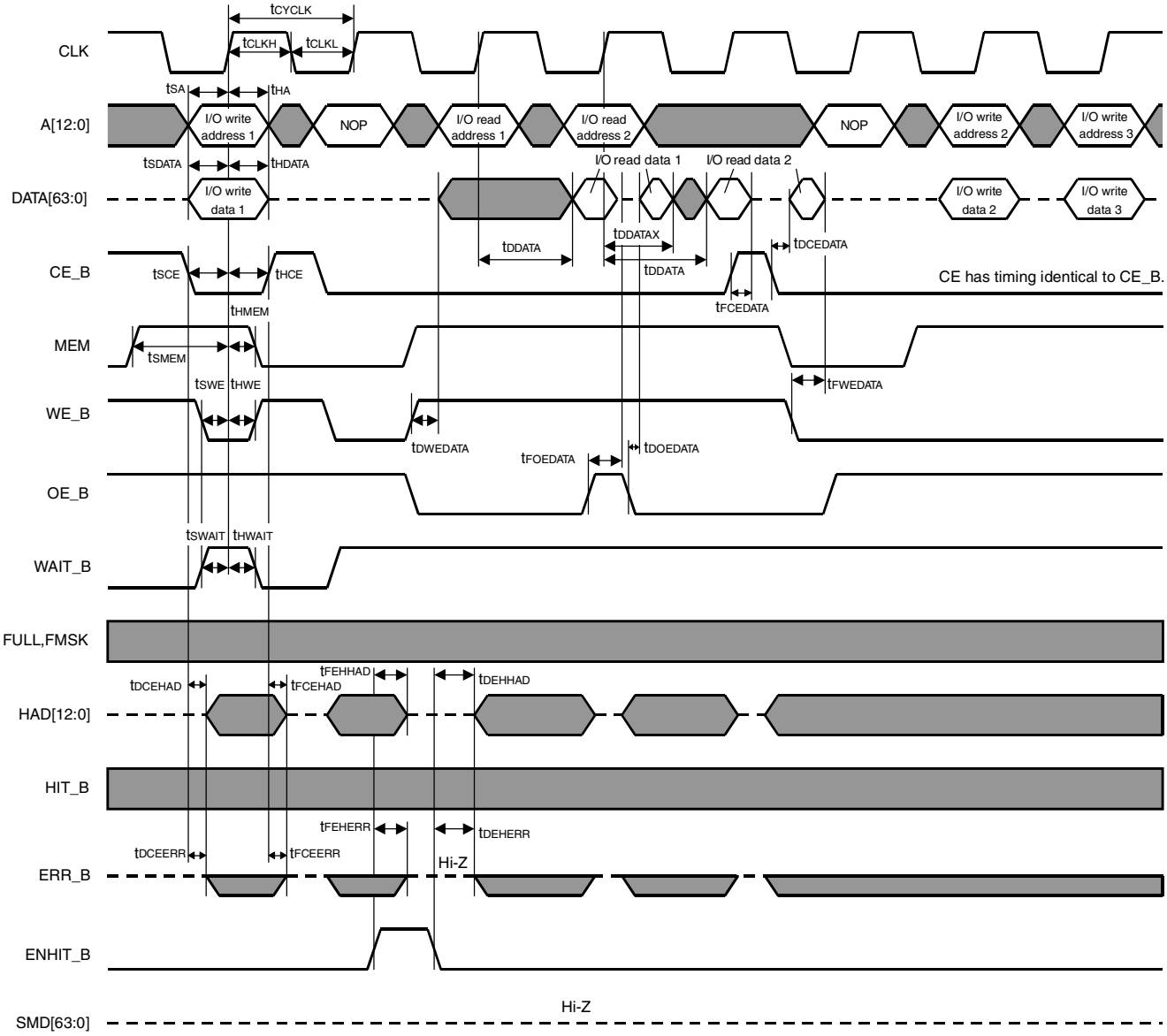
Remark CE is the inversion of CE_B.

(2) Memory access (FF mode)



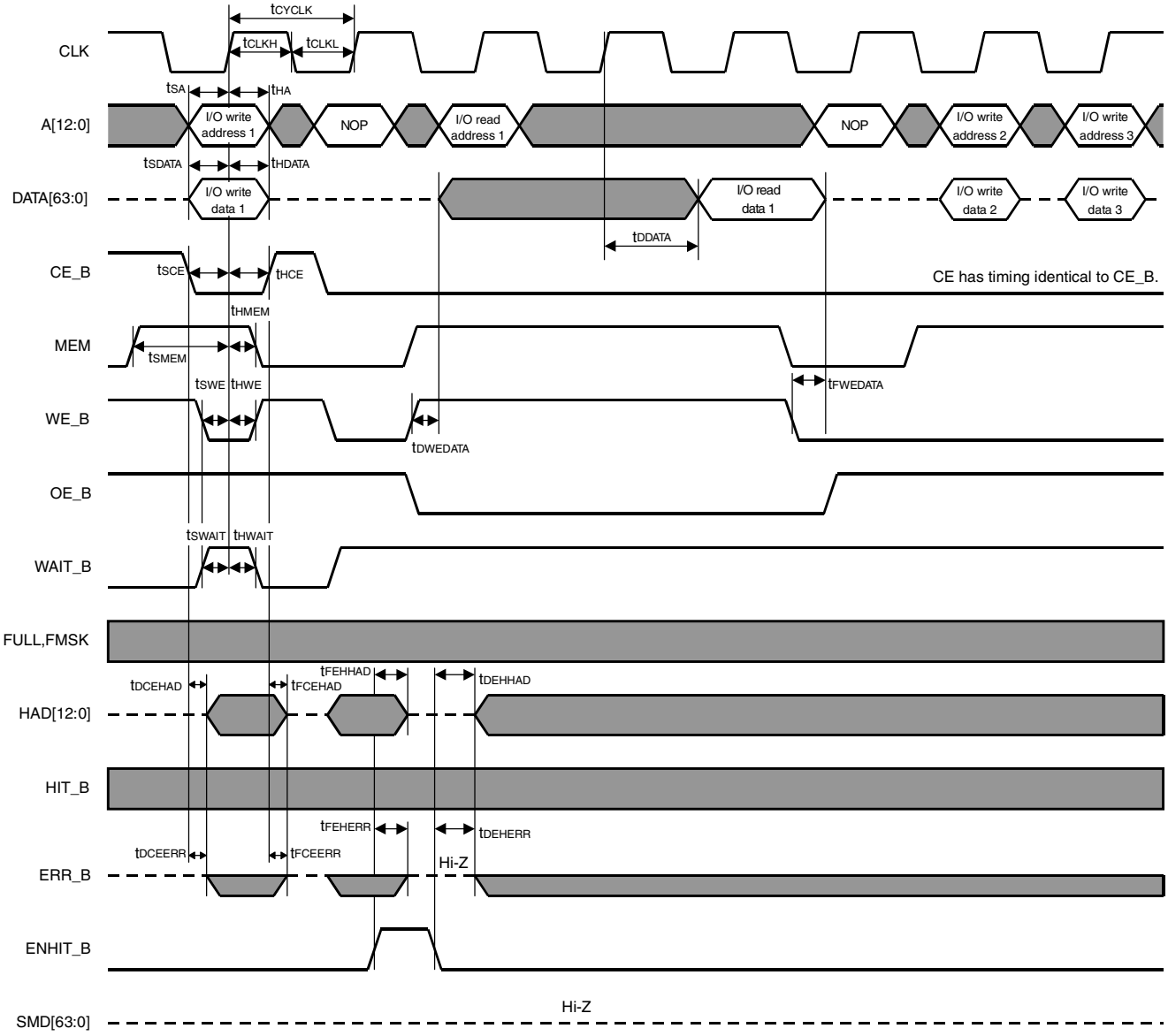
Remark CE is the inversion of CE_B.

(3) I/O access (normal mode)



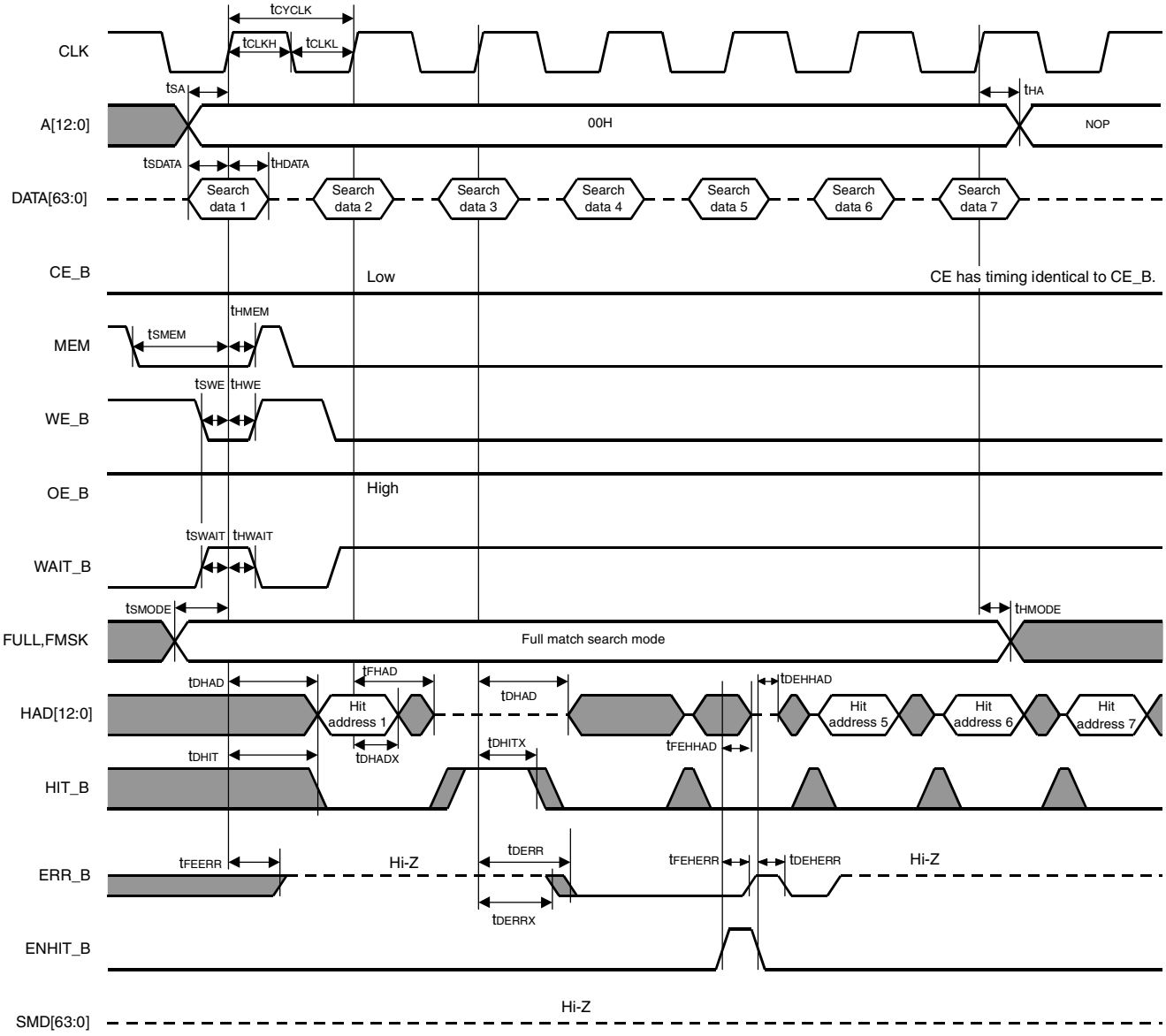
Remark CE is the inversion of CE_B.

(4) I/O access (FF mode)



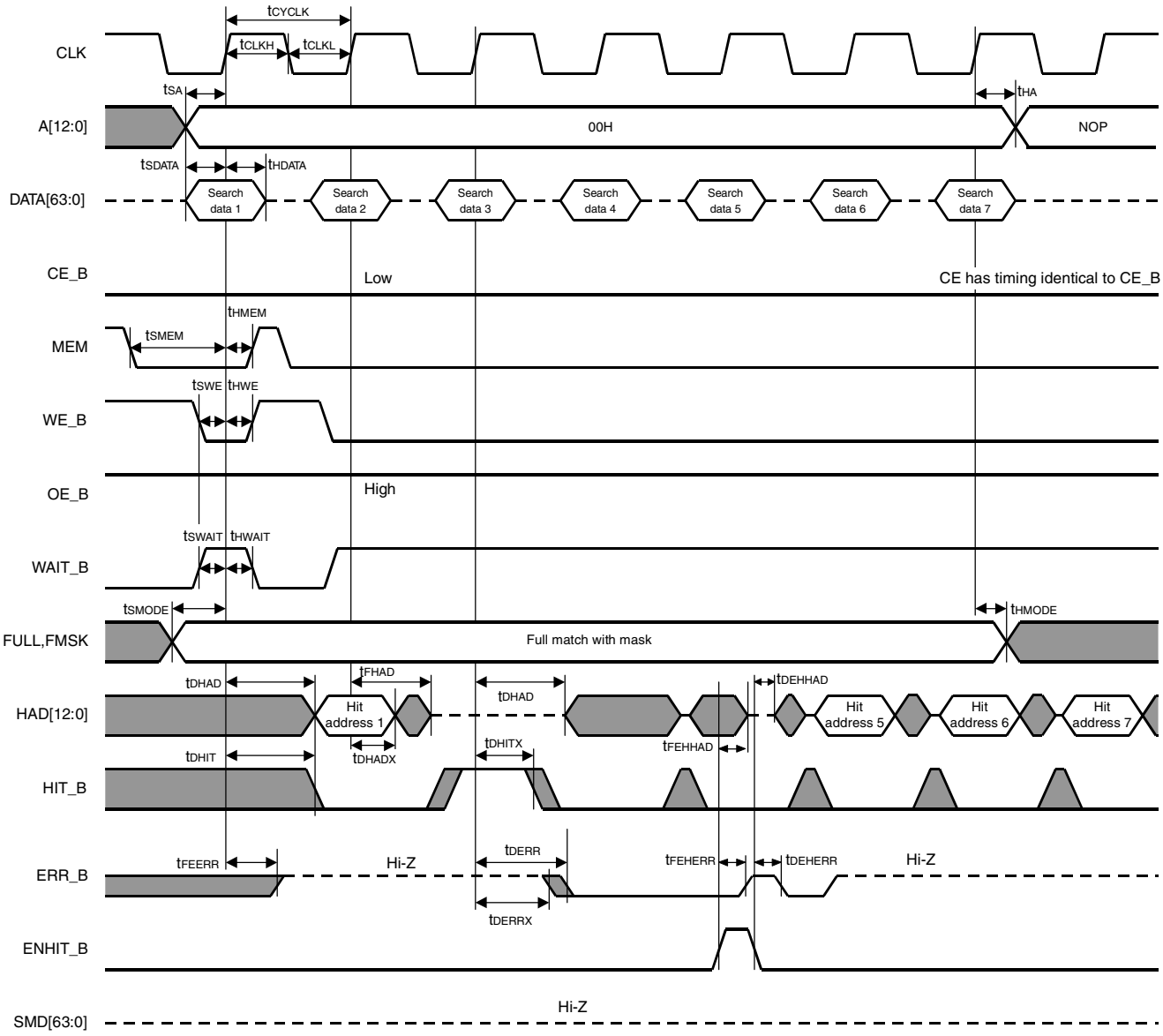
Remark CE is the inversion of CE_B.

(5) Full Match search (normal mode)



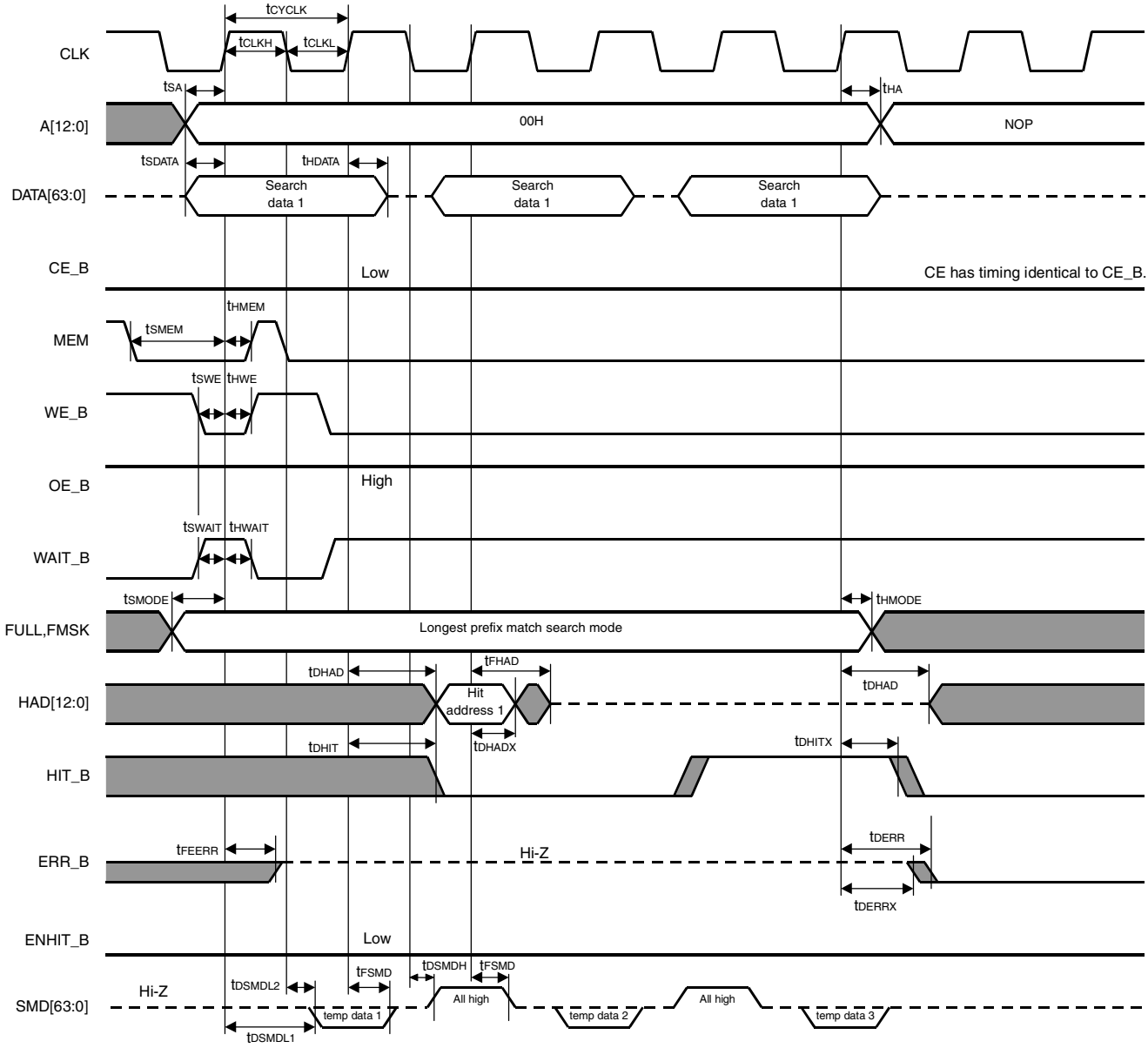
Remark CE is the inversion of CE_B.

(6) Full Match search with Mask (normal mode)



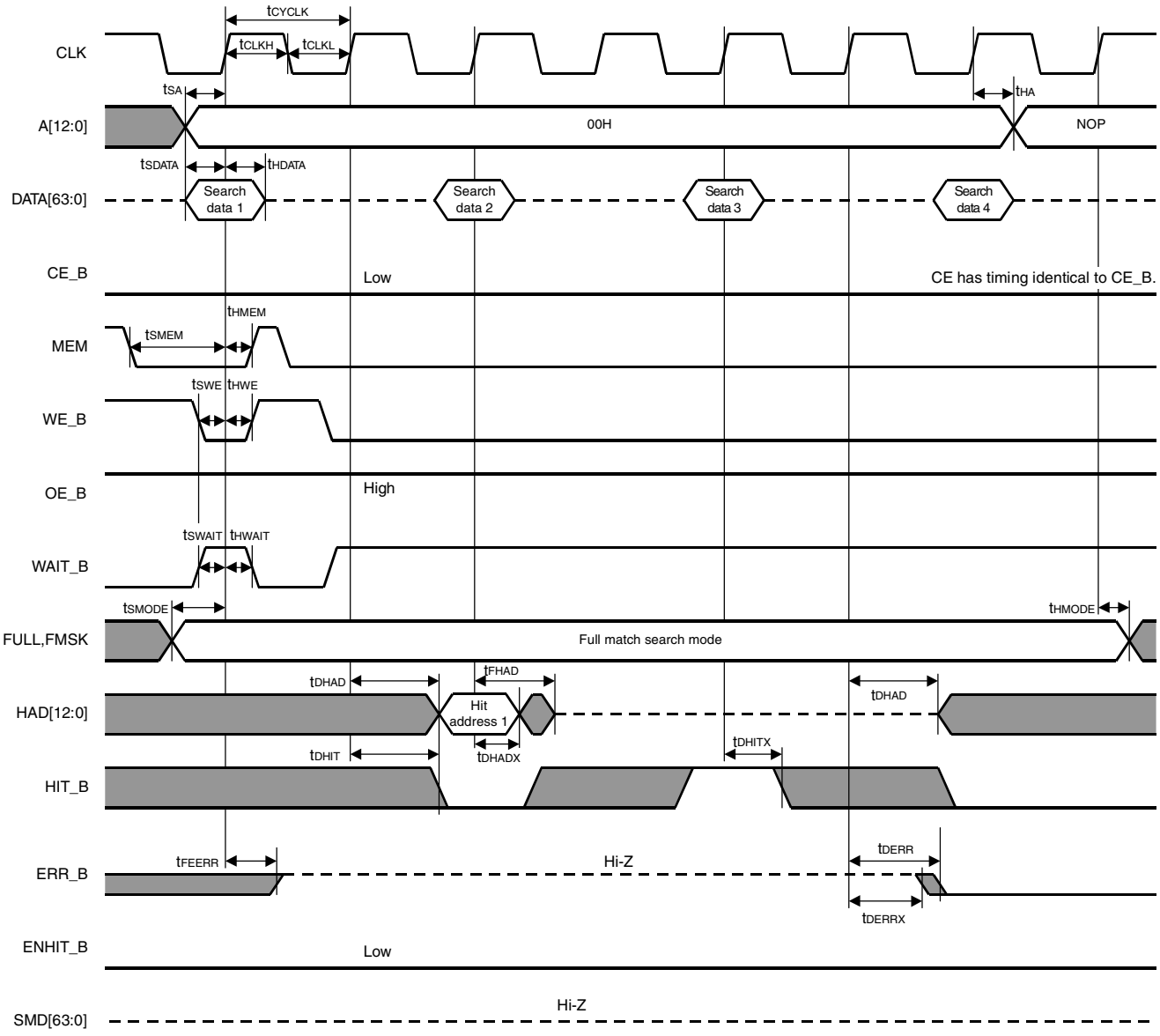
Remark CE is the inversion of CE_B.

(7) Longest Prefix Match search (normal mode)



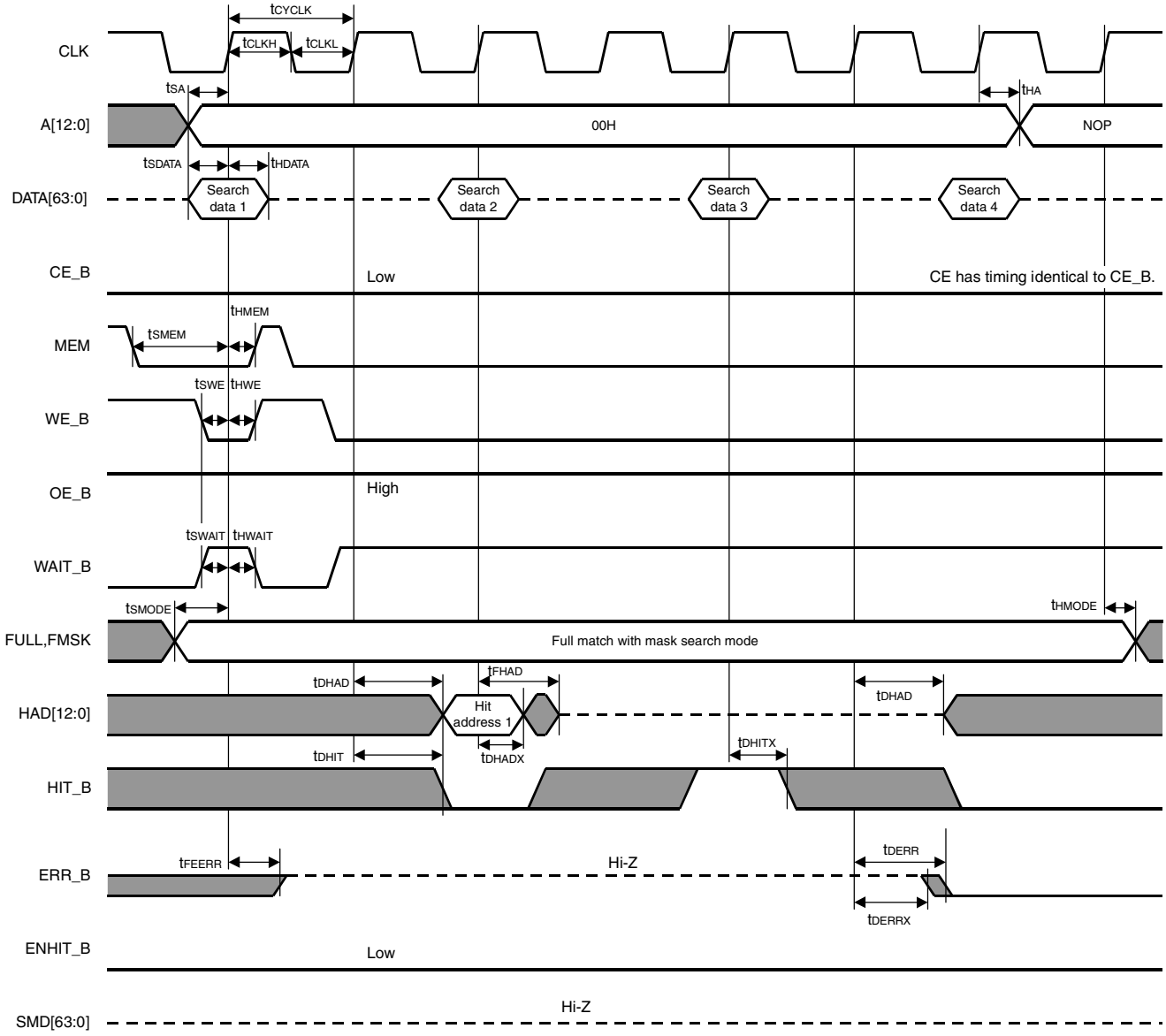
Remark CE is the inversion of CE_B.

(8) Full Match search (FF mode)



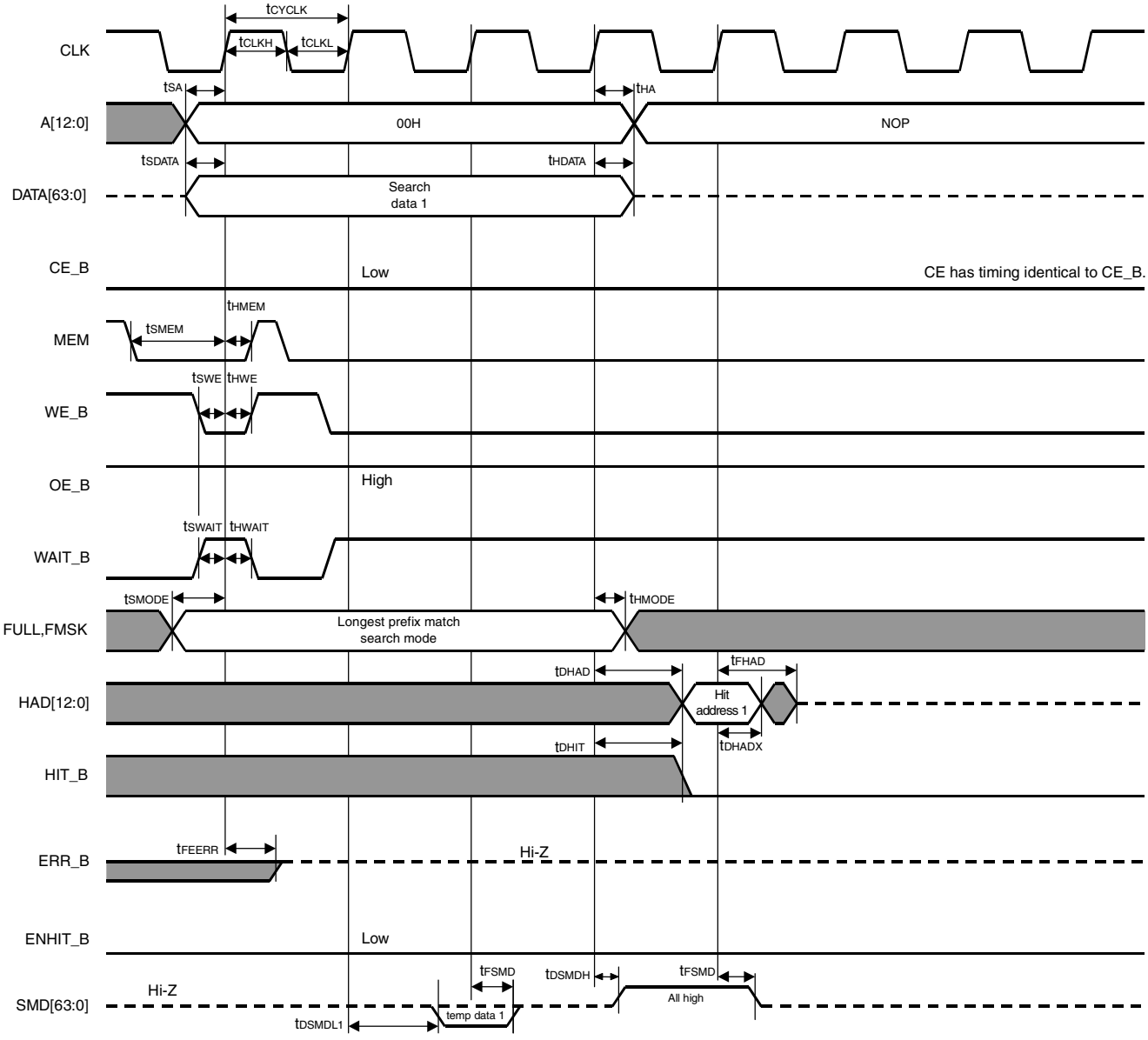
Remark CE is the inversion of CE_B.

(9) Full Match search with Mask (FF mode)



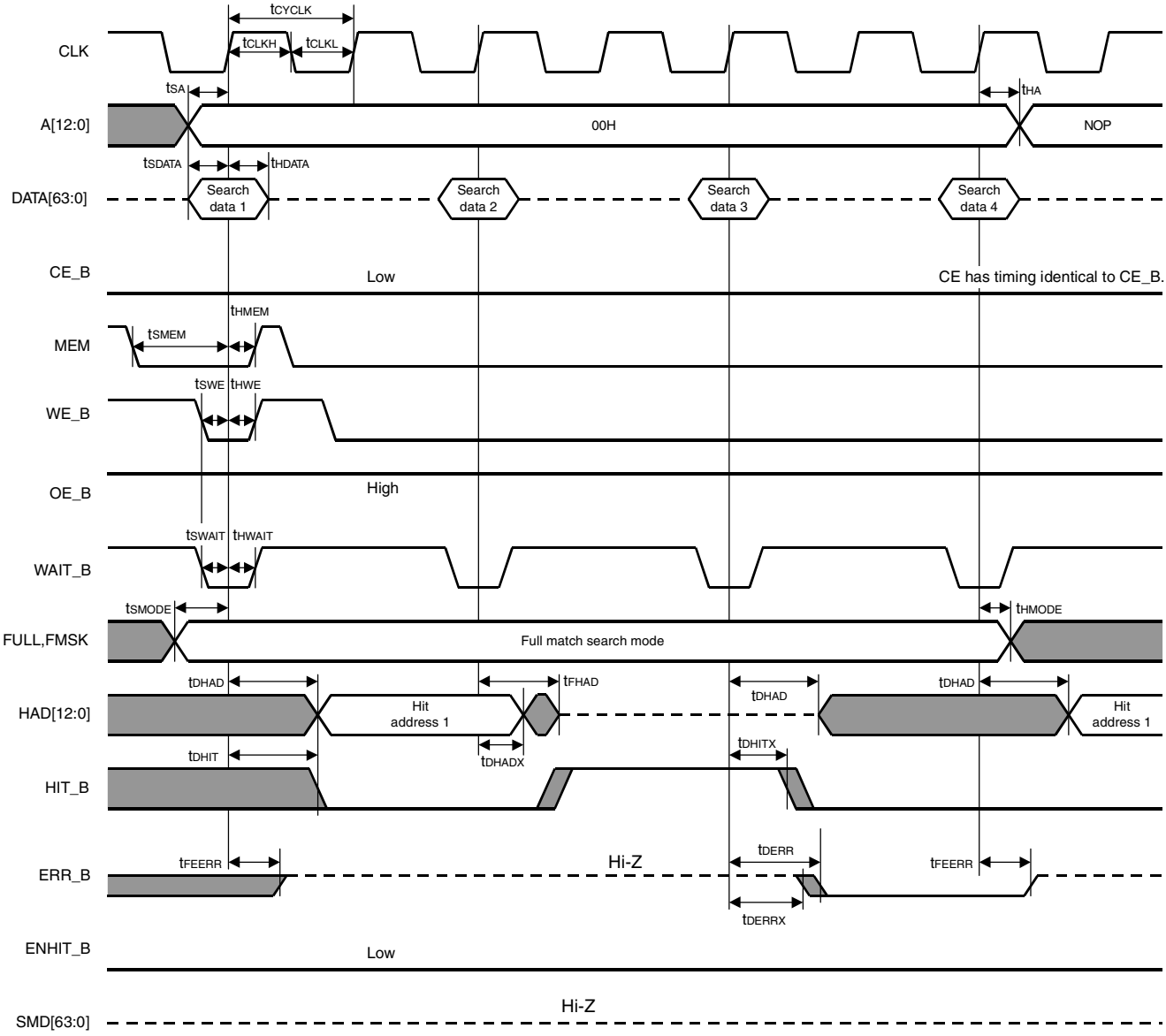
Remark CE is the inversion of CE_B.

(10) Longest Prefix Match search (FF mode)



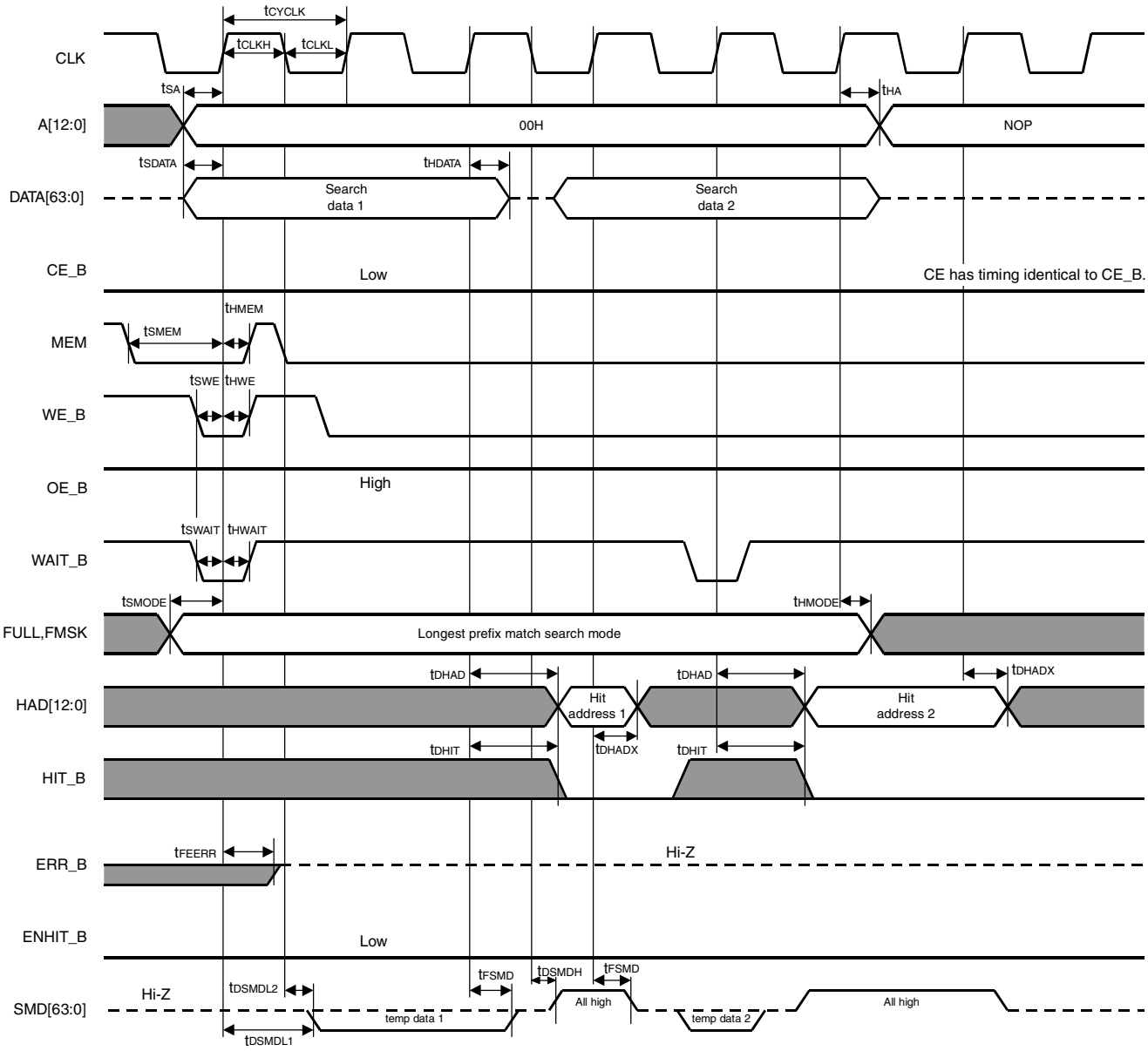
Remark CE is the inversion of CE_B.

(11) Full Match search (normal mode, insertion wait)



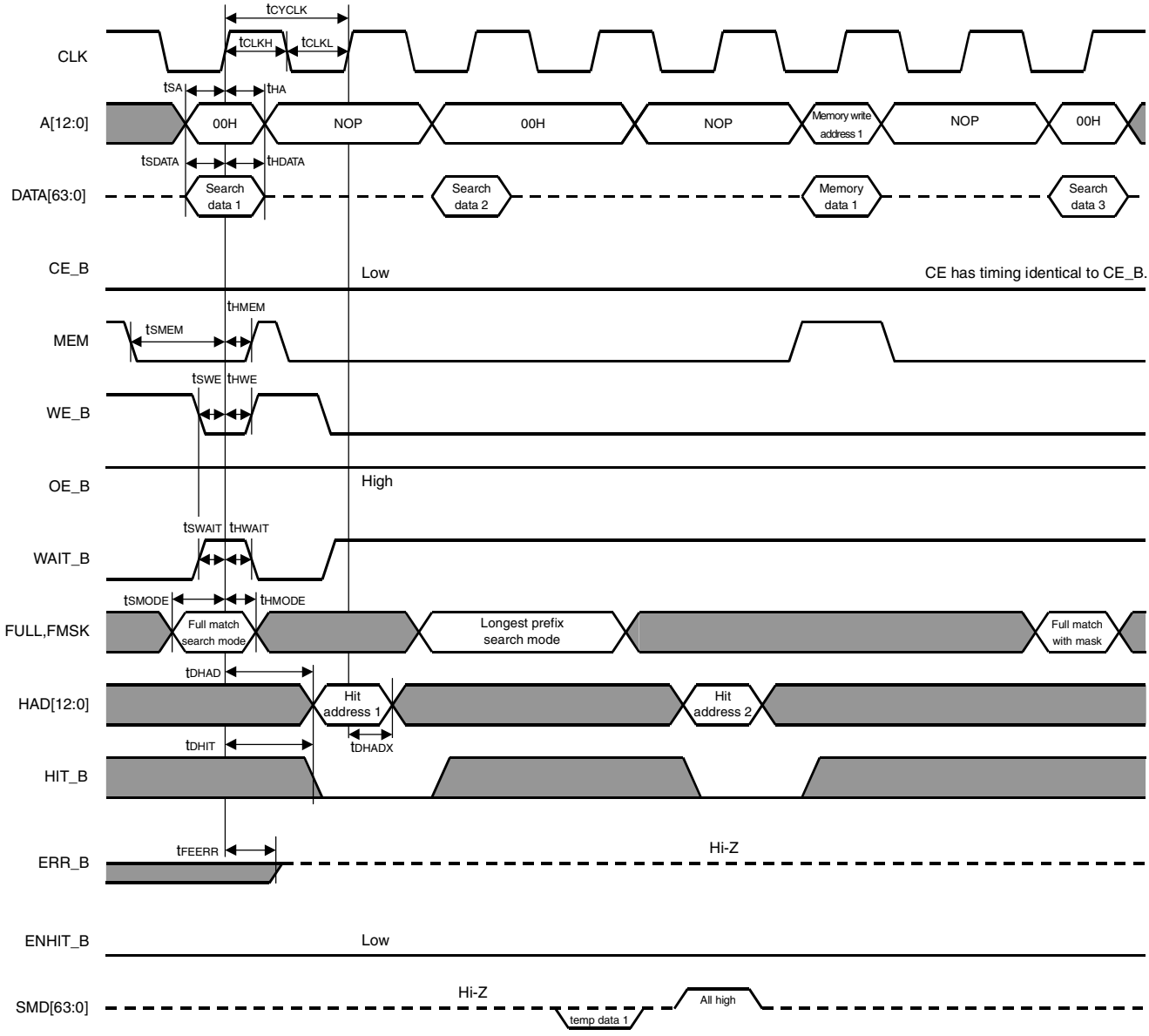
Remark CE is the inversion of CE_B.

(12) Longest Prefix Match search (normal mode, insertion wait)



Remark CE is the inversion of CE_B.

(13) Search → Memory access → Search (normal mode)



Remark CE is the inversion of CE_B.

5. RECOMMENDED SOLDERING CONDITIONS

The μPD98421 should be soldered and mounted under the following recommended conditions. For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual** (**C10535E**).

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Surface-mount type

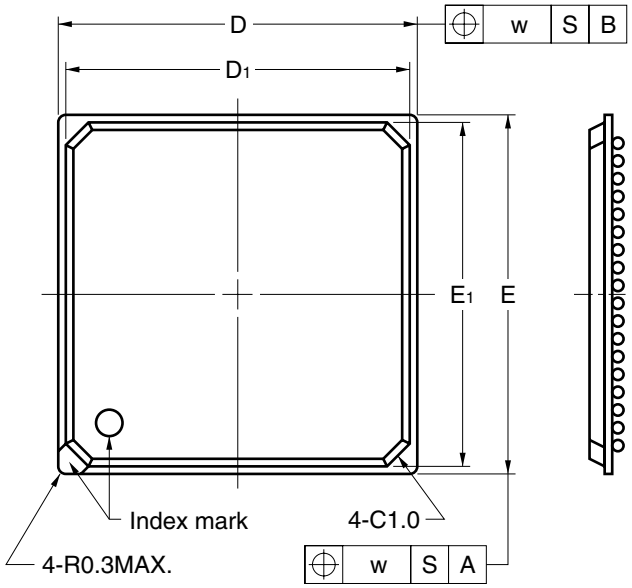
- **μPD98421F1-GA1: 240-pin plastic FBGA (16 × 16)**

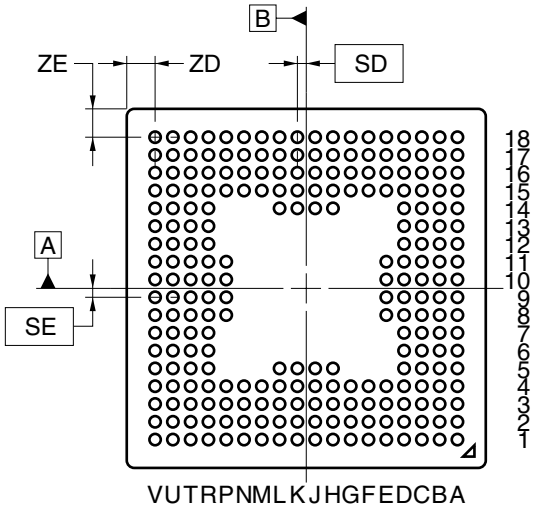
Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours)	IR30-103-2

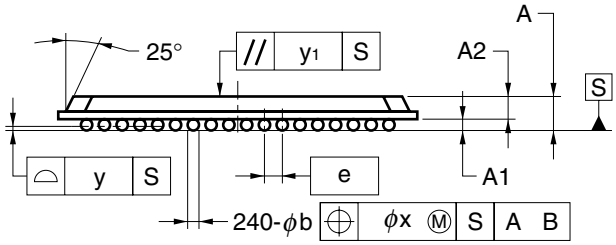
Note After opening a dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

6. PACKAGE DRAWING

240-PIN PLASTIC FBGA (16x16)







ITEM	MILLIMETERS
D	16.00±0.10
D_1	15.4
E	16.00±0.10
E_1	15.4
w	0.20
e	0.80
A	1.31±0.15
A_1	0.35±0.10
A_2	0.96
b	$0.50^{+0.05}_{-0.10}$
x	0.08
y	0.10
y_1	0.20
SD	0.40
SE	0.40
ZD	1.2
ZE	1.2

P240F1-80-GA1

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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