NEC

MOS INTEGRATED CIRCUIT

μPD98410

1.2G ATM SWITCH LSI

DESCRIPTION

The μPD98410 (NEASCOT-X10™) is an LSI integrating ATM switch functions on a single chip. It has four UTOPIA level2 interfaces and can switch 24 × 24 circuits by using a multi-PHY connection. This LSI also realizes a switching capacity of 1.2 Gbps by employing a common buffer type non-blocking switch and by using an externally connected SRAM to buffer cells.

FEATURES

- Conforms to ATM FORUM UNI Version 3.1 & 4.0
- Realizes all switching functions on one chip
- Non-blocking, switching capacity of 1.2 Gbps
- Switches 24 logical ports via four UTOPIA level2 (8 bits/40 MHz) interfaces
- Multiple speeds (155 Mbps, 52 Mbps, 25 Mbps, etc.)
- Supports 16K/32K/64K VP/VC and 1K/2K/4K multi-cast VP/VC
- Common buffer architecture using standard SRAM
- Cell buffer capacity: 12.8K/25.6K/51.2K cells
- Supports four QOS classes (CBR, VBR, ABR, and UBR)
- ABR traffic control (binary mode)
- Supports EPD (Early Packet Discard) and PPD (Partial Packet Discard)
- +3.3-V single power source (Can be also directly connected to +5 V TTL level signal)
- Test function: JTAG (IEEE 1149.1) supported

ORDERING INFORMATION

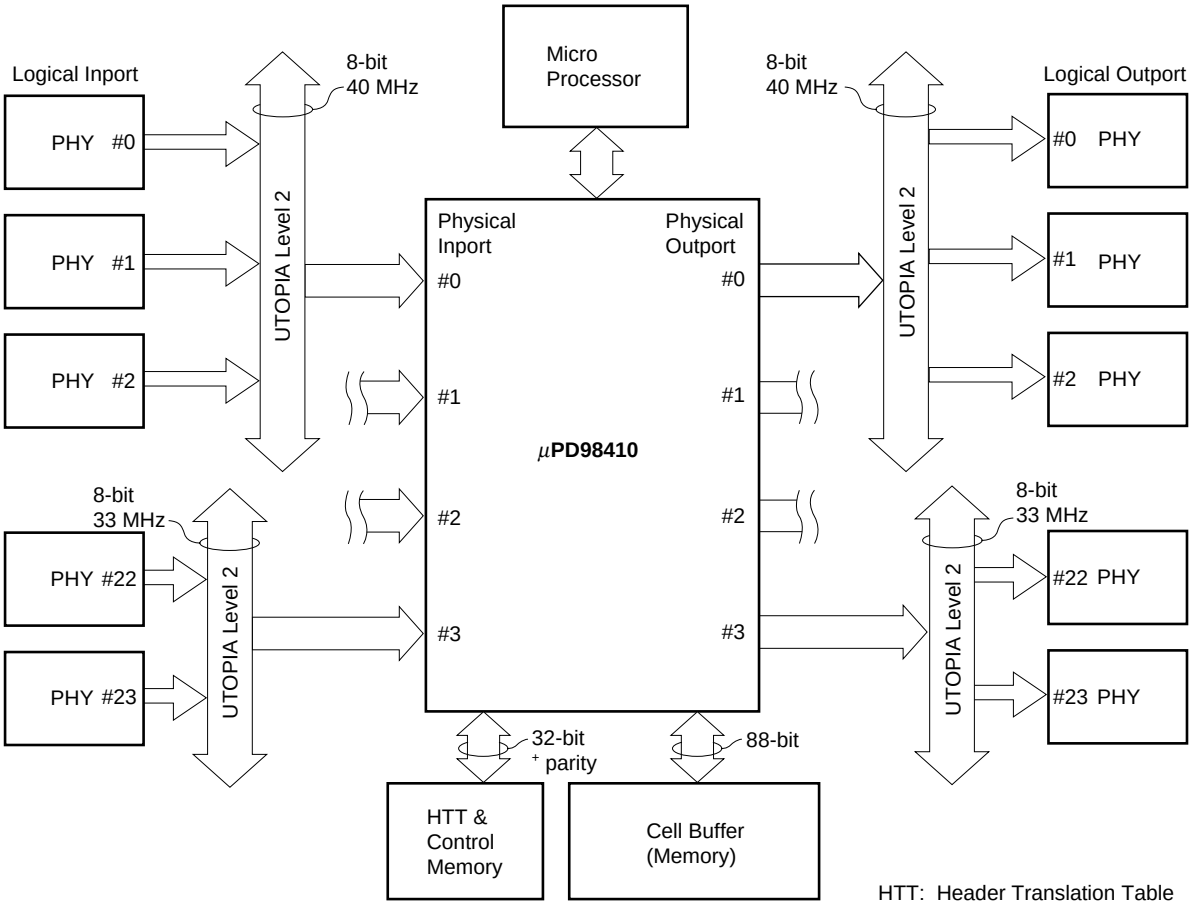
Part Number	Package
μPD98410S2-K6	580-pin plastic BGA (45 × 45 mm)

Remark In this document, active-low pins are indicated as xxx_B (_B following a pin name).

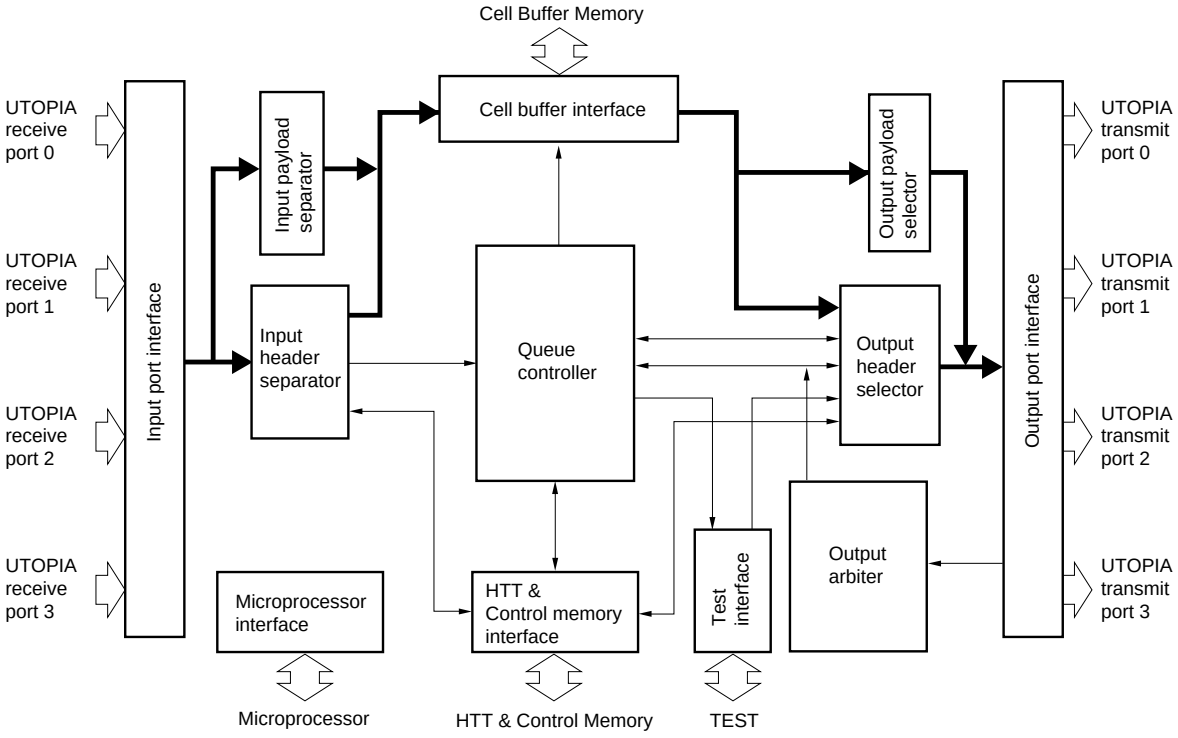
Document No. S12624EJ2V0DS00 (2nd edition)
Date Published June 1998 N CP(K)
Printed in Japan

SYSTEM CONFIGURATION EXAMPLE (APPLICATION)

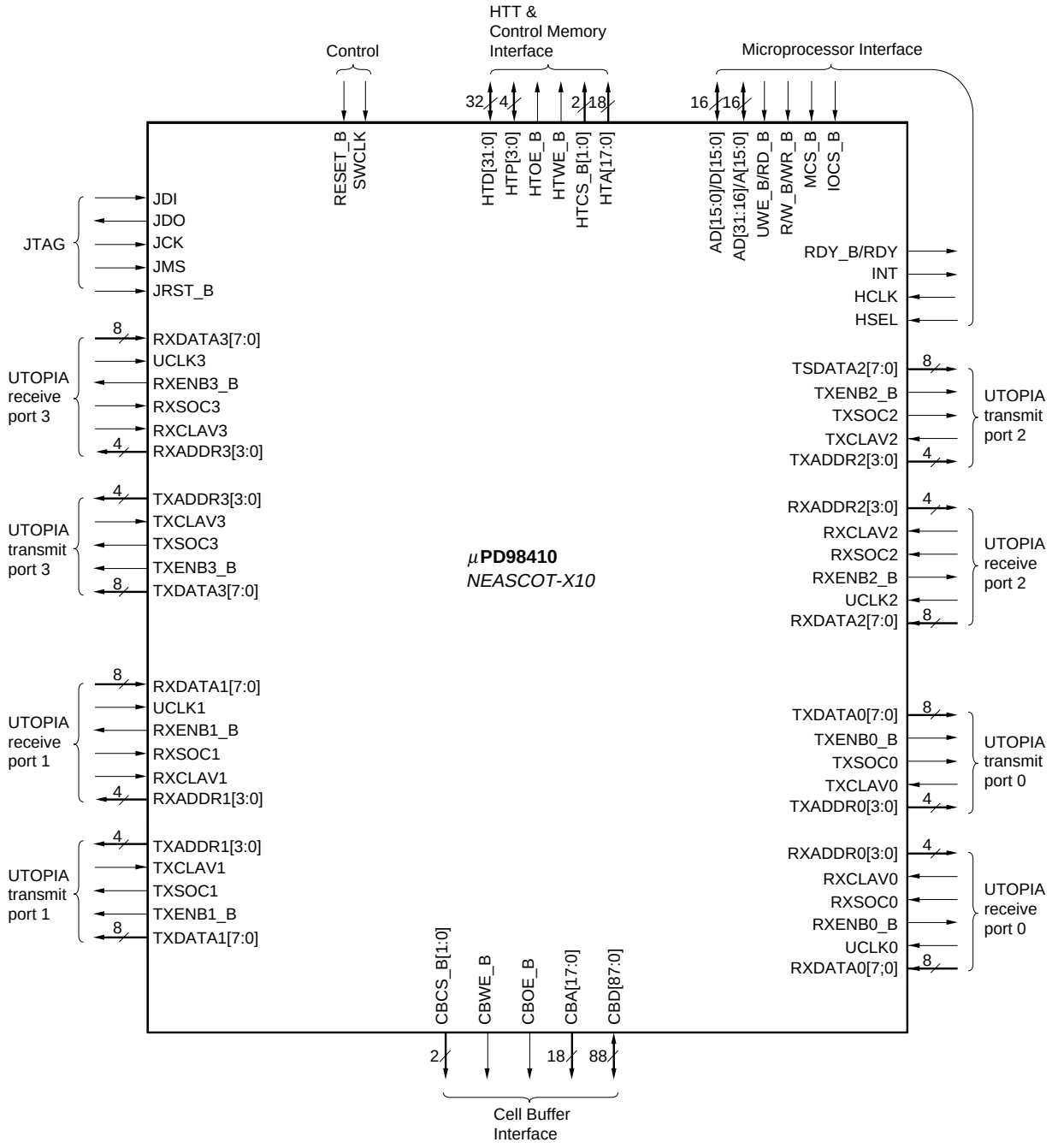
The μPD98410 realizes cell switching functions in the ATM layer by combining a microprocessor, cell buffer storage SRAM, and header translation table (HTT)/control information storage SRAM as shown below.



BLOCK DIAGRAM

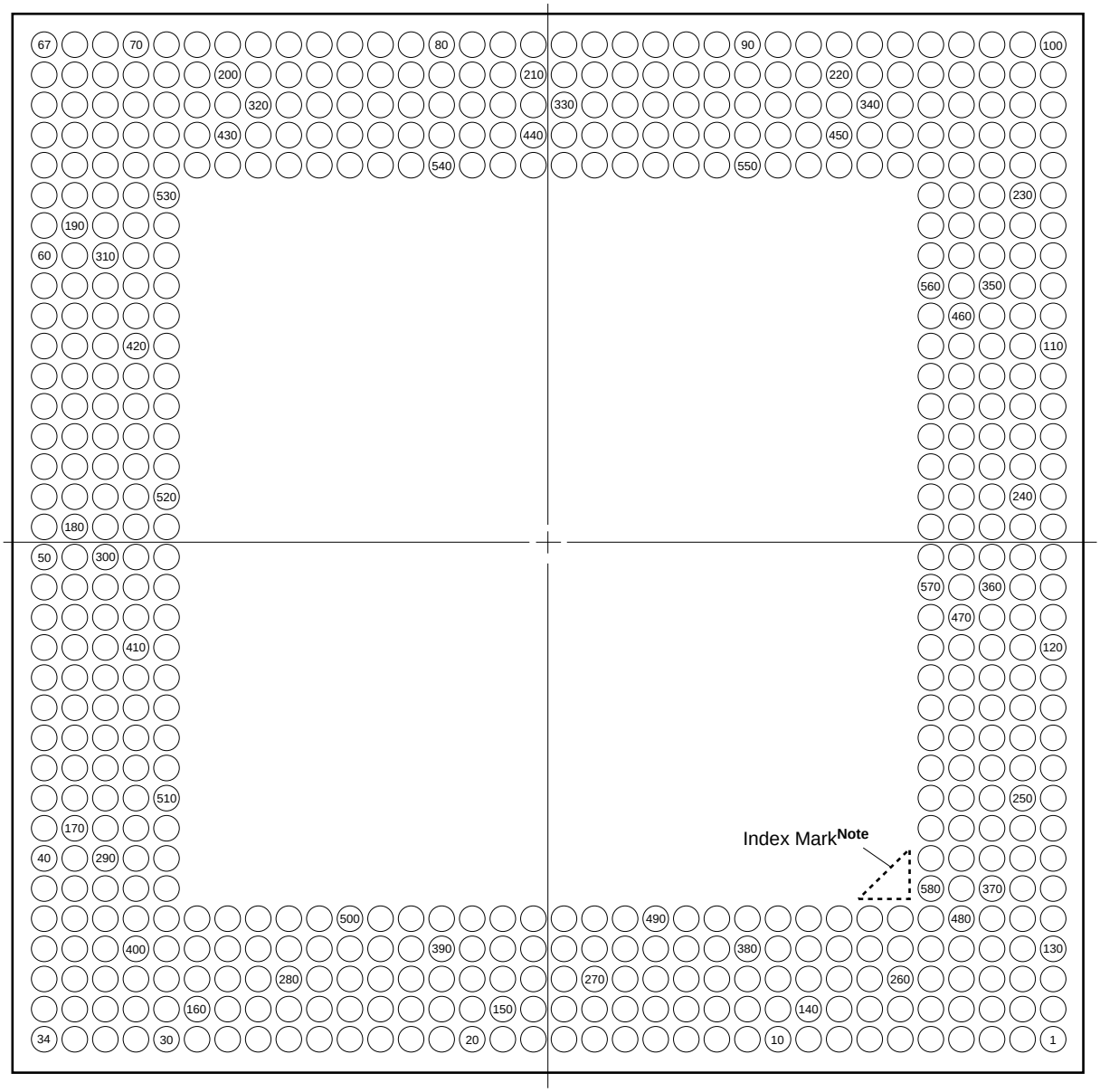


PIN CONFIGURATION



PIN CONFIGURATION (Bottom View)

580-pin BGA package



Note Index Mark is indicated in Top View.

PIN NAME

(1) Power

V_{DD}	:	Supply Voltage
GND	:	Ground

(2) UTOPIA

RXADDR3 to RXADDR0	:	Receive Address
RXDATA7 to RXDATA0	:	Receive Data Bus
RXSOC3 to RXSOC0	:	Receive Start of Cell
RXENB3_B to RXENB0_B	:	Receive Enable Data Transfers
RXCLAV3 to RXCLAV0	:	Receive Cell Buffer Available
UCLK3 to UCLK0	:	UTOPIA Clock
TXADDR3 to TXADDR0	:	Transmit Address
TXDATA7 to TXDATA0	:	Transmit Data Bus
TXSOC3 to TXSOC0	:	Transmit Start of Cell
TXENB3_B to TXENB0_B	:	Transmit Enable Data Transfers
TXCLAV3 to TXCLAV0	:	Transmit Cell Buffer Available

(3) Memory Interface

HTA17 to HTA0	:	HTT Memory Address
HTD31 to HTD0	:	HTT Memory Data Bus
HTP3 to HTP0	:	HTT Memory Data Bus Parity
HTCS1_B, HTCS0_B	:	HTT Memory Chip Select
HTWE_B	:	HTT Memory Write Enable
HTOE_B	:	HTT Memory Output Enable
CBA17 to CBA0	:	Cell Buffer Memory Address
CBD87 to CBD0	:	Cell Buffer Memory Data Bus
CBCS1_B, CBCS0_B	:	Cell Buffer Memory Chip Select
CBWE_B	:	Cell Buffer Memory Write Enable
CBOE_B	:	Cell Buffer Memory Output Enable

(4) CPU Interface

HSEL	:	Host Bus Mode Select
IOCS_B	:	I/O Chip Select
MCS_B	:	Memory Chip Select
RDY	:	I/O Ready, Memory Ready
INT	:	Interrupt Request
HCLK	:	Host Clock
AD31 to AD0	:	Address and Data
R/W_B	:	Read/Write
UWE_B	:	Upper Word Enable
A15 to A0	:	Address
D15 to D0	:	Data
WR_B	:	Write Strobe
RD_B	:	Read Strobe

(5) JTAG

JDI	:	JTAG Data Input
JDO	:	JTAG Data Output
JCK	:	JTAG Data Clock
JMS	:	JTAG Mode Select
JRST_B	:	JTAG Reset

(6) Other

SWCLK	:	System Clock
RESET_B	:	Hardware Reset
IC	:	Internal Connected
CG	:	Connect Ground
PU	:	Pull-up

PIN LAYOUT

(1/6)

Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O
1	GND		37	CBD72	I/O	73	RXDATA05	I
2	GND		38	CBD69	I/O	74	V_{DD}	
3	IC	O	39	CBD66	I/O	75	GND	
4	IC	O	40	CBD63	I/O	76	RXCLAV0	I
5	CG	I	41	IC	O	77	V_{DD}	
6	IC	O	42	CBD58	I/O	78	TXADDR01	O
7	JRST_B	I	43	CBD56	I/O	79	TXENB0_B	O
8	RXDATA36	I	44	CBD51	I/O	80	TXDATA04	O
9	RXDATA32	I	45	CBD49	I/O	81	TXDATA00	O
10	IC	O	46	CBD46	I/O	82	RXDATA26	I
11	RXSOC3	I	47	CBWE_B	O	83	V_{DD}	
12	RXADDR31	O	48	CBA17	O	84	RXDATA25	I
13	TXADDR31	O	49	GND		85	GND	
14	TXENB3_B	O	50	CBA13	O	86	GND	
15	V_{DD}		51	IC	O	87	RXCLAV2	I
16	TXDATA32	O	52	CBA9	O	88	RXADDR21	O
17	TXDATA30	O	53	CBA7	O	89	TXADDR21	O
18	TXDATA31	O	54	CBA4	O	90	TXCLAV2	I
19	RXDATA17	I	55	CBA0	O	91	GND	
20	RXDATA13	I	56	CBD41	I/O	92	TXDATA23	O
21	RXDATA10	I	57	CBD37	I/O	93	TXDATA20	O
22	RXENB1_B	O	58	CBD35	I/O	94	IOCS_B	I
23	V_{DD}		59	CBD30	I/O	95	RDY_B/RDY	O
24	RXADDR10	O	60	V_{DD}		96	CG	I
25	GND		61	CBD24	I/O	97	CG	I
26	V_{DD}		62	CBD20	I/O	98	IC	O
27	TXDATA15	O	63	CBD17	I/O	99	GND	
28	TXDATA11	O	64	CBD15	I/O	100	GND	
29	CBD86	I/O	65	GND		101	GND	
30	CBD84	I/O	66	GND		102	IC	O
31	CBD80	I/O	67	GND		103	V_{DD}	
32	V_{DD}		68	GND		104	AD18/A2	I/O
33	GND		69	CBD10	I/O	105	AD14/D14	I/O
34	GND		70	CBD7	I/O	106	AD10/D10	I/O
35	GND		71	CBD4	I/O	107	AD6/D6	I/O
36	CBD74	I/O	72	CBD2	I/O	108	AD3/D3	I/O

(2/6)

Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O
109	AD1/D1	I/O	146	TXDATA36	O	183	CBA2	O
110	HTA14	O	147	TXDATA33	O	184	CBD42	I/O
111	V_{DD}		148	TXDATA34	O	185	CBD38	I/O
112	HTA9	O	149	GND		186	V_{DD}	
113	V_{DD}		150	RXDATA15	I	187	CBD33	I/O
114	GND		151	RXDATA12	I	188	CBD28	I/O
115	HTCS1_B	O	152	V_{DD}		189	CBD26	I/O
116	GND		153	RXCLAV1	I	190	CBD23	I/O
117	HTCS0_B	O	154	RXADDR11	O	191	GND	
118	V_{DD}		155	TXADDR12	O	192	V_{DD}	
119	HTD29	I/O	156	TXCLAV1	I	193	CBD13	I/O
120	HTD26	I/O	157	TXDATA17	O	194	CBD12	I/O
121	HTD23	I/O	158	TXDATA13	O	195	GND	
122	HTD20	I/O	159	TXDATA10	O	196	CBD9	I/O
123	HTD16	I/O	160	V_{DD}		197	CBD8	I/O
124	HTD15	I/O	161	CBD82	I/O	198	IC	O
125	HTD10	I/O	162	CBD78	I/O	199	V_{DD}	
126	V_{DD}		163	CBD77	I/O	200	RXDATA06	I
127	HTD5	I/O	164	GND		201	RXDATA03	I
128	HTD2	I/O	165	CBD76	I/O	202	RXDATA01	I
129	SWCLK	I	166	CBD73	I/O	203	RXSOC0	I
130	V_{DD}		167	V_{DD}		204	RXADDR02	O
131	GND		168	CBD67	I/O	205	TXADDR03	O
132	GND		169	IC	O	206	TXCLAV0	I
133	GND		170	CBD62	I/O	207	TXDATA06	O
134	CG	I	171	CBD59	I/O	208	TXDATA02	O
135	CG	I	172	CBD57	I/O	209	V_{DD}	
136	IC	O	173	CBD53	I/O	210	RXDATA27	I
137	V_{DD}		174	V_{DD}		211	RXDATA23	I
138	GND		175	GND		212	RXDATA21	I
139	V_{DD}		176	CBCS1_B	O	213	RXENB2_B	O
140	RXDATA34	I	177	V_{DD}		214	RXADDR23	O
141	RXDATA30	I	178	CBA15	O	215	TXADDR23	O
142	V_{DD}		179	CBOE_B	O	216	TXADDR20	O
143	RXADDR33	O	180	CBA11	O	217	TXENB2_B	O
144	TXADDR33	O	181	V_{DD}		218	TXDATA25	O
145	TXCLAV3	I	182	CBA6	O	219	TXDATA22	O

(3/6)

Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O
220	HCLK	I	256	IC	I/O	293	V_{DD}	
221	MCS_B	I	257	IC	I/O	294	CBD54	I/O
222	R/W_B /WR_B	I	258	GND		295	CBD52	I/O
			259	GND		296	CBD48	I/O
223	AD31/A15	I/O	260	JDI	I	297	CBD47	I/O
224	AD28/A12	I/O	261	JCK	I	298	CBD45	I/O
225	AD27/A11	I/O	262	RXDATA37	I	299	CBCS0_B	O
226	GND		263	RXDATA33	I	300	CBA16	O
227	AD25/A9	I/O	264	RXDATA31	I	301	CBA12	O
228	AD22/A6	I/O	265	RXENB3_B	O	302	CBA10	O
229	AD20/A4	I/O	266	RXADDR32	O	303	CBA05	O
230	AD16/A0	I/O	267	RXADDR30	O	304	GND	
231	AD12/D12	I/O	268	TXADDR32	O	305	CBA01	O
232	AD8/D8	I/O	269	TXSOC3	O	306	GND	
233	V_{DD}		270	TXDATA37	O	307	CBD39	I/O
234	AD2/D2	I/O	271	V_{DD}		308	CBD34	I/O
235	GND		272	RXDATA14	I	309	GND	
236	HTA12	O	273	GND		310	CBD29	I/O
237	GND		274	RXDATA11	I	311	CBD25	I/O
238	HTA6	O	275	IC	O	312	CBD21	I/O
239	HTA4	O	276	RXSOC1	I	313	CBD18	I/O
240	HTA1	O	277	RXADDR13	O	314	CBD14	I/O
241	HTA3	O	278	TXADDR13	O	315	CBD11	I/O
242	HTOE_B	O	279	TXADDR10	O	316	GND	
243	HTD31	I/O	280	TXENB1_B	O	317	CBD5	I/O
244	HTD28	I/O	381	TXDATA14	O	318	CBD1	I/O
245	HTD24	I/O	282	TXDATA12	O	319	RXDATA07	I
246	GND		283	CBD85	I/O	320	RXDATA04	I
247	HTD17	I/O	284	GND		321	RXDATA00	I
248	V_{DD}		285	CBD79	I/O	322	RXENB0_B	O
249	HTD13	I/O	286	GND		323	RXADDR01	O
250	HTD8	I/O	287	V_{DD}		324	TXADDR02	O
251	HTD7	I/O	288	CBD70	I/O	325	TXADDR00	O
252	HTD4	I/O	289	CBD68	I/O	326	TXSOC0	O
253	HTD0	I/O	290	CBD65	I/O	327	TXDATA05	O
254	RESET_B	I	291	GND		328	TXDATA03	O
255	IC	I/O	292	GND		329	RXDATA24	I

(4/6)

Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O
330	RXDATA20	I	368	HTD9	I/O	406	CBD60	I/O
331	UCLK2	I	369	HTD6	I/O	407	CBD55	I/O
332	RXSOC2	I	370	GND		408	GND	
333	RXADDR22	O	371	V_{DD}		409	CBD50	I/O
334	GND		372	IC	I/O	410	V_{DD}	
335	TXADDR22	O	373	IC	O	411	CBD44	I/O
336	TXSOC2	O	374	V_{DD}		412	V_{DD}	
337	TXDATA26	O	375	CG	I	413	CBA14	O
338	V_{DD}		376	JDO	O	414	V_{DD}	
339	V_{DD}		377	JMS	I	415	CBA8	O
340	HSEL	I	378	RXDATA35	I	416	V_{DD}	
341	V_{DD}		379	GND		417	CBA3	O
342	AD30/A14	I/O	380	UCLK3	I	418	CBD43	I/O
343	AD29/A13	I/O	381	RXCLAV3	I	419	CBD40	I/O
344	AD26/A10	I/O	382	GND		420	CBD36	I/O
345	AD23/A7	I/O	383	TXADDR30	O	421	CBD32	I/O
346	AD19/A3	I/O	384	V_{DD}		422	CBD31	I/O
347	GND		385	TXDATA35	O	423	CBD27	I/O
348	AD13/D13	I/O	386	V_{DD}		424	CBD22	I/O
349	AD9/D9	I/O	387	RXDATA16	I	425	CBD19	I/O
350	AD7/D7	I/O	388	V_{DD}		426	CBD16	I/O
351	AD4/D4	I/O	389	UCLK1	I	427	IC	O
352	HTA17	O	390	V_{DD}		428	CBD6	I/O
353	HTA15	O	391	GND		429	CBD3	I/O
354	HTA11	O	392	RXADDR12	O	430	CBD0	I/O
355	HTA10	O	393	TXADDR11	O	431	GND	
356	HTA8	O	394	TXSOC1	O	432	RXDATA02	I
357	HTA5	O	395	TXDATA16	O	433	UCLK0	I
358	HTA2	O	396	GND		434	RXADDR03	O
359	HTWE_B	O	397	CBD87	I/O	435	RXADDR00	O
360	HTP3	I/O	398	CBD83	I/O	436	GND	
361	HTD27	I/O	399	CBD81	I/O	437	TXDATA07	O
362	GND		400	CBD75	I/O	438	V_{DD}	
363	HTP2	I/O	401	CBD71	I/O	439	TXDATA01	O
364	HTD21	I/O	402	GND		440	V_{DD}	
365	HTD18	I/O	403	IC	O	441	RXDATA22	I
366	HTD14	I/O	404	CBD64	I/O	442	V_{DD}	
367	HTD11	I/O	405	CBD61	I/O	443	V_{DD}	

(5/6)

Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O
444	V_{DD}		481	V_{DD}		518	GND	
445	RXADDR20	O	482	GND		519	V_{DD}	
446	V_{DD}		483	V_{DD}		520	GND	
447	TXDATA27	O	484	GND		521	V_{DD}	
448	TXDATA24	O	485	V_{DD}		522	GND	
449	TXDATA21	O	486	GND		523	V_{DD}	
450	GND		487	V_{DD}		524	GND	
451	INT	O	488	GND		525	V_{DD}	
452	UWE_B/RD_B	I	489	V_{DD}		526	GND	
453	GND		490	GND		527	V_{DD}	
454	AD24/A8	I/O	491	V_{DD}		528	GND	
455	AD21/A5	I/O	492	GND		529	V_{DD}	
456	AD17/A1	I/O	493	V_{DD}		530	GND	
457	AD15/D15	I/O	494	GND		531	V_{DD}	
458	AD11/D11	I/O	495	V_{DD}		532	GND	
459	GND		496	GND		533	V_{DD}	
460	AD5/D5	I/O	497	V_{DD}		534	GND	
461	AD0/D0	I/O	498	GND		535	V_{DD}	
462	HTA16	O	499	V_{DD}		536	GND	
463	HTA13	O	500	GND		537	V_{DD}	
464	V_{DD}		501	V_{DD}		538	GND	
465	HTA7	O	502	GND		539	V_{DD}	
466	V_{DD}		503	V_{DD}		540	GND	
467	HTA0	O	504	GND		541	V_{DD}	
468	V_{DD}		505	V_{DD}		542	GND	
469	HTD30	I/O	506	GND		543	V_{DD}	
470	V_{DD}		507	V_{DD}		544	GND	
471	HTD25	I/O	508	GND		545	V_{DD}	
472	HTD22	I/O	509	V_{DD}		546	GND	
473	HTD19	I/O	510	GND		547	V_{DD}	
474	HTP1	I/O	511	V_{DD}		548	GND	
475	HTD12	I/O	512	GND		549	V_{DD}	
476	GND		513	V_{DD}		550	GND	
477	HTP0	I/O	514	GND		551	V_{DD}	
478	HTD3	I/O	515	V_{DD}		552	GND	
479	HTD1	I/O	516	GND		553	V_{DD}	
480	PU	I	517	V_{DD}		554	GND	

(6/6)

Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O	Pin No.	Pin Name	I/O
555	V_{DD}	I	564	GND		573	V_{DD}	
556	GND		565	V_{DD}		574	GND	
557	V_{DD}		566	GND		575	V_{DD}	
558	GND		567	V_{DD}		576	GND	
559	V_{DD}		568	GND		577	V_{DD}	
560	GND		569	V_{DD}		578	GND	
561	V_{DD}		570	GND		579	V_{DD}	
562	GND		571	V_{DD}		580	GND	
563	V_{DD}		572	GND				

TABLE OF CONTENTS

1. PIN FUNCTION 14
1.1 Power Supply 14
1.2 UTOPIA Interface 15
1.3 Transmit Interface Signal 17
1.4 Memory Interface Signal 19
1.5 Microprocessor Interface Signal 21
1.6 JTAG Interface Signal 22
1.7 Other Interface Signals 22
1.8 Recommended Connections of Unused Pins 23
1.9 Pin Status at Reset 24

2. ELECTRICAL SPECIFICATIONS (PRELIMINARY) 25

3. PACKAGE DRAWINGS 40

4. RECOMMENDED SOLDERING CONDITIONS 41

1. PIN FUNCTION

Although the μPD98410 is a 3.3-V device, it can be directly connected to a PHY device, CPU, or memory having a 5-V TTL interface.

1.1 Power Supply

Pin Name	Pin No.	I/O	Function
V_{DD}	15, 23, 26, 32, 60, 74, 77, 83, 103, 111, 113, 118, 126, 130, 137, 139, 142, 152, 160, 167, 174, 177, 181, 186, 192, 199, 209, 233, 248, 271, 287, 293, 338, 339, 341, 371, 374, 384, 386, 388, 390, 410, 412, 414, 416, 438, 440, 442, 443, 444, 446, 464, 466, 468, 470, 481, 483, 485, 487, 489, 491, 493, 495, 497, 499, 501, 503, 505, 507, 509, 511, 513, 515, 517, 519, 521, 523, 525, 527, 529, 531, 533, 535, 537, 539, 541, 543, 545, 547, 549, 551, 553 555, 557, 559, 561, 563, 565, 567, 569, 571, 573, 575, 577, 579	–	These pins supply a voltage of +3.3±5%.
GND	1, 2, 25, 33, 34, 35, 49, 65 66, 67, 68, 75, 85, 86, 91, 99, 100, 101, 114, 116, 131, 132, 133, 138, 149, 164, 175, 191, 195, 226, 235, 237, 246, 258, 259, 273, 284, 286, 291, 292, 304, 306, 309, 316, 334, 347, 362, 370, 379, 382, 391, 396, 402, 408, 431, 436, 450, 453, 459, 476, 482, 484, 486, 488, 490, 492, 494, 496, 498, 500, 502, 504, 506, 508, 510, 512, 514, 516, 518, 520, 522, 524, 526, 528, 530, 532, 534, 536, 538, 540, 542, 544, 546, 548, 550, 552, 554, 556, 558, 560, 562, 564, 566, 568, 570, 572, 574, 576, 578, 580	–	These are ground pins.

1.2 UTOPIA Interface

The μPD98410 employs UTOPIA level2 (cell level transfer) as an interface between the PHY layer and ATM layer.

(1/2)

Pin Name	Pin No.	I/O	Function
RXADDR03 to RXADDR00	434, 204, 323, 435	O	Multi-PHY select address of receive interface 0. RXADDR03 is the MSB.
RXDATA07 to RXDATA00	319, 200, 73, 320, 201, 432, 202, 321	I	Cell data input of receive interface 0. Data is input from a PHY layer device in byte units. The μPD98410 reads the data in synchronization with the rising edge of UCLK0. RXDATA07 is the MSB.
RXSOC0	203	I	Cell transfer start signal of receive interface 0. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB0_B	322	O	Transfer enable signal of receive interface 0. Indicates to a PHY layer device that the μPD98410 is ready to receive data in the next clock cycle.
RXCLAV0	76	I	Cell transfer valid signal of receive interface 0. Inputs a signal indicating that there are no more cells to be supplied to the μPD98410 after transfer of the current cell has been completed.
UCLK0	433	I	UTOPIA clock input of receive interface 0. Data is transmitted or received in synchronization with the rising edge of this clock.
RXADDR13 to RXADDR10	277, 392, 154, 24	O	Multi-PHY select address of receive interface 1. RXADDR13 is the MSB.
RXDATA17 to RXDATA10	19, 387 150, 272, 20, 151, 274, 21	I	Cell data input of receive interface 1. Data is input from a PHY layer device in byte units. The μPD98410 reads the data in synchronization with the rising edge of UCLK1. RXDATA17 is the MSB.
RXSOC1	276	I	Cell transfer start signal of receive interface 1. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB1_B	22	O	Transfer enable signal of receive interface 1. Indicates to a PHY layer device that the μPD98410 is ready to receive data in the next clock cycle.
RXCLAV1	153	I	Cell transfer valid signal of receive interface 1. Inputs a signal indicating that there are no more cells to be supplied to the μPD98410 after transfer of the current cell has been completed.
UCLK1	389	I	UTOPIA clock input of receive interface 1. Data is transmitted or received in synchronization with the rising edge of this clock.

(2/2)

Pin Name	Pin No.	I/O	Function
RXADDR23 to RXADDR20	214, 333, 88, 445	O	Multi-PHY select address of receive interface 2. RXADDR23 is the MSB.
RXDATA27 to RXDATA20	210, 82, 84, 329, 211, 441, 212, 330	I	Cell data input of receive interface 2. Data is input from a PHY layer device in byte units. The μPD98410 reads the data in synchronization with the rising edge of UCLK2. RXDATA27 is the MSB.
RXSOC2	332	I	Cell transfer start signal of receive interface 2. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB2_B	213	O	Transfer enable signal of receive interface 2. Indicates to a PHY layer device that the μPD98410 is ready to receive data in the next clock cycle.
RXCLAV2	87	I	Cell transfer valid signal of receive interface 2. Inputs a signal indicating that there are no more cells to be supplied to the μPD98410 after transfer of the current cell has been completed.
UCLK2	331	I	UTOPIA clock input of receive interface 2. Data is transmitted or received in synchronization with the rising edge of this clock.
RXADDR33 to RXADDR30	143, 266, 12, 267	O	Multi-PHY select address of receive interface 3. RXADDR33 is the MSB.
RXDATA37 to RXDATA30	262, 8, 378, 140, 263 9, 264, 141	I	Cell data input of receive interface 3. Data is input from a PHY layer device in byte units. The μPD98410 reads the data in synchronization with the rising edge of UCLK3. RXDATA37 is the MSB.
RXSOC3	11	I	Cell transfer start signal of receive interface 3. This signal is input from a PHY layer device in synchronization with the first byte of cell data.
RXENB3_B	265	O	Transfer enable signal of receive interface 3. Indicates to a PHY layer device that the μPD98410 is ready to receive data in the next clock cycle.
RXCLAV3	381	I	Cell transfer valid signal of receive interface 3. Inputs a signal indicating that there are no more cells to be supplied to the μPD98410 after transfer of the current cell has been completed.
UCLK3	380	I	UTOPIA clock input of receive interface 3. Data is transmitted or received in synchronization with the rising edge of this clock.

1.3 Transmit Interface Signal

(1/2)

Pin Name	Pin No.	I/O	Function
TXADDR03 to TXADDR00	205, 324, 78, 325	O	Multi-PHY select address of transmit interface 0. TXADDR03 is the MSB.
TXDATA07 to TXDATA00	437, 207, 327, 80, 328, 208, 439, 81	O	Cell data output of transmit interface 0. Data is output to a PHY layer device in byte units. The μPD98410 outputs the data in synchronization with the rising edge of UCLK0. TXDATA07 is the MSB. (3-state buffer)
TXSOC0	326	O	Cell transfer start signal of transmit interface 0. This signal is output to a PHY layer device in synchronization with the first byte of transmit cell data. (3-state buffer)
TXENB0_B	79	O	Transfer enable signal of transmit interface 0. Indicates to a PHY layer device that data is output in the current clock cycle.
TXCLAV0	206	I	Cell transfer valid signal of transmit interface 0. Inputs a signal indicating that all of the next single cell of data can be received after transfer of the current cell has been completed.
TXADDR13 to TXADDR10	278, 155, 393, 279	O	Multi-PHY select address of transmit interface 1. TXADDR13 is the MSB.
TXDATA17 to TXDATA10	157, 395, 27, 281,158, 282, 28, 159	O	Cell data output of transmit interface 1. The μPD98410 outputs the data in synchronization with the rising edge of UCLK1. TXDATA17 is the MSB. (3-state buffer)
TXSOC1	394	O	Cell transfer start signal of transmit interface 1. This signal is output to a PHY layer device in synchronization with the first byte of transmit cell data. (3-state buffer)
TXENB1_B	280	O	Transfer enable signal of transmit interface 1. Indicates to a PHY layer device that data is output in the current clock cycle.
TXCLAV1	156	I	Cell transfer valid signal of transmit interface 1. Inputs a signal indicating that all of the next single cell of data can be received after transfer of the current cell has been completed.

(2/2)

Pin Name	Pin No.	I/O	Function
TXADDR23 to TXADDR20	215, 335, 89, 216	O	Multi-PHY select address of transmit interface 2. TXADDR23 is the MSB.
TXDATA27 to TXDATA20	447, 337, 218, 448, 92, 219, 449, 93	O	Cell data output of transmit interface 2. The μPD98410 outputs the data in synchronization with the rising edge of UCLK2. TXDATA27 is the MSB. (3-state buffer)
TXSOC2	336	O	Cell transfer start signal of transmit interface 2. This signal is output to a PHY layer device in synchronization with the first byte of transmit cell data. (3-state buffer)
TXENB2_B	217	O	Transfer enable signal of transmit interface 2. Indicates to a PHY layer device that data is output in the current clock cycle.
TXCLAV2	90	I	Cell transfer valid signal of transmit interface 2. Inputs a signal indicating that all of the next single cell of data can be received after transfer of the current cell has been completed.
TXADDR33 to TXADDR30	144, 268, 13, 383	O	Multi-PHY select address of transmit interface 3. TXADDR33 is the MSB.
TXDATA37 to TXDATA30	270, 146, 385, 148, 147, 16, 18, 17	O	Cell data output of transmit interface 3. The μPD98410 outputs the data in synchronization with the rising edge of UCLK3. TXDATA37 is the MSB. (3-state buffer)
TXSOC3	269	O	Cell transfer start signal of transmit interface 3. This signal is output to a PHY layer device in synchronization with the first byte of transmit cell data. (3-state buffer)
TXENB3_B	14	O	Transfer enable signal of transmit interface 3. Indicates to a PHY layer device that data is output in the current clock cycle.
TXCLAV3	145	I	Cell transfer valid signal of transmit interface 3. Inputs a signal indicating that all of the next single cell of data can be received after transfer of the current cell has been completed.

1.4 Memory Interface Signal

The μPD98410 has two types of memory interfaces. One is an HTT & control memory to store the header translation table of a cell and the address pointer to the cell buffer, and the other is a cell buffer memory that stores cell data.

(1) HTT & control memory interface signal

Pin Name	Pin No.	I/O	Function
HTA17 to HTA0	352, 462, 353, 110, 463, 236, 354, 355, 112, 356, 465, 238, 357, 239, 241, 358, 240, 467	O	Address output
HTD31 to HTD0	243, 469, 119, 244, 361, 120, 471, 245, 121, 472, 364, 122, 473, 365, 247, 123, 124, 366, 249, 475, 367, 125, 368, 250, 251, 369, 127, 252, 478, 128, 479, 253	I/O	Data I/O bus (32-bit/word units) (with pull-down resistor)
HTP3 to HTP0	360, 363, 474, 477	I/O	Parity I/O (with pull-down resistor)
HTCS1_B, HTCS0_B	115, 117	O	Chip select signal
HTWE_B	359	O	Write enable signal
HTOE_B	242	O	Output enable signal

(2) Cell buffer memory interface signal

Pin Name	Pin No.	I/O	Function
CBA17 to CBA0	48, 300, 178, 413, 50, 301, 180, 302, 52, 415, 53, 182, 303, 54, 417, 183, 305, 55	O	Address output
CBD87 to CBD0	397, 29, 283, 30, 398, 161, 399, 31, 285, 162, 163, 165, 400, 36, 166, 37, 401, 288, 38, 289, 168, 39, 290, 404, 40, 170, 405, 406, 171, 42, 172, 43, 407, 294, 173, 295, 44, 409, 45, 296, 297, 46, 298, 411, 418, 184, 56, 419, 307, 185, 57, 420, 58, 308, 187, 421, 422, 59, 310, 188, 423, 189, 311, 61, 190, 424, 312, 62 425, 313, 63, 426, 64 314, 193, 194, 315, 69, 196, 197, 70, 428, 317, 71, 429, 72, 318, 430	I/O	Data bus (88-bit/word units) (with pull-down resistor)
CBCS1_B, CBCS0_B	176 299	O	Chip select signal
CBWE_B	47	O	Write enable signal
CBOE_B	179	O	Output enable signal

1.5 Microprocessor Interface Signal

The μPD98410 supports the following two types of microprocessor interface:

- 32-bit address/data multiplexed synchronous bus
- 16-bit address/data separated asynchronous bus

The functions of some pins differ depending on the mode used.

(1) Microprocessor interface

Pin Name	Pin No.	I/O	Function
HSEL	340	I	Microprocessor interface select signal. When HSEL is low, the 32-bit multiplexed synchronous bus is selected; when it is high, the 16-bit separated asynchronous bus is selected.
IOCS_B	94	I	I/O chip select signal
MCS_B	221	I	Memory chip select signal
INT	451	O	Interrupt request signal

(2) 32-bit multiplexed synchronous interface

Pin Name	Pin No.	I/O	Function
HCLK	220	I	Microprocessor bus clock (8 to 33 MHz)
AD31 to AD0	223, 342, 343, 224, 225, 344, 227, 454, 345, 228, 455, 229, 346, 104, 456, 230, 457, 105, 348, 231, 458, 106, 349, 232, 350, 107, 460, 351, 108, 234, 109, 461	I/O	Address/data bus
R/W_B	222	I	Read/write select signal
UWE_B	452	I	High-order word enable signal
RDY_B	95	O	Ready signal (3-state buffer)

(3) 16-bit separated asynchronous interface

Pin Name	Pin No.	I/O	Function
HCLK	220	I	Connect this pin to GND, or pull it up to V_{DD}.
A15 to A0	223, 342, 343, 224, 225, 344, 227, 454, 345, 228, 455, 229, 346, 104, 456, 230	I	Address input
D15 to D0	457, 105, 348, 231, 458, 106, 349, 232, 350, 107, 460, 351, 108, 234, 109, 461	I/O	Data bus
WR_B	222	I	Write strobe signal
RD_B	452	I	Read strobe signal
RDY	95	O	Ready signal (3-state buffer)

1.6 JTAG Interface Signal

Pin Name	Pin No.	I/O	Function
JDI	260	I	JTAG serial data input
JDO	376	O	JTAG serial data output (normally open) (3-state buffer)
JCK	261	I	JTAG serial clock input
JMS	377	I	JTAG mode select signal
JRST_B	7	I	JTAG reset signal

1.7 Other Interface Signals

Pin Name	Pin No.	I/O	Function
SWCLK	129	I	System clock input (8 to 33 MHz)
RESET_B	254	I	Hardware reset signal (Schmitt input buffer)
CG	5, 96, 97,134, 135, 375	I	Normally connected to GND.
PU	480	I	Normally pulled up to V_{DD}.
IC	3, 4, 6, 10, 41, 98, 102, 136, 169, 198, 255, 256, 257, 275, 372, 373, 403, 427	O	Internally connected (normally open)

1.8 Recommended Connections of Unused Pins

Pin Name	I/O	Recommended Connections of Unused Pins
RXDATA07 to RXDATA00 RXDATA17 to RXDATA10 RXDATA27 to RXDATA20 RXDATA37 to RXDATA30	I	Connect to GND
RXSOC3 to RXSOC0	I	Connect to GND
RXCLAV3 to RXCLAV0	I	Connect to GND
UCLK3 to UCLK0	I	Connect to GND
TXCLAV3 to TXCLAV0	I	Connect to GND
HTD31 to HTD0	I/O (with pull-down resistor)	Open
HTP3 to HTP0	I/O (with pull-down resistor)	Open
CBD87 to CBD0	I/O (with pull-down resistor)	Open
HSEL	I	Connected to GND when 32-bit multiplexed synchronous bus is used. Pulled up to V_{DD} when 16-bit separated asynchro-nous bus is used.
HCLK	I	Pulled up to V_{DD} or connected to GND.
IOCS_B	I	Pulled up to V_{DD}
MCS_B	I	Pulled up to V_{DD}
AD31 to AD0	I/O	Pulled up to V_{DD}
A15 to A0	I	Connect to GND
D15 to D0	I/O	Pulled up to V_{DD}
R/W_B / WR_B	I	Pulled up to V_{DD}
UWE_B / RD_B	I	Pulled up to V_{DD}
JDI	I	Connect to GND
JCK	I	Connect to GND
JMS	I	Connect to GND
JRST_B	I	Connect to GND
All output pins	O	Open

1.9 Pin Status at Reset

Pin Name	I/O	Pin Status at Reset
RXADDR03 to RXADDR00 RXADDR13 to RXADDR10 RXADDR23 to RXADDR20 RXADDR33 to RXADDR30	O	High level
RXENB3_B to RXENB0_B	O	High level
TXADDR03 to TXADDR00 TXADDR13 to TXADDR10 TXADDR23 to TXADDR20 TXADDR33 to TXADDR30	O	High level
TXDATA07 to TXDATA00 TXDATA17 to TXDATA10 TXDATA27 to TXDATA20 TXDATA37 to TXDATA30	O (3-state buffer)	Hi-Z
TXSOC3 to TXSOC0	O (3-state buffer)	Hi-Z
TXENB3_B to TXENB0_B	O	High level
HTA17 to HTA0	O	Low level
HTCS1_B, HTCS0_B	O	High level
HTWE_B	O	High level
HTOE_B	O	High level
HTP3 to HTP0	I/O (with pull-down resistor)	Low level
HTD31 to HTD0	I/O (with pull-down resistor)	Low level
CBD87 to CBD0	I/O (with pull-down resistor)	Low level
CBA17 to CBA0	O	Low level
CBOE_B	O	High level
CBWE_B	O	High level
CBCS1_B, CBCS0_B	O	High level
INT	O	Low level
RDY	O (3-state buffer)	Hi-Z
AD31 to AD0	I/O	Hi-Z
D15 to D0	I/O	Hi-Z
JDO	O (3-state buffer)	Hi-Z

2. ELECTRICAL SPECIFICATIONS (PRELIMINARY)

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}		−0.5 to +4.6	V
Input voltage	V_I		−0.5 to +6.6	V
Output voltage	V_O		−0.5 to +6.6	V
Storage temperature	T_{stg}		−65 to +150	°C

Caution If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the product(s). Be sure to use the product(s) within the ratings.

Capacitance

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	Frequency = 1 MHz	–	10	20	pF
Output capacitance	C_O	Frequency = 1 MHz	–	10	20	pF
I/O capacitance	C_{IO}	Frequency = 1 MHz	–	10	20	pF

Recommended Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		3.135	3.300	3.465	V
Low-level input voltage	V_{IL}		0	–	0.8	V
High-level input voltage	V_{IH}		2.0	–	5.5	V
Operating temperature	T_A		0	–	+70	°C

DC Characteristics (T_A = 0 to +70 °C, V_{DD} = 3.3 V ± 5%)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output leakage current	I_{OZ}	$V_I = V_{DD}$ or GND	–	–	10	μA
Input leakage current	I_{LI1}	$V_I = V_{DD}$ or GND, **Note 1**	–	–	±10	μA
	I_{LI2}	$V_I = V_{DD}$ **Note 2** (50 kΩ pull-down)	25	120	220	μA
Low-level output current	I_{OL1}	V_{OL} = 0.4 V, **Note 3**	6.0	–	–	mA
	I_{OL2}	V_{OL} = 0.4 V, **Notes 4,5**	9.0	–	–	mA
	I_{OL3}	V_{OL} = 0.4 V, **Note 6**	12.0	–	–	mA
High-level output current	I_{OH1}	V_{OH} = 2.4 V, **Note 3**	−3.0	–	–	mA
	I_{OH2}	V_{OH} = 2.4 V, **Note 4**	−4.0	–	–	mA
	I_{OH3}	V_{OH} = 2.4 V, **Note 5** (UTOPIA)	−4.0	−8.0	–	mA
	I_{OH4}	V_{OH} = 2.4 V, **Note 6**	−5.0	–	–	mA
Low-level output voltage	V_{OL}	I_{OL} = 0 mA	–	–	0.1	V
High-level output voltage	V_{OH1}	I_{OH} = 0 mA, **Note 7**	V_{DD} – 0.2	–	–	V
High-level output voltage	V_{OH2}	I_{OH} = 0 mA, **Note 8**	V_{DD} – 0.4	–	–	V
Operating current	I_{DD}	$V_I = V_{DD}$ or GND	–	–	1000	mA

Notes 1. RXDATA03 through RXDATA00, RXDATA13 through RXDATA10, RXDATA23 through RXDATA20, RXDATA33 through RXDATA30, RXSOC3 through RXSOC0, RXCLAV3 through RXCLAV0, UCLK3 through UCLK0, TCLAV3 through TCLAV0, MCS_B, IOCS_B, R/W_B, UWE_B, HSEL, HCLK, JDI, JCK, JMS, JRST_B, SWCLK, and RESET_B pins

2. HTD31 through HTD0, HTP3 through HTP0, and CBD87 through CBD0 pins

3. INT and TDO pins

4. RXADDR03 through RXADDR00, RXADDR13 through RXADDR10, RXADDR23 through RXADDR20, RXADDR33 through RXADDR30, TXADDR03 through TXADDR00, TXADDR13 through TXADDR10, TXADDR23 through TXADDR20, TXADDR33 through TXADDR30, RENB3_B through RENB0_B, TENB3_B through TENB0_B, TXDATA07 through TXDAT00, TXDATA17 through TXDATA10, TXDATA27 through TXDATA20, TXDATA37 through TXDATA30, and TXSOC3 through TXSOC0 pins

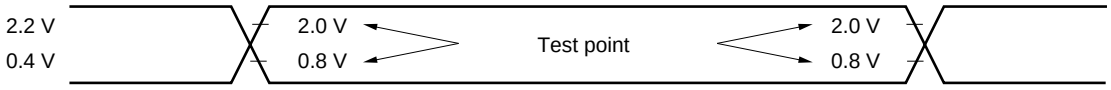
5. HTCS1_B, HTCS0_B, and CBCS1_B pins

6. HTA17 through HTA0, HTWE_B, HTOE_B, CBA17 through CBA0, CBCS0_B, CBWE_B, CBOE_B, RDY, and AD31 through AD0 pins

7. INT, JDO, RXADDR03 through RXADDR00, RXADDR13 through RXADDR10, RXADDR23 through RXADDR20, RXADDR33 through RXADDR30, TXADDR03 through TXADDR00, TXADDR13 through TXADDR10, TXADDR23 through TXADDR20, TXADDR33 through TXADDR30, RENB3_B through RENB0_B, TENB3_B through TENB0_B, TXDATA07 through TXDATA00, TXDATA17 through TXDATA10, TXDATA27 through TXDATA20, TXDATA37 through TXDATA30, TXSOC3 through TXSOC0, HTCS1_B, HTCS0_B, CBCS1_B, HTA17 through HTA0, HTWE_B, HTOE_B, CBA17 through CBA0, CBCS0_B, CBWE_B, CBOE_B, RDY, and AD31 through AD0 pins

8. HTD31 through HTD0, HTP3 through HTP0, and CBD87 through CBD0 pins

AC Test Output Waveform

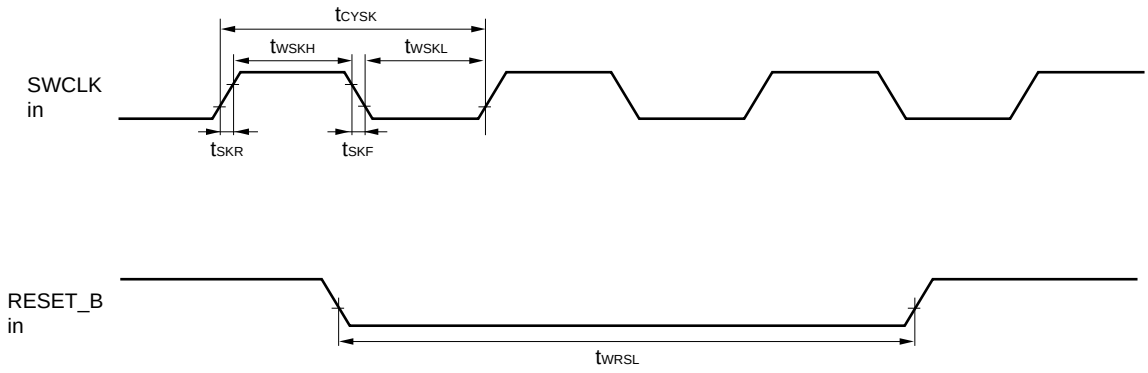


AC Characteristics (T_A = 0 to +70 °C, V_{DD} = 3.3 V ± 5%)

(1) Control signal

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SWCLK cycle time	t_{CYSK}		30		125	ns
SWCLK high-level width	t_{WSKH}		12		–	ns
SWCLK low-level width	t_{WSKL}		12		–	ns
SWCLK rise time	t_{SKR}		–		3	ns
SWCLK fall time	t_{SKF}		–		3	ns
RESET_B low-level width	t_{WRSL}		16		–	t_{CYSK}

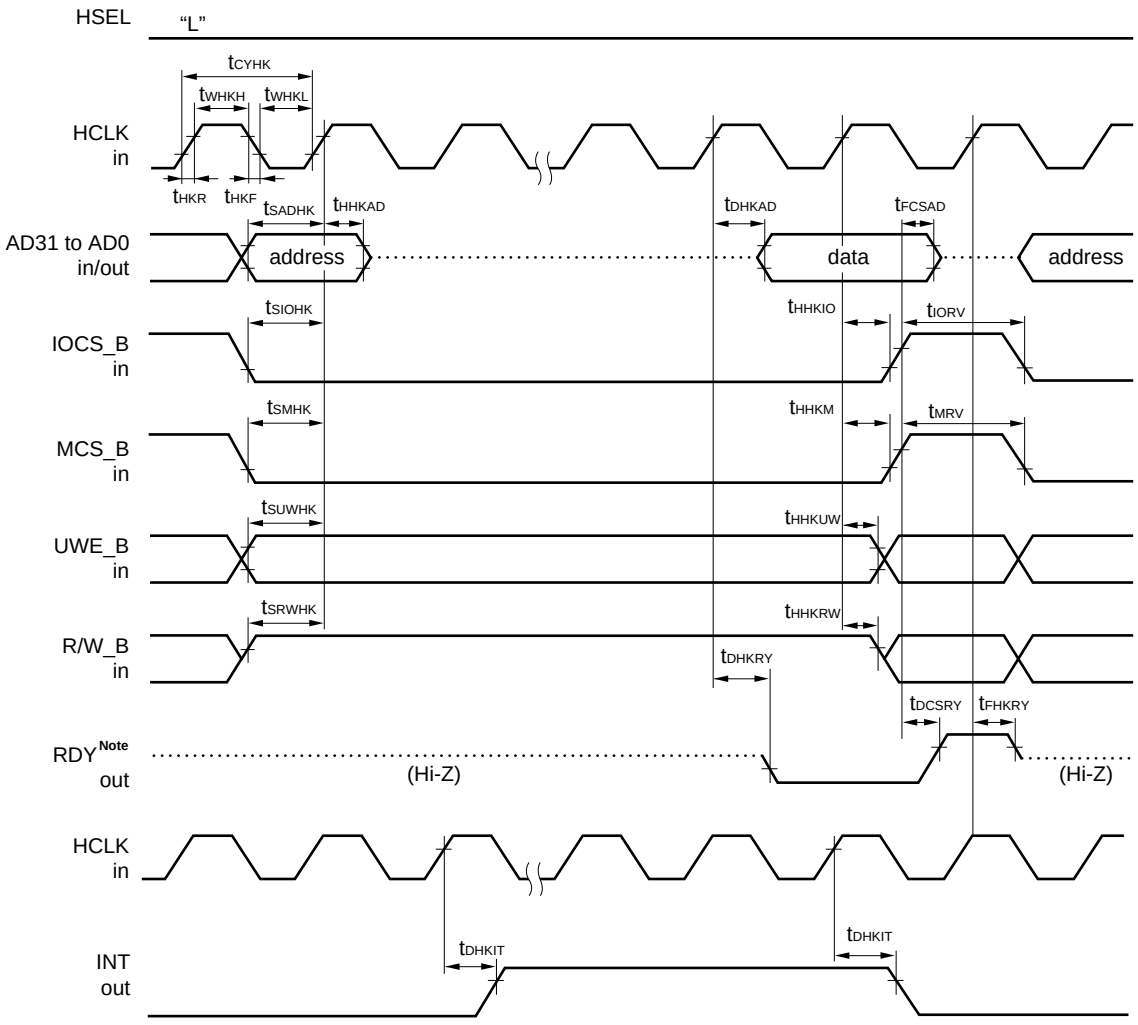
Control signal



(2) Processor interface (32-bit mode, read/write)

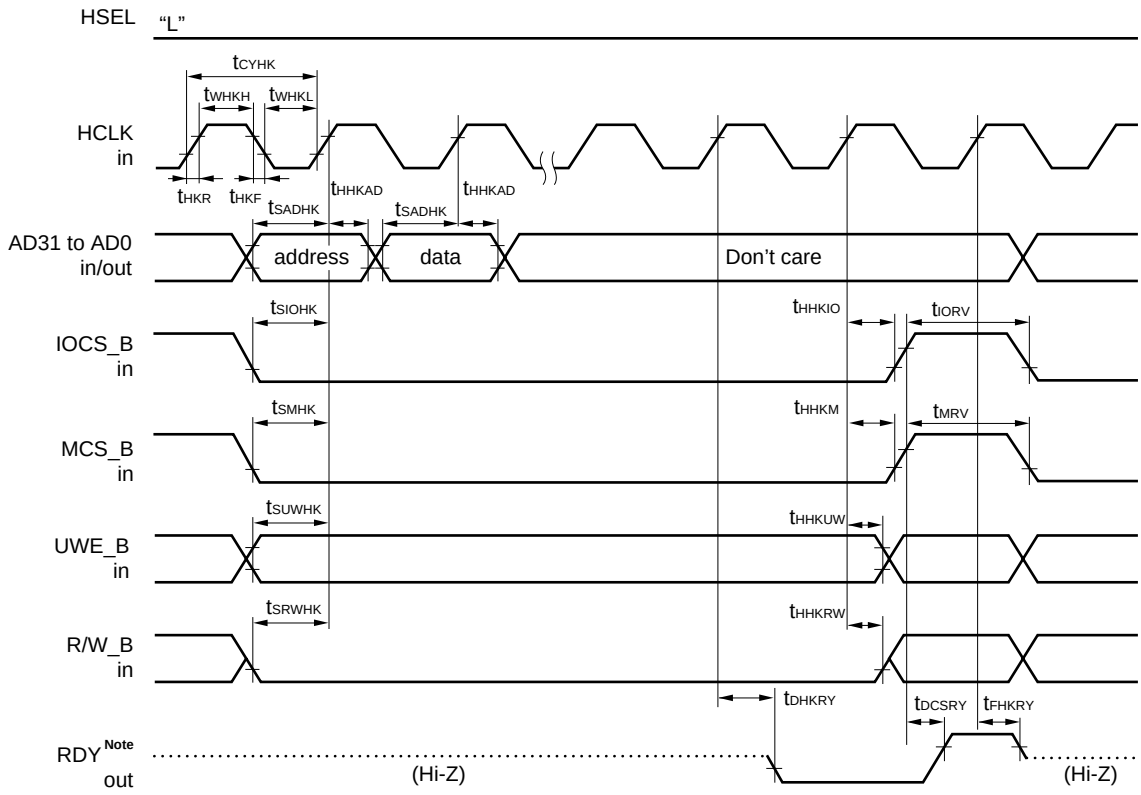
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
HCLK cycle time	t_{CYHK}		30		125	ns
HCLK high-level width	t_{WHKH}		12		–	ns
HCLK low-level width	t_{WHKL}		12		–	ns
HCLK rise time	t_{HKR}		–		3	ns
HCLK fall time	t_{HKF}		–		3	ns
HCLK↑→ INT output delay time	t_{DHKIT}	Load capacitance: 30 pF	1		17	ns
HCLK↑→ RDY low-level output delay time	t_{DHKRY}	Load capacitance: 70 pF	1		17	ns
IOCS_B↑ , MCS_B↑ → RDY high-level output delay time	t_{DCSRY}	Load capacitance: 70 pF	1		17	ns
HCLK↑→ RDY float output delay time	t_{FHKRY}	Load capacitance: 70 pF	1		17	ns
HCLK↑→ AD output delay time	t_{DHKAD}	Load capacitance: 70 pF	1		17	ns
IOCS_B↑, MCS_B↑→ AD float output delay time	t_{FCSAD}	Load capacitance: 70 pF	1		17	ns
AD setup time (vs. HCLK↑)	t_{SADHK}		8		–	ns
AD hold time (vs. HCLK ↑)	t_{HHKAD}		1		–	ns
IOCS_B setup time (vs. HCLK↑)	t_{SIOHK}		8		–	ns
IOCS_B hold time (vs. HCLK↑)	t_{HHKIO}		1		–	ns
IOCS_B recovery time	t_{IORV}		$2 \times t_{CYHK}$		–	ns
MCS_B setup time (vs. HCLK↑)	t_{SMHK}		8		–	ns
MCS_B hold time (vs. HCLK↑)	t_{HHKM}		1		–	ns
MCS_B recovery time	t_{MRV}		$2 \times t_{CYHK}$		–	ns
UWE_B setup time (vs. HCLK↑)	t_{SUWHK}		8		–	ns
UWE_B hold time (vs. HCLK↑)	t_{HHKUW}		1		–	ns
R/W_B setup time (vs. HCLK↑)	t_{SRWHK}		8		–	ns
R/W_B hold time (vs. HCLK↑)	t_{HHKRW}		1		–	ns

Processor Interface (32-bit mode, read)



Note (IOCS_B = "0" and MCS_B = "1") or (IOCS_B = "1" and MCS_B = "0")

Processor Interface (32-bit mode, write)



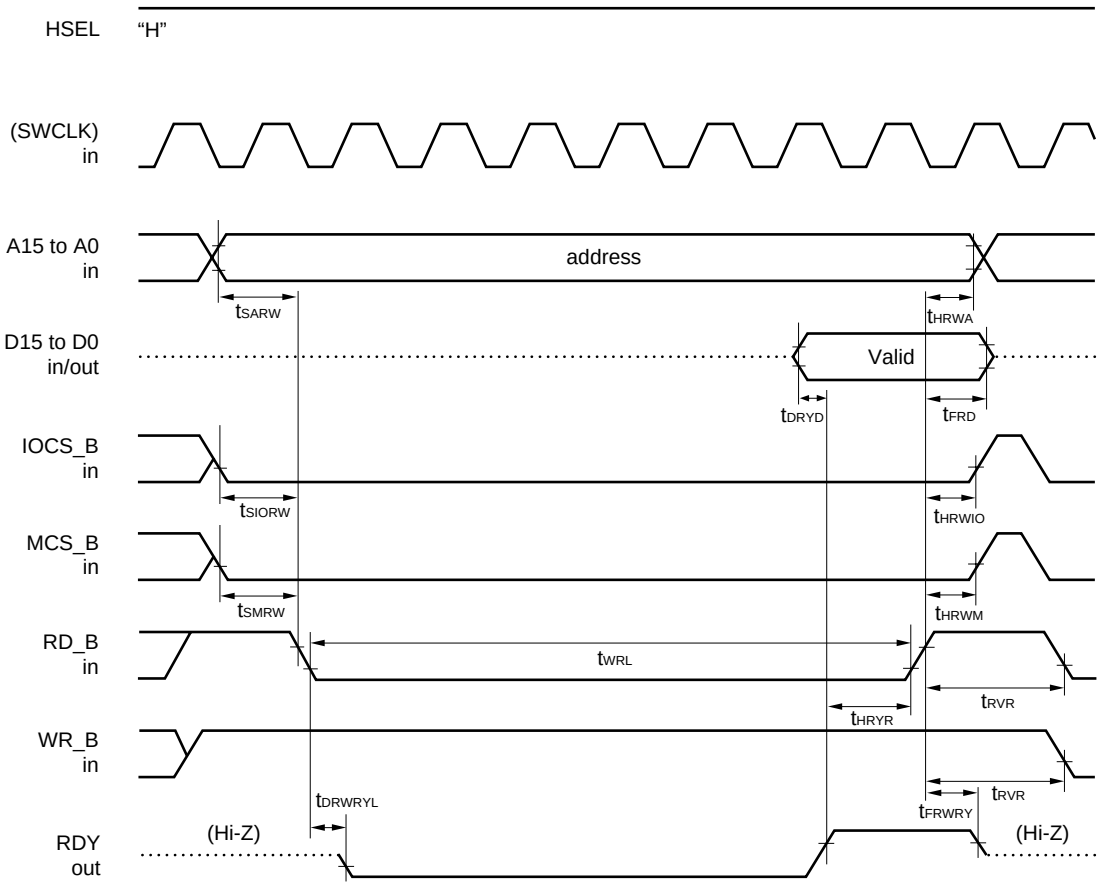
Note (IOCS_B = "0" and MCS_B = "1") or (IOCS_B = "1" and MCS_B = "0")

(3) Processor Interface (16-bit mode, read/write)

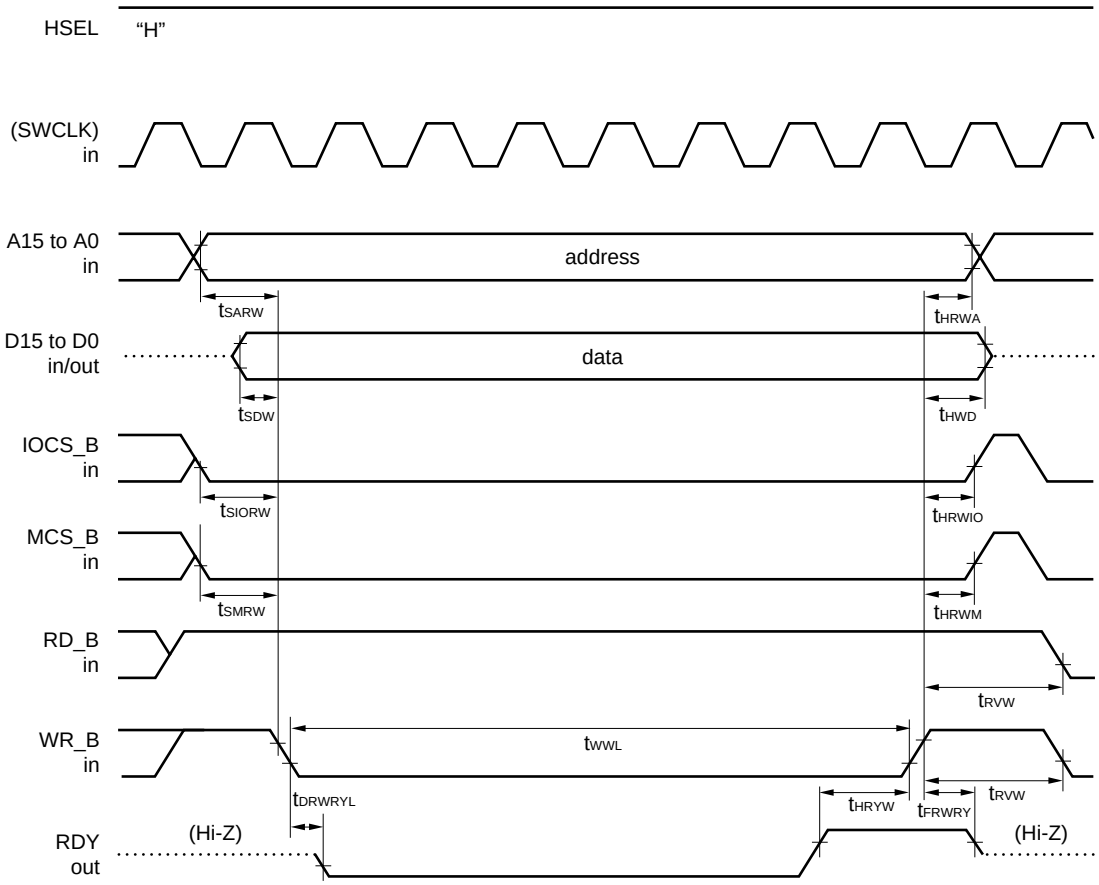
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
RD_B↓, WR_B↓→ RDY low-level output delay time	t_{DRWRYL}	Load capacitance: 70 pF	1		17	ns
RD_B↑, WR_B↑→ RDY float output delay time	t_{FRWRY}	Load capacitance: 70 pF	1		17	ns
Data output delay time (vs. RDY↑)	t_{DRYD}	Load capacitance: 70 pF	t_{WSKL} – 5			ns
RD_B↑→ data float output delay time	t_{FRD}	Load capacitance: 70 pF	1		17	ns
Data setup time (vs. WR_B↓)	t_{SDW}		8			ns
Data hold time (vs. WR_B↑)	t_{HWD}		1			ns
Address setup time (vs. RD_B↓, WR_B↓)	t_{SARW}		8			ns
Address hold time (vs. RD_B↑, WR_B↑)	t_{HRWA}		1			ns
IOCS_B setup time (vs. RD_B↓, WR_B↓)	t_{SIORW}		8			ns
IOCS_B hold time (vs. RD_B↑, WR_B↑)	t_{HRWIO}		1			ns
MCS_B setup time (vs. RD_B↓, WR_B↓)	t_{SMRW}		8			ns
MCS_B hold time (vs. RD_B↑, WR_B↑)	t_{HRWM}		1			ns
RD_B recovery time	t_{RVR}		2 × t_{CYSK}			ns
RD_B low-level width [Note]	t_{WRL}		50			ns
RD_B hold time (vs. RDY↑)	t_{HRYR}		1			ns
WR_B recovery time	t_{RVW}		2 × t_{CYSK}			ns
WR_B low-level width [Note]	t_{WWL}		50			ns
WR_B hold time (vs. RDY↑)	t_{HRYW}		1			ns

Note The low level is retained until RDY goes high.

Processor Interface (16-bit mode, read)



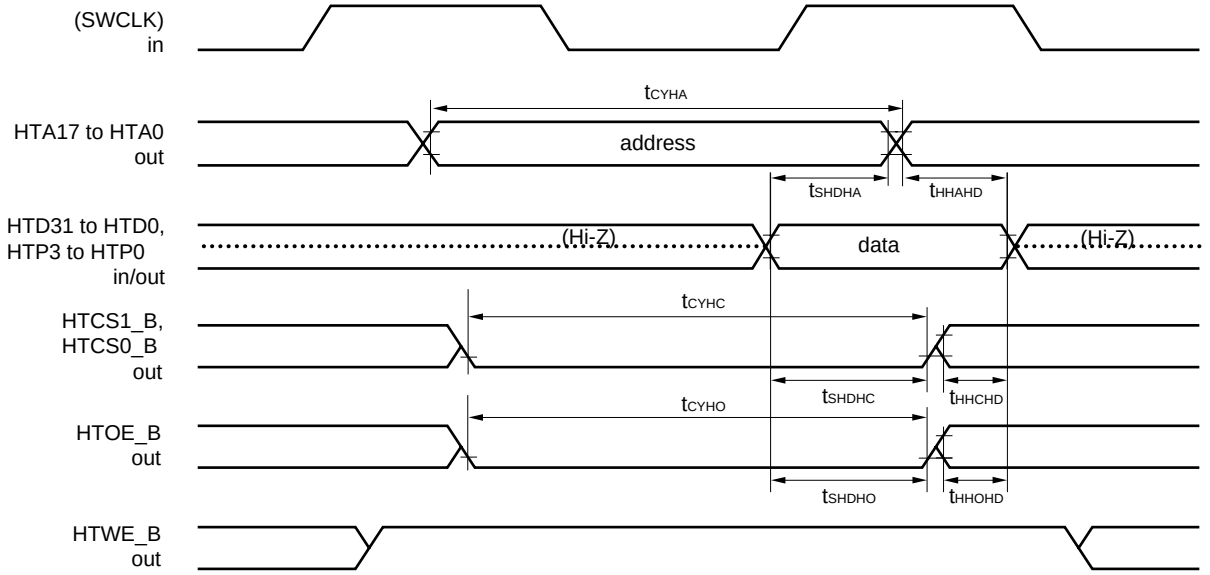
Processor Interface (16-bit mode, write)



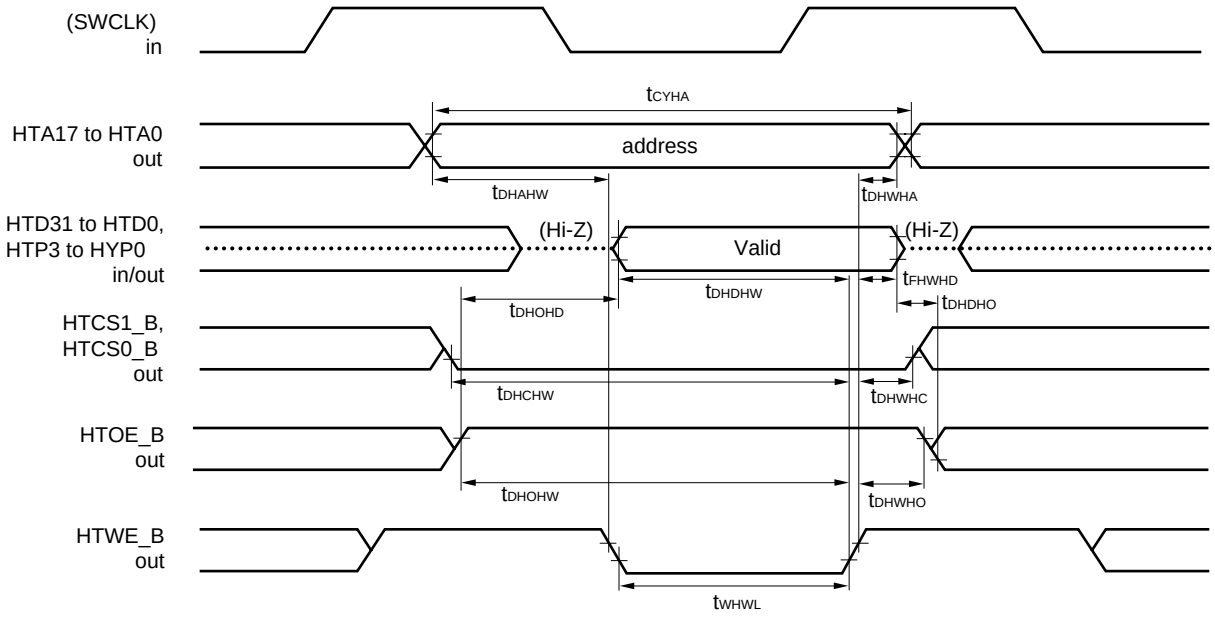
(4) HTT & control memory interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
HTA cycle time	t_{CYHA}	Load capacitance: 70 pF	t_{CYSK} – 2			ns
HTD, HTP setup time (vs. HTA)	t_{SHDHA}		9			ns
HTD, HTP hold time (vs. HTA)	t_{HHAHD}		1			ns
HTCS_B cycle time	t_{CYHC}	Load capacitance: 70 pF	t_{CYSK} – 2			ns
HTD, HTP setup time (vs. HTCS_B)	t_{SHDHC}		12			ns
HTD, HTP hold time (vs. HTCS_B)	t_{HHCHD}		1			ns
HTOE_B cycle time	t_{CYHO}	Load capacitance: 70 pF	t_{CYSK} – 2			ns
HTD, HTP setup time (vs. HTOE_B)	t_{SHDHO}		12			ns
HTD, HTP hold time (vs. HTOE_B)	t_{HHOHD}		1			ns
HTWE_B low-level width	t_{WHWL}	Load capacitance: 70 pF	t_{WSKL} – 3			ns
Data→ HTWE_B↑ output delay time	t_{DHDHW}	Load capacitance: 70 pF	t_{WSKL} – 4			ns
HTWE_B↑→ data float output delay time	t_{FHWHD}	Load capacitance: 50 pF	0			ns
HTA→ HTWE_B↓ output delay time	t_{DHAHW}	Load capacitance: 70 pF	t_{WSKH} – 6			ns
HTCS_B↓→ HTWE_B↑ output delay time	t_{DHCHW}	Load capacitance: 70 pF	t_{CYSK} – 8			ns
HTOE_B↑→ HTWE_B↑ output delay time	t_{DHOHW}	Load capacitance: 70 pF	t_{CYSK} – 8			ns
HTWE_B↑→ HTA output delay time	t_{DHWHA}	Load capacitance: 70 pF	0			ns
HTWE_B↑→ HTCS_B↑ output delay time	t_{DHWHC}	Load capacitance: 50 pF	0			ns
HTWE_B↑→ HTOE_B↓ output delay time	t_{DHWHO}	Load capacitance: 70 pF	0			ns
HTD float→ HTOE_B↓ output delay time	t_{DHDHO}	Load capacitance: 70 pF	0			ns
HTOE_B↑→ data output delay time	t_{DHOHD}	Load capacitance: 70 pF	t_{WSKH} – 5			ns

HTT & Control Memory Interface (Read)



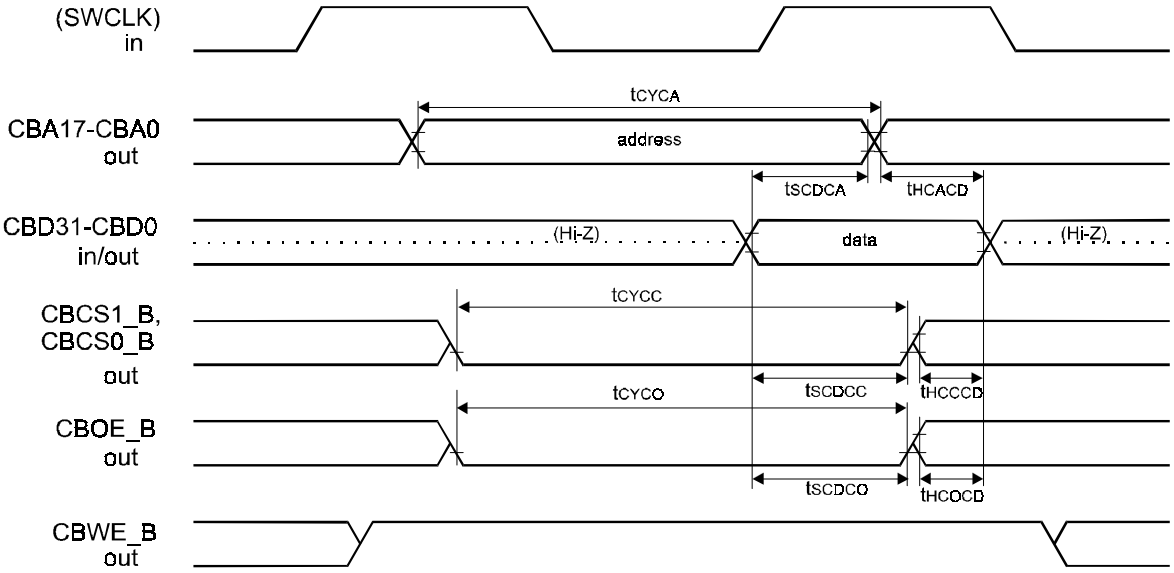
HTT & Control Memory Interface (Write)



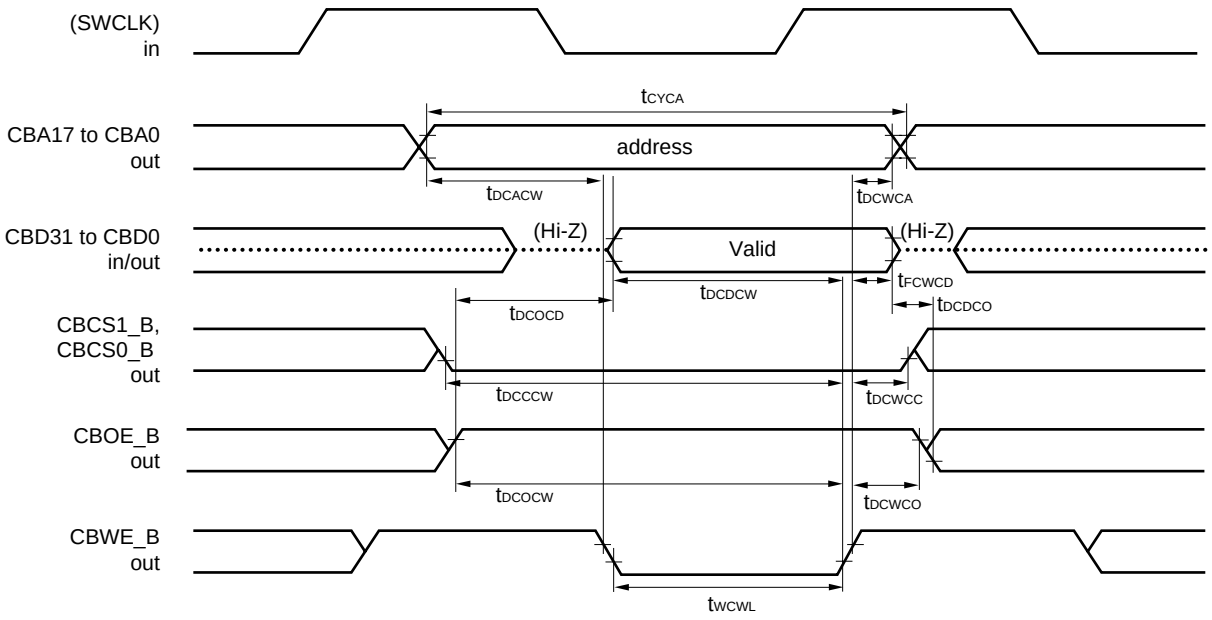
(5) Cell buffer memory interface

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CBA cycle time	t_{CYCA}	Load capacitance: 70 pF	t_{CYSK} – 2			ns
CBD setup time (vs. CBA)	t_{SCDCA}		9			ns
CBD hold time (vs. CBA)	t_{HCACD}		1			ns
CBCS_B cycle time	t_{CYCC}	Load capacitance: 70 pF	t_{CYSK} – 2			ns
CBD setup time (vs. CBCS_B)	t_{SCDCC}		12			ns
CBD hold time (vs. CBCS_B)	t_{HCCCD}		1			ns
CBOE_B cycle time	t_{CYCO}	Load capacitance: 70 pF	t_{CYSK} – 2			ns
CBD setup time (vs. CBOE_B)	t_{SCDCO}		12			ns
CBD hold time (vs. CBOE_B)	t_{HCOCD}		1			ns
CBWE_B low-level width	t_{WCWL}	Load capacitance: 70 pF	t_{WSKL} – 3			ns
Data→ CBWE_B↑ output delay time	t_{DCDCW}	Load capacitance: 70 pF	t_{WSKL} – 4			ns
CBWE_B↑→ data float output delay time	t_{FCWCD}	Load capacitance: 50 pF	0			ns
CBA→ CBWE_B↓ output delay time	t_{DCACW}	Load capacitance: 70 pF	t_{WSKH} – 6			ns
CBCS_B↓→ CBWE_B↓ output delay time	t_{DCCCW}	Load capacitance: 70 pF	t_{CYSK} – 8			ns
CBOE_B↑→ CBWE_B↓ output delay time	t_{DCOCW}	Load capacitance: 70 pF	t_{CYSK} – 8			ns
CBWE_B↑→ CBA output delay time	t_{DCWCA}	Load capacitance: 70 pF	0			ns
CBWE_B↑→ CBCS_B↑ output delay time	t_{DCWCC}	Load capacitance: 50 pF	0			ns
CBWE_B↑→ CBOE_B↓ output delay time	t_{DCWCO}	Load capacitance: 70 pF	0			ns
CBD float→ CBOE_B↓ output delay time	t_{DCDCO}	Load capacitance: 70 pF	0			ns
CBOB_B↑→ data output delay time	t_{DCOCD}	Load capacitance: 70 pF	t_{WSKH} – 5			ns

Cell Buffer Memory Interface (Read)



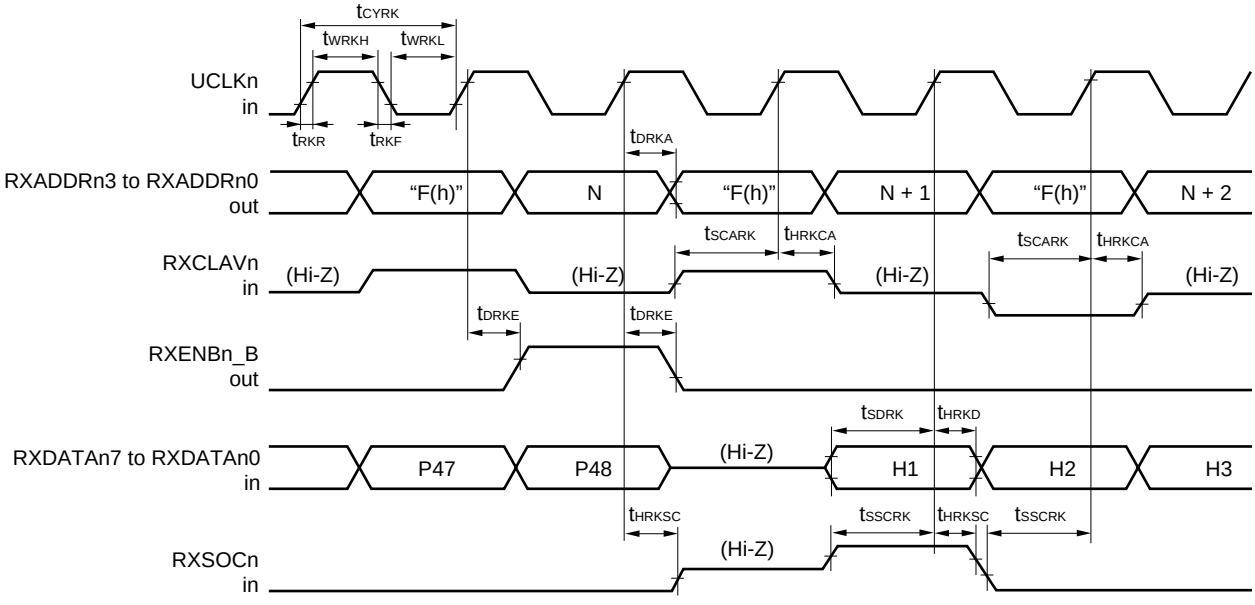
Cell Buffer Memory Interface (Write)



(6) UTOPIA interface (reception)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UCLK cycle time	t_{CYRK}		25		125	ns
UCLK high-level width	t_{WRKH}		10			ns
UCLK low-level width	t_{WRKL}		10			ns
UCLK rise time	t_{RKR}				2	ns
UCLK fall time	t_{RKF}				2	ns
UCLK↑→ RXADDR output delay time	t_{DRKA}	Load capacitance: 50 pF	1		15	ns
UCLK↑→ RXENB_B output delay time	t_{DRKE}	Load capacitance: 50 pF	1		15	ns
RXCLAV setup time (vs. UCLK↑)	t_{SCARK}		6			ns
RXCLAV hold time (vs. UCLK↑)	t_{HRKCA}		1			ns
RXDATA setup time (vs. UCLK↑)	t_{SDRK}		6			ns
RXDATA hold time (vs. UCLK↑)	t_{HRKD}		1			ns
RXSOC setup time (vs. UCLK↑)	t_{SSCRK}		6			ns
RXSOC hold time (vs. UCLK↑)	t_{HRKSC}		1			ns

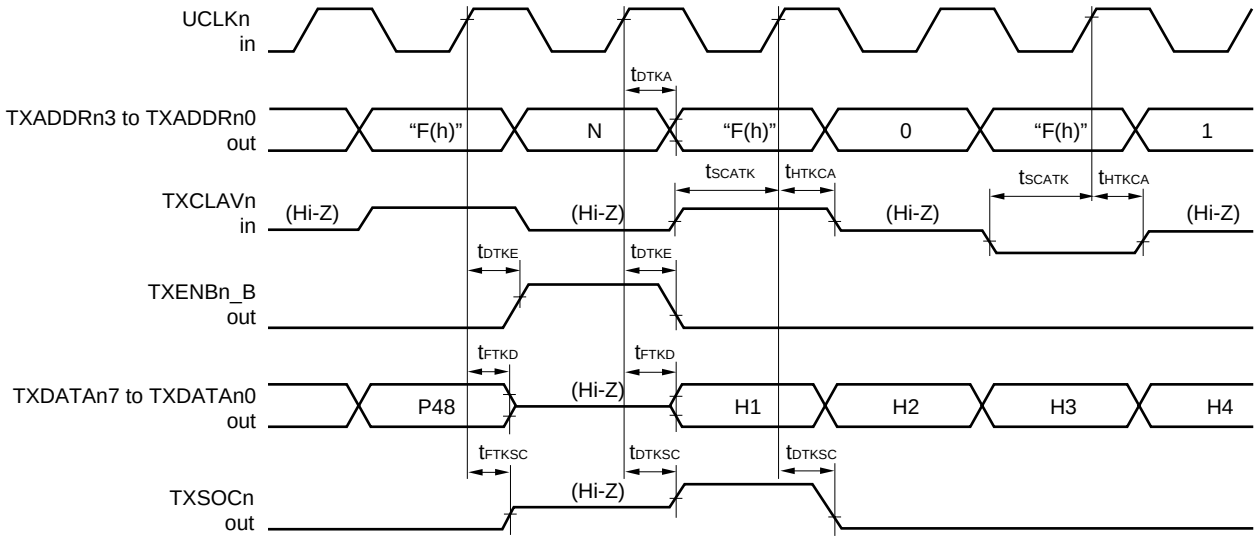
UTOPIA interface (reception) (n = 0 to 3)



(7) UTOPIA interface (transmission)

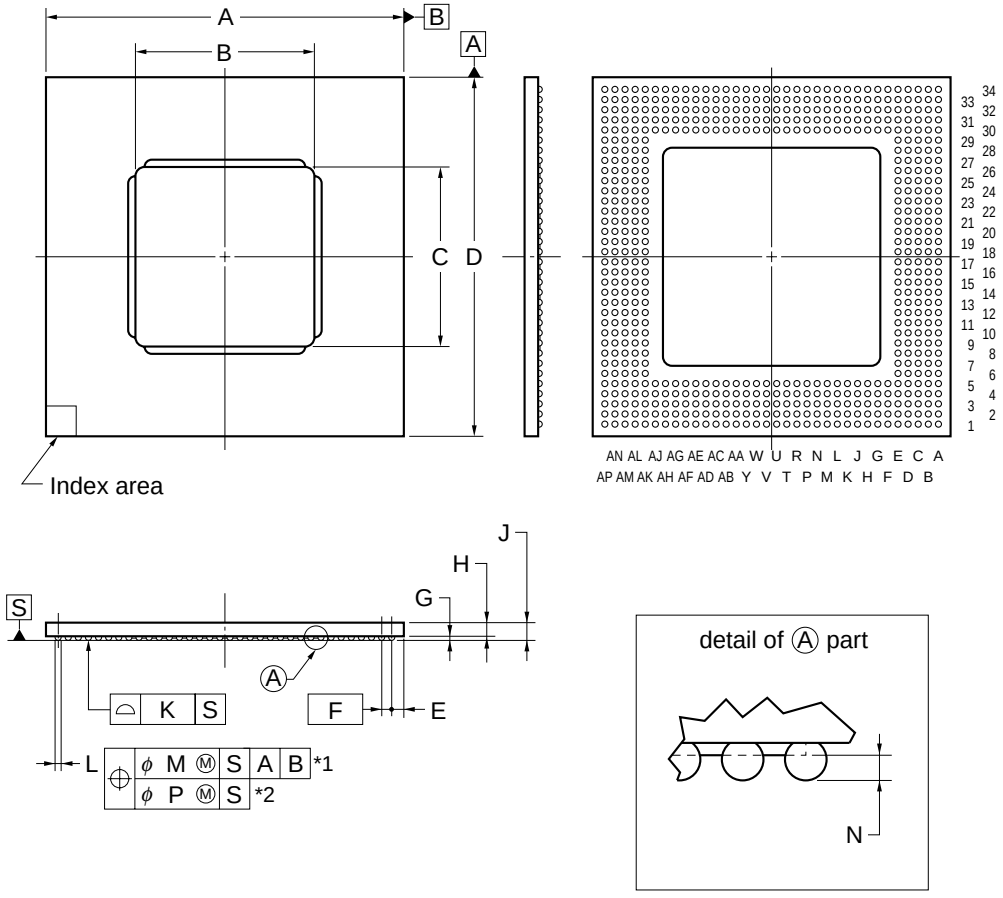
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UCLK TXADDR output delay time	t_{DTKA}	Load capacitance: 50 pF	1		15	ns
UCLK↑→ TXENB_B output delay time	t_{DTKE}	Load capacitance: 50 pF	1		15	ns
UCLK↑→ TXDATA output delay time	t_{DTKD}	Load capacitance: 50 pF	1		15	ns
UCLK↑→ TXDATA float output delay time	t_{FTKD}	Load capacitance: 50 pF	1		15	ns
UCLK↑→ TXSOC output delay time	t_{DTKSC}	Load capacitance: 50 pF	1		15	ns
UCLK↑→ TXSOC float output delay time	t_{FTKSC}	Load capacitance: 50 pF	1		15	ns
TXCLAV setup time (vs. UCLK↑)	t_{SCATK}		6			ns
TXCLAV hold time (vs. UCLK↑)	t_{HTKCA}		1			ns

UTOPIA interface (transmission) (n = 0 to 3)



3. PACKAGE DRAWINGS

580 PIN PLASTIC BGA (45x45)



NOTES

*1 Each ball centerline is located within ϕ0.30 mm of its true position (T.P.) at maximum material condition.

*2 Each ball centerline is located within ϕ0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	45.00±0.20
B	22.5
C	22.5
D	45.00±0.20
E	1.545
F	1.27 (T.P.)
G	0.60±0.10
H	1.88
J	2.48±0.30
K	0.15
L	ϕ0.75±0.15
M	0.30
N	0.25 MIN.
P	0.10

S580S2-K6-2

4. RECOMMENDED SOLDERING CONDITIONS

It is recommended to solder this product under the conditions described below.

For the details of the recommended soldering conditions, refer to Information Document **"Semiconductor Device Mounting Technology Manual" (C10535E)**.

For soldering methods and conditions other than those recommended, consult NEC.

Surface mount type

- μPD98410S2-K6: 580-pin plastic BGA (45 × 45 mm)

Soldering Method	Soldering Condition	Symbol of Recommended Soldering
Infrared reflow	Package peak temperature: 220 °C, Time: 60 seconds MAX. (at 183 °C MIN.), Number of times: 3 MAX., Number of days: 2 days [Note] (after that, prebaking is necessary at 125 °C for 20 hours) **<Precaution>** Products other than in heat-resistance trays (such as those packaged in a magazine, taping, or non-heat-resistance tray cannot be baked while they are in their package.	IR20-202-3
Partial heating	Pin temperature: 300 °C MAX., Time: 3 seconds MAX. (per side of device)	–

Note Number of days in storage after the dry pack has been opened. The storage conditions are at 25 °C, 65 % RH MAX.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

NEASCOT-X10 is a trademark of NEC Corporation.

The export of this product from Japan is prohibited without governmental license. To export or re-export this product from a country other than Japan may also be prohibited without a license from that country. Please call an NEC sales representative.

M4 96.5