NEC

MOS INTEGRATED CIRCUIT

μPD78P4908

16-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78P4908, 78K/IV series' product, is a one-time PROM version of the μPD784907 and μPD784908 with internal mask ROM.

Since user programs can be written to PROM, this microcomputer is best suited for evaluation in system development, manufacture of small quantities of multiple products, and fast start-up of applications.

For specific functions and other detailed information, consult the following user's manuals.
These manuals are required reading for design work.

μPD784908 Subseries User's Manual - Hardware : U11787E
78K/IV Series User's Manual - Instruction : U10905E

FEATURES

- 78K/IV series
- Internal PROM: 128 Kbytes
- Internal RAM: 4,352 bytes
- ★ Supply voltage: V_{DD} = 4.5 to 5.5 V
  (At main clock: f_{XX} = 12.58 MHz, internal system clock = f_{XX}: f_{CYK} = 79 ns)
  V_{DD} = 4.0 to 5.5 V
  (Other than above: f_{CYK} = 159 ns)

ORDERING INFORMATION

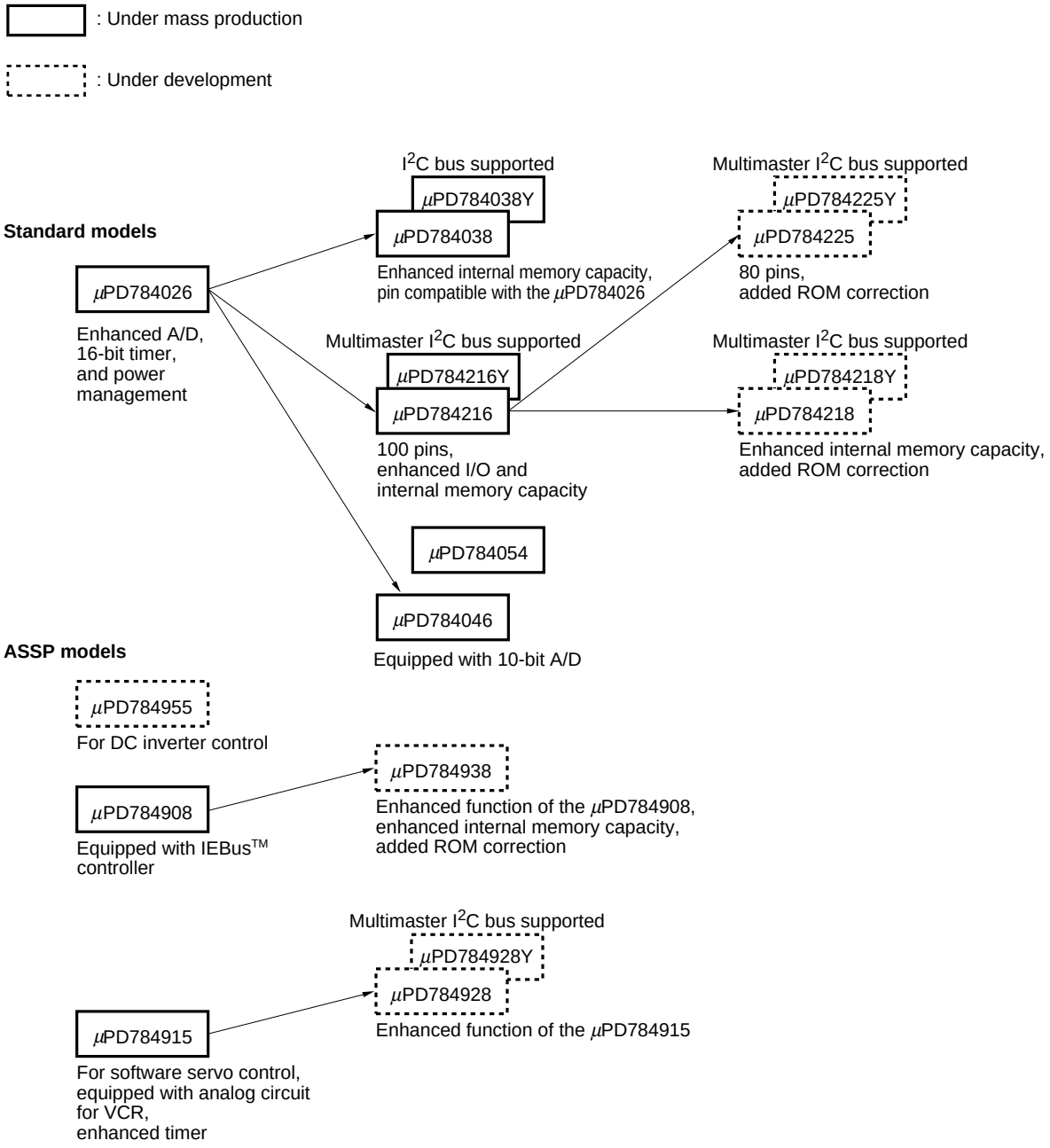
Part number	Package	Internal ROM
μPD78P4908GF-3BA	100-pin plastic QFP (14 × 20 mm)	One-time PROM

The information in this document is subject to change without notice.

Document No. U11681EJ2V0DS00 (2nd edition)
Date Published February 1999 N CP(K)
Printed in Japan

The mark ★ shows major revised points.

★ 78K/IV SERIES PRODUCT DEVELOPMENT DIAGRAM



FUNCTIONS

(1/2)

Item			Function		
Number of basic instructions (mnemonics)			113		
General-purpose register			8 bits × 16 registers × 8 banks, or 16 bits × 8 registers × 8 banks (memory mapping)		
★ Minimum instruction execution time			• 320 ns/636 ns/1.27 μs/2.54 μs (at 6.29 MHz) • 160 ns/320 ns/636 ns/1.27 μs (at 12.58 MHz)		
Internal memory		ROM	128 Kbytes		
		RAM	4,352 bytes		
Memory space			Program and data: 1 Mbyte		
I/O ports		Total	80		
		Input	8		
		Input/output	72		
	Additional function pins[Note]	LED direct drive outputs	24		
		Transistor direct drive	8		
		N-ch open drain	4		
Real-time output ports			4 bits × 2, or 8 bits × 1		
IEBus controller			Incorporated (simple version)		
Timer/counter			Timer/counter 0: (16 bits)	Timer register × 1 Capture register × 1 Compare register × 2	Pulse output capability • Toggle output • PWM/PPG output • One-shot pulse output
			Timer/counter 1: (16 bits)	Timer register × 1 Capture register × 1 Capture/compare register × 1 Compare register × 1	Real-time output port
			Timer/counter 2: (16 bits)	Timer register × 1 Capture register × 1 Capture/compare register × 1 Compare register × 1	Pulse output capability • Toggle output • PWM/PPG output
			Timer 3: (16 bits)	Timer register × 1 Compare register × 1	
Clock timer			Interrupt requests are generated at 0.5-second intervals. (A clock timer oscillator is incorporated.) ★ Either the main clock (6.29 MHz/12.58 MHz) or real-time clock (32.768 kHz) can be selected as the input clock.		
Clock output			Selected from f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, or $f_{CLK}/16$ (can be used as a 1-bit output port)		
PWM outputs			12-bit resolution × 2 channels		
Serial interface			UART/IOE (3-wire serial I/O) : 2 channels (incorporating baud rate generator) CSI (3-wire serial I/O) : 2 channels		

Note Additional function pins are included in the I/O pins.

(2/2)

Item		Function
A/D converter		8-bit resolution × 8 channels
Watchdog timer		1 channel
Standby		HALT/STOP/IDLE mode
Interrupt	Hardware source	27 (20 internal, 7 external (sampling clock variable input: 1))
	Software source	BRK or BRKCS instruction, operand error
	Nonmaskable	1 internal, 1 external
	Maskable	19 internal, 6 external
		• 4-level programmable priority • 3 operation statuses: vectored interrupt, macro service, context switching
★ Power supply voltage		• V_{DD} = 4.5 to 5.5 V (At main clock: f_{XX} = 12.58 MHz, internal system clock = f_{XX}: f_{CYK} = 79 ns) • V_{DD} = 4.0 to 5.5 V (Other than above: f_{CYK} = 159 ns)
Package		100-pin plastic QFP (14 × 20 mm)

CONTENTS

1. DIFFERENCES BETWEEN μPD78P4908 AND MASK ROM PRODUCTS

The μPD78P4908 is produced by replacing the mask ROM in the μPD784907 or μPD784908 with PROM to which data can be written. The functions of the μPD78P4908 are the same as those of the μPD784907 or μPD784908 except for the PROM specification such as writing and verification, except that the PROM size can be changed to 96 or 128 Kbytes, and except that the internal RAM size can be changed to 3,584 or 4,352 bytes.

Table 1-1 shows the differences between these products.

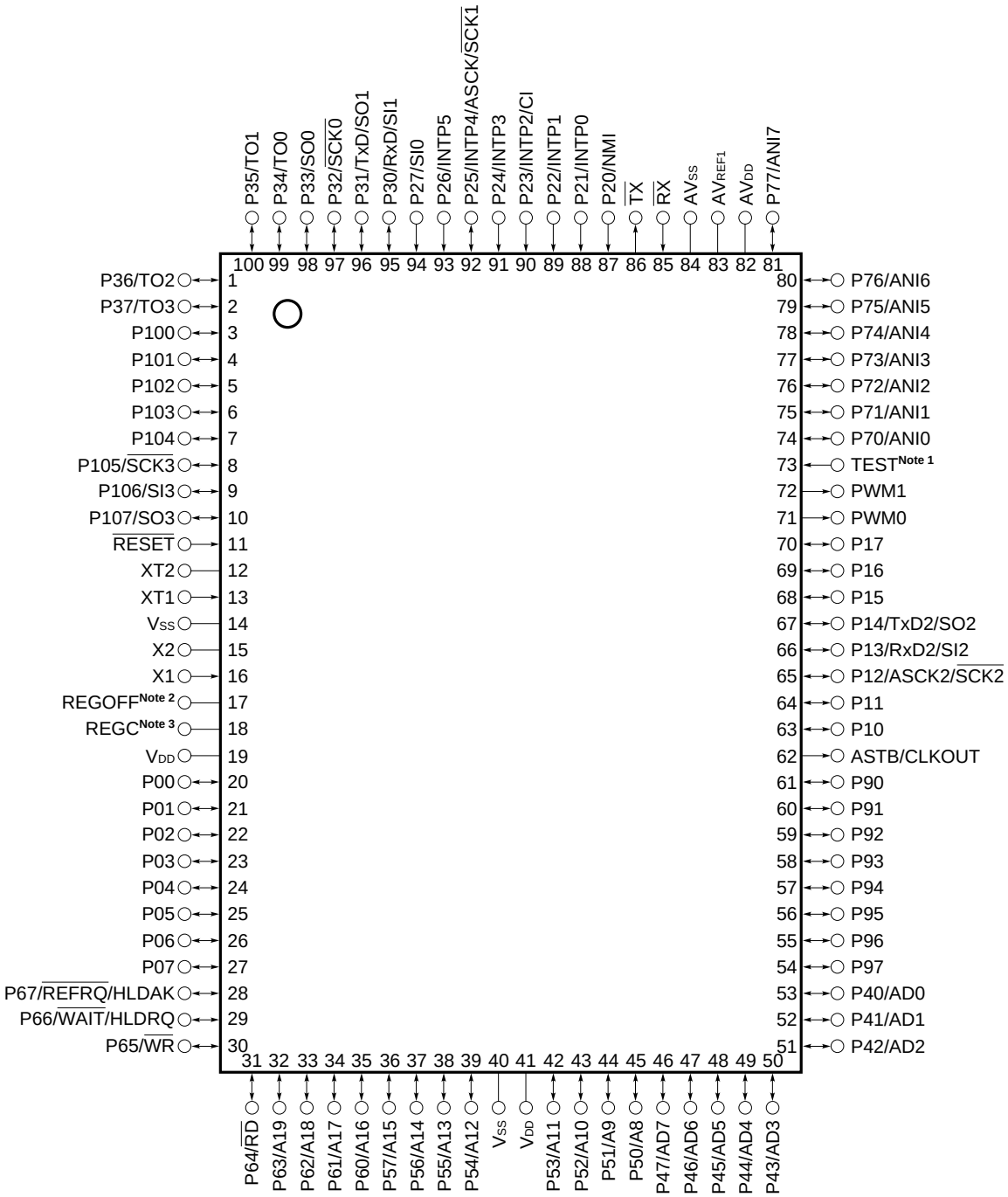
Table 1-1. Differences Between the μPD78P4908 and Mask ROM Products

Item \ Product name	μPD78P4908	μPD784907	μPD784908
Internal program memory	• 128-Kbyte PROM • Can be changed to 96 Kbytes by IMS	• 96-Kbyte mask ROM	• 128-Kbyte mask ROM
Internal RAM	• 4,352-byte internal RAM • Can be changed to 3,584 bytes by IMS	• 3,584-byte internal RAM	• 4,352-byte internal RAM
Pin connection	Pin functions related to writing or reading of PROM have been added to the μPD78P4908.		
★ Power supply voltage	• V_{DD} = 4.5 to 5.5 V (At main clock: f_{XX} = 12.58 MHz, internal system clock = f_{XX}: f_{CYK} = 79 ns) • V_{DD} = 4.0 to 5.5 V (Other than above: f_{CYK} = 159 ns)	• V_{DD} = 4.0 to 5.5 V (At main clock: f_{XX} = 12.58 MHz, internal system clock = f_{XX}: f_{CYK} = 79 ns) • V_{DD} = 3.5 to 5.5 V (Other than above: f_{CYK} = 159 ns)	
Electrical characteristics	Partially differs between these products.		

2. PIN CONFIGURATION (TOP VIEW)

(1) Normal operation mode

- 100-pin plastic QFP (14 × 20 mm)
  μPD78P4908GF-3BA



Notes 1. Connect the TEST pin to VSS directly.

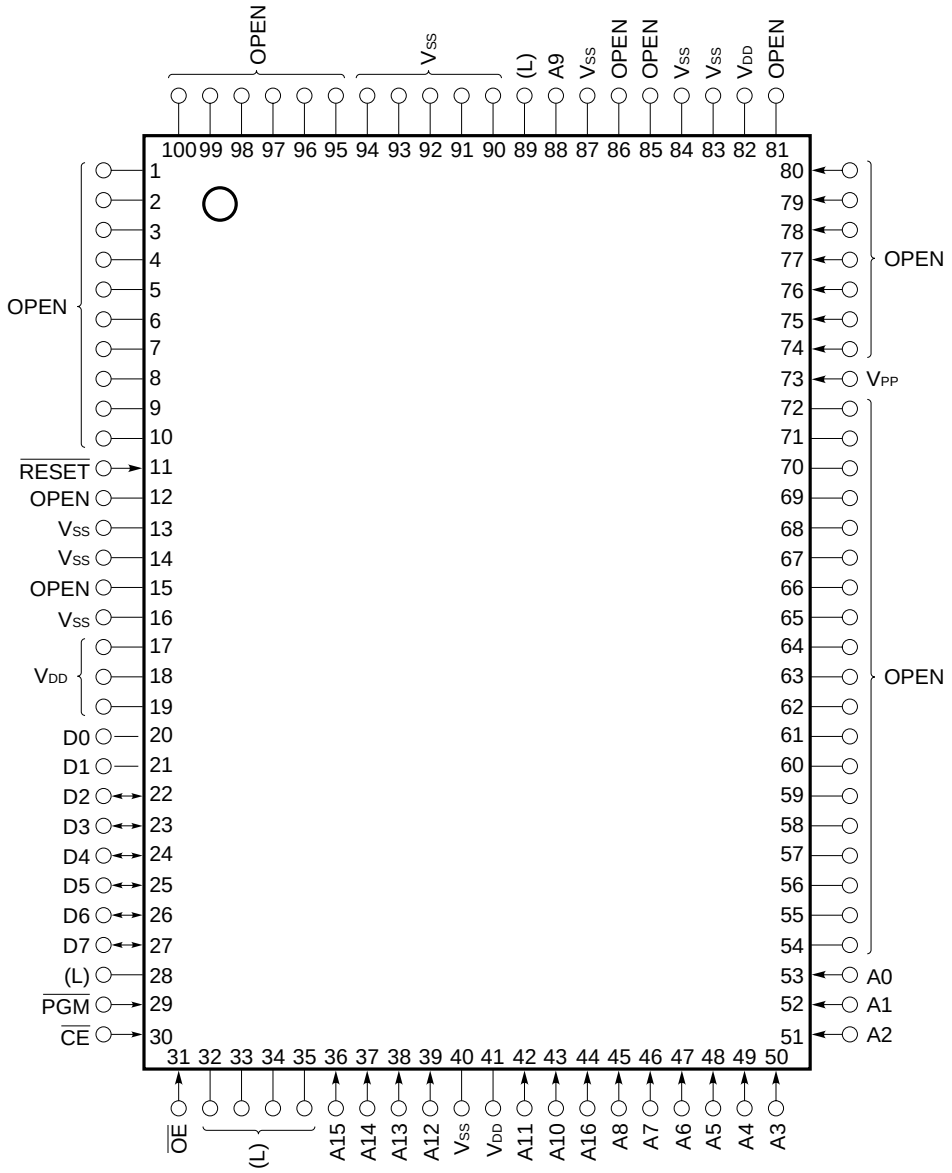
2. Connect the REGOFF pin to VSS directly (select regulator operation)

3. Connect the REGC pin to VSS through a 1-μF capacitor.

A8-A19 : Address bus
AD0-AD7 : Address/data bus
ANI0-ANI7 : Analog input
ASCK, ASCK2 : Asynchronous serial clock
ASTB : Address strobe
AV_{DD} : Analog power supply
AV_{REF1} : Reference voltage
AV_{SS} : Analog ground
CI : Clock input
CLKOUT : Clock output
HLDAK : Hold acknowledge
HLDRQ : Hold request
INTP0-INTP5 : Interrupt from peripherals
NMI : Non-maskable interrupt
P00-P07 : Port 0
P10-P17 : Port 1
P20-P27 : Port 2
P30-P37 : Port 3
P40-P47 : Port 4
P50-P57 : Port 5
P60-P67 : Port 6
P70-P77 : Port 7
P90-P97 : Port 9
P100-P107 : Port 10
PWM0, PWM1 : Pulse width modulation output
$\overline{RD}$: Read strobe
$\overline{REFRQ}$: Refresh request
REGC : Regulator capacitance
REGOFF : Regulator off
$\overline{RESET}$: Reset
$\overline{RX}$: IEBus receive data
RxD, RxD2 : Receive data
$\overline{SCK0}$-$\overline{SCK3}$: Serial clock
SI0-SI3 : Serial input
SO0-SO3 : Serial output
TEST : Test
TO0-TO3 : Timer output
$\overline{TX}$: IEBus transmit data
TxD, TxD2 : Transmit data
V_{DD} : Power supply
V_{SS} : Ground
$\overline{WAIT}$: Wait
$\overline{WR}$: Write strobe
X1, X2 : Crystal (main system clock)
XT1, XT2 : Crystal (watch)

(2) PROM programming mode

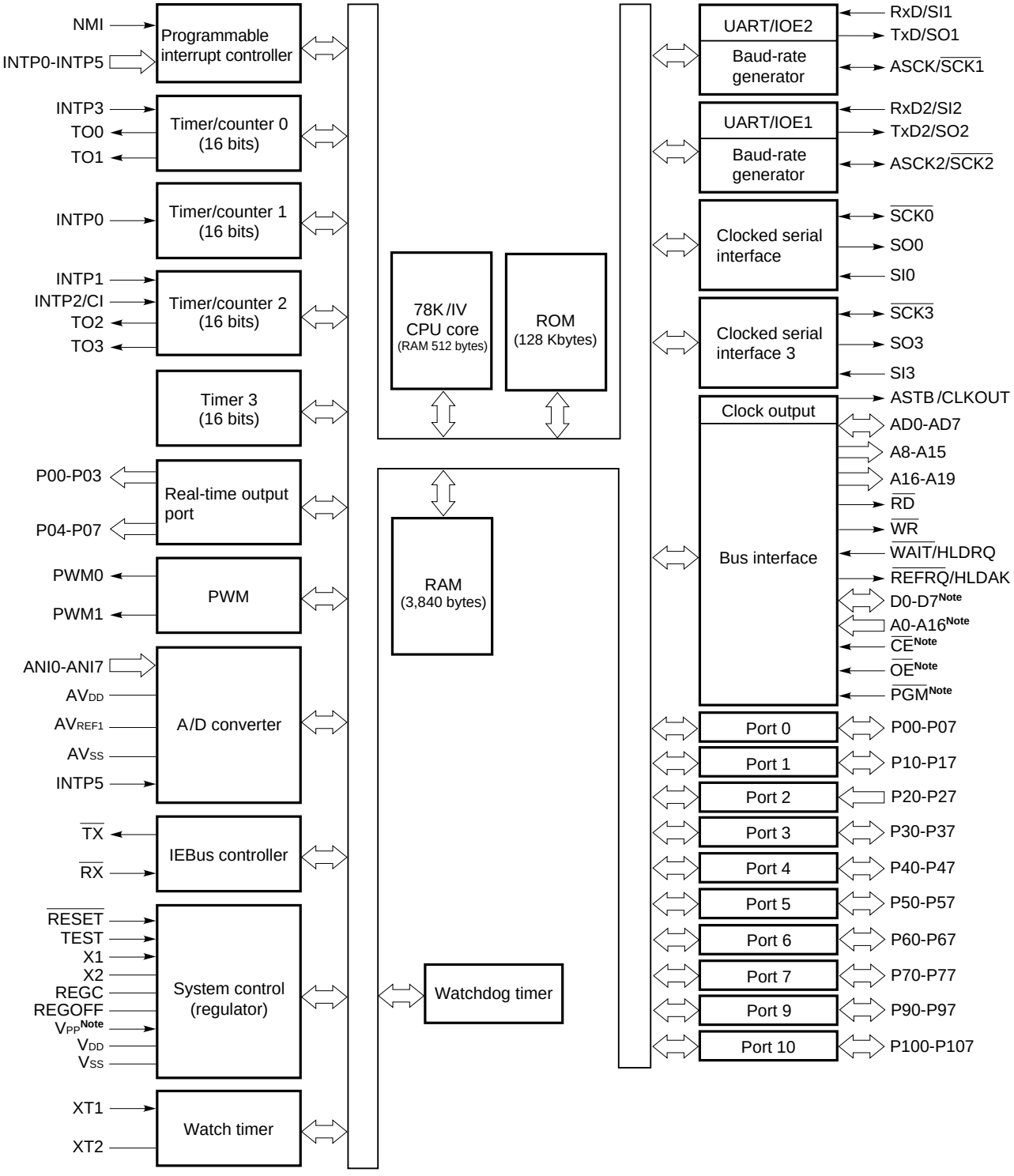
- 100-pin plastic QFP (14 × 20 mm)
  μPD78P4908GF-3BA



Caution L : Connect these pins separately to the V_{SS} pins through 10-kΩ pull-down resistors.
V_{SS} : To be connected to the ground.
Open : Nothing should be connected on these pins.
$\overline{RESET}$: Set a low-level input.

A0-A16 : Address bus
$\overline{CE}$: Chip enable
D0-D7 : Data bus
$\overline{OE}$: Output enable
$\overline{PGM}$: Program
$\overline{RESET}$: Reset
V_{DD} : Power supply
V_{PP} : Programming power supply
V_{SS} : Ground

3. BLOCK DIAGRAM



Note In the PROM programming mode.

4. PIN FUNCTIONS

4.1 PINS FOR NORMAL OPERATING MODE

(1) Port pins (1/2)

Pin	I/O	Also used as	Function
P00-P07	I/O	—	Port 0 (P0): • 8-bit I/O port. • Functions as a real-time output port (4 bits × 2). • Inputs and outputs can be specified bit by bit. • The use of built-in pull-up resistors can be simultaneously specified by software for all pins in input mode. • Can drive a transistor.
P10	I/O	—	Port 1 (P1): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of built-in pull-up resistors can be simultaneously specified by software for all pins in input mode. • Can drive LED.
P11		—	
P12		ASCK2/$\overline{\text{SCK2}}$	
P13		RxD2/SI2	
P14		TxD2/SO2	
P15-P17		—	
P20	Input	NMI	Port 2 (P2): • 8-bit input-only port. • P20 does not function as a general-purpose port (nonmaskable interrupt). However, the input level can be checked by an interrupt service routine. • The use of built-in pull-up resistors can be specified by software for pins P22 to P27 (in units of 6 bits). • The P25/INTP4/ASCK/$\overline{\text{SCK1}}$ pin functions as the $\overline{\text{SCK1}}$ input/output pin by CSIM1.
P21		INTP0	
P22		INTP1	
P23		INTP2/CI	
P24		INTP3	
P25		INTP4/ASCK/$\overline{\text{SCK1}}$	
P26		INTP5	
P27		SI0	
P30	I/O	RxD/SI1	Port 3 (P3): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of built-in pull-up resistors can be simultaneously specified by software for all pins in input mode. • P32 and P33 can be set as the N-ch open-drain pin.
P31		TxD/SO1	
P32		$\overline{\text{SCK0}}$	
P33		SO0	
P34-P37		TO0-TO3	
P40-P47	I/O	AD0-AD7	Port 4 (P4): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of built-in pull-up resistors can be simultaneously specified by software for all pins in input mode. • Can drive LED.

(1) Port pins (2/2)

Pin	I/O	Also used as	Function
P50-P57	I/O	A8-A15	Port 5 (P5): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of built-in pull-up resistors can be simultaneously specified by software for all pins in input mode. • Can drive LED.
P60-P63	I/O	A16-A19	Port 6 (P6): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of built-in pull-up resistors can be simultaneously specified by software for all pins in input mode.
P64		$\overline{RD}$	
P65		$\overline{WR}$	
P66		$\overline{WAIT}$/HLDRQ	
P67		$\overline{REFRQ}$/HLDAK	
P70-P77	I/O	ANI0-ANI7	Port 7 (P7): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit.
P90-P97	I/O	—	Port 9 (P9): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of built-in pull-up resistors can be simultaneously specified by software for all pins in input mode.
P100-P104	I/O	—	Port 10 (P10): • 8-bit I/O port. • Inputs and outputs can be specified bit by bit. • The use of built-in pull-up resistors can be simultaneously specified by software for all pins in input mode. • P105 and P107 can be set as the N-ch open-drain pin.
P105		$\overline{SCK3}$	
P106		SI3	
P107		SO3	

(2) Non-port pins (1/2)

Pin	I/O	Also used as	Function	
TO0-TO3	Output	P34-P37	Timer output	
CI	Input	P23/INTP2	Input of a count clock for timer/counter 2	
RxD	Input	P30/SI1	Serial data input (UART0)	
RxD2		P13/SI2	Serial data input (UART2)	
TxD	Output	P31/SO1	Serial data output (UART0)	
TxD2		P14/SO2	Serial data output (UART2)	
ASCK	Input	P25/INTP4/$\overline{\text{SCK1}}$	Baud rate clock input (UART0)	
ASCK2		P12/$\overline{\text{SCK2}}$	Baud rate clock input (UART2)	
SI0	Input	P27	Serial data input (3-wire serial I/O 0)	
SI1		P30/RxD	Serial data input (3-wire serial I/O 1)	
SI2		P13/RxD2	Serial data input (3-wire serial I/O 2)	
SI3		P106	Serial data input (3-wire serial I/O 3)	
SO0	Output	P33	Serial data output (3-wire serial I/O 0)	
SO1		P31/TxD	Serial data output (3-wire serial I/O 1)	
SO2		P14/TxD2	Serial data output (3-wire serial I/O 2)	
SO3		P107	Serial data output (3-wire serial I/O 3)	
$\overline{\text{SCK0}}$	I/O	P32	Serial clock I/O (3-wire serial I/O 0)	
$\overline{\text{SCK1}}$		P25/INTP4/ASCK	Serial clock I/O (3-wire serial I/O 1)	
$\overline{\text{SCK2}}$		P12/ASCK2	Serial clock I/O (3-wire serial I/O 2)	
$\overline{\text{SCK3}}$		P105	Serial clock I/O (3-wire serial I/O 3)	
NMI	Input	P20	External interrupt request	—
INTP0		P21		• Input of a count clock for timer/counter 1 • Capture/trigger signal for CR11 or CR12
INTP1		P22		• Input of a count clock for timer/counter 2 • Capture/trigger signal for CR22
INTP2		P23/CI		• Input of a count clock for timer/counter 2 • Capture/trigger signal for CR21
INTP3		P24		• Input of a count clock for timer/counter 0 • Capture/trigger signal for CR02
INTP4		P25/ASCK/$\overline{\text{SCK1}}$		—
INTP5		P26		Input of a conversion start trigger for A/D converter
AD0-AD7	I/O	P40-P47	Time multiplexing address/data bus (for connecting external memory)	
A8-A15	Output	P50-P57	High-order address bus (for connecting external memory)	
A16-A19	Output	P60-P63	High-order address during address expansion (for connecting external memory)	
$\overline{\text{RD}}$	Output	P64	Strobe signal output for reading the contents of external memory	
$\overline{\text{WR}}$	Output	P65	Strobe signal output for writing on external memory	
$\overline{\text{WAIT}}$	Input	P66/HLDRQ	Wait signal insertion	
$\overline{\text{REFRQ}}$	Output	P67/HLDAK	Refresh pulse output to external pseudo static memory	
HLDRQ	Input	P66/$\overline{\text{WAIT}}$	Input of bus hold request	
HLDAK	Output	P67/$\overline{\text{REFRQ}}$	Output of bus hold response	
ASTB	Output	CLKOUT	Latch timing output of time multiplexing address (A0-A7) (for connecting external memory)	

(2) Non-port pins (2/2)

Pin	I/O	Also used as	Function
CLKOUT	Output	ASTB	Clock output
PWM0	Output	—	PWM output 0
PWM1	Output	—	PWM output 1
$\overline{RX}$	Input	—	Data input (IEBus)
$\overline{TX}$	Output	—	Data output (IEBus)
★ REGC	—	—	Capacitor connection for stabilizing the regulator output/Power supply when the regulator is stopped. Connect to V_{SS} via a 1-μF capacitor.
★ REGOFF	—	—	Signal for specifying regulator operation. Directly connect to V_{SS} (regulator selected).
$\overline{RESET}$	Input	—	Chip reset
X1	Input	—	Crystal input for system clock oscillation (A clock pulse can also be input to the X1 pin.)
X2	—		
XT1	Input	—	Real-time clock connection
XT2	—	—	
ANI0-ANI7	Input	P70-P77	Analog voltage inputs for the A/D converter
AV_{REF1}	—	—	Application of A/D converter reference voltage
AV_{DD}			Positive power supply for the A/D converter
AV_{SS}			Ground for the A/D converter
V_{DD}			Positive power supply
V_{SS}			Ground
TEST	Input		Directly connect to V_{SS}. (The TEST pin is for the IC test.)

4.2 PINS FOR PROM PROGRAMMING MODE ($V_{PP} \geq$ +5 V or +12.5 V, $\overline{RESET}$ = L)

4.2.1 Pin Functions

Pin name	I/O	Function
V_{PP}	—	PROM programming mode selection High voltage input during program write or verification
$\overline{RESET}$	Input	PROM programming mode selection
A0-A16		Address bus
D0-D7	I/O	Data bus
$\overline{CE}$	Input	PROM enable input/program pulse input
$\overline{OE}$		Read strobe input to PROM
$\overline{PGM}$		Program/program inhibit input during PROM programming mode
V_{DD}	—	Positive power supply
V_{SS}	—	GND

4.2.2 Pin Functions

(1) V_{PP} (Programming power supply): Input

Input pin for setting the μPD78P4908 to the PROM programming mode. When the input voltage on this pin is +6.5 V or more and when $\overline{\text{RESET}}$ input goes low, the μPD78P4908 enters the PROM programming mode. When $\overline{\text{CE}}$ is made low for V_{PP} = +12.5 V and $\overline{\text{OE}}$ = high, program data on D0 to D7 can be written into the internal PROM cell selected by A0 to A16.

(2) $\overline{\text{RESET}}$ (Reset): Input

Input pin for setting the μPD78P4908 to the PROM programming mode. When input on this pin is low, and when the input voltage on the V_{PP} pin goes +5 V or more, the μPD78P4908 enters the PROM programming mode.

(3) A0 to A16 (Address bus): Input

Address bus that selects an internal PROM address (0000H to 1FFFFH)

(4) D0 to D7 (Data bus): I/O

Data bus through which a program is written on or read from internal PROM

(5) $\overline{\text{CE}}$ (Chip enable): Input

This pin inputs the enable signal from internal PROM. When this signal is active, a program can be written or read.

(6) $\overline{\text{OE}}$ (Output enable): Input

This pin inputs the read strobe signal to internal PROM. When this signal is made active for $\overline{\text{CE}}$ = low, a one-byte program in the internal PROM cell selected by A0 to A16 can be read onto D0 to D7.

(7) $\overline{\text{PGM}}$ (Program): Input

The input pin for the operation mode control signal of the internal PROM.
Upon activation, writing to the internal PROM is enabled.
Upon inactivation, reading from the internal PROM is enabled.

(8) V_{DD}

Positive power supply pin

(9) V_{SS}

Ground potential pin

4.3 I/O CIRCUITS FOR PINS AND HANDLING OF UNUSED PINS

Table 4-1 describes the types of I/O circuits for pins and the handling of unused pins.

Figure 4-1 shows the configuration of these various types of I/O circuits.

Table 4-1. Types of I/O Circuits for Pins and Handling of Unused Pins (1/2)

Pin	I/O circuit type	I/O	Recommended connection method for unused pins
P00-P07	5-A	I/O	Input state: To be connected to V_{DD} Output state: To be left open
P10, P11			
P12/ASCK2/$\overline{SCK2}$	8-A		
P13/RxD2/SI2	5-A		
P14/TxD2/SO2			
P15-P17			
P20/NMI	2	Input	To be connected to V_{DD} or V_{SS}
P21/INTP0			
P22/INTP1	2-A		To be connected to V_{DD}
P23/INTP2/CI			
P24/INTP3			
P25/INTP4/ASCK/$\overline{SCK1}$	8-A	I/O	Input state: To be connected to V_{DD} Output state: To be left open
P26/INTP5	2-A	Input	To be connected to V_{DD}
P27/SI0			
P30/RxD/SI1	5-A	I/O	Input state: To be connected to V_{DD} Output state: To be left open
P31/TxD/SO1			
P32/$\overline{SCK0}$	10-A		
P33/SO0			
P34/TO0-P37/TO3	5-A		
P40/AD0-P47/AD7			
P50/A8-P57/A15			
P60/A16-P63/A19			
P64/$\overline{RD}$			
P65/$\overline{WR}$			
P66/$\overline{WAIT}$/HLDRQ			
P67/$\overline{REFRQ}$/HLDAK			
P70/ANI0-P77/ANI7	20	I/O	Input state: To be connected to V_{DD} or V_{SS} Output state: To be left open
P90-P97	5-A		
P100-P104			
P105/$\overline{SCK3}$	10-A		
P106/SI3	8-A		
P107/SO3	10-A		
ASTB/CLKOUT	4	Output	To be left open

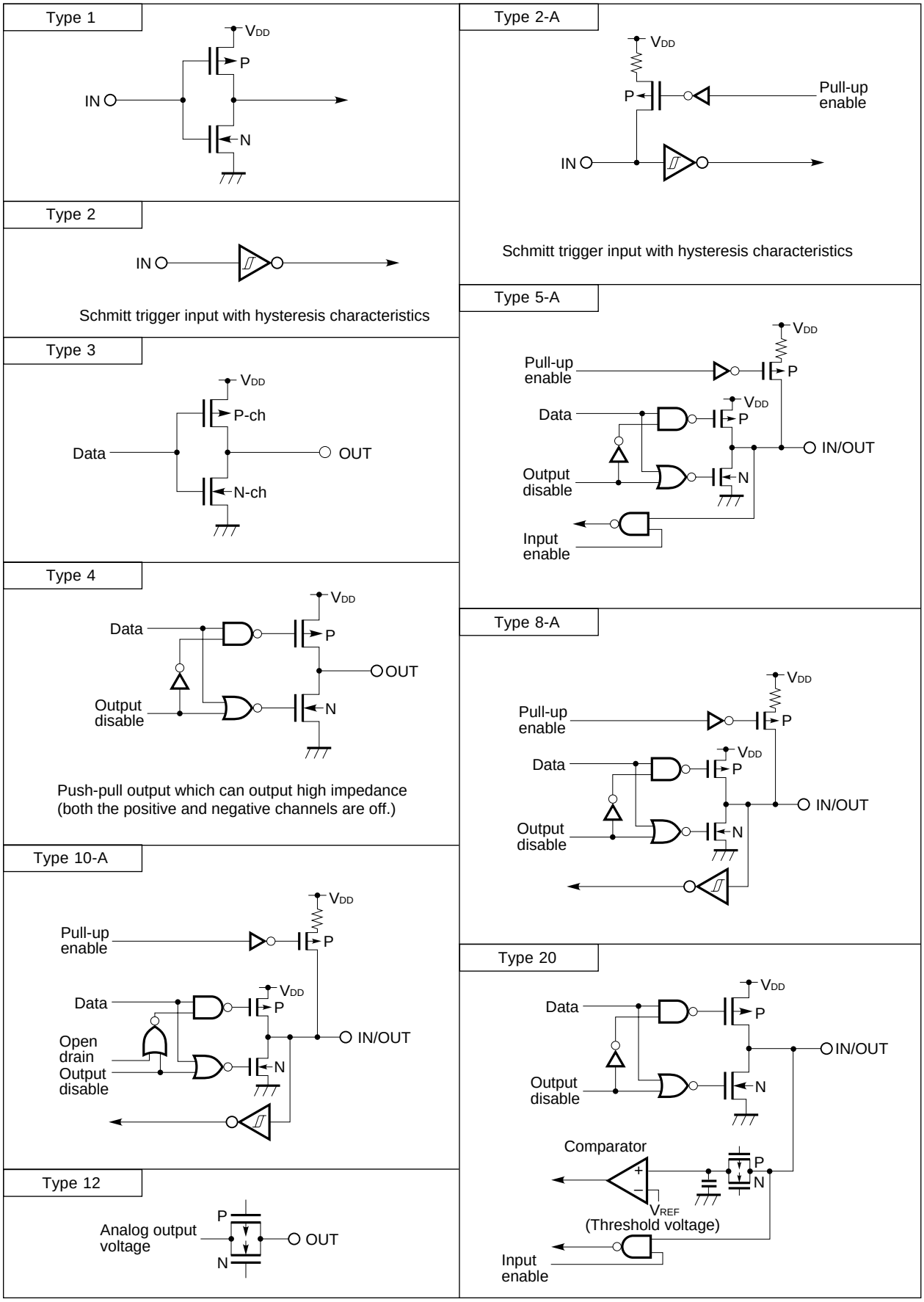
Table 4-1. Types of I/O Circuits for Pins and Handling of Unused Pins (2/2)

Pin	I/O circuit type	I/O	Recommended connection method for unused pins
$\overline{\text{RESET}}$	2	Input	—
TEST	1		To be connected to V_{SS} directly
XT2	—	—	To be left open
XT1		Input	To be connected to V_{SS}
PWM0, PWM1	3	Output	To be left open
★ $\overline{\text{RX}}$	1	Input	To be connected to V_{DD} or V_{SS}
$\overline{\text{TX}}$	3	Output	To be left open
AV_{REF1}	—	—	To be connected to V_{SS}
AV_{SS}			
AV_{DD}			To be connected to V_{DD}

Caution When the I/O mode of an I/O dual-function pin is unpredictable, connect the pin to V_{DD} through a resistor of 10 to 100 kΩ (particularly when the voltage of the reset input pin becomes higher than that of the low level input at power-on or when I/O is switched by software).

Remark Since type numbers are consistent in the 78K series, those numbers are not always serial in each product. (Some circuits are not included.)

Figure 4-1. I/O Circuits for Pins



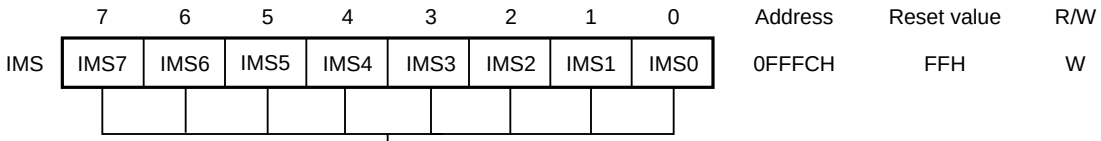
5. INTERNAL MEMORY SIZE SELECT REGISTER (IMS)

This register enables the software to avoid using part of the internal memory. The IMS can be set to establish the same memory mapping as used in mask ROM products that have different internal memory (ROM and RAM) configurations.

The IMS is set using 8-bit memory operation instructions.

A $\overline{\text{RESET}}$ input sets the IMS to FFH.

Figure 5-1. Internal Memory Size Select Register (IMS)



IMS0-7	Memory size
FFH	Same as the μPD784908
EEH	Same as the μPD784907
Other than the above	Not to be set

The IMS is not contained in a mask ROM product (μPD784907 or μPD784908). But the action is not affected if the write command to the IMS is executed to the mask ROM product.

6. PROM PROGRAMMING

The μPD78P4908 has an on-chip 128-KB PROM device for use as program memory. When programming, set the V_{PP} and $\overline{RESET}$ pins for PROM programming mode. See **2. PIN CONFIGURATION (TOP VIEW) (2) PROM programming mode** with regard to handling of other, unused pins.

6.1 OPERATION MODE

PROM programming mode is selected when +6.5 V is added to the V_{DD} pin, +12.5 V is added to the V_{PP} pin, or low-level input is added to the $\overline{RESET}$ pin. This mode can be set to operation mode by setting the $\overline{CE}$ pin, $\overline{OE}$ pin, and $\overline{PGM}$ pin as shown in Table 6-1 below.

In addition, the PROM contents can be read by setting read mode.

Table 6-1. PROM Programming Operation Mode

Pin / Operation mode	$\overline{RESET}$	V_{PP}	V_{DD}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	D0-D7
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				×	H	H	High impedance
				×	L	L	
Read		+5 V	+5 V	L	L	H	Data output
Output disable				L	H	×	High impedance
Standby				H	×	×	High impedance

Remark × = L or H

(1) Read mode

Set $\overline{CE}$ to L and $\overline{OE}$ to L to set read mode.

(2) Output disable mode

Set $\overline{OE}$ to H to set high impedance for data output and output disable mode.

Consequently, if several μPD78P4908 devices are connected to a data bus, the $\overline{OE}$ pins can be controlled to select data output from any of the devices.

(3) Standby mode

Set $\overline{CE}$ to H to set standby mode.

In this mode, data output is set to high impedance regardless of the $\overline{OE}$ setting.

(4) Page data latch mode

At the beginning of page write mode, set $\overline{CE}$ to H, $\overline{PGM}$ to H, and $\overline{OE}$ to L to set page data latch mode.

In this mode, 1 page (4 bytes) of data are latched to the internal address/data latch circuit.

(5) Page write mode

After latching the address and data for one page (4 bytes) using page data latch mode, adding a 0.1 ms program pulse (active, low) to the $\overline{PGM}$ pin with both $\overline{CE}$ and $\overline{OE}$ set to H causes page write to be executed. Later, setting both $\overline{CE}$ and $\overline{OE}$ to L causes program verification to be executed.

If programming is not completed after one program pulse, the write and verify operations may be repeated X times (where $X \leq 10$).

(6) Byte write mode

Adding a 0.1 ms program pulse (active, low) to the $\overline{PGM}$ pin with setting $\overline{CE}$ to L and $\overline{OE}$ to H causes byte write to be executed. Later, setting $\overline{OE}$ to L causes program verification to be executed.

If programming is not completed after one program pulse, the write and verify operations may be repeated X times (where $X \leq 10$).

(7) Program verify mode

Set $\overline{CE}$ to L, $\overline{PGM}$ to H, and $\overline{OE}$ to L to set program verify mode. Use verify mode for verification following each write operation.

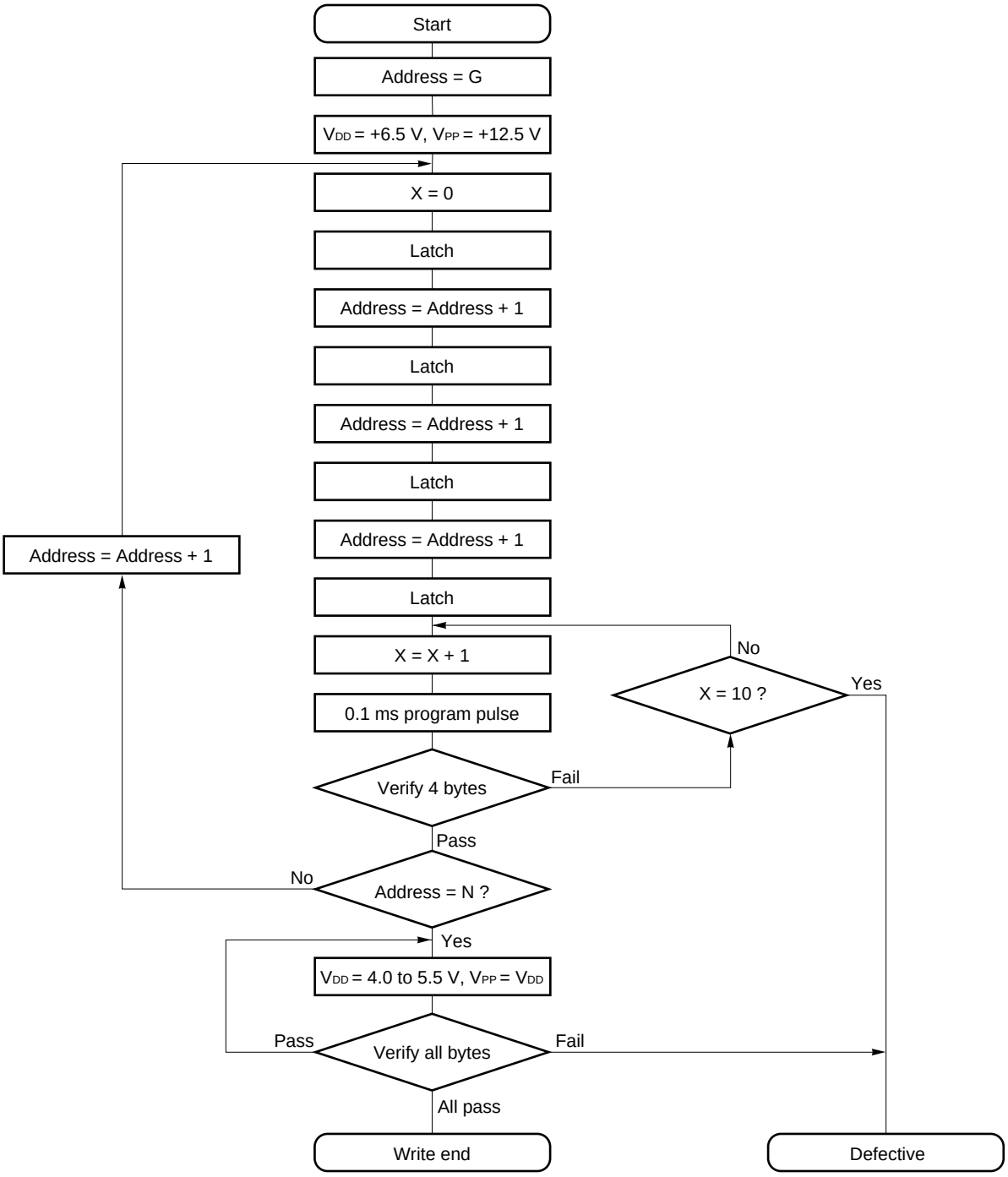
(8) Program inhibit mode

Program inhibit mode is used to write to a single device when several μPD78P4908 devices are connected in parallel to $\overline{OE}$, V_{PP}, and D0 to D7 pins.

Use the page write mode or byte write mode described above for each write operation. Write operations cannot be done for devices in which the $\overline{PGM}$ pin has been set to H.

6.2 PROM WRITE SEQUENCE

Figure 6-1. Page Program Mode Flowchart



Remark G = Start address
N = Program end address

Figure 6-2. Page Program Mode Timing

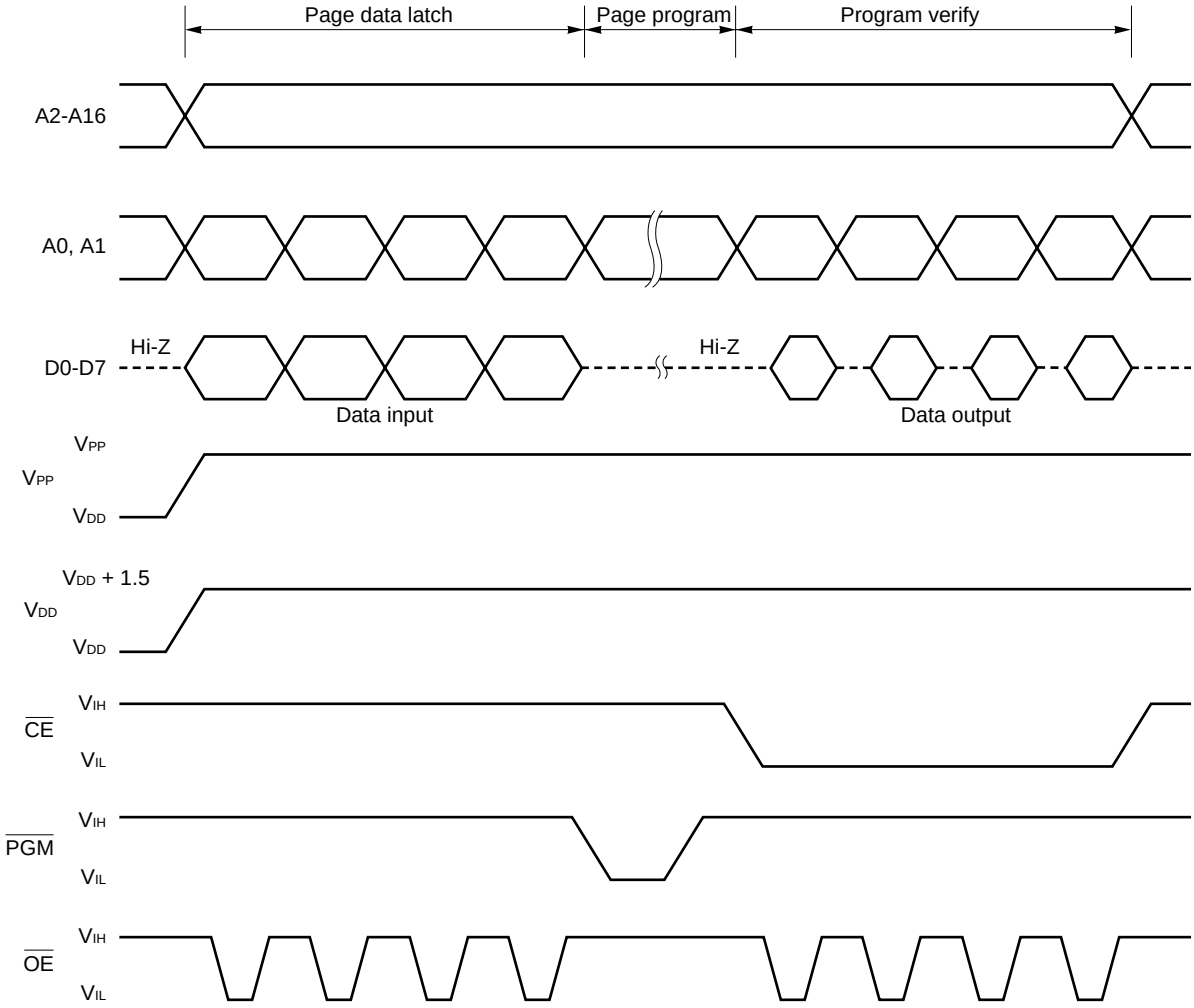
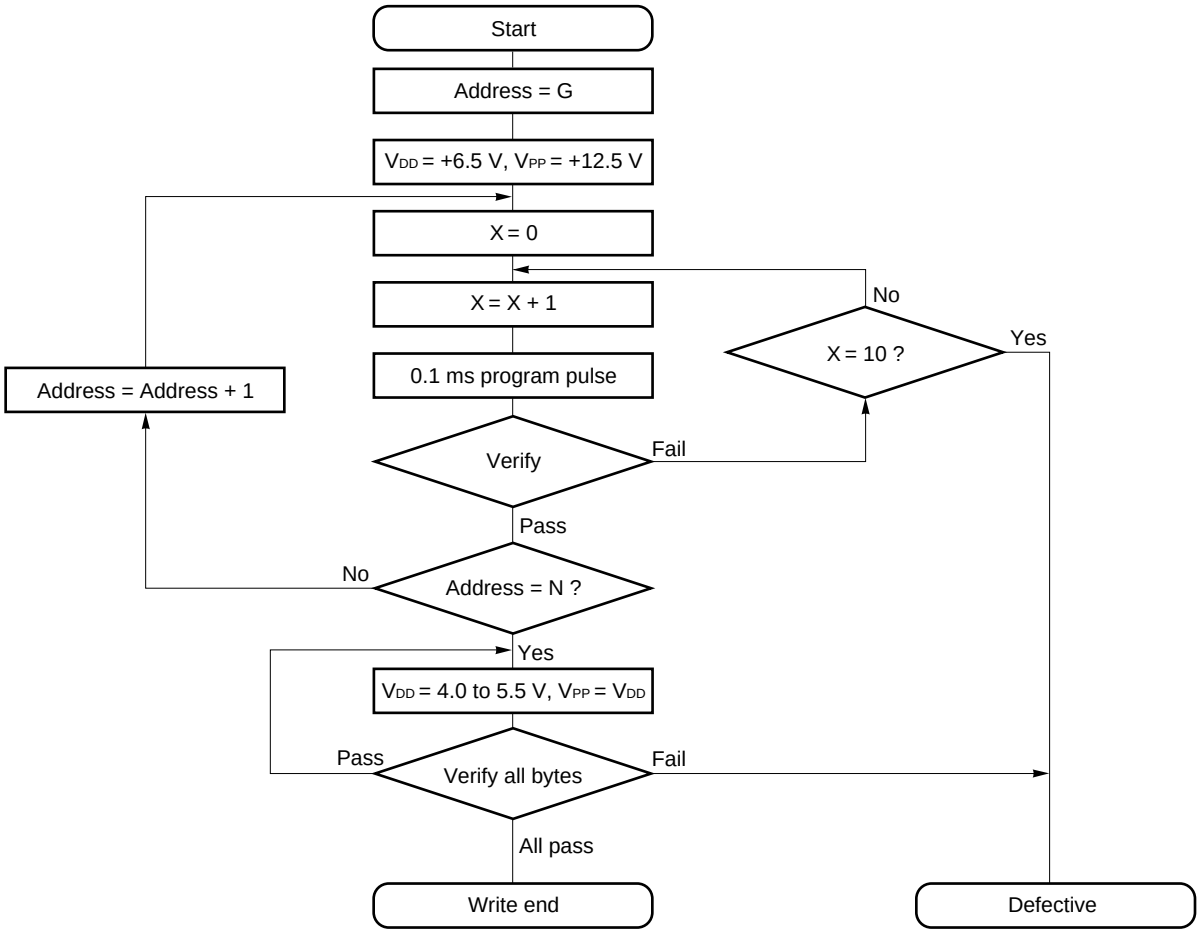
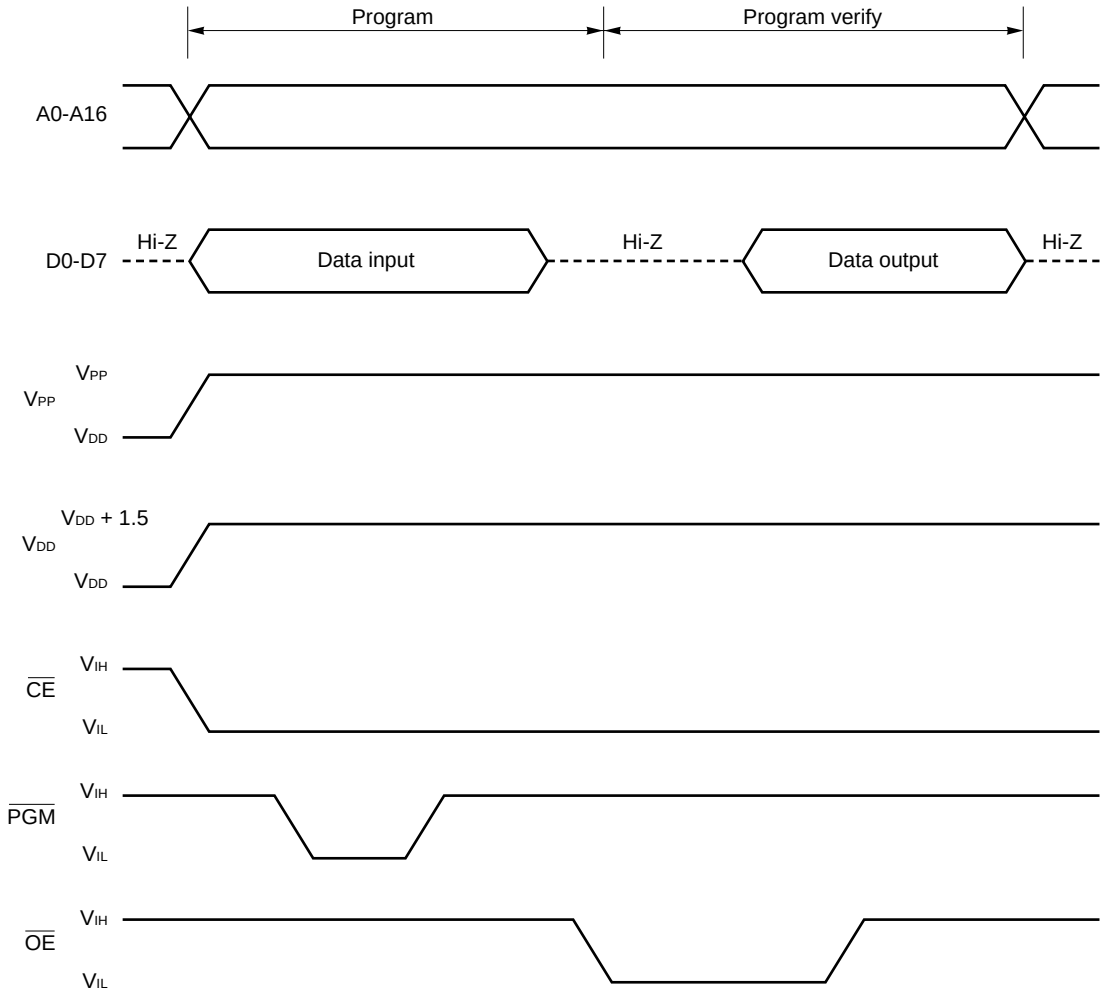


Figure 6-3. Byte Program Mode Flowchart



Remark G = Start address
N = Program end address

Figure 6-4. Byte Program Mode Timing



Cautions 1. Add V_{DD} before V_{PP}, and turn off the V_{DD} after V_{PP}.

2. Do not allow V_{PP} to exceed 13.5 V including overshoot.

3. Reliability problems may result if the device is inserted or pulled out while 12.5 V is applied at V_{PP}.

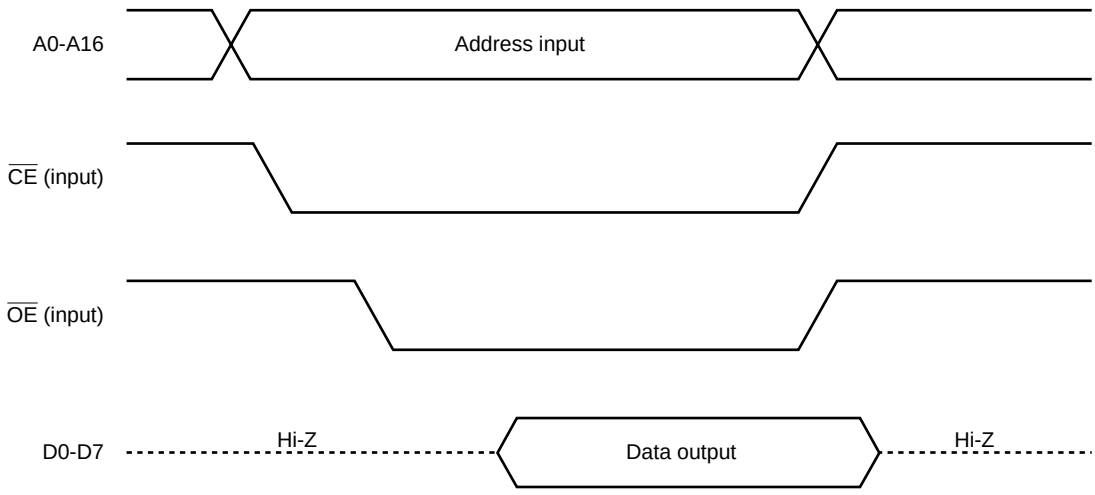
6.3 PROM READ SEQUENCE

Follow this sequence to read the PROM contents to an external data bus (D0 to D7).

(1) Set the $\overline{\text{RESET}}$ pin to low level and add 5 V to the V_{PP} pin. See **2. PIN CONFIGURATION (TOP VIEW) (2) PROM programming mode** with regard to handling of other, unused pins.
(2) Add 5 V to the V_{DD} and V_{PP} pins.
(3) Input the data address to be read to pins A0 to A16.
(4) Set read mode.
(5) Output the data to pins D0 to D7.

Figure 6-5 shows the timing of steps (2) to (5) above.

Figure 6-5. PROM Read Timing



7. SCREENING ONE-TIME PROM PRODUCTS

NEC cannot execute a complete test of one-time PROM products (μPD78P4908GF-3BA) due to their structure before shipment. It is recommended that you screen (verify) PROM products after writing necessary data into them and storing them at 125°C for 24 hours.

8. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}		–0.3 to +7.0	V
	AV_{DD}		–0.3 to V_{DD} + 0.3	V
	AV_{SS}		–0.3 to +0.3	V
Input voltage	V_{I1}	For pins other than V_{PP}, A9	–0.3 to V_{DD} + 0.3	V
	V_{I2}	V_{PP}, A9	–0.3 to +13.5	V
Analog input voltage	V_{AN}		AV_{SS} – 0.3 to AV_{REF1} + 0.3	V
Output voltage	V_O		–0.3 to V_{DD} + 0.3	V
Output low current	I_{OL}	One pin	10	mA
		Total for the P00-P07, P30-P37, P54-P57, P60-P67, and P100-P107 pins	50	mA
		Total for the P10-P17, P40-P47, P50-P53, P70-P77, P90-P97, PWM0, PWM1, and $\overline{TX}$ pins	50	mA
Output high current	I_{OH}	One pin	–6	mA
		Total for the P00-P07, P30-P37, P54-P57, P60-P67, and P100-P107 pins	–30	mA
		Total for the P10-P17, P40-P47, P50-P53, P70-P77, P90-P97, PWM0, PWM1, and $\overline{TX}$ pins	–30	mA
A/D converter reference input voltage	AV_{REF1}		–0.3 to V_{DD} + 0.3	V
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

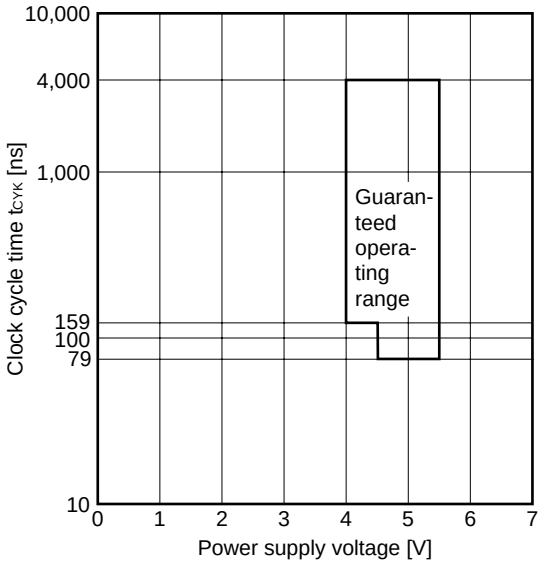
Caution Absolute maximum ratings are rated values beyond which physical damage will be caused to the product; if the rated value of any of the parameters in the above table is exceeded, even momentarily, the quality of the product may deteriorate. Always use the product within its rated values.

Remark Unless otherwise stated, the characteristics of a dual-function pin are the same as those of a port pin.

OPERATING CONDITIONS

- Operating ambient temperature (T_A): –40 °C to +85 °C
- Power supply voltage and clock cycle time: See **Figure 8-1**.
- Internal regulator operation selected (REGOFF pin: low level)

Figure 8-1. Power Supply Voltage and Clock Cycle Time



CAPACITANCE (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz 0 V on pins other than measured pins			15	pF
Output capacitance	C_O				15	pF
I/O capacitance	C_{IO}				15	pF

★ **MAIN OSCILLATOR CHARACTERISTICS (T_A = –40 °C to +85 °C, V_{DD} = 4.0 to 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Oscillator frequency	f_{XX}	Ceramic or crystal resonator	2	12.58	MHz

Caution When using the clock generator, run wires according to the following rules to avoid effects such as stray capacitance:

- **Minimize the wiring length.**
- **Never cause the wires to cross other signal lines.**
- **Never cause the wires to run near a line carrying a large varying current.**
- **The grounding point of the capacitor of the oscillator circuit must always be the same potential as V_{SS1}. Never connect the capacitor to a ground pattern carrying a large current.**
- **Never extract a signal from the oscillator.**

★ **Remark** Connect a 12.582912 or 6.291456 MHz oscillator to operate the internal clock timer with the main clock.

CLOCK OSCILLATOR CHARACTERISTICS (T_A = –40 °C to +85 °C, V_{DD} = 4.0 to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillator frequency	f_{XT}	Ceramic or crystal resonator	32	32.768	35	kHz
Oscillation settling time	t_{SXT}	V_{DD} = 4.5 to 5.5 V		1.2	2	s
					10	s
Oscillation hold voltage	V_{DDXT}		4.0		5.5	V
Watch timer operating voltage	V_{DDW}		4.0		5.5	V

DC CHARACTERISTICS (T_A = –40 °C to +85 °C, V_{DD} = AV_{DD} = 4.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input low voltage**Note 5**	V_{IL1}	For pins other than those described in **Notes 1 and 2**	–0.3		0.3 V_{DD}	V
	V_{IL2}	For pins described in **Note 1**	–0.3		0.2 V_{DD}	V
	V_{IL3}	V_{DD} = 4.5 to 5.5 V For pins described in **Note 2**	–0.3		+0.8	V
Input high voltage	V_{IH1}	For pins other than those described in **Notes 1 and 2**	0.7 V_{DD}		V_{DD} + 0.3	V
	V_{IH2}	For pins described in **Note 1**	0.8 V_{DD}		V_{DD} + 0.3	V
	V_{IH3}	V_{DD} = 4.5 to 5.5 V For pins described in **Note 2**	2.2		V_{DD} + 0.3	V
Output low voltage	V_{OL1}	I_{OL} = 20 μA			0.1	V
		I_{OL} = 100 μA			0.2	V
		I_{OL} = 2 mA			0.4	V
	V_{OL2}	I_{OL} = 8 mA For pins described in **Note 4** V_{DD} = 4.5 to 5.5 V			1.0	V
Output high voltage	V_{OH1}	I_{OH} = -20 μA	V_{DD} – 0.1			V
		I_{OH} = -100 μA	V_{DD} – 0.2			V
		I_{OH} = -2 mA	V_{DD} – 1.0			V
	V_{OH2}	V_{DD} = 4.5 to 5.5 V I_{OH} = -5 mA For pins described in **Note 3**	V_{DD} – 2.4			V

Notes 1. X1, X2, $\overline{\text{RESET}}$, P12/ASCK2/$\overline{\text{SCK2}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK/$\overline{\text{SCK1}}$, P26/INTP5, P27/SI0, P32/$\overline{\text{SCK0}}$, P33/SO0, P105/$\overline{\text{SCK3}}$, P106/SI3, P107/SO3, XT1, XT2

2. P40/AD0-P47/AD7, P50/A8-P57/A15, P60/A16-P67/$\overline{\text{REFRQ}}$/HLDAK, P00-P07

3. P00-P07

4. P10-P17, P40/AD0-P47/AD7, P50/A8-P57/A15

5. Other than pull-up resistors

DC CHARACTERISTICS (T_A = –40 °C to +85 °C, V_{DD} = AV_{DD} = 4.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LI1}	0 V ≤ V_I ≤ V_{DD}	For pins other than X1 and XT1			±10	μA
	I_{LI2}		X1, XT1			±20	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}				±10	μA
V_{DD} supply current**Note**	I_{DD1}	Operation mode	f_{XX} = 12.58 MHz V_{DD} = 4.5 to 5.5 V		20	40	mA
★			f_{XX} = 6.29 MHz V_{DD} = 4.0 to 5.5 V		10	20	mA
	I_{DD2}	HALT mode	f_{XX} = 12.58 MHz V_{DD} = 4.5 to 5.5 V f_{CLK} = f_{XX}/8 (STBC = B1H) Peripheral operation stops.		5.2	10.4	mA
★			f_{XX} = 6.29 MHz V_{DD} = 4.0 to 5.5 V f_{CLK} = f_{XX}/8 (STBC = 31H) Peripheral operation stops.		2.6	5.2	mA
	I_{DD3}	IDLE mode	f_{XX} = 12.58 MHz V_{DD} = 4.5 to 5.5 V		2.4	4.8	mA
★			f_{XX} = 6.29 MHz V_{DD} = 4.0 to 5.5 V		1.8	3.6	mA
Pull-up resistor	R_L	V_I = 0 V		15		80	kΩ

Note These values are valid when the internal regulator is ON (REGOFF pin = low level). They do not include the AV_{DD} and AV_{REF1} currents.

AC CHARACTERISTICS (T_A = –40°C to +85°C, V_{DD} = AV_{DD} = 4.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

(1) Read/write operation

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Address setup time (to ASTB↓)	t_{SAST}	V_{DD} = 5.0 V	(0.5 + a)T – 11	29		ns
ASTB high-level width	t_{WSTH}	V_{DD} = 5.0 V	(0.5 + a)T – 17	23		ns
Address hold time (to ASTB↓)	t_{HSTLA}	V_{DD} = 5.0 V	0.5T – 19	21		ns
Address hold time (to $\overline{RD}$↑)	t_{HRA}	V_{DD} = 5.0 V	0.5T – 14	26		ns
Delay from address to $\overline{RD}$↓	t_{DAR}	V_{DD} = 5.0 V	(1 + a)T – 5	74		ns
Address float time (to $\overline{RD}$↓)	t_{FRA}			0		ns
Delay from address to data input	t_{DAID}	V_{DD} = 5.0 V	(2.5 + a + n)T – 37		400	ns
Delay from ASTB↓ to data input	t_{DSTID}	V_{DD} = 5.0 V	(2 + n)T – 35		283	ns
Delay from $\overline{RD}$↓ to data input	t_{DRID}	V_{DD} = 5.0 V	(1.5 + n)T – 40		238	ns
Delay from ASTB↓ to $\overline{RD}$↓	t_{DSTR}	V_{DD} = 5.0 V	0.5T – 9	31		ns
Data hold time (to $\overline{RD}$↑)	t_{HRID}			0		ns
Delay from $\overline{RD}$↑ to address active	t_{DRA}	V_{DD} = 5.0 V	0.5T – 2	38		ns
Delay from $\overline{RD}$↑ to ASTB↑	t_{DRST}	V_{DD} = 5.0 V	0.5T – 9	31		ns
$\overline{RD}$ low-level width	t_{WRL}	V_{DD} = 5.0 V	(1.5 + n)T – 25	94		ns
Delay from address↓ to $\overline{WR}$↓	t_{DAW}	V_{DD} = 5.0 V	(1 + a)T – 5	74		ns
Address hold time (to $\overline{WR}$↑)	t_{HWA}	V_{DD} = 5.0 V	0.5T – 14	26		ns
Delay from ASTB↓ to data output	t_{DSTOD}	V_{DD} = 5.0 V	0.5T + 15		55	ns
Delay from $\overline{WR}$↓ to data output	t_{DWOD}				15	ns
Delay from ASTB↓ to $\overline{WR}$↓	t_{DSTW}	V_{DD} = 5.0 V	0.5T – 9	31		ns
Data setup time (to $\overline{WR}$↑)	t_{SODWR}	V_{DD} = 5.0 V	(1.5 + n)T – 20	99		ns
Data hold time (to $\overline{WR}$↑)	t_{HWOD}	V_{DD} = 5.0 V	0.5T – 14	26		ns
Delay from $\overline{WR}$↑ to ASTB↑	t_{DWST}	V_{DD} = 5.0 V	0.5T – 9	31		ns
$\overline{WR}$ low-level width	t_{WWL}	V_{DD} = 5.0 V	(1.5 + n)T – 25	94		ns

Remark T: t_{CYK} (system clock cycle time) V_{DD} = 5.0 V T = 79 ns (MIN.)
a: 1 during address wait, otherwise, 0
n: Number of wait states ($n \geq 0$)

(2) External wait timing

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Delay from address to $\overline{WAIT}$↓ input	t_{DAWT}	V_{DD} = 5.0 V	(2 + a)T – 40		198	ns
Delay from ASTB↓ to $\overline{WAIT}$↓ input	t_{DSTWT}	V_{DD} = 5.0 V	1.5T – 40		79	ns
Hold time from ASTB↓ to $\overline{WAIT}$	t_{HSTWT}	V_{DD} = 5.0 V	(0.5 + n)T + 5	124		ns
Delay from ASTB↓ to $\overline{WAIT}$↑	t_{DSTWTH}	V_{DD} = 5.0 V	(1.5 + n)T – 40		238	ns
Delay from $\overline{RD}$↓ to $\overline{WAIT}$↓ input	t_{DRWTL}	V_{DD} = 5.0 V	T – 40		39	ns
Hold time from $\overline{RD}$↓ to $\overline{WAIT}$	t_{HRWT}	V_{DD} = 5.0 V	nT + 5	84		ns
Delay from $\overline{RD}$↓ to $\overline{WAIT}$↑	t_{DRWTH}	V_{DD} = 5.0 V	(1 + n)T – 40		198	ns
Delay from $\overline{WAIT}$↑ to data input	t_{DWTID}	V_{DD} = 5.0 V	0.5T – 5		35	ns
Delay from $\overline{WAIT}$↑ to $\overline{RD}$↑	t_{DWTR}	V_{DD} = 5.0 V	0.5T	40		ns
Delay from $\overline{WAIT}$↑ to $\overline{WR}$↑	t_{DWTW}	V_{DD} = 5.0 V	0.5T	40		ns
Delay from $\overline{WR}$↓ to $\overline{WAIT}$↓ input	t_{DWWTL}	V_{DD} = 5.0 V	T – 40		39	ns
Hold time from $\overline{WR}$↓ to $\overline{WAIT}$	t_{HWWT}	V_{DD} = 5.0 V	nT + 5	84		ns
Delay from $\overline{WR}$↓ to $\overline{WAIT}$↑	t_{DWWTH}	V_{DD} = 5.0 V	(1 + n)T – 40		198	ns

Remark T: t_{CYK} (system clock cycle time) V_{DD} = 5.0 V T = 79 ns (MIN.)
a: 1 during address wait, otherwise, 0
n: Number of wait states ($n \geq 0$)

(3) Bus hold timing

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Delay from HLDRQ↑ to float	t_{FHQC}	V_{DD} = 5.0 V	(2 + 4 + a + n)T + 50		765	ns
Delay from HLDRQ↑ to HLDAK↑	$t_{DHQHHAH}$	V_{DD} = 5.0 V	(3 + 4 + a + n)T + 30		825	ns
Delay from float to HLDAK↑	t_{DCFHA}	V_{DD} = 5.0 V	T + 30		109	ns
Delay from HLDRQ↓ to HLDAK↓	$t_{DHQLHAL}$	V_{DD} = 5.0 V	2T + 40		199	ns
Delay from HLDRQ↓ to active	t_{DHAC}	V_{DD} = 5.0 V	T – 20	59		ns

Remark T: t_{CYK} (system clock cycle time) V_{DD} = 5.0 V T = 79 ns (MIN.)
a: 1 during address wait, otherwise, 0
n: Number of wait states (n ≥ 0)

(4) Refresh timing

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Random read/write cycle time	t_{RC}	V_{DD} = 5.0 V	3T	238		ns
$\overline{REFRQ}$ low-level pulse width	t_{WRFQL}	V_{DD} = 5.0 V	1.5T – 25	94		ns
Delay from ASTB↓ to $\overline{REFRQ}$	t_{DSTRFQ}	V_{DD} = 5.0 V	0.5T – 9	31		ns
Delay from $\overline{RD}$↑ to $\overline{REFRQ}$	t_{DRRFQ}	V_{DD} = 5.0 V	1.5T – 9	110		ns
Delay from $\overline{WR}$↑ to $\overline{REFRQ}$	t_{DWRFQ}	V_{DD} = 5.0 V	1.5T – 9	110		ns
Delay from $\overline{REFRQ}$↑ to ASTB	t_{DRFQST}	V_{DD} = 5.0 V	0.5T – 9	31		ns
$\overline{REFRQ}$ high-level pulse width	t_{WRFQH}	V_{DD} = 5.0 V	1.5T – 25	94		ns

Remark T: t_{CYK} (system clock cycle time) V_{DD} = 5.0 V T = 79 ns (MIN.)

SERIAL OPERATION (T_A = –40 °C to +85 °C, V_{DD} = 4.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

(1) CSI, CSI3

Parameter	Symbol	Conditions			MIN.	MAX.	Unit
Serial clock cycle time ($\overline{SCK0}$, $\overline{SCK3}$)	t_{CYSK0}	Input	f_{CLK} = f_{XX}		8/f_{XX}		ns
			Other than f_{CLK} = f_{XX}		4/f_{CLK}		ns
		Output	Other than f_{CLK} = f_{XX}/8		8/f_{XX}		ns
			f_{CLK} = f_{XX}/8		16/f_{XX}		ns
Serial clock low-level width ($\overline{SCK0}$, $\overline{SCK3}$)	t_{WSKL0}	Input	f_{CLK} = f_{XX}		4/f_{XX} – 40		ns
			Other than f_{CLK} = f_{XX}		2/f_{CLK} – 40		
		Output	Other than f_{CLK} = f_{XX}/8		4/f_{XX} – 40		μs
			f_{CLK} = f_{XX}/8		8/f_{XX} – 40		
Serial clock high-level width ($\overline{SCK0}$, $\overline{SCK3}$)	t_{WSKH0}	Input	f_{CLK} = f_{XX}		4/f_{XX} – 40		ns
			Other than f_{CLK} = f_{XX}		2/f_{CLK} – 40		
		Output	Other than f_{CLK} = f_{XX}/8		4/f_{XX} – 40		μs
			f_{CLK} = f_{XX}/8		8/f_{XX} – 40		
Setup time for SI0, SI3 (to $\overline{SCK0}$, $\overline{SCK3}$↑)	t_{SSSK0}				80		ns
Hold time for SI0, SI3 (to $\overline{SCK0}$, $\overline{SCK3}$↑)	t_{HSSK0}	External clock			1/f_{CLK} + 80		ns
		Internal clock			80		
Output delay time for SO0, SO3 (to $\overline{SCK0}$, $\overline{SCK3}$↓)	t_{DSBSK1}	CMOS push-pull output		External clock	0	1/f_{CLK} + 150	ns
				Internal clock	0	150	ns
	t_{DSBSK2}	Open-drain output R_L = 1 kΩ		External clock	0	1/f_{CLK} + 400	ns
				Internal clock	0	400	ns
Output hold time for SO0, SO3 (to $\overline{SCK0}$, $\overline{SCK3}$↑)	t_{HSBSK}	When data is transferred			0.5t_{CYSK0} – 40		ns

Remarks 1. The values in this table are those when f_{XX} = 12.58 MHz, C_L is 100 pF.

2. f_{CLK}: System clock frequency (selectable from f_{XX}, f_{XX}/2, f_{XX}/4, and f_{XX}/8 by the standby control register (STBC))

★ **3.** f_{XX} : Oscillation frequency (f_{XX} = 12.58 MHz or f_{XX} = 6.29 MHz)

(2) IOE1, IOE2 (T_A = –40 °C to +85 °C, V_{DD} = AV_{DD} = 4.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Serial clock cycle time ($\overline{SCK1}$, $\overline{SCK2}$)	t_{CYSK1}	Input	V_{DD} = 4.5 to 5.5 V	640		ns
				1,280		ns
		Output	Internal, divided by 8	T		ns
Serial clock low-level width ($\overline{SCK1}$, $\overline{SCK2}$)	t_{WSKL1}	Input	V_{DD} = 4.5 to 5.5 V	280		ns
				600		ns
		Output	Internal, divided by 8	0.5T – 40		ns
Serial clock high-level width ($\overline{SCK1}$, $\overline{SCK2}$)	t_{WSKH1}	Input	V_{DD} = 4.5 to 5.5 V	280		ns
				600		ns
		Output	Internal, divided by 8	0.5T – 40		ns
Setup time for SI1 and SI2 (to $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{SSSK1}			40		ns
Hold time for SI1 and SI2 (to $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{HSSK1}			40		ns
Output delay time for SO1 and SO2 (to $\overline{SCK1}$, $\overline{SCK2}$↓)	t_{DSOSK}			0	50	ns
Output hold time for SO1 and SO2 (to $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{HSOSK}	When data is transferred		$0.5t_{CYSK1}$ – 40		ns

Remarks 1. The values in this table are those when C_L is 100 pF.

2. T: Serial clock cycle set by software. The minimum value is $8/f_{XX}$.

(3) UART, UART2 (T_A = –40 °C to +85 °C, V_{DD} = AV_{DD} = 4.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASCK clock input cycle time	t_{CYASK}	V_{DD} = 4.5 to 5.5 V	160		ns
			320		ns
ASCK clock low-level width	t_{WASKL}	V_{DD} = 4.5 to 5.5 V	65		ns
			120		ns
ASCK clock high-level width	t_{WASKH}	V_{DD} = 4.5 to 5.5 V	65		ns
			120		ns

CLOCK OUTPUT OPERATION (T_A = –40°C to +85°C, V_{DD} = AV_{DD} = 4.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
CLKOUT cycle time	t_{CYCL}	nT	79	32,000	ns
CLKOUT low-level width	t_{CLL}	V_{DD} = 4.5 to 5.5 V, 0.5T – 10	30		ns
		0.5T – 20	20		ns
CLKOUT high-level width	t_{CLH}	V_{DD} = 4.5 to 5.5 V, 0.5T – 10	30		ns
		0.5T – 20	20		ns
★ CLKOUT rise time	t_{CLR}	4.5 V ≤ V_{DD} < 5.5 V		10	ns
		4.0 V ≤ V_{DD} < 4.5 V		20	ns
★ CLKOUT fall time	t_{CLF}	4.5 V ≤ V_{DD} < 5.5 V		10	ns
		4.0 V ≤ V_{DD} < 4.5 V		20	ns

Remark n: Dividing ratio set by software in the CPU (n = 1, 2, 4, 8, and 16)
T: t_{CYK} (system clock cycle time)

OTHER OPERATIONS (T_A = –40 °C to +85 °C, V_{DD} = AV_{DD} = 4.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
NMI low-level width	t_{WNIL}		10		μs
NMI high-level width	t_{WNIH}		10		μs
INTP0 low-level width	t_{WIT0L}		4 t_{CYSMP}		ns
INTP0 high-level width	t_{WIT0H}		4 t_{CYSMP}		ns
Low-level width for INTP1-INTP3 and CI	t_{WIT1L}		4 t_{CYCPU}		ns
High-level width for INTP1-INTP3 and CI	t_{WIT1H}		4 t_{CYCPU}		ns
Low-level width for INTP4 and INTP5	t_{WIT2L}		10		μs
High-level width for INTP4 and INTP5	t_{WIT2H}		10		μs
$\overline{\text{RESET}}$ low-level width**Note**	t_{WRSL}		10		μs
$\overline{\text{RESET}}$ high-level width	t_{WRSH}		10		μs

Note Use the $\overline{\text{RESET}}$ low-level width to ensure the lapse of the oscillation settling time when the power is applied.

Remark t_{CYSMP}: Sampling clock set by software
t_{CYCPU}: CPU operation clock set by software in the CPU

A/D CONVERTER CHARACTERISTICS (T_A = –40 °C to +85 °C, V_{DD} = AV_{DD} = AV_{REF1} = 4.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution				8			bit
Total error[Note]		IEAD = 00H	FR = 0			0.6	%
			FR = 1			1.5	%
		IEAD = 01H	V_{DD} = 4.5 to 5.5 V		1	2.2	%
Quantization error						±1/2	LSB
Conversion time	t_{CONV}	FR = 1 120/f_{CLK}		9.5		480	μs
		FR = 0 240/f_{CLK}		19.1		960	μs
Sampling time	t_{SAMP}	FR = 1 18/f_{CLK}		1.4		72	μs
		FR = 0 36/f_{CLK}		2.9		144	μs
Analog input impedance	R_{AN}				1,000		MΩ
AV_{REF1} impedance	R_{REF1}			3	10		kΩ
AV_{DD} power supply voltage	AI_{DD1}	CS = 1			2.0	5.0	mA
	AI_{DD2}	CS = 0, STOP mode			1.0	20	μA

Note Quantization error is not included. This parameter is indicated as the ratio to the full-scale value.

Caution To execute the conversion by the A/D converter set port 7, multiplexed with the A/D input lines, to output mode to prevent data from being inverted.

Remark f_{CLK}: System clock frequency (selectable from f_{XX}, f_{XX}/2, f_{XX}/4, and f_{XX}/8 by the standby control register (STBC))

IEBus CONTROLLER CHARACTERISTICS (T_A = –40°C to +85°C, V_{DD} = AV_{DD} = AV_{REF1} = 4.5 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IEBus standard frequency[Note 1]	f_S	Transfer speed: mode 1	6.20	6.29	6.39	MHz
Driver delay time (delay from $\overline{TX}$ output to bus line)[Note 2]	t_{DTX}	C_L = 50 pF[Note 3]			1.5	μs
Receiver delay time (delay from bus line to $\overline{RX}$ output)[Note 2]	t_{DRX}				0.7	μs
Transmission delay on bus[Note 2]	t_{DBUS}				0.85	μs

Notes 1. The value conforms to the IEBus standard. The IEBus controller is operable within the range of the oscillator frequency of oscillator characteristics.

2. The value is measured when IEBus system clock: f_X = 6.29 MHz.

3. C_L is the load capacitance of $\overline{TX}$ output line.

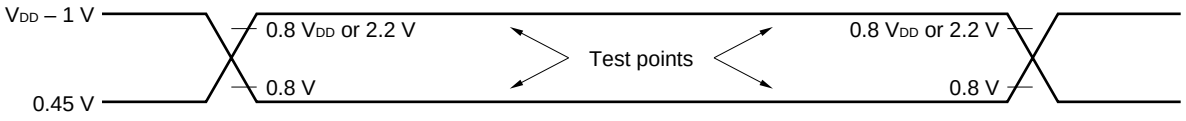
DATA RETENTION CHARACTERISTICS (T_A = –40 °C to +85 °C)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode		2.5		5.5	V
Data retention current	I_{DDDR}	STOP mode	V_{DDDR} = 2.5 V, AV_{REF} = 0 V **Note 1**		2	10	μA
★			V_{DDDR} = 4.0 to 5.5 V, AV_{REF1} = 0 V **Note 1**		10	50	μA
V_{DD} rise time	t_{RVD}			200			μs
V_{DD} fall time	t_{FVD}			200			μs
V_{DD} hold time (to STOP mode setting)	t_{HVD}			0			ms
STOP clear signal input time	t_{DREL}			0			ms
Oscillation settling time	t_{WAIT}	Crystal resonator		30			ms
		Ceramic resonator		5		0.1 V_{DDDR}	ms
Input low voltage	V_{IL}	Specific pins **Note 2**		0		V_{DDDR}	V
Input high voltage	V_{IH}			0.9 V_{DDDR}			V

Notes 1. Valid when input voltages to the pins described in Note 2 satisfy V_{IL} or V_{IH} in the above table.

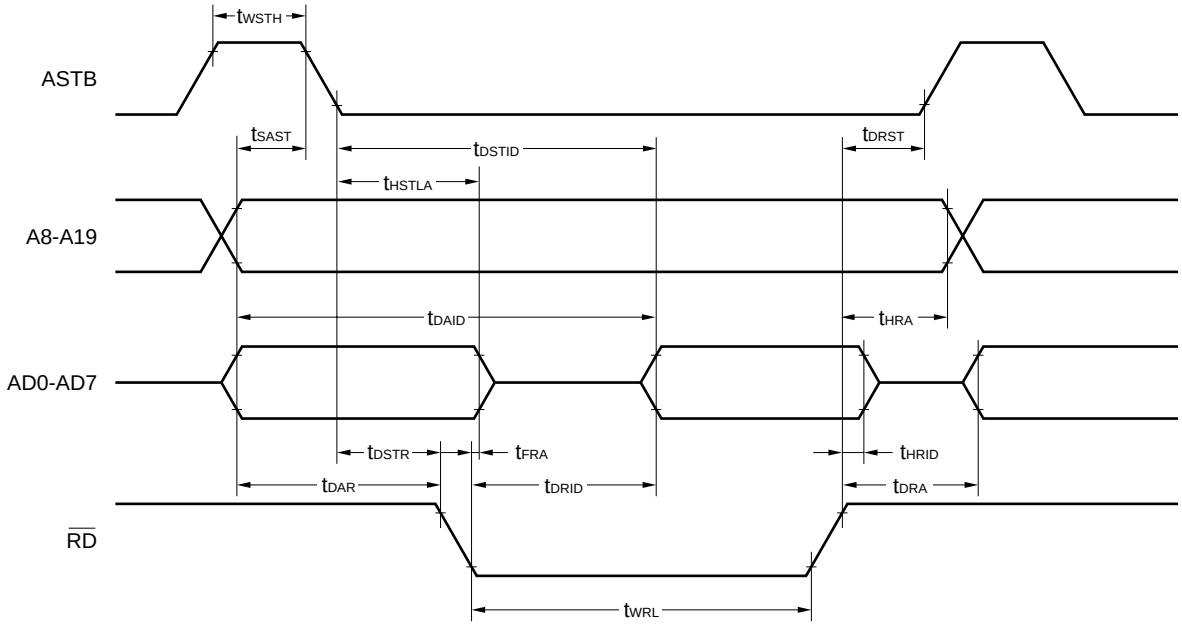
2. $\overline{\text{RESET}}$, P12/ASCK2/$\overline{\text{SCK2}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK/$\overline{\text{SCK1}}$, P26/INTP5, P27/SI0, P32/$\overline{\text{SCK0}}$, P33/SO0, P105/$\overline{\text{SCK3}}$, P106/SI3, and P107/SO3 pins

AC TIMING TEST POINTS

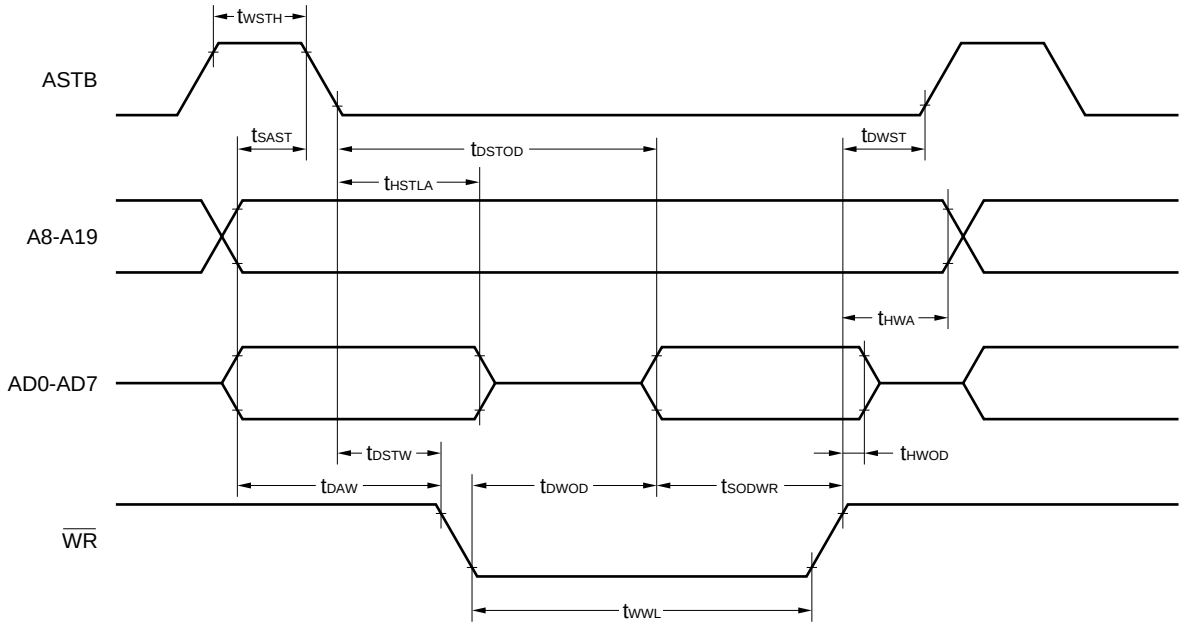


TIMING WAVEFORM

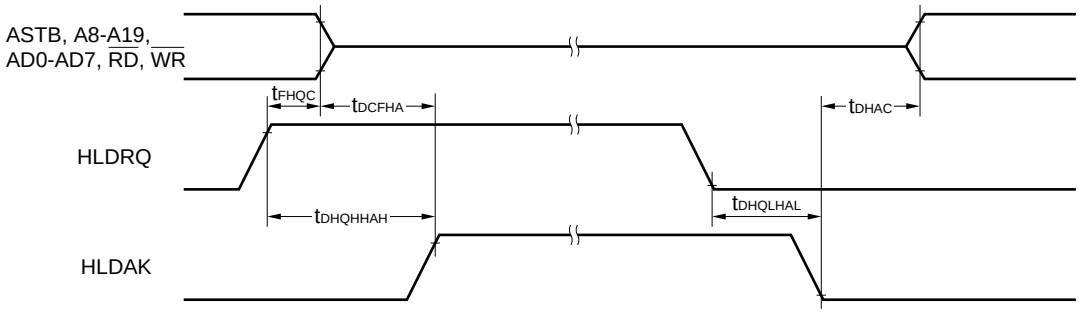
(1) Read operation



(2) Write operation

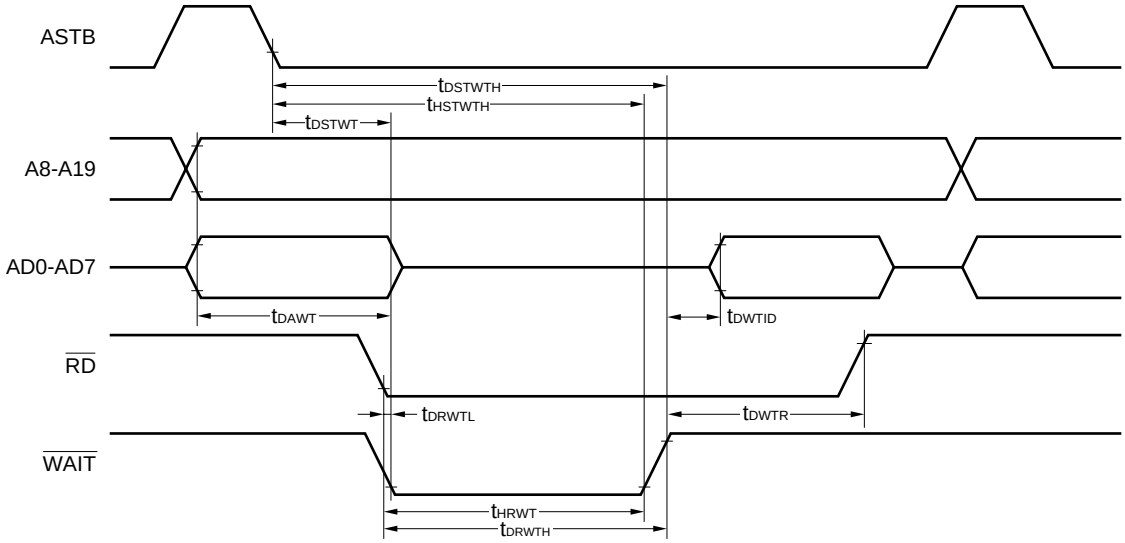


HOLD TIMING

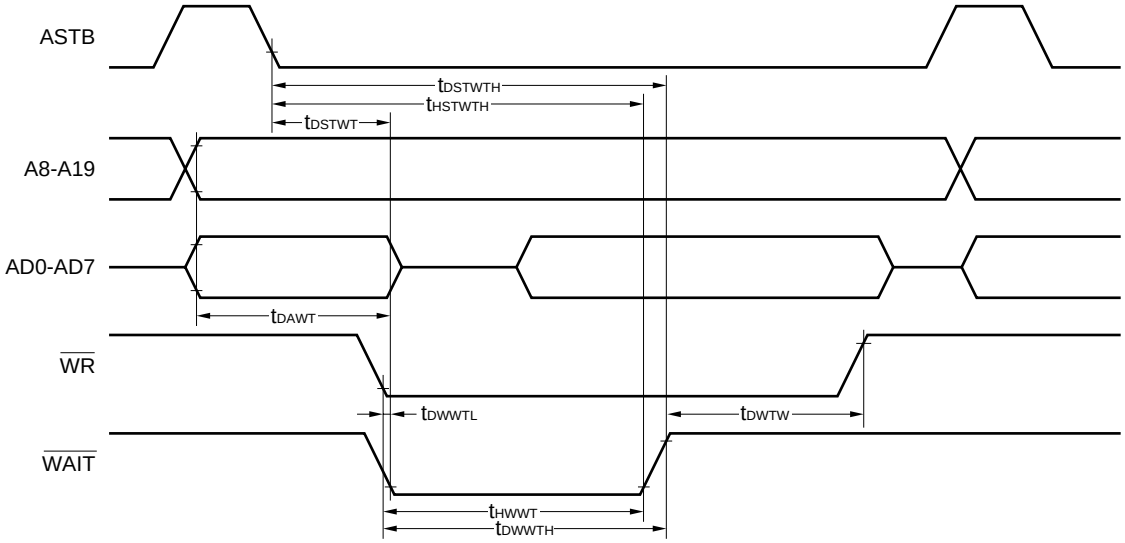


EXTERNAL WAIT SIGNAL INPUT TIMING

(1) Read operation

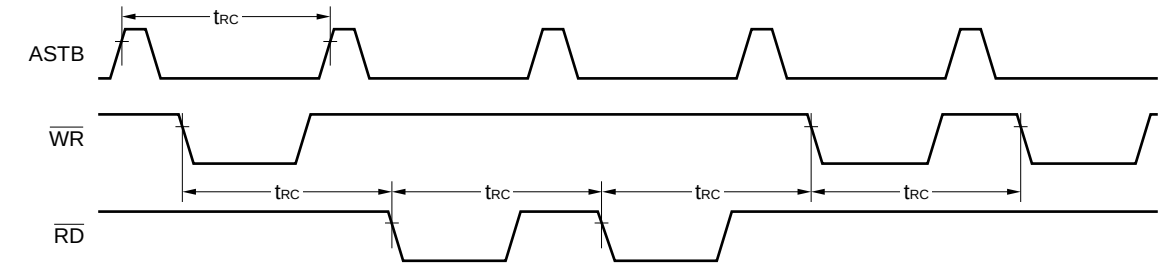


(2) Write operation

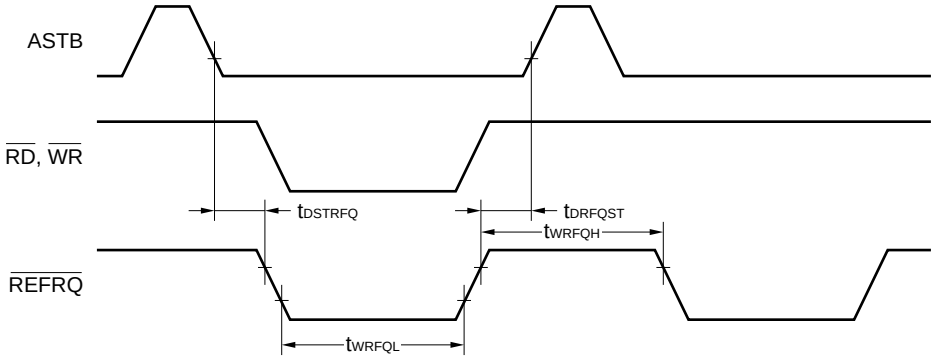


REFRESH TIMING WAVEFORM

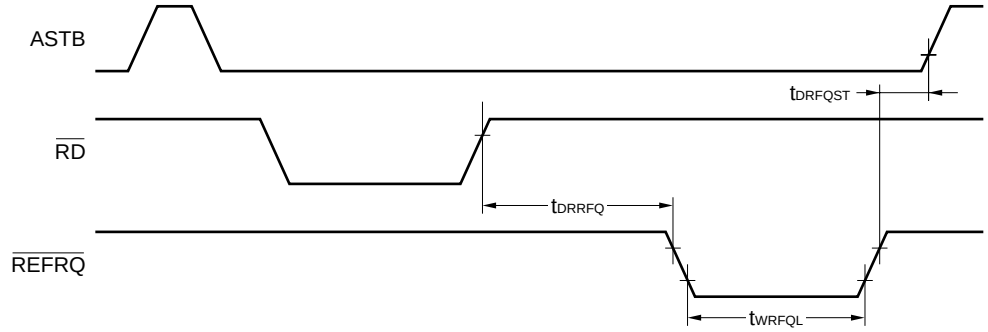
(1) Random read/write cycle



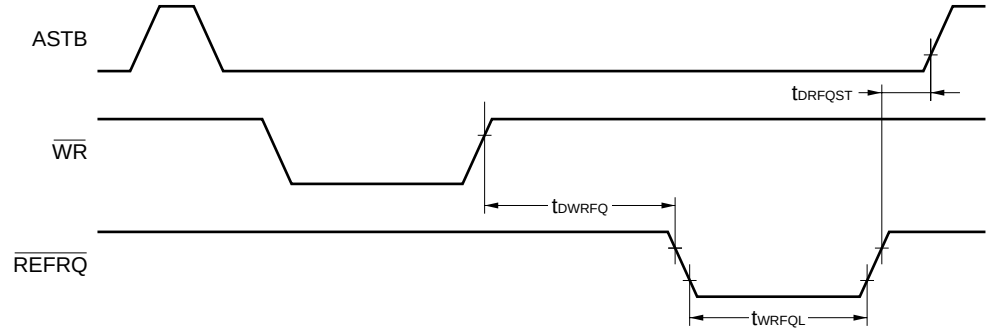
(2) When refresh memory is accessed for a read and write at the same time



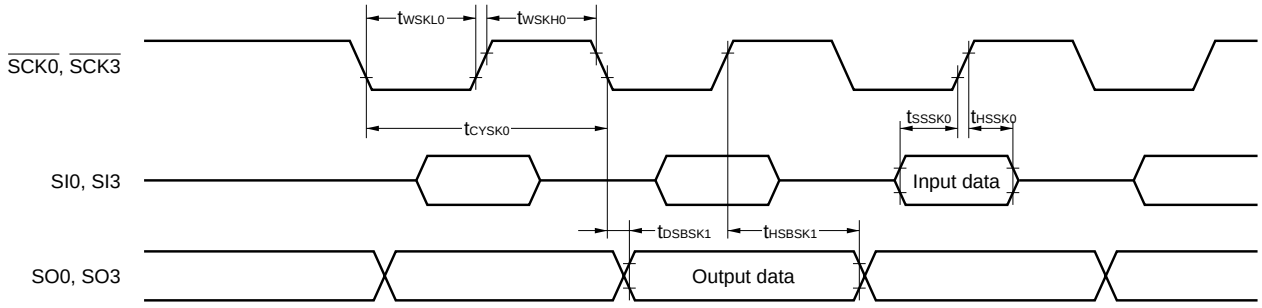
(3) Refresh after a read



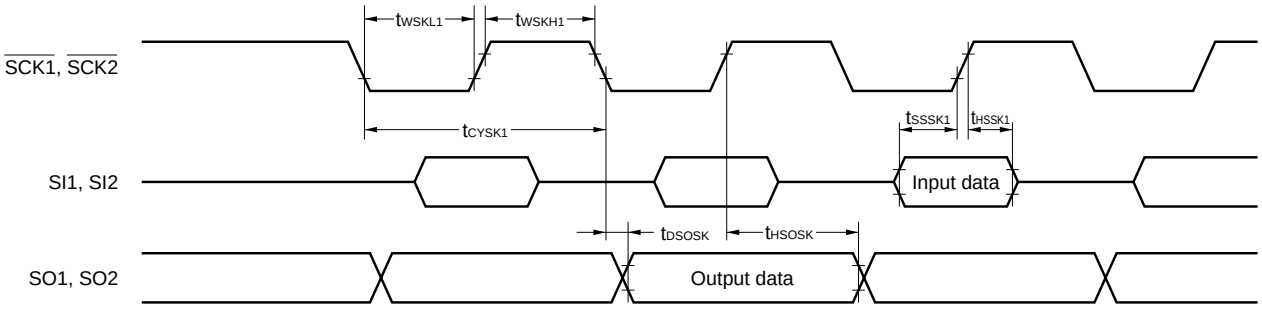
(4) Refresh after a write



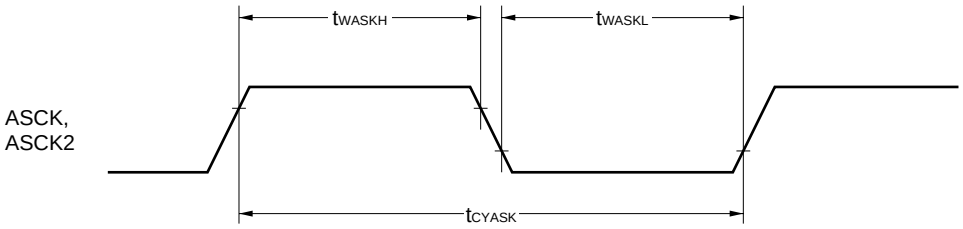
SERIAL OPERATION (CSI, CSI3)



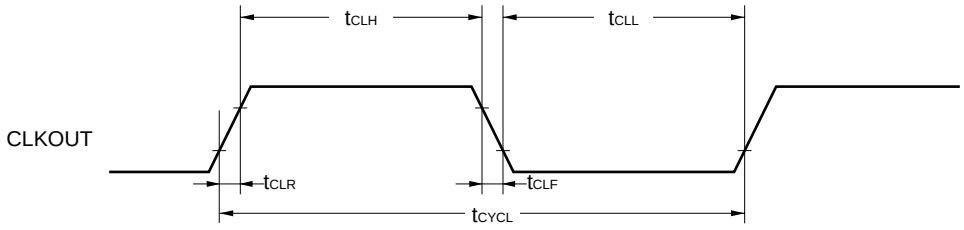
SERIAL OPERATION (IOE1, IOE2)



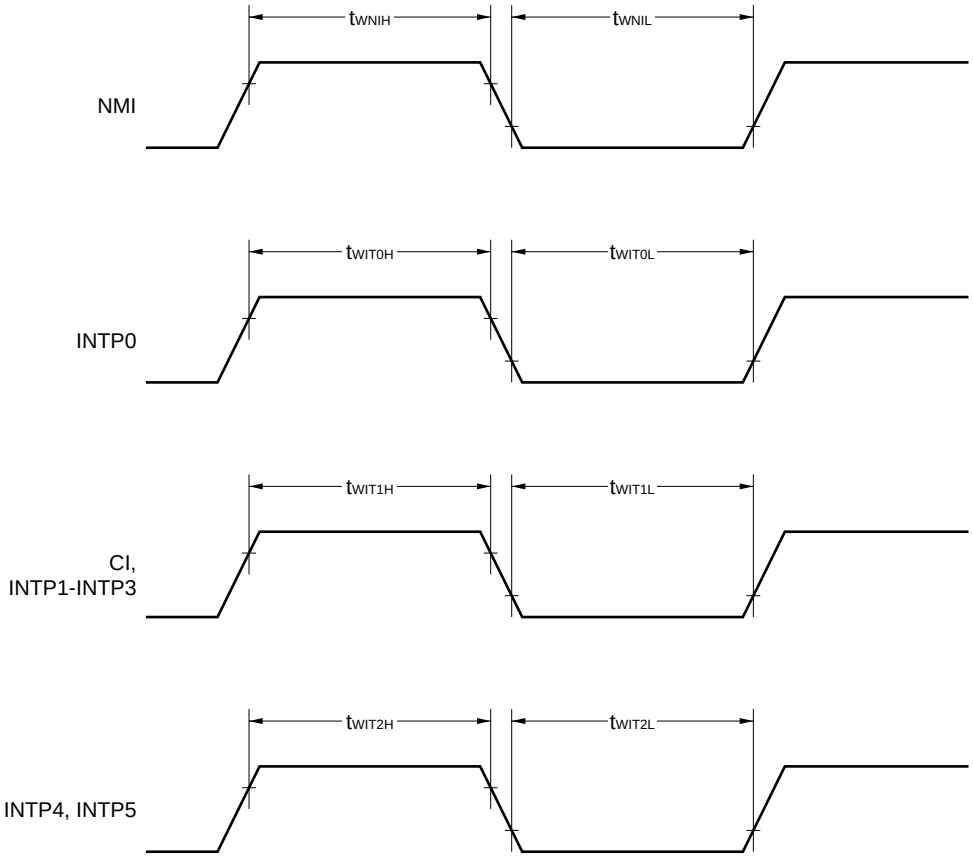
SERIAL OPERATION (UART, UART2)



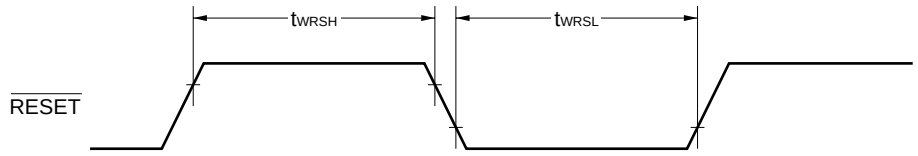
CLOCK OUTPUT TIMING



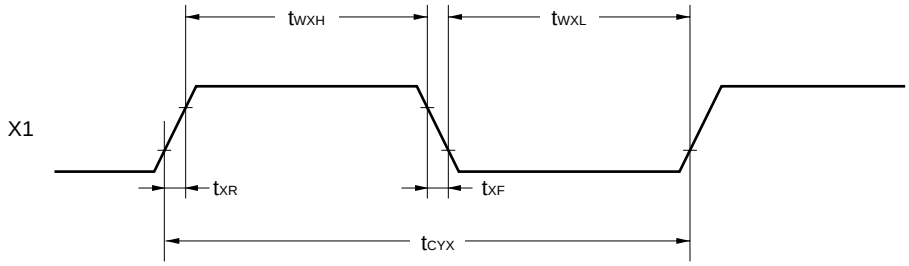
INTERRUPT REQUEST INPUT TIMING



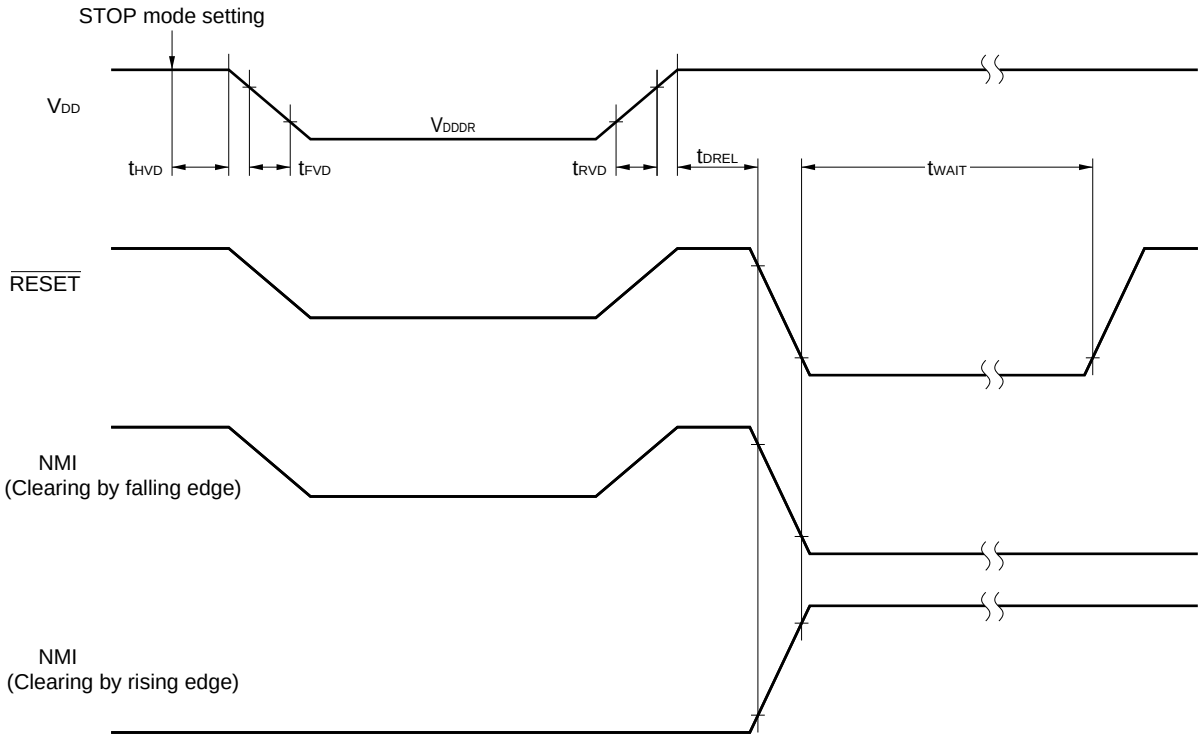
RESET INPUT TIMING



EXTERNAL CLOCK TIMING



DATA RETENTION CHARACTERISTICS



DC PROGRAMMING CHARACTERISTICS (T_A = 25°C ±5°C, V_{SS} = 0 V)

Parameter	Symbol	Symbol[Note 1]	Conditions	MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH}	V_{IH}		2.2		V_{DDP} + 0.3	V
Low-level input voltage	V_{IL}	V_{IL}		–0.3		+0.8	V
Input leakage current	I_{LIP}	I_{LI}	$0 \le V_I \le V_{DDP}$[Note 2]			±10	μA
High-level output voltage	V_{OH}	V_{OH}	I_{OH} = –400 μA	2.4			V
Low-level output voltage	V_{OL}	V_{OL}	I_{OL} = 2.1 mA			0.45	V
Output leakage current	I_{LO}	–	$0 \le V_O \le V_{DDP}$, $\overline{OE}$ = V_{IH}			±10	μA
V_{DDP} supply voltage	V_{DDP}	V_{CC}	Program memory write mode	6.25	6.5	6.75	V
			Program memory read mode	4.5	5.0	5.5	V
V_{PP} supply voltage	V_{PP}	V_{PP}	Program memory write mode	12.2	12.5	12.8	V
			Program memory read mode	V_{PP} = V_{DDP}			V
V_{DDP} supply current	I_{DD}	I_{DD}	Program memory write mode		10	40	mA
			Program memory read mode		10	40	mA
V_{PP} supply current	I_{PP}	I_{PP}	Program memory write mode		5	50	mA
			Program memory read mode		1.0	100	μA

Notes 1. Symbols for the corresponding μPD27C1001A

2. The V_{DDP} represents the V_{DD} pin as viewed in the programming mode.

AC PROGRAMMING CHARACTERISTICS (T_A = 25°C ±5°C, V_{SS} = 0 V)

PROM Write Mode (Page Program Mode)

Parameter	Symbol[Note 1]	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time	t_{AS}		2			μs
$\overline{CE}$ set time	t_{CES}		2			μs
Input data setup time	t_{DS}		2			μs
Address hold time	t_{AH}		2			μs
	t_{AHL}		2			μs
	t_{AHV}		0			μs
Input data hold time	t_{DH}		2			μs
Output data hold time	t_{DF}		0		130	ns
V_{PP} setup time	t_{VPS}		2			μs
V_{DDP} setup time	t_{VDS}[Note 2]		2			μs
Initial program pulse width	t_{PW}		0.095	0.1	0.105	ms
$\overline{OE}$ set time	t_{OES}		2			μs
Valid data delay time from $\overline{OE}$	t_{OE}			1	2	ns
$\overline{OE}$ pulse width in the data latch	t_{LW}		1			μs
$\overline{PGM}$ setup time	t_{PGMS}		2			μs
$\overline{CE}$ hold time	t_{CEH}		2			μs
$\overline{OE}$ hold time	t_{OEH}		2			μs

Notes 1. These symbols (except t_{VDS}) correspond to those of the corresponding μPD27C1001A.

2. For μPD27C1001A, read t_{VDS} as t_{VCS}.

PROM Write Mode (Byte Program Mode)

Parameter	Symbol[Note 1]	Conditions	MIN.	TYP.	MAX.	Unit
Address setup time	t_{AS}		2			μs
$\overline{CE}$ set time	t_{CES}		2			μs
Input data setup time	t_{DS}		2			μs
Address hold time	t_{AH}		2			μs
Input data hold time	t_{DH}		2			μs
Output data hold time	t_{DF}		0		130	ns
V_{PP} setup time	t_{VPS}		2			μs
V_{DDP} setup time	t_{VDS}[Note 2]		2			μs
Initial program pulse width	t_{PW}		0.095	0.1	0.105	ms
$\overline{OE}$ set time	t_{OES}		2			μs
Valid data delay time from $\overline{OE}$	t_{OE}			1	2	ns

Notes 1. These symbols (except t_{VDS}) correspond to those of the corresponding μPD27C1001A.

2. For μPD27C1001A, read t_{VDS} as t_{VCS}.

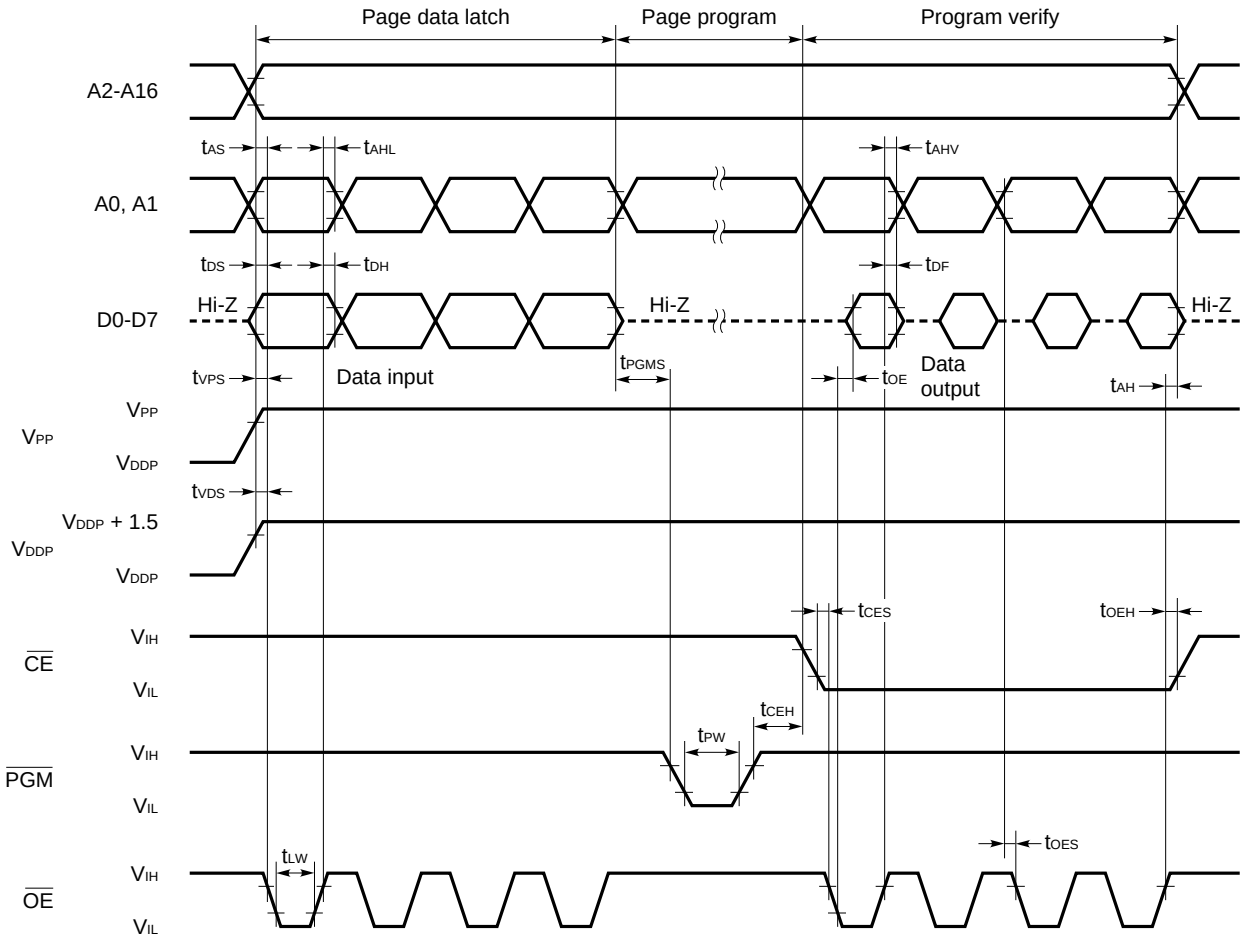
PROM Read Mode

Parameter	Symbol[Note 1]	Conditions	MIN.	TYP.	MAX.	Unit
Data output time from address	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$			200	ns
Delay from $\overline{CE} \downarrow$ to data output	t_{CE}	$\overline{OE} = V_{IL}$		1	2	μs
Delay from $\overline{OE} \downarrow$ to data output	t_{OE}	$\overline{CE} = V_{IL}$		1	2	μs
Data hold time to $\overline{OE}\uparrow$ or $\overline{CE}\uparrow$[Note 2]	t_{DF}	$\overline{CE} = V_{IL}$ or $\overline{OE} = V_{IL}$	0		60	ns
Data hold time to address	t_{OH}	$\overline{CE} = \overline{OE} = V_{IL}$	0			ns

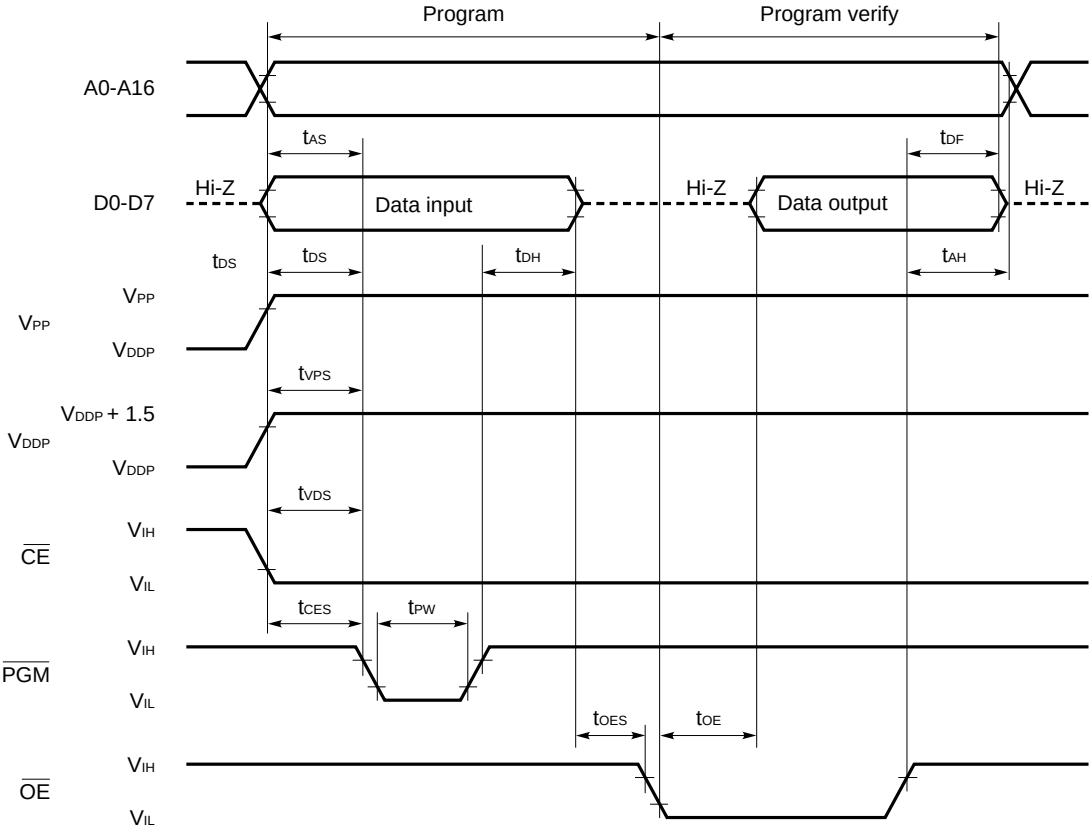
Notes 1. These symbols correspond to those of the corresponding μPD27C1001A.

2. t_{DF} is the time measured from when either $\overline{OE}$ or $\overline{CE}$ reaches V_{IH}, whichever is faster.

PROM Write Mode Timing (Page Program Mode)



PROM Write Mode Timing (Byte Program Mode)

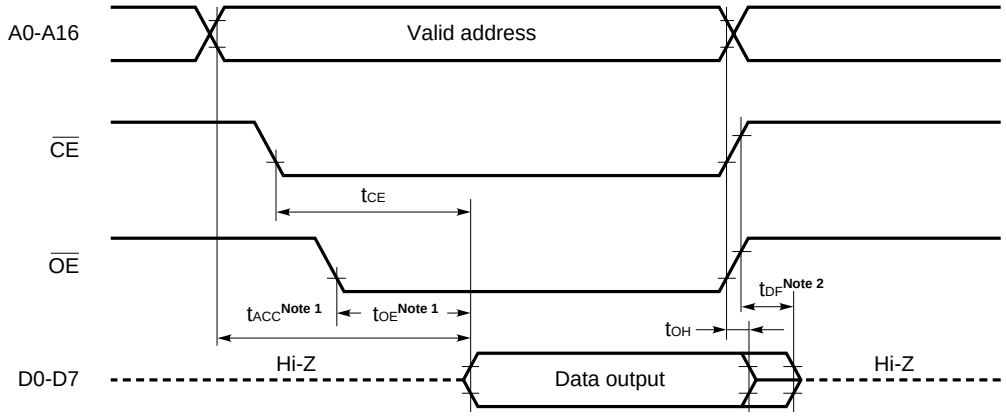


Cautions 1. V_{DDP} must be applied before V_{PP}, and must be cut after V_{PP}.

2. V_{PP} including overshoot must not exceed 13.5 V.

3. Plugging in or out the board with the V_{PP} pin supplied with 12.5 V may adversely affect its reliability.

PROM Read Mode Timing

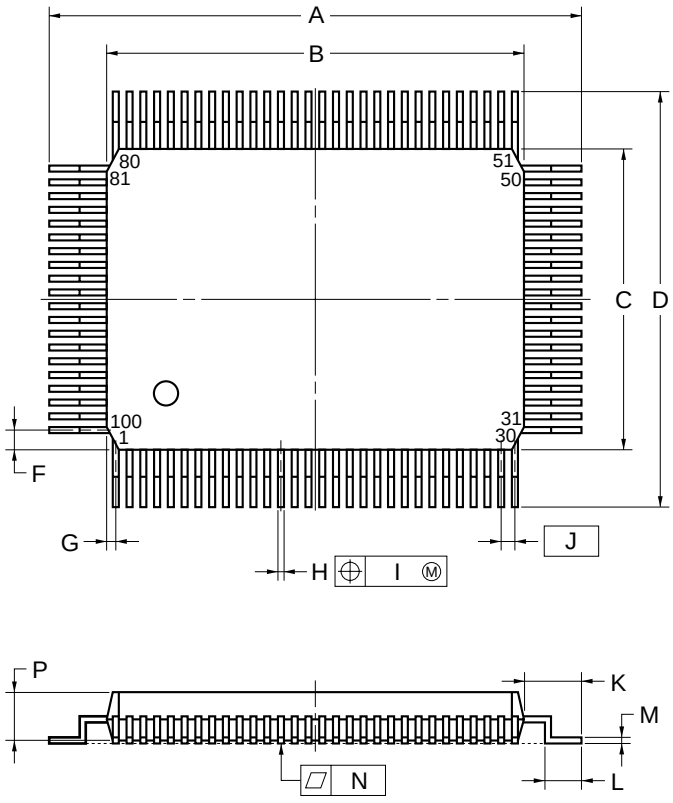


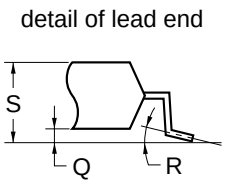
Notes 1. For reading within t_{ACC}, the delay of the $\overline{OE}$ input from falling edge of $\overline{CE}$ must be within t_{ACC}-t_{OE}.

2. t_{DF} is the time measured from when either $\overline{OE}$ or $\overline{CE}$ reaches V_{IH}, whichever is faster.

9. PACKAGE DRAWING

100PIN PLASTIC QFP (14x20)





NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

Remark The shape and material of the ES version are the same as those of the corresponding mass-produced product.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7±0.1	$0.106^{+0.005}_{-0.004}$
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P100GF-65-3BA1-3

10. RECOMMENDED SOLDERING CONDITIONS

The conditions listed below shall be met when soldering the μPD78P4908.

For details of the recommended soldering conditions, refer to our document **Semiconductor Device Mounting Technology Manual (C10535E)**.

Please consult with our sales offices in case any other soldering process is used, or in case soldering is done under different conditions.

Table 10-1. Soldering Conditions for Surface-Mount Devices

μPD78P4908GF-3BA: 100-pin plastic QFP (14 × 20 mm)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235°C Reflow time: 30 seconds or less (210°C or more) Maximum allowable number of reflow processes: 2 Exposure limit: 7 days**Note** (20 hours of pre-baking is required at 125°C afterward)	IR35-207-2
VPS	Peak package's surface temperature: 215°C Reflow time: 40 seconds or less (200°C or more) Maximum allowable number of reflow processes: 2 Exposure limit: 7 days**Note** (20 hours of pre-baking is required at 125°C afterward)	VP15-207-2
Wave soldering	Solder temperature: 260°C or less Flow time: 10 seconds or less Number of flow processes: 1 Preheating temperature: 120°C MAX. (measured on the package surface) Exposure limit: 7 days**Note** (20 hours of pre-baking is required at 125°C afterward)	WS60-207-1
Partial heating method	Terminal temperature: 300°C or less Heat time: 3 seconds or less (for one side of a device)	–

Note Maximum number of days during which the product can be stored at a temperature of 25°C and a relative humidity of 65% or less after dry-pack package is opened.

Caution Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78P4908.
See also **(5) Notes on using development tools**.

(1) Language processing software

RA78K4	Assembler package for all 78K/IV series models
CC78K4	C compiler package for all 78K/IV series models
DF784908	Device file for μPD784908 subseries models
CC78K4-L	C compiler library source file for all 78K/IV series models

(2) PROM write tools

PG-1500	PROM programmer
PA-78P4908GF	Programmer adapter, connects to PG-1500
PG-1500 controller	Control program for PG-1500

(3) Debugging tools

- **When using the in-circuit emulator IE-78K4-NS**

IE-78K4-NS	In-circuit emulator for all 78K/IV series models
IE-70000-MC-PS-B	Power supply unit for IE-78K4-NS
★ IE-70000-98-IF-C	Interface adapter when the PC-9800 series computer (other than a notebook) is used as the host machine (C bus compatible)
★ IE-70000-CD-IF-A	PC card and interface cable when a notebook is used as the host machine (PCMCIA socket compatible)
★ IE-70000-PC-IF-C	Interface adapter when the IBM PC/AT™ compatible is used as the host machine (ISA compatible)
★ IE-7000-PCI-IF	Adapter when a computer with a PCI bus as the host machine
IE-784908-NS-EM1**Note**	Emulation board for evaluating μPD784908 subseries models
NP-100GF**Note**	Emulation probe for 100-pin plastic QFP (GF-3BA type)
EV-9200GF-100	Socket for mounting on target system board made for 100-pin plastic QFP (GF-3BA type). Used in LCC mode.
ID78K4-NS	Integrated debugger for IE-78K4-NS
SM78K4	System simulator for all 78K/IV series models
DF784908	Device file for μPD784908 subseries models

Note Under development

- **When using the in-circuit emulator IE-784000-R**

IE-784000-R	In-circuit emulator for all 78K/IV series models
★ IE-70000-98-IF-C	Interface adapter when the PC-9800 series computer (other than a notebook) is used as the host machine (C bus compatible)
★ IE-70000-PC-IF-C	Interface adapter when the IBM PC/AT compatible is used as the host machine (ISA bus compatible)
★ IE-7000-PCI-IF	Adapter when a computer with a PCI bus as the host machine
IE-78000-R-SV3	Interface adapter and cable when the EWS is used as the host machine
IE-784908-NS-EM1 IE-784908-R-EM1	Emulation board for evaluating μPD784908 subseries models
IE-784000-R-EM	Emulation board for all 78K/IV series models
IE-78K4-R-EX2	Conversion board for emulation probes required to use the IE-784908-NS-EM1 on the IE-784000-R. The board is not needed when the conventional product IE-784908-R-EM1 is used.
EP-78064-GF-R	Emulation probe for 100-pin plastic QFP (GF-3BA type)
EV-9200GF-100	Socket for mounting on target system board made for 100-pin plastic QFP (GF-3BA type)
ID78K4	Integrated debugger for IE-784000-R
SM78K4	System simulator for all 78K/IV series models
DF784908	Device file for μPD784908 subseries models

(4) Real-time OS

RX78K/IV	Real-time OS for 78K/IV series models
MX78K4	OS for 78K/IV series models

(5) Notes when using development tools

- The ID78K4-NS, ID78K4, and SM78K4 can be used in combination with the DF784908.
- The CC78K4 and RX78K/IV can be used in combination with the RA78K4 and DF784908.
- The NP-100GF is a product from Naito Densei Machida Mfg. Co., Ltd. (044-822-3813). Consult the NEC sales representative for purchasing.
- The host machines and operating systems corresponding to each software are shown below.

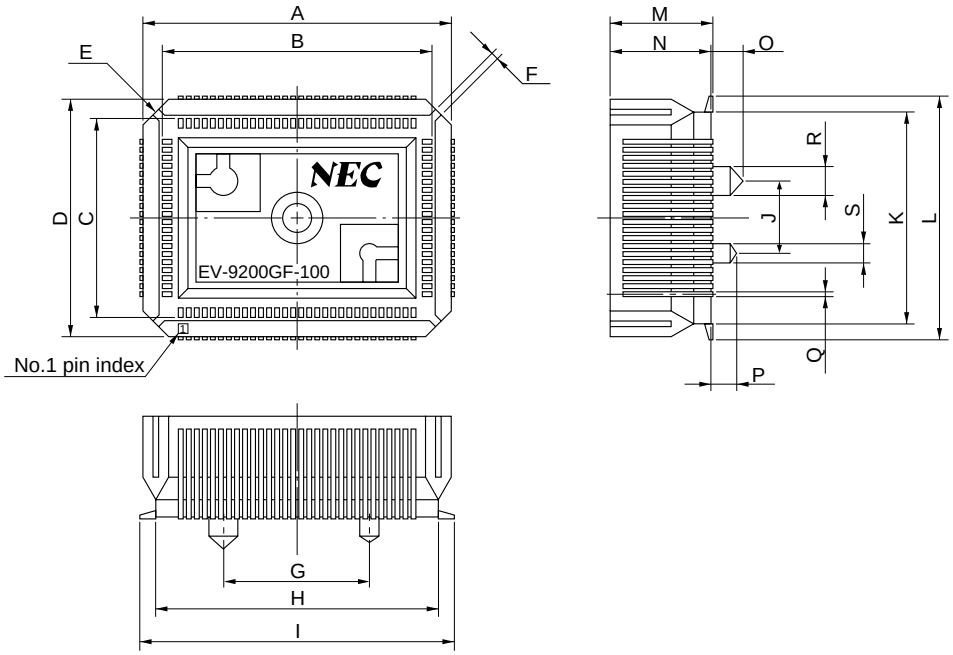
Host machine [OS] / Software	PC	EWS
	PC-9800 series [Windows™] IBM PC/AT compatibles [Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K4	○Note	○
CC78K4	○Note	○
PG-1500 controller	○Note	–
ID78K4-NS	○	–
ID78K4	○	○
SM78K4	○	–
RX78K/IV	○Note	○
MX78K4	○Note	○

Note Software under MS-DOS

APPENDIX B CONVERSION SOCKET (EV-9200GF-100) PACKAGE DRAWING

Connect the μPD78P4908GF-3BA (100-pin plastic QFP (14 × 20 mm)) to the circuit board in combination with the EV-9200GF-100.

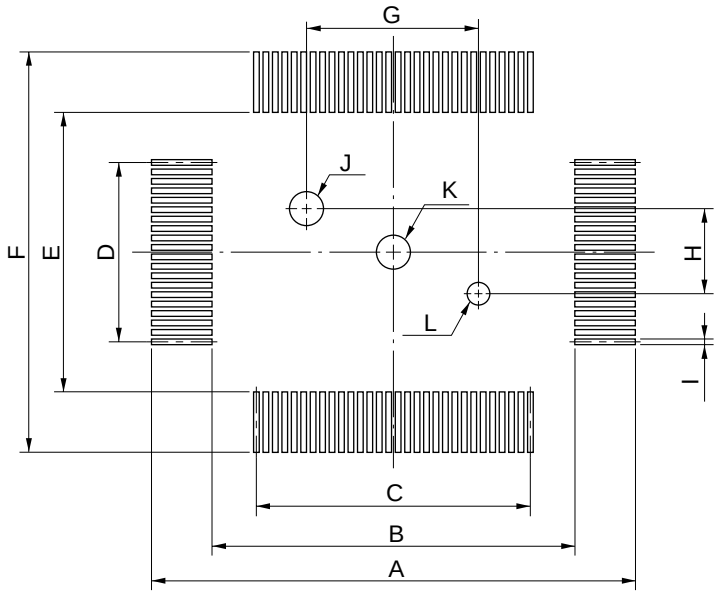
Figure B-1. Package Drawings of EV-9200GF-100 (Reference)



EV-9200GF-100-G0

ITEM	MILLIMETERS	INCHES
A	24.6	0.969
B	21	0.827
C	15	0.591
D	18.6	0.732
E	4-C 2	4-C 0.079
F	0.8	0.031
G	12.0	0.472
H	22.6	0.89
I	25.3	0.996
J	6.0	0.236
K	16.6	0.654
L	19.3	076
M	8.2	0.323
N	8.0	0.315
O	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	φ2.3	φ0.091
S	φ1.5	φ0.059

Figure B-2. Recommended Pattern to Mount EV-9200GF-100 on a Substrate (Reference)



EV-9200GF-100-P1E

ITEM	MILLIMETERS	INCHES
A	26.3	1.035
B	21.6	0.85
C	$0.65\pm0.02\times29=18.85\pm0.05$	$0.026^{+0.001}_{-0.002}\times1.142=0.742^{+0.002}_{-0.002}$
D	$0.65\pm0.02\times19=12.35\pm0.05$	$0.026^{+0.001}_{-0.002}\times0.748=0.486^{+0.003}_{-0.002}$
E	15.6	0.614
F	20.3	0.799
G	12 ± 0.05	$0.472^{+0.003}_{-0.002}$
H	6 ± 0.05	$0.236^{+0.003}_{-0.002}$
I	0.35 ± 0.02	$0.014^{+0.001}_{-0.001}$
J	$\phi2.36\pm0.03$	$\phi0.093^{+0.001}_{-0.002}$
K	$\phi2.3$	$\phi0.091$
L	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

APPENDIX C RELATED DOCUMENTS

Documents Related to Devices

Document name		Document No.	
		Japanese	English
μPD784907, 784908 Data Sheet		U11680J	U11680E
μPD78P4908 Data Sheet		U11681J	This document
μPD784908 Subseries User's Manual – Hardware		U11787J	U11787E
μPD784908 Subseries Special Function Registers		U11589J	—
78K/IV Series User's Manual – Instruction		U10905J	U10905E
78K/IV Series Instruction Table		U10594J	—
78K/IV Series Instruction Set		U10595J	—
78K/IV Series Application Note	Software Basic	U10095J	U10095E

Documents Related to Development Tools (User's Manual)

Document name		Document No.	
		Japanese	English
RA78K4 Assembler Package	Operation	U11334J	U11334E
	Language	U11162J	U11162E
RA78K Series Structured Assembler Preprocessor		U11743J	U11743E
CC78K4 C Compiler	Operation	U11572J	U11572E
	Language	U11571J	U11571E
PG-1500 PROM Programmer		U11940J	U11940E
PG-1500 Controller PC-9800 Series (MS-DOS™) Base		EEU-704	EEU-1291
PG-1500 Controller IBM PC Series (PC DOS™) Base		EEU-5008	U10540E
★ IE-78K4-NS		U13356J	U13356E
IE-784000-R		U12903J	U12903E
IE-784908-R-EM1		U11876J	—
★ IE-784908-NS-EM1		U13743J	On preparation
EP-78064		EEU-934	EEU-1469
SM78K4 System Simulator Windows Base	Reference	U10093J	U10093E
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092J	U10092E
ID78K4-NS Integrated Debugger PC Base	Reference	U12796J	U12796E
ID78K4 Integrated Debugger Windows Base	Reference	U10440J	U10440E
ID78K4 Integrated Debugger HP-UX, SunOS, NEWS-OS Base	Reference	U11960J	U11960E

Caution The above documents may be revised without notice. Use the latest versions when you design application systems.

Documents Related to Software to Be Incorporated into the Product (User's Manual)

Document name		Document No.	
		Japanese	English
78K/IV Series Real-Time OS	Fundamental	U10603J	U10603E
	Installation	U10604J	U10604E
	Debugger	U10364J	—
OS for 78K/IV Series MX78K4	Fundamental	U11779J	—

Other Documents

Document name	Document No.	
	Japanese	English
★ NEC IC Package Manual (CD-ROM)	–	C13388E
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Device	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Guide to Quality Assurance for Semiconductor Devices	—	MEI-1202
Guide for Products Related to Microcomputer: Other Companies	U11416J	—

Caution The above documents may be revised without notice. Use the latest versions when you design application systems.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.l.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH
Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

NEC Electronics (France) S.A.
Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

NEC Electronics (France) S.A.
Spain Office
Madrid, Spain
Tel: 91-504-2787
Fax: 91-504-2860

NEC Electronics (Germany) GmbH
Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
United Square, Singapore 1130
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.
Electron Devices Division
Rodovia Presidente Dutra, Km 214
07210-902-Guarulhos-SP Brasil
Tel: 55-11-6465-6810
Fax: 55-11-6465-6829

J99.1

IEBus is a trademark of NEC Corporation.
MS-DOS and Windows are either registered trademarks or trademarks of Microsoft Corporation in the United States and/or other countries.
PC/AT and PC DOS are trademarks of IBM Corporation.
HP9000 series 700 and HP-UX are trademarks of Hewlett-Packard Company.
SPARCstation is a trademark of SPARC International, Inc.
Solaris and SunOS are trademarks of Sun Microsystems, Inc.
NEWS and NEWS-OS are trademarks of SONY Corporation.

Some related documents may be preliminary versions. Note that, however, what documents are preliminary is not indicated in this document.

The export of this product from Japan is regulated by the Japanese government. To export this product may be prohibited without governmental license, the need for which must be judged by the customer. The export or re-export of this product from a country other than Japan may also be prohibited without a license from that country. Please call an NEC sales representative.

The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

M4 96.5