NEC

MOS Integrated Circuit

μPD78P328

16/8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD78P328 is a product provided by replacing the μPD75328's internal mask ROM with one-time PROM or EPROM.

The one-time PROM version is programmable only once and is useful for small-lot production of many different products and early development and time-to-market of application sets.

The EPROM version is reprogrammable, and suited for the evaluation of systems.

Functions are described in detail in the following user's manual. Be sure to read it before designing.

μPD78328 User's Manual: IEU-1268

FEATURES

- μPD78328 compatible
  - For mass-production, the μPD78P328 can be replaced with the μPD78328 incorporating mask ROM
- Internal PROM: 16,384 x 8 bits
  - Programmable once only (one-time PROM version without window)
  - Erasable with ultraviolet rays and electrically programmable (EPROM version with window)
- PROM programming characteristics: μPD27C256A compatible
- The μPD78P328 is a QTOP™ microcontroller.

Remark QTOP microcontroller is a general term for microcontrollers which incorporates one-time PROM, and are totally supported by NEC's programming service (from programming to marking, screening, and verification).

ORDERING INFORMATION

Part Number	Package	Internal ROM
μPD78P328CW	64-pin plastic shrink DIP (750 mils)	One-time PROM
μPD78P328GF-3BE	64-pin plastic QFP (14 x 20 mm)	One-time PROM
μPD78P328DW	64-pin ceramic shrink DIP (750 mils) (with window)	EPROM

Functions common to the one-time PROM and EPROM versions are referred to as PROM functions throughout this document.

The information in this document is subject to change without notice.

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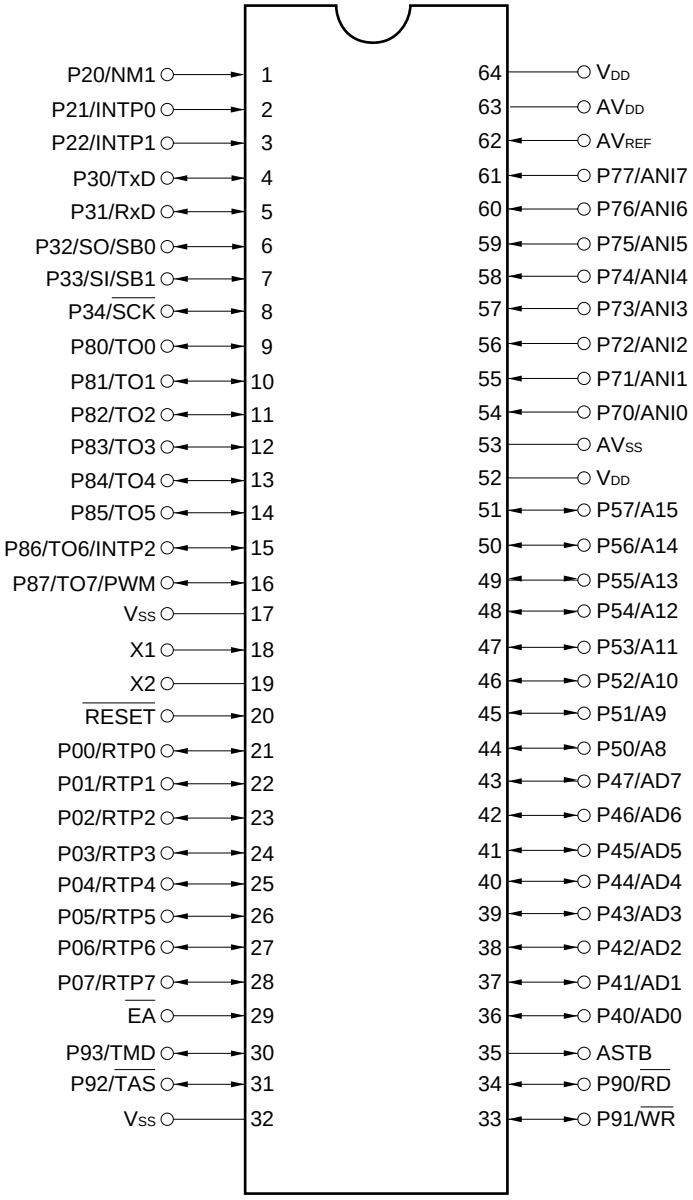
Printed in Japan

The mark ★ shows revised points.

PIN CONFIGURATIONS

(1) Normal operating mode

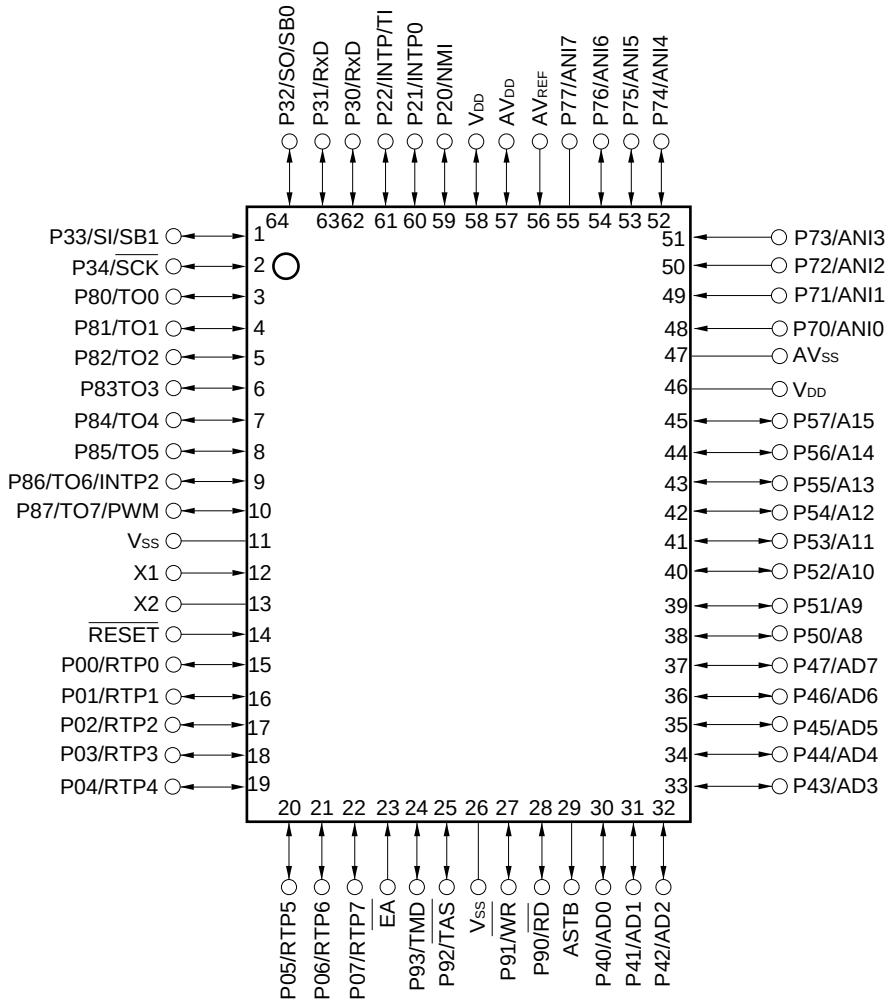
- **64-pin plastic shrink DIP (750 mils)**
  μPD78P328CW
- **64-pin ceramic shrink DIP (750 mils) (with window)**
  μPD78P328DW



Remark These pins are compatible with the μPD78328CW pins.

• **64-pin plastic QFP (14 x 20 mm)**

μPD78P328GF-3BE



Remark These pins are compatible with the μPD78328GF pins.

P00-P07	:	Port 0
P20-P22	:	Port 2
P30-P34	:	Port 3
P40-P47	:	Port 4
P50-P57	:	Port 5
P70-P77	:	Port 7
P80-P87	:	Port 8
P90-P93	:	Port 9
A8-A15	:	Address8-15
AD0-AD7	:	Address0-7/Data0-7
ANI0-ANI7	:	Analog Input0-7
TO0-TO7	:	Timer Output0-7
NMI	:	Nonmaskable Interrupt
PWM	:	Pulse Wide Modulation Output
INTP0-INTP2	:	Interrupt From Peripherals0-2
RTP0-RTP7	:	Real-Time Port0-7
TxD	:	Transmit Data
RxD	:	Receive Data
SI	:	Serial Input
SO	:	Serial Output
SB0-SB1	:	Serial Bus0-1
$\overline{RD}$	:	Read Strobe
$\overline{WR}$	:	Write Strobe
ASTB	:	Address Strobe
$\overline{EA}$	:	External Access
$\overline{RESET}$	:	Reset
$\overline{SCK}$	:	Serial Clock
$\overline{TAS}$	:	Turbo Access Strobe
TMD	:	Turbo Mode
X1, X2	:	Crystal1, 2
AV_{DD}	:	Analog V_{DD}
AV_{REF}	:	Analog Reference Voltage
AV_{SS}	:	Analog V_{SS}
V_{DD}	:	Power Supply
V_{SS}	:	Ground

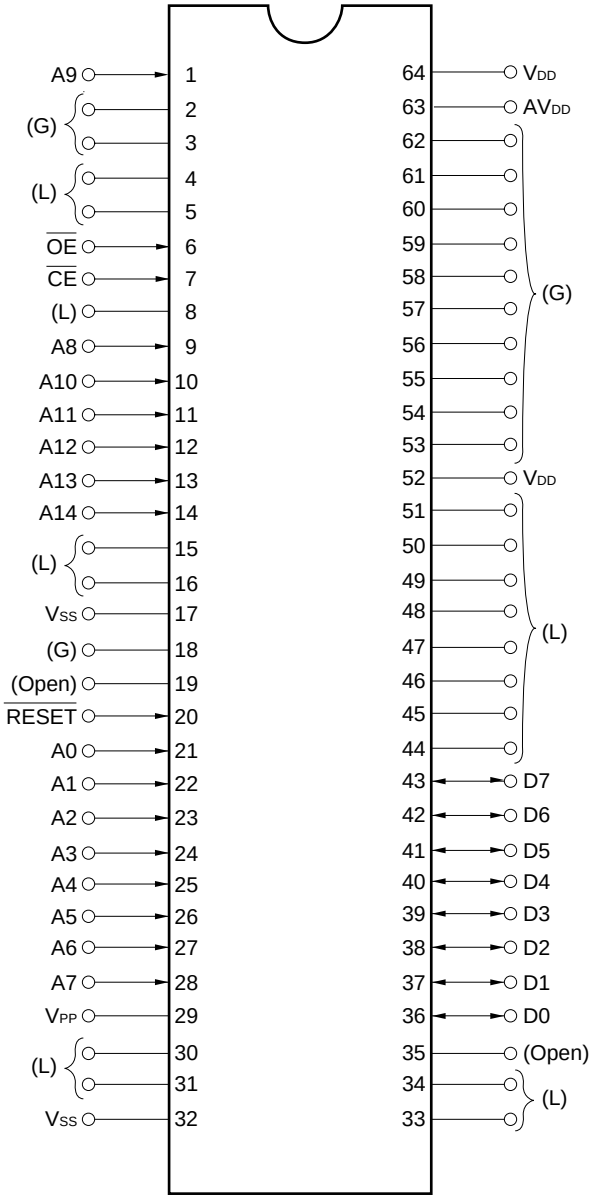
(2) PROM programming mode ($\overline{RESET}$ = H, AV_{DD} = L)

- **64-pin plastic shrink DIP (750 mils)**

  μPD78P328CW

- **64-pin ceramic shrink DIP (750 mils) (with window)**

  μPD78P328DW



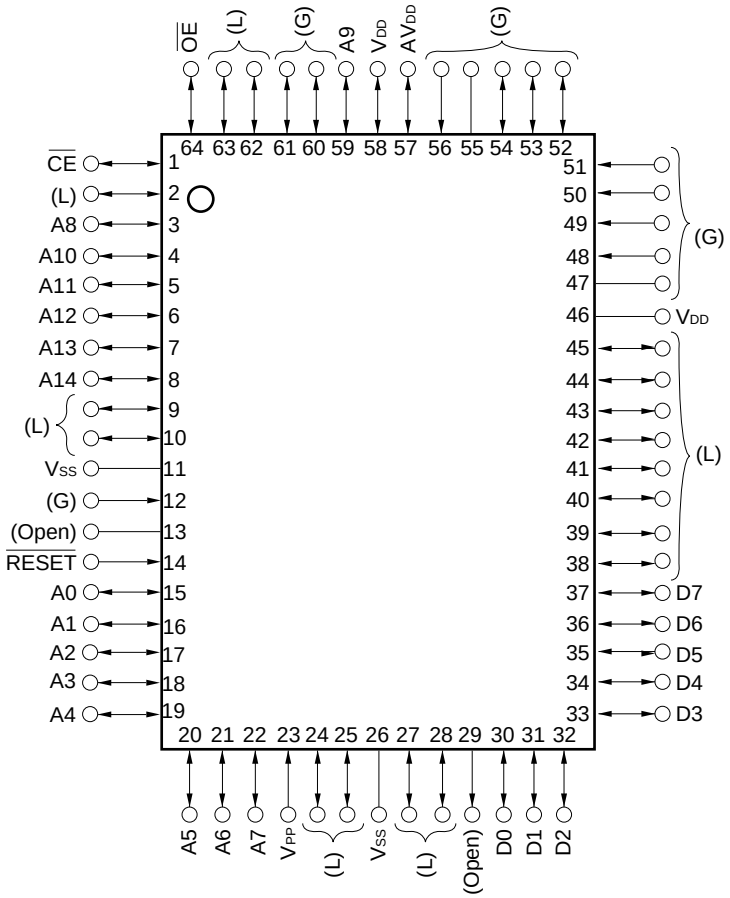
Caution The recommended connection of the unused pins in the PROM programming mode are indicated in parentheses.

L : Connect each pin to V_{SS} via a resistor.

G : Connect the pin to V_{SS}.

Open : Leave the pin unconnected.

• **64-pin plastic QFP (14 x 20 mm)**
μPD78P328GF-3BE



Caution The recommended connection of the unused pins in the PROM programming mode are indicated in parentheses.

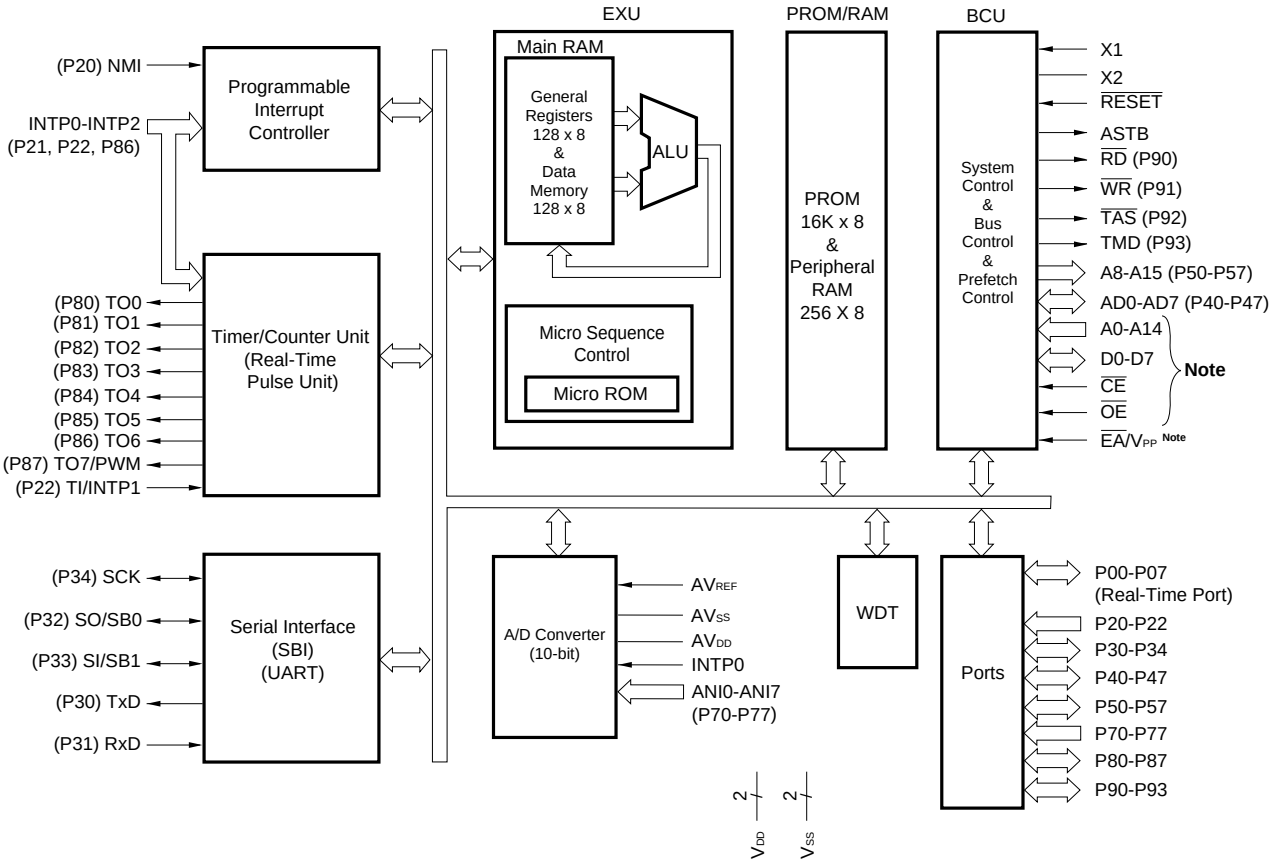
L : Connect each pin to V_{SS} via a resistor.

G : Connect the pin to V_{SS}.

Open : Leave the pin unconnected.

A0-A14	: Address0-14	AV_{DD}	: Analog V_{DD}
D0-D7	: Data0-7	V_{DD}	: Power Supply
$\overline{CE}$	: Chip Enable	V_{SS}	: Ground
$\overline{OE}$	: Output Enable	V_{PP}	: Programming Power Supply
$\overline{RESET}$	: Reset		

BLOCK DIAGRAM



Note During PROM programming mode

CONTENTS

1. PIN FUNCTIONS

1.1 Normal Operating Mode

(1) Port Pins

Pin Name	Input/Output	Function	Alternate Function
P00-P07	Input/Output	PORT0 4-/8-bit input/output port Input or output mode can be specified bit-wise. The port can also operate as a real-time output port.	RTP0-RTP7
P20	Input	PORT 2 3-bit input-only port	NMI
P21			INTP0
P22			INTP1/TI
P30	Input/Output	PORT 3 5-bit input/output port Input or output mode can be specified bit-wise.	TxD
P31			RxD
P32			SO/SB0
P33			SI/SB1
P34			$\overline{SCK}$
P40-P47	Input/Output	PORT 4 8-bit input/output port Input or output mode can be specified in 8-bit units.	AD0-AD7
P50-P57	Input/Output	PORT 5 8-bit input/output port Input or output mode can be specified bit-wise.	A8-A15
P70-P77	Input	PORT 7 8-bit input-only port	ANI0-ANI7
P80	Input/Output	PORT 8 8-bit input/output port Input or output mode can be specified bit-wise.	TO0
P81			TO1
P82			TO2
P83			TO3
P84			TO4
P85			TO5
P86			TO6/INTP2
P87			TO7/PWM
P90	Input/Output	PORT 9 4-bit input/output port Input or output mode can be specified bit-wise.	$\overline{RD}$
P91			$\overline{WR}$
P92			$\overline{TAS}$
P93			TMD

(2) Non-Port Pins (1/2)

Pin Name	Input/Output	Function	Alternate Function
RTP0-RTP7	Output	Real-time output port which outputs a pulse in synchronization with the trigger signal from real-time pulse unit (RPU).	P00-P07
NMI	Input	Edge-detected nonmaskable interrupt request input. The rising or falling edge can be selected for the valid edge by setting the mode register.	P20
INTP0	Input	Edge-detected external interrupt request input. The valid edge can be specified in the mode register.	P21
INTP1			P22/T1
INTP2			P86/TO6
TI	Input	External count clock input pin to timer 1 (TM1).	S22/INTP1
RxD	Input	Serial data input pin to asynchronous serial interface (UART).	P30
TxD	Output	Serial data output pin from asynchronous serial interface (UART).	P31
SO	Output	Serial data output pin from clocked serial interface in 3-wire mode.	P32/SB0
SI	Input	Serial data input pin to clocked serial interface in 3-wire mode.	P33/SB1
SB0	Input/Output	Serial data input/output pins to/from clocked serial interface in SBI mode.	P32/SO
SB1			P33/SI
$\overline{SCK}$	Input/Output	Serial clock input/output pin to/from clocked serial interface.	P34
AD0-AD7	Input/Output	Multiplexed address/data bus used when external memory is added.	P40-P47
A8-A15	Output	Address bus used when external memory is added.	P50-P57
TO0	Output	Pulse output from real-time pulse unit.	P80
TO1			P81
TO2			P82
TO3			P83
TO4			P84
TO5			P85
TO6			P86/INTP2
TO7			P87/PWM
PWM	Output	PWM signal output from real-time pulse unit.	P87/TO7
$\overline{RD}$	Output	Strobe signal output for external memory read operation.	P90
$\overline{WR}$		Strobe signal output for external memory write operation.	P91
* $\overline{TAS}$		Control signal output pins to access turbo access manager (μPD71P301). Note	P92
TMD			P93
ASTB	Output	Timing signal output pin to externally latch an address information output to port 4 for external memory access.	—
$\overline{EA}$	Input	For μPD78P328, normally connect the $\overline{EA}$ pin to V_{DD}. When the $\overline{EA}$ pin is connected to V_{SS}, the μPD78P328 enters the ROMless mode and external memory is accessed. The $\overline{EA}$ pin level cannot be changed during operation.	—

Note Turbo access manager (μPD71P301) is available for maintenance purposes only.

(2) Non-Port Pins (2/2)

Pin Name	Input/Output	Function	Alternate Function
ANI0-ANI7	Input	Analog input to A/D converter.	P70-P77
AV_{REF}	Input	A/D converter reference voltage input.	—
AV_{DD}	—	A/D converter analog power supply.	—
AV_{SS}	—	A/D converter GND.	—
$\overline{RESET}$	Input	System reset input.	—
X1	Input	Crystal connection pin for system clock generation. To supply external clock,	—
X2	—	input to the X1 and input reverse signal to the X2 pin (X2 pin can be unconnected.)	—
V_{DD}	—	Positive power supply pin.	—
V_{SS}	—	GND pin.	—

1.2 PROM Programming Mode ($\overline{RESET}$ = H, AV_{DD} = L)

Pin Name	Input/Output	Function
AV_{DD}	Input	PROM programming mode setting.
$\overline{RESET}$		
A0-A14	—	Address bus.
D0-D7	—	Data bus.
$\overline{CE}$	Input	PROM enable to PROM.
$\overline{OE}$	Input	Read strobe to PROM.
V_{PP}	—	Write power supply.
V_{DD}		Positive power supply.
V_{SS}		GND.

1.3 Pin Input/Output Circuits and Recommended Connection of Unused Pins

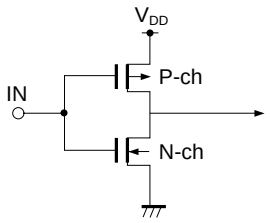
Table 1-1 and Figure 1-1 show the pin input/output circuit schematically.

Table 1-1. Pin Input/Output Circuits and Recommended Connection of Unused Pins

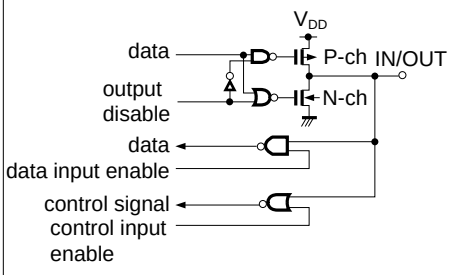
Pin	Input/Output circuit type	Recommended connection of unused pins
P00P07/RTP0-RTP7	5	Input state: Independently connect to V_{DD} or V_{SS} via a resistor. Output state: Leave Open.
P21/NMI P21/INTP0 P27/INTP6/TI	2	Connect to V_{SS}.
P30/TxD P31/RxD	5	Input state: Independently connect to V_{DD} or V_{SS} via a resistor. Output state: Leave Open.
P32/SO/SB0 P33/SI/SB1 P34/$\overline{SCK}$	8	
P40/AD0-P47/AD0-AD7 P50/P57/A8-A15	5	
P70-P77/ANI0-ANI7	9	Connect to V_{SS}.
P80-P85/TO0-TO5	5	Input state: Independently connect to V_{DD} or V_{SS} via a resistor. Output state: Leave Open.
P86/TO6/INTP2	6	
P87/TO7/PWM	5	
P90/$\overline{RD}$ P91/$\overline{WR}$ P92/$\overline{TAS}$ P93/TMD	5	
ASTB	4	Leave Open.
EA	1	—
$\overline{RESET}$	2	—
AV_{REF}, AV_{SS}	—	Connect to V_{SS}.
V_{DD}	—	Connect to V_{DD}.

Figure 1-1. Pin Input/Output Circuits

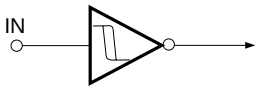
TYPE 1



TYPE 6

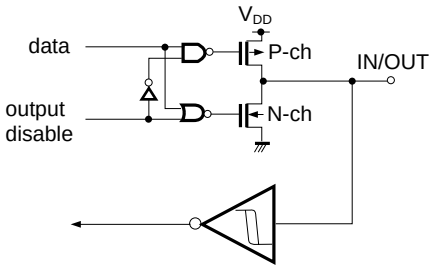


TYPE 2

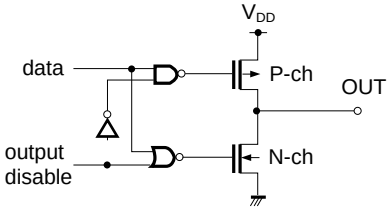


Schmitt-triggerred input with hysteresis characteristics

TYPE 8

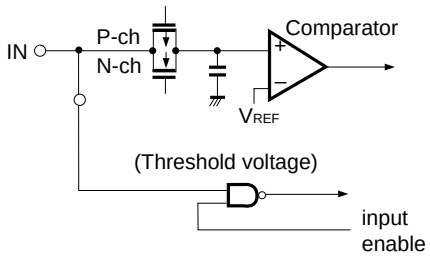


TYPE 4

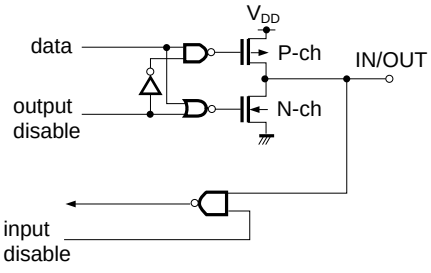


Push-pull output that can be placed in high impedance (both P-ch and N-ch off).

TYPE 9



TYPE 5



2. DIFFERENCES BETWEEN μPD78P328 and μPD78328

The μPD78P328 is a product provided by replacing the μPD78328's on-chip mask ROM with one-time PROM or EPROM. Thus, the μPD78P328 and μPD78328 are the same in function except for the ROM specifications such as write or verify. Table 2-1 lists the differences between these two products.

This Data Sheet describes the PROM specification function. Refer to the μPD78328 documents for details of other functions.

Table 2-1. Differences between μPD78P328 and μPD78328

Item	**μPD78P328**		μPD78328
Internal program memory (electrical program)	One-time PROM (programmable only once)	EPROM (reprogrammable)	Mask ROM (nonprogrammable)
PROM programming pin	Contained		Not contained
Package	• 64-pin plastic shrink DIP • 64-pin plastic QFP	• 64-pin ceramic shrink DIP (with window)	• 64-pin plastic shrink DIP • 64-pin plastic QFP
* Electrical specifications	Current dissipations are different.		
* Others	Noise immunity and noise radiation differ because circuit complexity and mask layout are different.		

* **Caution The noise immunity and noise radiation differ between the PROM and mask ROM versions. To replace the PROM version with the mask ROM version when shifting from experimental production to mass production, evaluate your system by using the CS version (not ES version) of the mask ROM version.**

3. PROM PROGRAMMING

The PROM incorporated in the μPD78P328 is a 16,384 x 8-bit electrically writable PROM. For programming, set the PROM programming mode by using the $\overline{\text{RESET}}$ and AV_{DD} pins.

The programming characteristics are compatible with the μPD27C256A programming characteristics.

Table 3-1. Pin Function in Programming Mode

Function	Normal Operating Mode	Programming Mode
Address input	P00-P07, P80, P20, P81-P85	A0-A14
Data input	P40-P47	D0-D7
Chip enable/program pulse	P33	$\overline{\text{CE}}$
Output enable	P32	$\overline{\text{OE}}$
Program voltage	$\overline{\text{EA}}$	V_{PP}
Mode control	$\overline{\text{RESET}}$, AV_{DD}	

3.1 Operation Mode

To set the program write/verify mode, set $\overline{\text{RESET}}$ = H and AV_{DD} = L. For the mode, the operation mode can be selected by setting the $\overline{\text{CE}}$ and $\overline{\text{OE}}$ pins, as listed in Table 3-2.

To read the PROM contents, set the read mode.

Connect the unused pins exactly as indicated on Pin Configuration.

Table 3-2. PROM Programming Operation Mode

Mode	$\overline{\text{RESET}}$	AV_{DD}	$\overline{\text{CE}}$	$\overline{\text{OE}}$	V_{PP}	V_{DD}	D0-D7
Program write	H	L	L	H	+12.5 V	+6 V	Data input
Program verify			H	L			Data output
Program inhibit			H	H			High impedance
Read			L	L	+5 V	+5 V	Data output
Output disable			L	H			High impedance
Standby			H	L/H			High impedance

Caution When V_{PP} is set to +12.5 V and V_{DD} is set to +6V, setting both $\overline{\text{CE}}$ and $\overline{\text{OE}}$ to L is inhibited.

3.2 PROM Write Procedure

The write procedure into PROM is as follows: (See also Figure 3-2).

(1) Fix $\overline{\text{RESET}}$ = H and AV_{DD} = L. Connect other unused pins exactly as indicated in section "Pin Configuration."
(2) Supply +6 V to the V_{DD} and +12.5 V to the V_{PP} pin.
(3) Supply an initial address.
(4) Supply write data.
(5) Supply 1 ms program pulse (active low) to the $\overline{\text{CE}}$ pin.
(6) Execute the verify mode. Check whether or not the write data is written normally.
  • When it is written normally: Proceed to step (8).
  • When it is not written normally: Repeat steps (4) to (6).
  If the data is not written normally after 25 repetitions of the steps, proceed to step (7).
(7) Assume the device to be defective. Stop write operation.
(8) Supply write data and X (number of steps (4) to (6) repetitions) x 3 ms program pulses (additional write).
(9) Increment the address.
(10) Repeat steps (4) to (9) to the last address.

Figure 3-1 shows the PROM Write/Verify Timing Steps (2) to (8) above.

Figure 3-1. PROM Write/Verify Timing

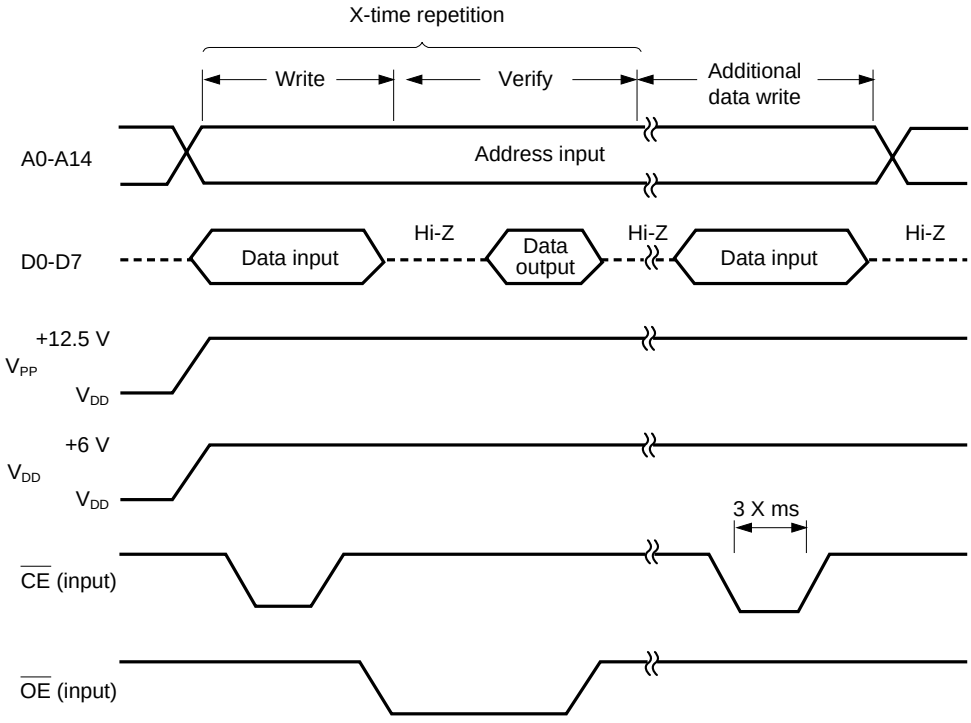
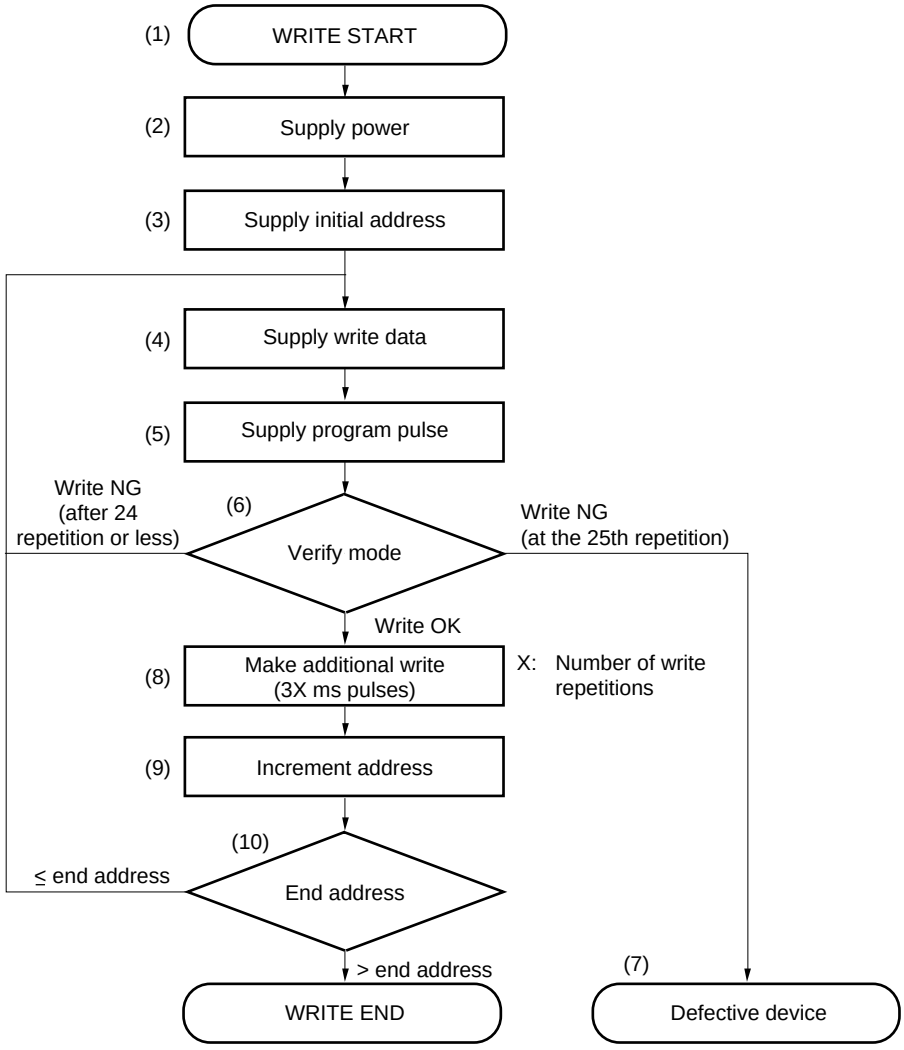


Figure 3-2. Write Procedure Flowchart



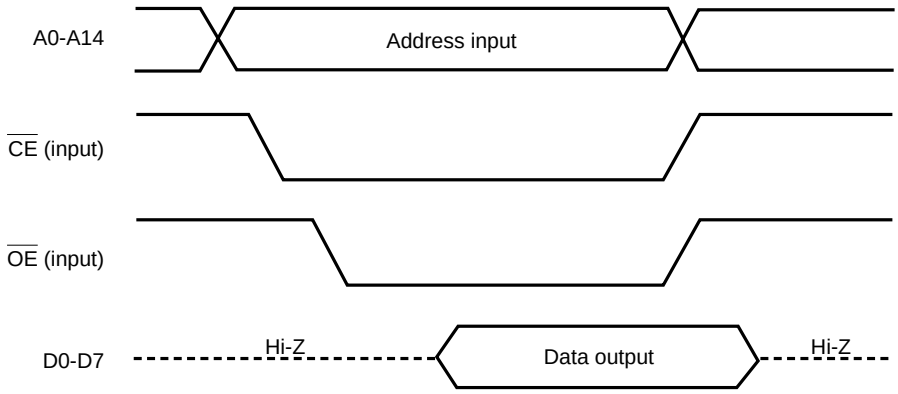
3.3 PROM Read Procedure

The read procedure of the PROM contents into the external data bus (D0-D7) is as follows.

(1) Fix $\overline{\text{RESET}}$ = H and AV_{DD} = L. Connect other unused pins exactly as indicated on Pin Configuration.
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) Input the address of the data to be read to the A0-A14 pins.
(4) Execute the read mode.
(5) The data is output to the D0-D7 pins.

Figure 3-3 shows the PROM read timing steps (2) to (5) above.

Figure 3-3. PROM Read Timing



4. ERASURE CHARACTERISTICS (EPROM VERSION ONLY)

The data written into the μPD78P328DW program memory can be erased (FFH) and new data can be rewritten into the memory.

To erase data, apply light with a wave length shorter than 400 nm to the window. Normally, apply ultraviolet rays having the 254-nm wave length. The radiation amount required to completely erase data is as follows:

- Ultraviolet strength x erasure time: 15 W•s/cm^2 or more
- Erasure time: 15 to 20 minutes when a 12,000 μW/cm^2 ultraviolet lamp is used. However, the time may be prolonged due to ultraviolet lamp performance deterioration, dirty window, etc.

For erasure, place an ultraviolet lamp at a position within 2.5 cm from the window. If a filter is attached to the ultraviolet lamp, remove the filter before applying ultraviolet rays.

5. WINDOW SEAL (EPROM VERSION ONLY)

If the μPD78P328DW window is exposed to sunlight or fluorescent lamp light for hours, EPROM data may be erased and the internal circuit may operate erroneously. To prevent such accidents from occurring, put a protective seal on the window.

A protective seal whose quality is guaranteed by NEC is attached to every EPROM version with window at shipment.

6. ONE-TIME PROM VERSION SCREENING

The one-time PROM versions (μPD78P328CW, 78P328GF-3BE) cannot be completely tested by NEC for shipment because of their structure. For screening, it is recommended to verify PROM after storing the necessary data under the following conditions:

NEC provides chargeable services ranging from one-time PROM writing to marking, screening, and verification for QTOP microcontroller products. For details, contact an NEC sales representative.

Storage temperature	Storage time
125°C	24 hours

7. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Test Conditions		Ratings	Unit
Power supply voltage	V_{DD}			–0.5 to +7.0	V
	V_{DD}			–0.5 to V_{DD} +0.5	V
	V_{PP}			–0.5 to +13.5	V
	AV_{SS}			–0.5 to +0.5	V
Input voltage	V_{I1}	**Note 1**		–0.5 to V_{DD} +0.5	V
	V_{I2}	P20/NIM (A9) PIN		–0.5 to +13.5	V
Output voltage	V_O			–0.5 to V_{DD} +0.5	V
Output current, low	I_{OL}	All output pins		4.0	mA
		Total for all pins		90	mA
Output current, high	I_{OH}	All output pins		–1.0	mA
		Total for all pins		–20	mA
Analog input voltage	V_{IAN}	**Note 2**	$AV_{DD} > V_{DD}$	-0.5 to V_{DD} +0.5	V
			$V_{DD} \geq AV_{DD}$	-0.5 to AV_{DD} +0.5	V
A/D converter reference input voltage	AV_{REF}		$AV_{DD} > V_{DD}$	-0.5 to V_{DD} +0.3	V
			$V_{DD} \geq AV_{DD}$	-0.5 to AV_{DD} +0.3	V
Operating ambient temperature	T_A			–10 to +70	°C
Storage temperature	T_{stg}			–65 to +150	°C

Notes 1. Pins except for P20/NMI (A9), P70/ANI0-P77/ANI7

2. P70/ANI0-P77/ANI7

* **Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter, even momentarily. In other words, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.**

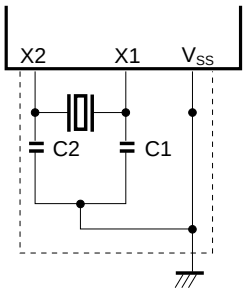
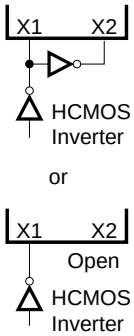
Recommended Operation Conditions

Oscillation frequency	T_A	V_{DD}
8 MHz ≤ f_{XX} ≤ 16 MHz	–10 to +70 ˚C	+5.0 V ±5%

Capacitance (T_A = 25 °C, V_{SS} = V_{DD} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz			10	pF
Output capacitance	C_O	Unmeasured pins returned to 0 V			20	pF
I/O capacitance	C_{IO}				20	pF

Oscillator Characteristics (T_A = –10 to +70 °C, V_{DD} = +5 V±5%, V_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	MIN.	MAX.	Unit
Ceramic or crystal resonator		Oscillation frequency (f_{XX})	8	16	MHz
External clock		X1 input frequency (f_X)	8	16	MHz
		X1 input rise, fall time (f_{XR}, t_{XF})	0	20	ns
		X1 input high, low level width (t_{WXH}, t_{WXL})	25	80	ns

Caution When using the system clock oscillator, wire the portion enclosed in dotted line in the figure as follows to avoid adverse influences on the wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring over the other signal lines. Do not route the wiring in the vicinity of lines through which a high fluctuating current flows.**
- **Always keep the ground point of the capacitor of the oscillator circuit at the same potential as V_{SS}. Do not connect the power source pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

Recommended Oscillator Constants

Ceramic resonator

Manufacturer Name	Part Number	Frequency [MHz]	Recommended Constants	
			C1 [pF]	C2 [pF]
MURATA	CSA8.00MT	8.0	30	30
	CSA12.0MT	12.0		
	CSA16.00MX040	16.0	15	15
	CST8.00MTW	8.0	Internal	Internal
	CST12.00MTW	12.0		
	CST16.00MXW0C3	16.0		

DC Characteristics (T_A = –10 to +70 °C, V_{DD} = +5 V ±5%, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, low	V_{IL}			0		0.8	V
Input voltage, high	V_{IH1}	**Note 1**		2.2			V
	V_{IH2}	**Note 2**		0.8V_{DD}			
Output voltage, low	V_{OL}	I_{OL} = 2.0 mA				0.45	V
Output voltage, high	V_{OH}	I_{OH} = –400 μA		V_{DD}–1.0			V
Input leakage current	I_{LI}	0 V ≤ V_I ≤ V_{DD}				±10	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}				±10	μA
V_{DD} power supply current	I_{DD1}	Operation mode			45	75	mA
	I_{DD2}	HALT mode			25	45	mA
Data retention voltage	V_{DDDR}	STOP mode		2.5			V
Data retention current	I_{DDDR}	STOP mode	V_{DDDR} = 2.5 V		3	15	μA
			V_{DDDR} = 5.0 V ±5%		10	50	μA

Notes 1. Pins except for $\overline{\text{RESET}}$, X1, X2, P20/NMI, P21/INTP0, P22/INTP1/TI, P86/INTP2/TO0, P32/SO/SB0, P33/SI/SB1, or P34/$\overline{\text{SCK}}$.

2. $\overline{\text{RESET}}$, X1, X2, P20/NMI, P21/INTP0, P22/INTP1/TI, P86/INTP2/TO0, P32/SO/SB0, P33/SI/SB1, or P34/$\overline{\text{SCK}}$ pins.

AC Characteristics (T_A = –10 to +70 °C, V_{DD} = +5 V ±5%, V_{SS} = 0 V)

Discontinuous read/write operation (when general-purpose memory is connected)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
System clock cycle time	t_{CYK}		125	250	ns
Address setup time (to ASTB ↓)	t_{SAST}		22		ns
Address hold time (from ASTB ↓)	t_{HSTA}		32		ns
Address → $\overline{RD}$ ↓ delay time	t_{DAR}		85		ns
$\overline{RD}$ ↓ → address float time	t_{FRA}			8	ns
Address → data input time	t_{DAID}			222	ns
$\overline{RD}$ ↓ → data input time	t_{DRID}			112	ns
ASTB ↓ → $\overline{RD}$ ↓ delay time	t_{DSTR}		42		ns
Data hold time (from $\overline{RD}$ ↑)	t_{HRID}		0		ns
$\overline{RD}$ ↑ → address active time	t_{DRA}		37		ns
$\overline{RD}$ low-level width	t_{WRL}		147		ns
ASTB high-level width	t_{WSTH}		37		ns
Address → $\overline{WR}$ ↓ delay time	t_{DAW}		85		ns
ASTB ↓ → data output time	t_{DSTOD}			102	ns
WR ↓ → data output time	t_{DWOD}			40	ns
ASTB ↓ → $\overline{WR}$ ↓ delay time	t_{DSTW}		42		ns
Data setup time (to $\overline{WR}$ ↑)	t_{SODW}		137		ns
Data hold time (from $\overline{WR}$ ↑)	t_{HWOD}		32		ns
$\overline{WR}$ ↑ → ASTB ↓ delay time	t_{DWST}		42		ns
$\overline{WR}$ low-level width	t_{WWL}		147		ns

t_{CYK}-Dependent Bus Timings

Parameter	Calculation expression	MIN./MAX.	Unit
t_{SAST}	0.5T – 40	MIN.	ns
t_{HSTA}	0.5T – 30	MIN.	ns
t_{DAR}	T – 40	MIN.	ns
t_{DAID}	(2.5 + n) T – 90	MAX.	ns
t_{DRID}	(1.5 + n) T – 75	MAX.	ns
t_{DSTR}	0.5T – 20	MIN.	ns
t_{DRA}	0.5T – 25	MIN.	ns
t_{WRL}	(1.5 + n) T – 40	MIN.	ns
t_{WSTH}	0.5T – 25	MIN.	ns
t_{DAW}	T – 40	MIN.	ns
t_{DSTOD}	0.5T + 40	MAX.	ns
t_{DSTW}	0.5T – 20	MIN.	ns
t_{SODW}	1.5T – 50	MIN.	ns
t_{HWOD}	0.5T – 30	MIN.	ns
t_{DWST}	0.5T – 20	MIN.	ns
t_{WWL}	(1.5 + n) T – 40	MIN.	ns

Remarks 1. T = t_{CYK} = 1/f_{CLK} (f_{CLK} is the internal system clock frequency and is provided by dividing f_{XX} or f_X by two).

2. n is the number of wait cycles defined by user software.

3. Only parameters listed in the table are dependent on t_{CYK}.

Serial Operation (T_A = –10 to +70 °C, V_{DD} = +5 V ±5%, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	MAX.	Unit
Serial clock cycle time	t_{CYSK}	Input	External clock	1		μs
		Output	Internal divide by 8	8T		t_{CYK}
			Internal divide by 32	32T		t_{CYK}
Serial clock high-level width	t_{WSKL}	Input	External clock	420		ns
		Output	Internal divide by 8	4T–80		ns
			Internal divide by 32	16T–100		ns
Serial clock high-level width	t_{WSKH}	Input	External clock	420		ns
		Output	Internal divide by 8	4T–80		ns
			Internal divide by 32	16T–100		ns
SI setup time (to $\overline{SCK}$ ↑)	t_{SRXSK}			80		ns
SI hold time (from $\overline{SCK}$ ↑)	t_{HSKRX}			80		ns
SO/SB0, SI/SB1 output delay time (from $\overline{SCK}$ ↓)	t_{DSBSK1}	CMOS push-pull output (3-wire serial I/O mode)		0	210	ns
	t_{DSBSK2}	Open drain output (SBI mode), RL = 1 kΩ		0	600	ns
SB0, SB1 high hold time (from $\overline{SCK}$ ↑)	t_{HSBSK}	SBI mode		4T		t_{CYK}
SB0, SB1 low setup time (from $\overline{SCK}$ ↓)	t_{SSBSK}			4T		t_{CYK}
SB0, SB1 low-level width	t_{WSBL}			4T–20		ns
SB0, SB1 high-level width	t_{WBSH}			4T–20		ns

Remark T = t_{CYK} = 1/f_{CLK} (f_{CLK} is the internal system clock frequency and is provided by dividing f_{XX} or f_X by two.)

Other operations (T_A = –10 to +70°C, V_{DD} = +5 V±5%, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
NMI high-, low-level widths	t_{WNIH}, t_{WNIL}		5		μs
INTP0 high-, low-level widths	t_{WIOH}, t_{WIOL}		8T		t_{CYK}
INTP1 high-, low-level widths	t_{WI1H}, t_{WI1L}		8T		t_{CYK}
INTP2 high-, low-level widths	t_{WI2H}, t_{WI2L}		8T		t_{CYK}
$\overline{\text{RESET}}$ high-, low-level widths	t_{WRSH}, t_{WRSL}		5		μs
TI high-, low-level widths	t_{WTIH}, t_{WTIL}	TM1 In the event counter mode	8T		t_{CYK}

Remark T = t_{CYK} = 1/f_{CLK} (f_{CLK} is the internal system clock frequency and is provided by dividing f_{XX} or f_X by two.)

External clock timing (T_A = –10 to +70°C, V_{DD} = +5 V±5%, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
X1 input high-, low-level widths	t_{WXH}, t_{WXL}		25	80	ns
X1 input rise, fall times	t_{XR}, t_{XF}		0	20	ns
TI input cycle time	t_{CYK}		62	125	ns

A/D Converter (T_A = –10 to +70°C, V_{DD} = +5 V±5%, V_{SS} = AV_{SS} = 0 V, V_{DD} –0.5 V ≤ AV_{DD} ≤ V_{DD})

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Resolution				10			bit
Total error Note1		4.5 V ≤ AV_{REF} ≤ AV_{DD}				±0.4	%FSR
		3.4 V ≤ AV_{REF} ≤ AV_{DD}				±0.7	%FSR
Quantification error						±1/2	LSB
Conversion time	t_{CONV}			144			t_{CYK}
Sampling time	t_{SAMP}			24			t_{CYK}
Zero scale error Note1		4.5 V ≤ AV_{REF} ≤ AV_{DD}			+1.5	±2.5	LSB
		3.4 V ≤ AV_{REF} ≤ AV_{DD}			+1.5	±4.5	LSB
Fullscale error Note1		4.5 V ≤ AV_{REF} ≤ AV_{DD}			+1.5	±2.5	LSB
		3.4 V ≤ AV_{REF} ≤ AV_{DD}			+1.5	±4.5	LSB
Nonlinear error Note1		4.5 V ≤ AV_{REF} ≤ AV_{DD}			+1.5	±2.5	LSB
		3.4 V ≤ AV_{REF} ≤ AV_{DD}			+1.5	±4.5	LSB
Analog input voltage Note2	V_{IAN}			–0.3		AV_{DD}	V
Basic voltage	AV_{REF}			3.4		AV_{DD}	V
AV_{REF} current	AI_{REF}				1.0	3.0	mA
AV_{DD} supply current	AI_{DD}				2.0	6.0	mA
A/D converter data	AI_{DDDR}	STOP mode	AV_{DDDR} = 2.5 V		2.0	10	μA
retention current			AV_{DDDR} = 5 V±5%		10	50	μA

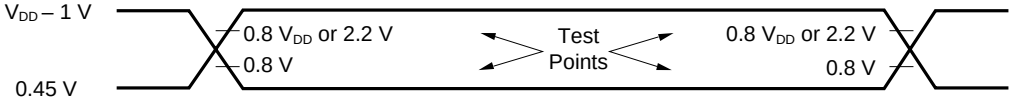
Notes 1. Quantization error is excluded.

2. When –0.3 V ≤ V_{IAN} ≤ 0 V, conversion result is 000H.
When 0 V < V_{IAN} < AV_{REF}, conversion is executed by 10-bit resolution.
When AV_{REF} ≤ V_{IAN} ≤ AV_{DD}, conversion result is 3 FFH.

Standby flag retention characteristics (T_A = –10°C to 70°C)

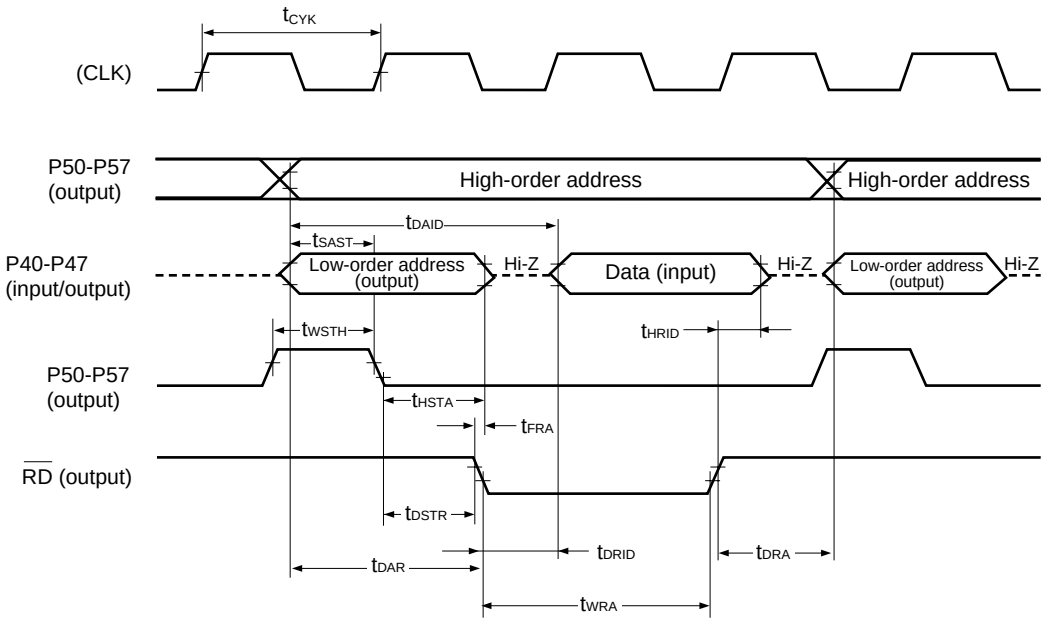
Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Standby flag retention power supply voltage	V_{DDDR}		2.5	5.5	V
V_{DD} rising, falling time	t_{RVD}, t_{FVD}		200		ns

AC Timing Test Points

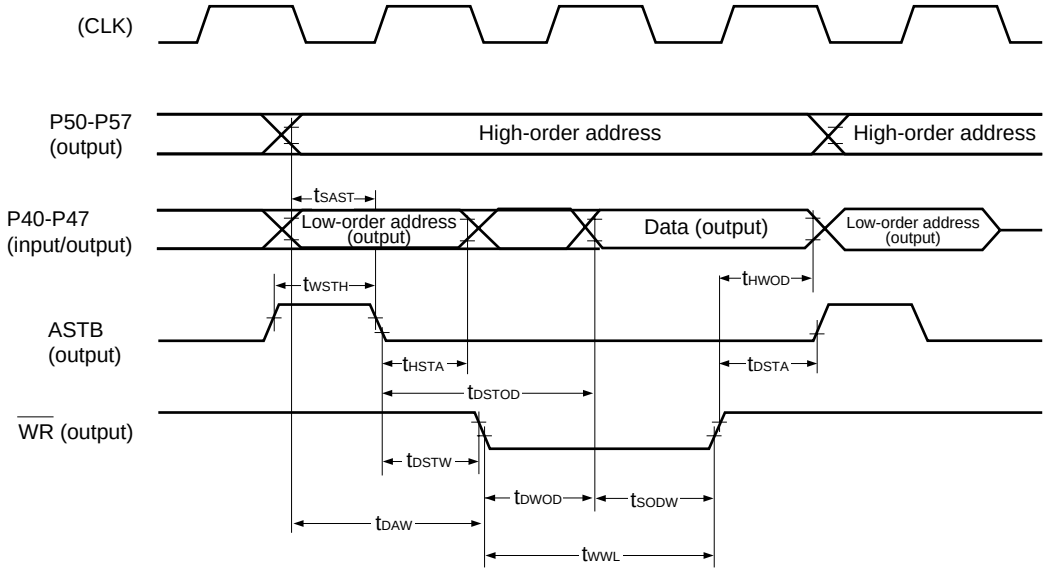


Timing Wave Forms

Discontinuous Read Operation

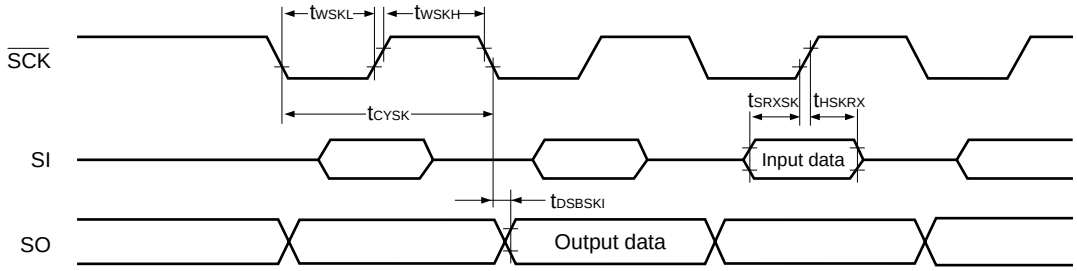


Discontinuous Write Operation



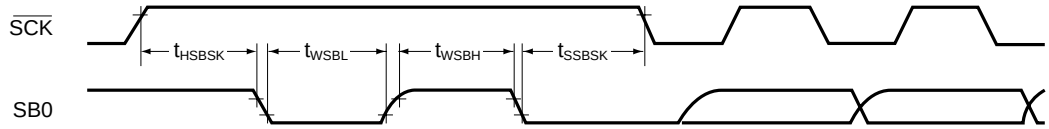
Serial Operation

Three-Wire Serial I/O Mode:

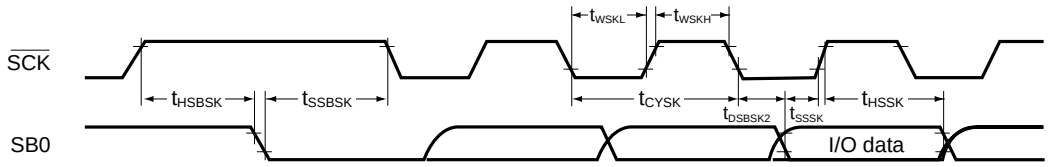


SBI Mode

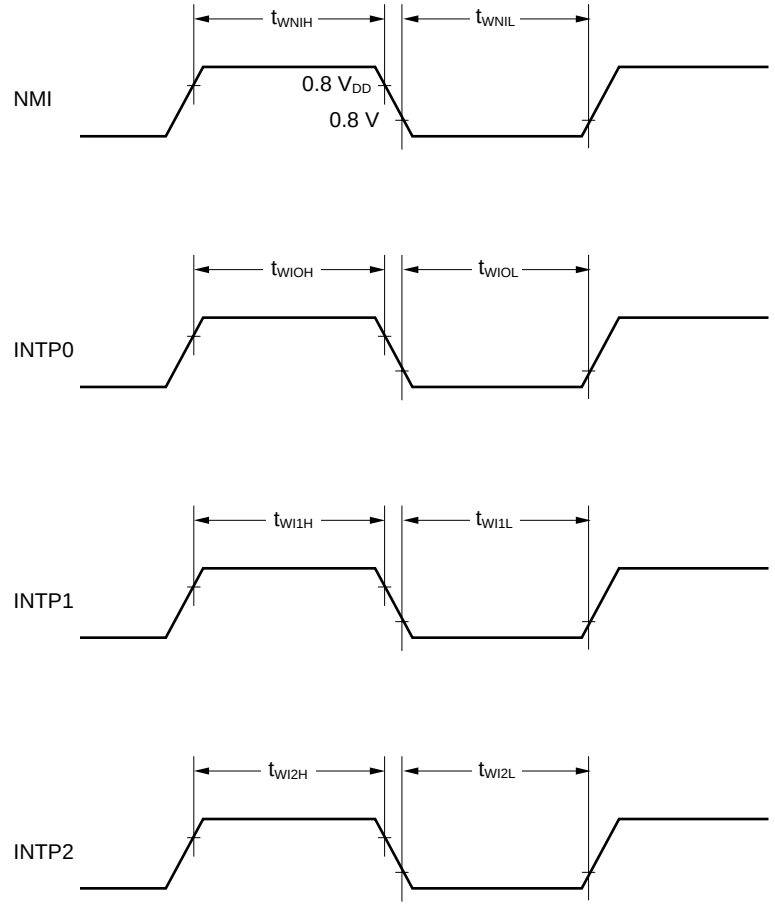
Bus Release Signal Transfer



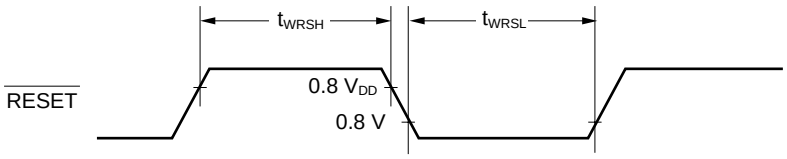
Command Signal Transfer



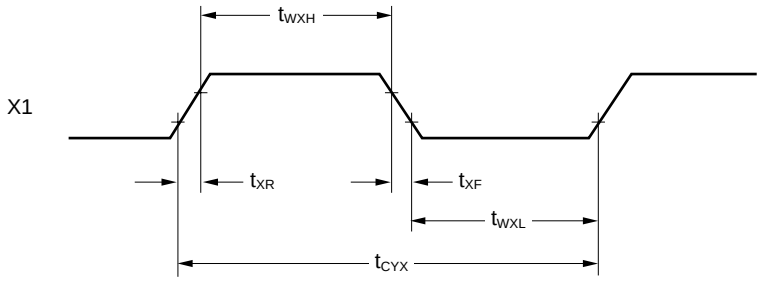
Interrupt Input Timing



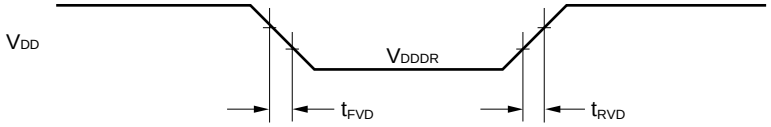
Reset Input Timing



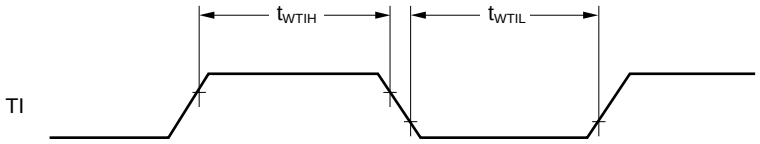
External Clock Timing



Standby Flag Retention Timing



TI Pin Input Timing



DC Programming Characteristics (T_A = 25 ± 5 °C, V_{SS} = 0 V)

Parameter	Symbol	Symbol Note1	Test conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	V_{IH}		2.2		V_{DDP} +0.3	V
Input voltage, low	V_{IL}	V_{IL}		–0.3		0.8	V
Input leakage current	I_{LIP}	I_{LI}	$0 \le V_I \le V_{DDP}$ Note 2			±10	μA
Output voltage, high	V_{OH}	V_{OH}	I_{OH} = –400 μA	2.4			V
Output voltage, low	V_{OL}	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Input current	I_{A9}	—	A9 (P20/NMI) pin			±10	μA
Output leakage current	I_{LO}	—	$0 \le V_O \le V_{DDP}$, $\overline{OE}$ = V_{IN}			10	μA
PROG pin high voltage input current	I_{IP}	—				±10	μA
V_{DDP} power supply voltage	V_{DDP}	V_{DD}	Program memory write mode	5.75	6.0	6.25	V
			Program memory read mode	4.5	5.0	5.5	V
V_{PP} power supply voltage	V_{PP}	V_{PP}	Program memory write mode	12.2	12.5	12.8	V
			Program memory read mode	V_{PP} = V_{DDP}			V
V_{DDP} power supply current	I_{DD}	I_{DD}	Program memory write mode		10	30	mA
			Program memory read mode $\overline{CE}$ = V_{IL}, OE = V_{IN}		10	30	mA
V_{PP} power supply current	I_{PP}	I_{PP}	Program memory write mode $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IN}		10	30	mA
			Program memory read mode		1	100	μA

Notes 1. Corresponding μPD27C256A symbols.

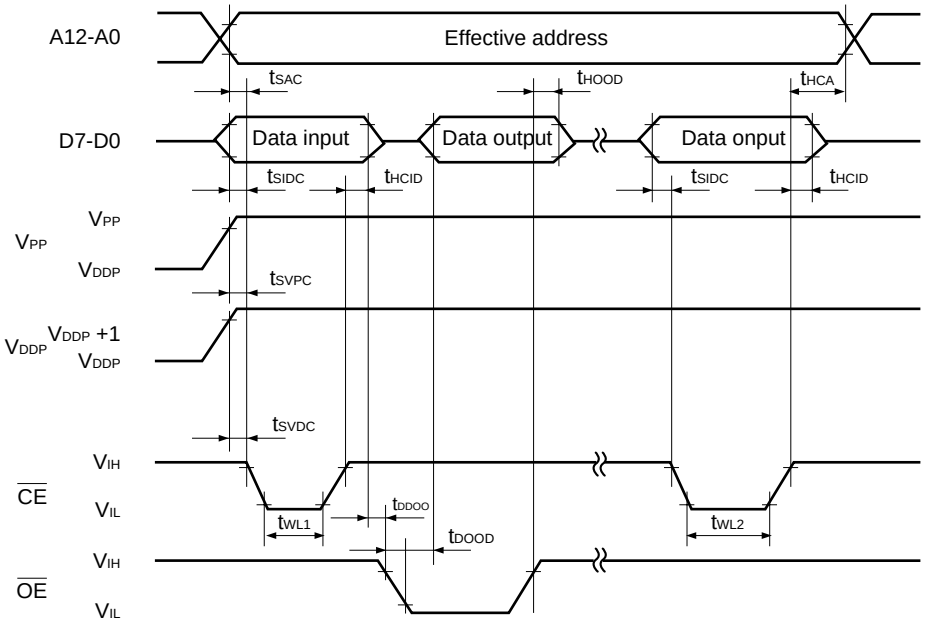
2. V_{DDP} is V_{DD} pin during the programming mode.

AC Programming Characteristics (T_A = 25 ± 5 °C, V_{SS} = 0 V)

Parameter	Symbol	Symbol Note	Test conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{CE}$ ↓)	t_{SAC}	t_{AS}		2			μs
Data → $\overline{OE}$ ↓ delay time	t_{DDOO}	t_{OES}		2			μs
Input data setup time (to $\overline{CE}$ ↓)	t_{SIDC}	t_{DS}		2			μs
Address hold time (from $\overline{CE}$ ↑)	t_{HCA}	t_{AH}		2			μs
Input data hold time (from $\overline{CE}$ ↑)	t_{HCID}	t_{DH}		2			μs
Output data hold time (from $\overline{OE}$ ↑)	t_{HOOD}	t_{DF}		0		130	ns
V_{PP} setup time (to $\overline{CE}$ ↓)	t_{SVPC}	t_{VPS}		2			μs
V_{DDP} setup time (to $\overline{CE}$ ↓)	t_{SVDC}	t_{VDS}		2			μs
Initial program pulse width	t_{WL1}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{WL2}	t_{OPW}		2.85		78.75	ms
Address → data output time	t_{DAOD}	t_{ACC}	$\overline{OE}$ = V_{IL}			2	μs
$\overline{OE}$ ↓ → data output time	t_{DOOD}	t_{OE}				1	μs
Data hold time (from $\overline{OE}$ ↑)	t_{HCOD}	t_{DF}		0		130	ns
Data hold time (from address)	t_{HAOD}	t_{OH}	$\overline{OE}$ = V_{IL}	0			ns

Note Corresponding μPD27C256A symbols.

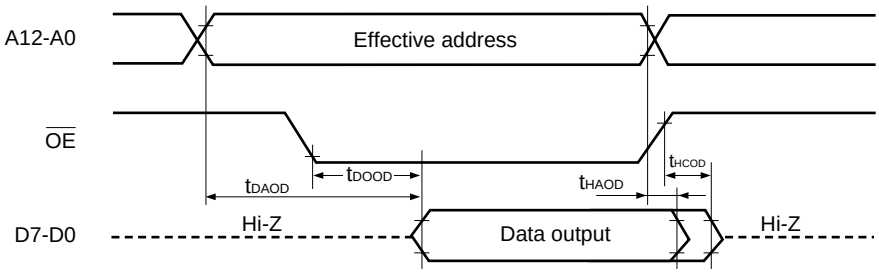
PROM Write Mode Timing



Cautions 1. Apply V_{DDP} before V_{PP} and remove it after V_{PP}.

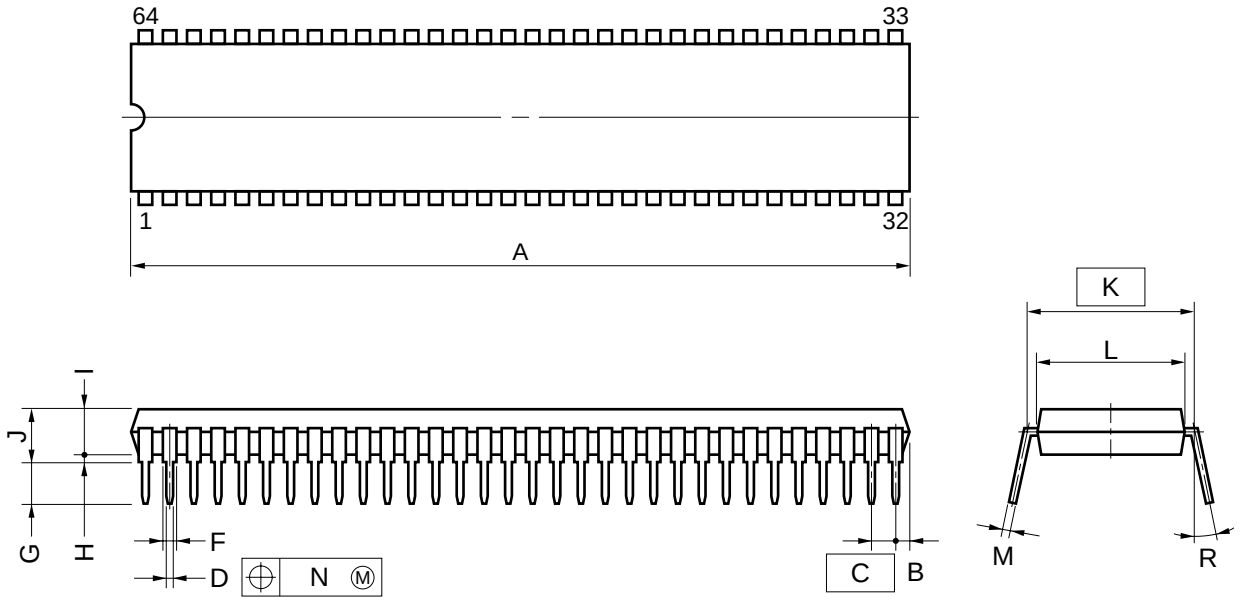
2. V_{PP} must not exceed +13 V, including the overshoot.

PROM Read Mode Timing



8. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



NOTE

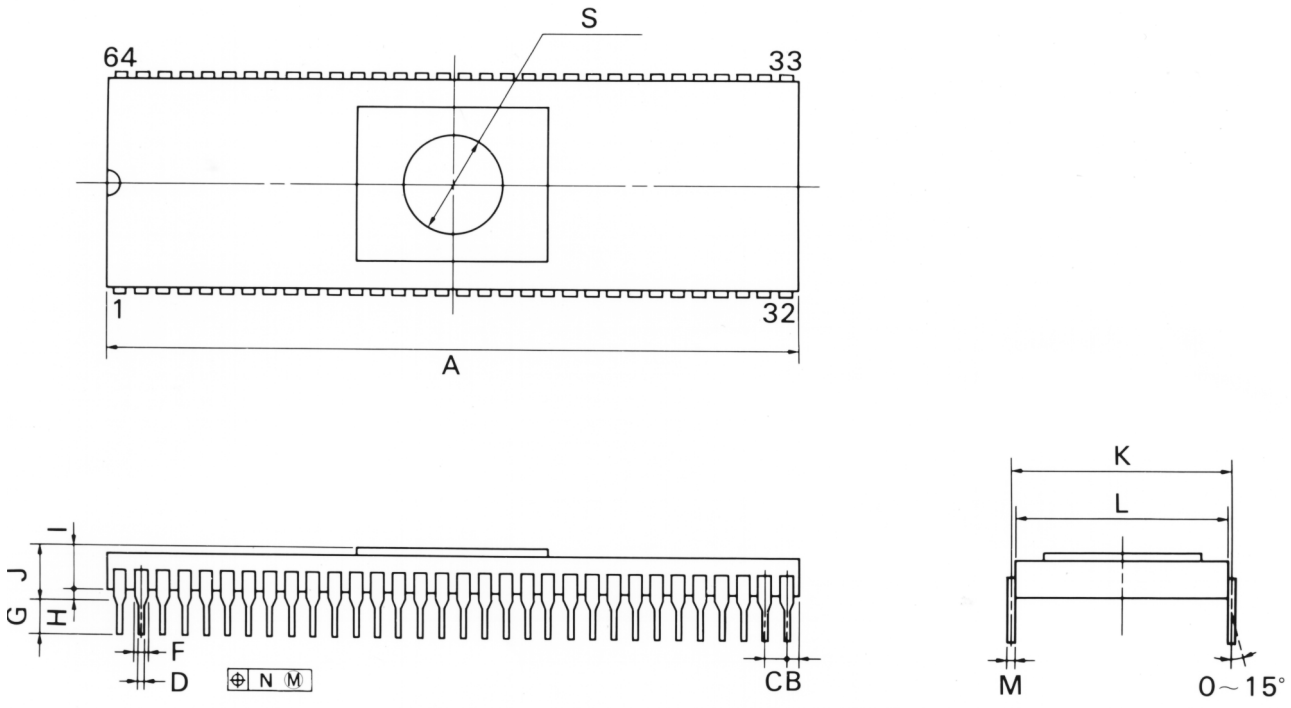
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

64PIN CERAMIC SHRINK DIP (750 mil)



P64DW-70-750A

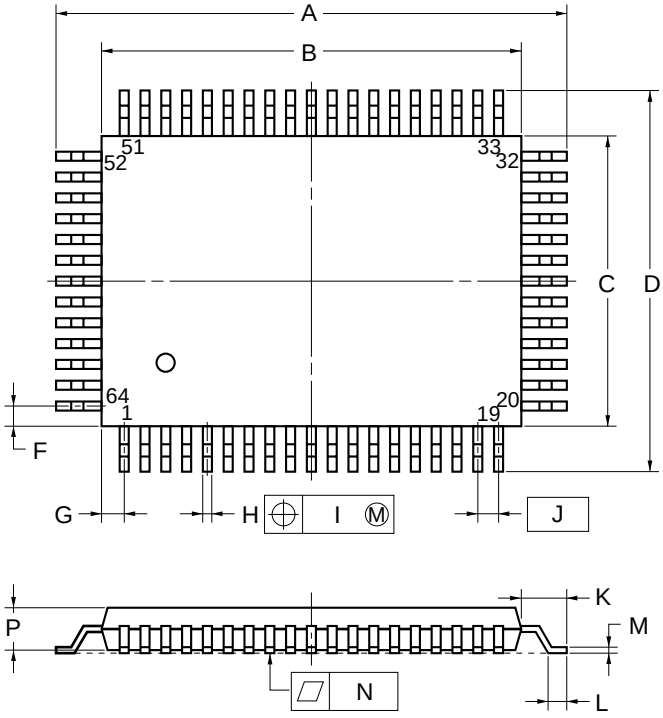
NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

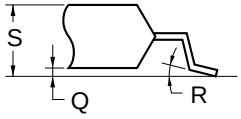
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.310 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.46^{\pm 0.05}$	$0.018^{\pm 0.002}$
F	0.8 MIN.	0.031 MIN.
G	$3.5^{\pm 0.3}$	$0.138^{\pm 0.012}$
H	1.0 MIN.	0.039 MIN.
I	3.0	0.118
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	18.8	0.740
M	$0.25^{\pm 0.05}$	$0.010^{+0.002}_{-0.003}$
N	0.25	0.01
S	ϕ8.89	ϕ0.350

64 PIN PLASTIC QFP (14×20)



detail of lead end



NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.008}_{-0.009}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P64GF-100-3B8,3BE,3BR-2

9. RECOMMENDED SOLDERING CONDITIONS *

It is recommended that this device be soldered under the following conditions.

For details on the recommended soldering conditions, refer to information document **"Semiconductor Devices Mounting Technology Manual" (IEI-1207)**.

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

Table 9-1. Soldering Conditions for Surface Mount Devices

μPD78P328GF-3BE: 64-pin plastic QFP (14 x 20 mm)

Soldering Method	Soldering Conditions	Recommended Soldering Code
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (210°C min.), Number of times: 2 max, Maximum number of days: 7 days[Note] (thereafter, 20 hours of prebaking is required at 125°C) < Cautions > (1) Wait for the device temperature to return to normal after the first reflow before starting the second reflow. (2) Do not perform flux cleaning with water after the first reflow.	IR35-207-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (200°C min.), Number of times: 2 max, Maximum number of days: 7 days[Note] (thereafter, 20 hours of prebaking is required at 125°C) < Cautions > (1) Wait for the device temperature to return to normal after the first reflow before starting the second reflow. (2) Do not perform flux cleaning with water after the first reflow.	VP15-207-2
Wave soldering	Soldering bath temperature: 260°C max., Time: 10 seconds max., Number of times: 1, Preheating temperature: 120°C max. (package surface temperature), Maximum number of days: 7 days[Note] (thereafter, 20 hours of prebaking is required at 125°C).	WS60-207-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Note Number of days after unpacking the dry pack. Storage conditions are 25°C and 65% RH max.

Caution Do not use different soldering methods together (except the partial heating method).

Table 9-2. Soldering Conditions for Through-hole Devices

μPD78P328CW: 64-pin Plastic Shrink DIP (750 mils)
μPD78P328DW: 64-pin Ceramic Shrink DIP (750 mils) (with window)

Soldering Method	Soldering Conditions
Wave soldering (pin only)	Soldering bath temperature: 260°C max., Time: 10 seconds max.
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin)

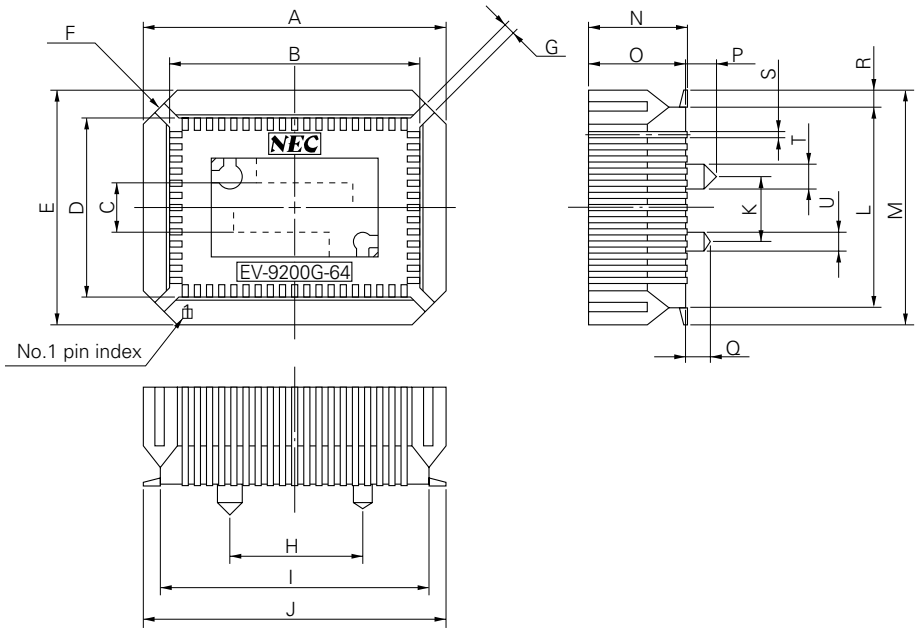
Caution Apply wave soldering only to the pins and be careful so as not to bring solder into direct contact with the package.

APPENDIX A. DRAWINGS OF CONVERSION SOCKET AND RECOMMENDED FOOTPRINT

* The emulation probe (EP-78327GF-R) for the μPD78P328GF-3BE is connected with the target system in combination with the conversion socket (EV-9200G-64).

The drawings of the socket and recommended footprint are shown below.

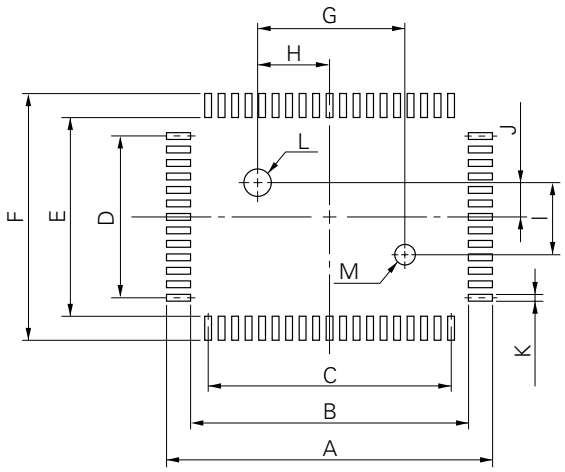
Figure A-1. Drawing of Conversion Socket (EV-9200G-64)
(for reference only)



EV-9200G-64-G0

ITEM	MILLIMETERS	INCHES
A	25.0	0.984
B	20.30	0.799
C	4.0	0.157
D	14.45	0.569
E	19.0	0.748
F	4-C 2.8	4-C 0.11
G	0.8	0.031
H	11.0	0.433
I	22.0	0.866
J	24.7	0.972
K	5.0	0.197
L	16.2	0.638
M	18.9	0.744
O	8.0	0.315
N	7.8	0.307
P	2.5	0.098
Q	2.0	0.079
R	1.35	0.053
S	0.35±0.1	$0.014^{+0.004}_{-0.005}$
T	φ2.3	φ0.091
U	φ1.5	φ0.059

Figure A-2. Recommended Footprint for EV-9200G-64 (for reference only)



EV-9200G-64-P0

ITEM	MILLIMETERS	INCHES
A	25.7	1.012
B	21.0	0.827
C	1.0±0.02 × 18=18.0±0.05	$0.039^{+0.002}_{-0.001}\times 0.709=0.709^{+0.002}_{-0.003}$
D	1.0±0.02 × 12=12.0±0.05	$0.039^{+0.002}_{-0.001}\times 0.472=0.472^{+0.003}_{-0.002}$
E	15.2	0.598
F	19.9	0.783
G	11.00±0.08	$0.433^{+0.004}_{-0.003}$
H	5.50±0.03	$0.217^{+0.001}_{-0.002}$
I	5.00±0.08	$0.197^{+0.003}_{-0.004}$
J	2.50±0.03	$0.098^{+0.002}_{-0.001}$
K	0.6±0.02	$0.024^{+0.001}_{-0.002}$
L	φ2.36±0.03	$\phi 0.093^{+0.001}_{-0.002}$
M	φ1.57±0.03	$\phi 0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

* APPENDIX B. TOOLS

B.1 Development Tools

The following development tools are readily available to support development of systems using the μPD78P328:

Language Processor

78K/III Series relocatable assembler (RA78K/III)	Relocatable assembler common to the 78K/III series. Since it contains the macro function, the development efficiency can be improved. A structured assembler which enables you to explicity describe program control structure is also attached and program productivity and maintenance can be improved.			
	Host machine			Ordering code
		OS	Supply medium	(product name)
	PC-9800 series	MS-DOS™	3.5-inch 2HD	μS5A13RA78K3
			5-inch 2HD	μS5A10RA78K3
	IBM PC/AT™ and compatible machine	PC DOS™	3.5-inch 2HC	μS7B13RA78K3
			5-inch 2HC	μS7B10RA78K3
	HP9000 series 700™	HP-UX™	DAT	μS3P16RA78K3
	SPARCstation™	SunOS™	Cartridge tape	μS3K15RA78K3
	NEWS™	NEWS-OS™	(QIC-24)	μS3R15RA78K3
78K/III Series C compiler (CC78K/III)	C compiler common to the 78K/III series. This is a program to convert a program written in C language into an object code executable with a microcontroller. When using the compiler, 78K/III series relocatable assembler(RA78K/III) is necessary.			
	Host machine			Ordering code
		OS	Supply medium	(product name)
	PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13CC78K3
			5-inch 2HD	μS5A10CC78K3
	IBM PC/AT™ and compatible machine	PC DOS	3.5-inch 2HC	μS7B13CC78K3
			5-inch 2HC	μS7B10CC78K3
	HP9000 series 700	HP-UX	DAT	μS3P16CC78K3
	SPARCstation	SunOS	Cartridge tape	μS3K15CC78K3
	NEWS	NEWS-OS	(QIC-24)	μS3R15CC78K3

Remark The operation of the relocatable assembler and C compiler is guaranteed only on the host machine under the operating systems listed above.

PROM Write Tools

Hard-ware	PG-1500	PG-1500 is a PROM programmer which enables you to program single chip micro-controllers containing PROM by stand-alone or host machine operation by connecting an attached board and optional programmer adapter to PG-1500. It also enables you to program typical PROM devices of 256K bits to 4M bits.			
	UNISITE 2900	PROM programmer manufactured by Data I. O. Japan.			
	PA-78P328CW PA-78P328GF	PROM programmer adapters to write programs onto the μPD78P328 on a general purpose PROM programmer such as PG-1500. PA-78P328CW ... μPD78P328CW and 78P328DW PA-78P328GF ... μPD78P328GF			
Soft-ware	PG-1500 controller	Connects PG-1500 and a host machine by a serial or parallel interface and controlls PG-1500 on the host machine.			
		Host machine			Ordering code
			OS	Supply medium	(product name)
		PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13PG1500
				5-inch 2HD	μS5A10PG1500
		IBM PC/AT and compatible machine	PC DOS	3.5-inch 2HD	μS7B13PG1500
				5-inch 2HC	μS7B10PG1500

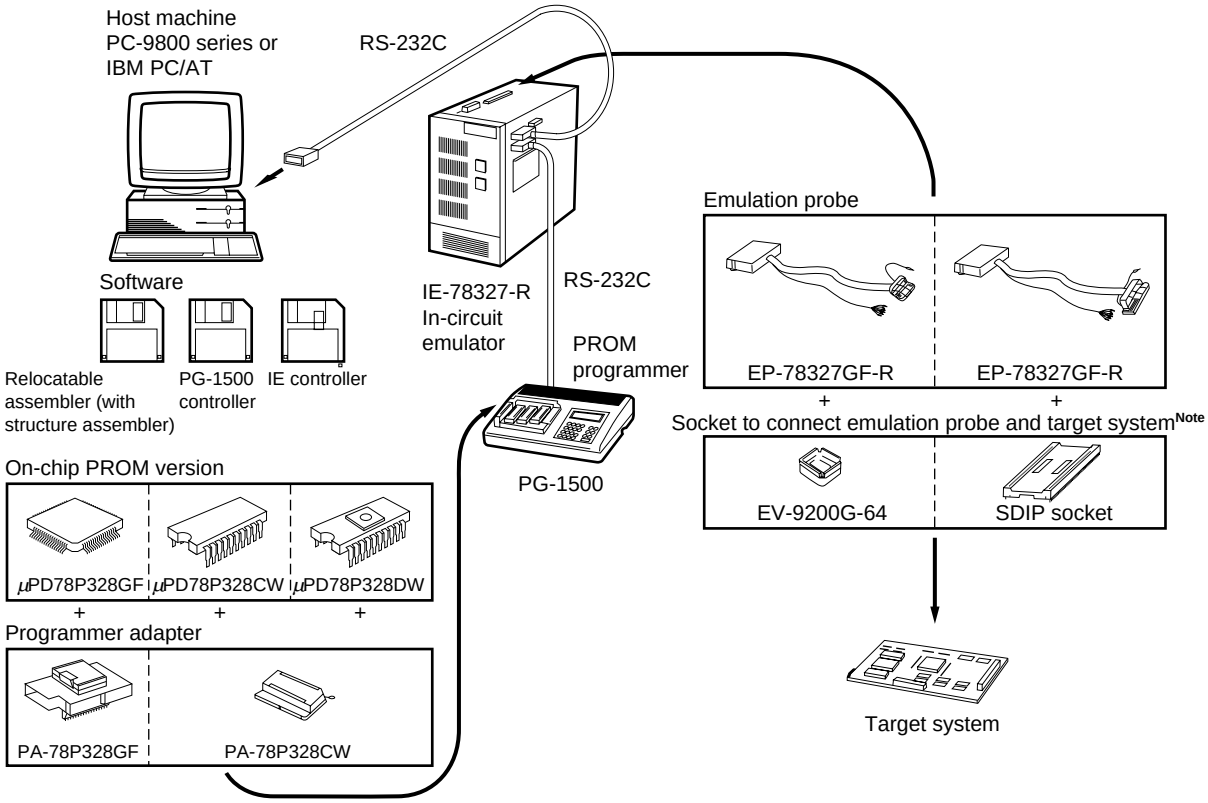
Remark The operation of the PG-1500 controller is guaranteed only on the host machine under the operating systems listed above.

Debugging Tools

Hard-ware	IE-78327-R	IE-78327-R is an in-circuit emulator that can be used for application system development and debugging.			
	EP-78327CW-R	Emulation probe for 64-pin plastic shrink DIP to connect IE-78327-R to the target system.			
	EP-78327GF-R	Emulation probe for 94-pin plastic QFP to connect IE-78327-R to the target system.			
	EV-9200G-64	One conversion socket EV-9200G-64 used for connection to the target system is attached.			
Soft-ware	IE-78327-R control program (IE controller)	Program to control IE-78327-R on a host machine. Automatic execution of commands, etc., is enabled for more efficient debugging.			
		Host machine			Ordering code
			OS	Supply medium	(product name)
		PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13IE78327
				5-inch 2HD	μS5A10IE78327
		IBM PC/AT and compatible machine	PC DOS	3.5-inch 2HD	μS7B13IE78327
				5-inch 2HC	μS7B10IE78327

Remark The operation of the IE controller is guaranteed only on the host machine under the operating systems listed above.

Development Tool Configuration



Note The socket is attached to the emulation probe.

Remarks 1. The host machine and PG-1500 can be connected directly by RS-232-C.

2. Supply media of software are represented as 3.5-inch floppy disks in the figure above.

B.2 Evaluation Tools

The following evaluation tools are provided to evaluate the μPD78P328 function:

Ordering Code (product name)	Host Machine	Function
EB-78327-98	PC-9800 series	The μPD78P328 function can be easily evaluated by connecting the evaluation tool to a host machine. The EB-78327-98/PC command system basically is compliant with the IE-78327-R command system. Thus, easy transition to application system development process by IE-78327-R can be made. The evaluation tools enable turbo access manager (μPD71P301)Note to be mounted on the printed circuit board.
EB-78327-PC	IBM PC/AT and compatible machine	

Note Turbo access manager (μPD71P301) is available for maintenance purpose only.

Cautions 1. EB-78327-98/PC is not the μPD78P328 application system development tool.

2. EB-78327-98/PC does not contain the emulation function at internal PROM execution of the μPD78P328.

B.3 Embedded Software

The following embedded software products are readily available to support more efficient program development and maintenance:

Real-time OS

Real-time OS (RX78K/III)	The purpose of RX78K/III is to realize a multi-task environment in a control area which requires real-time processing. RX78K/III allocates idle times of CPU to other processing to improve overall performance of the system. RX78K/III provides a system call based on the μITRON specification. RX78K/III assembler package provides the RX78K/III nucleus and a tool (configurator) to prepare multiple information tables.			
	Host machine			Ordering code (product name)
		OS	Supply medium	
	PC-9800 series	MS-DOS	3.5-inch 2HD	μS5A13RX78320
			5-inch 2HD	μS5A10RX78320
	IBM PC/AT and compatible machine	PC DOS	3.5-inch 2HC	μS7B13RX78320
			5-inch 2HC	μS7B10RX78320

Caution When purchasing the RX78K/III, fill in the purchase application form in advance, and sign the User's Agreement.

Remark When using the RX78K/III Real-time OS, the RA78K/III assembler package (option) is necessary.

Fuzzy Inference Development Support System

Fuzzy knowledge Data Preparation Tool (FE9000, FE9200)	Program supporting input of fuzzy knowledge data (fuzzy rule and membership function), input/editing (edit), and evaluation (simulation).				
	Host machine				Ordering code
		OS		Supply medium	(product name)
	PC-9800 series	MS-DOS		3.5-inch 2HD	μS5A13FE9000
				5-inch 2HD	μS5A10FE9000
	IBM PC/AT and compatible machine	PC DOS	Windows™	3.5-inch 2HC	μS7B13FE9200
				5-inch 2HC	μS7B10FE9200
Translator (FT78K3)Note	Program converting fuzzy knowledge data obtained by using fuzzy knowledge data preparation tool to the assembler source program for the RA78K/III.				
	Host machine				Ordering code
		OS		Supply medium	(product name)
	PC-9800 series	MS-DOS		3.5-inch 2HD	μS5A13FT78K3
				5-inch 2HD	μS5A10FT78K3
	IBM PC/AT and compatible machine	PC DOS		3.5-inch 2HC	μS7B13FT78K3
				5-inch 2HC	μS7B10FT78K3
Fuzzy Inference Module (FI78K/III)Note	Program executing fuzzy inference. Fuzzy inference is executed by linking fuzzy knowledge data converted by translator.				
	Host machine				Ordering code
		OS		Supply medium	(product name)
	PC-9800 series	MS-DOS		3.5-inch 2HD	μS5A13FI78K3
				5-inch 2HD	μS5A10FI78K3
	IBM PC/AT and compatible machine	PC DOS		3.5-inch 2HC	μS7B13FI78K3
				5-inch 2HC	μS7B10FI78K3
Fuzzy Inference Debugger (FD78K/III)	Support software evaluating and adjusting fuzzy knowledge data at hardware level by using in-circuit emulator.				
	Host machine				Ordering code
		OS		Supply medium	(product name)
	PC-9800 series	MS-DOS		3.5-inch 2HD	μS5A13FD78K3
				5-inch 2HD	μS5A10FD78K3
	IBM PC/AT and compatible machine	PC DOS		3.5-inch 2HC	μS7B13FD78K3
				5-inch 2HC	μS7B10FD78K3

Note Under development

[MEMO]

NOTES FOR CMOS DEVICES

(1) PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

(2) HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

(3) STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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License not needed: μPD78P328DW
The customer must judge the need for license: μPD78P328CW, 78P328GF-3BE

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