

## 8 BIT SINGLE-CHIP MICROCOMPUTER

The  $\mu$ PD78P238 is an 8-bit single-chip microcomputer produced by replacing the mask ROM in the  $\mu$ PD78238 with one-time PROM or EPROM. Since a user program can be written on the one-time PROM or EPROM, this microcomputer is suitable for the evaluation of the system to be developed and small production.

The following user's manual describes the details of the functions of the  $\mu$ PD78P238. Be sure to read it before designing an application system.

$\mu$ PD78234 Series User's Manual, Hardware: IEU-718

78K/II Series User's Manual, Instruction : IEU-754

## FEATURES

- Compatible with the  $\mu$ PD78234 or the  $\mu$ PD78238
- Built-in EPROM
  - $\mu$ PD78P238KF : Reprogrammable (suitable for system evaluation)
  - $\mu$ PD78P238GC/GJ/LQ: Programmable only once (suitable for small production)
  - QTOP™ microcomputer

**Remark** The QTOP microcomputer is a single-chip microcomputer with a built-in one-time PROM that is totally supported by NEC. The support includes writing application programs, marking, screening, and verification. ★

## ORDERING INFORMATION

Part number	Package	Internal ROM	
$\mu$ PD78P238GC-3B9	80-pin plastic QFP (14 × 14 mm)	One-time PROM	
$\mu$ PD78P238GC-xxx-3B9	80-pin plastic QFP (14 × 14 mm)	One-time PROM (QTOP microcomputer)	★
$\mu$ PD78P238GJ-5BG	94-pin plastic QFP (20 × 20 mm)	One-time PROM	
$\mu$ PD78P238GJ-xxx-5BG	94-pin plastic QFP (20 × 20 mm)	One-time PROM (QTOP microcomputer)	★
$\mu$ PD78P238LQ	84-pin plastic QFJ (1150 × 1150 mil)	One-time PROM	
$\mu$ PD78P238LQ-xxx	84-pin plastic QFJ (1150 × 1150 mil)	One-time PROM (QTOP microcomputer)	★
$\mu$ PD78P238KF	94-pin ceramic WQFN (20 × 20 mm)	EPROM	

**Remark** xxx: ROM code number

## QUALITY GRADE

Standard

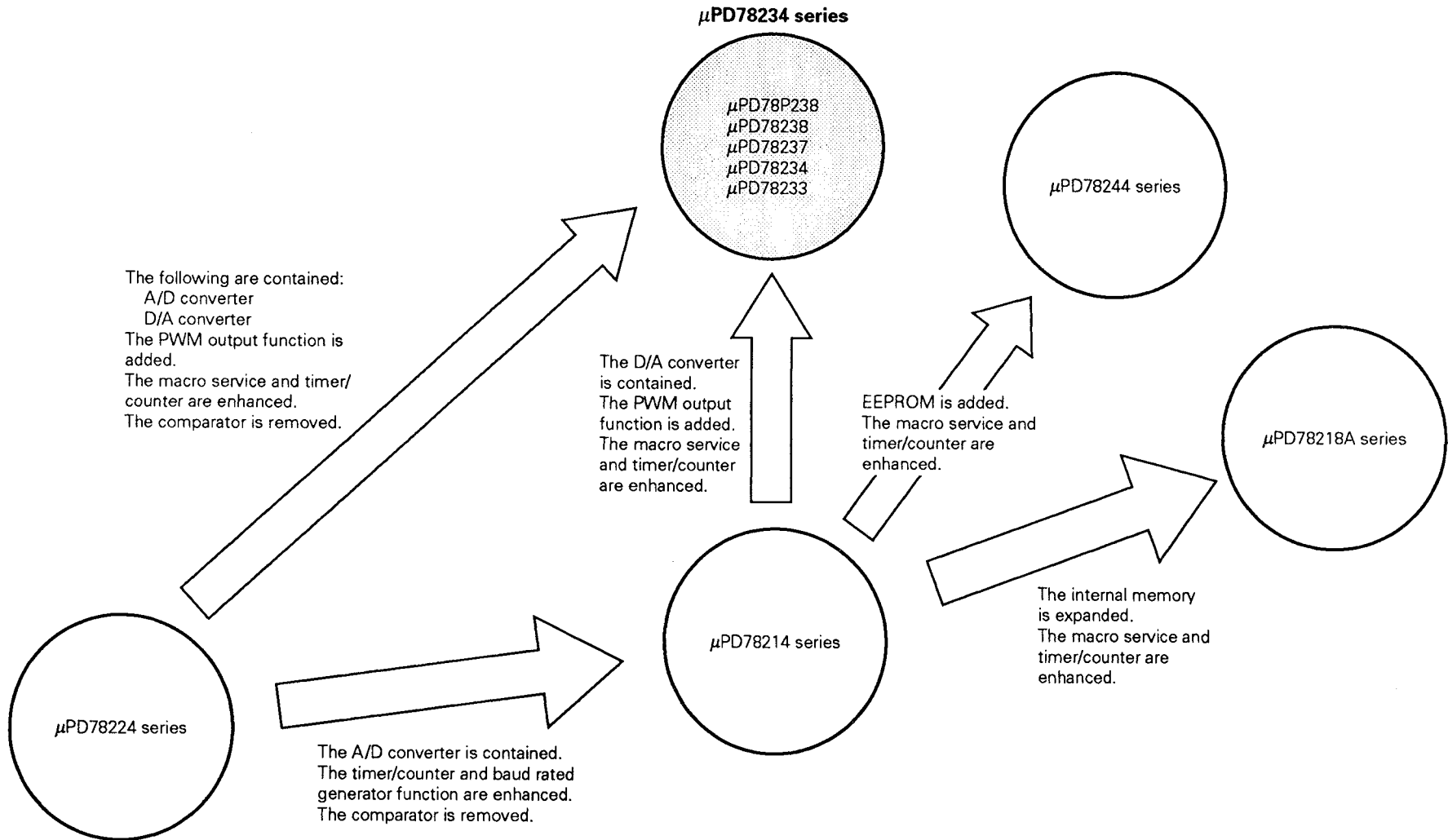
Please refer to *Quality Grades on NEC Semiconductor Devices* (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

In this document, the word "PROM" refers to both one-time PROM and EPROM.

The information in this document is subject to change without notice.

Major changes in this revision are indicated by stars (★) in the margins.

### DIAGRAM OF 78K/II PRODUCT DEVELOPMENT



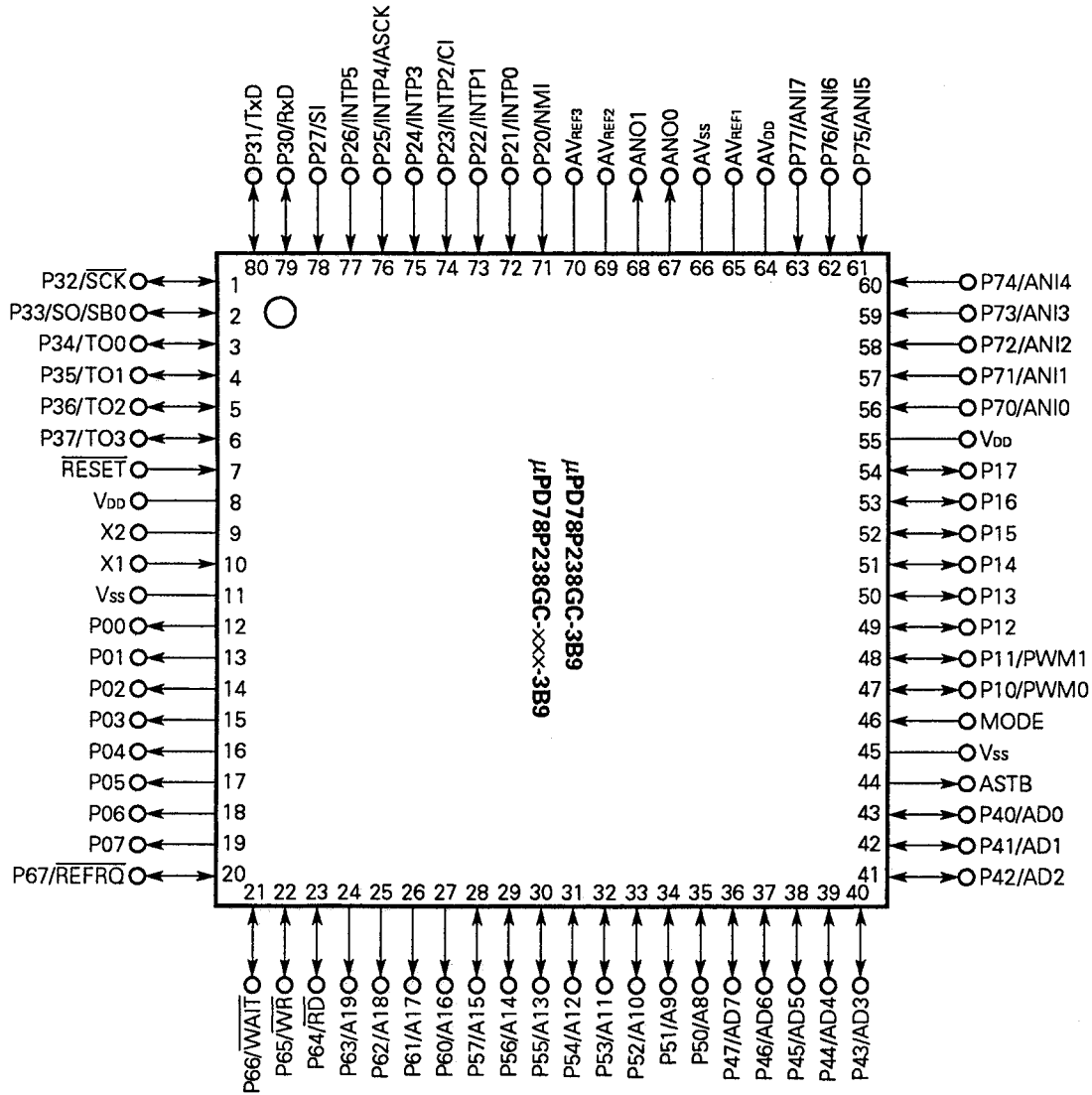
FUNCTIONS

Item	Function
Number of basic instructions (mnemonics)	65
Minimum instruction execution time	333 ns (at 12 MHz)
Internal memory size	PROM 32K bytes
	RAM 1024 bytes
Address space	1M bytes
Number of I/O pins	Input ports : 16 } Pull-up resistor provided I/O ports : 36 } (to be specified by software): 42 inputs LED operable : 24 outputs Transistor operable: 8 outputs Output ports : 12
General register	8 bits × 8 × 4 banks (memory mapping)
Timer/counter	16-bit timer/counter Pulse output possible { Timer register × 1 (Toggled output) Capture register × 1 (PWM/PPG output) Compare register × 2 (One-shot pulse output)
	8-bit timer/counter 1 Pulse output possible { Timer register × 1 (Real-time output: Capture/compare register × 1 4 bits × 2) Compare register × 1
	8-bit timer/counter 2 Pulse output possible { Timer register × 1 (Toggled output) Capture register × 1 (PWM/PPG output) Compare register × 2
	8-bit timer/counter 3 { Timer register × 1 Compare register × 1
PWM output function	12-bit resolution × 2 channels
Serial interface	UART : 1 channel (baud rate generator contained) Clock synchronous serial I/O : 1 channel
A/D converter	8-bit resolution × 8 channels
D/A converter	8-bit resolution × 2 channels
Interrupt function	19 sources (external: 7, internal: 12) and BRK instruction 2 priority levels (programmable) Two types of interrupt processing modes (vectored interrupt function and macro service function)
Instruction set	16-bit arithmetic/logical instructions Multiply/divide instructions (8 bits × 8 bits, 16 bits + 8 bits) Bit manipulation instructions BCD correction instructions, etc.
Package	94-pin ceramic WQFN (20 × 20 mm) 80-pin plastic QFP (14 × 14 mm) 94-pin plastic QFP (20 × 20 mm) 84-pin plastic QFJ (1150 × 1150 mil)

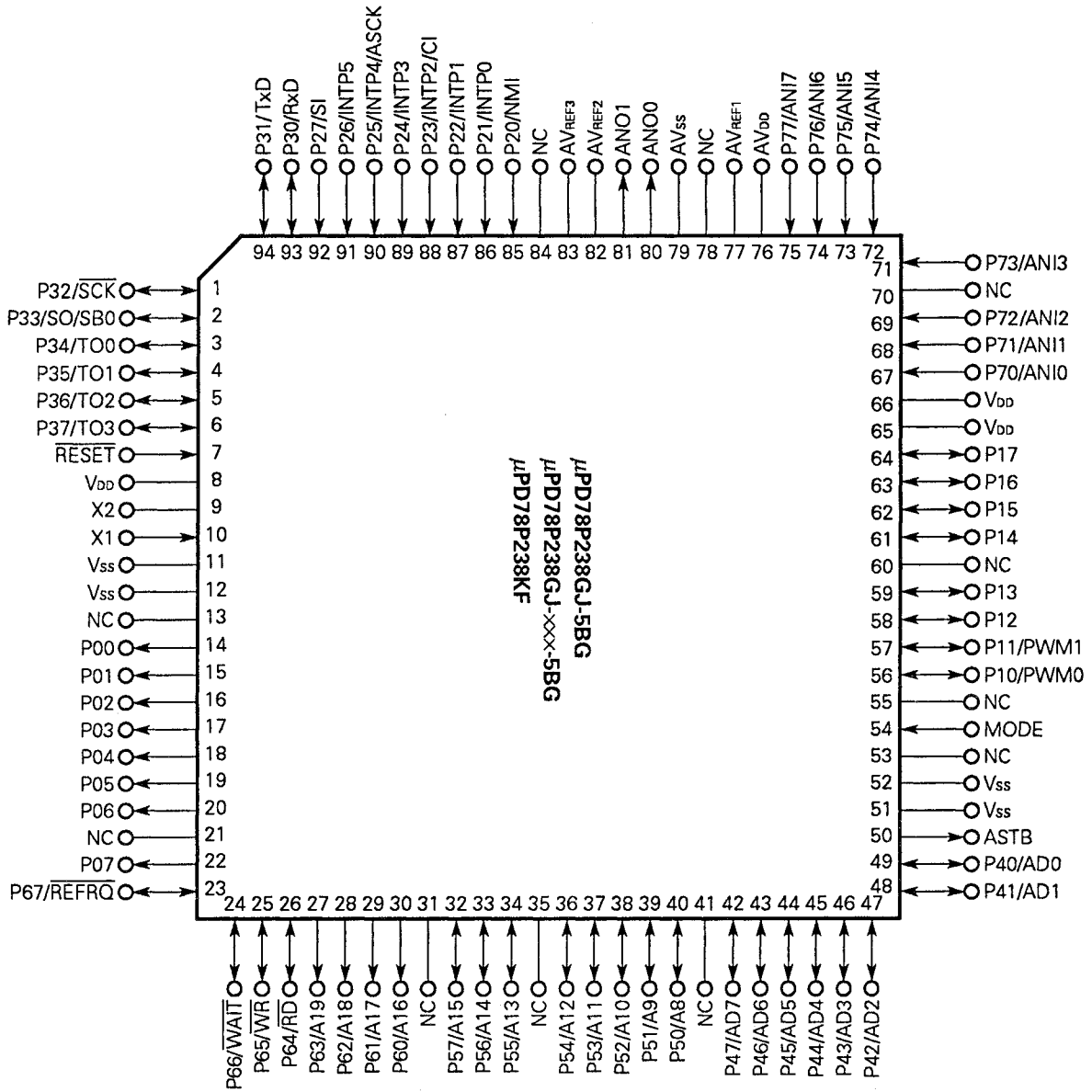
PIN CONFIGURATION (TOP VIEW)

(1) Normal operation mode

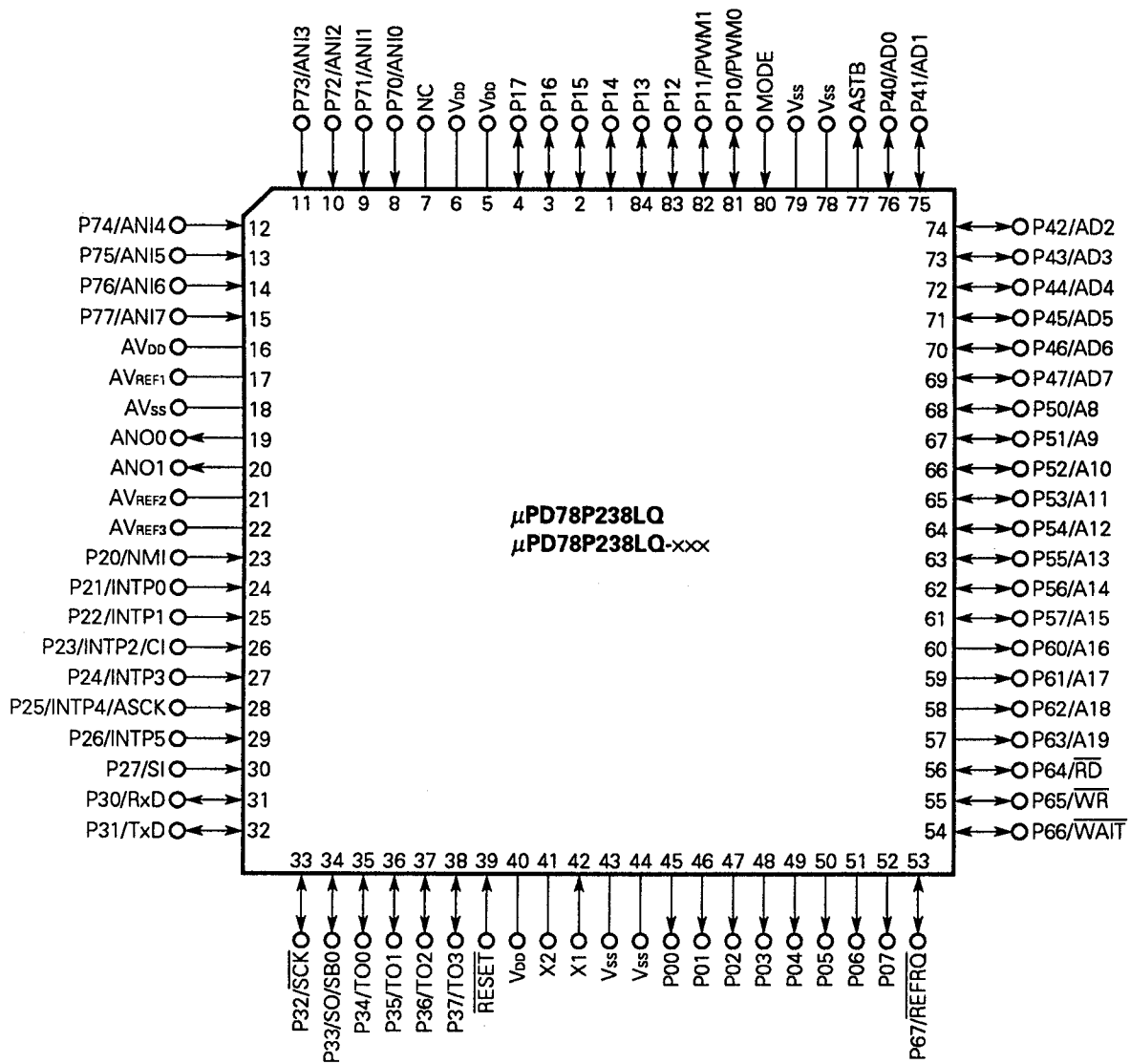
80-pin plastic QFP (14 × 14 mm)



94-pin plastic QFP (20 × 20 mm)  
 94-pin ceramic WQFN (20 × 20 mm)



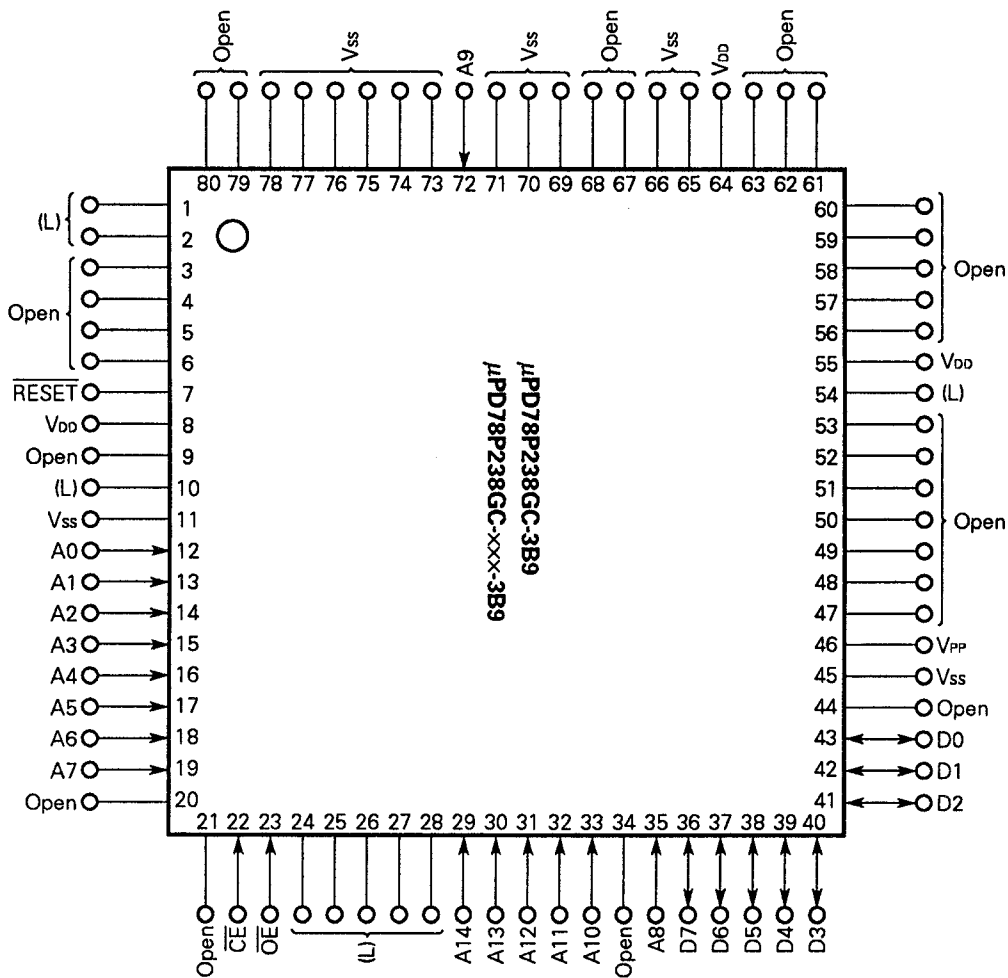
84-pin plastic QFJ (1150 × 1150 mil)



P00-P07	: Port 0	A8-A19	: Address bus
P10-P17	: Port 1	$\overline{RD}$	: Read strobe
P20-P27	: Port 2	$\overline{WR}$	: Write strobe
P30-P37	: Port 3	$\overline{WAIT}$	: Wait
P40-P47	: Port 4	$\overline{ASTB}$	: Address strobe
P50-P57	: Port 5	$\overline{REFRQ}$	: Refresh request
P60-P67	: Port 6	$\overline{RESET}$	: Reset
P70-P77	: Port 7	X1, X2	: Crystal
TO0-TO3	: Timer output	MODE	: Mode
CI	: Clock input	ANI0-ANI7	: Analog input
RxD	: Receive data	ANO0, ANO1	: Analog output
TxD	: Transmit data	$AV_{REF1}$ - $AV_{REF3}$	: Reference voltage
$\overline{SCK}$	: Serial clock	$AV_{DD}$	: Analog power supply
ASCK	: Asynchronous serial clock	$AV_{SS}$	: Analog ground
SB0	: Serial bus	$V_{DD}$	: Power supply
SI	: Serial input	$V_{SS}$	: Ground
SO	: Serial output	NC	: No connection
PWM0, PWM1	: Pulse width modulation output		
NMI	: Non-maskable interrupt		
INTP0-INTP5	: Interrupt from peripherals		
AD0-AD7	: Address/data bus		

(2) PROM programming mode

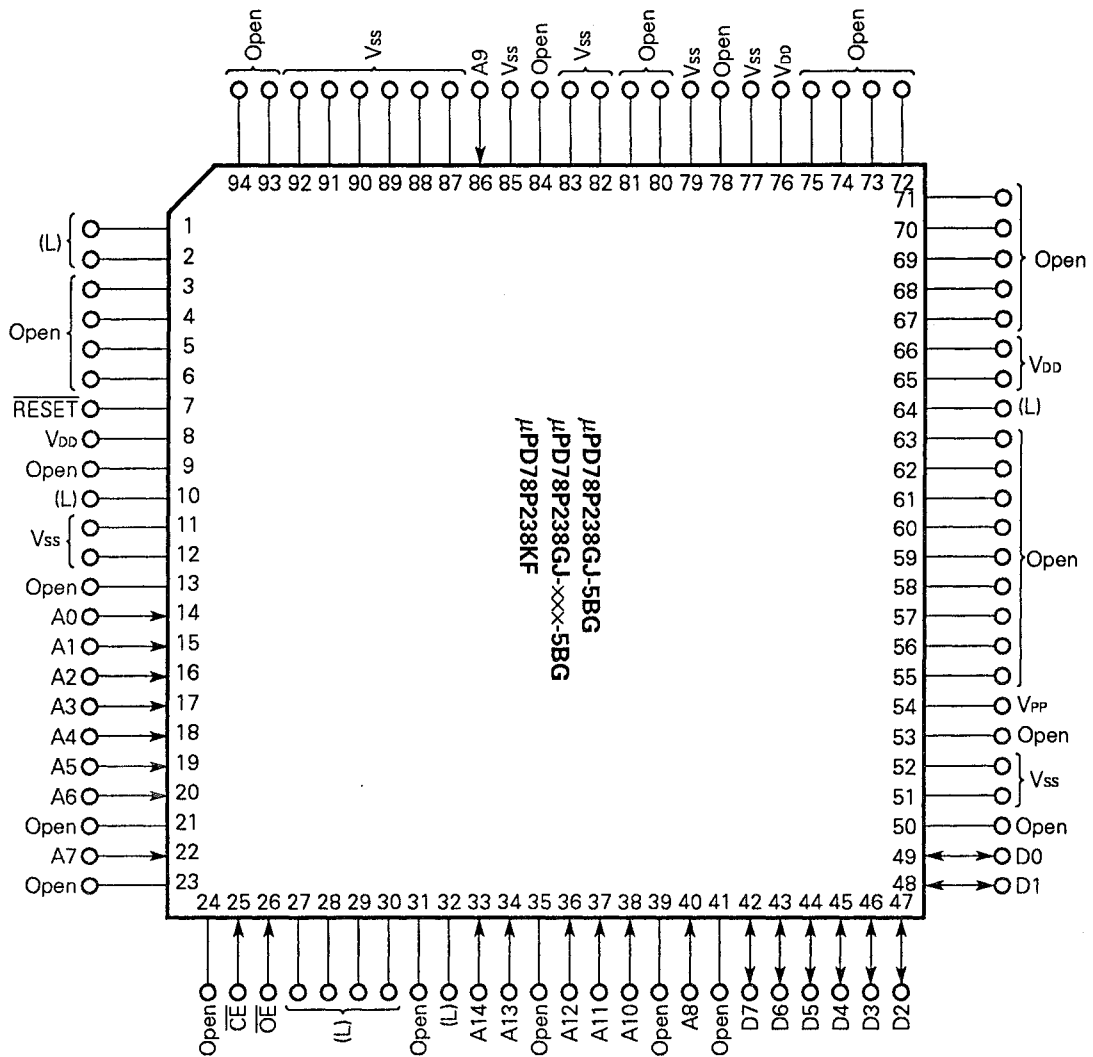
80-pin plastic QFP ( 14 × 14 mm)



- Caution L** : Connect these pins separately to the Vss pins through pull-down resistors.
- Vss** : To be connected to the ground.
- Open** : Nothing should be connected on these pins.
- RESET** : Set a low-level input.

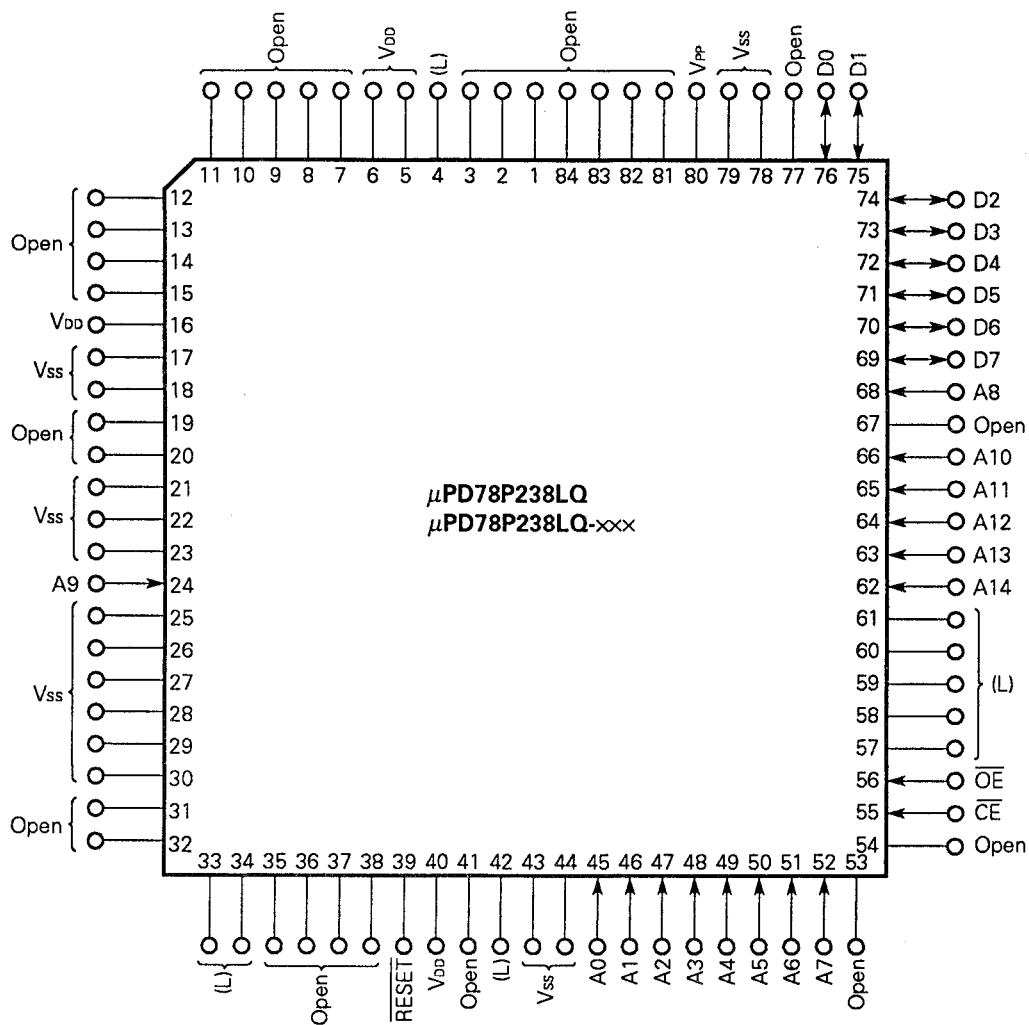


94-pin plastic QFP (20 × 20 mm)  
 94-pin ceramic WQFN (20 × 20 mm)



- Caution L** : Connect these pins separately to the V<sub>SS</sub> pins through pull-down resistors.
- V<sub>SS</sub>** : To be connected to the ground.
- Open** : Nothing should be connected on these pins.
- RESET** : Set a low-level input.

84-pin plastic QFJ (1150 × 1150 mil)

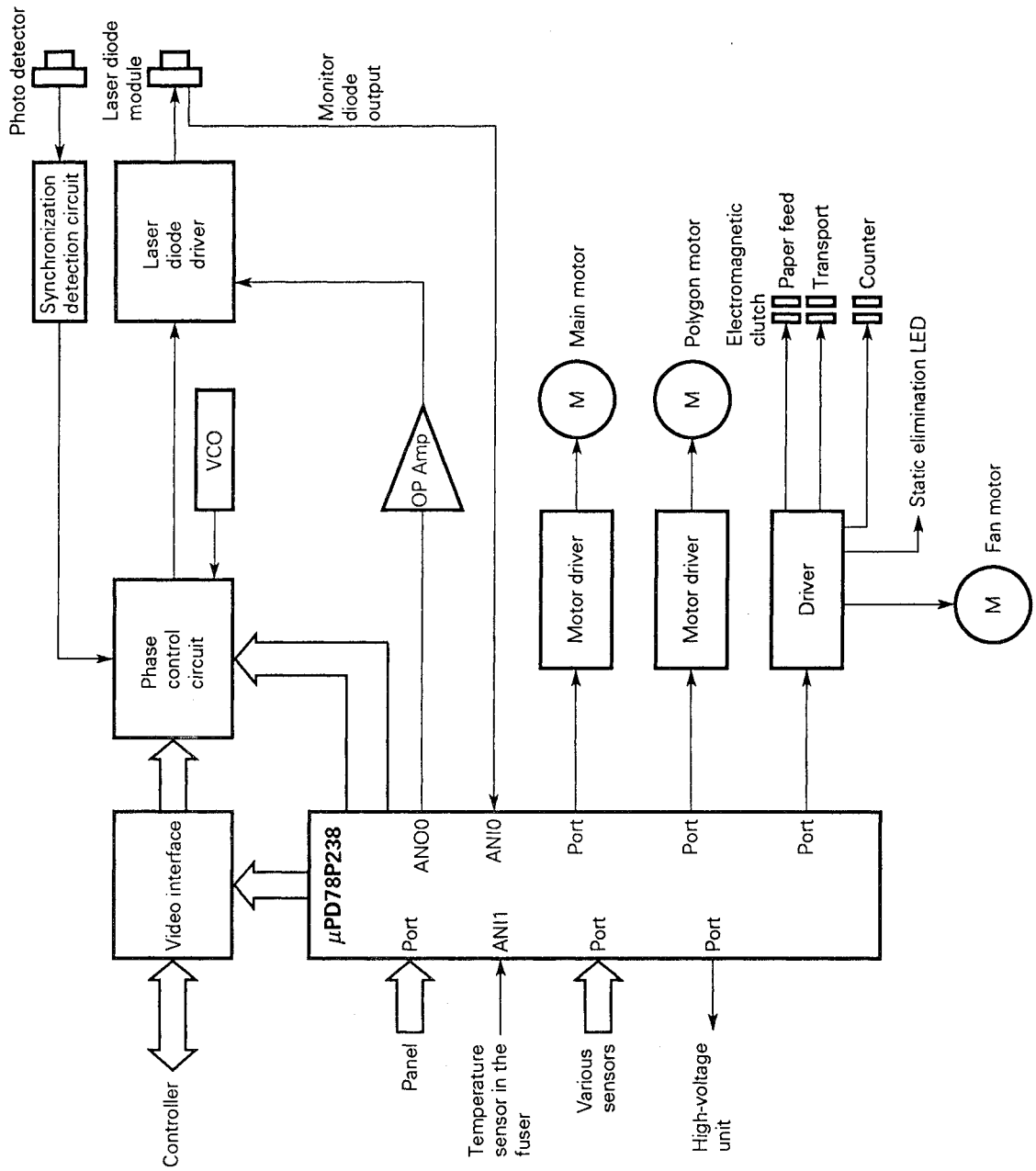


- Caution L** : Connect these pins separately to the Vss pins through pull-down resistors.
- Vss** : To be connected to the ground.
- Open** : Nothing should be connected on these pins.
- RESET** : Set a low-level input.

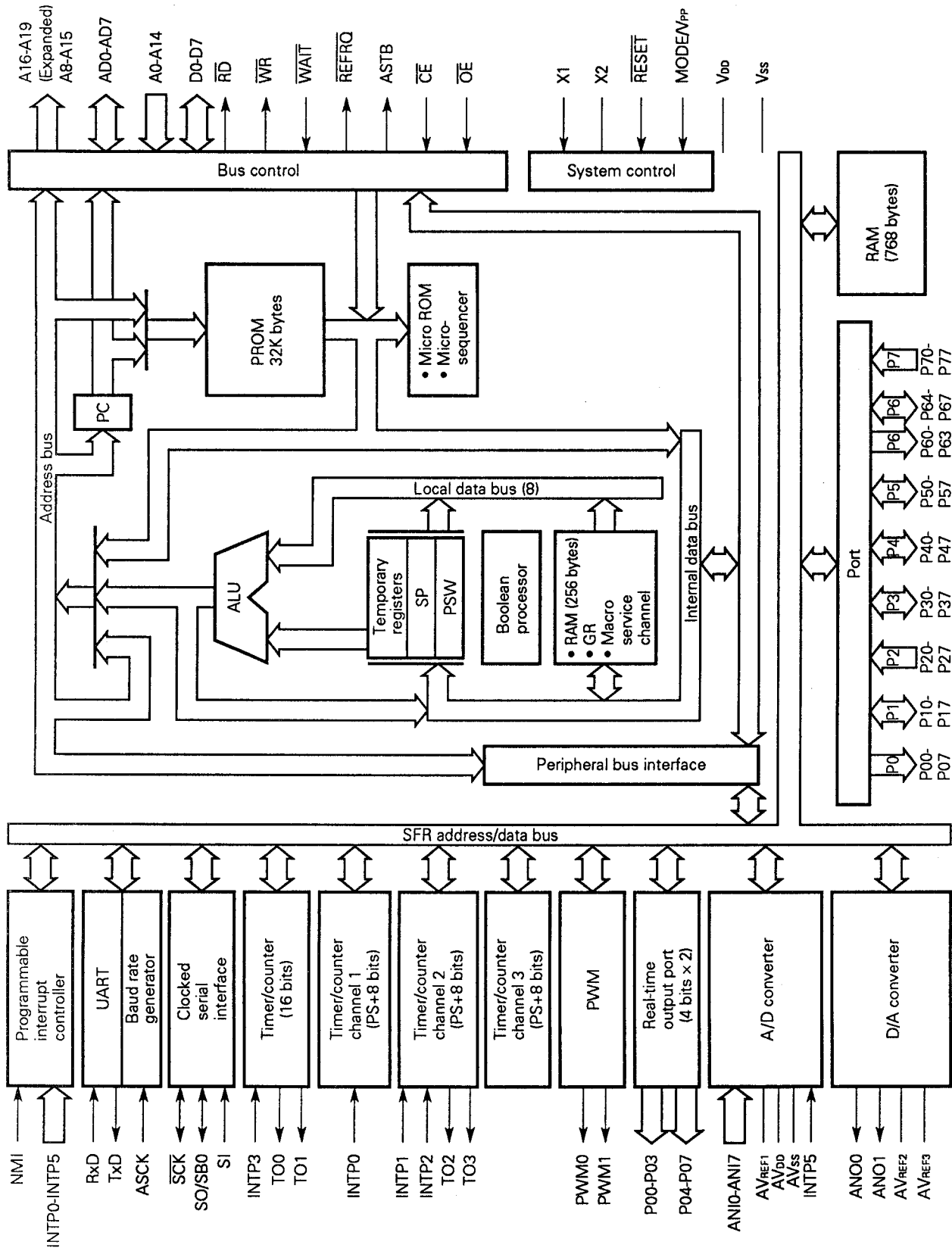
- VPP** : Programming power supply
- RESET** : Reset
- A0-A14** : Address bus
- D0-D7** : Data bus

- CE** : Chip enable
- OE** : Output enable
- VDD** : Power supply
- VSS** : Ground

EXAMPLE OF SYSTEM CONFIGURATION (LASER BEAM PRINTER)



INTERNAL BLOCK DIAGRAM



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## 1. DIFFERENCES BETWEEN THE $\mu$ PD78P238 AND $\mu$ PD78234/ $\mu$ PD78238

The  $\mu$ PD78P238 is produced by replacing the mask ROM in the  $\mu$ PD78238 with PROM on which data can be written. The functions of the  $\mu$ PD78P238 are the same as those of the  $\mu$ PD78238 except for the PROM specification such as writing and verification, and except that a ROM-less operation cannot be performed. Setting the internal memory select register (IMS) allows the PROM specification and the functions, except for the ROM-less operation, of the  $\mu$ PD78P238 to be the same as those of the  $\mu$ PD78234. Table 1-1 shows the differences between these products.

For the details of the CPU function and built-in hardware, refer to  *$\mu$ PD78234 User's Manual, Hardware* or other manuals.

**Table 1-1 Differences between the  $\mu$ PD78P238 and  $\mu$ PD78234/ $\mu$ PD78238**

Item	$\mu$ PD78P238	$\mu$ PD78238	$\mu$ PD78234
Internal program memory	32K-byte PROM 16K bytes can also be selected by the IMS register.	32K-byte mask ROM	16K-byte mask ROM
Built-in RAM	1024 bytes: 640 bytes can also be selected by the IMS register.	1024 bytes	640 bytes
ROM-less operation	Impossible	Possible by setting the MODE pin to high.	
Package	80-pin plastic QFP (14 × 14 mm) 94-pin plastic QFP (20 × 20 mm) 84-pin plastic QFJ (1150 × 1150 mil)		
	94-pin ceramic WQFN (20 × 20 mm)	—	

2. PIN FUNCTIONS

2.1 PORT PINS

Pin	I/O	Dual-function	Function
P00-P07	O	–	Port 0 (P0): Functions as a real-time output port (4 bits × 2). Can drive a transistor.
P10	I/O	PWM0	Port 1 (P1): Inputs and outputs can be specified bit by bit. The use of the pull-up resistors can be specified by software for the pins in the input mode together. Can drive LED.
P11		PWM1	
P12-P17		–	
P20	I	NMI	Port 2 (P2): P20 does not function as a general port (nonmaskable interrupt). However, the input level can be checked in an interrupt service routine. The use of the pull-up resistors can be specified by software for pins P22 to P27 (in units of 6 bits).
P21		INTP0	
P22		INTP1	
P23		INTP2/CI	
P24		INTP3	
P25		INTP4/ASCK	
P26		INTP5	
P27		SI	
P30	I/O	RxD	Port 3 (P3): Inputs and outputs can be specified bit by bit. The use of the pull-up resistors can be specified by software for the pins in the input mode together.
P31		TxD	
P32		SCK	
P33		SO/SB0	
P34-P37		TO0-TO3	
P40-P47	I/O	AD0-AD7	Port 4 (P4): Inputs and outputs can be specified in units of 8 bits. The use of the pull-up resistors can be specified by software in units of 8 bits.
P50-P57	I/O	A8-A15	Port 5 (P5): Inputs and outputs can be specified bit by bit. The use of the pull-up resistors can be specified by software for the pins in the input mode together.
P60-P63	O	A16-A19	Port 6 (P6): Inputs and outputs can be specified for P64-P67 bit by bit. The use of the pull-up resistors can be specified by software for pins P64 to P67 in the input mode together.
P64	I/O	$\overline{RD}$	
P65		$\overline{WR}$	
P66		$\overline{WAIT}$	
P67		$\overline{REFRQ}$	
P70-P77	I	ANI0-ANI7	Port 7 (P7)

## 2.2 NON-PORT PINS

Pin	I/O	Function	Dual-function
T00-T03	O	Timer output	P34-P37
CI	I	Input of a count clock for an 8-bit timer/counter 2	P23/INTP2
RxD	I	Serial data input (UART)	P30
TxD	O	Serial data output (UART)	P31
ASCK	I	Baud rate clock input (UART)	P25/INTP4
SBO	I/O	Serial data I/O (SBI)	P33/SO
SI	I	Serial data input (three-wire serial I/O)	P27
SO	O	Serial data output (three-wire serial I/O)	P33/SB0
SCK	I/O	Serial clock I/O (SBI, three-wire serial I/O)	P32
NMI	I	External interrupt request	P20
INTP0			P21
INTP1			P22
INTP2			P23/CI
INTP3			P24
INTP4			P25/ASCK
INTP5			P26
AD0-AD7	I/O	Time multiplexing address/data bus (for connecting external memory)	P40-P47
A8-A15	O	High-order address bus (for connecting external memory)	P50-P57
A16-A19	O	High-order address bus during address expansion (for connecting external memory)	P60-P63
$\overline{RD}$	O	Strobe signal output for reading the contents of external memory	P64
$\overline{WR}$	O	Strobe signal output for writing on external memory	P65
$\overline{WAIT}$	I	Wait signal insertion	P66
ASTB	O	Latch timing output of time multiplexing address (A0-A7) (for connecting external memory)	-
$\overline{REFRQ}$	O	Refresh pulse output to external pseudostatic memory	P67
$\overline{RESET}$	I	Chip reset	-
X1	I	Crystal input for system clock generation (A clock pulse can also be input to the X1 pin.)	-
X2			
MODE	I	Specification of PROM operation Normally, low-level input	-
ANI0-ANI7	I	Analog voltage inputs for the A/D converter	P70-P77
ANO0, ANO1	O	Analog voltage outputs for the D/A converter	-
$AV_{REF1}$	-	Application of A/D converter reference voltage	-
$AV_{REF2}, AV_{REF3}$		Application of D/A converter reference voltage	
$AV_{DD}$		Positive power supply for the A/D converter	
$AV_{SS}$		Ground for the A/D converter	
$V_{DD}$		Positive power supply	
$V_{SS}$		Ground	
NC		Not connected internally	



2.3 PROM PROGRAMMING MODE ( $V_{PP} \geq 5\text{ V}$ ,  $\overline{\text{RESET}} = \text{L}$ )

2.3.1 List of Pin Functions

Pin	I/O	Function
$V_{PP}$	-	Setting the μPD78P238 to the PROM programming mode: High-voltage apply pin for writing or verifying a program
$\overline{\text{RESET}}$	I	PROM programming mode
A0 - A14		Address bus
D0 - D7	I/O	Data bus
$\overline{\text{CE}}$	I	PROM enable input or program pulse input
$\overline{\text{OE}}$		Read strobe input to PROM
$V_{DD}$	-	Positive power supply
$V_{SS}$		Ground

### 2.3.2 Pin Functions

(1) **V<sub>PP</sub> (Programming power supply): Input**

Input pin for setting the  $\mu$ PD78P238 to the PROM programming mode. When the input voltage on this pin is 5 V or more and when  $\overline{\text{RESET}}$  input goes low, the  $\mu$ PD78P238 the PROM programming mode. When  $\overline{\text{CE}}$  is made low for  $V_{PP} = 12.5$  V and  $\overline{\text{OE}} = \text{high}$ , program data on D0 to D7 can be written into the internal PROM cell selected by A0 to A14.

(2)  **$\overline{\text{RESET}}$ : Input**

Input pin for setting the  $\mu$ PD78P238 to the PROM programming mode. When input on this pin is low, and when the input voltage on the  $V_{PP}$  pin goes 5 V or more, the  $\mu$ PD78P238 enters the PROM programming mode.

(3) **A0 to A14 (Address bus): Input**

Address bus that selects an internal PROM address (0000H to 7FFFH)

(4) **D0 to D7 (Data bus): I/O**

Data bus through which a program is written on or read from internal PROM

(5)  **$\overline{\text{CE}}$  (Chip enable): Input**

This pin inputs the enable signal from internal PROM. When this signal is active, a program can be written or read.

(6)  **$\overline{\text{OE}}$  (Output enable): Input**

This pin inputs the read strobe signal to internal PROM. When this signal is made active for  $\overline{\text{CE}} = \text{low}$ , a one-byte program in the internal PROM cell selected A0 to A14 can be read onto D0 to D7.

(7) **V<sub>DD</sub>**

Positive power supply pin

(8) **V<sub>SS</sub>**

Ground potential pin

**2.4 MEMORY MAPPING IN THE μPD78P238**

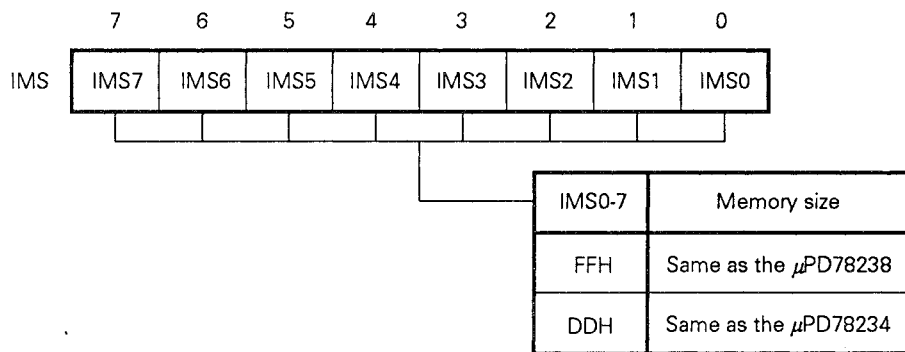
The μPD78P238 contains 32K-byte PROM and 1024-byte RAM. It differs a little in memory mapping from the μPD78234. To eliminate the difference, the μPD78P238 is provided with the memory-size change function to make part of internal memory unused by software.

A memory-size change register (IMS) is used to change the size of memory. To map memory into the μPD78P238 in the same way as the μPD78234, be sure to write on this register immediately after resetting the μPD78P238.

Writing on the IMS register is enabled by an 8-bit manipulation instruction. Fig. 2-1 shows the format of the register.

$\overline{\text{RESET}}$  input changes the size of memory in the μPD78P238 to FFH (the same size of memory as that in the μPD78238).

**Fig. 2-1 Memory-Size Change Register (IMS)**



**Caution** The μPD78234 and μPD78238 are not provided with this register. However, the write instruction to the register does not influence their operations.

### 3. PROGRAMMING IN THE $\mu$ PD78P238

The program memory in the  $\mu$ PD78P238 is an electrically writable PROM of  $32768 \times 8$  bits. Use the MODE/ $V_{PP}$  and  $\overline{\text{RESET}}$  pins to set the  $\mu$ PD78P238 to the PROM programming mode when programming on the PROM. Other unused pins are handled as shown in pin configuration (2).

The  $\mu$ PD78P238 provides programming characteristics compatibility with the  $\mu$ PD27C256A<sup>Note</sup>.

★ **Note** The  $\mu$ PD27C256A is not provided with the 100- $\mu$ s program-pulse mode.

#### 3.1 OPERATING MODE

When 5 V or more is applied to the MODE/ $V_{PP}$  pin and when a low-level pulse is applied to the  $\overline{\text{RESET}}$  pin, the  $\mu$ PD78P238 enters the PROM programming mode. This mode varies to each operating mode shown in Table 3-1 according to how to set the  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  pins.

Setting the  $\mu$ PD78P238 to the read mode enables it to read the contents of PROM.

**Table 3-1 Operating Modes for Programming on PROM**

Mode	Pin	$\overline{\text{RESET}}$	MODE/ $V_{PP}$	$V_{DD}$	$\overline{\text{CE}}$	$\overline{\text{OE}}$	D0 to D7
Program write		L	+12.5 V	+6 V	L	H	Data input
Program verify	H				L	Data output	
Program inhibit	H				H	High impedance	
Read			+5 V	+5 V	L	L	Data output
Output disable	L				H	High impedance	
Standby	H				L/H	High impedance	

**Caution** Do not set both  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  to L when MODE/ $V_{PP}$  is set to +12.5 V and  $V_{DD}$  to +6 V.

### 3.2 PROCEDURE FOR WRITING ON PROM

The following is a procedure for writing on PROM. Data can be written at high speed.

- (1) Always set the  $\overline{\text{RESET}}$  pin to low. Apply +5 V to the MODE/V<sub>PP</sub> pin. Connect other unused pins as shown in pin configuration (2).
- (2) Apply +6 V to the V<sub>DD</sub> pin and +12.5 V to the MODE/V<sub>PP</sub> pin.
- (3) Set an initial address.
- (4) Input write data.
- (5) Input a 1 ms program pulse (active low) to the  $\overline{\text{CE}}$  pin.
- (6) Verify mode: If data are written, go to step (8); if not, repeats steps (4) to (6). If no data are written yet after they are repeated 25 times, go to step (7).
- (7) Assume the device to be defective and stop write operation.
- (8) Input write data and a program pulse of (number of times steps (4) to (6) were repeated) × 3 ms (additional writing).
- (9) Increment the address.
- (10) Repeat steps (4) to (9) until the address exceeds the last address.

Fig. 3-1 is a timing chart of these steps (2) to (8).

**Fig. 3-1 PROM Write/Verify Timing Chart**

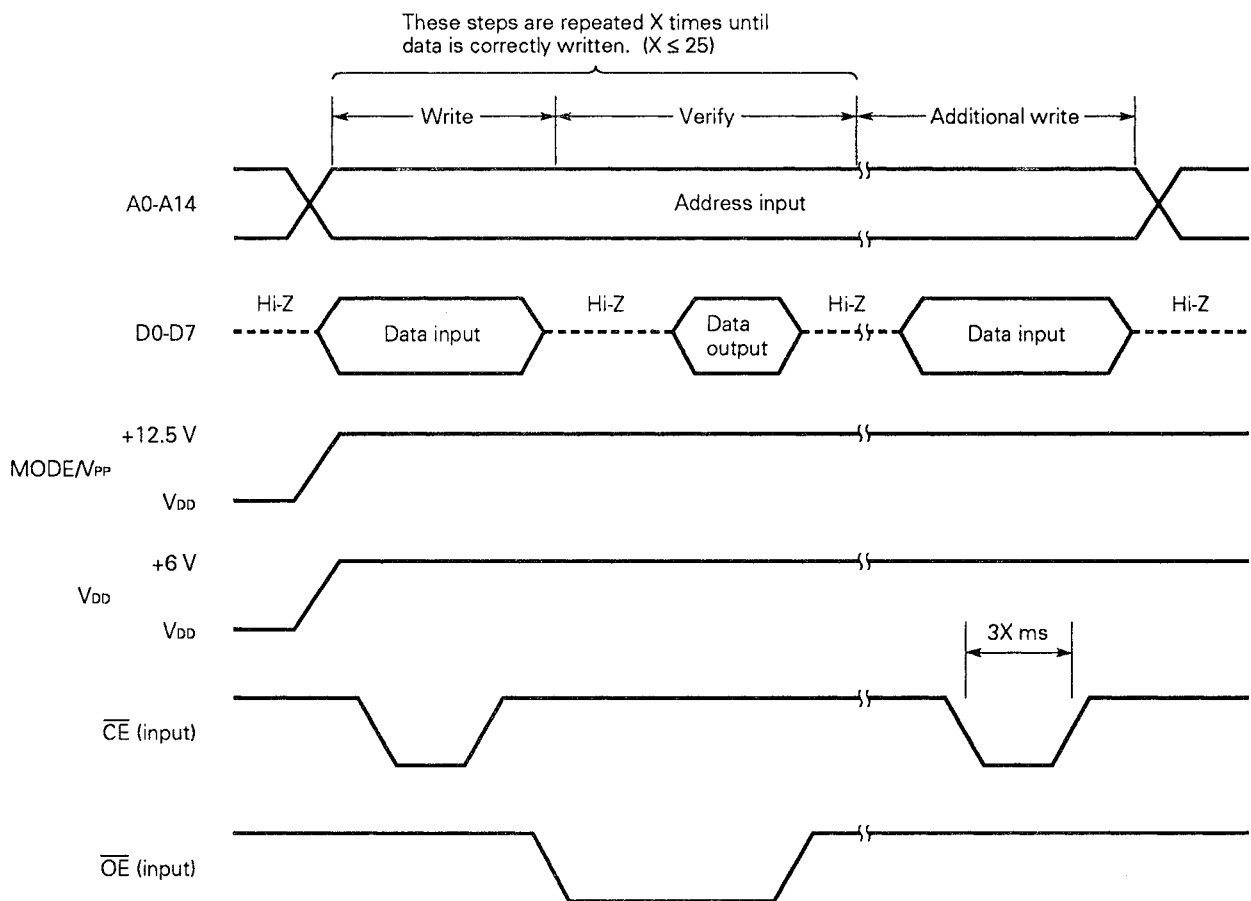
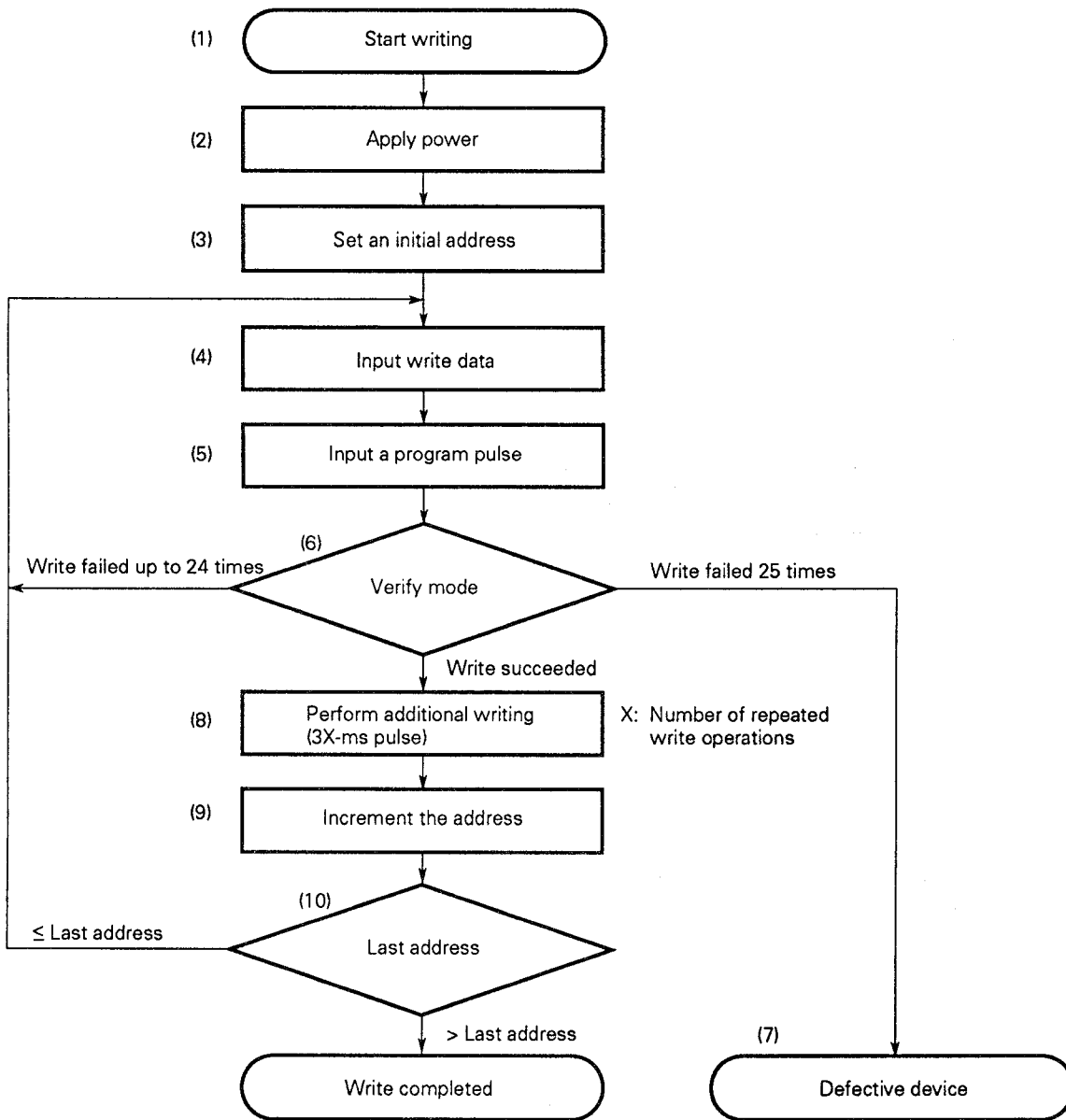


Fig. 3-2 Flowchart of Procedure for Writing



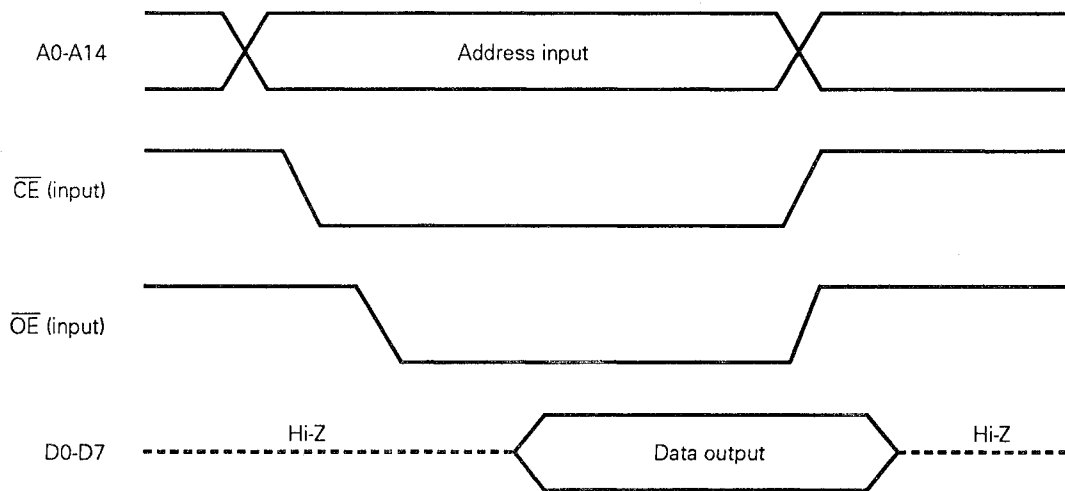
**3.3 PROCEDURE FOR READING FROM PROM**

The contents of PROM can be read out to the external data bus (D0 to D7) in the following steps:

- (1) Always set the RESET pin to low. Apply +5 V to the MODE/V<sub>PP</sub> pin. Connect other unused pins as shown in **pin configuration (2)**.
- (2) Apply +5 V to the V<sub>DD</sub> and V<sub>PP</sub> pins.
- (3) Input the address of data to be read into the A0 to A14 pins.
- (4) Read mode
- (5) Output the data on the D0 to D7 pins.

Fig. 3-3 is a timing chart of these steps (2) to (5).

**Fig. 3-3 PROM Read Timing Chart**



#### 4. ERASURE CHARACTERISTICS ONLY FOR THE $\mu$ PD78P238KF

The programmed data (FFH) of the  $\mu$ PD78P238KF can be erased by exposure to light with a wavelength less than approx. 400 nm.

To erase the contents of program memory in the  $\mu$ PD78P238KF, expose the erasure window to ultraviolet light with the wavelength of 254 nm. The amount of light required to completely erase the contents of program memory is a minimum of  $15 \text{ W}\cdot\text{s}/\text{cm}^2$  (intensity of ultraviolet light  $\times$  erasing time). It takes about 15 to 20 minutes to expose the erasure window to a  $12,000 \mu\text{W}/\text{cm}^2$  ultraviolet lamp. It may, however, take more time due to the fallen performance of this ultraviolet lamp, dirt on the package window, or suchlike. Note that the  $\mu$ PD78P238KF should be placed less than 2.5 cm from the ultraviolet lamp during erasure. In addition, if a filter is attached to the ultraviolet lamp, remove the filter before erasure.

#### 5. PROTECTIVE FILM COVERING THE ERASURE WINDOW ONLY FOR THE $\mu$ PD78P238KF

The erasure window should be covered with a protective film when not erasing the contents of EPROM to prevent erroneously erasing the contents of memory by exposure to light other than that of the lamp for erasing the contents of the EPROM, and to prevent internal circuits other than the EPROM from malfunctioning due to the light.

#### 6. SCREENING ONE-TIME PROM PRODUCTS

NEC cannot execute a complete test of one-time PROM products ( $\mu$ PD78P238GC-3B9,  $\mu$ PD78P238GJ-5BG, and  $\mu$ PD78P238LQ) due to their structure before shipment. It is recommended that you screen (verify) PROM products after writing necessary data into them and storing them at  $125^\circ\text{C}$  for 24 hours.

NEC offers a charged service called QTOP microcomputer service. This service includes writing to one-time PROM, marking, screening, and verification.

Ask your sales representative for details.



7. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T<sub>a</sub> = 25 °C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V <sub>DD</sub>		-0.5 to +7.0	V
	AV <sub>DD</sub>		AV <sub>SS</sub> to V <sub>DD</sub> +0.5	V
	AV <sub>SS</sub>		-0.5 to +0.5	V
Input voltage	V <sub>I1</sub>		-0.5 to V <sub>DD</sub> +0.5	V
	V <sub>I2</sub>	MODE/V <sub>PP</sub> and P21/INTP0/A9 pins in the PROM programming mode	-0.5 to +13.5	V
Output voltage	V <sub>O</sub>		-0.5 to V <sub>DD</sub> +0.5	V
Low-level output current	I <sub>OL</sub>	1 pin	15	mA
		Total of all output pins	100	mA
High-level output current	I <sub>OH</sub>	1 pin	-10	mA
		Total of all output pins	-50	mA
A/D converter reference input voltage	AV <sub>REF1</sub>		-0.5 to V <sub>DD</sub> +0.3	V
D/A converter reference input voltage	AV <sub>REF2</sub>		-0.5 to V <sub>DD</sub> +0.3	V
	AV <sub>REF3</sub>		-0.5 to V <sub>DD</sub> +0.3	V
Operating temperature	T <sub>opt</sub>		-40 to +85	°C
Storage temperature	T <sub>stg</sub>		-65 to +150	°C

**Caution** Absolute maximum ratings are rated values beyond which some physical damages may be caused to the product; if any of the parameters in the table above exceeds its rated value even for a moment, the quality of the product may deteriorate. Be sure to use the product within the rated values. ★

OPERATING CONDITIONS

Clock frequency	Operating temperature (T <sub>opt</sub> )	Supply voltage (V <sub>DD</sub> )
4 MHz ≤ f <sub>xx</sub> ≤ 12 MHz	-40 to +85 °C	+5.0 V ±10 %

CAPACITANCE (T<sub>a</sub> = 25 °C, V<sub>DD</sub> = V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C <sub>I</sub>	f = 1 MHz			20	pF
Output capacitance	C <sub>O</sub>	0 V on pins other than measured pins			20	pF
I/O capacitance	C <sub>IO</sub>				20	pF

OSCILLATOR CHARACTERISTICS ( $T_a = -40$  to  $+85$  °C,  $V_{DD} = +5$  V  $\pm 10$  %,  $V_{SS} = 0$  V)

Resonator	Recommended circuit	Parameter	Min.	Max.	Unit
Ceramic resonator or crystal		Oscillator frequency ( $f_{xx}$ )	4	12	MHz
External clock		X1 input frequency ( $f_x$ )	4	12	MHz
		X1 input rising and falling times ( $t_{xR}$ , $t_{xF}$ )	0	30	ns
		X1 input high-level and low-level widths ( $t_{wxH}$ , $t_{wxL}$ )	30	130	ns

**Caution** When the clock oscillator is used, conform to the following guidelines when wiring at the portions surrounded by dotted lines in the figure above to eliminate the influence of the wiring capacity.

- The wiring must be as short as possible.
- Other signal lines must not run in these areas.
- Any line carrying a high fluctuating current must be kept away as far as possible.
- The grounding point of the capacitor of the oscillator must have the same potential as that of  $V_{SS}$ . It must not be grounded to ground patterns carrying a large current.
- No signal must be taken from the oscillator.

DC CHARACTERISTICS (T<sub>a</sub> = -40 to +85 °C, V<sub>DD</sub> = AV<sub>DD</sub> = +5 V ±10 %, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Low-level input voltage	V <sub>IL</sub>		0		0.8	V	
High-level input voltage	V <sub>IH1</sub>	Pins other than those shown in Note 1	2.2		V <sub>DD</sub>	V	
	V <sub>IH2</sub>	Pins shown in Note 1	0.8V <sub>DD</sub>		V <sub>DD</sub>	V	
Low-level output voltage	V <sub>OL1</sub>	I <sub>OL</sub> = 2.0 mA			0.45	V	
	V <sub>OL2</sub>	I <sub>OL</sub> = 8.0 mA <sup>Note 2</sup>			1.0	V	
High-level output voltage	V <sub>OH1</sub>	I <sub>OH</sub> = -1.0 mA	V <sub>DD</sub> - 1.0			V	
	V <sub>OH2</sub>	I <sub>OH</sub> = -100 μA	V <sub>DD</sub> - 0.5			V	
	V <sub>OH3</sub>	I <sub>OH</sub> = -5.0 mA <sup>Note 3</sup>	2.0			V	
X1 low-level input current	I <sub>IL</sub>	0 V ≤ V <sub>i</sub> ≤ V <sub>IL</sub>			-100	μA	
X1 high-level input current	I <sub>IH</sub>	V <sub>IH2</sub> ≤ V <sub>i</sub> ≤ V <sub>DD</sub>			100	μA	
Input leakage current	I <sub>LI</sub>	0 V ≤ V <sub>i</sub> ≤ V <sub>DD</sub>			±10	μA	
Output leakage current	I <sub>LO</sub>	0 V ≤ V <sub>o</sub> ≤ V <sub>DD</sub>			±10	μA	
V <sub>DD</sub> supply current	I <sub>DD1</sub>	Operating mode, f <sub>xx</sub> = 12 MHz		20	40	mA	
	I <sub>DD2</sub>	HALT mode, f <sub>xx</sub> = 12 MHz		7	20	mA	
Data retention voltage	V <sub>DDDR</sub>	STOP mode	2.5		5.5	V	
Data retention current	I <sub>DDDR</sub>	STOP mode	V <sub>DDDR</sub> = 2.5 V			10	μA
			V <sub>DDDR</sub> = 5 V ±10 %			20	μA
Pull-up resistor	R <sub>L</sub>	V <sub>i</sub> = 0 V	15	40	80	kΩ	

- Notes 1.** Pins X1, X2,  $\overline{\text{RESET}}$ , P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK, P26/INTP5, P27/SI, P32/ $\overline{\text{SCK}}$ , P33/SO/SB0, and MODE  
**2.** Pins P10-P17, P40/AD0-P47/AD7, and P50/A8-P57/A15  
**3.** Pins P00-P07

AC CHARACTERISTICS ( $T_a = -40$  to  $+85$  °C,  $V_{DD} = AV_{DD} = +5$  V  $\pm 10$  %,  $V_{SS} = AV_{SS} = 0$  V)

## Read/write operation (1/2)

Parameter	Symbol	Conditions	Min.	Max.	Unit
X1 input clock cycle time	$t_{CYX}$		82	250	ns
Address setup time (referred to $ASTB\downarrow$ )	$t_{SAST}^*$		52		ns
Address hold time (referred to $ASTB\downarrow$ ) <b>Note</b>	$t_{HSTA}$		25		ns
Address hold time (referred to $\overline{RD}\uparrow$ )	$t_{HRA}$		30		ns
Address hold time (referred to $\overline{WR}\uparrow$ )	$t_{HWA}$		30		ns
Delay from address to $\overline{RD}\downarrow$	$t_{DAR}^*$		129		ns
Address float time (referred to $\overline{RD}\downarrow$ )	$t_{FAR}^*$		11		ns
Delay from address to data input	$t_{DAID}^*$	The number of wait cycles = 0		228	ns
Delay from $ASTB\downarrow$ to data input	$t_{DSTID}^*$	The number of wait cycles = 0		181	ns
Delay from $\overline{RD}\downarrow$ to data input	$t_{DRID}^*$	The number of wait cycles = 0		99	ns
Delay from $ASTB\downarrow$ to $\overline{RD}\downarrow$	$t_{DSTR}^*$		52		ns
Data hold time (referred to $\overline{RD}\uparrow$ )	$t_{HRID}$		0		ns
Delay from $\overline{RD}\uparrow$ to address active	$t_{DRA}^*$		124		ns
Delay from $\overline{RD}\uparrow$ to $ASTB\uparrow$	$t_{DRST}^*$		124		ns
$\overline{RD}$ low-level width	$t_{WRL}^*$	The number of wait cycles = 0	124		ns
$ASTB$ high-level width	$t_{WSTH}^*$		52		ns
Delay from address to $\overline{WR}\downarrow$	$t_{DAW}^*$		129		ns
Delay from $ASTB\downarrow$ to data output	$t_{DSTOD}^*$			142	ns
Delay from $\overline{WR}\downarrow$ to data output	$t_{DWOD}$			60	ns
★ Delay from $ASTB\downarrow$ to $\overline{WR}\downarrow$	$t_{DSTW1}^*$	When refresh is inhibited	52		ns
	$t_{DSTW2}^*$	When refresh is allowed	129		ns
Data setup time (referred to $\overline{WR}\uparrow$ )	$t_{SODWR}^*$	The number of wait cycles = 0	146		ns
Data setup time (referred to $\overline{WR}\downarrow$ )	$t_{SODWF}^*$	When refresh is allowed	22		ns
Data hold time (referred to $\overline{WR}\uparrow$ ) <b>Note</b>	$t_{HWOD}$		20		ns
Delay from $\overline{WR}\uparrow$ to $ASTB\uparrow$	$t_{DWST}^*$		42		ns

**Note** The hold time includes the time for holding  $V_{OH}$  and  $V_{OL}$  on the load conditions of  $C_L = 100$  pF and  $R_L = 2$  k $\Omega$ .

**Remarks 1.** The values listed in the above table are obtained when  $f_{XX} = 12$  MHz and  $C_L = 100$  pF.

**2.** See  **$t_{CYX}$ -dependent bus timing definition** for additional information about the parameters with an asterisk in the symbol column.

## Read/write operation (2/2)

Parameter	Symbol	Conditions	Min.	Max.	Unit
WR low-level width	$t_{WWL1}^*$	When refresh is inhibited The number of wait cycles = 0	196		ns
	$t_{WWL2}^*$	When refresh is allowed The number of wait cycles = 0	114		ns
Delay from address to $\overline{WAIT}\downarrow$ input	$t_{DAWT}^*$			146	ns
Delay from $ASTB\downarrow$ to $\overline{WAIT}\downarrow$ input	$t_{DSTWT}^*$			84	ns
Hold time from $ASTB\downarrow$ to $\overline{WAIT}$	$t_{HSTWT}^*$	The number of external cycles = 1	174		ns
Delay from $ASTB\downarrow$ to $\overline{WAIT}\uparrow$	$t_{DSTWTH}^*$	The number of external cycles = 1		273	ns
Delay from $\overline{RD}\downarrow$ to $\overline{WAIT}\downarrow$ input	$t_{DRWTL}^*$			22	ns
Hold time from $\overline{RD}\downarrow$ to $\overline{WAIT}$	$t_{HRWT}^*$	The number of external cycles = 1	87		ns
Delay from $\overline{RD}\downarrow$ to $\overline{WAIT}\uparrow$	$t_{DRWTH}^*$	The number of external cycles = 1		186	ns
Delay from $\overline{WAIT}\uparrow$ to data input	$t_{DWTID}^*$			62	ns
Delay from $\overline{WAIT}\uparrow$ to $\overline{WR}\uparrow$	$t_{DWTW}^*$		154		ns
Delay from $\overline{WAIT}\uparrow$ to $\overline{RD}\uparrow$	$t_{DWTR}^*$		72		ns
Delay from $\overline{WR}\downarrow$ to $\overline{WAIT}$ input (when refresh is inhibited)	$t_{DWWTL}^*$			22	ns
Hold time from $\overline{WR}\downarrow$ to $\overline{WAIT}$	When refresh is inhibited	$t_{HWWT1}^*$	The number of external cycles = 1	87	ns
	When refresh is allowed	$t_{HWWT2}^*$	The number of external cycles = 1	5	ns
Delay from $\overline{WR}\downarrow$ to $\overline{WAIT}\uparrow$	When refresh is inhibited	$t_{DWWTH1}^*$	The number of external cycles = 1		186
	When refresh is allowed	$t_{DWWTH2}^*$	The number of external cycles = 1		104
Delay from $\overline{RD}\uparrow$ to $\overline{REFRQ}\downarrow$	$t_{DRRFQ}^*$		154		ns
Delay from $\overline{WR}\uparrow$ to $\overline{REFRQ}\downarrow$	$t_{DWRFQ}^*$		72		ns
REFRQ low-level width	$t_{WRFQL}^*$		120		ns
Delay from $\overline{REFRQ}\uparrow$ to $ASTB\uparrow$	$t_{DRFQST}^*$		280		ns

Remarks 1. The values listed in the above table are obtained when  $f_{xx} = 12$  MHz and  $C_L = 100$  pF.

2. See **tcvx-dependent bus timing definition** for additional information about the parameters with an asterisk in the symbol column.

## Serial operation

Parameter	Symbol	Conditions		Min.	Max.	Unit
Serial clock cycle time	tcvsk	Input	External clock	1.0		$\mu$ s
		Output	Internal clock divided by 16	1.3		$\mu$ s
			Internal clock divided by 64	5.3		$\mu$ s
Serial clock low-level width	twskl	Input	External clock	420		ns
		Output	Internal clock divided by 16	556		ns
			Internal clock divided by 64	2.5		$\mu$ s
Serial clock high-level width	twskh	Input	External clock	420		ns
		Output	Internal clock divided by 16	556		ns
			Internal clock divided by 64	2.5		$\mu$ s
SI, SB0 setup time (referred to $\overline{\text{SCK}}\uparrow$ )	tsssk			150		ns
SI, SB0 hold time (referred to $\overline{\text{SCK}}\uparrow$ )	tsssk			400		ns
SO/SB0 output delay time (referred to $\overline{\text{SCK}}\downarrow$ )	tdsbsk1	CMOS push-pull output (three-wire serial I/O mode)		0	300	ns
	tdsbsk2	Open-drain output (SBI mode), $R_L = 1 \text{ k}\Omega$		0	800	ns
SB0 high hold time (referred to $\overline{\text{SCK}}\uparrow$ )	tsssk	SBI mode		4		tcvx
SB0 low setup time (referred to $\overline{\text{SCK}}\downarrow$ )	tsssk			4		tcvx
SB0 low-level width	twsbl			4		tcvx
SB0 high-level width	twsbh			4		tcvx

**Remark** The values listed in the above table are obtained when  $f_{xx} = 12 \text{ MHz}$  and  $C_L = 100 \text{ pF}$ .

**Other operations**

Parameter	Symbol	Conditions	Min.	Max.	Unit
NMI low-level width	tWNIL		10		μs
NMI high-level width	tWNIH		10		μs
INTP0-INTP5 low-level width	tWITL		24		tcyx
INTP0-INTP5 high-level width	tWITH		24		tcyx
RESET low-level width	tWRSL		10		μs
RESET high-level width	tWRSH		10		μs

**External clock timing**

Parameter	Symbol	Conditions	Min.	Max.	Unit
X1 input low-level width	twXL		30	130	ns
X1 input high-level width	twXH		30	130	ns
X1 input rising time	txR		0	30	ns
X1 input falling time	txF		0	30	ns
X1 input clock cycle time	tcyx		82	250	ns

**A/D CONVERTER CHARACTERISTICS** (T<sub>a</sub> = -40 to +85 °C, V<sub>DD</sub> = AV<sub>DD</sub> = +5 V ±10 %, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution			8			bit
Total error <sup>Note 1</sup>		4.0 V ≤ AV <sub>REF1</sub> ≤ AV <sub>DD</sub> T <sub>a</sub> = -10 to +70 °C			0.4	%
		3.4 V ≤ AV <sub>REF1</sub> ≤ AV <sub>DD</sub>			0.8	%
		4.0 V ≤ AV <sub>REF1</sub> ≤ AV <sub>DD</sub>			0.6	%
Quantizing error					±1/2	LSB
Conversion time	tCONV	When the FR bit in ADM is 0	360			tcyx
		When the FR bit in ADM is 1	240			tcyx
Sampling time	tSAMP	When the FR bit in ADM is 0	72			tcyx
		When the FR bit in ADM is 1	48			tcyx
Analog input voltage	V <sub>IAN</sub>		-0.3		AV <sub>REF1</sub> + 0.3	V
Analog input impedance	R <sub>AN</sub>			1000		MΩ
Reference voltage	AV <sub>REF1</sub>		3.4		AV <sub>DD</sub>	V
AV <sub>REF</sub> current	AI <sub>REF1</sub>	f <sub>XX</sub> = 12 MHz		1.5	3.0	mA
		<sup>Note 2</sup>		0.7	1.5	mA
AV <sub>DD</sub> supply current	AI <sub>DD1</sub>	f <sub>XX</sub> = 12 MHz		1.4	3.0	mA
	AI <sub>DD2</sub>	<sup>Note 3</sup>		10	20	μA

**Notes 1.** Quantizing error is excluded. The total error is represented in percent with respect to a full-scale value.

**2.** When the CS bit in the ADM register is set to 0.

**3.** When the CS bit in the ADM register is set to 0 in the STOP mode.

D/A CONVERTER CHARACTERISTICS ( $T_a = -40$  to  $+85$  °C,  $AV_{REF2} = V_{DD} = AV_{DD} = +5$  V  $\pm 10$  %,  $AV_{REF3} = V_{SS} = 0$  V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution					8	bit
Total error		Load condition: 4 M $\Omega$ , 30 pF			0.4	%
		Load condition: 2 M $\Omega$ , 30 pF			0.6	%
		$AV_{REF2} = 0.75V_{DD}$ , $AV_{REF3} = 0.25V_{DD}$ Load condition: 4 M $\Omega$ , 30 pF			0.6	%
		$AV_{REF2} = 0.75V_{DD}$ , $AV_{REF3} = 0.25V_{DD}$ Load condition: 2 M $\Omega$ , 30 pF			0.8	%
Settling time		Load condition: 2 M $\Omega$ , 30 pF			10	$\mu$ s
Output resistor	$R_o$	Note		20		k $\Omega$
Analog reference voltage	$AV_{REF2}$		$0.75V_{DD}$		$V_{DD}$	V
Analog reference voltage	$AV_{REF3}$		0		$0.25V_{DD}$	V
Reference supply input current	$AI_{REF2}$		0		5	mA
Reference supply input current	$AI_{REF3}$		-5		0	mA

Note When DACS0 and DACS1 are set to 7FH.



tcyx-dependent bus timing definition (1/2)

Parameter	Symbol	Calculation formula	Min./Max.	12 MHz	Unit
X1 input clock cycle time	tcyx		Min.	82	ns
Address setup time (referred to ASTB↓)	tsAST	tcyx - 30	Min.	52	ns
Delay from address to $\overline{RD}\downarrow$	tdAR	2tcyx - 35	Min.	129	ns
Address float time (referred to $\overline{RD}\downarrow$ )	tfAR	tcyx/2 - 30	Min.	11	ns
Delay from address to data input	tdAID	(4 + 2n)tcyx - 100	Max.	228 <i>Note</i>	ns
Delay from ASTB↓ to data input	tdSTID	(3 + 2n)tcyx - 65	Max.	181 <i>Note</i>	ns
Delay from $\overline{RD}\downarrow$ to data input	tdRID	(2 + 2n)tcyx - 64	Max.	100 <i>Note</i>	ns
Delay from ASTB↓ to $\overline{RD}\downarrow$	tdSTR	tcyx - 30	Min.	52	ns
Delay from $\overline{RD}\uparrow$ to address active	tdRA	2tcyx - 40	Min.	124	ns
Delay from $\overline{RD}\uparrow$ to ASTB↑	tdRST	2tcyx - 40	Min.	124	ns
$\overline{RD}$ low-level width	twRL	(2 + 2n)tcyx - 40	Min.	124 <i>Note</i>	ns
ASTB high-level width	twSTH	tcyx - 30	Min.	52	ns
Delay from address to $\overline{WR}\downarrow$	tdAW	2tcyx - 35	Min.	129	ns
Delay from ASTB↓ to data output	tdSTOD	tcyx + 60	Max.	142	ns
Delay from ASTB↓ to $\overline{WR}\downarrow$	tdSTW1	tcyx - 30 (When refresh is inhibited)	Min.	52	ns
	tdSTW2	2tcyx - 35 (When refresh is allowed)	Min.	129	ns
Data setup time (referred to $\overline{WR}\uparrow$ )	tsODWR	(3 + 2n)tcyx - 100	Min.	146 <i>Note</i>	ns
Data setup time (referred to $\overline{WR}\downarrow$ )	tsODWF	tcyx - 60 (When refresh is allowed)	Min.	22	ns
Delay from $\overline{WR}\uparrow$ to ASTB↑	tdWST	tcyx - 40	Min.	42	ns
$\overline{WR}$ low-level width	twWL1	(3 + 2n)tcyx - 50 (When refresh is inhibited)	Min.	196 <i>Note</i>	ns
	twWL2	(2 + 2n)tcyx - 50 (When refresh is allowed)	Min.	114 <i>Note</i>	ns
Delay from address to $\overline{WAIT}\downarrow$ input	tdAWT	3tcyx - 100	Max.	146	ns
Delay from ASTB↓ to $\overline{WAIT}\downarrow$ input	tdSTWT	2tcyx - 80	Max.	84	ns

**Remark** n represents the number of wait cycles.

**Note** When n = 0

tcvx-dependent bus timing definition (2/2)

Parameter	Symbol	Calculation formula	Min./Max.	12 MHz	Unit	
Hold time from ASTB↓ to WAIT	tHSTWT	$2Xtcvx + 10$	Min.	174 <b>Note</b>	ns	
Delay from ASTB↓ to WAIT↑	tdSTWTH	$2(1 + X)tcvx - 55$	Max.	273 <b>Note</b>	ns	
Delay from RD↓ to WAIT↓ input	tDRWTL	$tcvx - 60$	Max.	22	ns	
Hold time from RD↓ to WAIT	tHRWT	$(2X - 1)tcvx + 5$	Min.	87 <b>Note</b>	ns	
Delay from RD↓ to WAIT↑ delay	tDRWTH	$(2X + 1)tcvx - 60$	Max.	186 <b>Note</b>	ns	
Delay from WAIT↑ to data input	tdWTD	$tcvx - 20$	Max.	62	ns	
Delay from WAIT↑ to WR↑	tdWTR	$2tcvx - 10$	Min.	154	ns	
Delay from WAIT↑ to RD↑	tdWTR	$tcvx - 10$	Min.	72	ns	
Delay from WR↓ to WAIT input (when refresh is inhibited)	tdWWTL	$tcvx - 60$	Max.	22	ns	
Hold time from WR↓ to WAIT	When refresh is inhibited	tHWWT1	$(2X - 1)tcvx + 5$	Min.	87 <b>Note</b>	ns
	When refresh is allowed	tHWWT2	$2(X - 1)tcvx + 5$	Min.	5 <b>Note</b>	ns
Delay from WR↓ to WAIT↑	When refresh is inhibited	tdWWTH1	$(2X + 1)tcvx - 60$	Max.	186 <b>Note</b>	ns
	When refresh is allowed	tdWWTH2	$2Xtcvx - 60$	Max.	104 <b>Note</b>	ns
Delay from RD↑ to REFRQ↓	tDRRFQ	$2tcvx - 10$	Min.	154	ns	
Delay from WR↑ to REFRQ↓	tDWRFQ	$tcvx - 10$	Min.	72	ns	
REFRQ low-level width	tWRFQL	$2tcvx - 44$	Min.	120	ns	
Delay from REFRQ↑ to ASTB↑	tDRFAST	$4tcvx - 48$	Min.	280	ns	

- Remarks 1.** X: External wait cycle (1, 2, ...)  
**2.** tcvx ≅ 82 ns (fxx = 12 MHz)  
**3.** n represents the number of wait cycles.

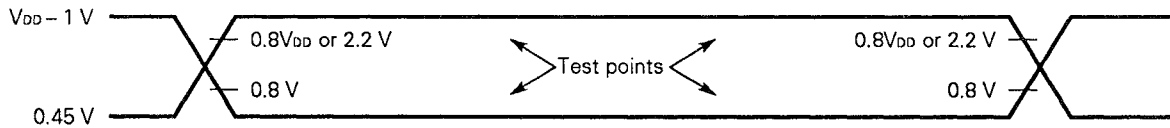
**Note** When X = 1

DATA RETENTION CHARACTERISTICS (T<sub>a</sub> = -40 to +85 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data retention voltage	V <sub>DDDR</sub>	STOP mode	2.5		5.5	V
Data retention current	I <sub>DDDR</sub>	V <sub>DDDR</sub> = 2.5 V			10	μA
		V <sub>DDDR</sub> = 5 V ±10 %			20	μA
V <sub>DD</sub> rising time	t <sub>RV</sub>		200			μs
V <sub>DD</sub> falling time	t <sub>FD</sub>		200			μs
V <sub>DD</sub> hold time (referred to STOP mode setting)	t <sub>HV</sub>		0			ms
STOP release signal input time	t <sub>DREL</sub>		0			ms
Oscillation settling wait time	t <sub>WAIT</sub>	Crystal resonator	30			ms
		Ceramic resonator	5			ms
Low-level input voltage	V <sub>IL</sub>	Specified pins <b>Note</b>	0		0.1V <sub>DDDR</sub>	V
High-level input voltage	V <sub>IH</sub>		0.9V <sub>DDDR</sub>		V <sub>DDDR</sub>	V

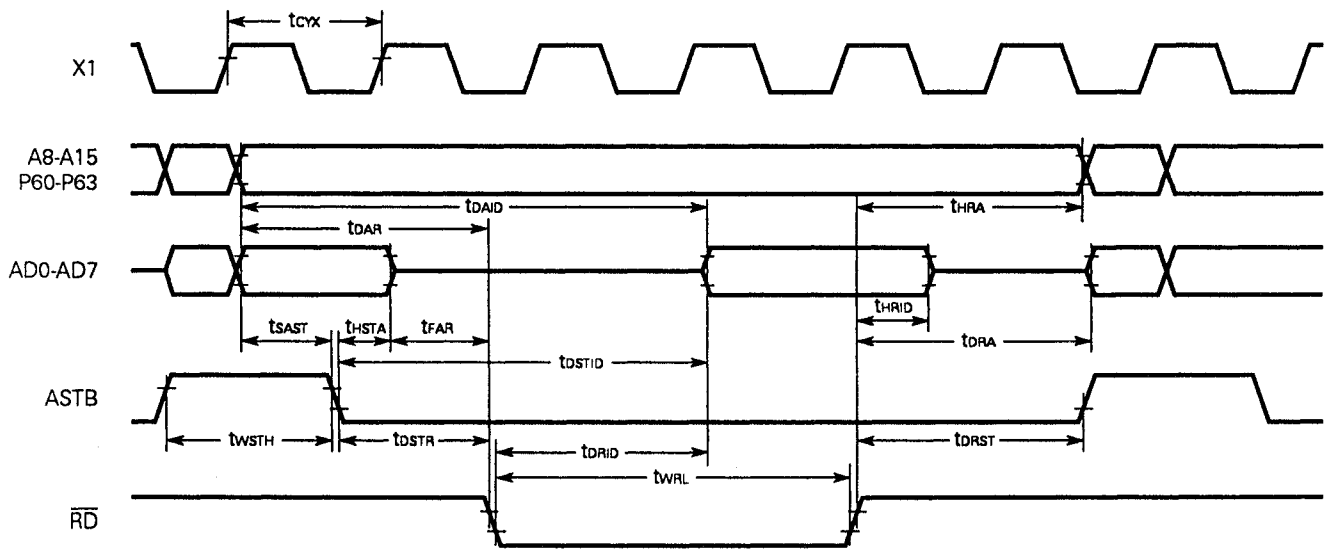
**Note** Pins RESET, MODE, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK, P26/INTP5, P27/SI, P32/SCK, and P33/SO/SB0

AC Timing Test Points

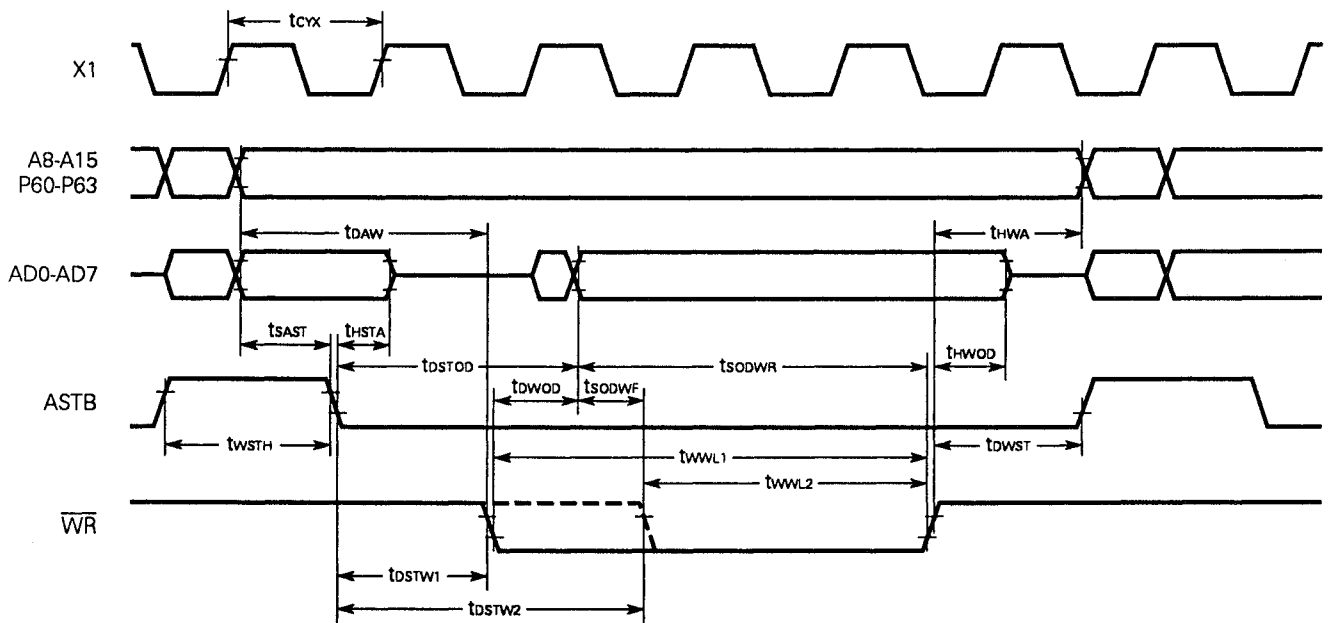


Timing Waveform

Read operation:

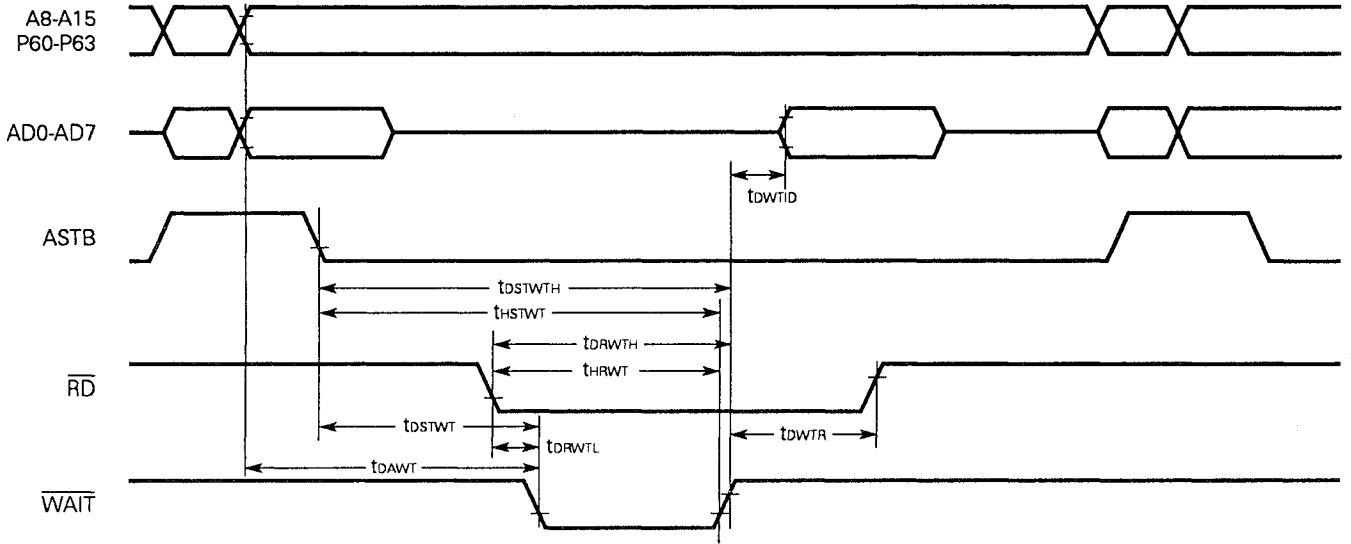


Write operation:

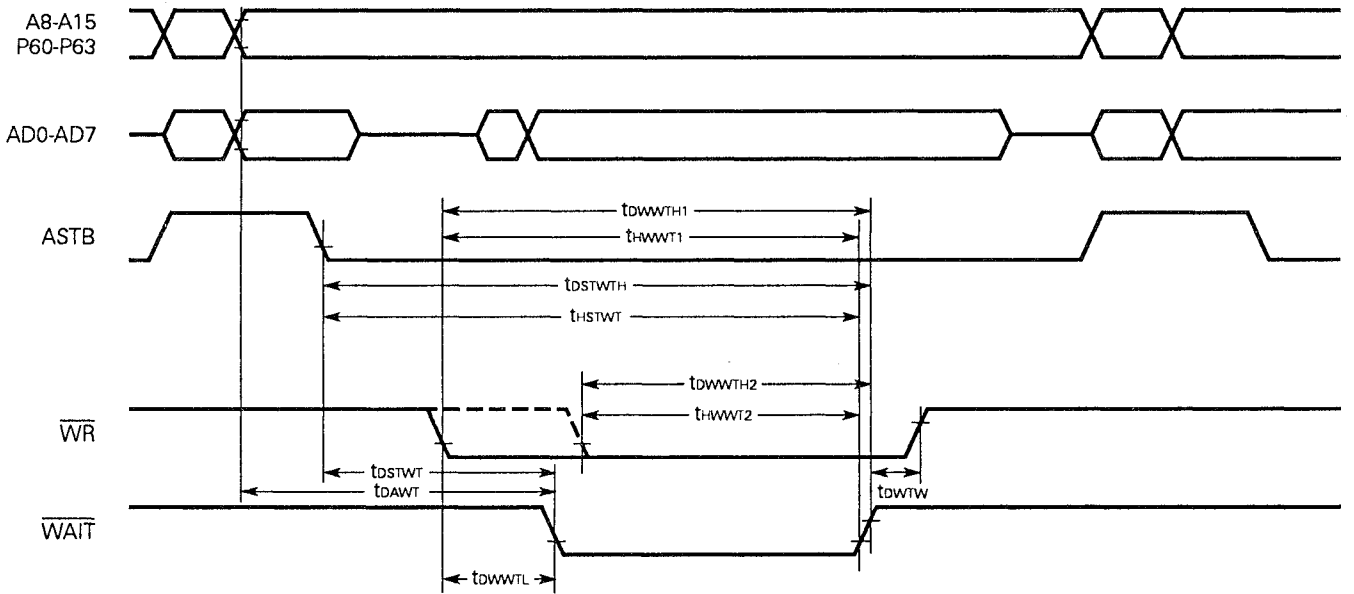


External WAIT Signal Input Timing

Read operation: ★

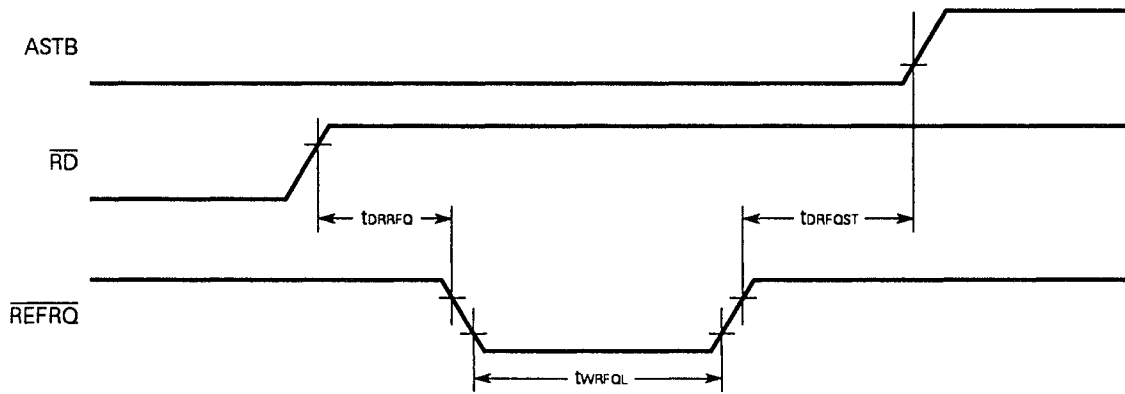


Write operation:

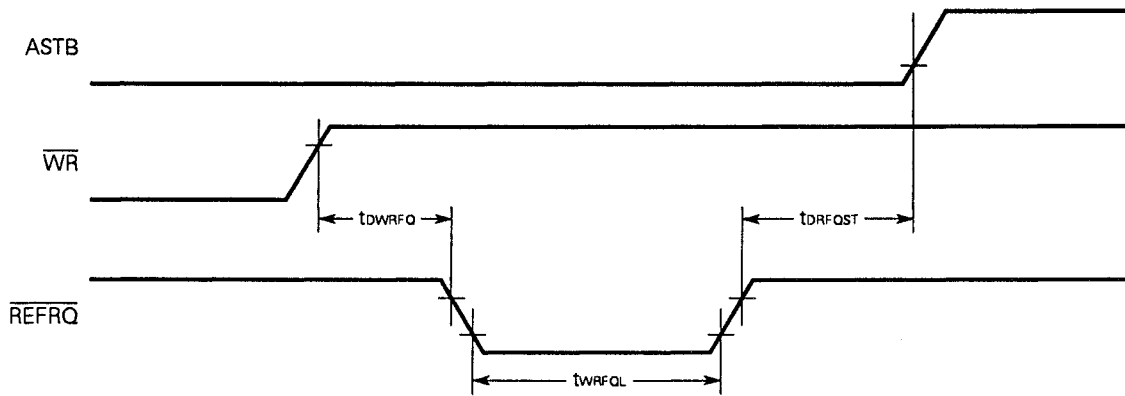


Timing Waveform for Refresh

Refresh after reading:

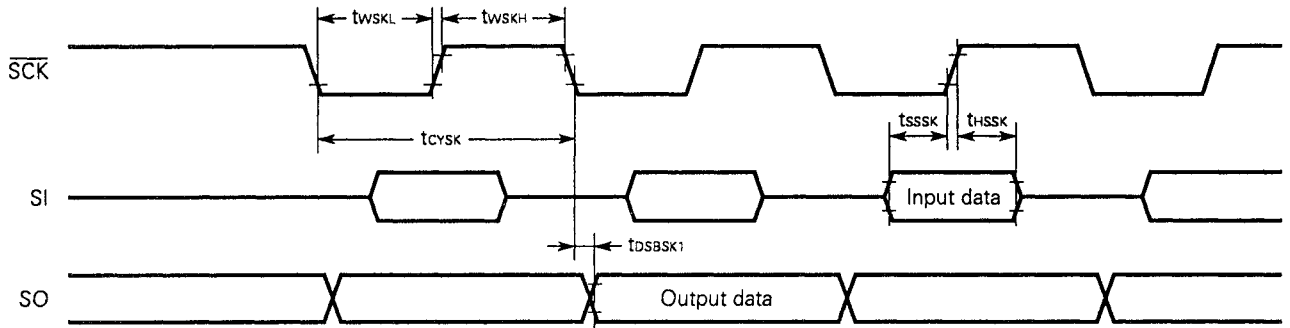


Refresh after writing:



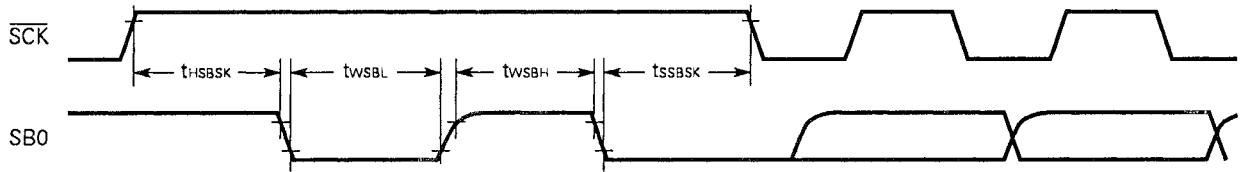
**Serial Operation**

**Three-wire serial I/O mode:**

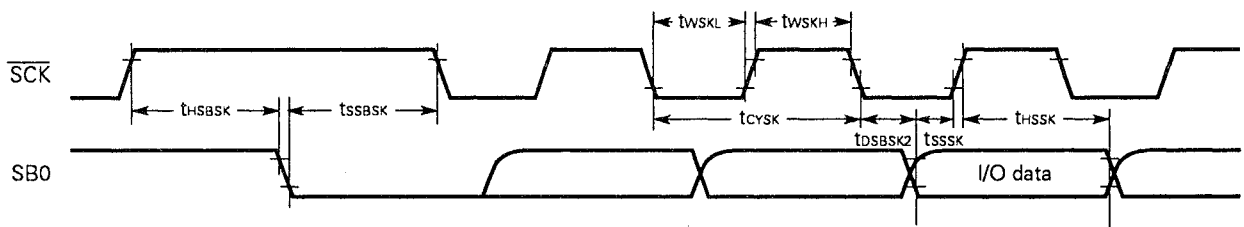


**SBI Mode**

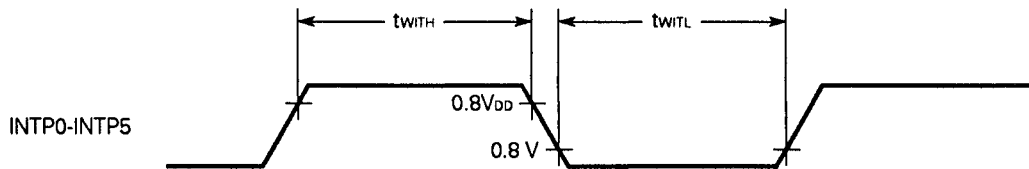
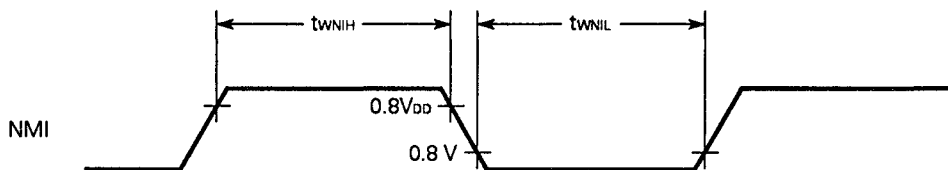
**Bus release signal transfer:**



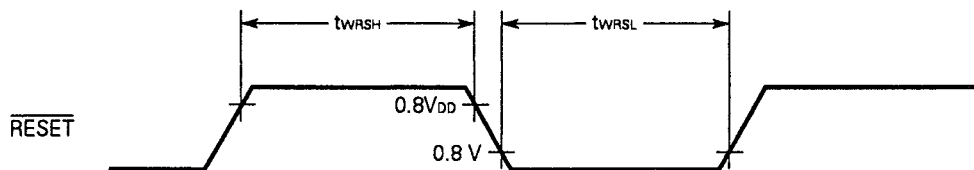
**Command signal transfer:**



**Interrupt Input Timing**

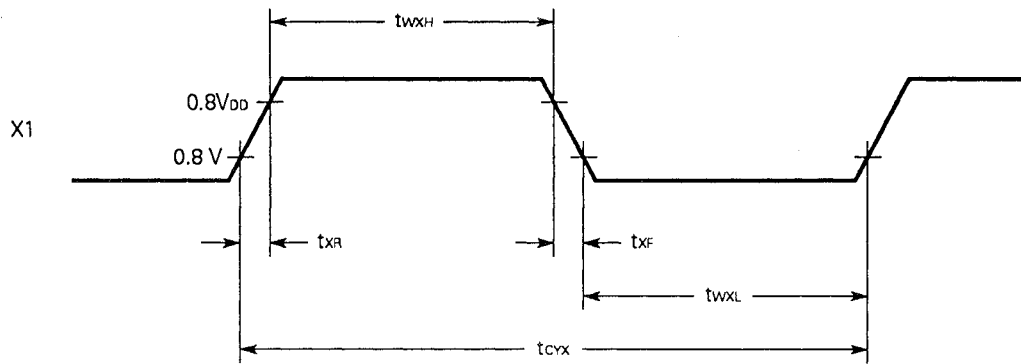


**Reset Input Timing**

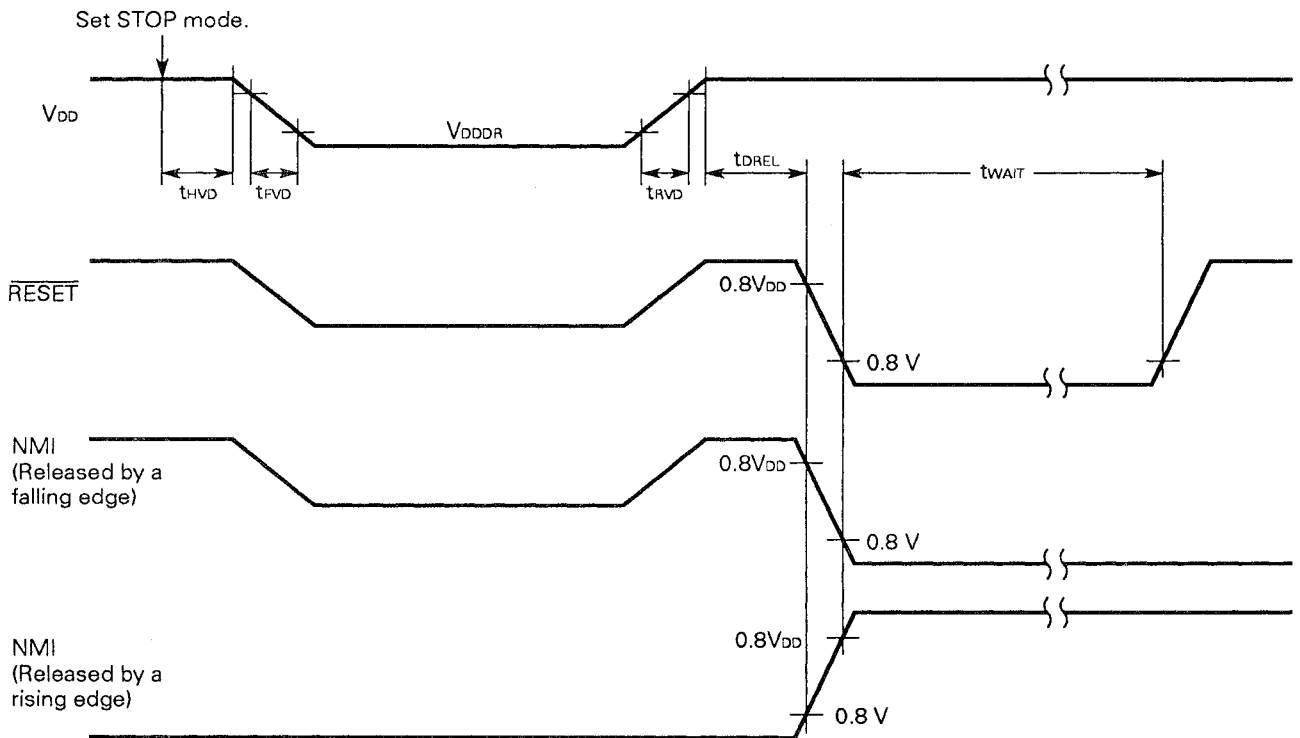




External Clock Timing



Data Retention Timing



DC PROGRAMMING CHARACTERISTICS (T<sub>a</sub> = 25 ± 5 °C, V<sub>PP</sub> ≥ 4.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Symbol Note	Conditions	Min.	Typ.	Max.	Unit
High-level input voltage	V <sub>IH</sub>	V <sub>IH</sub>		2.4		V <sub>DDP</sub> + 0.3	V
Low-level input voltage	V <sub>IL</sub>	V <sub>IL</sub>		-0.3		0.8	V
Input leakage current	I <sub>LIP</sub>	I <sub>LI</sub>	0 ≤ V <sub>I</sub> ≤ V <sub>DDP</sub>			10	μA
High-level output voltage	V <sub>OH1</sub>	V <sub>OH1</sub>	I <sub>OH</sub> = -400 μA	2.4			V
	V <sub>OH2</sub>	V <sub>OH2</sub>	I <sub>OH</sub> = -100 μA	V <sub>DD</sub> - 0.7			V
Low-level output voltage	V <sub>OL</sub>	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA			0.45	V
Output leakage current	I <sub>LO</sub>		0 ≤ V <sub>O</sub> ≤ V <sub>DDP</sub> , $\overline{OE} = V_{IH}$			10	μA
V <sub>DDP</sub> supply voltage	V <sub>DDP</sub>	V <sub>CC</sub>	Program memory write mode	5.75	6.0	6.25	V
			Program memory read mode	4.5	5.0	5.5	V
V <sub>PP</sub> supply voltage	V <sub>PP</sub>	V <sub>PP</sub>	Program memory write mode	12.2	12.5	12.8	V
			Program memory read mode	V <sub>PP</sub> = V <sub>DDP</sub>			V
V <sub>DDP</sub> supply current	I <sub>DD</sub>	I <sub>CC</sub>	Program memory write mode		5	30	mA
			Program memory read mode $\overline{CE} = V_{IL}, V_I = V_{IH}$		5	30	mA
V <sub>PP</sub> supply current	I <sub>PP</sub>	I <sub>PP</sub>	Program memory write mode $\overline{CE} = V_{IL}, \overline{OE} = V_{IH}$		5	30	mA
			Program memory read mode		1	100	μA

Note Symbols for the corresponding μPD27C256A

**PROGRAM OPERATION**

**AC characteristics** ( $T_a = 25 \pm 5 \text{ }^\circ\text{C}$ ,  $V_{PP} \geq 4.5 \text{ V}$ ,  $V_{DD} = 6 \pm 0.25 \text{ V}$ ,  $V_{PP} = 12.5 \pm 0.3 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ )

Parameter	Symbol	Symbol Note	Conditions	Min.	Typ.	Max.	Unit
Address set up time (referred to $\overline{CE}\downarrow$ )	t <sub>SAC</sub>	t <sub>AS</sub>		2			μs
$\overline{OE}$ high level hold time (referred to input data disable)	t <sub>HOLD</sub>	t <sub>OES</sub>		2			μs
Input data setup time (referred to $\overline{CE}\downarrow$ )	t <sub>SIDC</sub>	t <sub>DS</sub>		2			μs
Address hold time (referred to $\overline{CE}\uparrow$ )	t <sub>HCA</sub>	t <sub>AH</sub>		2			μs
Input data hold time (referred to $\overline{CE}\uparrow$ )	t <sub>HCID</sub>	t <sub>DH</sub>		2			μs
Output data hold time (referred to $\overline{OE}\uparrow$ )	t <sub>HOOD</sub>	t <sub>DF</sub>		0		130	ns
V <sub>PP</sub> setup time (referred to $\overline{CE}\downarrow$ )	t <sub>SVPC</sub>	t <sub>VPS</sub>		1			ms
V <sub>DDP</sub> setup time (referred to $\overline{CE}\downarrow$ )	t <sub>SVDC</sub>	t <sub>VCS</sub>		1			ms
Initial program pulse width	t <sub>WL1</sub>	t <sub>PW</sub>		0.95	1.0	1.05	ms
Additional program pulse width	t <sub>WL2</sub>	t <sub>OPW</sub>		2.85		78.75	ms
Delay from $\overline{OE}\downarrow$ to data output time	t <sub>DOOD</sub>	t <sub>OE</sub>				150	ns

**Note** Symbols for corresponding μPD27C256A

**READ OPERATION**

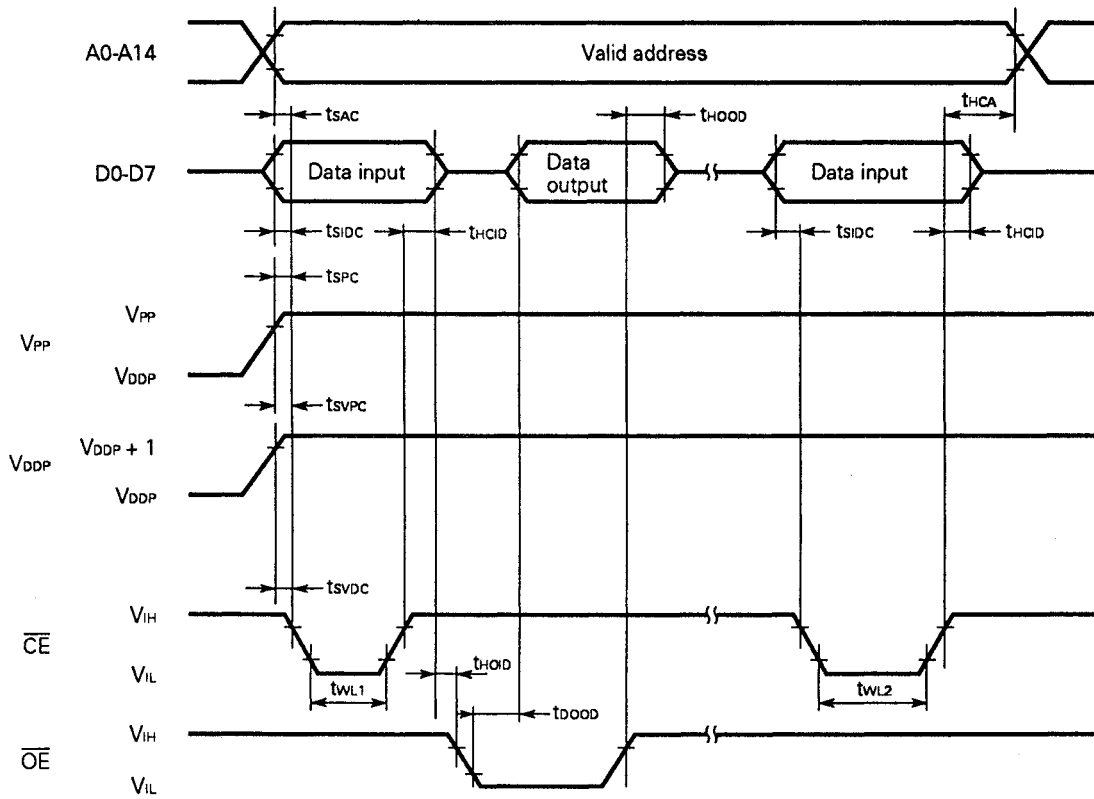
**AC characteristics** ( $T_a = 25 \pm 5 \text{ }^\circ\text{C}$ ,  $V_{PP} \geq 4.5 \text{ V}$ ,  $V_{DD} = 5 \pm 0.5 \text{ V}$ ,  $V_{PP} = V_{DDP}$ ,  $V_{SS} = 0 \text{ V}$ )

Parameter	Symbol	Symbol Note 1	Conditions	Min.	Typ.	Max.	Unit
Delay from address to data output	t <sub>DAOD</sub>	t <sub>ACC</sub>	$\overline{CE} = \overline{OE} = V_{IL}$			200	ns
Delay from $\overline{CE}\downarrow$ to data output	t <sub>DCOD</sub>	t <sub>CE</sub>	$\overline{OE} = V_{IL}$			200	ns
Delay from $\overline{OE}\downarrow$ to data output	t <sub>DOOD</sub>	t <sub>OE</sub>	$\overline{CE} = V_{IL}$			75	ns
Data hold time (referred to $\overline{OE}\uparrow$ or $\overline{CE}\uparrow$ ) <b>Note 2</b>	t <sub>HCOD</sub>	t <sub>DF</sub>	$\overline{CE} = V_{IL}$ or $\overline{OE} = V_{IL}$	0		60	ns
Data hold time (referred to address)	t <sub>HAOD</sub>	t <sub>OH</sub>	$\overline{CE} = \overline{OE} = V_{IL}$	0			ns

**Notes 1.** Symbols for the corresponding μPD27C256A

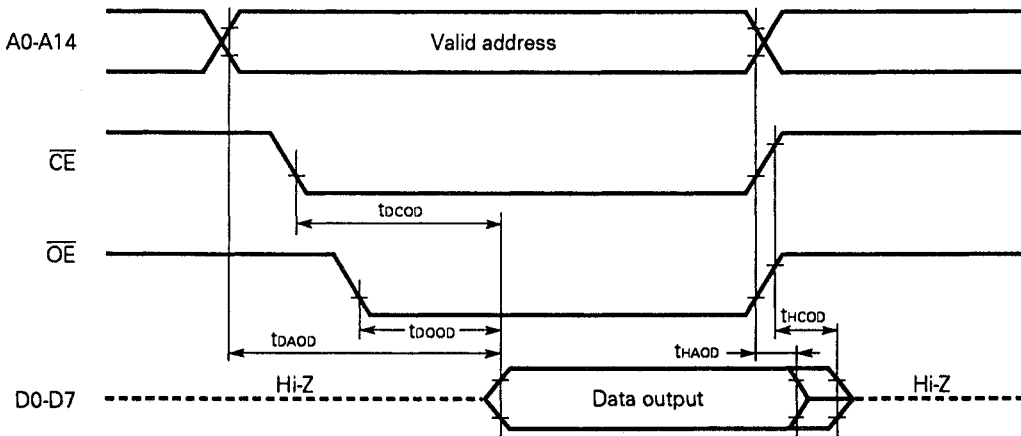
**2.** t<sub>HCOD</sub> is the time measured from when either  $\overline{OE}$  or  $\overline{CE}$  reaches  $V_{IH}$ , whichever is faster.

PROM Write Mode Timing

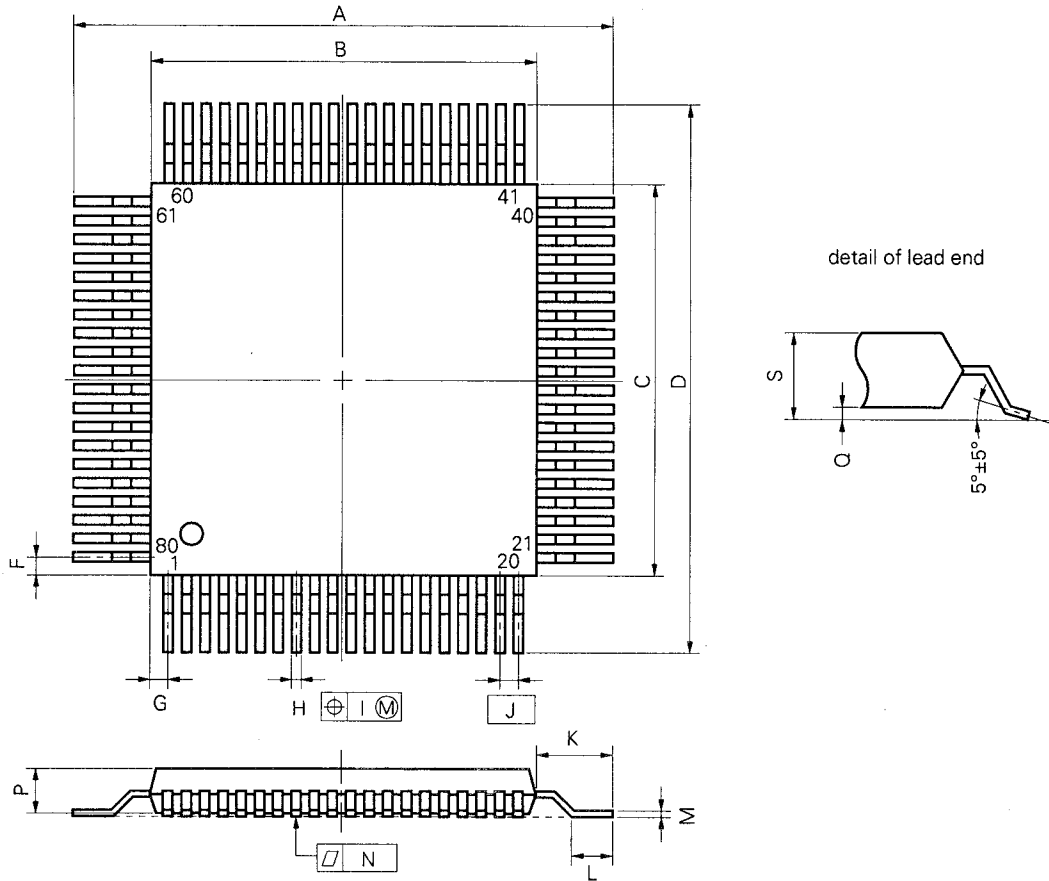


- Cautions 1.** VDDP must be applied before VPP, and must be cut after VPP.
- 2.** VPP including overshoot must not exceed +13 V.

PROM Read Mode Timing



8. PACKAGE DRAWINGS  
80 PIN PLASTIC QFP (□14)



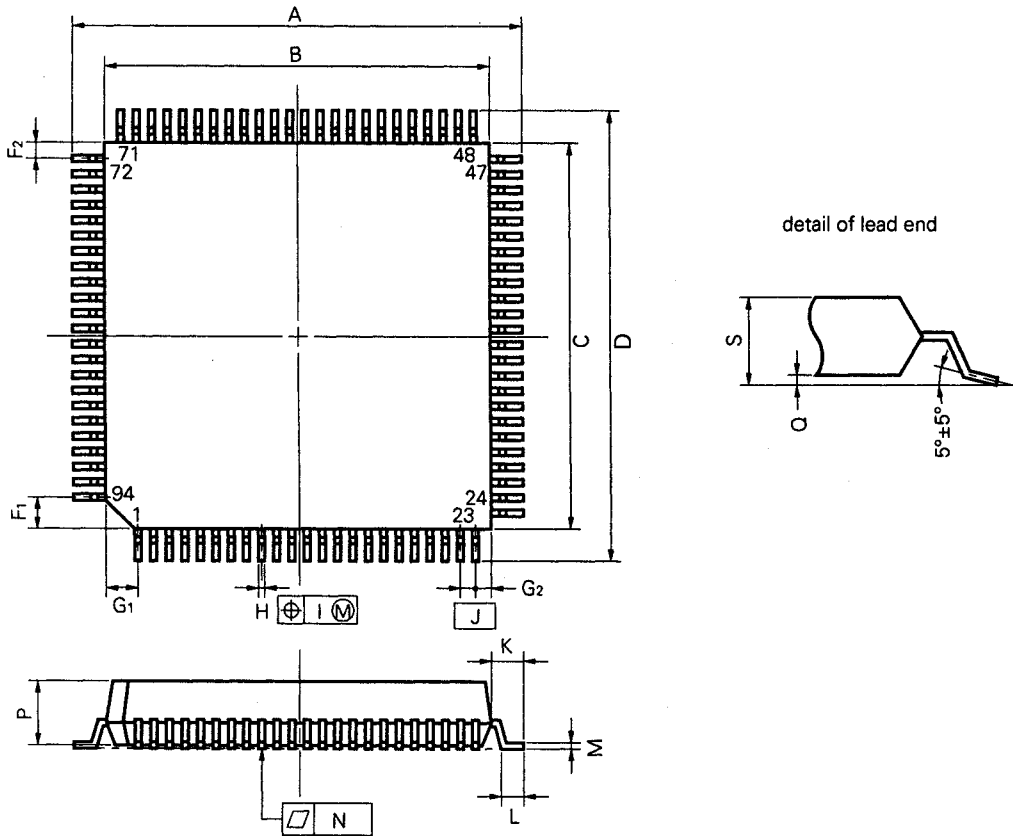
**NOTE**

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

S80GC-65-3B9-3

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	0.551 <sup>+0.009</sup> <sub>-0.008</sub>
C	14.0±0.2	0.551 <sup>+0.009</sup> <sub>-0.008</sub>
D	17.2±0.4	0.677±0.016
F	0.8	0.031
G	0.8	0.031
H	0.30±0.10	0.012 <sup>+0.004</sup> <sub>-0.005</sub>
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	0.031 <sup>+0.009</sup> <sub>-0.008</sub>
M	0.15 <sup>+0.10</sup> <sub>-0.05</sub>	0.006 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

94 PIN PLASTIC QFP (□20)



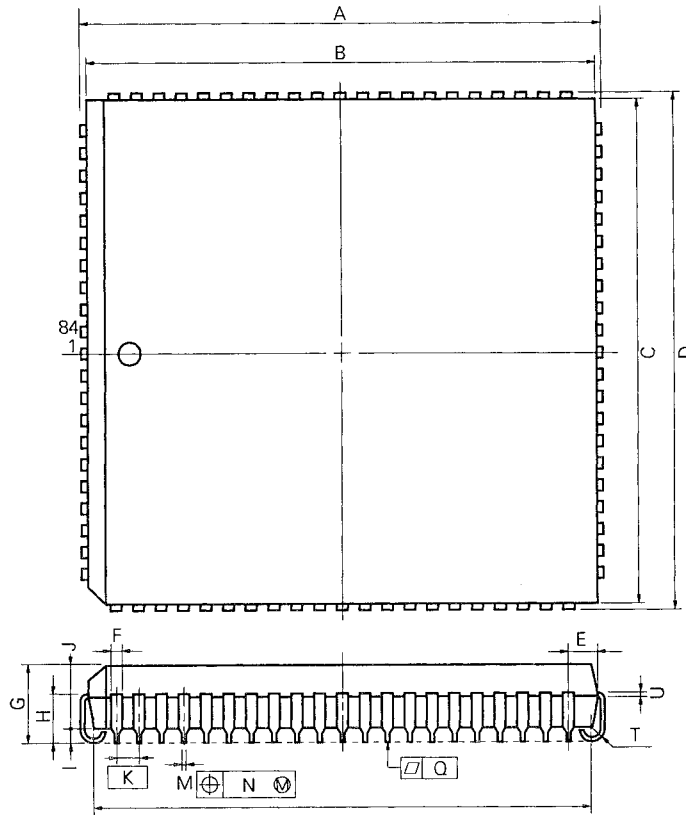
**NOTE**

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

S94GJ-80-5BG-2

ITEM	MILLIMETERS	INCHES
A	23.2±0.4	0.913 <sup>+0.017</sup> <sub>-0.016</sub>
B	20.0±0.2	0.787 <sup>+0.009</sup> <sub>-0.008</sub>
C	20.0±0.2	0.787 <sup>+0.009</sup> <sub>-0.008</sub>
D	23.2±0.4	0.913 <sup>+0.017</sup> <sub>-0.016</sub>
F <sub>1</sub>	1.6	0.063
F <sub>2</sub>	0.8	0.031
G <sub>1</sub>	1.6	0.063
G <sub>2</sub>	0.8	0.031
H	0.35±0.10	0.014 <sup>+0.004</sup> <sub>-0.005</sub>
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	0.031 <sup>+0.009</sup> <sub>-0.008</sub>
M	0.15 <sup>+0.10</sup> <sub>-0.05</sub>	0.006 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.12	0.005
P	3.7	0.146
Q	0.1±0.1	0.004±0.004
S	4.0 MAX.	0.158 MAX.

84 PIN PLASTIC QFJ (□1150 mil)



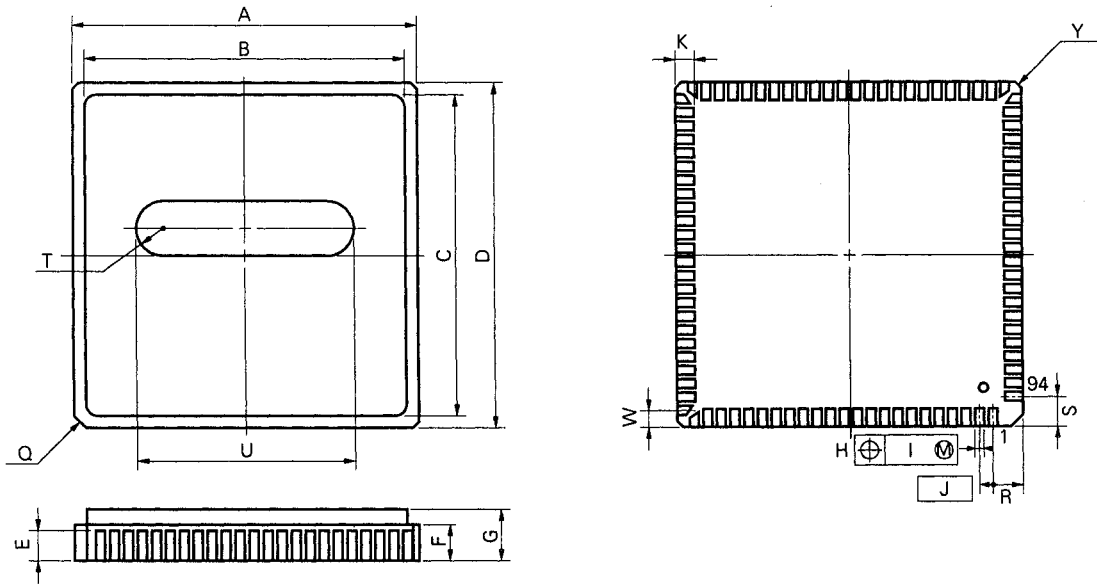
P84L-50A3-2

**NOTE**

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	30.2±0.2	1.189±0.008
B	29.28	1.153
C	29.28	1.153
D	30.2±0.2	1.189±0.008
E	1.94±0.15	0.076 <sup>+0.007</sup> <sub>-0.008</sub>
F	0.6	0.024
G	4.4±0.2	0.173 <sup>+0.009</sup> <sub>-0.008</sub>
H	2.8±0.2	0.110 <sup>+0.009</sup> <sub>-0.008</sub>
I	0.9 MIN.	0.035 MIN.
J	3.4	0.134
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	0.016 <sup>+0.004</sup> <sub>-0.005</sub>
N	0.12	0.005
P	28.20±0.20	1.110 <sup>+0.009</sup> <sub>-0.008</sub>
Q	0.15	0.006
T	R 0.8	R 0.031
U	0.20 <sup>+0.10</sup> <sub>-0.05</sub>	0.008 <sup>+0.004</sup> <sub>-0.002</sub>

94 PIN CERAMIC WQFN



**NOTE**

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

X94KW-80A-1

ITEM	MILLIMETERS	INCHES
A	20.0±0.4	0.787 <sup>+0.017</sup> <sub>-0.016</sub>
B	18.0	0.709
C	18.0	0.709
D	20.0±0.4	0.787 <sup>+0.017</sup> <sub>-0.016</sub>
E	1.94	0.076
F	2.14	0.084
G	4.064 MAX.	0.160 MAX.
H	0.51±0.10	0.020±0.004
I	0.08	0.003
J	0.8 (T.P.)	0.031 (T.P.)
K	1.0±0.2	0.039 <sup>+0.009</sup> <sub>-0.008</sub>
Q	C 1.0	C 0.039
R	1.6	0.063
S	1.6	0.063
T	R 1.75	0.069
U	11.5	0.453
W	0.75±0.2	0.030 <sup>+0.008</sup> <sub>-0.009</sub>



**9. RECOMMENDED SOLDERING CONDITIONS**

The following conditions (see table below) must be met when soldering this product.

For the details of the recommended soldering conditions refer to our document *SMD Surface Mount Technology Manual* (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

**Table 9-1 Soldering Conditions for Surface-Mount Devices**

**(1) μPD78P238GC-3B9: 80-pin plastic QFP (14 × 14 mm)**

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 230 °C Reflow time: 30 seconds or less (at 210 °C or more) Number of reflow processes: 1 Exposure limit: 2 days <sup>Note</sup> (16 hours of pre-baking is required at 125 °C afterward.)	IR30-162-1
VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (at 200 °C or more) Number of reflow processes: 1 Exposure limit: 2 days <sup>Note</sup> (16 hours of pre-baking is required at 125 °C afterward.)	VP15-162-1
Partial heating method	Terminal temperature: 300 °C or less Flow time: 3 seconds or less (for each side of device)	-

**(2) μPD78P238GJ-5BG: 94-pin plastic QFP (20 × 20 mm)**

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 230 °C Reflow time: 30 seconds or less (at 210 °C or more) Number of reflow processes: 1 Exposure limit: 7 days <sup>Note</sup> (10 hours of pre-baking is required at 125 °C afterward.)	IR30-107-1
VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (at 200 °C or more) Number of reflow processes: 1 Exposure limit: 7 days <sup>Note</sup> (10 hours of pre-baking is required at 125 °C afterward.)	VP15-107-1
Partial heating method	Terminal temperature: 300 °C or less Flow time: 3 seconds or less (for each side of device)	-

**(3) μPD78P238LQ: 84-pin plastic QFJ (1150 × 1150 mil)**

Soldering process	Soldering conditions	Symbol
VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (at 200 °C or more) Number of reflow processes: 1 Exposure limit: 7 days <sup>Note</sup> (10 hours of pre-baking is required at 125 °C afterward.)	VP15-107-1
Partial heating method	Terminal temperature: 300 °C or less Flow time: 3 seconds or less (for each side of device)	-

**Note** Exposure limit before soldering after dry-pack package is opened.

Storage conditions: Temperature of 25 °C and maximum relative humidity at 65 % or less

**Caution** Do not apply more than a single process at once, except for "Partial heating method."

**Notice**

Other versions of the products are available. For these versions, the recommended reflow soldering conditions have been mitigated as follows:  
Higher peak temperature (235 °C), two-stage, and longer exposure limit.  
Contact an NEC representative for details.

## APPENDIX A DEVELOPMENT TOOLS

The following tools are prepared for developing a system that uses the  $\mu$ PD78P238:

## Software for language processing

RA78K/II <sup>Note 1, Note 2</sup>	Assembler package used for all 78K/II series products
CC78K/II <sup>Note 1, Note 2</sup>	C compiler package used for all 78K/II series products
CC78K/II-L <sup>Note 1, Note 2</sup>	C compiler library source file used for all 78K/II series products

## PROM programming tools

PG-1500	PROM programmer
PA-78P238GC PA-78P238GJ PA-78P238KF PA-78P238LQ	Programmer adapter for connecting to the PG-1500
PG-1500 controller <sup>Note 1</sup>	Control program for the PG-1500

## Debugging tools

IE-78230-R-A IE-78230-R <sup>Note 3</sup>	In-circuit emulator used for all $\mu$ PD78234 series products
IE-78200-R-BK	Break board used for all 78K/II series products
IE-78230-R-EM IE-78200-R-EM <sup>Note 3</sup>	Emulation board for evaluating $\mu$ PD78234 series products
EP-78230GC-R EP-78230GJ-R EP-78230LQ-R	Emulation probe used for all $\mu$ PD78234 series products
EV-9200G-94 EV-9200GC-80	Socket to be mounted on the circuit board of the user system. It is used for the 94-pin plastic QFP and 80-pin plastic QFP.
EV-9900	Jig for removing the $\mu$ PD78P238KF from the EV-9200G-94
SD78K/II <sup>Note 1</sup>	Screen debugger for the IE-78230-R-A
DF78230 <sup>Note 1</sup>	Device file for $\mu$ PD78234 series products

## Real-time OS

RX78K/II <sup>Note 1, Note 2</sup>	Real-time OS used for all 78K/II series products
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**Notes 1.** For the PC-9800 series (MS-DOS™) or IBM PC/AT™ (PC DOS™)

**2.** For the HP9000 series 300™ (HP-UX™), SPARCstation™ (Sun OST™), or EWS-4800 series™ (EWS-UX/V™)

**3.** For maintenance only

**Fuzzy inference development support system**

FE9000 <sup>Note 1</sup>	Tool for creating fuzzy knowledge data
FT9080 <sup>Note 1</sup>	Translator
FI78K/II <sup>Note 1</sup>	Fuzzy inference module
FD78K/II <sup>Note 1, Note 4</sup>	Fuzzy inference debugger

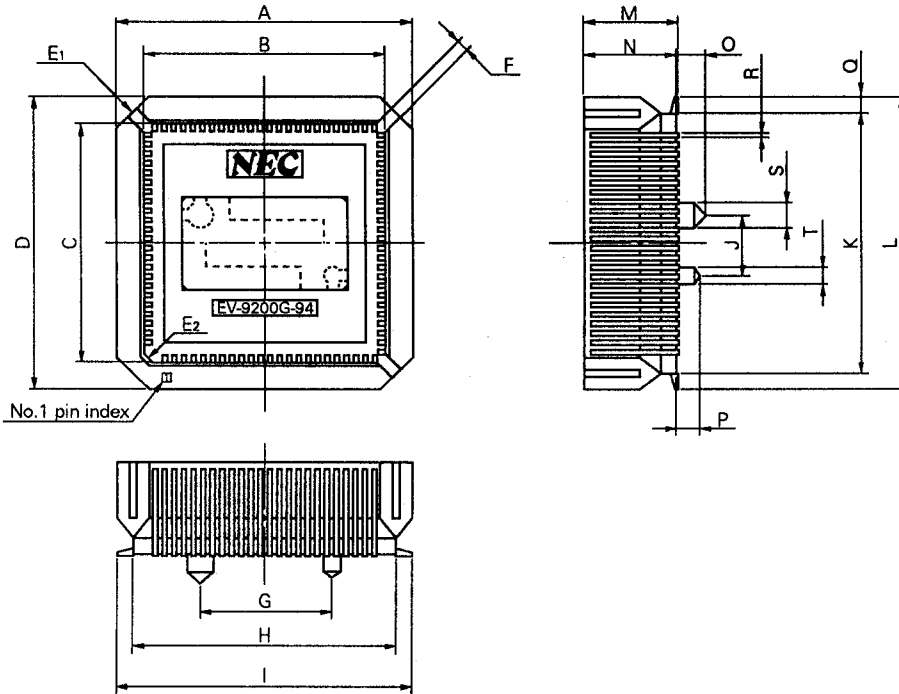
- Notes**
1. For the PC-9800 series (MS-DOS™) or IBM PC/AT™ (PC DOST™)
  2. For the HP9000 series 300™ (HP-UX™), SPARCstation™ (Sun OST™), or EWS-4800 series™ (EWS-UX/V™)
  3. For maintenance only
  4. Under development

**Remark** Refer to the *78K/II Series Development Tools Selection Guide* (EF-231) for development tools manufactured by third parties.

★ DRAWINGS OF THE CONVERSION SOCKET (EV-9200G-94) AND RECOMMENDED PATTERN ON BOARDS (UNIT: mm)

Fig. A-1 Drawings of the EV-9200G-94 (Reference)

Based on EV-9200G-94  
(1) Package drawing (in mm)

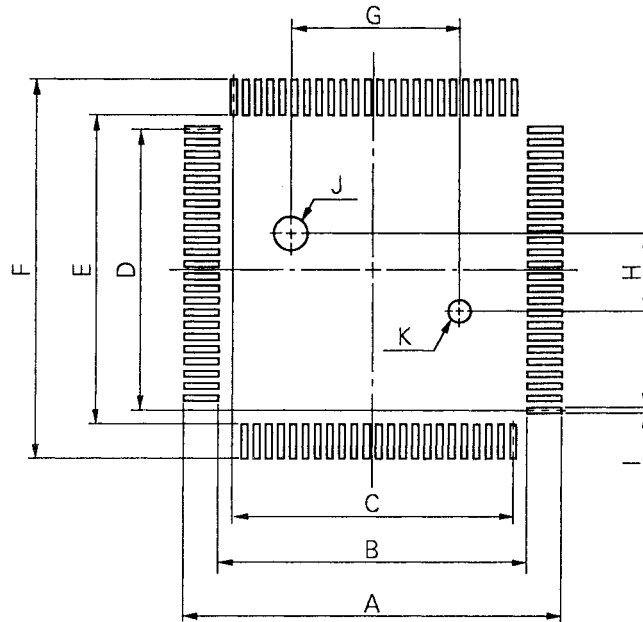


EV-9200G-94-G0

ITEM	MILLIMETERS	INCHES
A	25.0	0.984
B	20.35	0.801
C	20.35	0.801
D	25.0	0.984
E1	4-C 2.8	4-C 0.11
E2	C 1.5	C 0.059
F	0.8	0.031
G	11.0	0.433
H	22.0	0.866
I	24.7	0.972
J	5.0	0.197
K	22.0	0.866
L	24.7	0.972
M	8.0	0.315
N	7.8	0.307
O	2.5	0.098
P	2.0	0.079
Q	1.35	0.053
R	0.35±0.1	0.014 <sup>+0.004</sup> <sub>-0.005</sub>
S	φ2.3	φ0.091
T	φ1.5	φ0.059

Fig. A-2 Recommended Pattern on Boards for the EV-9200G-94 (Reference)

Based on EV-9200G-94  
(2) Pad drawing (in mm)



EV-9200G-94-P0

ITEM	MILLIMETERS	INCHES
A	25.7	1.012
B	21.0	0.827
C	$0.8 \pm 0.02 \times 23 = 18.4 \pm 0.05$	$0.031^{+0.002}_{-0.001} \times 0.906 = 0.724^{+0.003}_{-0.002}$
D	$0.8 \pm 0.02 \times 23 = 18.4 \pm 0.05$	$0.031^{+0.002}_{-0.001} \times 0.906 = 0.724^{+0.003}_{-0.002}$
E	21.0	0.827
F	25.7	1.012
G	$11.00 \pm 0.08$	$0.433^{+0.004}_{-0.003}$
H	$5.00 \pm 0.08$	$0.197^{+0.003}_{-0.004}$
I	$0.5 \pm 0.02$	$0.02^{+0.001}_{-0.002}$
J	$\phi 2.36 \pm 0.03$	$\phi 0.093^{+0.001}_{-0.002}$
K	$\phi 1.57 \pm 0.03$	$\phi 0.062^{+0.001}_{-0.002}$

**Caution** Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

★ APPENDIX B RELATED DOCUMENTS

Documents related to the device

Document name		Document No.
μPD78234 Series User's Manual, Hardware		IEU-718
78K/II Series User's Manual, Instruction		IEU-754
78K/II Series Application Note	Basic	IEA-607
	Application	IEA-700
	Floating-Point Arithmetic Operation Programs	IEA-686
78K/II Series Selection Guide		IF-304
78K/II Series Instruction Set		IEM-5102
μPD78234 Series Special Function Registers		IEM-5515

Documents related to development tools (user's manual)

Document name		Document No.
RA78K Series Assembler Package	Operation	EEU-809
	Language	EEU-815
RA78K Series Structured Assembler Preprocessor		EEU-817
CC78K Series C Compiler	Operation	EEU-656
	Language	EEU-655
CC78K Series Library Source File		EEU-777
PG-1500 PROM Programmer		EEU-651
PG-1500 Controller		EEU-704
IE-78230-R-A In-Circuit Emulator		EEU-789
IE-78230-R In-Circuit Emulator	Hardware	EEU-682
	Software	EEU-685
SD78K/II Screen Debugger	Tutorial	EEU-841
	Reference	EEU-813
78K/II Series Development Tools Selection Guide		EF-231

**Caution** The above documents may be revised without notice. Use the latest versions when you design an application system.

**Documents related to software to be incorporated into the product (user's manual)**

Document name		Document No.
RX78K/II Real Time OS	Tutorial	EEU-910
	Installation	EE7-884
	Debugger	EEU-895
	Technical	EEU-885
Tool for Creating Fuzzy Knowledge Data		EEU-829
78K/0, 78K/II, and 87AD Series Fuzzy Inference Development Support System	Translator	EEU-862
78K/II Series Fuzzy Inference Development Support System	Fuzzy Inference Module	EEU-860
78K/II Series Fuzzy Inference Debugger		EEU-917

**Other documents**

Document name	Document No.
QTOP Microcomputer Pamphlet	IB-5040
Package Manual	IEI-1213
SMD Surface Mount Technology Manual	IEI-1207
Quality Grades on NEC Semiconductor Devices	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System	IEM-1203
Electrostatic Discharge (ESD) Test	MEM-1201
Guide to Quality Assurance for Semiconductor Devices	MEI-1202

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[MEMO]



**Cautions on CMOS Devices****① Countermeasures against static electricity for all MOSs**

**Caution** When handling MOS devices, take care so that they are not electrostatically charged. Strong static electricity may cause dielectric breakdown in gates. When transporting or storing MOS devices, use conductive trays, magazine cases, shock absorbers, or metal cases that NEC uses for packaging and shipping. Be sure to ground MOS devices during assembling. Do not allow MOS devices to stand on plastic plates or do not touch pins. Also handle boards on which MOS devices are mounted in the same way.

**② CMOS-specific handling of unused input pins**

**Caution** Hold CMOS devices at a fixed input level.

Unlike bipolar or NMOS devices, if a CMOS device is operated with no input, an intermediate-level input may be caused by noise. This allows current to flow in the CMOS device, resulting in a malfunction. Use a pull-up or pull-down resistor to hold a fixed input level. Since unused pins may function as output pins at unexpected times, each unused pin should be separately connected to the  $V_{DD}$  or GND pin through a resistor. If handling of unused pins is documented, follow the instructions in the document.

**③ Statuses of all MOS devices at initialization**

**Caution** The initial status of a MOS device is unpredictable when power is turned on.

Since characteristics of a MOS device are determined by the amount of ions implanted in molecules, the initial status cannot be determined in the manufacture process. NEC has no responsibility for the output statuses of pins, input and output settings, and the contents of registers at power on. However, NEC assures operation after reset and items for mode setting if they are defined.

When you turn on a device having a reset function, be sure to reset the device first.

[MEMO]

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Application examples recommended by NEC Corporation

Standard: Computer, Office equipment, Communication equipment, Test and Measurement equipment, Machine tools, Industrial robots, Audio and Visual equipment, Other consumer products, etc.

Special: Automotive and Transportation equipment, Traffic control systems, Antidisaster systems, Anticrime systems, etc.

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