NEC

MOS INTEGRATED CIRCUIT

μPD78P148

8 BIT SINGLE-CHIP MICROCOMPUTER

The μPD78P148 is produced by replacing the mask ROM in the μPD78146 and the μPD78148 with PROM. The μPD78146 and the μPD78148 were produced by substantially making the functions of the μPD78138 that is well received as a VCR servo control microcomputer powerful.

There are two types of built-in PROM: one-time PROM in which data can be written once, and EPROM to which programs can be re-written after previously written programs have been erased.

One-time PROM products are suited for system evaluation in development, manufacture of small quantities of multiple products, and early stage start-up of applications.

An external memory expansion function is not provided.

The following user's manual describes the details of functions. Be sure to read it before design.

- **μPD78148 User's Manual: IEU-1319**

FEATURES

- Pin compatible with the μPD78146 or the μPD78148
- Bulk program memory (PROM): 32768 × 8 bits
- 100-pin plastic QFP
  0.65 mm pitch, 14 × 20 mm excluding the dimensions of the pins
- Operational amplifiers: 2
- Serial interface: 2 channels
- 8-bit resolution A/D converter: 15 channels
- High-speed multiplier (hardware)
- Dual clock configuration
- Real-time output ports: 18
- More powerful super timer unit
- More powerful PWM output function (6 outputs in total)
- Hardware for receiving a remote controller signal
- PROM programming characteristics: Compatible with the μPD27C256A

APPLICATIONS

The μPD78P148 applies to system control or servo control of VCRs of normal type and camcoder type.

ORDERING INFORMATION

Part number	Package	Built-in ROM
μPD78P148GF-3BA	100-pin plastic QFP (14 × 20 mm)	One-time PROM
μPD78P148K	100-pin ceramic WQFN (14 × 20 mm)	EPROM

In this manual, the description of the PROM is for both a one-time PROM and EPROM.

The information in this document is subject to change without notice.

Document No. U10220EJ4V0DS00 (4th edition)
(Previous No. IC-2766)
Date Published September 1995 P
Printed in Japan

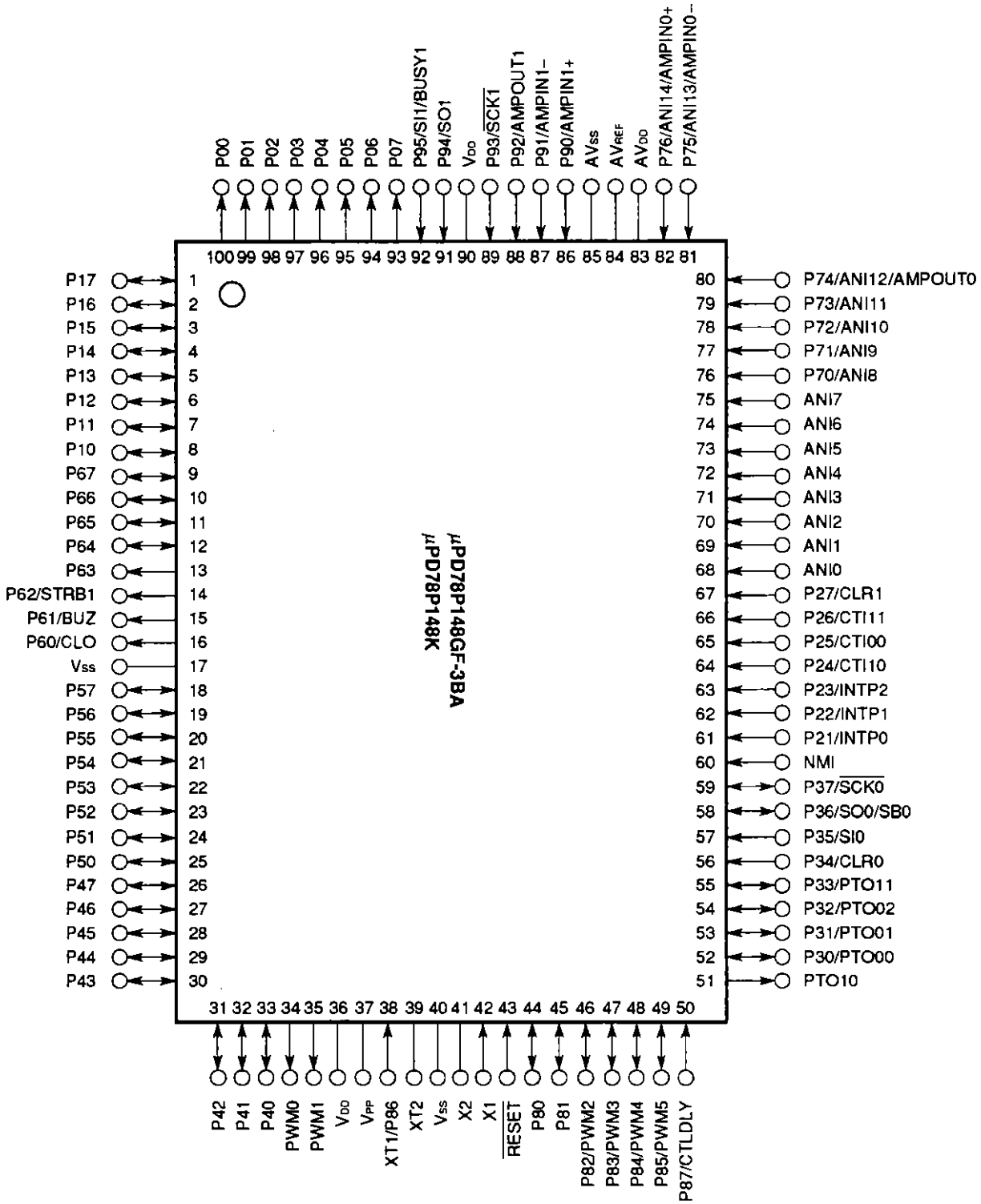
Major changes in this revision are indicated by stars (★) in the margins.

FUNCTIONAL OVERVIEW

Item	Function
Number of basic instructions	64
Minimum instruction execution time	0.33 μs (at 12 MHz)
Internal memory	• Program memory : 32768 × 8 bits (PROM) • Data memory : 816 × 8 bits
General register	8 bits × 8 × 4 banks (memory mapping)
Instruction set	• 16-bit addition, subtraction, comparison • Signed multiplication (signed 16 bits × unsigned 8 bits) • Unsigned multiplication/division (16 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (transfer, Boolean operation, set, reset, test)
I/O line	76 in total • Input port : 24 (10 ports can also be used as A/D converter input or analog pins for operational amplifiers.) • Output port : 12 • I/O port : 40
Super timer unit	• Timer : 16 bits × 3 8 bits × 3 • Counter : 22-bit free running counter (FRC) × 1 6-bit up/down counter (UDC) × 1 • Capture register : 22 bits × 2 16 bits × 3 8 bits × 2 • Compare register : 16 bits × 7 8 bits × 3 • PWM output : 12 bits × 2 (carrier frequency: 46.9/23.4 kHz) 14 bits × 1 (carrier frequency: 5.9 kHz) 8 bits × 3 (carrier frequency: 5.9 kHz)
Multiplier	Signed 16 bits × signed 16 bits. Operation time: 2.67 μs (at 12 MHz)
Real-time output port	• Timer-connected port output function • 18 built-in ports in total • The timer for an output trigger can be selected.
Serial interface	2 built-in channels • SIO0: Either NEC format serial bus interface (SBI) or 3-wire serial interface can be selected. • SIO1: Only a 3-wire serial interface is specified. The automatic data send/receive function is provided. (Send/receive buffer: 48 bytes)
A/D converter	8-bit resolution × 15 inputs (7 inputs can also be used as input ports.)
Analog circuit	2 operational amplifiers (Each amplifier can be used separately.)
Interrupt	• Interrupt source: 25 (5 external and 20 internal) • One of the two service modes can be selected (vector interrupt/macro service)
Clock	• Dual clock configuration (Either a main system clock or subsystem clock can be selected.) • Can perform counting in the standby mode.
Standby	STOP/HALT mode
Pull-up resistor	48, built-in (The use of built-in pull-up resistors can be specified by software.)

PIN CONFIGURATION (TOP VIEW)

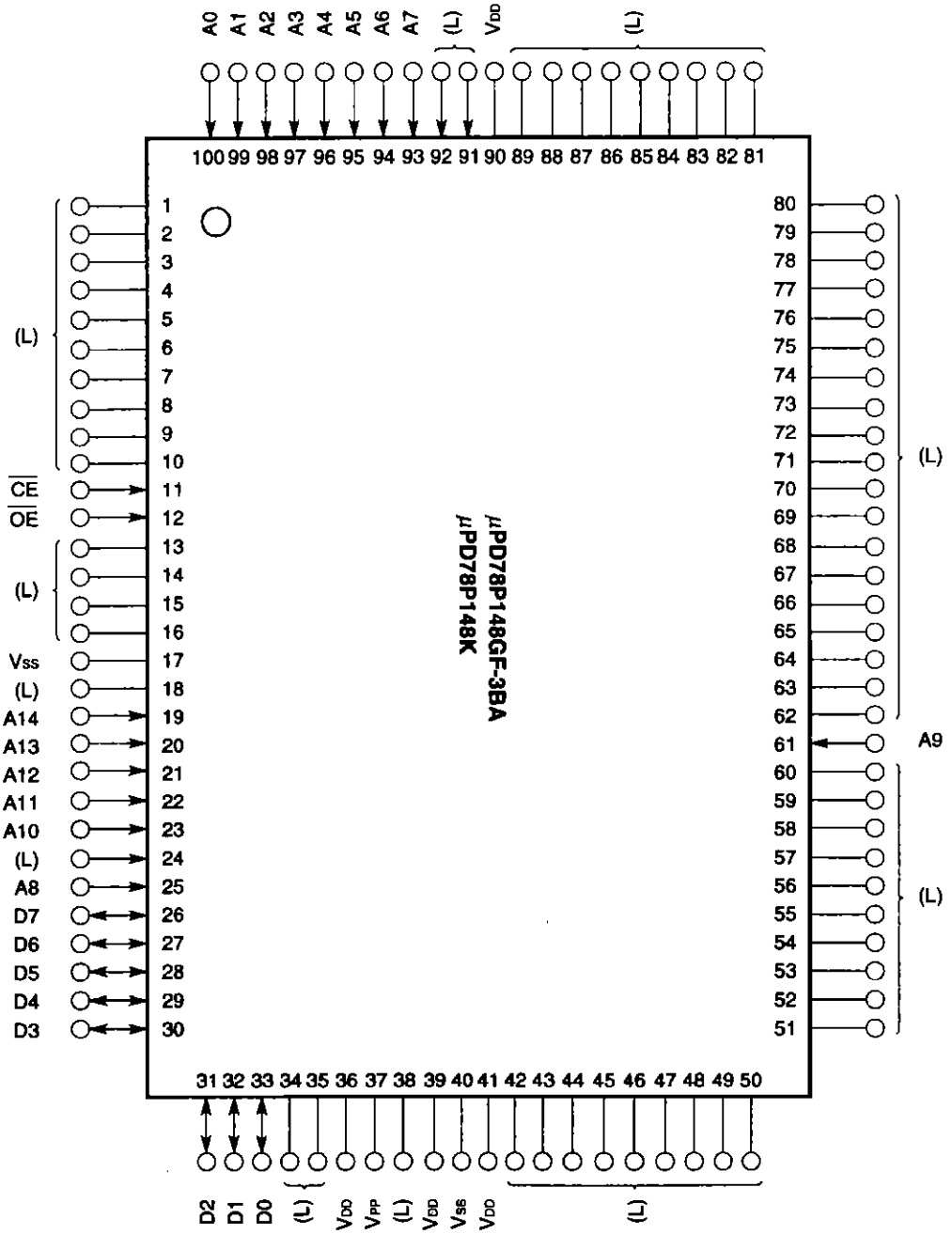
(1) Normal operation mode



Remark Connect V_{PP} to Vss in the normal operation mode.

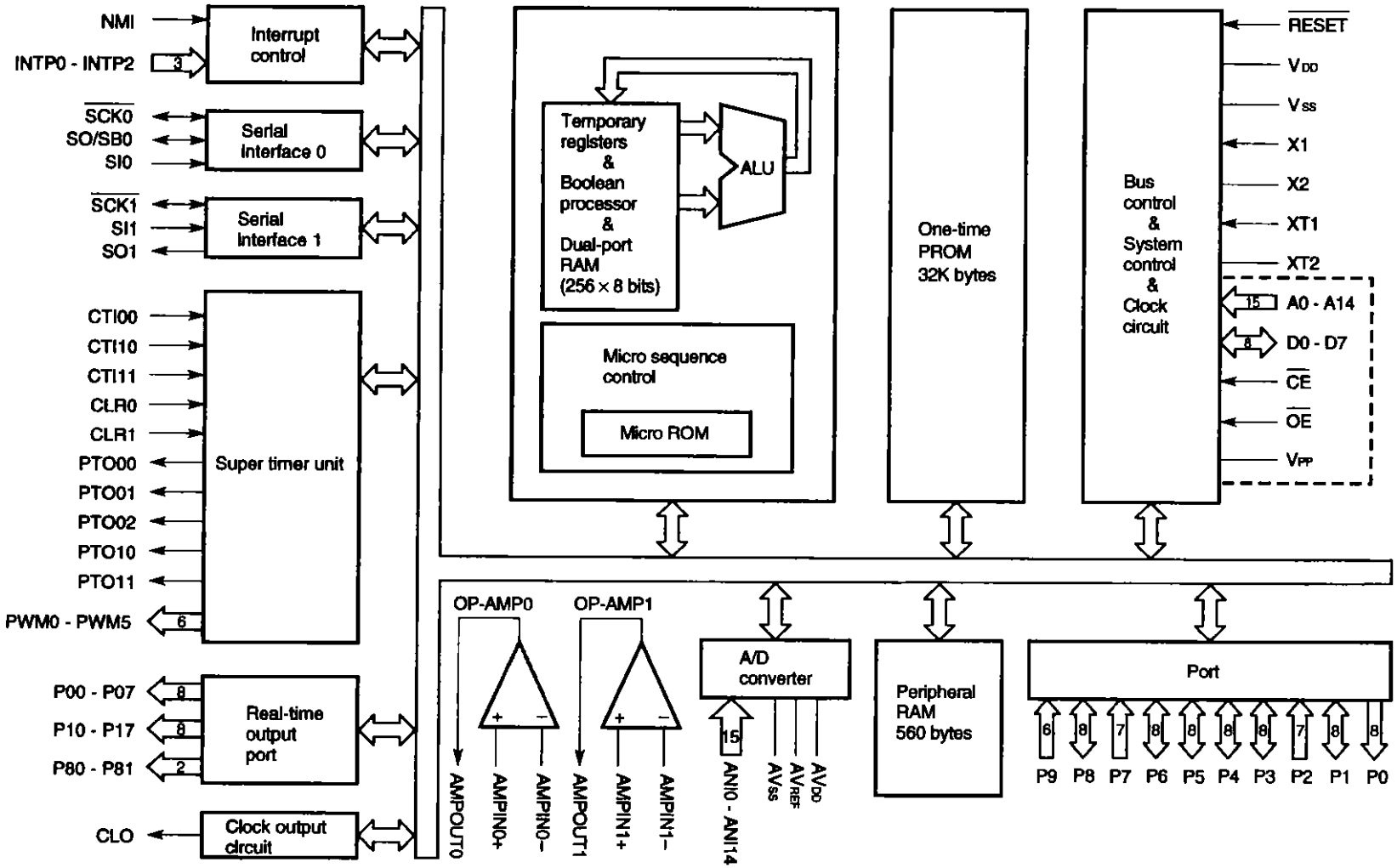
P00 - P07 : Port 0
P10 - P17 : Port 1
P21 - P27 : Port 2
P30 - P37 : Port 3
P40 - P47 : Port 4
P50 - P57 : Port 5
P60 - P67 : Port 6
P70 - P76 : Port 7
P80 - P87 : Port 8
P90 - P95 : Port 9
PWM0 - PWM5 : Pulse width modulation output 0 - 5
CTI00, CTI10, CTI11
: Capture trigger input 00, 10, 11
CLR0, CLR1 : Timer clear input 0, 1
PTO00 - PTO02, PTO10, PTO11
: Programmable timer output 00 - 02, 10, 11
SI0, SI1 : Serial input 0, 1
SO0, SO1 : Serial output 0, 1
SB0 : Serial bus 0
$\overline{SCK0}$, $\overline{SCK1}$: Serial clock 0, 1
STRB1 : Serial data transfer strobe 1
CTLDLY : Control delay input
ANI0 - ANI14 : Analog input 0 - 14
AMPIN0–, AMPIN1–
: Analog amplifier 0, 1 input (–)
AMPIN0+, AMPIN1+
: Analog amplifier 0, 1 input (+)
AMPOUT0, AMPOUT1
: Analog amplifier 0, 1 output
NMI : Nonmaskable interrupt
INTP0 - INTP2 : Interrupt from peripherals 0 - 2
CLO : Clock output
BUZ : Buzzer clock
AV_{REF} : Analog reference voltage
AV_{DD} : Analog power supply
AVss : Analog ground
X1, X2 : Crystal 1, 2 (Main system clock)
XT1, XT2 : Crystal 1, 2 (Subsystem clock)
$\overline{RESET}$: Reset
V_{DD} : Power supply
Vss : Ground

(2) PROM programming mode



A0 - A14: Address $\overline{CE}$: Chip enable
D0 - D7 : Data $\overline{OE}$: Output enable

Cautions 1. (L) : Connect these pins separately to the Vss pins through pull-down resistors.
2. Vss : To be connected to the ground.



Remark The portion enclosed by a dashed line applies only in the PROM programming mode.

CONTENTS

1. PIN FUNCTIONS

1.1 PORT PINS (1/2)

Pin name	I/O	Dual-function pin	Function
P00 - P07	O	(A0 - A7)	Port 0 (P0): • Can be specified to output or high impedance in units of bits. • Also function as an 8 bits × 1 or 4 bits × 2 real-time output port.
P10 - P17	I/O	–	Port 1 (P1): • Can be specified to input or output bit by bit. • Can directly drive LED. • The use of built-in pull-up resistors can be specified by software (P10 - P17). • Can be specified as a real-time output port bit by bit.
P21	I	INTP0 (A9)	Port 2 (P2): • The use of built-in pull-up resistors can be specified by software (P22 - P27).
P22		INTP1	
P23		INTP2	
P24		CTI10	
P25		CTI00	
P26		CTI11	
P27		CLR1	
P30	I/O	PTO00	Port 3 (P3): P30 - P33: I/O port (Can be specified to input or output bit by bit.) P34, P35 : Input port P36, P37 : I/O port (Can be specified to input or output bit by bit.) • The use of built-in pull-up resistors can be specified by software (P30 - P37) .
P31		PTO01	
P32		PTO02	
P33		PTO11	
P34	I	CLR0	
P35		SI0	
P36	I/O	SO0/SB0	
P37		$\overline{SCK0}$	
P40 - P47	I/O	(D0 - D7)	Port 4 (P4): • Can be specified to input or output in units of 8 bits. • Can directly drive LED. • The use of built-in pull-up resistors can be specified by software (P40 - P47).
P50	I/O	(A8)	Port 5 (P5): • Can be specified to input or output bit by bit. • Can directly drive LED. • The use of built-in pull-up resistors can be specified by software (P50 - P57).
P51		–	
P52 - P56		(A10 - A14)	
P57		–	

Remark Pins in parentheses indicate the pins used in the PROM programming mode.

PORT PINS (2/2)

Pin name	I/O	Dual-function pin	Function
P60	O	CLO	Port 6 (P6): P60 - P63: Output port P64 - P67: I/O port (Can be specified to input or output bit by bit.) • The use of built-in pull-up resistors can be specified by software (P64 - P67).
P61		BUZ	
P62		STRB1	
P63		–	
P64	I/O	($\overline{OE}$)	
P65		($\overline{CE}$)	
P66, P67		–	
P70	I	ANI8	Port 7 (P7)
P71		ANI9	
P72		ANI10	
P73		ANI11	
P74		AMPOUT0/ANI12	
P75		AMPIN0–/ANI13	
P76		AMPIN0+/ANI14	
P80	I/O	–	Port 8 (P8): P80 - P85: I/O port (Can be specified to input or output bit by bit.) P86, P87 : Input port • The use of built-in pull-up resistors can be specified by software (P80 - P85). • P80 and P81 can be specified as a real-time output port bit by bit.
P81			
P82		PWM2	
P83		PWM3	
P84		PWM4	
P85		PWM5	
P86	I	XT1	
P87		CTLDLY	
P90	I	AMPIN1+	Port 9 (P9)
P91		AMPIN1–	
P92		AMPOUT1	
P93		$\overline{SCK1}$	
P94		SO1	
P95		SI1	

Remark Pins in parentheses indicate the pins used in the PROM programming mode.

1.2 NON-PORT PINS (IN THE NORMAL OPERATION MODE) (1/2)

Pin name	I/O	Dual-function pin	Function
PWM0, PWM1	O	–	Super timer unit PWM output
PWM2 - PWM5	O	P82 - P85	Super timer unit PWM output
CLR0	I	P34	Super timer unit input
CTI00		P25	
CLR1		P27	
CTI10		P24	
CTI11		P26	
PTO00	O	P30	Super timer unit output
PTO01		P31	
PTO02		P32	
PTO10		–	
PTO11	O	P33	Super timer unit output Can output the drive waveform corresponding to VISS/VASS postwriting.
SI0	I	P35	Serial data input 0
SO0	I/O	P36/SB0	Serial data output 0 (3-wire serial I/O mode)
SB0	I/O	P36/SO0	Serial data input/output 0 (SBI mode)
$\overline{SCK0}$	I/O	P37	Serial clock input/output 0
SI1	I	P95	Serial data input 1
SO1	O	P94	Serial data output 1
$\overline{SCK1}$	I/O	P93	Serial clock input/output 1
STRB1	O	P62	Strobe output during automatic SIO1 data transfer
NMI	I	–	Non-maskable interrupt request input
INTP0	I	P21 (A9)	External interrupt request input
INTP1		P22	
INTP2		P23	
CTLDLY	–	P87	External time constant circuit connection: The external time constant circuit of CR is connected to this pin when PTO11 is used as VISS/VASS postwriting.
CLO	O	P60	Clock output
ANI0 - ANI7	Analog input	–	Analog signal input to A/D converter
ANI8 - ANI11		P70 - P73	
ANI12		P74/AMPOUT0	
ANI13		P75/AMPIN0–	
ANI14		P76/AMPIN0+	

Remark Pins in parentheses indicate the pins used in the PROM programming mode.

NON-PORT PINS (IN THE NORMAL OPERATION MODE) (2/2)

Pin name	I/O	Dual-function pin	Function
AMPIN0–	Analog input	P75/ANI13	Inverted input to operational amplifier 0
AMPIN0+		P76/ANI14	Uninverted input to operational amplifier 0
AMPOUT0	O	P74/ANI12	Operational amplifier 0 output
AMPIN1–	Analog input	P91	Inverted input to operational amplifier 1
AMPIN1+		P90	Uninverted input to operational amplifier 1
AMPOUT1	O	P92	Operational amplifier 1 output
$\overline{\text{RESET}}$	I	–	Reset input
BUZ	O	P61	Buzzer output
AV_{DD}	–	–	Main power supply of an analog circuit
AV_{SS}	–	–	Ground potential of an analog circuit
AV_{REF}	–	–	Reference voltage input to A/D converter
X1	I	–	Crystal connection for main system clock oscillation.
X2	–		
XT1	I	P86	Crystal connection for subsystem clock oscillation.
XT2	–	–	Crystal connection for clock oscillation
V_{DD}	–	–	Main power supply of a digital circuit
V_{SS}	–	–	Ground potential of a digital circuit
(V_{PP})	–	–	Connect to V_{SS}.

Remark Pins in parentheses indicate the pins used in the PROM programming mode.

1.3 NON-PORT PINS (PROM PROGRAMMING MODE)

Pin name	I/O	Dual-function pin	Function
A0 - A7	I	P00 - P07	Address input
A8		P50	
A9		P21/INTP0	
A10 - A14		P52 - P56	
D0 - D7	I/O	P40 - P47	Data I/O
$\overline{\text{CE}}$	I	P65	Program pulse input
$\overline{\text{OE}}$	I	P64	Output enable input
V_{PP}		–	High-voltage application for writing or verifying a program
V_{DD}		–	Power supply
V_{SS}		–	GND potential

2. DIFFERENCES BETWEEN THE μPD78P148 AND μPD78146/μPD78148

The μPD78P148 is produced by replacing the mask ROM in the μPD78146 and μPD78148 with PROM. Table 2-1 shows the differences between these products.

Table 2-1 Differences between μPD78P148 and μPD78146/μPD78148

Item	μPD78P148	μPD78146	μPD78148
Program memory	• PROM • 32768 bytes	• Mask ROM • 24576 bytes	• Mask ROM • 32768 bytes
Internal memory size change register (IMS)	Provided (**Fig. 2-1** shows the format of IMS.)	Not provided	
Pin connection	In the μPD78P148, the functions to read/write the PROM are added to the pins.		

Fig. 2-1 Format of the Internal Memory Size Change Register (IMS)

	7	6	5	4	3	2	1	0	Address	When reset	R/W
IMS	ROM3	ROM2	ROM1	ROM0	RAM3	RAM2	RAM1	RAM0	FFCFH	FEH	W

RAM3	RAM2	RAM1	RAM0	Internal RAM size change
1	1	0	1	688 bytes
1	1	1	0	816 bytes
Other than above				Not to be set

ROM3	ROM2	ROM1	ROM0	Internal ROM size change
1	1	1	1	32768 bytes
1	1	1	0	24576 bytes
Other than above				Not to be set

3. PROM PROGRAMMING

The program memory in the μPD78P148 is an electrically writable PROM of 32768 × 8 bits. When programming this PROM, use the V_{PP} and $\overline{RESET}$ pins to set the μPD78P148 to the PROM programming mode. Table 3-1 lists the pins to be used in this mode.

The μPD78P148 provides programming characteristics compatibility with the μPD27C256A.

Table 3-1 Pin Functions in PROM Programming Mode

Pin	Function
$\overline{RESET}$	Low level pulse input to set the μPD78P148 to the PROM programming mode
V_{PP}	PROM programming voltage input
A0 - A14	Address input
D0 - D7	Data input (when writing), data output (when verifying or reading)
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
V_{DD}	Power supply input
V_{SS}	GND potential

3.1 PROM PROGRAMMING OPERATING MODE

When +6 V is applied to the V_{DD} pin and when +12.5 V is applied to the V_{PP} pin, the μPD78P148 enters the program write/verify mode. This mode varies to each operating mode shown in Table 3-2 according to how to set the $\overline{CE}$ and $\overline{OE}$ pins.

Setting the μPD78P148 to the read mode enables it to read the contents of PROM.

Table 3-2 Operating Modes for Programming on PROM

Mode \ Pin	$\overline{RESET}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{DD}	D0 - D7
Program write	L	L	H	+12.5 V	+6 V	Data Input
Program verify		H	L			Data output
Program inhibit		H	H			High impedance
Read		L	L	+5 V	+5 V	Data output
Output disable		L	H			High impedance
Standby		H	L/H			High impedance

Caution Do not set both $\overline{CE}$ and $\overline{OE}$ to L when V_{PP} is set to +12.5 V and V_{DD} to +6 V.

3.2 CONNECTION OF UNUSED PINS IN THE PROM PROGRAMMING MODE

Table 3-3 lists the connections of the pins not to be used in the PROM programming mode.

Table 3-3 Connection of Unused Pins in the PROM Programming Mode

Pin	Recommended connection of unused pins
X1	Connected to Vss via pull-down resistor
X2	Connected to V_{DD} via pull-up resistor
XT1/P86	Connected to Vss via pull-down resistor
XT2	Connected to V_{DD} via pull-up resistor
P00 - P07	Each pin is connected to Vss via pull-down resistor.
P10 - P17	
P22 - P27	
P30 - P33	
P34 - P37	
P51, P57	
P60 - P63	
P66, P67	
P70 - P76	
P80 - P85	
P87	
P90, P91	
P92 - P95	
AV_{DD}	
AV_{REF}	
ANI0 - ANI7	
AV_{SS}	
PTO10	
PWM0, PWM1	

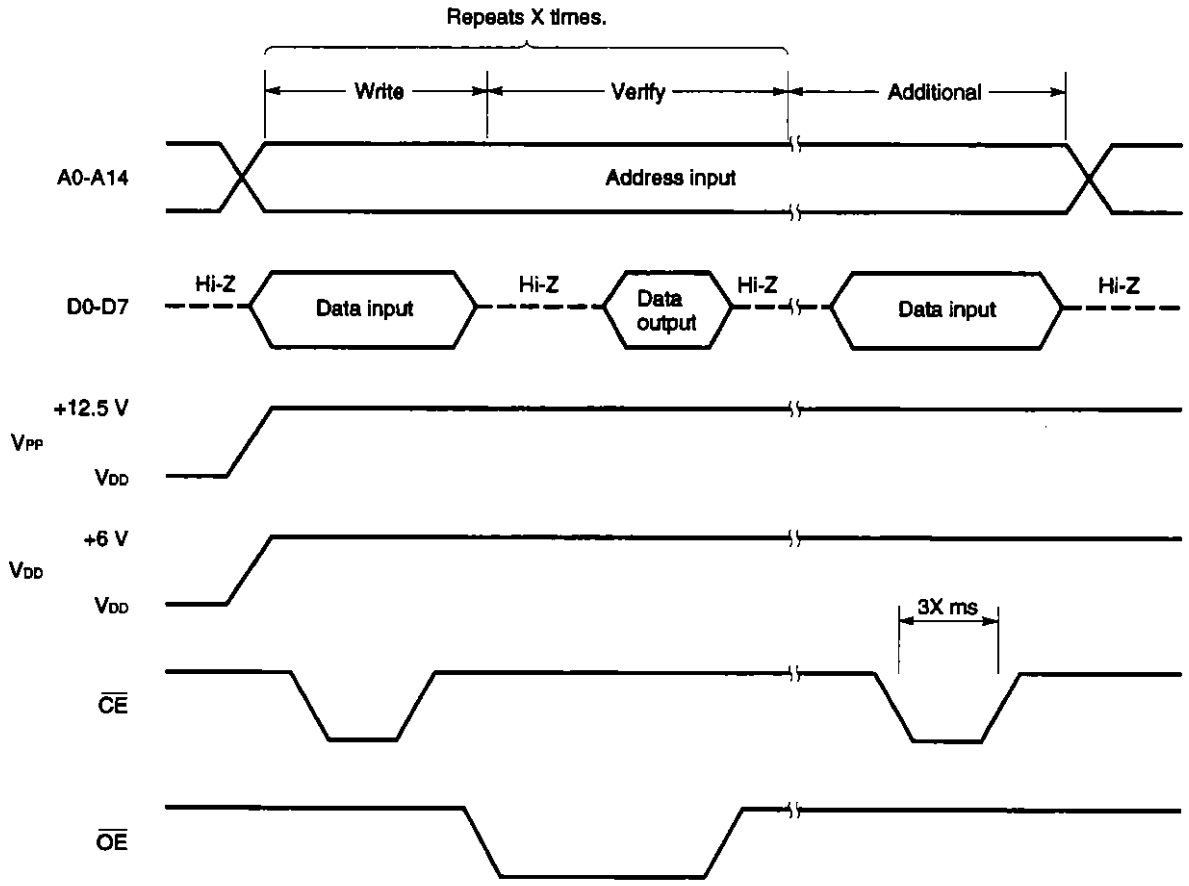
3.3 PROCEDURE FOR WRITING ON PROM

The following is a procedure for writing on PROM. Data can be written at high speed.

(1) Always set the $\overline{\text{RESET}}$ pin to low. Handle other unused pins as shown in Table 3-3.
(2) Apply +6 V to the V_{DD} pin and +12.5 V to the V_{PP} pin.
(3) Set an initial address.
(4) Input write data.
(5) Input a 1 ms program pulse (active low) to the $\overline{\text{CE}}$ pin.
(6) Verify mode: If data are written, go to step (8); if not, repeats steps (4) to (6). If no data are written yet after they are repeated 25 times, go to step (7).
(7) Assume the device to be defective and stop write operation.
(8) Input write data and a program pulse of (number of times steps (4) to (6) were repeated: X) × 3 ms (additional writing).
(9) Increment the address.
(10) Repeat steps (4) to (9) until the address exceeds the last address.

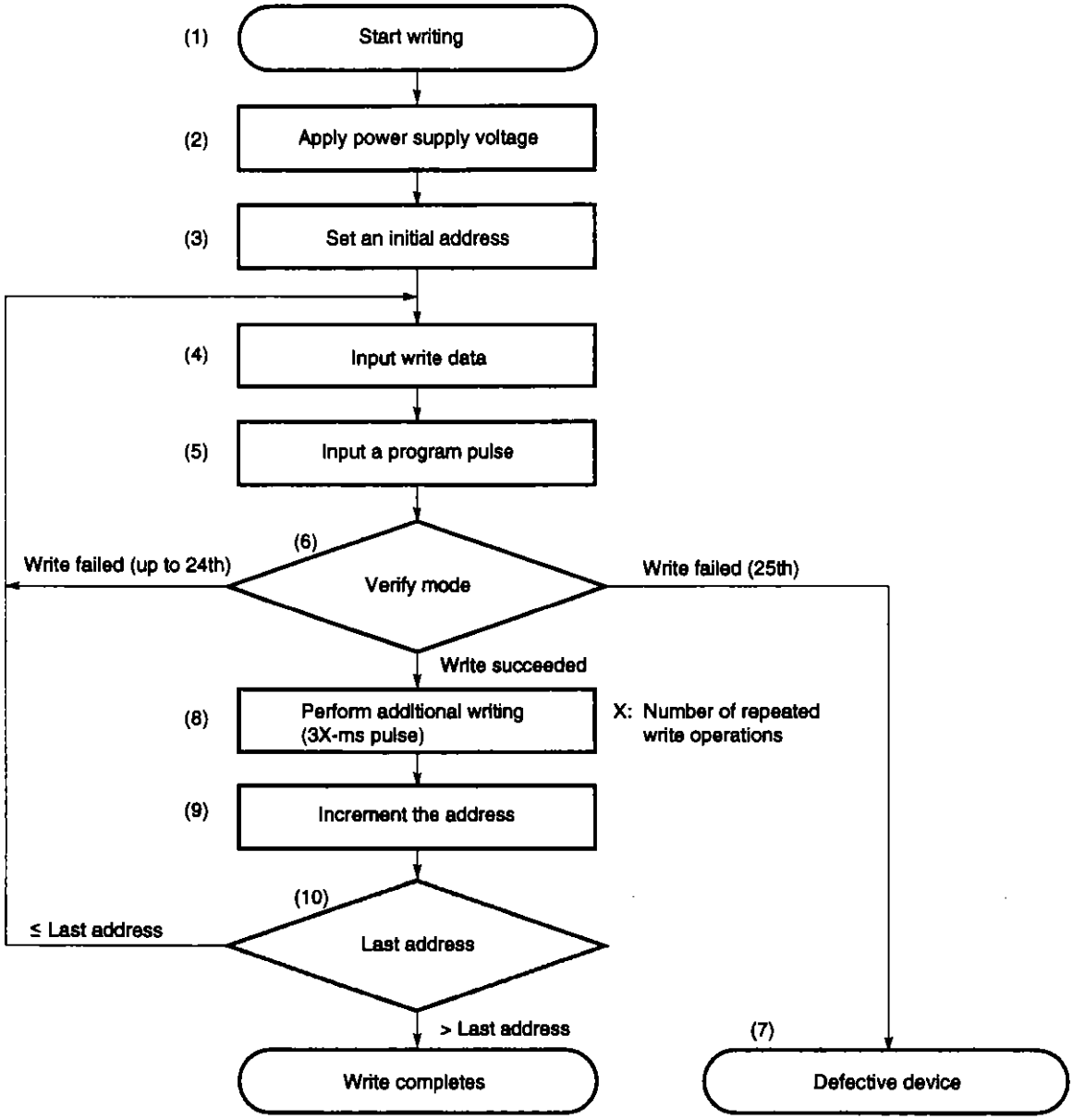
Fig. 3-1 is a timing chart of these steps (2) to (8).

Fig. 3-1 PROM Write/Verify Timing Chart



Cautions 1. V_{DD} must be applied before V_{PP}, and must be cut after V_{PP}.
2. V_{PP} including overshoot must not exceed +13 V.

Fig. 3-2 Flowchart of Procedure for Writing



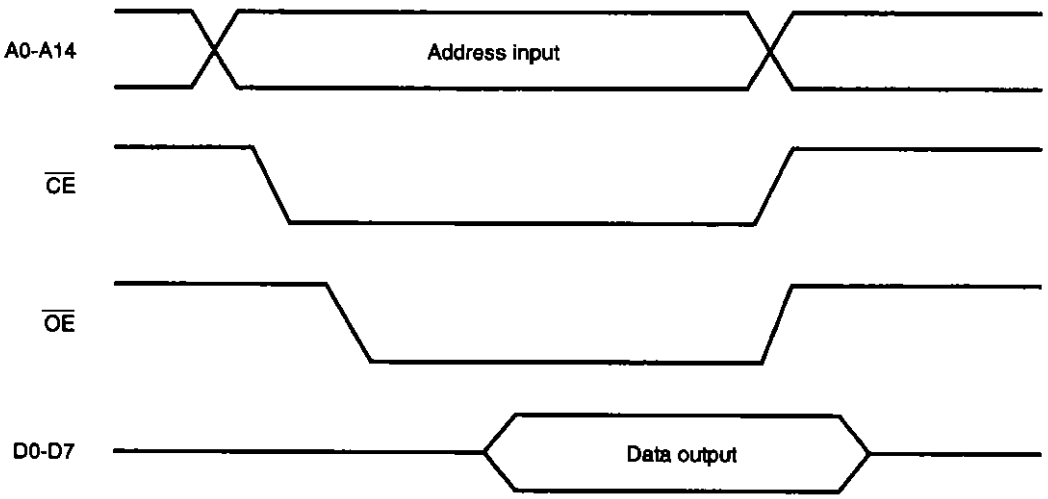
3.4 PROCEDURE FOR READING FROM PROM

The contents of PROM can be read out to the external data bus (D0 to D7) in the following steps:

(1) Always set the $\overline{\text{RESET}}$ pin to low. Handle other unused pins as shown in Table 3-3.
(2) Apply +5 V to the V_{DD} and V_{PP} pins.
(3) Input the address of data to be read into the A0 to A14 pins.
(4) Read mode
(5) Output the data on the D0 to D7 pins.

Fig. 3-3 is a timing chart of these steps (2) to (5).

Fig. 3-3 PROM Read Timing Chart



4. ERASURE CHARACTERISTICS ONLY FOR THE μPD78P148K

The programmed data of the μPD78P148K can be erased by exposure to light with a wavelength less than approx. 400 nm (all of the EPROM data are set to FFH).

To erase the contents of program memory in the μPD78P148K, expose the erasure window to ultraviolet light with the wavelength of 254 nm. The amount of light required to completely erase the contents of program memory is a minimum of 15 W•s/cm^2 (intensity of ultraviolet light × erasing time). It takes about 15 to 20 minutes to expose the erasure window to a 12000 μW/cm^2 ultraviolet lamp. It may, however, take more time due to the fallen performance of this ultraviolet lamp, dirt on the package window, or suchlike. Note that the μPD78P148K should be placed less than 2.5 cm from the ultraviolet lamp during erasure. In addition, if a filter is attached to the ultraviolet lamp, remove the filter before erasure.

5. PROTECTIVE FILM COVERING THE ERASURE WINDOW ONLY FOR THE μPD78P148K

The erasure window should be covered with a protective film when not erasing the contents of EPROM. This is to prevent the contents of memory from being erased erroneously by exposure to light other than the EPROM-contents erasing lamp. This is also to prevent any malfunction of the internal circuits other than the EPROM due to the light.

6. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}	$\|V_{DD} - AV_{DD}\| \le 0.5$ V	−0.5 to +7.0	V
	AV_{DD}		−0.5 to +7.0	V
	AV_{REF}	$V_{DD} \ge AV_{DD}$	−0.5 to AV_{DD} + 0.3	V
		$V_{DD} < AV_{DD}$	−0.5 to V_{DD} + 0.3	V
	AV_{SS}		−0.5 to + 0.5	V
Input voltage	V_I		−0.5 to V_{DD} + 0.5	V
Analog input voltage	V_{IAN}	$V_{DD} \ge AV_{DD}$	−0.5 to AV_{DD} + 0.5	V
		$V_{DD} < AV_{DD}$	−0.5 to V_{DD} + 0.5	V
Output voltage	V_O		−0.5 to V_{DD} + 0.5	V
Low-level output current	I_{OL}	1 pin	15	mA
		Total of all output pins	100	mA
High-level output current	I_{OH}	1 pin	−10	mA
		Total of all output pins	−50	mA
Operating ambient temperature	T_A		−10 to +70	°C
Storage temperature	T_{stg}		−65 to +150	°C

Caution If even one of the above parameters exceeds the absolute maximum rating (even momentarily), the product may deteriorate. It is also possible that the absolute maximum rating may physically damage the product. So be sure not to exceed the absolute maximum ratings when using the products.

OPERATING CONDITIONS

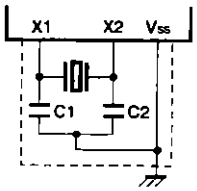
Clock frequency	Operating ambient temperature (T_A)	Supply voltage (V_{DD})
4 MHz ≤ f_{XX} ≤ 12 MHz	−10 to +70 °C	+4.5 V to +5.5 V
32 kHz ≤ f_{XT} ≤ 35 kHz		+2.0 V to +5.5 V (only for clock operation)

CAPACITANCE (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_I	fc = 1 MHz 0 V on pins other than measured pins			20	pF
Output capacitance	C_O				20	pF
I/O capacitance	C_{IO}				20	pF

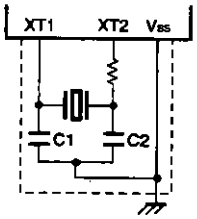
★ **OSCILLATOR CHARACTERISTICS (MAIN CLOCK)**

(T_A = −10 to +70 °C, V_{DD} = AV_{DD} = 5.0 V ±10 %, V_{SS} = AV_{SS} = 0 V)

Resonator	Recommended circuit	Parameter	Min.	Max.	Unit
Crystal resonator		Oscillation frequency (f_{XX})	4	12	MHz

★ **OSCILLATOR CHARACTERISTICS (SUBCLOCK)**

(T_A = −10 to +70 °C, V_{DD} = AV_{DD} = 2.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Resonator	Recommended circuit	Parameter	Min.	Max.	Unit
Crystal resonator		Oscillation frequency (f_{XT})	32	35	kHz

★ **Caution When the main system clock oscillator or the subsystem clock oscillator is used, conform to the following guidelines when wiring at the portions of surrounded by dotted lines in the figures above to eliminate the influence of the wiring capacity.**

- **The wiring must be as short as possible.**
- **Other signal lines must not run in these areas, and any line carrying a high fluctuating current must be kept away as far as possible.**
- **The grounding point of the capacitor of the oscillator must have the same potential as that of Vss. It must not be grounded to ground patterns carrying a large current.**
- **No signal must be taken from the oscillator.**

When the subsystem clock is used, pay special attention to its wiring since the subsystem clock oscillator has low amplification to minimize current consumption.

DC CHARACTERISTICS (T_A = −10 to +70 °C, V_{DD} = AV_{DD} = 5.0 V ±10 %, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Low-level input voltage	V_{IL}			0		0.8	V
High-level input voltage	V_{IH1}	Pins other than those shown in Note 1		2.2		V_{DD}	V
	V_{IH2}	Pins shown in Note 1	Note 2	0.8V_{DD}		V_{DD}	V
Low-level output voltage	V_{OL1}	I_{OL} = 2.0 mA				0.45	V
	V_{OL2}	I_{OL} = 8.0 mA	Note 3			1.00	V
High-level output voltage	V_{OH1}	I_{OH} = −1.0 mA		V_{DD} − 1.0			V
	V_{OH2}	I_{OH} = −100 μA		V_{DD} − 0.5			V
	V_{OH3}	I_{OH} = −5.0 mA	Note 4	2.0			V
Input leakage current	I_{LI}	0 V ≤ V_I ≤ V_{DD}				±10	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}				±10	μA
AV_{REF} current	AI_{REF}				0.2	1.0	mA
V_{DD} supply current	I_{DD1}	Operating mode, f_{XX} = 12 MHz			30	50	mA
	I_{DD2}	HALT mode, f_{XX} = 12 MHz			7	30	mA
Data retention voltage	V_{DDDR}	STOP mode		2.0			V
Data retention current Note 5, Note 6	I_{DD3}	STOP mode V_{DDDR} = 5.5 V	When the subclock operates		15	70	μA
			When the subclock does not operate		0.5	40	μA
		STOP mode V_{DDDR} = 3.0 V	When the subclock operates		3.0	14.0	μA
			When the subclock does not operate		0.3	8.0	μA
		STOP mode V_{DDDR} = 2.0 V	When the subclock operates		1.5	9.0	μA
			When the subclock does not operate		0.2	6.0	μA
Pull-up resistor	R_L	V_I = 0 V		15	30	80	kΩ

Notes 1. Pins X1, X2, $\overline{\text{RESET}}$, NMI, P21/INTP0, P22/INTP1, P23/INTP2, P24/CTI10, P25/CTI00, P26/CTI11, P27/CLR1, P34/CLR0, P35/SI0, P36/SO0/SB0, P37/$\overline{\text{SCK0}}$, P93/$\overline{\text{SCK1}}$, P95/SI1, and MODE

2. When using the XT1/P86 pin for input, disconnect the clock noise eliminator and feedback resistor.

3. Pins P10 - P17, P40 - P47, P50 - P57

4. Pins P00 - P07

5. Current through the AV_{REF} pin is excluded.

6. When the subclock is not operating in the STOP mode, disconnect the feedback resistor and clock noise eliminator, and connect the XT1 pin to V_{DD}.

DC CHARACTERISTICS (T_A = +25 °C, V_{SS} = AV_{SS} = 0 V)

Parameter		Symbol	Conditions		Min.	Type	Max.	Unit
Data retention current	Note1, Note2	I_{DD3}	STOP mode V_{DDDR} = 5.5 V	When the subclock operates		15.0	40.0	μA
				When the subclock does not operate		0.5	10.0	μA
			STOP mode V_{DDDR} = 3.0 V	When the subclock operates		3.0	10.0	μA
				When the subclock does not operate		0.3	5.0	μA
			STOP mode V_{DDDR} = 2.0 V	When the subclock operates		1.5	7.0	μA
				When the subclock does not operate		0.2	4.0	μA

Notes 1. Current through the AV_{REF} pin is excluded.

2. When the subclock is not operating in the STOP mode, disconnect the feedback resistor and clock noise eliminator and connect the XT1 pin to V_{DD}.

AC CHARACTERISTICS (T_A = −10 to +70 °C, V_{DD} = AV_{DD} = 5.0 V ±10 %, V_{SS} = AV_{SS} = 0 V)

Serial Interface

(1) Channel 0

Parameter	Symbol	Conditions		Min.	Max.	Unit
Serial clock cycle time	t_{CYSK0}	Input	External clock	1.0		μs
		Output	f_{CLK} divided by 8	1.3		μs
			f_{CLK} divided by 32	5.3		μs
Serial clock low-level width	t_{WSKL0}	Input	External clock	420		ns
		Output	f_{CLK} divided by 8	556		ns
			f_{CLK} divided by 32	2.5		μs
Serial clock high-level width	t_{WSKH0}	Input	External clock	420		ns
		Output	f_{CLK} divided by 8	556		ns
			f_{CLK} divided by 32	2.5		μs
SI0, SB0 setup time (to $\overline{SCK0}$ ↑)	t_{SSSK0}			150		ns
SI0, SB0 hold time (to $\overline{SCK0}$ ↑)	t_{HSSK0}			400		ns
SO0, SB0 output delay time (to $\overline{SCK0}$ ↓)	$t_{DSBSK01}$	CMOS push-pull output (Three-wire serial I/O mode)		0	300	ns
	$t_{DSBSK02}$	Open-drain output (SBI mode), R_L = 1 kΩ		0	800	ns
SB0 high hold time (to $\overline{SCK0}$ ↑)	t_{HSBSK0}	SBI mode		4t_{CYX}		ns
SB0 low setup time (to $\overline{SCK0}$ ↓)	t_{SSBSK0}			4t_{CYX}		ns
SB0 low-level width	t_{WSBL0}			4t_{CYX}		ns
SB0 high-level width	t_{WSBH0}			4t_{CYX}		ns

Remarks 1. The values listed in the above table are obtained when f_{XX} = 12 MHz and C_L = 100 pF.

★ **2.** f_{CLK} indicates the internal system clock (f_{XX} divided by 2).

★ **3.** t_{CYX} = 1/f_{XX}

(2) Channel 1

Parameter	Symbol	Conditions		Min.	Max.	Unit
Serial clock cycle time	t_{CYSK1}	External clock input	Automatic transfer	17t_{CYX}		ns
			Three-wire	13t_{CYX}		ns
		Output	f_{CLK} divided by 8	1.3		μs
			f_{CLK} divided by 32	5.3		μs
			f_{CLK} divided by 64	10.6		μs
Serial clock low-level width	t_{WSKL1}	External clock input	Automatic transfer	5t_{CYX}		ns
			Three-wire	5t_{CYX}		ns
		Output	f_{CLK} divided by 8	620		ns
			f_{CLK} divided by 32	2.6		μs
			f_{CLK} divided by 64	5.3		μs
Serial clock high-level width	t_{WSKH1}	External clock input	Automatic transfer	9t_{CYX}		ns
			Three-wire	5t_{CYX}		ns
		Output	f_{CLK} divided by 8	620		ns
			f_{CLK} divided by 32	2.6		μs
			f_{CLK} divided by 64	5.3		μs
SI1 setup time (to $\overline{SCK1}$ ↑)	t_{SSSK1}			100		ns
SI1 hold time (to $\overline{SCK1}$ ↑)	t_{HSSK1}			400		ns
SO1 output delay time (to $\overline{SCK1}$ ↓)	t_{DSBSK1}			0	300	ns
$\overline{SCK1}$(8) ↑ → STRB1 ↑	t_{DSTRB1}			t_{WSKH1}	t_{CYSK1}	
Strobe signal high-level width	t_{WSTRB1}			t_{CYSK1} − 30	t_{CYSK1} + 30	ns
BUSY1 setup time referred to BUSY1 detection	t_{SBUSY1}			100		ns
BUSY1 hold time referred to BUSY1 detection	t_{HBUSY1}			100		ns
BUSY inactive → $\overline{SCK1}$(1) ↓	t_{LBUSY1}				t_{CYSK1} + t_{WSKH1}	

Remarks 1. The values listed in the above table are obtained when fxx = 12 MHz and C_L = 100 pF.

2. f_{CLK} indicates the internal system clock (fxx divided by 2). ★

3. t_{CYK} = 1/fxx ★

4. The parenthesized number as in $\overline{SCK1}$(n) indicates that n−1 $\overline{SCK1}$ pulses precede this particular $\overline{SCK1}$(n) pulse.

5. $\overline{BUSY1}$ is detected when (n+2) × t_{CYSK1} has passed after $\overline{SCK1}$(8) ↑ (n = 0, 1, ···).

OTHER OPERATIONS (T_A = −10 to +70 °C, V_{DD} = AV_{DD} = 5.0 V ±10 %, V_{SS} = AV_{SS} = 0 V)

Parameter		Symbol	Conditions	Min.	Max.	Unit
CTI00, CTI10, CTI11 low-level width		t_{WCTL}		4t_{CYX}		ns
CTI00, CTI10, CTI11 high-level width		t_{WCTH}		4t_{CYX}		ns
CLR1 low-level width		t_{WCR1L}	Digital noise elimnator not used	4t_{CYX}		ns
			Digital noise eliminator used ICR bit 4 = 0	160t_{CYX}		ns
			Digital noise eliminator used ICR bit 4 = 1	256t_{CYX}		ns
CLR1 high-level width		t_{WCR1H}	Digital noise elimnator not used	4t_{CYX}		ns
			Digital noise eliminator used ICR bit 4 = 0	160t_{CYX}		ns
			Digital noise eliminator used ICR bit 4 = 1	256t_{CYX}		ns
Digital noise eliminator	Removed pulse width	t_{WSEP}	ICR bit 4 = 0		152t_{CYX}	ns
			ICR bit 4 = 1		248t_{CYX}	ns
	Passed pulse width		ICR bit 4 = 0	160t_{CYX}		ns
			ICR bit 4 = 1	256t_{CYX}		ns
H_{SYNC} synchronization time (CLR1 ↑ → H_{SYNC} ↓)		t_{DHS}	ICR bit 4 = 0	772t_{CYX}	778t_{CYX}	ns
			ICR bit 4 = 1	760t_{CYX}	766t_{CYX}	ns
★ H_{SYNC} cycle time		t_{CYCHS}	When f_{XX} is 12 MHz	63.5		μs
★ H_{SYNC} active level width		t_{WHS}	When f_{XX} is 12 MHz	5		μs
NMI low-level width		t_{WNIL}		10		μs
NMI high-level width		t_{WNIH}		10		μs
INTP0 - INTP2 low-level width		t_{WIPL}		4t_{CYX}		ns
INTP0 - INTP2 high-level		t_{WIPH}		4t_{CYX}		ns
$\overline{RESET}$ low-level width		t_{WRSL}		10		μs

★ **Remark** t_{CYX} = 1/f_{XX}

CLOCK OUTPUT OPERATION (T_A = −10 to +70 °C, V_{DD} = AV_{DD} = 5.0 V ±10 %, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Calculation formula	Min.	Max.	Unit
CLO cycle time	t_{CYCL}		333	2667	ns
CLO low-level width	t_{CLL}	t_{CYCL}/2 ±50	116	1384	ns
CLO high-level width	t_{CLH}	t_{CYCL}/2 ±50	116	1384	ns
CLO rising time	t_{CLR}			50	ns
CLO falling time	t_{CLF}			50	ns

Remark The values in the table are obtained when f_{XX} = 12 MHz and C_L = 100 pF.

DATA MEMORY LOW-VOLTAGE DATA RETENTION CHARACTERISTICS

(T_A = −10 to +70 °C, AV_{SS} = V_{SS} = AV_{REF} = 0 V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Data retention voltage	V_{DDDR}	STOP mode[Note 1]		2.0		5.5	V
Data retention current [Note 2, Note 3]	I_{DD3}	STOP mode V_{DDDR} = 5.5 V	When the subclock operates		15.0	70.0	μA
			When the subclock does not operate		0.5	40.0	μA
		STOP mode V_{DDDR} = 3.0 V	When the subclock operates		3.0	14.0	μA
			When the subclock does not operate		0.3	8.0	μA
		STOP mode V_{DDDR} = 2.0 V	When the subclock operates		1.5	9.0	μA
			When the subclock does not operate		0.2	6.0	μA
Data retention current (T_A = 25 °C) [Note 2, Note 3]	I_{DD3}	STOP mode V_{DDDR} = 5.5 V	When the subclock operates		15.0	40.0	μA
			When the subclock does not operate		0.5	10.0	μA
		STOP mode V_{DDDR} = 3.0 V	When the subclock operates		3.0	10.0	μA
			When the subclock does not operate		0.3	5.0	μA
		STOP mode V_{DDDR} = 2.0 V	When the subclock operates		1.5	7.0	μA
			When the subclock does not operate		0.2	4.0	μA
V_{DD} rising time	t_{RVD}			200			μs
V_{DD} falling time	t_{FVD}			200			μs
V_{DD} retention time (referred to STOP mode setting)	t_{HVD}			0			ms
STOP release signal input time	t_{DREL}			0			ms
Low-level input voltage	V_{IL}	Specified pins[Note 4]		0		0.1V_{DDDR}	V
High-level input voltage	V_{IH}			0.9V_{DDDR}		V_{DDDR}	V

Notes 1. The voltage to keep the subclock operating is lower than the data retention voltage.

2. Current through the AV_{REF} pin is excluded.

3. When using the XT1/P86 pin for input, disconnect the feedback resistor and clock noise eliminator.

4. Pins NMI, $\overline{\text{RESET}}$, P21/INTP0, P22/INTP1, P23/INTP2, P24/CTI10, P25/CTI00, P26/CTI11, P27/CLR1, P34/CLR0, P35/SI0, P36/SO0/SB0, P37/$\overline{\text{SCK0}}$, P93/$\overline{\text{SCK1}}$, P95/SI1, MODE, and P86/XT1 (when the subclock is not operating)

CLOCK FUNCTION (T_A = −10 to +70 °C, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Voltage to keep the subclock operating	V_{DDXT}		2.0			V
Operating voltage for hardware clock function	V_{DDW}		2.0			V

FLAG FOR DETECTING A BREAK OF SUBCLOCK OPERATION

(T_A = −10 to +70 °C, V_{DD} = AV_{DD} = 5.0 V ±10 %, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Time duration detected as a break of oscillating	T_{OSCF}		45			μs

A/D CONVERTER CHARACTERISTICS

(T_A = −10 to +70 °C, V_{DD} = AV_{DD} = 5.0 V ±10 %, 3.8 V ≤ AV_{REF} ≤ V_{DD}, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution			8			bit
Total error		4.0 V ≤ AV_{REF} ≤ V_{DD}			0.4	%
		3.8 V ≤ AV_{REF} ≤ V_{DD}			0.8	%
Quantization error					±1/2	LSB
Conversion time	t_{CONV}	ADM0 bit 4 = 0 [Note]	360t_{CYX}			ns
		ADM0 bit 4 = 1 [Note]	240t_{CYX}			ns
Sampling time	t_{SAMP}	ADM0 bit 4 = 0 [Note]	72t_{CYX}			ns
		ADM0 bit 4 = 1 [Note]	48t_{CYX}			ns
Analog input voltage	V_{IAN}		−0.3		AV_{REF} + 0.3	V
Reference voltage	AV_{REF}		3.8		V_{DD}	V
AV_{REF} current	AI_{REF}			0.2	1.0	mA

Note The time specified by ADM0 is used even for conversion with ADM1.

CHARACTERISTICS OF THE OPERATIONAL AMPLIFIERS

(T_A = −10 to +70 °C, V_{DD} = AV_{DD} = 5.0 V ±10 %, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Open-loop gain	Av		60			dB
Voltage range for common-mode input	V_{ICM}		0.5		3.3	V
Input offset voltage	V_{OS}			±10	±20	mV
High-level output current	I_{OHOP}	V_{DD} = 5.0 V, V_{OH} = V_{DD}/2	−4.0	−12.0		mA
Low-level output current	I_{OLOP}	V_{DD} = 5.0 V, V_{OL} = V_{DD}/2	50	130		μA
Slew rate	+			1		V/μs
	−			−4		V/ms
Common-mode rejection ratio	CMRR		60			dB
Supply-voltage rejection ratio	PSRR		60			dB
Unity-gain frequency	fo		1			MHz

Caution For stable operation, do not decrease the operational amplifier gain below 20 dB.

RECCTL WRITE CIRCUIT (T_A = −10 to +70 °C, V_{DD} = AV_{DD} = 5.0 V ±10 %, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CTLDLY charge current	I_{OHCTL}	V_{DD} = 5.0 V V_{OH} = 0 V	−500	−900	−1300	μA
CTLDLY discharge current	I_{OLCTL}	V_{DD} = 5.0 V V_{OL} = 5.0 V	1300	2200	3200	μA
PTO10, PTO11 high-level output current	I_{OHPTO}	V_{DD} = 5.0 V V_{OH} = 0 V	−6	−12	−22	mA

Caution When a 1-μF capacitor is connected, the time constant for PTO10 or PTO11 is 2 to 5 ms.

DC PROGRAMMING CHARACTERISTICS (T_A = +25 ±5 °C, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Symbol Note	Conditions	Min.	Typ.	Max.	Unit
High-level input voltage	V_{IH}	V_{IH}		2.4		V_{DDP}+0.3	V
Low-level input voltage	V_{IL}	V_{IL}		–0.3		0.8	V
Input leakage current	I_{LIP}	I_{LI}	0 ≤ V_I ≤ V_{DDP}			10	μA
High-level output voltage	V_{OH1}	V_{OH1}	I_{OH} = –400 μA	2.4			V
	V_{OH2}	V_{OH2}	I_{OH} = –100 μA	V_{DDP}-0.7			V
Low-level output voltage	V_{OL}	V_{OL}	I_{OL} = 2.1 mA			0.45	V
Output leakage current	I_{LO}		0 ≤ V_I ≤ V_{DDP}, $\overline{OE}$ = V_{IH}			10	μA
V_{DD} supply voltage	V_{DDP}	V_{DD}	Program memory write mode	5.75	6.0	6.25	V
			Program memory read mode	4.50	5.0	5.50	V
V_{PP} supply voltage	V_{PP}	V_{PP}	Program memory write mode	12.2	12.5	12.8	V
			Program memory read mode	V_{PP} = V_{DDP}			V
V_{DD} supply current	I_{DD}	I_{DD}	Program memory write mode		20	30	mA
			Program memory read mode $\overline{CE}$ = V_{IL}, V_I = V_{IH}		20	30	mA
V_{PP} supply current	I_{PP}	I_{PP}	Program memory write mode $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		5	30	mA
			Program memory read mode		1	100	μA

Note Symbols for the corresponding μPD27C256A

AC PROGRAMMING CHARACTERISTICS

(T_A = +25 ±5 °C, V_{DD} = AV_{DD} = 6 ±0.25 V, V_{PP} = 12.5 ±0.3 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Symbol Note	Conditions	Min.	Typ.	Max.	Unit
Address set up time to $\overline{CE}\downarrow$	t_{SAC}	t_{AS}		2			μs
$\overline{OE}\downarrow$ delay time from data	t_{DDOO}	t_{OES}		2			μs
Input data setup time to $\overline{CE}\downarrow$	t_{SIDC}	t_{DS}		2			μs
Address hold time to $\overline{CE}\uparrow$	t_{HCA}	t_{AH}		2			μs
Input data hold time to $\overline{CE}\uparrow$	t_{HCID}	t_{DH}		2			μs
Output data hold time to $\overline{OE}\uparrow$	t_{HOOD}	t_{DF}		0		130	ns
V_{PP} setup time to $\overline{CE}\downarrow$	t_{SVPC}	t_{VPS}		1			ms
V_{DD} setup time to $\overline{CE}\downarrow$	t_{SVDC}	t_{VDS}		1			ms
Initial program pulse width	t_{WL1}	t_{PW}		0.95	1.00	1.05	ms
Additional program pulse width	t_{WL2}	t_{OPW}		2.85		78.75	ms
$\overline{OE}\downarrow\rightarrow$ data output time	t_{DOOD}	t_{CE}				150	ns

Note Symbols for corresponding μPD27C256A

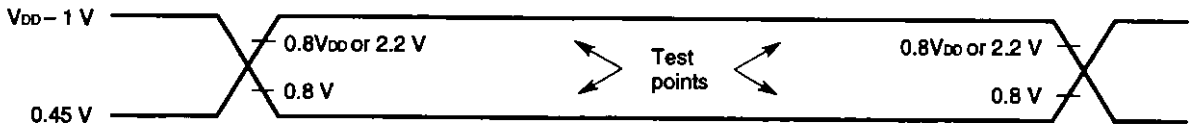
READ OPERATION (T_A = +25 ±5 °C, V_{DD} = AV_{DD} = V_{PP} = 5 ±0.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Symbol Note 1	Conditions	Min.	Typ.	Max.	Unit
Data output time from address	t_{DAOD}	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			200	ns
$\overline{CE}\downarrow\rightarrow$ data output time	t_{DCOD}	t_{CE}	$\overline{OE}$ = V_{IL}			200	ns
$\overline{OE}\downarrow\rightarrow$ data output time	t_{DOOD}	t_{OE}	$\overline{CE}$ = V_{IL}			75	ns
Data hold time to $\overline{OE}\uparrow$ or $\overline{CE}\uparrow$ Note 2	t_{HCOD}	t_{DF}	$\overline{CE}$ = V_{IL} or $\overline{OE}$ = V_{IL}	0		60	ns
Data hold time to address	t_{HAOD}	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0			ns

Notes 1. Symbols for the corresponding μPD27C256A

2. t_{HCOD} is the time measured from when either $\overline{OE}$ or $\overline{CE}$ reaches V_{IH}, whichever is faster.

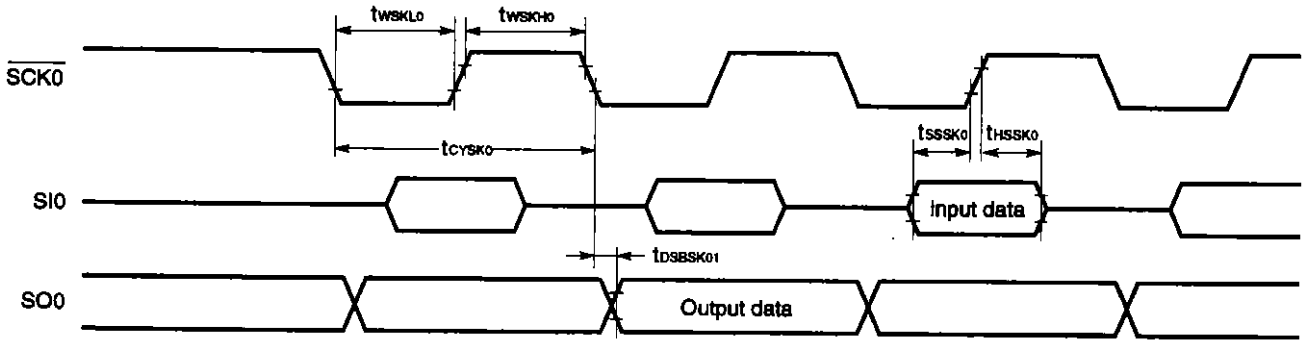
AC Timing Test Points



TIMING WAVEFORM

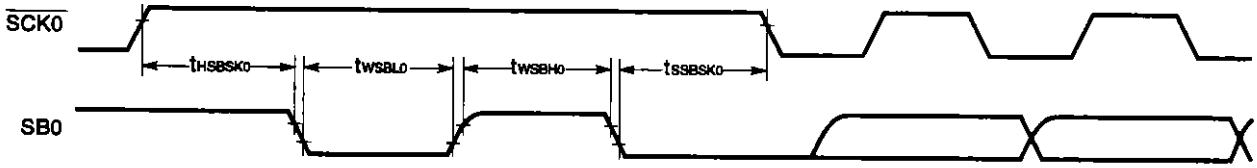
Serial Operation (SIO0)

Three-wire serial I/O mode

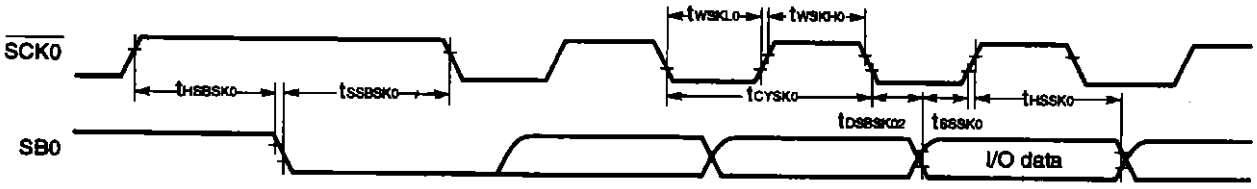


SBI Mode

Bus release signal transfer

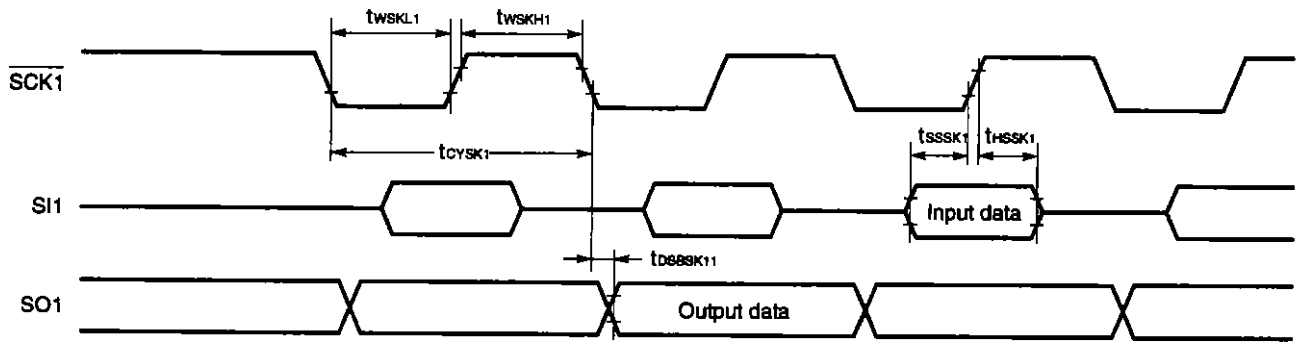


Command signal transfer



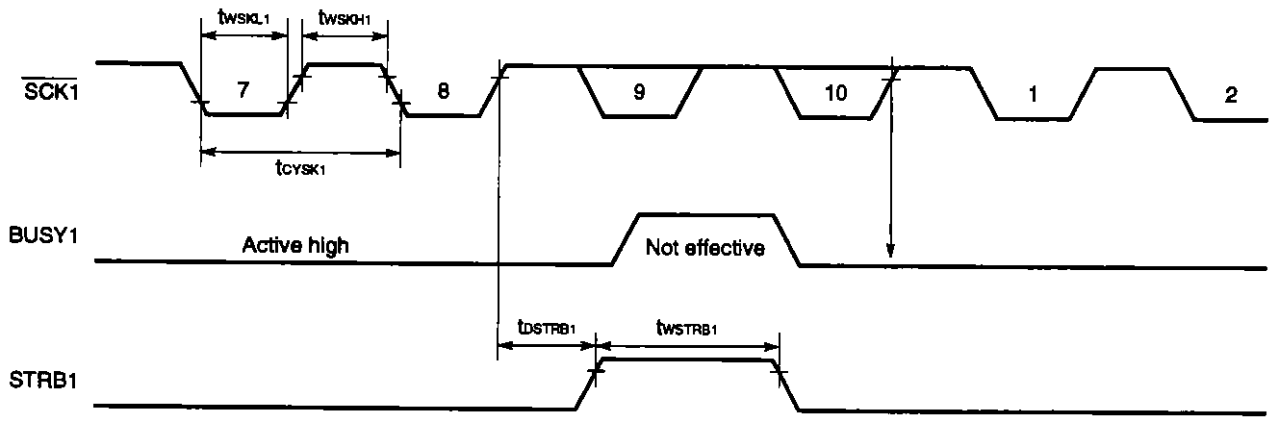
Serial Operation (SIO1)

Three-wire serial I/O mode

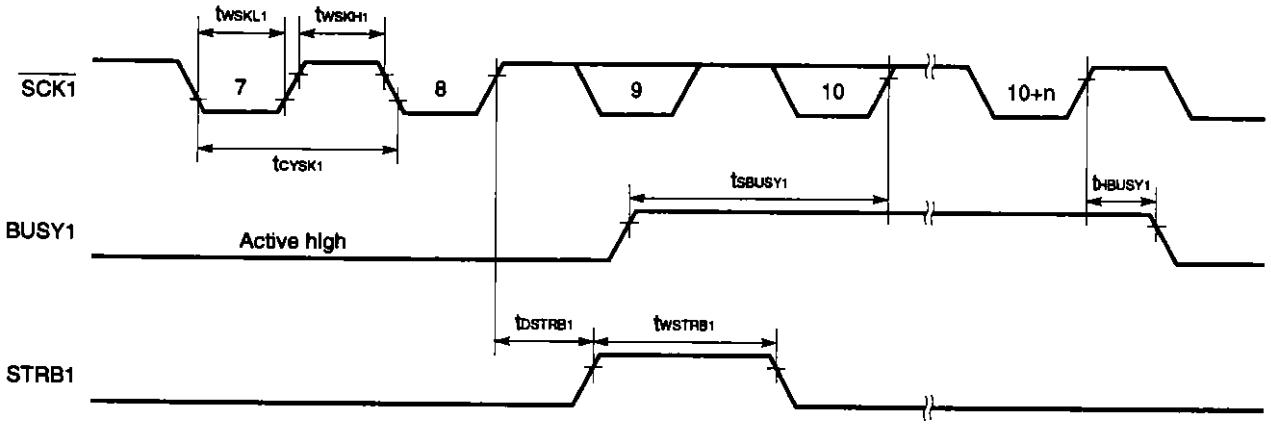


Automatic Transfer Mode (Internal Clock)

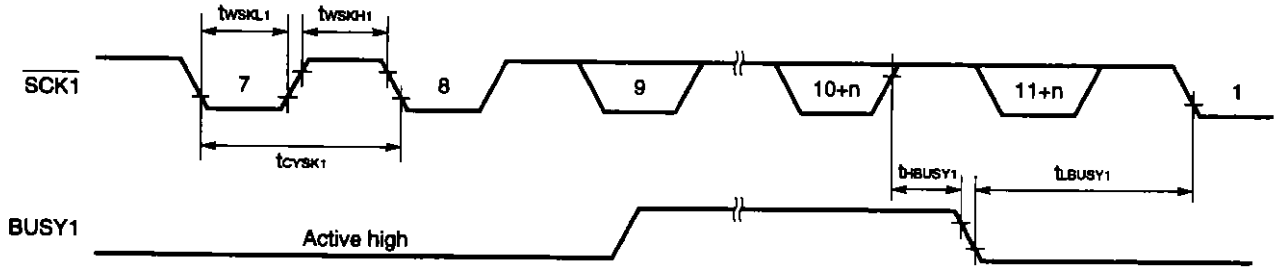
Without busy-state processing



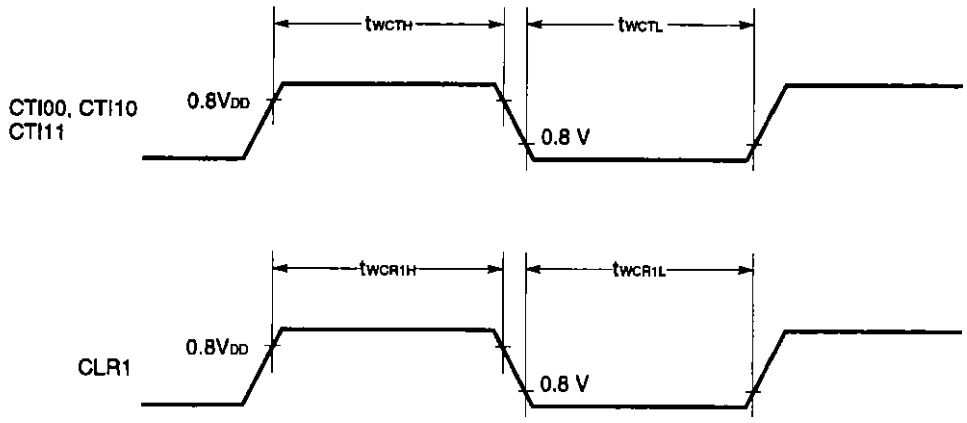
When the busy-state processing continues



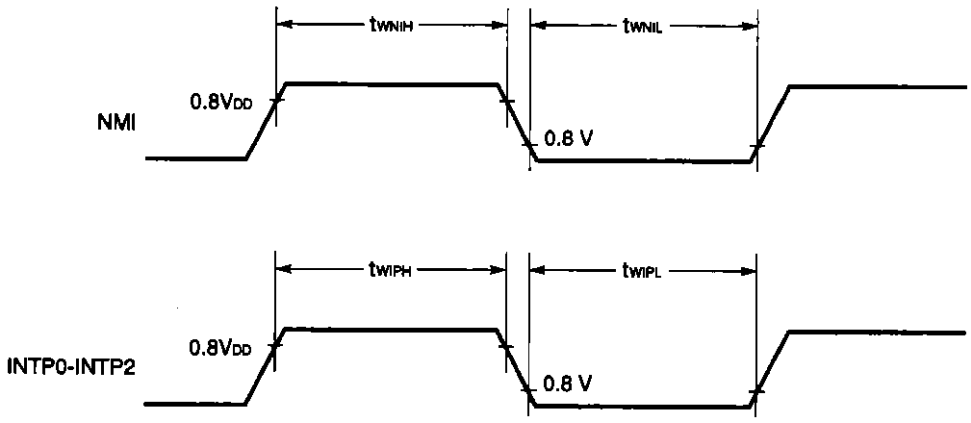
When the busy-state processing ends



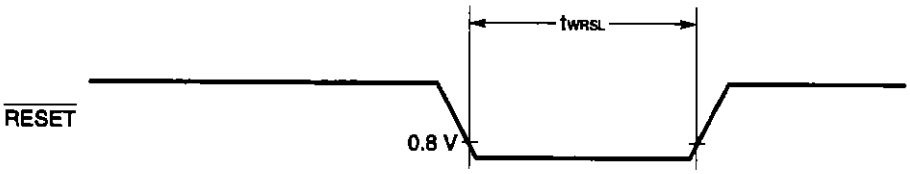
Super Timer Unit Input Timing



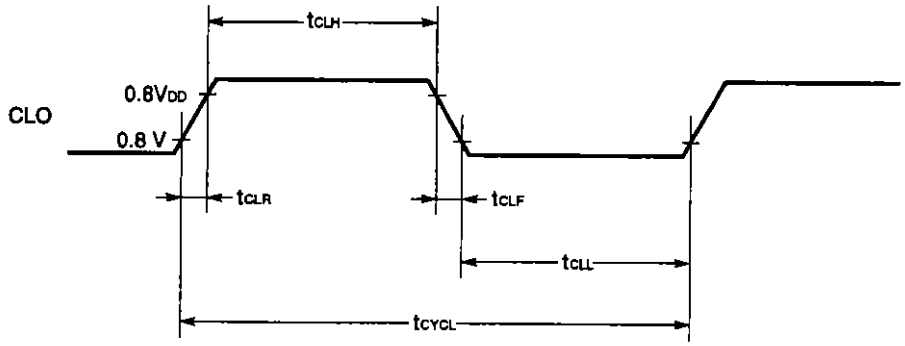
Interrupt Input Timing



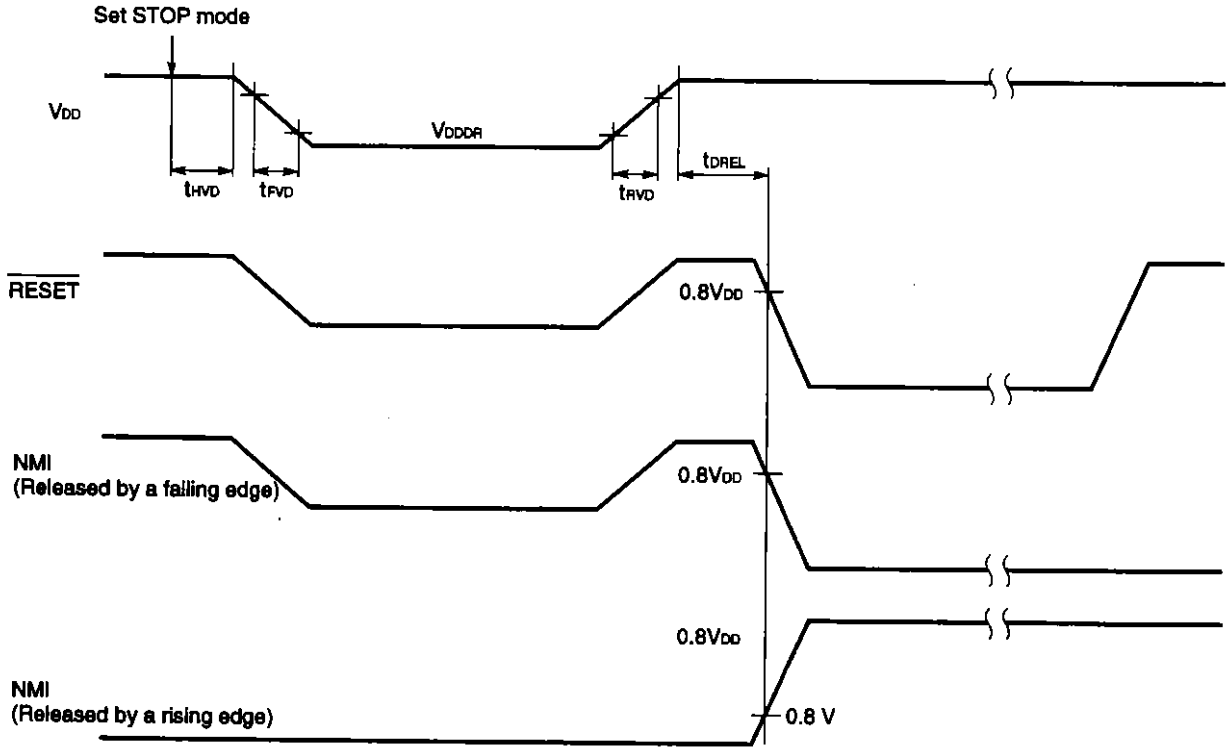
Reset Input Timing



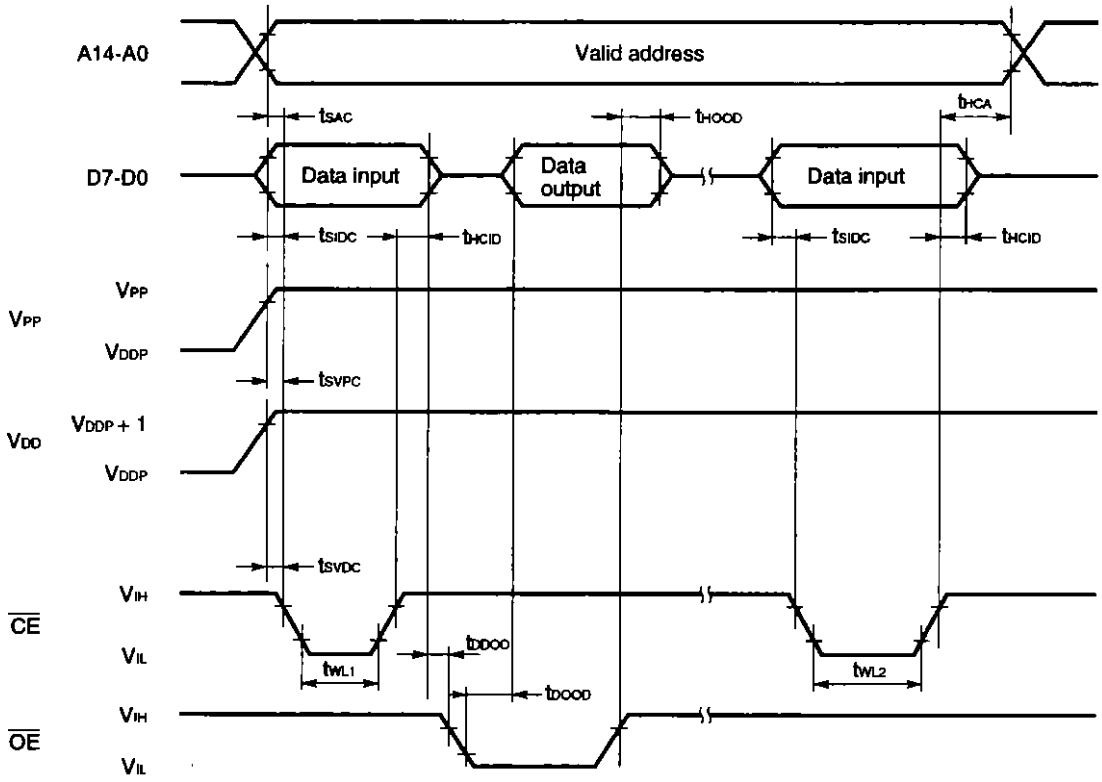
Clock Output Timing



Data Retention Timing



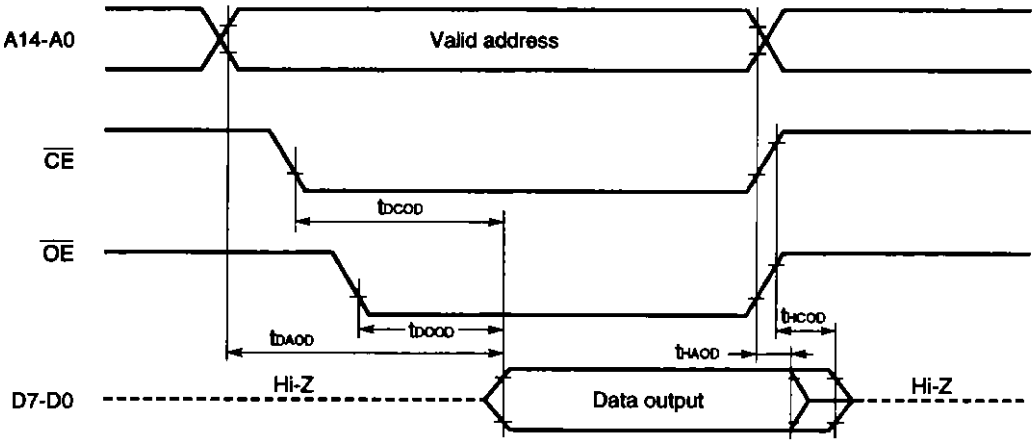
One-Time PROM Write Mode Timing



Cautions 1. V_{DD} must be applied before V_{PP}, and must be cut after V_{PP}.

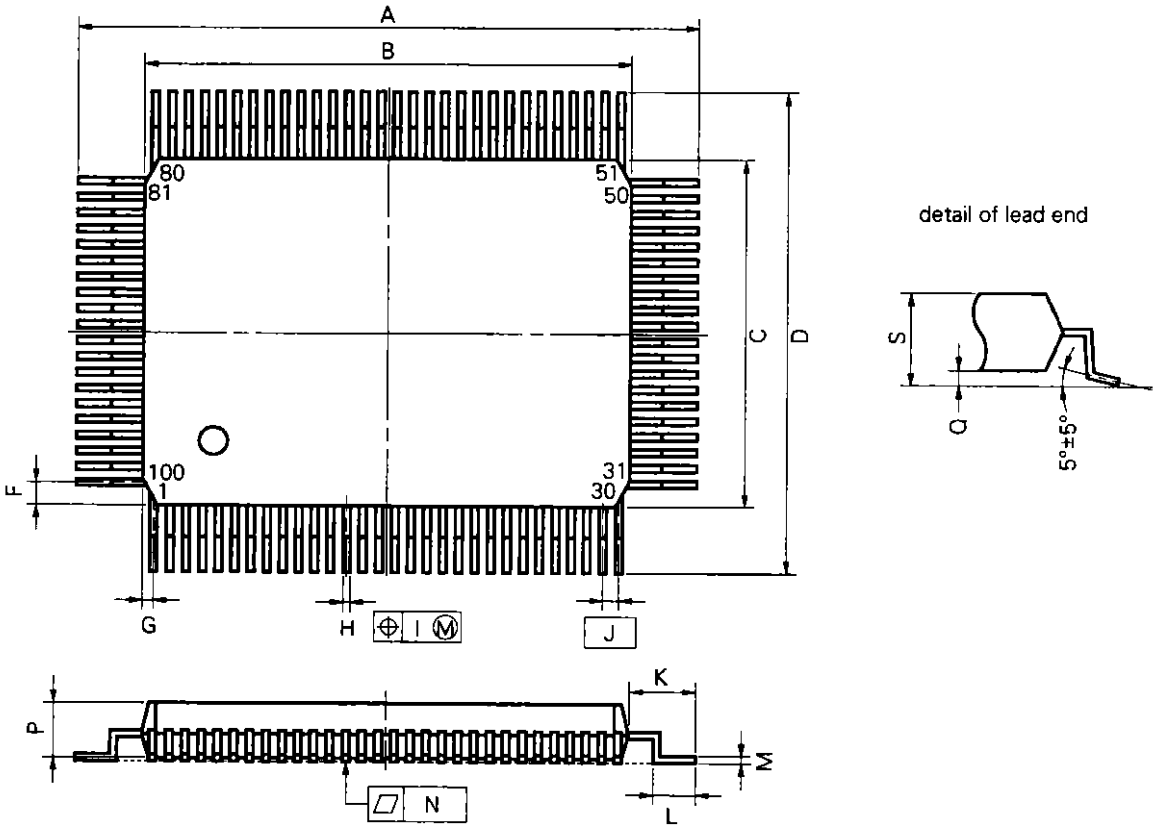
2. V_{PP} including overshoot must not exceed +13 V.

One-Time PROM Read Mode Timing



7. PACKAGE DRAWING

100 PIN PLASTIC QFP (14×20)



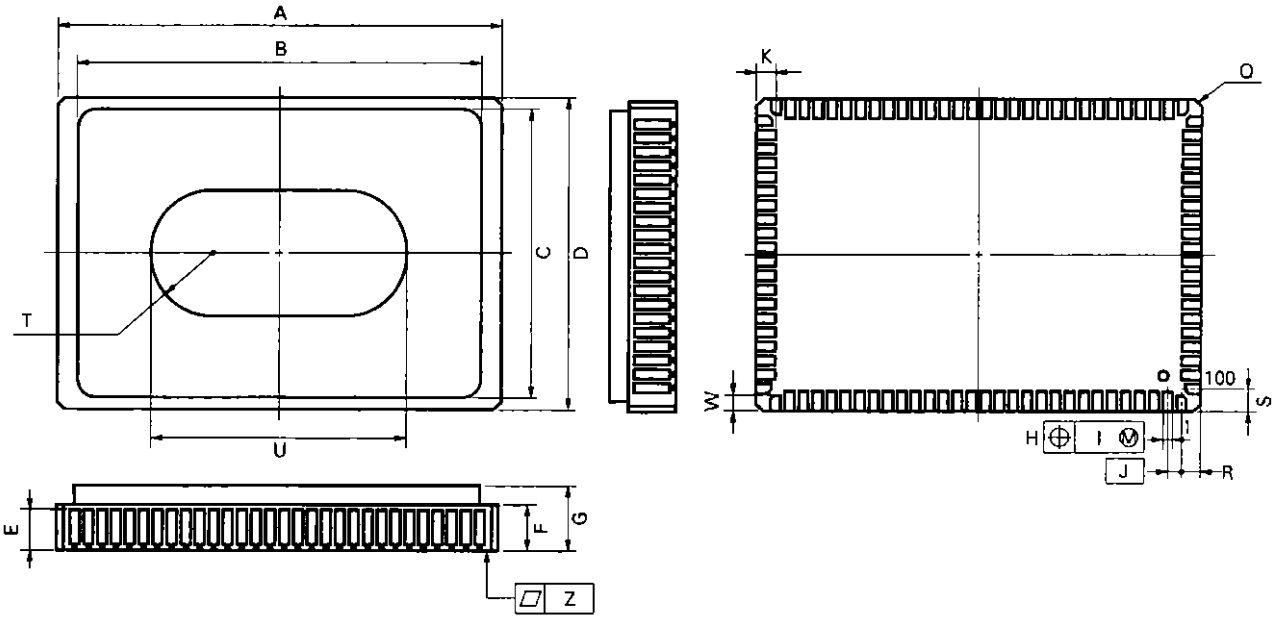
P100GF-65-3BA1-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

100 PIN CERAMIC WQFN



NOTE

Each lead centerline is located within 0.06 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

X100KW-65A-1

ITEM	MILLIMETERS	INCHES
A	20.6±0.4	0.811±0.016
B	19.0	0.748
C	13.8	0.543
D	14.6±0.4	0.575±0.016
E	1.94	0.076
F	2.14	0.084
G	3.5 MAX.	0.138 MAX.
H	0.45±0.10	$0.018^{+0.004}_{-0.005}$
I	0.06	0.003
J	0.65	0.026
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
Q	C 0.3	C 0.012
R	0.875	0.034
S	1.125	0.044
T	R 3.17	R 0.125
U	12.0	0.472
W	0.75±0.2	$0.030^{+0.008}_{-0.009}$
Z	0.10	0.004

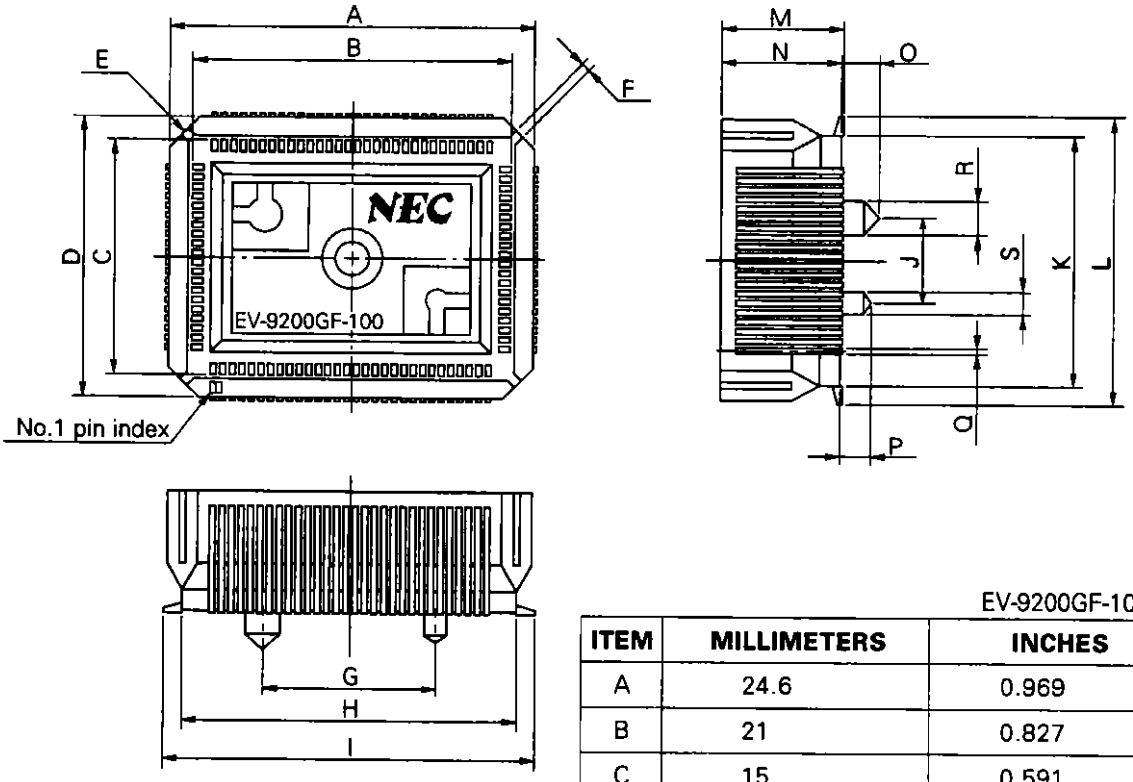
PACKAGE DRAWING AND PAD DRAWING OF THE EV-9200GF-100

The μPD78146GF can be mounted on the board using the conversion socket EV-9200GF-100, which has the same pin configuration as a QFP chip.

The package dimensions and pad pattern of the EV-9200GF-100 are shown below.

Based on EV-9200GF-100

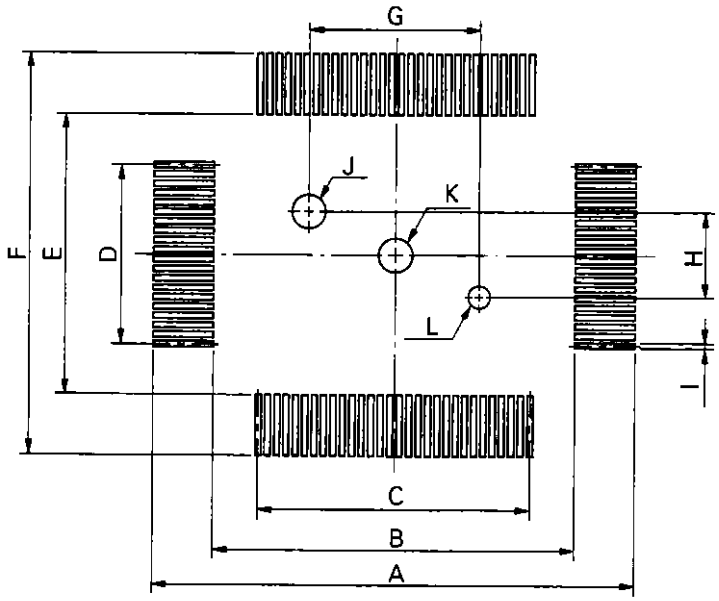
(1) Package drawing (in mm)



EV-9200GF-100-G0

ITEM	MILLIMETERS	INCHES
A	24.6	0.969
B	21	0.827
C	15	0.591
D	18.6	0.732
E	4-C 2	4-C 0.079
F	0.8	0.031
G	12.0	0.472
H	22.6	0.89
I	25.3	0.996
J	6.0	0.236
K	16.6	0.654
L	19.3	076
M	8.2	0.323
N	8.0	0.315
O	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	φ2.3	φ0.091
S	φ1.5	φ0.059

Based on EV-9200GF-100
(2) Pad drawing (in mm)



EV-9200GF-100-P0

ITEM	MILLIMETERS	INCHES
A	26.3	1.035
B	21.6	0.85
C	0.65±0.02 × 29=18.85±0.05	$0.026^{+0.001}_{-0.002} \times 1.142 = 0.742^{+0.002}_{-0.002}$
D	0.65±0.02 × 19=12.35±0.05	$0.026^{+0.001}_{-0.002} \times 0.748 = 0.486^{+0.003}_{-0.002}$
E	15.6	0.614
F	20.3	0.799
G	12±0.05	$0.472^{+0.003}_{-0.002}$
H	6±0.05	$0.236^{+0.003}_{-0.002}$
I	0.35±0.02	$0.014^{+0.001}_{-0.001}$
J	φ2.36±0.03	$\phi 0.093^{+0.001}_{-0.002}$
K	φ2.3	φ0.091
L	φ1.57±0.03	$\phi 0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

8. RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

For the details of the recommended soldering conditions refer to our document *SMD Surface Mount Technology Manual* (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 8-1 Soldering Conditions for Surface-Mount Devices

μPD78P148GF-3BA: 100-pin plastic QFP (14 mm × 20 mm excluding the dimensions of the pins)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C Reflow time: 30 seconds or less (at 210 °C or higher) Number of reflow processes: 1 Exposure limit: 7 days[Note] (20 hours of pre-baking is required at 125 °C afterward.)	IR35-207-1
VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (at 200 °C or higher) Number of reflow processes: 1 Exposure limit: 7 days[Note] (20 hours of pre-baking is required at 125 °C afterward.)	VP15-207-1
Partial heating method	Terminal temperature: 300 °C or below Flow time: 3 seconds or less (one side per device)	–

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: Temperature of 25 °C and maximum relative humidity at 65 % or less

Caution Do not apply more than a single process at once, except for "Partial heating method."

APPENDIX A DIFFERENCES BETWEEN μPD78P148 AND RELATED PRODUCTS (μPD78146, μPD78148, AND μPD78138)

Function		μPD78146	μPD78148	μPD78P148	μPD78138
Minimum instruction execution time		0.33 μs (at 12 MHz)			
ROM type		Mask ROM		PROM	Mask ROM
ROM capacity		24K bytes	32K bytes		
RAM capacity		688 bytes[Note 1]	816 bytes[Note 1]		640 bytes
I/O	Port	76[Note 2]			58
	A/D	15			8
	Others	6 (for operational amplifier I/O)			0
Real-time output port		18 (Output trigger timer can be selected.)			8 (Output trigger timer only is set.)
Super timer unit	Timer	• 16 bits × 3 • 8 bits × 3			• 16 bits × 3 • 7 bits × 1
	Counter	• 22-bit free running counter × 1 • 6-bit up/down counter × 1			• 18-bit free running counter × 1
	Capture register	• 22 bits × 2 • 16 bits × 3 • 8 bits × 2			• 18 bits × 1 • 16 bits × 4 • 7 bits × 1
	Compare register	• 16 bits × 7 • 8 bits × 3			• 16 bits × 6 • 7 bits × 1
	PWM output	• 12 bits × 2 channels (carrier frequency: 46.9 kHz/23.4 kHz) • 14 bits × 1 channel (carrier frequency 5.9 kHz) • 8 bits × 3 channels (carrier frequency: 5.9 kHz)			• 12 bits × 2 channels (carrier frequency: 46.9 kHz/23.4 kHz)
Multiply instructions		• MULUW: 16 bits (absolute value) × 8 bits (absolute value) • MULSW: 16 bits (complement) × 8 bits (absolute value)			
Multiplier		16 bits (complement) × 16 bits (complement) Operation time: 2.67 μs			–
A/D converter		8-bit resolution × 15 channels (7 channels can also be used as ports.)			8-bit resolution × 8 channels
Serial interface		2 channels	• Channel 0: Either 3-wire SIO or SBI can be selected. • Channel 1: Only 3-wire SIO is set. 48-byte automatic data send/receive function is provided.	1 channel	Either 3-wire SIO or SBI can be selected.
Analog circuit		2 operational amplifiers are provided.			–
Interrupt	External	5			5
	Internal	20			12
Package		100-pin plastic QFP (0.65 mm pitch, 14 × 20 mm) 100-pin ceramic WQFN (14 × 20 mm) (μPD78P148 only)			80-pin plastic QFP (0.8 mm pitch, 14 × 20 mm)
$\overline{V_{SYNC}}$ separator		Removed pulse width: Either 12.7 μs or 20.7 μs can be selected.			Removed pulse width: Either 5.3 μs or 12.0 μs can be selected.
Remote controller signal reception circuit		8-bit timer 4 (TM4) is provided.			–
Clock function		The clock function of hardware is provided.			–

Notes 1. Total of dual-port RAM (256 bytes) and peripheral RAM.

2. 10 port pins are also used for analog input to the A/D converter or as analog pins for the operational amplifiers.

APPENDIX B DEVELOPMENT TOOLS

The following tools are provided for developing a system that employs the μPD78P148.

[Hardware]

IE-78140-R	In-circuit emulator applicable for the μPD78146, μPD78148, and μPD78P148. For debugging, connect the emulator to the host machine. The connection of the emulator to the host machine enables symbolic debugging and object file transfer between the emulator and the host machine, thus enhancing debugging efficiency. The emulator has two RS-232-C serial interfaces channels. It can be connected to PROM programmer PG-1500. It also has the Centronics interface so that an object file and symbol file can be downloaded at high speed.
EP-78140GF-R	Emulation probe for the μPD78146GF-xxx-3BA, μPD78148GF-xxx-3BA, and μPD78P148GF-3BA. A 100-pin conversion socket, EV-9200GF-100, is supplied with the emulation probe, enabling easy development of a system.
EV-9200GF-100	Conversion socket produced for the 100-pin plastic QFP (14 × 20 mm). This socket is mounted on the PC board of the user system. The socket is used together with the EP-78140GF-R.
EV-9900	Jig used for removing the μPD78P148K from the EV-9200GF-100
PG-1500	A PROM programmer. Programs can be written into PROMs in a stand-alone mode or by remote control from a host machine when this programmer is connected with the accessory board and optional programmer adapter. Products programmable with the PG-1500 are commonly used PROMs (256K-bit to 4M-bit) and single chip microcomputers containing PROM.
PA-78P148GF PA-78P148K	PROM programmer adapter for the μPD78P148. The adapter is used with the PG-1500.

[Software]

<table>
<tr><td rowspan="4">RA78K/I relocatable assembler</td><td colspan="4">This relocatable assembler can be used for all 78K/I series emulators. With its macro functions, it allows the user to improve program development efficiency. A structured-programming assembler is also provided, which enables explicit description of program control structures. This assembler greatly improves productivity in program production and maintenance.</td></tr>
<tr><td>Host machine</td><td>OS</td><td>Distribution media</td><td>Part number</td></tr>
<tr><td>PC-9800 series</td><td rowspan="2">MS-DOS™ Ver. 3.30 to Ver. 5.00A Note</td><td>3.5-inch 2HD</td><td>μS5A13RA78K1</td></tr>
<tr><td>IBM PC/AT™ or compatibles</td><td>See [OS for IBM PC].</td><td>5.25-inch 2HD</td><td>μS5A10RA78K1</td></tr>
<tr><td rowspan="4">IE-78140-R control program (IE controller)</td><td colspan="4">This control program allows the user to control the IE-78140-R from the host machine. Its automatic command execution function ensures more efficient debugging.</td></tr>
<tr><td>Host machine</td><td>OS</td><td>Distribution media</td><td>Part number</td></tr>
<tr><td>PC-9800 series</td><td rowspan="2">MS-DOS Ver. 3.30 to Ver. 5.00A Note</td><td>3.5-inch 2HD</td><td>μS5A13IE78140</td></tr>
<tr><td>IBM PC/AT or compatibles</td><td>See [OS for IBM PC].</td><td>5.25-inch 2HD</td><td>μS5A10IE78140</td></tr>
<tr><td rowspan="4">PG-1500 controller</td><td colspan="4">This program enables the host machine to control the PG-1500 under the serial interface and parallel interface.</td></tr>
<tr><td>Host machine</td><td>OS</td><td>Distribution media</td><td>Part number</td></tr>
<tr><td>PC-9800 series</td><td rowspan="2">MS-DOS Ver. 3.30 to Ver. 5.00A Note</td><td>3.5-inch 2HD</td><td>μS5A13PG1500</td></tr>
<tr><td>IBM PC/AT or compatibles</td><td>See [OS for IBM PC].</td><td>5.25-inch 2HD</td><td>μS5A10PG1500</td></tr>
<tr><td colspan="2"></td><td>3.5-inch 2HD</td><td>μS7B13PG1500</td></tr>
<tr><td colspan="2"></td><td>5.25-inch 2HC</td><td>μS7B10PG1500</td></tr>
</table>

★ μS7B10RA78K1

★ μS7B10IE78140

Note These software products cannot use the task swap function, which is available in MS-DOS Ver. 5.00 and Ver. 5.00A.

Remark The operation of software products that include the assembler and IE controller is guaranteed only under the OSs on the corresponding host machines described above.

★ **[OS for IBM PC]**

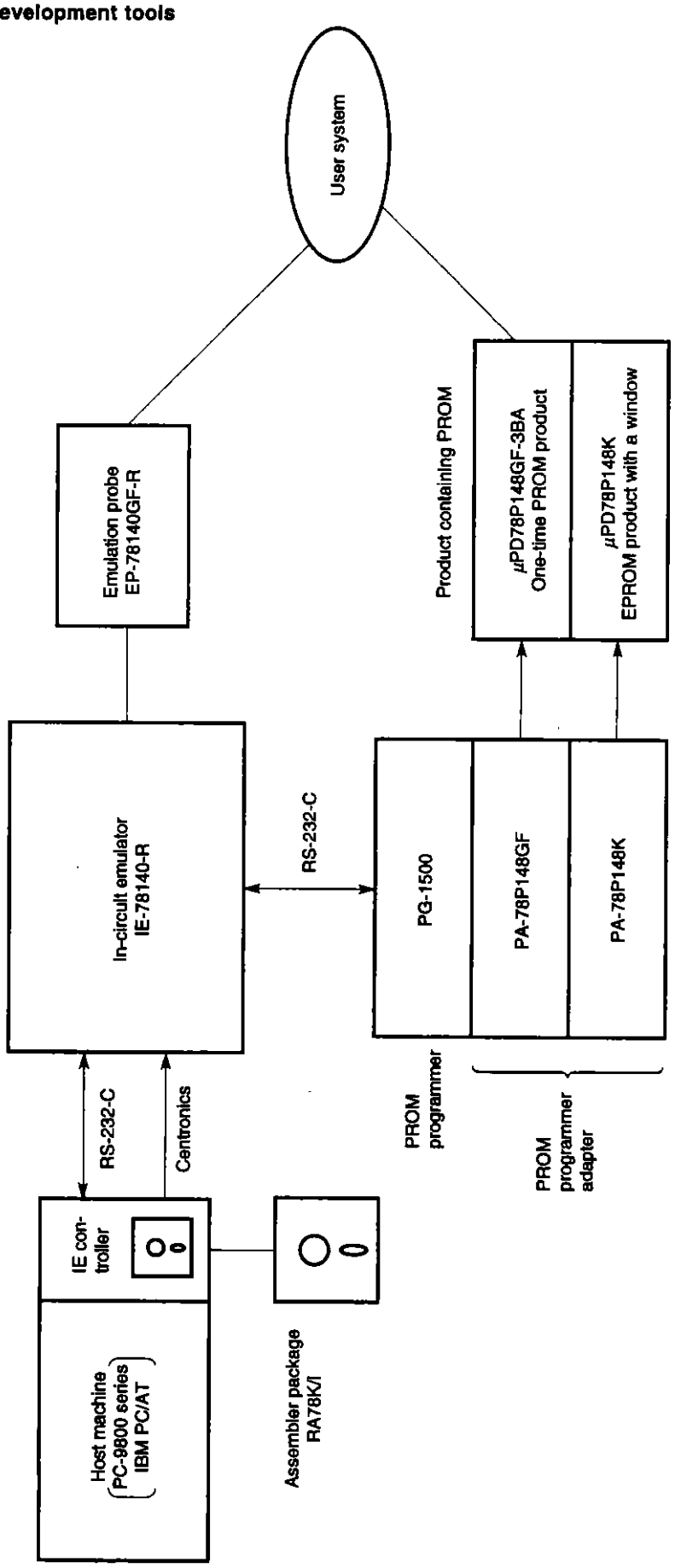
The following operating systems are supported for IBM PC.

OS	Version
PC DOS™	Ver. 3.1 to Ver. 6.3
	J6.1/V[Note] to J6.3/V[Note]
IBM DOS™	J5.02/V[Note]
MS-DOS	Ver. 5.0 to Ver. 6.2
	5.0/V[Note] to 6.2/V[Note]

Note Supports English mode only.

Caution These software products cannot use the task swap function, which is available in MS-DOS Ver. 5.00 and after.

Configuration of development tools



[MEMO]

Cautions on CMOS Devices

① **Countermeasures against static electricity for all MOSs**

Caution When handling MOS devices, take care so that they are not electrostatically charged.

Strong static electricity may cause dielectric breakdown in gates. When transporting or storing MOS devices, use conductive trays, magazine cases, shock absorbers, or metal cases that NEC uses for packaging and shipping. Be sure to ground MOS devices during assembling. Do not allow MOS devices to stand on plastic plates or do not touch pins.

Also handle boards on which MOS devices are mounted in the same way.

② **CMOS-specific handling of unused input pins**

Caution Hold CMOS devices at a fixed input level.

Unlike bipolar or NMOS devices, if a CMOS device is operated with no input, an intermediate-level input may be caused by noise. This allows current to flow in the CMOS device, resulting in a malfunction. Use a pull-up or pull-down resistor to hold a fixed input level. Since unused pins may function as output pins at unexpected times, each unused pin should be separately connected to the V_{DD} or GND pin through a resistor.

If handling of unused pins is documented, follow the instructions in the document.

③ **Statuses of all MOS devices at initialization**

Caution The initial status of a MOS device is unpredictable when power is turned on.

Since characteristics of a MOS device are determined by the amount of ions implanted in molecules, the initial status cannot be determined in the manufacture process. NEC has no responsibility for the output statuses of pins, input and output settings, and the contents of registers at power on. However, NEC assures operation after reset and items for mode setting if they are defined.

When you turn on a device having a reset function, be sure to reset the device first.

The export of this product from Japan is regulated by the Japanese government. To export this product may be prohibited without governmental license, the need for which must be judged by the customer. The export or re-export of this product from a country other than Japan may also be prohibited without a license from that country. Please call an NEC sales representative.

M4 94.11