NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT
μPD78P138

8 BIT SINGLE-CHIP MICROCOMPUTER

The μPD78P138 is produced by replacing the mask ROM of the μPD78138 with PROM. ★

There are two types of internal PROM: one-time PROM in which data can be written once, and EPROM to which programs can be re-written after previously written programs have been erased.

One-time PROM products are suited for system evaluation in development, manufacture of small quantities of multiple products, and early stage start-up of applications.

> The EPROM versions of the μPD78P138 are not intended for use in mass-produced products; they do not have reliability high enough for such purposes. Their use should be restricted to functional evaluation in experiment or trial manufacture.

The reader should also refer to the publications on the μPD78134A, μPD78136, and μPD78138.

FEATURES

- The pins are compatible with the μPD78134A, μPD78136, or μPD78138.
- Internal PROM: 32768 × 8 bits
- Size of the internal memory can be changed.
- PROM programming characteristics: compatible with the μPD27C256A

★

ORDERING INFORMATION

Part number	Package	Internal ROM	Quality grade
μPD78P138GF-3B9	80-pin plastic QFP	One-time PROM	Standard
μPD78P138K	80-pin LCC with a window	EPROM	Not applied

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

In this manual, the description of the PROM is for both a one-time PROM and EPROM.

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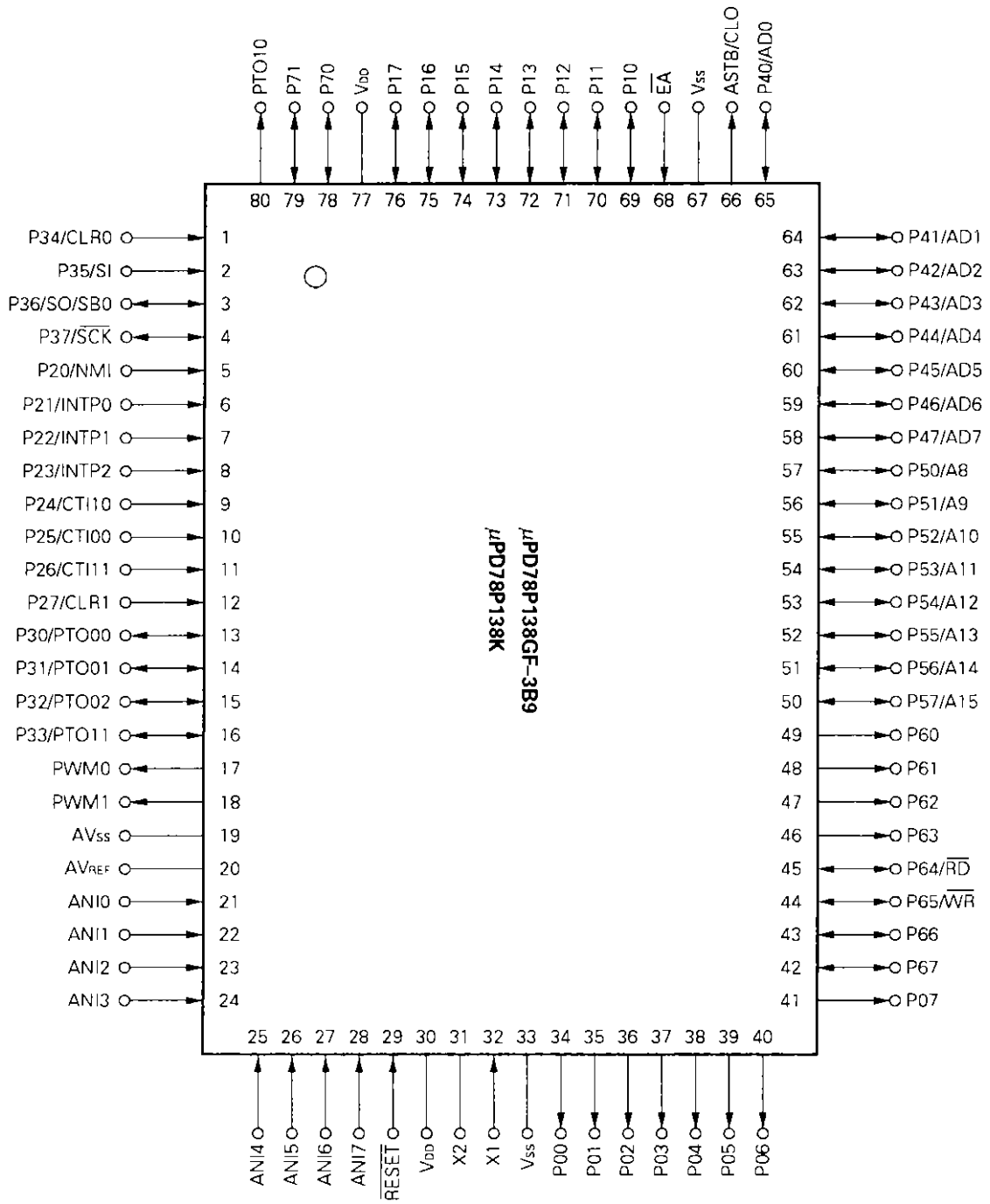
Date Published January 1993P
Printed in Japan

The mark ★ shows major revised point.

PIN CONFIGURATION (TOP VIEW)

80-pin plastic QFP

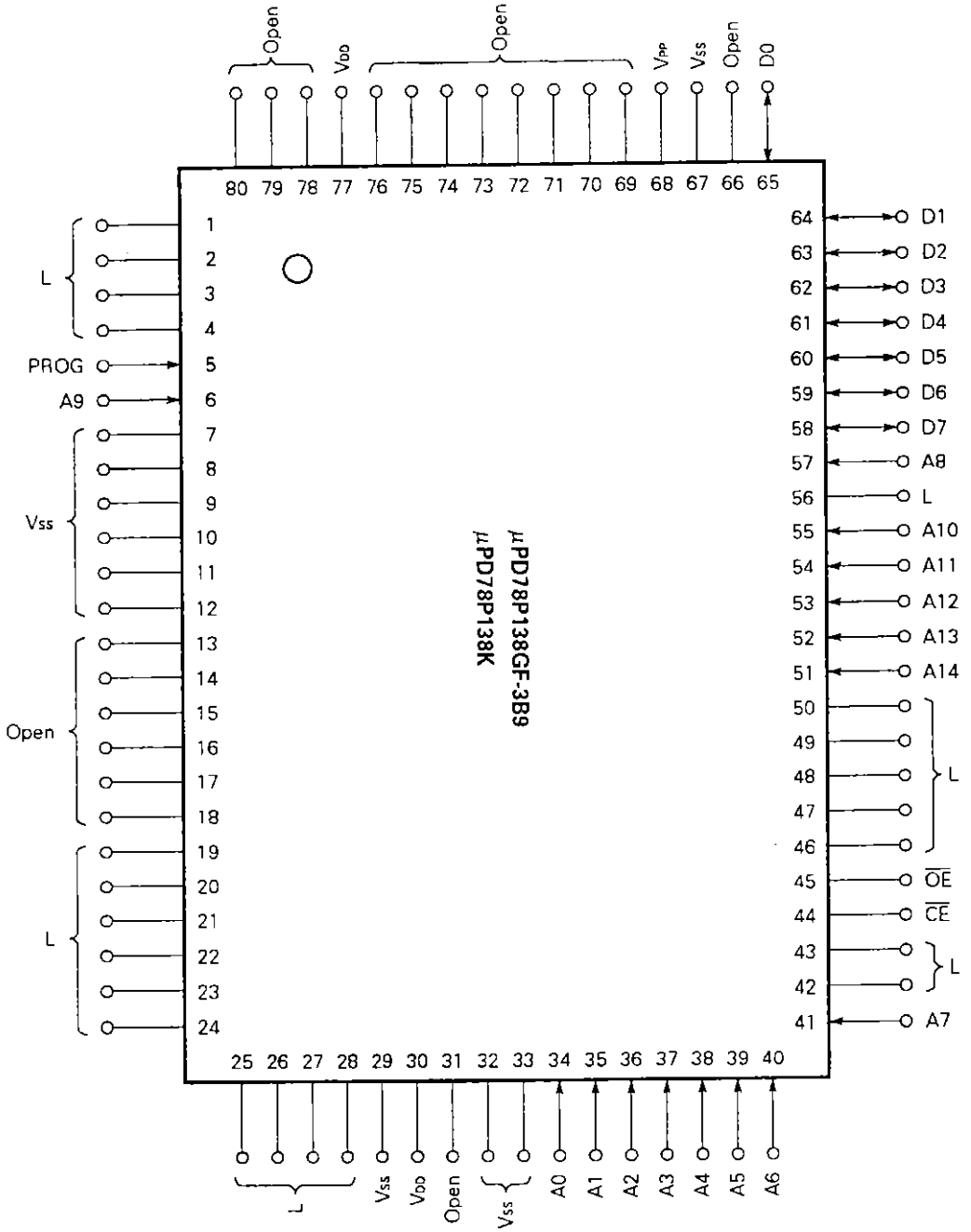
(1) Normal operation mode



P00-P07	:	Port 0
P10-P17	:	Port 1
P20-P27	:	Port 2
P30-P37	:	Port 3
P40-P47	:	Port 4
P50-P57	:	Port 5
P60-P67	:	Port 6
P70, P71	:	Port 7
PWM0, PWM1	:	Pulse width modulation output
CLO	:	Clock output
ANI0-ANI7	:	Analog input
AV_{REF}	:	Reference voltage
AV_{SS}	:	Analog Vss
X1, X2	:	Crystal
$\overline{RESET}$	:	Reset

CTI00, CTI10, CTI11	:	Capture trigger input
CLR0, CLR1	:	Timer clear input
PTO00-PTO02, PTO10, PTO11	:	Programmable timer input
NMI	:	Nonmaskable interrupt
INTP0-INTP2	:	Interrupt from peripherals
SI	:	Serial input
SO	:	Serial output
SB0	:	Serial bus
$\overline{SCK}$	:	Serial clock
AD0-AD7	:	Address data
A8-A15	:	Address
$\overline{RD}$	:	Read
$\overline{WR}$	:	Write
ASTB	:	Address strobe
$\overline{EA}$	:	External access

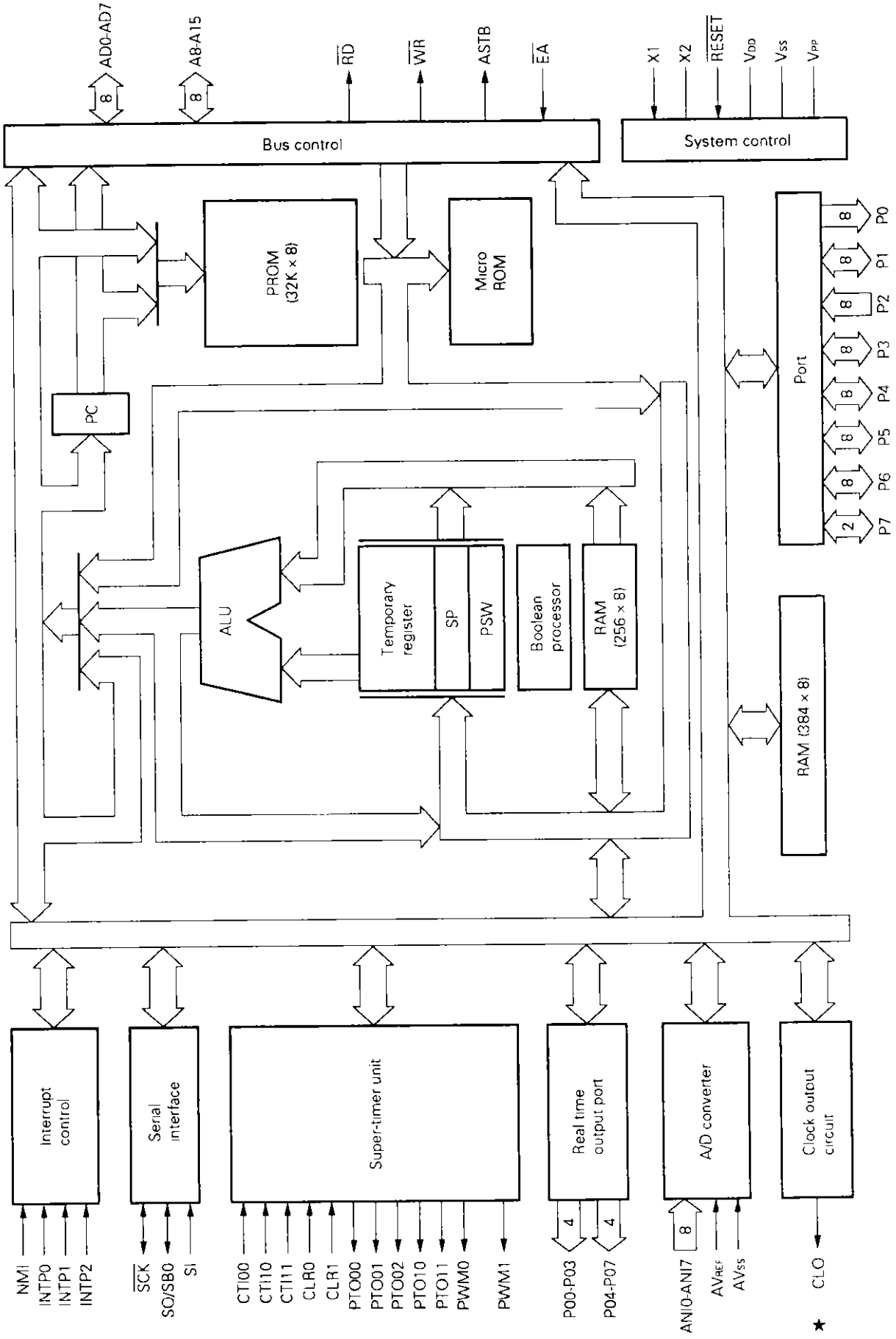
(2) PROM programming mode



A0-A14: Address
D0-D7 : Data
PROG : Program
$\overline{CE}$: Chip enable
$\overline{OE}$: Output enable

Cautions 1. L : Connect these pins separately to the Vss pins through pull-down resistors.
2. Vss : To be connected to the ground.
3. Open: Nothing should be connected on these pins.

BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

1.1 PORT PINS

Pin name	I/O	Dual-function pin( ) Note	Function
P00-P07	O	(A0-A7)	Port 0 (P0) : Can be specified to output or high impedance 8 bits by 8 bits. Also function as a real-time output port.
P10-P17	I/O	–	Port 1 (P1) : Can be specified to input or output bit by bit. Can directly drive LED. Software pull-up resistor (P10-P17) can be built in.
P20	I	NMI(PROG)	Port 2 (P2) : Also function as external interrupt pins or various trigger pins. Software pull-up resistor (P22-P27) can be built in.
P21		INTP0(A9)	
P22		INTP1	
P23		INTP2	
P24		CTI10	
P25		CTI00	
P26		CTI11	
P27		CLR1	
P30	I/O	PTO00	Port 3 (P3) : P30-P33, P36, P37: I/O port (Can be specified to input or output bit by bit.) P34, P35: Input port Also function as various control pins. Software pull-up resistor (P30-P37) can be built in.
P31		PTO01	
P32		PTO02	
P33		PTO11	
P34	I	CLR0	
P35		SI	
P36	I/O	SO/SB0	
P37		$\overline{SCK}$	
P40-P47	I/O	AD0-AD7 (D0-D7)	Port 4 (P4) : Can be specified to input or output 8 bits by 8 bits. Also function as address/data bus for when external memory is connected. Software pull-up resistor (P40-P47) can be built in.
P50	I/O	A8(A8)	Port 5 (P5) : Can be specified to input or output bit by bit. Also function as address output bus for when external memory is connected. Software pull-up resistor (P50-P57) can be built in.
P51		A9	
P52-P56		A10-A14 (A10-A14)	
P57		A15	

Note Pins in parentheses indicate the pins used in the PROM programming mode.

Pin name	I/O	Dual-function pin( ) Note	Function
P60-P63	O	–	Port 6 (P6) : Also function as control signal pin for when external memory is connected. Software pull-up resistor (P64-P67) can be built in.
P64	I/O	$\overline{RD}$($\overline{OE}$)	
P65		$\overline{WR}$($\overline{CE}$)	
P66-P67		–	
P70-P71	I/O	–	Port 7 (P7) : Can be specified to input or output 2 bits by 2 bits. Software pull-up resistor (P70, P71) can be built in.

Note Pins in parentheses indicate the pins used in the PROM programming mode.

1.2 NON-PORT PINS (IN NORMAL OPERATION MODE)

Pin name	I/O	Dual-function pin( ) Note	Function
PWM0, PWM1	O	–	Super timer unit PWM output
ANI0-ANI7	I	–	Analog voltage input to A/D converter
AV_{REF}		–	Reference voltage input to A/D converter
AVss		–	Ground potential of A/D converter
NMI	I	P20 (PROG)	Non-maskable interrupt request input. Either rising edge or falling edge can be selected via mode register (INTM0).
INTP0	I	P21 (A9)	External interrupt request input . Rising edge, falling edge, or rising and falling edges can be selected via mode register (INTM0).
INTP1	I	P22	External interrupt request input. Rising edge or rising and falling edges can be selected via mode register (INTM0)
INTP2		P23	
SI	I	P35	Serial data input (3-wire serial I/O mode)
SO	I/O	P36/SB0	Serial data output (3-wire serial I/O mode)
SB0	I/O	P36/SO	Serial data input (SBI mode)
$\overline{SCK}$	I/O	P37	Serial clock input/output
CTI00	I	P25	Super timer unit capture trigger input
CTI10		P24	
CTI11		P26	
CLR0	I	P34	Super timer unit timer clear signal input
CLR1		P27	
PTO00	I/O	P30	Super timer unit timer output
PTO01		P31	
PTO02		P32	
PTO10	O	–	
PTO11	I/O	P33	
AD0-AD7	I/O	P40-P47 (D0-D7)	Time multiplexing address/data bus for when external memory is connected
A8	I/O	P50(A8)	Address output port for when external memory is connected
A9		P51	
A10-A14		P52-P56 (A10-A14)	
A15		P57	
$\overline{RD}$	O	P64($\overline{OE}$)	Strobe signal output for reading external memory
$\overline{WR}$	O	P65($\overline{CE}$)	Strobe signal output for writing external memory
ASTB	O	CLO	Timing signal output that externally latches address data for accessing external memory

Note Pins in parentheses indicate the pins used in the PROM programming mode.

Pin name	I/O	Dual-function pin Note	Function
CLO	O	ASTB	Clock output
$\overline{EA}$	I	V_{PP}	External expansion function control input
X1	I	–	Crystal connection for system clock signal oscillation. Input the externally supplied clock signal to X1 and input its inverted phase to X2.
X2	–		
$\overline{RESET}$	I	–	System reset input. Contains an analog delay noise reduction circuit.
V_{DD}		–	Positive power supply
Vss		–	GND potential

Note Pins in parentheses indicate the pins used in the PROM programming mode.

1.3 NON-PORT PINS (PROM PROGRAMMING MODE)

Pin name	I/O	Dual-function pin	Function
A0-A7	I	P00-P07	Address input
A8		P50/A8	
A9		P21/INTP0	
A10-A14		P52-P56/A10-A14	
D0-D7	I/O	P40-P47/AD0-AD7	Data I/O
$\overline{CE}$	I	P65/$\overline{WR}$	Program pulse input
$\overline{OE}$	I	P64/$\overline{RD}$	Output enable input
PROG		P20/NMI	High-voltage application for writing or verifying a program
V_{PP}		$\overline{EA}$	High-voltage application for writing or verifying a program. Normally, functions as $\overline{EA}$ pin.
V_{DD}		–	Power supply
Vss		–	GND potential

1.4 INPUT/OUTPUT CIRCUITS AND CONNECTION OF UNUSED PINS

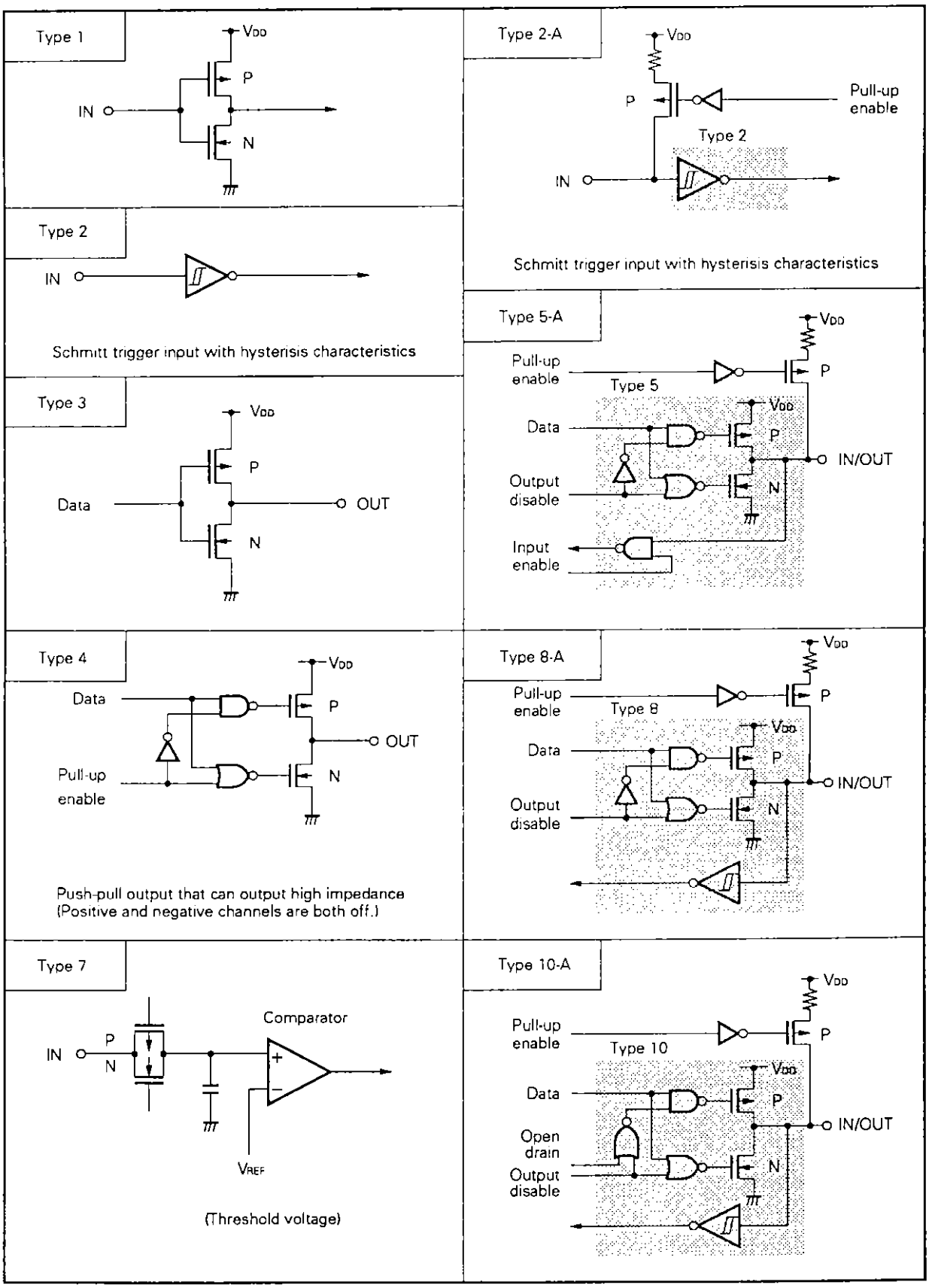
Table 1-1 and Fig. 1-1 show simplified pin input/output circuits. Table 1-1 also shows how unused pins are to be handled in normal operation mode. See **Section 3.2** for the connection of the pins unused in the PROM programming mode.

Table 1-1 I/O Circuit Type of Each Pin and Connection of Unused Pins in Normal Operation Mode

Pin name ( ) Note	I/O circuit type	Recommended connection of unused pins
P00-P07(A0-A7)	4	Open
P10-P17	5-A	Input : Connected to V_{DD} via pull-up resistor Output: Open
P20/NMI(PROG)	2	Connected to V_{DD}
P21/INTP0(A9)		
P22-P23/INTP1-INTP2	2-A	
P24/CTI10		
P25/CTI00		
P26/CTI11		
P27/CLR1		
P30-P32/PTO00-PTO02	5-A	Input : Connected to V_{DD} via pull-up resistor Output: Open
P33/PTO11		
P34/CLR0	2-A	Connected to V_{DD}
P35/SI		
P36/SO/SB0	10-A	Connected to V_{DD} via pull-up resistor
P37/$\overline{SCK}$	8-A	
P40-P47/AD0-AD7(D0-D7)	5-A	Input : Connected to V_{DD} via pull-up resistor Output: Open
P50/A8(A8)		
P51/A9		
P52-P56/A10-A14(A10-A14)		
P57/A15		
P60-P63	3	Open
P64/$\overline{RD}$($\overline{OE}$)	5-A	Input : Connected to V_{DD} via pull-up resistor Output: Open
P65/$\overline{WR}$($\overline{CE}$)		
P66, P67		
P70, P71		
PWM0, PWM1	3	Open
PTO10		
ANI0-ANI7	7	Connected to Vss
$\overline{EA}$/V_{PP}	1	—
ASTB/CLO	3	Open
$\overline{RESET}$	2	—
AV_{REF}	–	Connected to Vss
AVss		

Note Pins in parentheses indicate the pins used in the PROM programming mode.

Fig. 1-1 Pin Input/Output Circuits



2. DIFFERENCES BETWEEN PROM PRODUCTS AND MASK ROM PRODUCTS

2.1 DIFFERENCES BETWEEN THE μPD78P138 AND μPD78134A/μPD78136/μPD78138

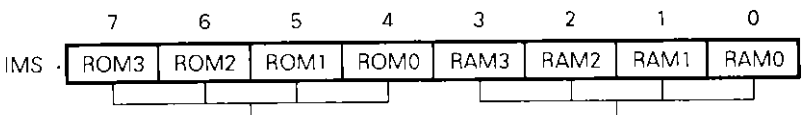
Table 2-1 shows the differences between these products.

For the details of the CPU function and built-in hardware, refer to the publications on the μPD78134A, μPD78136, and μPD78138.

Table 2-1 Differences between μPD78P138 and μPD78134A/μPD78136/μPD78138

Item	μPD78P138	μPD78134A	μPD78136	μPD78138
Program memory	• PROM • 32768 bytes	• Mask ROM • 16384 bytes	• Mask ROM • 24576 bytes	• Mask ROM • 32768 bytes
Internal memory size change register (IMS)	Provided (**Fig. 2-1** shows the format of IMS.)	Not provided		
Pin connection	In the μPD78P138, the functions to read/write the PROM are added to the pins.			

Fig. 2-1 Format of the Internal Memory Size Change Register (IMS)



RAM3	RAM2	RAM1	RAM0	Internal RAM size change
1	1	0	1	640 bytes
0	1	1	1	384 bytes

Caution No values other than above shall be set.

ROM3	ROM2	ROM1	ROM0	Internal ROM size change
1	1	1	1	32768 bytes
1	1	1	0	24576 bytes
0	1	0	1	16384 bytes

Caution No values other than above shall be set.

★ 2.2 DIFFERENCES BETWEEN THE μPD78138 SERIES AND μPD78134

The differences between the μPD78138 series (μPD78134A, μPD78136, μPD78138, and μPD78P138) and μPD78134 are as follows:

① ROM/RAM size

Item	μPD78134	μPD78134A	μPD78136	μPD78138	μPD78P138
ROM	16K bytes (Mask ROM)		24K bytes (Mask ROM)	32K bytes (Mask ROM)	32K bytes (PROM)
RAM	384 bytes		640 bytes		

② Added instructions

The following 15 instructions are added in the μPD78138 series.

Signed multiply instruction	: MULSW r
8-bit data transfer instruction	: MOV A, [HL+]
	MOV [HL+], A
	MOV A, [DE]
	MOV [DE], A
	MOV A, [DE+]
	MOV [DE+], A
	MOV A, !addr16
	MOV !addr16, A
	XCH A, [HL]
	XCH A, [DE]
	XCH A, word [r1]
8-bit arithmetic/logical instruction	: ALU A, [DE]
	ALU A, word [r1]
Call instruction	: CALL rp

Remark Legend

A	: Register A
rp	: AX, BC, DE, or HL
r	: A, X, B, C, D, E, H, or L
r1	: A or B
word	: 16-bit immediate data or label
!addr16	: 0000H-FFFFH immediate data or label
HL	: Register pair
DE	: Register pair
ALU	: Generic for all the mnemonics of the 8-bit arithmetic/logical instructions (ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP)

③ **Operation when a value is written in an event counter compare register (ECCO or ECC1)**

- μPD78134 : Clears the event counter (EC).
- μPD78138 series: Clears the event counter (EC) when 0xxxxxxxB is written. Does not clear event counter (EC) when 1xxxxxxxB is written.

④ **Threshold width for pulse elimination for the digital noise eliminator**

- μPD78134 : 40/f_{CLK}
- μPD78138 series: 32/f_{CLK} or 72/f_{CLK} selectable

⑤ **PWM carrier frequency**

- μPD78134 : 23.4 kHz
- μPD78138 series: 23.4 kHz or 46.9 kHz selectable

⑥ **Restrictions are lifted for the real-time output port control mode in macro service**

In the μPD78138 series, the restriction that the output timing data must be stored in ROM in the real-time output control mode in macro service in the μPD78134 is lifted.

3. PROM PROGRAMMING

The program memory in the μPD78P138 is an electrically writable PROM of 32768 × 8 bits. When programming this PROM, use the PROG and $\overline{\text{RESET}}$ pins to set the μPD78P138 to the PROM programming mode. Table 3-1 lists the pins to be used in this mode.

The μPD78P138 provides programming characteristics compatibility with the μPD27C256A.

Table 3-1 Pin Functions in PROM Programming Mode

Pin	Function
PROG	High-voltage input to set the μPD78P138 to the PROM programming mode
$\overline{\text{RESET}}$	Low level pulse input to set the μPD78P138 to the PROM programming mode
V_{PP}	PROM programming voltage input
A0-A14	Address input
D0-D7	Data input (when writing), data output (when verifying or reading)
$\overline{\text{CE}}$	Chip enable input
$\overline{\text{OE}}$	Output enable input
V_{DD}	Power supply input
V_{SS}	GND potential

3.1 PROM PROGRAMMING OPERATING MODE

When +6 V is applied to the V_{DD} pin and when +12.5 V is applied to the V_{PP} pin, the μPD78P138 enters the program write/verify mode. This mode varies to each operating mode shown in Table 3-2 according to how to set the $\overline{\text{CE}}$ and $\overline{\text{OE}}$ pins.

Setting the μPD78P138 to the read mode enables it to read the contents of PROM.

Table 3-2 Operating Modes for Programming on PROM

Mode \ Pin	PROG	$\overline{\text{RESET}}$	$\overline{\text{CE}}$	$\overline{\text{OE}}$	V_{PP}	V_{DD}	D0-D7
Program write	+12.5 V	L	L	H	+12.5 V	+6 V	Data input
Program verify			H	L			Data output
Program inhibit			H	H			High impedance
Read			L	L	+5 V	+5 V	Data output
Output disable			L	H			High impedance
Standby			H	L/H			High impedance

Caution Do not set both $\overline{\text{CE}}$ and $\overline{\text{OE}}$ to L when V_{PP} is set to +12.5 V and V_{DD} to +6 V.

3.2 CONNECTION OF UNUSED PINS IN THE PROM PROGRAMMING MODE

Table 3-3 lists the connections of the pins not to be used in the PROM programming mode.

Table 3-3 Connection of Unused Pins in the PROM Programming Mode

Pin	Recommended connection of unused pins
P10-P17	Open
P22-P27	Connected to Vss
P30-P33	Open
P34-P37	Connected to Vss via pull-down resistor
P51, P57	
P60-P63	
P66, P67	
P70, P71	Open
PWM0, PWM1	
ANI0-ANI7	Connected to Vss via pull-down resistor
AV_{REF}, AVss	
ASTB/CLO	Open
PTO10	
X1	Connected to Vss
X2	Open

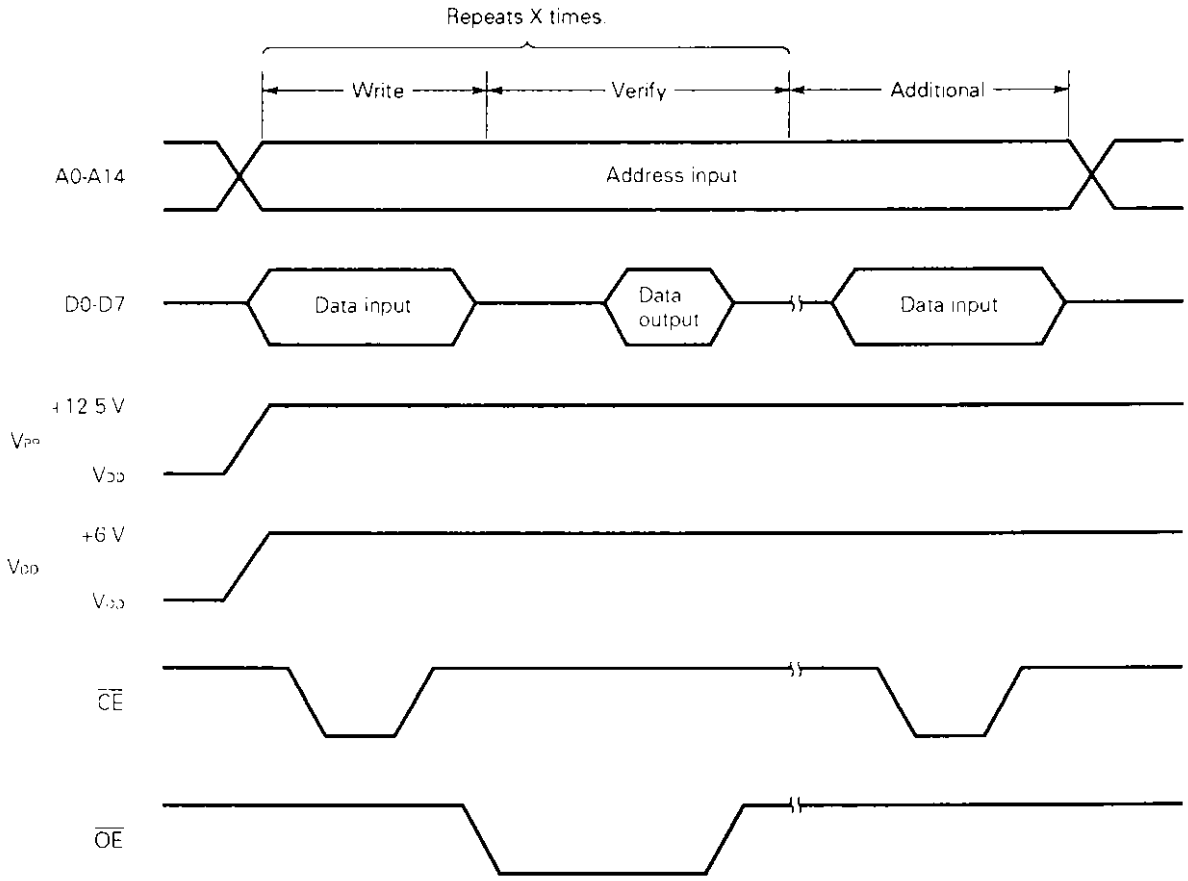
3.3 PROCEDURE FOR WRITING ON PROM

The following is a procedure for writing on PROM. Data can be written at high speed.

(1) Always set the $\overline{\text{RESET}}$ pin to low. Apply +12.5 V to the PROG pin. Handle other unused pins as shown in Table 3-3.
(2) Apply +6 V to the V_{DD} pin and +12.5 V to the V_{PP} pin.
(3) Set an initial address.
(4) Input write data.
(5) Input a 1 ms program pulse (active low) to the $\overline{\text{CE}}$ pin.
(6) Verify mode: If data are written, go to step (8); if not, repeats steps (4) to (6). If no data are written yet after they are repeated 25 times, go to step (7).
(7) Assume the device to be defective and stop write operation.
(8) Input write data and a program pulse of (number of times steps (4) to (6) were repeated: X) × 3 ms (additional writing).
(9) Increment the address.
(10) Repeat steps (4) to (9) until the address exceeds the last address.

Fig. 3-1 is a timing chart of these steps (2) to (8).

Fig. 3-1 PROM Write/Verify Timing Chart



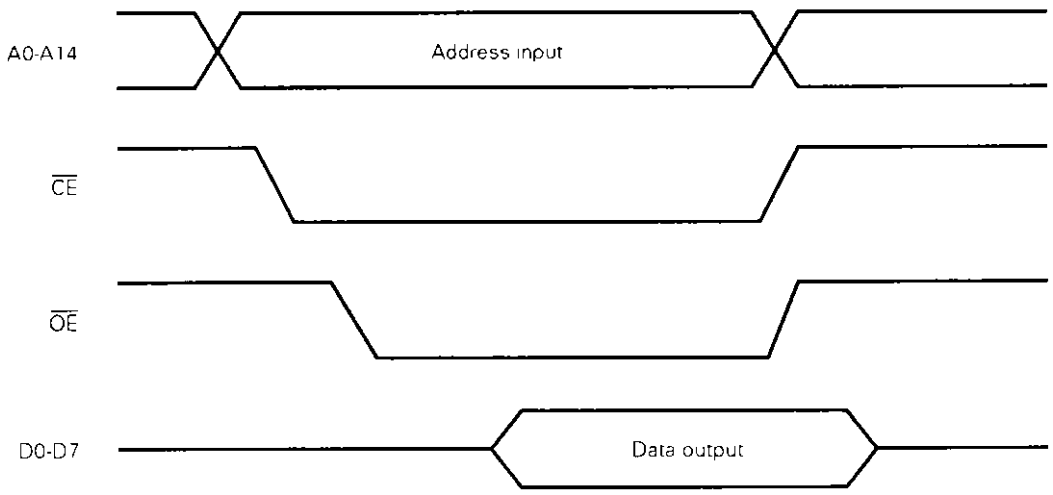
3.4 PROCEDURE FOR READING FROM PROM

The contents of PROM can be read out to the external data bus (D0 to D7) in the following steps:

(1) Always set the $\overline{\text{RESET}}$ pin to low. Apply +12.5 V to the PROG pin. Handle other unused pins as shown in Table 3-3.
(2) Apply +5 V to the V_{DD} and V_{PP} pins.
(3) Input the address of data to be read into the A0 to A14 pins.
(4) Read mode
(5) Output the data on the D0 to D7 pins.

Fig. 3-2 is a timing chart of these steps (2) to (5).

Fig. 3-2 PROM Read Timing Chart



4. ERASURE CHARACTERISTICS ONLY FOR THE μPD78P138K

The programmed data of the μPD78P138K can be erased by exposure to light with a wavelength less than approx. 400 nm (all of the EPROM data are set to FFH).

To erase the contents of program memory in the μPD78P138K, expose the erasure window to ultraviolet light with the wavelength of 254 nm. The amount of light required to completely erase the contents of program memory is a minimum of 15 W•s/cm^2 (intensity of ultraviolet light × erasing time). It takes about 15 to 20 minutes to expose the erasure window to a 12000 μW/cm^2 ultraviolet lamp. It may, however, take more time due to the fallen performance of this ultraviolet lamp, dirt on the package window, or suchlike. Note that the μPD78P138K should be placed less than 2.5 cm from the ultraviolet lamp during erasure. In addition, if a filter is attached to the ultraviolet lamp, remove the filter before erasure.

5. PROTECTIVE FILM COVERING THE ERASURE WINDOW ONLY FOR THE μPD78P138K

The erasure window should be covered with a protective film when not erasing the contents of EPROM. This is to prevent the contents of memory from being erased erroneously by exposure to light other than the EPROM-contents erasing lamp. This is also to prevent any malfunction of the internal circuits other than the EPROM due to the light.

6. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}		−0.5 to +7.0	V
	AV_{REF}		−0.5 to V_{DD}	V
	AVss		−0.5 to +0.5	V
Input voltage	V_I		−0.5 to V_{DD} + 0.5	V
Output voltage	V_O		−0.5 to V_{DD} + 0.5	V
Low output current	I_{OL}	1 pin	15	mA
		Total of all output pins	100	mA
High output current	I_{OH}	1 pin	−10	mA
		Total of all output pins	−50	mA
Operating temperature	T_{OPT}		−10 to +70	°C
Storage temperature	T_{STG}		−65 to +150	°C

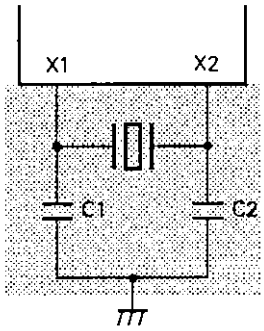
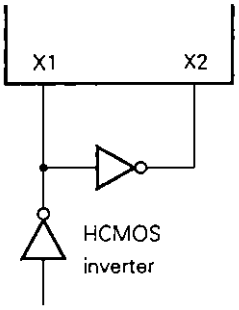
OPERATING CONDITIONS

Clock frequency	Operating temperature (T_a)	Supply voltage (V_{DD})
4 MHz ≤ f_{XX} ≤ 12 MHz	−10 to +70 °C	+5.0 V ±10 %

CAPACITANCE (T_a = 25 °C, V_{DD} = Vss = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input capacitance	C_I			20	pF	f_C = 1 MHz 0 V on pins other than measured pins
Output capacitance	C_O			20	pF	
I/O capacitance	C_{IO}			20	pF	

OSCILLATOR CHARACTERISTICS (T_a = -10 to +70 °C, V_{DD} = +5.0 V ±10 %, Vss = 0 V)

Resonator	Recommended circuit	Parameter	Min.	Max.	Unit	
Ceramic or crystal resonator		Oscillation frequency (fxx)	4 or 6 Note	12	MHz	
External clock		X1 input frequency (fx)	4 or 6 Note	12	MHz	
		X1 input rising (falling) time (t_{XR}, t_{XF})	0	30	ns	
		X1 input high-level (low-level) width (t_{WXH}, t_{WXL})	30	130	ns	★

Cautions 1. The oscillation circuit must be as near pins X1 and X2 as possible.

2. No signals are allowed in the shaded portion.

Note When an A/D converter is used : 6 MHz
When an A/D converter is not used: 4 MHz

DC CHARACTERISTICS (T_a = -10 to +70 °C, V_{DD} = +5.0 V ±10 %, Vss = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Low-level input voltage	V_{IL}	0		0.8	V		
High-level input voltage	V_{IH1}	2.2		V_{DD}	V	Pins other than those shown in **Note 1**	
	V_{IH2}	0.8V_{DD}		V_{DD}	V	Pins shown in **Note 1**	
Low-level output voltage	V_{OL1}			0.45	V	I_{OL} = 2.0 mA, except for **Note 2**	
	V_{OL2}			1.0	V	I_{OL} = 8.0 mA **Note 2**	
High-level output voltage	V_{OH1}	V_{DD} – 1.0			V	I_{OH} = –1.0 mA, except for **Note 3**	
	V_{OH2}	V_{DD} – 0.5			V	I_{OH} = –100 μA, except for **Note 3**	
	V_{OH3}	2.0			V	I_{OH} = –5.0 mA **Note 3**	
Input leakage current	I_{LI}			±10	μA	0 V ≤ V_I ≤ V_{DD}	
Output leakage current	I_{LO}			±10	μA	0 V ≤ V_O ≤ V_{DD}	
AV_{REF} current	AI_{REF}		1.5	5.0	mA	Operation mode, fxx = 12 MHz	
V_{DD} supply current	I_{DD}		20	40	mA	Operation mode, fxx = 12 MHz	
Data retention voltage	V_{DDDR}	2.0		5.5	V	STOP mode	
Data retention current	I_{DDDR}		1	10	μA	STOP mode	V_{DDDR} = 2.0 V
			2	20	μA		V_{DDDR} = 5 V ±10 %
Pull-up resistor	R_L	15	40	80	kΩ	V_I = 0 V	

Notes 1. Pins X1, X2, $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2, P24/CTI10, P25/CTI00, P26/CTI11, P27/CLR1, P34/CLR0, P35/SI, P36/SO/SB0, P37/$\overline{\text{SCK}}$, and $\overline{\text{EA}}$

2. Pins P10-P17

3. Pins P00-P07

AC CHARACTERISTICS (T_a = -10 to +70 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

Read/Write Operation

Parameter	Symbol		Min.	Max.	Unit	Conditions
X1 input clock cycle time	t_{CYX}		82	250	ns	
Address setup time (to ASTB↓)	t_{SAST}	*	52		ns	
Address hold time (to ASTB↓)	t_{HSTA}		25		ns	R_L = 5 kΩ, C_L = 50 pF
Address → $\overline{RD}$↓ delay time	t_{DAR}	*	129		ns	
Address float time (to $\overline{RD}$↓)	t_{FAR}	*	11		ns	
Address → data input time	t_{DAID}	*		228	ns	
ASTB↓ → data input time	t_{DSTID}	*		181	ns	
$\overline{RD}$↓ → data input time	t_{DRID}	*		99	ns	
ASTB↓ → $\overline{RD}$↓ delay time	t_{DSTR}	*	52		ns	
Data hole time (to $\overline{RD}$↑)	t_{HRID}		0		ns	
$\overline{RD}$↑ → address active time	t_{DRA}	*	124		ns	
$\overline{RD}$↑ → ASTB↑ delay time	t_{DRST}	*	124		ns	
$\overline{RD}$ low-level width	t_{WRL}	*	124		ns	
ASTB high-level width	t_{WSTH}	*	52		ns	
Address → $\overline{WR}$↓ delay time	t_{DAW}	*	129		ns	
ASTB↓ → data output time	t_{DSTOD}	*		142	ns	
$\overline{WR}$↓ → data output time	t_{OWOD}			60	ns	
ASTB↓ → $\overline{WR}$↓ delay time	t_{DSTW}	*	52		ns	
Data setup time (to $\overline{WR}$↑)	t_{SODWR}	*	146		ns	
Data hold time (to $\overline{WR}$↑) **Note**	t_{HWOD}	*	22		ns	
$\overline{WR}$↑ → ASTB↑ delay time	t_{DWST}	*	42		ns	
$\overline{WR}$ low-level width	t_{WWL}	*	196		ns	

Note The hold time includes the time for holding V_{OH} and V_{OL} on the load conditions of C_L = 100 pF and R_L = 2 kΩ.

Remarks 1. The values listed in the above table are obtained when fxx = 12 MHz and C_L = 100 pF.

2. See **t_{CXY}-Dependent Bus Timing Definition** for additional information about the parameters with an asterisk (*) in the symbol column.

t_{CYX}-Dependent Bus Timing Definition

Parameter	Symbol	Calculation formula	Min./Max.	12 MHz	Unit
X1 input clock cycle time	t_{CYX}		Min.	82	ns
Address setup time (to ASTB↓)	t_{SAST}	t_{CYX} – 30	Min.	52	ns
Address → $\overline{RD}$↓ delay time	t_{DAR}	2t_{CYX} – 35	Min.	129	ns
Address float time (to $\overline{RD}$↓)	t_{FAR}	t_{CYX}/2 – 30	Min.	11	ns
Address → data input time	t_{DAID}	(4 + 2n)t_{CYX} – 100	Max.	228	ns
ASTB↓ → data input time	t_{DSTID}	(3 + 2n)t_{CYX} – 65	Max.	181	ns
RD↓ → data input time	t_{DRID}	(2 + 2n)t_{CYX} – 65	Max.	99	ns
ASTB↓ → $\overline{RD}$↓ delay time	t_{DSTR}	t_{CYX} – 30	Min.	52	ns
$\overline{RD}$↑ → address active time	t_{DRA}	2t_{CYX} – 40	Min.	124	ns
$\overline{RD}$↑ → ASTB↑ delay time	t_{DRST}	2t_{CYX} – 40	Min.	124	ns
$\overline{RD}$ low level width	t_{WRL}	(2 + 2n)t_{CYX} – 40	Min.	124	ns
ASTB high-level width	t_{WSTH}	t_{CYX} – 30	Min.	52	ns
Address → $\overline{WR}$↓ delay time	t_{DAW}	2t_{CYX} – 35	Min.	129	ns
ASTB↓ → data output time	t_{DSTOD}	t_{CYX} + 60	Max.	142	ns
ASTB↓ → $\overline{WR}$↓ delay time	t_{DSTW}	t_{CYX} – 30	Min.	52	ns
Data setup time (to $\overline{WR}$↑)	t_{SODWR}	(3 + 2n)t_{CYX} – 100	Min.	146	ns
Data setup time (to $\overline{WR}$↓)	t_{SODWF}	t_{CYX} – 60	Min.	22	ns
$\overline{WR}$↑ → ASTB↑ delay time	t_{DWST}	t_{CYX} – 40	Min.	42	ns
$\overline{WR}$ low-level width	t_{WWL}	(3 + 2n)t_{CYX} – 50	Min.	196	ns

Remarks 1. n represents the number of wait cycles inserted according to the specification of the memory mapping register (MM).

2. The standard values for 12 MHz are obtained when n is 0.

3. The items that are not listed in the above table do not depend on the clock frequency (fxx).

Serial Operation

Parameter	Symbol	Min.	Max.	Unit	Conditions	
Serial clock cycle time	t_{CYSK}	1.0		μs	Input	External clock
		1.3		μs	Output	f_{CLK} divided by 8
		5.3		μs		f_{CLK} divided by 32
Serial clock low-level width	t_{WSKL}	420		ns	Input	External clock
		556		ns	Output	f_{CLK} divided by 8
		2.5		μs		f_{CLK} divided by 32
Serial clock high-level width	t_{WSKH}	420		ns	Input	External clock
		556		ns	Output	f_{CLK} divided by 8
		2.5		μs		f_{CLK} divided by 32
SI, SB0 setup time (to $\overline{SCK}\uparrow$)	t_{SSSK}	150		ns		
SI, SB0 hold time (to $\overline{SCK}\uparrow$)	t_{HSSK}	400		ns		
SO/SB0 output delay time (to $\overline{SCK}\downarrow$)	t_{DSBSK1}	0	300	ns	CMOS push-pull output (three-wire serial I/O mode)	
	t_{DSBSK2}	0	800	ns	Open-drain output (SBI mode), R_L = 1kΩ	
SB0 high hold time (to $\overline{SCK}\uparrow$)	t_{HSBSK}	4		t_{CYX}	SBI mode	
SB0 low setup time (to $\overline{SCK}\downarrow$)	t_{SSBSK}	4		t_{CYX}		
SB0 low-level width	t_{WSBL}	4		t_{CYX}		
SB0 high-level width	t_{WSBH}	4		t_{CYX}		

Remarks 1. The values listed in the above table are obtained when fxx = 12 MHz and C_L = 100 pF.

2. f_{CLK} indicates the internal system clock (fx or fxx divided by 2).

Other Operations

	Parameter		Symbol	Min.	Max.	Unit	Conditions	
	CTI00, CTI10, CTI11 low-level width		t_{WCTL}	4		t_{CYX}		
	CTI00, CTI10, CTI11 high-level width		t_{WCTH}	4		t_{CYX}		
	CLR1 low-level width		t_{WCR1L}	4		t_{CYX}	Digital noise eliminator not used	
★				40		t_{CYX}	Digital noise eliminator used	ICR.4 = 0 Note
★				80		t_{CYX}		ICR.4 = 1 Note
	CLR1 high-level width		t_{WCR1H}	4		t_{CYX}	Digital noise eliminator not used	
★				40		t_{CYX}	Digital noise eliminator used	ICR.4 = 0 Note
★				80		t_{CYX}		ICR.4 = 1 Note
	Digital noise eliminator	Removed pulse width	t_{WSEP}		32	t_{CYX}	ICR.4 = 0 Note	
		Passed pulse width		40		t_{CYX}		
		Removed pulse width			72	t_{CYX}	ICR.4 = 1 Note	
		Passed pulse width		80		t_{CYX}		
	NMI low-level width		t_{WNIL}	10		μs		
	NMI high-level width		t_{WNIH}	10		μs		
	INTP0-INTP2 low-level width		t_{WNIPL}	4		t_{CYX}		
	INTP0-INTP2 high-level width		t_{WNIPH}	4		t_{CYX}		
	$\overline{\text{RESET}}$ low-level width		t_{WRSL}	10		μs		
	$\overline{\text{RESET}}$ high-level width		t_{WRSH}	10		μs		

Note Bit 4 of the input control register (ICR)

Clock Output Operation

Parameter	Symbol	Calculation formula	Min.	Max.	Unit
CLO cycle time	t_{CYCL}		333	2667	ns
CLO low-level width	t_{CLL}	$t_{CYCL}/2 \pm 50$	116	138	ns
CLO high-level width	t_{CLH}	$t_{CYCL}/2 \pm 50$	116	138	ns
CLO rising time	t_{CLR}			50	ns
CLO falling time	t_{CLF}			50	ns

Remark The values in the table are obtained when fxx = 12 MHz and C_L = 100 pF.

External Clock Timing

Parameter	Symbol	Min.	Max.	Unit	Conditions
X1 input low-level width	t_{WXL}	30	130	ns	
X1 input high-level width	t_{WXH}	30	130	ns	
X1 input rising time	t_{XR}	0	30	ns	
X1 input falling time	t_{XF}	0	30	ns	
X1 input clock cycle time	t_{CYX}	82	250	ns	

A/D CONVERTER CHARACTERISTICS (T_a = −10 to +70 °C, V_{DD} = +5.0 V ±10 %, 3.8 V ≤ AV_{REF} ≤ V_{DD}, AVss = Vss = 0 V)

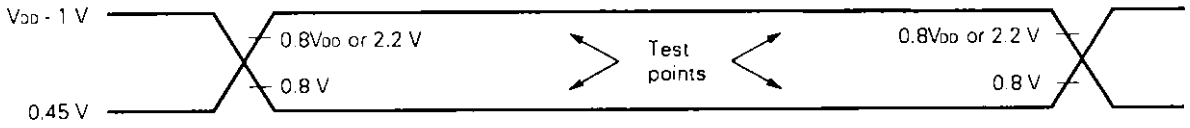
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Resolution		8			bit	
Total error				0.4	%	4.0 V ≤ AV_{REF} ≤ V_{DD}
				0.8	%	3.8 V ≤ AV_{REF} ≤ V_{DD}
Quantization error				±1/2	LSB	
Conversion time	t_{CONV}	360			t_{CYX}	83 ns ≤ t_{CYX} ≤ 125 ns
		240			t_{CYX}	125 ns ≤ t_{CYX} ≤ 250 ns
Sampling time	t_{SAMP}	72			t_{CYX}	83 ns ≤ t_{CYX} ≤ 125 ns
		48			t_{CYX}	125 ns ≤ t_{CYX} ≤ 250 ns
Analog input voltage	V_{IAN}	-0.3		AV_{REF} + 0.3	V	
Analog input impedance	R_{AN}		1000		MΩ	
Reference voltage	AV_{REF}	3.8		V_{DD}	V	
AV_{REF} current	AI_{REF}		1.5	5.0	mA	Normal operation mode, f_{XX} = 12 MHz
			0.7	1.5	mA	STOP mode

DATA MEMORY LOW-VOLTAGE DATA RETENTION CHARACTERISTICS (T_a = -10 to +70 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Data retention voltage	V_{DDDR}	2.0		5.5	V	STOP mode
Data retention current	I_{DDDR}		1	10	μA	V_{DDDR} = 2.0 V
			2	20	μA	V_{DDDR} = 5 V ±10 %
V_{DD} rising time	t_{RVD}	200			μs	
V_{DD} falling time	t_{FVD}	200			μs	
STOP release signal input time	t_{DREL}	0			ms	
Low-level input voltage	V_{IL}	0		0.1V_{DD}	V	Specified pins **Note**
High-level input voltage	V_{IH}	0.9V_{DD}		V_{DD}	V	

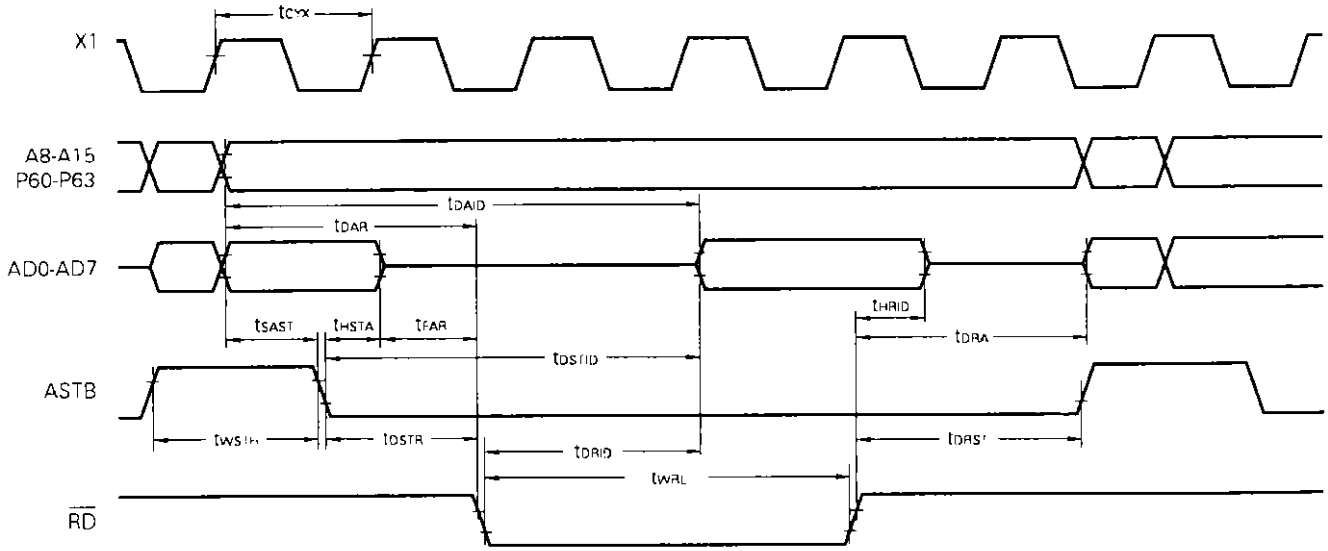
Note Pins $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2, P24/CTI10, P25/CTI00, P26/CTI11, P27/CLR1, P34/CLR0, P35/SI, P36/SO/SB0, P37/$\overline{\text{SCK}}$, and $\overline{\text{EA}}$

AC Timing Test Points

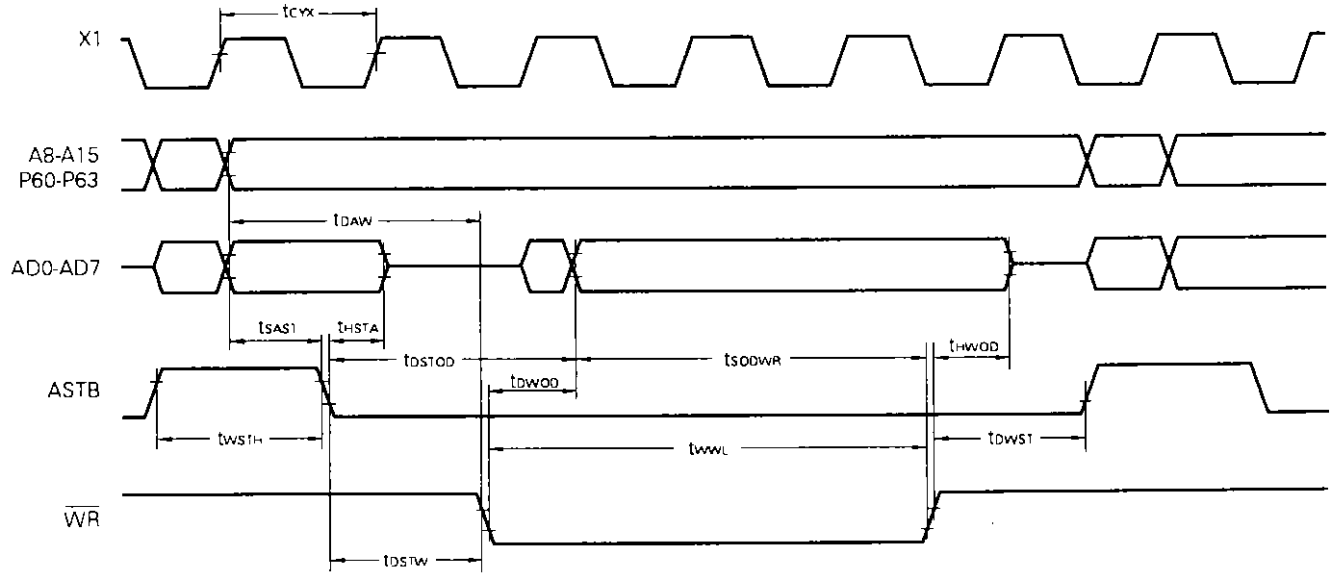


Timing Waveform

Read operation:

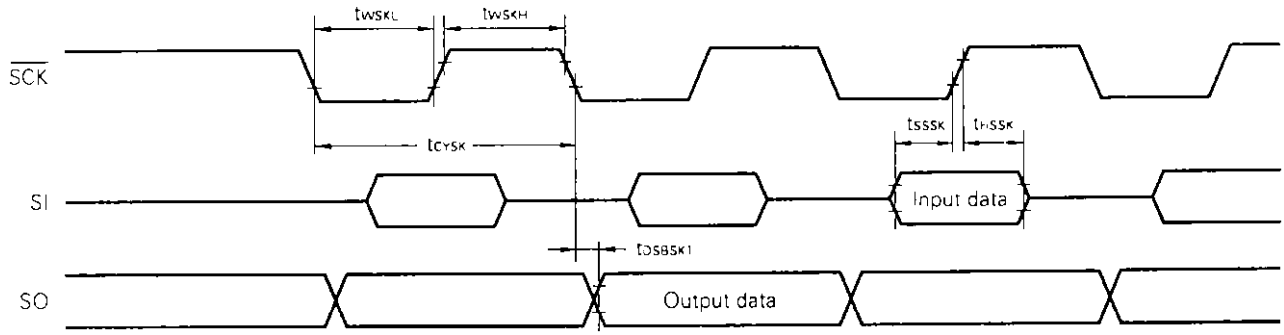


Write operation:



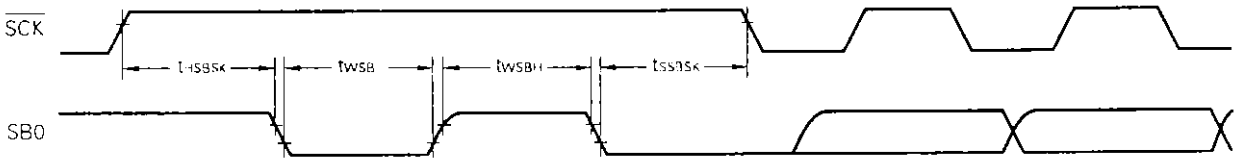
Serial Operation

Three-wire serial I/O mode:

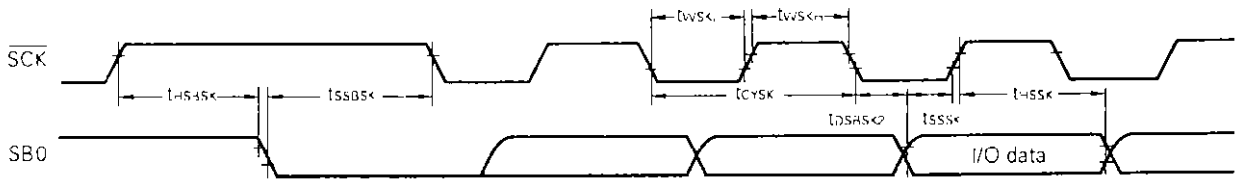


SBI Mode

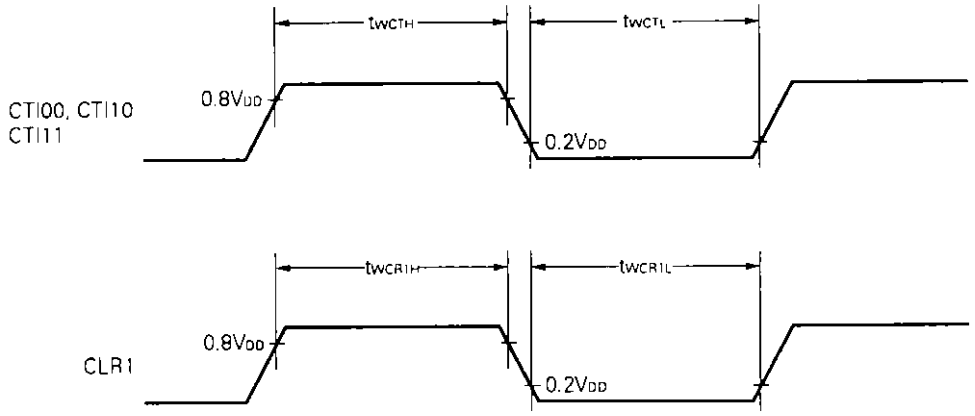
Bus release signal transfer:



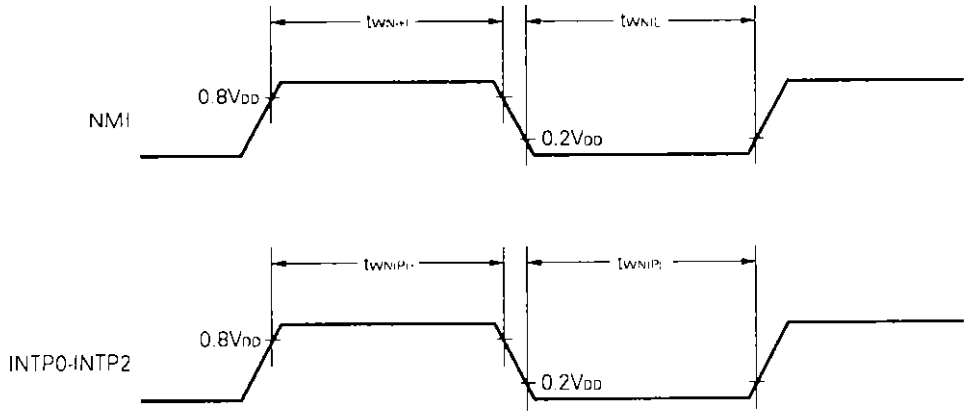
Command signal transfer:



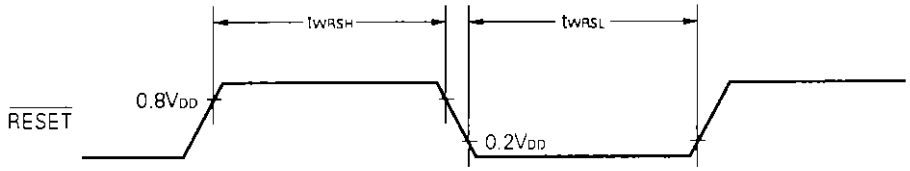
Super Timer Unit Input Timing



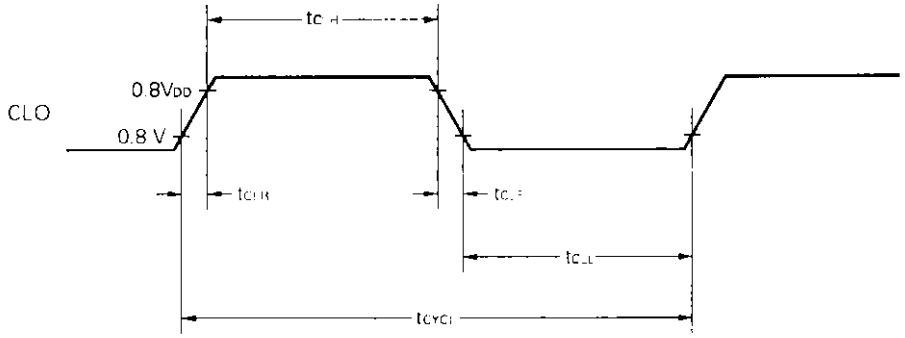
Interrupt Input Timing



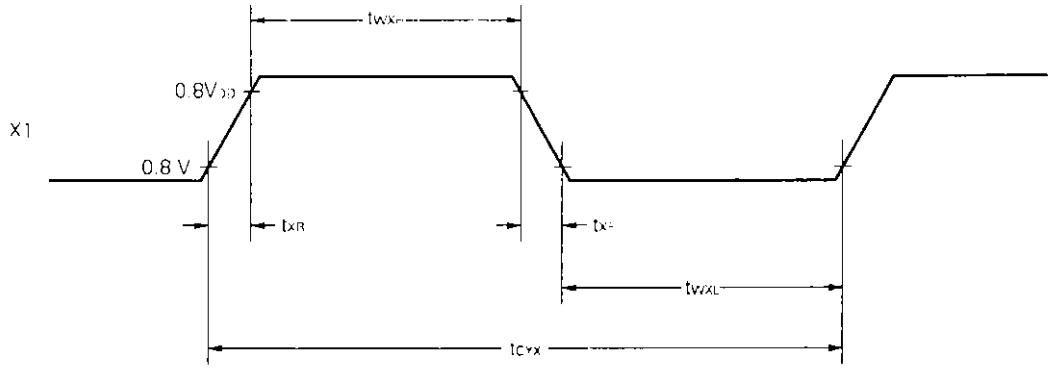
Reset Input Timing



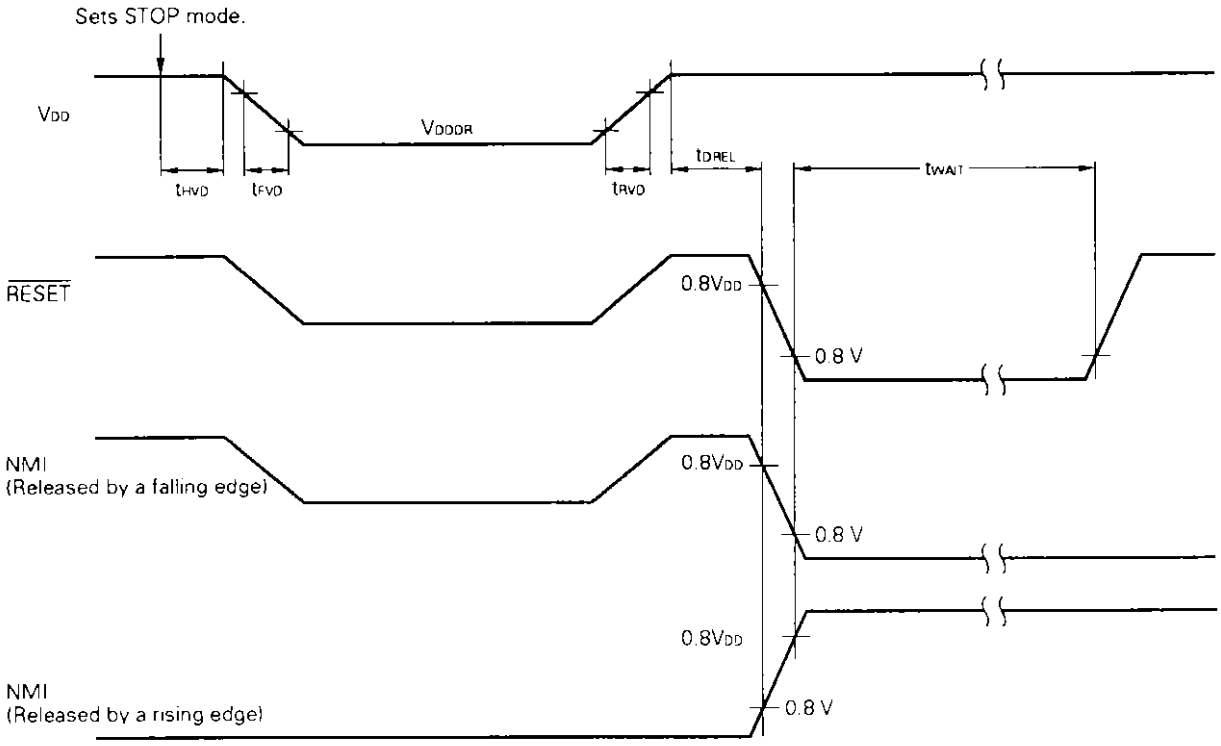
Clock Output Timing



External Clock Timing



Data Retention Timing



DC PROGRAMMING CHARACTERISTICS (T_a = 25 ± 5 °C, V_{IP} = 12.5 ±0.5 V, Vss = 0 V)

Item	Symbol	Symbol Note	Min.	Typ.	Max.	Unit	Condition
High-level input voltage	V_{IH}	V_{IH}	2.4		V_{DDP}+0.3	V	
Low-level input voltage	V_{IL}	V_{IL}	−0.3		0.8	V	
Input leakage current	I_{LI}	I_{LI}			10	μA	$0 \le V_I \le V_{DDP}$
High-level output voltage	V_{OH}	V_{OH}	2.4			V	I_{OH} = −400 μA
Low-level output voltage	V_{OL}	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output leakage current	I_{LO}				10	μA	$0 \le V_O \le V_{DDP}$, $\overline{OE}$ = V_{IH}
NMI pin high-voltage input current	I_{IP}				±10	μA	
V_{DDP} supply voltage	V_{DDP}	V_{CC}	5.75	6.0	6.25	V	Program memory write mode
			4.5	5.0	5.5	V	Program memory read mode
V_{PP} supply voltage	V_{PP}	V_{PP}	12.2	12.5	12.8	V	Program memory write mode
			V_{PP} = V_{DDP}			V	Program memory read mode
V_{DDP} supply current	I_{DD}	I_{CC}		5	30	mA	Program memory write mode
				5	30	mA	Program memory read mode $\overline{CE}$ = V_{IL}, V_I = V_{IH}
V_{PP} supply current	I_{PP}	I_{PP}		5	30	mA	Program memory write mode $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}
				1	100	μA	Program memory read mode

Note Symbols for the corresponding μPD27C256A

AC PROGRAMMING CHARACTERISTICS

(T_a = 25 ±5 °C, V_{DD} = 6.0 ±0.25 V, V_{IP} = 12.5 ±0.5 V, V_{PP} = 12.5 ±0.3 V, Vss = 0 V)

Item	Symbol	Symbol Note	Min.	Typ.	Max.	Unit	Conditions
Address set up time to $\overline{CE}\downarrow$	t_{SAC}	t_{AS}	2			μs	
$\overline{OE}\downarrow$ delay time from data	t_{DDOO}	t_{OES}	2			μs	
Input data setup time to $\overline{CE}\downarrow$	t_{SIDC}	t_{DS}	2			μs	
Address hold time to $\overline{CE}\uparrow$	t_{HCA}	t_{AH}	2			μs	
Input data hold time to $\overline{CE}\uparrow$	t_{HCID}	t_{DH}	2			μs	
Output data hold time to $\overline{OE}\uparrow$	t_{HOOD}	t_{DF}	0		130	ns	
V_{PP} setup time to $\overline{CE}\downarrow$	t_{SVPS}	t_{VPS}	1			ms	
V_{DDP} setup time to $\overline{CE}\downarrow$	t_{SVDC}	t_{VDS}	1			ms	
Initial program pulse width	t_{WL1}	t_{PW}	0.95	1.0	1.05	ms	
Additional program pulse width	t_{WL2}	t_{OPW}	2.85		78.75	ms	
NMI high-voltage input setup time to $\overline{CE}\downarrow$	t_{SPC}		2			μs	

Note Symbols for corresponding μPD27C256A

READ OPERATION ★

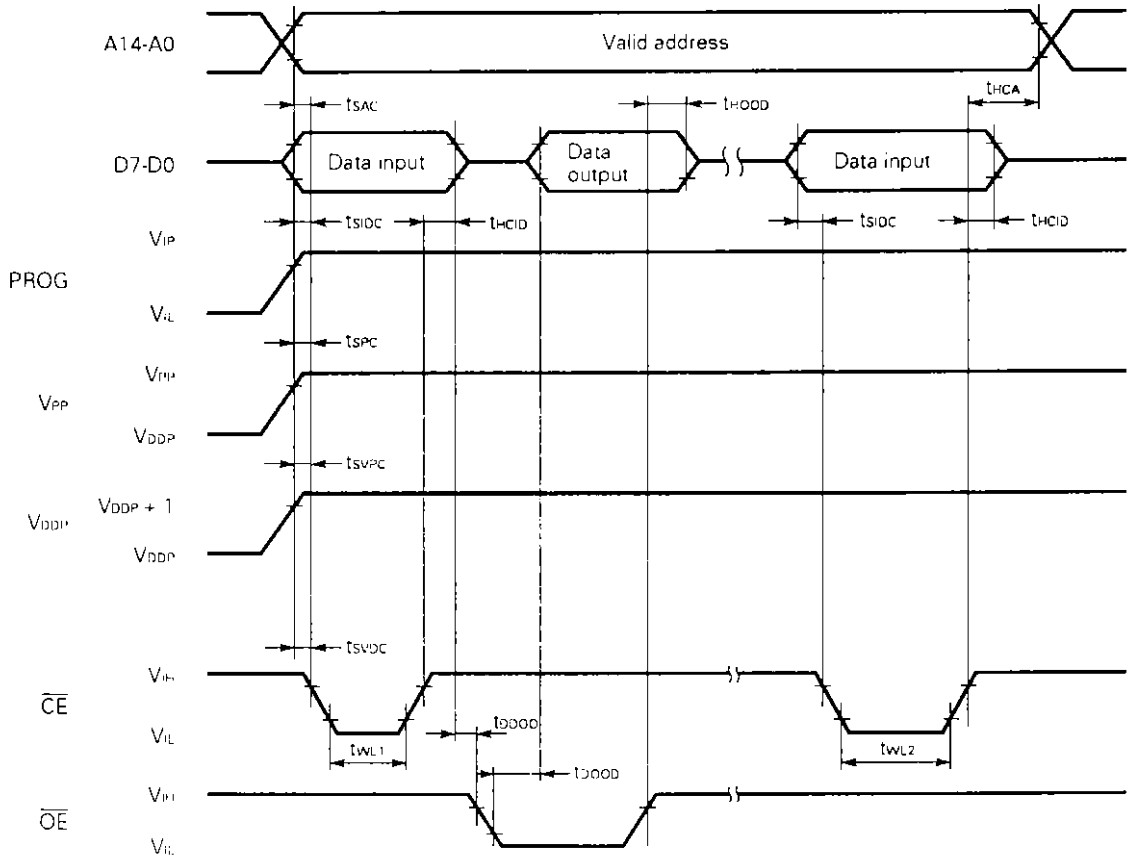
(T_a = 25 ±5 °C, V_{DD} = 5.0 ±0.5 V, V_{IP} = 12.5 ±0.5 V, V_{PP} = V_{DDP}, Vss = 0 V)

Item	Symbol	Symbol Note 1	Min.	Typ.	Max.	Unit	Conditions
Data output time from address	t_{DAOD}	t_{ACC}			2	μs	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}\downarrow\rightarrow$ data output time	t_{DCOD}	t_{CE}			2	μs	$\overline{OE}$ = V_{IL}
$\overline{OE}\downarrow\rightarrow$ data output time	t_{DOOD}	t_{OE}			1	μs	$\overline{CE}$ = V_{IL}
Data hold time to $\overline{OE}\uparrow$ or $\overline{CE}\uparrow$ Note 2	t_{HCOD}	t_{DF}	0		130	ns	$\overline{CE}$ = V_{IL} or $\overline{OE}$ = V_{IL}
Data hold time to address	t_{HAOD}	t_{OH}	0			ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Notes 1. Symbols for the corresponding μPD27C256A

2. t_{HCOD} is the time measured from when either $\overline{OE}$ or $\overline{CE}$ reaches V_{IH}, whichever is faster.

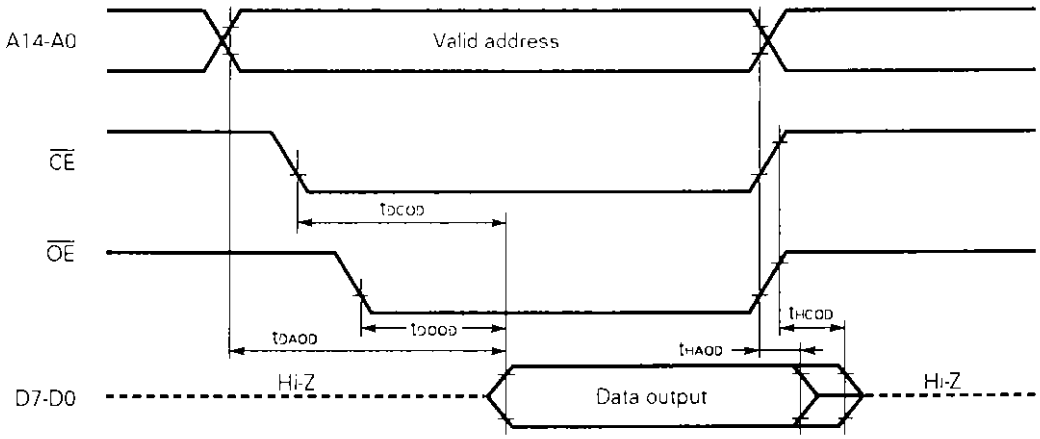
One-Time PROM Write Mode Timing



Cautions 1. V_{DDP} must be applied before V_{PP}, and must be cut after V_{PP}.

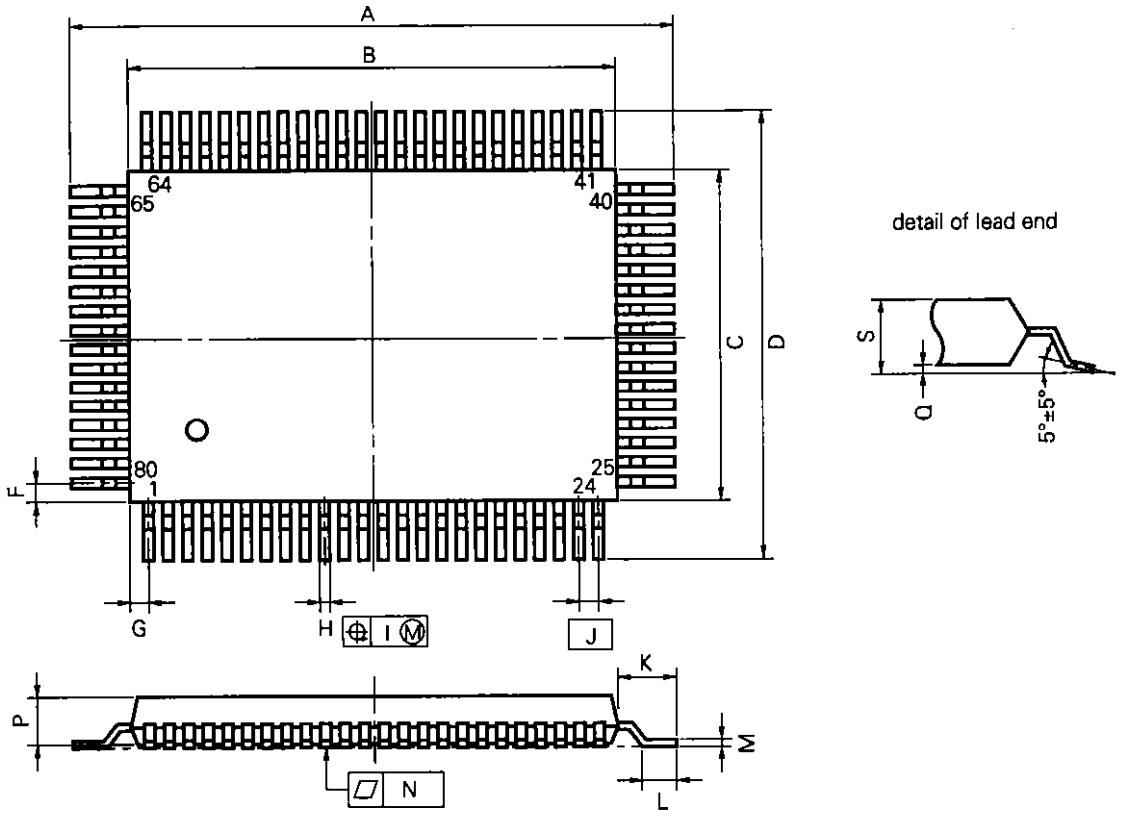
2. V_{PP} including overshoot must not exceed +13 V.

One-Time PROM Read Mode Timing



7. PACKAGE DIMENSIONS

80 PIN PLASTIC QFP (14×20)



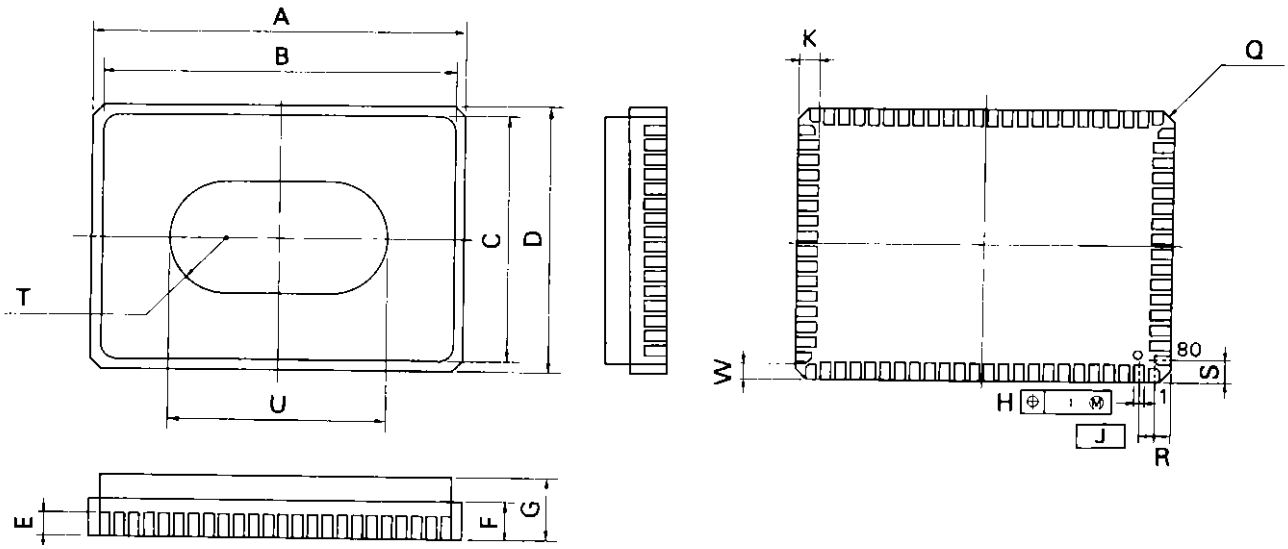
P80GF-80-3B9-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	0.8	0.031
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

★ 80PIN LCC



X80KW-80A

NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$20.0^{\pm 0.4}$	$0.787^{+0.017}_{-0.016}$
B	19.0	0.748
C	13.2	0.520
D	$14.2^{\pm 0.4}$	$0.559^{\pm 0.016}$
E	1.64	0.065
F	2.14	0.084
G	4.064 MAX.	0.160 MAX.
H	$0.51^{\pm 0.10}$	$0.020^{\pm 0.004}$
I	0.08	0.003
J	0.8 (T.P.)	0.031 (T.P.)
K	$1.0^{\pm 0.2}$	$0.039^{+0.008}_{-0.009}$
Q	C0.5	C0.020
R	0.8	0.031
S	1.1	0.043
T	R3.0	R0.118
U	12.0	0.472
W	$0.75^{\pm 0.2}$	$0.030^{+0.008}_{-0.009}$

8. RECOMMENDED SOLDERING CONDITIONS ★

The following conditions (see table below) must be met when soldering this product.

For the details of the recommended soldering conditions refer to our document "SMT MANUAL" (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 8-1 Soldering Conditions for Surface-Mount Devices

μPD78P138GF-3B9: 80-pin plastic QFP (14 mm × 20 mm excluding the dimensions of the pins)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 230 °C Reflow time: 30 seconds or less (at 210 °C or higher) Number of reflow processes: 1 Exposure limit: 2 days Note (16 hours of pre-baking is required at 125 °C afterward.)	IR30-162-1
VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (at 200 °C or higher) Number of reflow processes: 1 Exposure limit: 2 days Note (16 hours of pre-baking is required at 125 °C afterward.)	VP15-162-1
Partial heating method	Terminal temperature: 300 °C or below Flow time: 3 seconds or less (one side per device)	–

Note Exposure limit before soldering after dry-pack package is opened.
Storage conditions: Temperature of 25 °C and maximum relative humidity at 65 % or less

Caution Do not apply more than a single process at once, except for "Partial heating method."

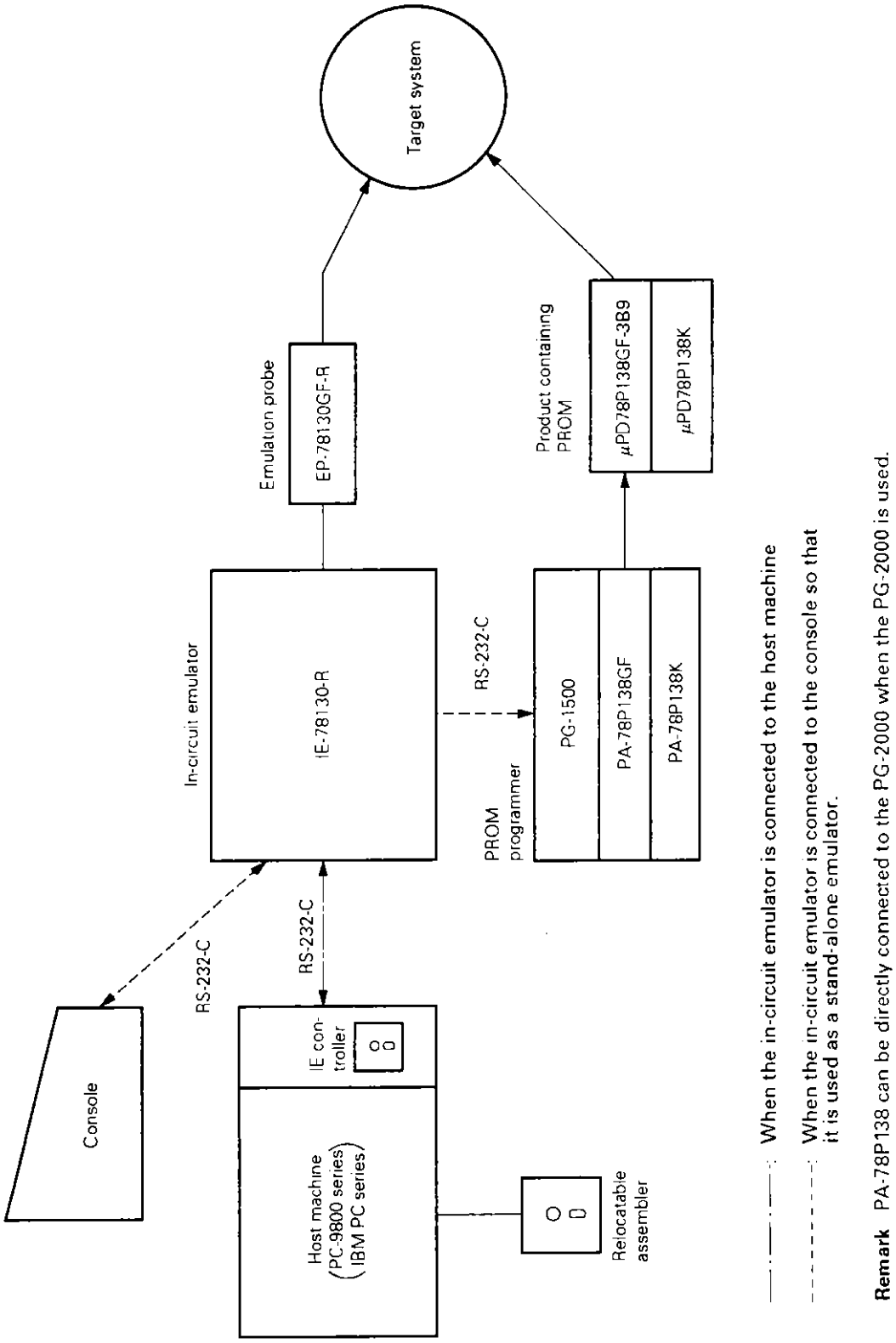
★ APPENDIX DEVELOPMENT TOOLS

The following development tools are readily available for development of systems using the μPD78P138.

Hardware	IE-78130-R	IE-78130-R is an in-circuit emulator which can be used for developing and debugging application systems for μPD78P138. This emulator is connected to the host machine or console when debugging is performed. The connection of the emulator to the host machine enables symbolic debugging and file transfer between the emulator and the host machine for enhancement of debugging efficiency. IE-78130-R has the Centronics interface in addition to two channels of the RS-232-C serial interfaces, so that it can be connected to the PROM programmer such as PG-1500.			
	EP-78130GF-R	EP-78130GF-R is an emulation probe for connecting the IE-78130-R to a target system.			
	PA-78P138GF PA-78P138K	PA-78P138GF and PA-78P138K are socket adapters for writing a program into μPD78P138GF/K using PG-1500.			
Software	IE-78130-R control program (IE-controller)	Host machine	OS	Distribution media	Part number
		PC-9800 series	MS-DOS™ (Ver. 3.10 to Ver. 3.30C)	5-inch 2HD	μS5A10IE78130
				3.5-inch 2HD	μS5A13IE78130
		IBM PC series	PC DOS™ (Ver. 3.1 to Ver. 3.3	5-inch 2HC	μS7B10IE78130
	RA78K/I relocatable assembler	Host machine	OS	Distribution media	Part number
		PC-9800 series	MS-DOS (Ver. 3.10 to Ver. 3.30C)	5-inch 2HD	μS5A10RA78K1
				3.5-inch 2HD	μS5A13RA78K1
		IBM PC series	PC DOS (Ver. 3.1 to Ver. 3.3)	5-inch 2HC	μS7B10RA78K1

Remark IE-controller and assembler operations are guaranteed only on the host machine and by the OS mentioned above.

Configuration of development tools ★



Remark PA-78P138 can be directly connected to the PG-2000 when the PG-2000 is used.

Cautions on CMOS Devices

① **Countermeasures against static electricity for all MOSs**

Caution **When handling MOS devices, take care so that they are not electrostatically charged.**

Strong static electricity may cause dielectric breakdown in gates. When transporting or storing MOS devices, use conductive trays, magazine cases, shock absorbers, or metal cases that NEC uses for packaging and shipping. Be sure to ground MOS devices during assembling. Do not allow MOS devices to stand on plastic plates or do not touch pins. Also handle boards on which MOS devices are mounted in the same way.

② **CMOS-specific handling of unused input pins**

Caution **Hold CMOS devices at a fixed input level.**

Unlike bipolar or NMOS devices, if a CMOS device is operated with no input, an intermediate-level input may be caused by noise. This allows current to flow in the CMOS device, resulting in a malfunction. Use a pull-up or pull-down resistor to hold a fixed input level. Since unused pins may function as output pins at unexpected times, each unused pin should be separately connected to the V_{DD} or GND pin through a resistor.

If handling of unused pins is documented, follow the instructions in the document.

③ **Statuses of all MOS devices at initialization**

Caution **The initial status of a MOS device is unpredictable when power is turned on.**

Since characteristics of a MOS device are determined by the amount of ions implanted in molecules, the initial status cannot be determined in the manufacture process. NEC has no responsibility for the output statuses of pins, input and output settings, and the contents of registers at power on. However, NEC assures operation after reset and items for mode setting if they are defined.

When you turn on a device having a reset function, be sure to reset the device first.

[MEMO]

We recommend to refer to the following separate manual provided for this product.

- μPD78138 USER'S MANUAL (Document No.: IEU-1324)

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