DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD78P098B

8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD78P098B is a member of the μPD78098B Subseries of the 78K/0 Series and is provided with an internal one-time PROM.

Because this device can be programmed by users, it is ideally suited for applications involving the evaluation of systems in development stages, small-scale production of many different products, and rapid development and time-to-market of a new product.

The functions are explained in detail in the following manuals. Be sure to read these manuals when designing your system.

μPD78098B Subseries User's Manual : U12761E
78K/0 Series User's Manual - Instructions : U12326E

FEATURES

- EMI noise reduced product
- Pin-compatible with mask ROM version (except V_{PP} pin)
- Internal PROM: 60 Kbytes Note 1
  Programmable only once (ideal for small-scale production)
- Internal high-speed RAM : 1024 bytes
- Buffer RAM : 32 bytes
- Internal expansion RAM : 2048 bytes Note 2
- Operating voltage same as mask ROM version (V_{DD} = 2.7 to 5.5 V)
- Supports QTOP™ microcontroller

Notes 1. The internal PROM capacity can be changed by using the internal memory size switching register (IMS).

2. Internal expansion RAM capacity can be changed by using the internal expansion RAM size switching register (IXS).

Remark 1. "QTOP microcontroller" is a generic name for one-time PROM-containing microcontrollers totally supported by NEC's writing service (writing, marking, screening, and verification).

2. To find how the PROM version differs from the mask ROM version, refer to **"1. DIFFERENCES BETWEEN μPD78P098B AND MASK ROM VERSIONS."**

ORDERING INFORMATION

Part Number	Package
μPD78P098BGC-3B9	80-pin plastic QFP (14 × 14 mm)

The information in this document is subject to change without notice.

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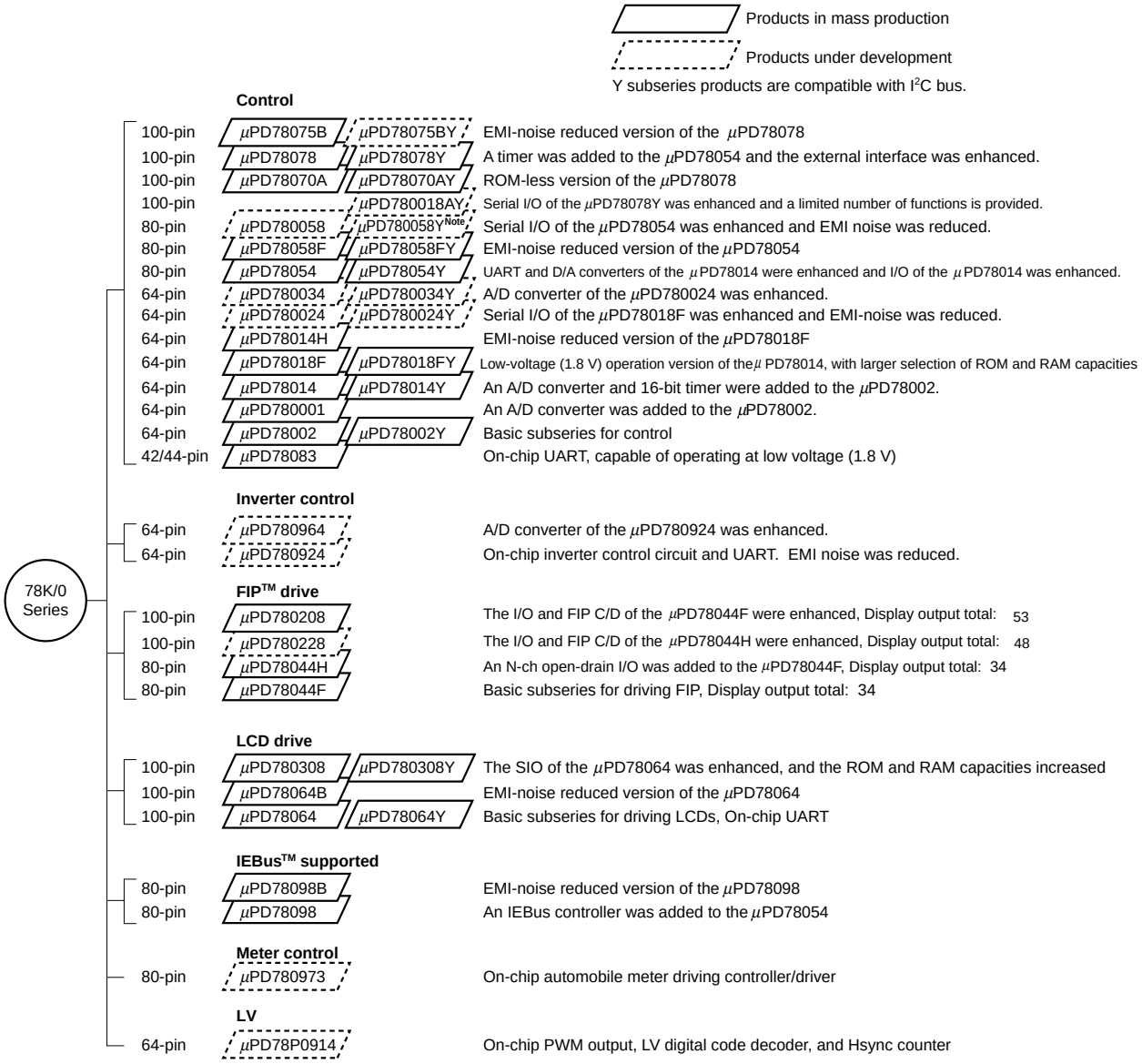
78K/0 Series Development

The following shows the 78K/0 Series products development. Subseries name are shown inside frames.



Note Under development

The following lists the main functional differences between subseries products.

Subseries Name \ Function		ROM Capacity	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-bit	16-bit	Watch	WDT							
Control	μPD78075B	32K-40K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	88	1.8 V	A
	μPD78078	48K-60K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24K-60K	2 ch							3 ch (time division UART: 1 ch)	68	1.8 V	
	μPD78058F	48K-60K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16K-60K										2.0 V	
	μPD780034	8K-32K					–	8 ch	–	3 ch (UART: 1 ch, time division 3-wire: 1 ch)	51	1.8 V	
	μPD780024						8 ch	–					
	μPD78014H									2 ch	53	1.8 V	
	μPD78018F	8K-60K											
	μPD78014	8K-32K										2.7 V	
	μPD780001	8K		–	–					1 ch	39		N/A
	μPD78002	8K-16K			1 ch		–				53		A
	μPD78083				–		8 ch			1 ch (UART: 1 ch)	33	1.8 V	N/A
Inverter control	μPD780964	8K-32K	3 ch	**Note**	–	1 ch	–	8 ch	–	2 ch (UART: 2 ch)	47	2.7 V	A
	μPD780924						8 ch	–					
FIP drive	μPD780208	32K-60K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	2 ch	74	2.7 V	N/A
	μPD780228	48K-60K	3 ch	–	–					1 ch	72	4.5 V	
	μPD78044H	32K-48K	2 ch	1 ch	1 ch						68	2.7 V	
	μPD78044F	16K-40K								2 ch			
LCD drive	μPD780308	48K-60K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	3 ch (time division UART: 1 ch)	57	2.0 V	N/A
	μPD78064B	32K								2 ch (UART: 1 ch)			
	μPD78064	16K-32K											
IEBus supported	μPD78098B	40K-60K	2 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	69	2.7 V	A
	μPD78098	32K-60K											
Meter	μPD780973	24K-32K	3 ch	1 ch	1 ch	1 ch	5 ch	–	–	2 ch (UART: 1 ch)	56	4.5 V	N/A
LV	μPD78P0914	32K	6 ch	–	–	1 ch	8 ch	–	–	2 ch	54	4.5 V	A

Note 10-bit timer: 1 channel

Remark A : Available
N/A : Not available

Function Outline

Item		Function
Internal memory		• PROM : 60 Kbytes Note 1 • RAM High-speed RAM : 1024 bytes Buffer RAM : 32 bytes Expansion RAM : 2048 bytes Note 2
Memory space		64 Kbytes
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Minimum instruction execution time		Minimum instruction execution time variable function
	With main system clock	0.5 μs/1.0 μs/2.0 μs/4.0 μs/8.0 μs/16.0 μs (@ 6.0-MHz operation)
	With subsystem clock	122 μs (@ 32.768-kHz operation)
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulate (set, reset, test, Boolean operation) • BCD adjust, etc.
I/O ports		Total : 69 • CMOS input : 2 • CMOS I/O : 63 • N-ch open-drain I/O : 4
IEBus controller		Effective transmission rate: 3.9 kbps/17 kbps/26 kbps
A/D converter		8-bit resolution × 8 channels
D/A converter		8-bit resolution × 2 channels
Serial interface		• 3-wire serial I/O/SBI/2-wire serial I/O mode selectable : 1 channel • 3-wire serial I/O mode (with up to 32-byte auto send/receive function) : 1 channel • 3-wire serial I/O/UART mode selectable : 1 channel
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel
Timer output		3 (14-bit PWM output: 1)
Clock output		15.6 kHz, 31.3 kHz, 62.5 kHz, 125 kHz, 250 kHz, 500 kHz, 1.0 MHz, 2.0 MHz, 4.0 MHz (@ 6.0-MHz operation with main system clock) 32.768 kHz (@ 32.768-kHz operation with subsystem clock)
Buzzer output		977 Hz, 1.95 kHz, 3.9 kHz, 7.8 kHz (@ 6.0-MHz operation with main system clock)

Notes 1. The internal PROM capacity can be changed by using the internal memory size switching register (IMS).

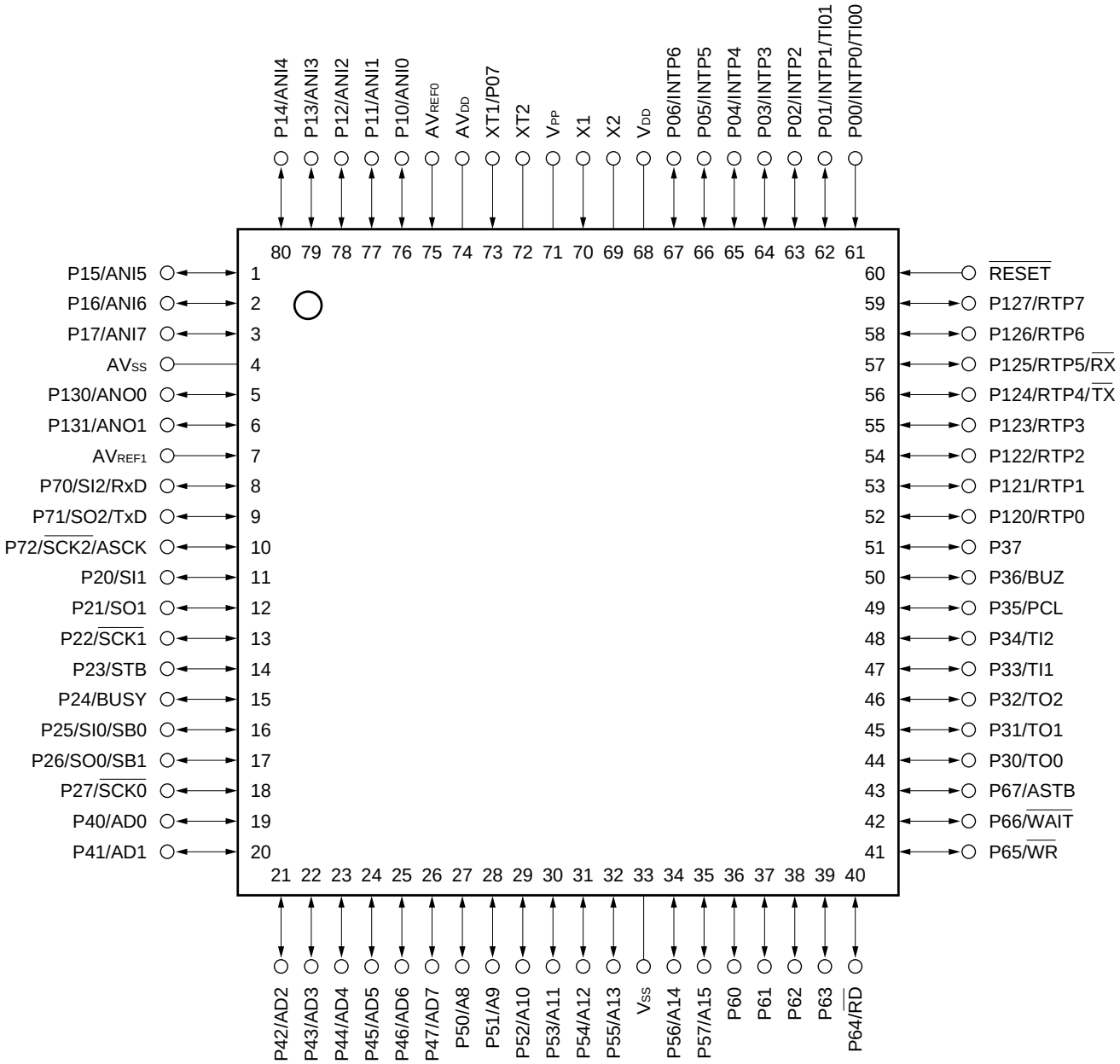
2. 0 or 2048 bytes can be selected by using the internal expansion RAM size switching register (IMS).

Item		Function
Vectored interrupt source	Maskable	Internal: 14, external: 7
	Non-maskable	Internal: 1
	Software	1
Test input		Internal: 1, external: 1
Operating power supply voltage		V_{DD} = 2.7 to 5.5 V
Package		80-pin plastic QFP (14 × 14 mm)

PIN CONFIGURATION (Top View)

(1) Normal operation mode

- **80-pin plastic QFP (14 X 14 mm)**
  μPD78P098BGC-3B9



Cautions 1. Connect V_{PP} pin directly to V_{SS}.

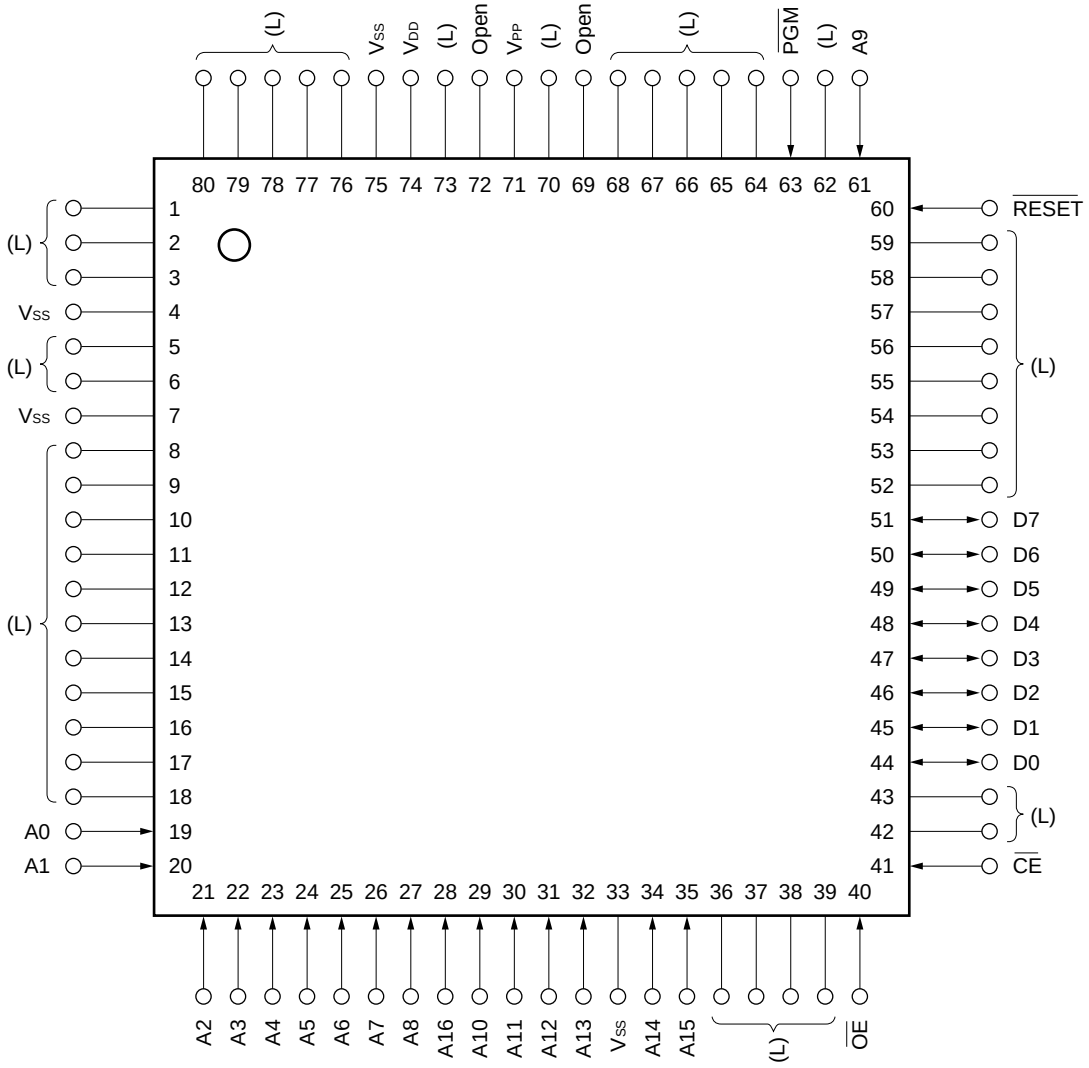
2. The AV_{DD} pin functions as both an A/D converter power supply and a port power supply. When the μPD78P098B is used in applications where the noise generated inside the microcontroller needs to be reduced, connect the AV_{DD} pin to another power supply that has the same potential as V_{DD}.

3. The AV_{SS} pin functions both as a ground of the A/D and D/A converters and as a ground of a port. When the μPD78P098B is used in applications where the noise generated inside the microcontroller needs to be reduced, connect the AV_{SS} pin to a ground line other than V_{SS}.

A8 to A15 : Address Bus
AD0 to AD7 : Address/Data Bus
ANI0 to ANI7 : Analog Input
ANO0, ANO1 : Analog Output
ASCK : Asynchronous Serial Clock
ASTB : Address Strobe
AV_{DD} : Analog Power Supply
AV_{REF0}, AV_{REF1} : Analog Reference Voltage
AV_{SS} : Analog Ground
BUSY : Busy
BUZ : Buzzer Clock
INTP0 to INTP6 : Interrupt from Peripherals
P00 to P07 : Port0
P10 to P17 : Port1
P20 to P27 : Port2
P30 to P37 : Port3
P40 to P47 : Port4
P50 to P57 : Port5
P60 to P67 : Port6
P70 to P72 : Port7
P120 to P127 : Port12
P130, P131 : Port13
PCL : Programmable Clock
$\overline{RD}$: Read Strobe
$\overline{RESET}$: Reset
RTP0 to RTP7 : Real-Time Output Port
$\overline{RX}$: Receive Data (IEBus Controller)
RxD : Receive Data (UART)
SB0, SB1 : Serial Bus
$\overline{SCK0}$ to $\overline{SCK2}$: Serial Clock
SI0 to SI2 : Serial Input
SO0 to SO2 : Serial Output
STB : Strobe
TI00, TI01 : Timer Input
TI1, TI2 : Timer Input
TO0 to TO2 : Timer Output
$\overline{TX}$: Transmit Data (IEBus Controller)
TxD : Transmit Data (UART)
V_{DD} : Power Supply
V_{PP} : Programming Power Supply
V_{SS} : Ground
$\overline{WAIT}$: Wait
$\overline{WR}$: Write Strobe
X1, X2 : Crystal (Main System Clock)
XT1, XT2 : Crystal (Subsystem Clock)

(2) PROM programming mode

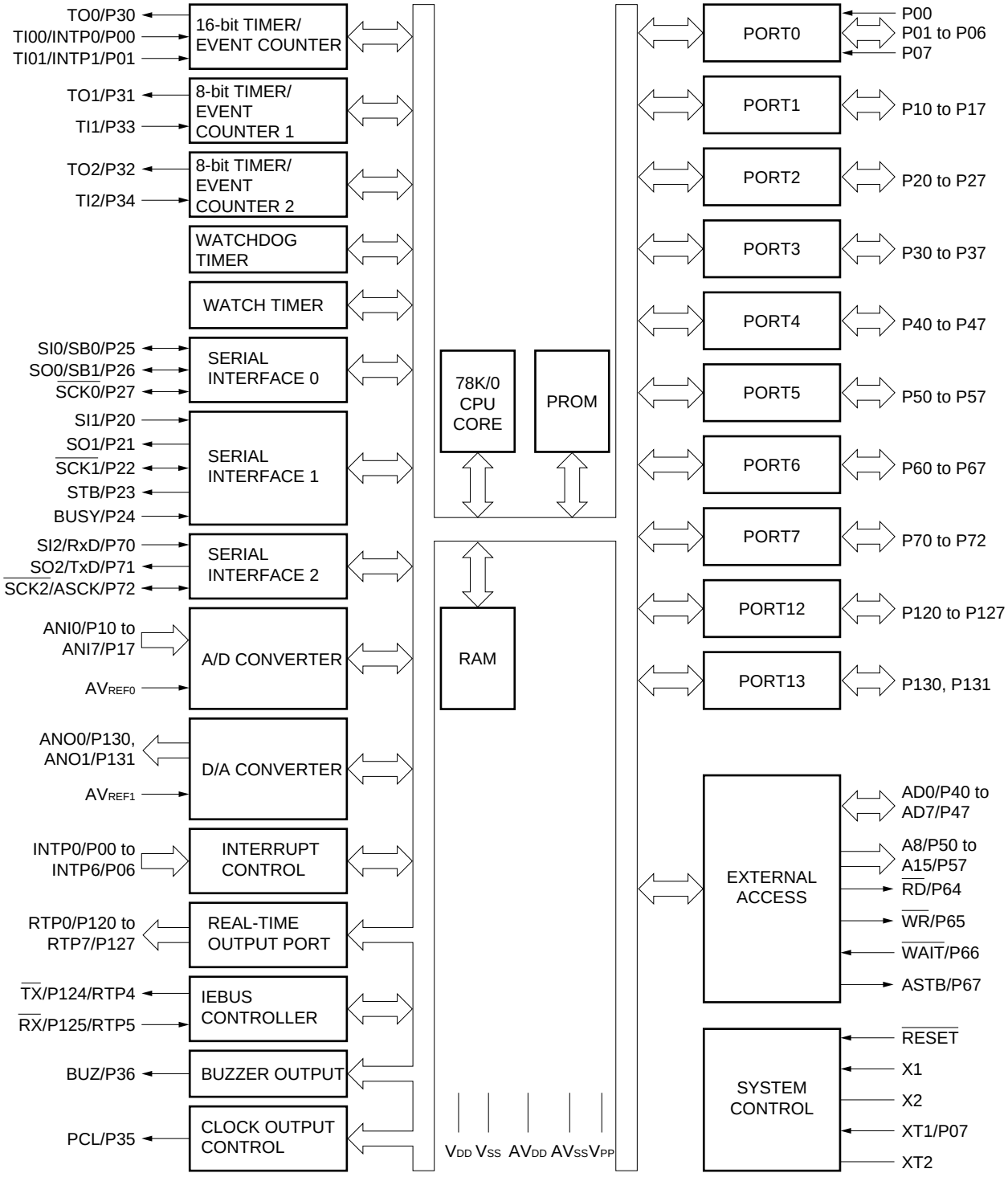
- **80-pin plastic QFP (14 × 14 mm)**
  μPD78P098BGC-3B9



Cautions 1. (L) : Individually connect to V_{SS} via a pull-down resistor.
2. V_{SS} : Connect to ground.
3. $\overline{RESET}$: Keep at low level.
4. Open : Leave open.

A0 to A16	:	Address Bus	$\overline{RESET}$	:	Reset
$\overline{CE}$	:	Chip Enable	V_{DD}	:	Power Supply
D0 to D7	:	Data Bus	V_{PP}	:	Programming Power Supply
$\overline{OE}$	:	Output Enable	V_{SS}	:	Ground
$\overline{PGM}$	:	Program			

BLOCK DIAGRAM



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1. DIFFERENCES BETWEEN μPD78P098B AND MASK ROM VERSIONS

The μPD78P098B is provided with a one-time PROM to which a program can be written only once.

The functions of the μPD78P098B, except the PROM specification and the mask option of pins P60 through P63, can be set to be the same as those of the mask ROM version by using the internal memory size switching register and internal expansion RAM size switching register.

Table 1-1 shows the differences between the μPD78P098B and mask ROM versions.

Table 1-1. Differences between μPD78P098B and Mask ROM Versions

Item	μPD78P098B	Mask ROM Versions
Internal ROM structure	One-time PROM	Mask ROM
Internal ROM capacity	60 Kbytes	μPD78095B : 40 Kbytes μPD78096B : 48 Kbytes μPD78098B : 60 Kbytes
Internal expansion RAM capacity	2048 bytes	μPD78095B, 78096B : none μPD78098B : 2048 bytes
Change internal ROM capacity by internal memory size switching register (IMS)	Available Note 1	Not available Note 2
Change internal expansion RAM capacity with the internal expansion RAM size switching register (IXS)	Available Note 3	Not available
IC pin	Not provided	Provided
V_{PP} pin	Provided	Not provided
On-chip pull-up resistor mask option for P60 to P63	Not provided	Provided
Electrical specifications, recommended soldering conditions	Refer to the data sheet for each product	

Notes 1. Internal PROM capacity is 60 Kbytes after $\overline{\text{RESET}}$ input.
2. Except when using external device expansion function with the μPD78098B.
3. Internal expansion RAM capacity is 2048 bytes after $\overline{\text{RESET}}$ input.

Caution There are differences in noise immunity and noise radiation between the PROM versions and mask ROM versions. When pre-producing an application set with the PROM version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the set using consumer samples (not engineering samples) of the mask ROM versions.

Remark The internal expansion RAM size switching register (IXS) is only incorporated in the μPD78098B and 78P098B.

2. PIN FUNCTIONS

2.1 Pins in Normal Operation Mode

(1) Port pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P00	Input	Port 0.	Input only	Input	INTP0/TI00
P01	I/O	8-bit I/O port.	Input/output can be specified in 1-bit units. When using as an input port, an on-chip pull-up resistor can be connected by means of software.	Input	INTP0/TI00
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P06					INTP6
P07 Note 1	Input		Input only	Input	XT1
P10 to P17	I/O	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. When using as an input port, an on-chip pull-up resistor can be connected by means of software. Note 2		Input	ANI0 to ANI7
P20	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units. When using as an input port, an on-chip pull-up resistor can be connected by means of software. Note 2		Input	SI1
P21					SO1
P22					$\overline{\text{SCK1}}$
P23					STB
P24					BUSY
P25					SI0/SB0
P26					SO0/SB1
P27					$\overline{\text{SCK0}}$
P30	I/O	Port 3. 8-bit I/O port. Input/output can be specified in 1-bit units. When using as an input port, an on-chip pull-up resistor can be connected by means of software. Note 2		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					–

Notes 1. When using the P07/XT1 pin as an input port, set bit 6 (FRC) of the processor clock control register (PCC) to 1. Do not use the feedback resistor of the subsystem clock oscillator.

2. When using the P10/AN10 to P17/AN17 pins as the analog inputs of the A/D converter, on-chip pull-up resistors are automatically unconnected.

(1) Port pins (2/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P40 to P47	I/O	Port 4. 8-bit I/O port. Input/output can be specified in 8-bit units. When using as an input port, an on-chip pull-up resistor can be connected by means of software. Test input flag (KRIF) is set to 1 when detecting the falling edge.		Input	AD0 to AD7
P50 to P57	I/O	Port 5. 8-bit I/O port. Can directly drive LEDs. Input/output can be specified in 1-bit units. When using as an input port, an on-chip pull-up resistor can be connected by means of software.		Input	A8 to A15
P60	I/O	Port 6. 8-bit I/O port. Input/output can be specified in 1-bit units.	N-ch open-drain I/O port. Can directly drive LEDs.	Input	–
P61					
P62					
P63					
P64			When using as an input port, an on-chip pull-up resistor can be connected by means of software.	Input	$\overline{RD}$
P65					$\overline{WR}$
P66					$\overline{WAIT}$
P67					ASTB
P70	I/O	Port 7. 3-bit I/O port. Input/output can be specified in 1-bit units. When using as an input port, an on-chip pull-up resistor can be connected by means of software.		Input	SI2/RxD
P71					SO2/TxD
P72					$\overline{SCK2}$/ASCK
P120 to P123	I/O	Port 12. 8-bit I/O port. Input/output can be specified in 1-bit units. When using as an input port, an on-chip pull-up resistor can be connected by means of software.		Input	RTP0 to RTP3
P124					RTP4/$\overline{TX}$
P125					RTP5/$\overline{RX}$
P126, P127					RTP6, RTP7
P130, P131	I/O	Port 13. 2-bit I/O port. Input/output can be specified in 1-bit units. When using as an input port, an on-chip pull-up resistor can be connected by means of software.		Input	ANO0, ANO1

Caution For pins that also function as port pins, do not perform the following operations during A/D conversion. If these operations are performed, the total error ratings cannot be kept.
(1) Rewrite the output latch whose pin is used as a port pin.
(2) Change the output level of the pin used as an output pin, even if it is not used as a port pin.

(2) Non-port pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input for which the effective edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
INTP6				P06
SI0	Input	Serial interface serial data input.	Input	P25/SB0
SI1				P20
SI2				P70/RxD
SO0	Output	Serial interface serial data output.	Input	P26/SB1
SO1				P21
SO2				P71/TxD
SB0	I/O	Serial interface serial data input/output.	Input	P25/SI0
SB1				P26/SO0
$\overline{SCK0}$	I/O	Serial interface serial clock input/output.	Input	P27
$\overline{SCK1}$				P22
$\overline{SCK2}$				P72/ASCK
STB	Output	Strobe signal output for serial interface automatic transmission/reception.	Input	P23
BUSY	Input	Busy input for serial interface automatic transmission/reception.	Input	P24
RxD	Input	Serial data input for asynchronous serial interface.	Input	P70/SI2
TxD	Output	Serial data output for asynchronous serial interface.	Input	P71/SO2
ASCK	Input	Serial clock input for asynchronous serial interface.	Input	P72/$\overline{SCK2}$
TI00	Input	External count clock input to 16-bit timer (TM0).	Input	P00/INTP0
TI01		Capture trigger signal input to capture register (CR00).		P01/INTP1
TI1		External count clock input to 8-bit timer (TM1).		P33
TI2		External count clock input to 8-bit timer (TM2).		P34
TO0	Output	16-bit timer (TM0) output (shared with 14-bit PWM output).	Input	P30
TO1		8-bit timer (TM1) output.		P31
TO2		8-bit timer (TM2) output.		P32
PCL	Output	Clock output (for trimming of main system clock and subsystem clock)	Input	P35
BUZ	Output	Buzzer output	Input	P36
RTP0 to RTP3	Output	Real-time output port outputting data in synchronization with trigger.	Input	P120 to P123
RTP4				P124/$\overline{TX}$
RTP5				P125/$\overline{RX}$
RTP6, RTP7				P126, P127
$\overline{TX}$	Output	Data output for IEBus controller.	Input	P124/RTP4
$\overline{RX}$	Input	Data input for IEBus controller.	Input	P125/RTP5

(2) Non-port pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
AD0 to AD7	I/O	Low-order address/data bus when external memory is connected.	Input	P40 to P47
A8 to A15	Output	High-order address bus when external memory is connected.	Input	P50 to P57
$\overline{RD}$	Output	Strobe signal output for read operation on external memory.	Input	P64
$\overline{WR}$		Strobe signal output for write operation on external memory.	Input	P65
$\overline{WAIT}$	Input	Wait state insertion for external memory access.	Input	P66
ASTB	Output	Strobe output to externally latch address information output to ports 4 and 5 to access external memory.	Input	P67
ANI0 to ANI7	Input	Analog input of A/D converter.	Input	P10 to P17
ANO0, ANO1	Output	Analog output of D/A converter.	Input	P130, P131
AV_{REF0}	Input	Reference voltage input of A/D converter.	–	–
AV_{REF1}	Input	Reference voltage input of D/A converter.	–	–
AV_{DD}	–	Analog power supply of A/D converter. (alternate function : port power supply).	–	–
AV_{SS}	–	Ground potential of A/D converter and D/A converter. (alternate function : port ground potential)	–	–
$\overline{RESET}$	Input	System reset input.	–	–
X1	Input	Crystal resonator connection for main system clock oscillation.	–	–
X2	–		–	–
XT1	Input	Crystal resonator connection for subsystem clock oscillation.	Input	P07
XT2	–		–	–
V_{DD}	–	Positive power supply (except for ports and analog units).	–	–
V_{PP}	–	High-voltage application for program write/verify. Connect to V_{SS} directly in normal operation mode.	–	–
V_{SS}	–	Ground (except for ports and analog units).	–	–

Cautions 1. The AV_{DD} pin functions as both an A/D converter power supply and a port power supply. When the μPD78P098B is used in applications where the noise generated inside the microcontroller needs to be reduced, connect the AV_{DD} pin to another power supply that has the same potential as V_{DD}.

2. The AV_{SS} pin functions both as a ground of the A/D and D/A converters and as a ground of a port. When the μPD78P098B is used in applications where the noise generated inside the microcontroller needs to be reduced, connect the AV_{SS} pin to a ground line other than V_{SS}.

2.2 Pins in PROM Programming Mode

Pin Name	I/O	Function
$\overline{\text{RESET}}$	Input	PROM programming mode setting. When +5 V or +12.5 V is applied to the V_{PP} pin, and low level is applied to the $\overline{\text{RESET}}$ pin, PROM programming mode is set.
V_{PP}	Input	PROM programming mode setting and high-voltage application for program write/verify.
A0 to A16	Input	Address bus.
D0 to D7	I/O	Data bus.
$\overline{\text{CE}}$	Input	PROM enable input/program pulse input.
$\overline{\text{OE}}$	Input	Read strobe input to PROM.
$\overline{\text{PGM}}$	Input	Program/program inhibit input in PROM programming mode.
V_{DD}	–	Positive power supply.
V_{SS}	–	Ground.

2.3 Pin I/O Circuits and Connection of Unused Pins

Table 2-1 shows the types of I/O circuits for the various pins and the connection of unused pins.

For the configuration of the various I/O circuits, refer to Figure 2-1.

Table 2-1. I/O Circuit Type of Each Pin (1/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection When Not Used
P00/INTP0/TI00	2	Input	Connect to V_{SS}.
P01/INTP1/TI01	8-D	I/O	Individually connect to V_{SS} via a resistor.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P06/INTP6			
P07/XT1	16	Input	Connect to V_{DD} or V_{SS}.
P10/ANI0 to P17/ANI7	11-C	I/O	Individually connect to V_{DD} or V_{SS} via a resistor.
P20/SI1	8-D		
P21/SO1	5-J		
P22/$\overline{\text{SCK1}}$	8-D		
P23/STB	5-J		
P24/BUSY	8-D		
P25/SI0/SB0	10-C		
P26/SO0/SB1			
P27/$\overline{\text{SCK0}}$			
P30/TO0	5-J		
P31/TO1			
P32/TO2			
P33/TI1	8-D		
P34/TI2			

Table 2-1. I/O Circuit Type of Each Pin (2/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connection When Not Used
P35/PCL	5-J	I/O	Individually connect to V_{DD} or V_{SS} via a resistor.
P36/BUZ			
P37			
P40/AD0 to P47/AD7	5-O		Individually connect to V_{DD} via a resistor.
P50/A8 to P57/A15	5-J		Individually connect to V_{DD} or V_{SS} via a resistor.
P60 to P63	13-H		Individually connect to V_{DD} via a resistor.
P64/$\overline{RD}$	5-J		Individually connect to V_{DD} or V_{SS} via a resistor.
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
P70/SI2/RxD	8-D		
P71/SO2/TxD	5-J		
P72/$\overline{SCK2}$/ASCK	8-D		
P120/RTP0 to P123/RTP3	5-J		
P124/RTP4/$\overline{TX}$			
P125/RTP5/$\overline{RX}$			
P126/RTP6, P127/RTP7			
P130/ANO0, P131/ANO1	12-B		Individually connect to V_{SS} via a resistor.
$\overline{RESET}$	2	Input	–
XT2	16	–	Leave open
AV_{REF0}	–		Connect to V_{SS}.
AV_{REF1}			Connect to V_{DD}.
AV_{DD}			Connect to another power supply of the same potential as V_{DD}.
AV_{SS}			Connect to another ground of the same potential as V_{SS}.
V_{PP}			Directly connect to V_{SS}.

Figure 2-1. I/O Circuits of Pins (1/2)

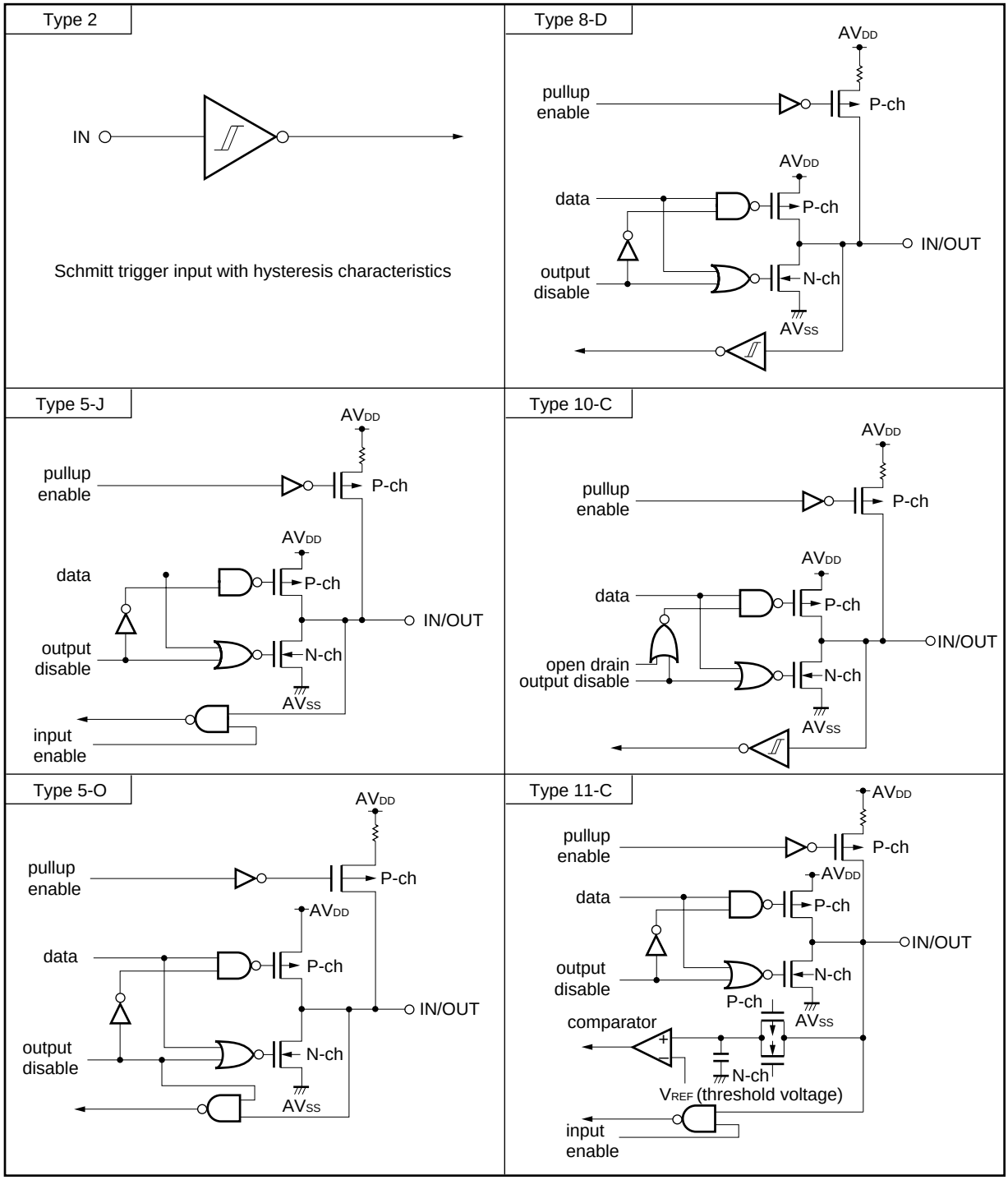
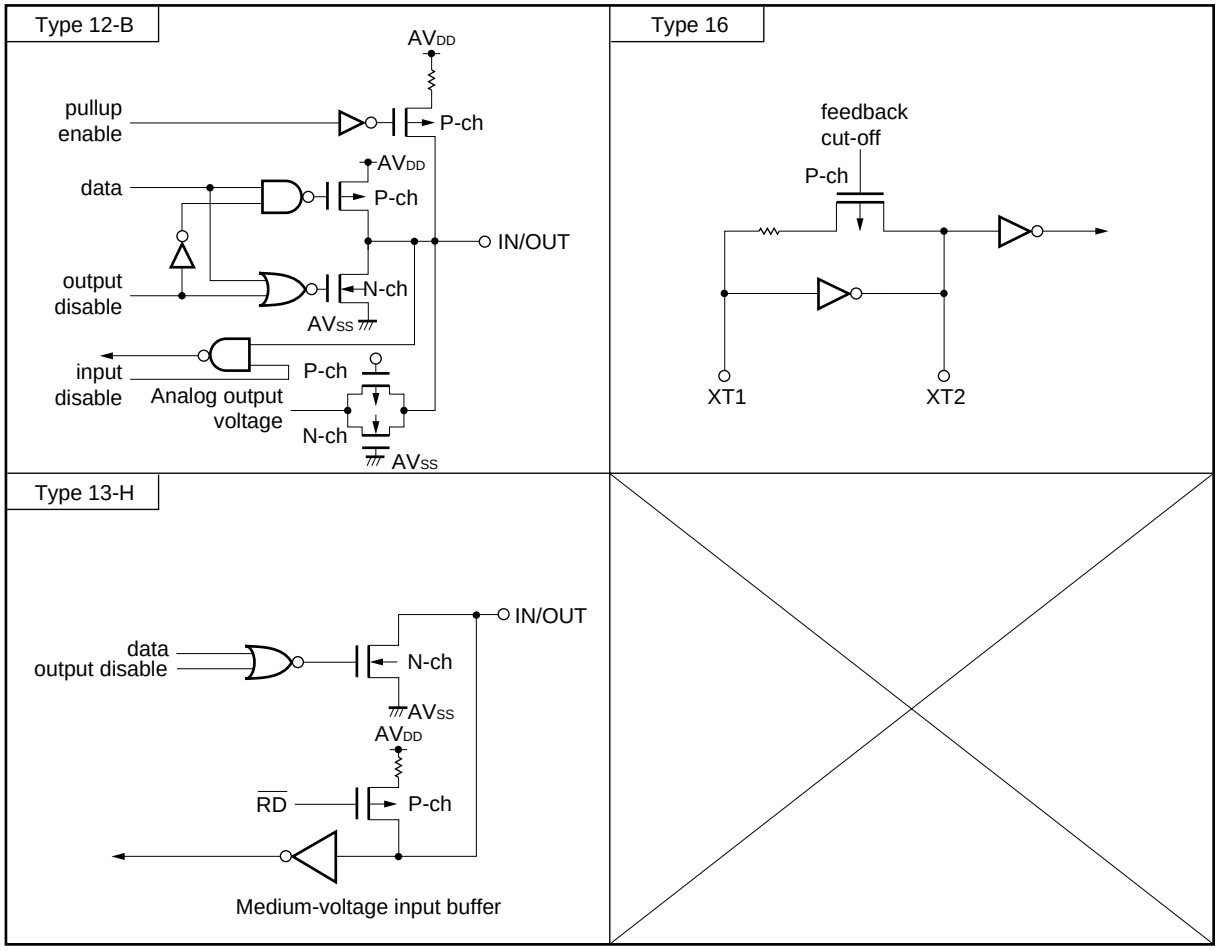


Figure 2-1. I/O Circuits of Pins (2/2)



3. INTERNAL MEMORY SIZE SWITCHING REGISTER (IMS)

This register specifies via software the part of the internal memory that is not used. By using this register, the internal memory (ROM) of the μPD78P098B can be mapped in the same manner as that of a mask ROM version.

IMS is set by an 8-bit memory manipulation instruction.

The contents of this register are set to CFH after $\overline{\text{RESET}}$ input.

Figure 3-1. Format of the Internal Memory Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

ROM3	ROM2	ROM1	ROM0	Selects internal ROM capacity
1	0	1	0	40 Kbytes
1	1	0	0	48 Kbytes
1	1	1	0	56 Kbytes[Note]
1	1	1	1	60 Kbytes
Others				Setting prohibited

RAM2	RAM1	RAM0	Selects internal high-speed RAM capacity
1	1	0	1024 bytes
Others			Setting prohibited

Note When using the external device expansion function, set the internal PROM capacity to 56 Kbytes or less.

Table 3-1 shows the value settings of IMS to map the memory of the μPD78P098B in the same manner as that of the respective mask ROM version.

Table 3-1. Value Settings of the Internal Memory Size Switching Register

Mask ROM Version	IMS Value Setting
μPD78095B	CAH
μPD78096B	CCH
μPD78098B	CFH

4. INTERNAL EXPANSION RAM SIZE SWITCHING REGISTER (IXS)

This register specifies the internal expansion RAM capacity via software. By using this register, the internal expansion RAM of the μPD78P098B can be mapped in the same manner as that of a mask ROM model.

IXS is set by an 8-bit memory manipulation instruction.

The contents of this register are set to 08H after $\overline{\text{RESET}}$ input.

Figure 4-1. Format of Internal Expansion RAM Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
IXS	0	0	0	0	IXRAM3	IXRAM2	IXRAM1	IXRAM0	FFF4H	08H	W

IXRAM3	IXRAM2	IXRAM1	IXRAM0	Selects internal expansion RAM capacity
1	1	0	0	No internal expansion RAM
1	0	0	0	2048 bytes (F000H to F7FFH)
Others				Setting prohibited

Table 4-1 shows the value settings of IXS to map the internal expansion RAM of the μPD78P098B in the same manner as that of the respective mask ROM version.

Table 4-1. Value Settings of Internal Expansion RAM Size Switching Register

Mask ROM Version	IXS Value Setting
μPD78095B	0CH Note
μPD78096B	
μPD78098B	08H

Note Even when a program for the μPD78P098B in which “MOV IXS, #0CH” is coded is executed on the μPD78095B, 78096B, or 78098B, no operation is affected.

5. PROM PROGRAMMING

The μPD78P098B is provided with a 60-Kbyte PROM as a program memory. When programming this memory, it must be set in the PROM programming mode by using the V_{PP} and $\overline{RESET}$ pins. For connections of the unused pins, refer to **(2) PROM programming mode** in **PIN CONFIGURATION (Top View)**.

Caution Write the program to addresses in the range 0000H through EFFFH (specify the last address as EFFFH). A program cannot be written with a PROM programmer that cannot specify write addresses.

5.1 Operation Modes

When +5 V or +12.5 V is applied to the V_{PP} pin and low level is applied to the $\overline{RESET}$ pin, the PROM programming mode is set. In this mode, the operation modes shown in Table 5-1 can be selected by using the $\overline{CE}$, $\overline{OE}$, and $\overline{PGM}$ pins.

The contents of the PROM can be read in the read mode.

Table 5-1. Operation Modes in PROM Programming Mode

Pin / Operation Mode	$\overline{RESET}$	V_{PP}	V_{DD}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	D0 to D7
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				×	H	H	High impedance
				×	L	L	
Read		+5 V	+5 V	L	L	H	Data output
Output disable				L	H	×	High impedance
Standby				H	×	×	High impedance

×: L or H

(1) Read mode

This mode is set when both the $\overline{CE}$ and $\overline{OE}$ pins are made low.

(2) Output disable mode

When the $\overline{OE}$ pin is made high, data output goes into a high-impedance state, and the output disable mode is set.

If two or more μPD78P098Bs are connected to the data bus, therefore, data can be read from any one of the devices by controlling the $\overline{OE}$ pin.

(3) Standby mode

The standby mode is set when the $\overline{CE}$ pin is made high.

In this mode, data output goes into a high-impedance state regardless of the status of the $\overline{OE}$ pin.

(4) Page data latch mode

The page data latch mode is set when the $\overline{CE}$ and $\overline{PGM}$ pins are made high and the $\overline{OE}$ pin is made low at the beginning of the page write mode.

In this mode, data of 1 page and 4 bytes is latched to the on-chip address/data latch circuit.

(5) Page write mode

Page write is executed by applying a 0.1-ms program pulse (active low) to the $\overline{PGM}$ pin with the $\overline{CE}$ and $\overline{OE}$ pins made high after addresses and data of 1 page and 4 bytes have been latched in the page data latch mode. After that, the program can be verified by making both the $\overline{CE}$ and $\overline{OE}$ pins low.

If the program cannot be written by one program pulse, writing and verifying are repeated X times ($X \leq 10$).

(6) Byte write mode

Byte write is executed by applying a 0.1-ms program pulse (active low) to the $\overline{PGM}$ pin with the $\overline{CE}$ pin made low and $\overline{OE}$ pin high. The program is verified by later making the $\overline{OE}$ pin low.

If the program cannot be written by one program pulse, writing and verifying are repeated X times ($X \leq 10$).

(7) Program verify mode

Program verify mode is set when the $\overline{CE}$ and $\overline{OE}$ pins are made low and the $\overline{PGM}$ pin is made high.

After writing the program, check in this mode whether the program has been correctly written.

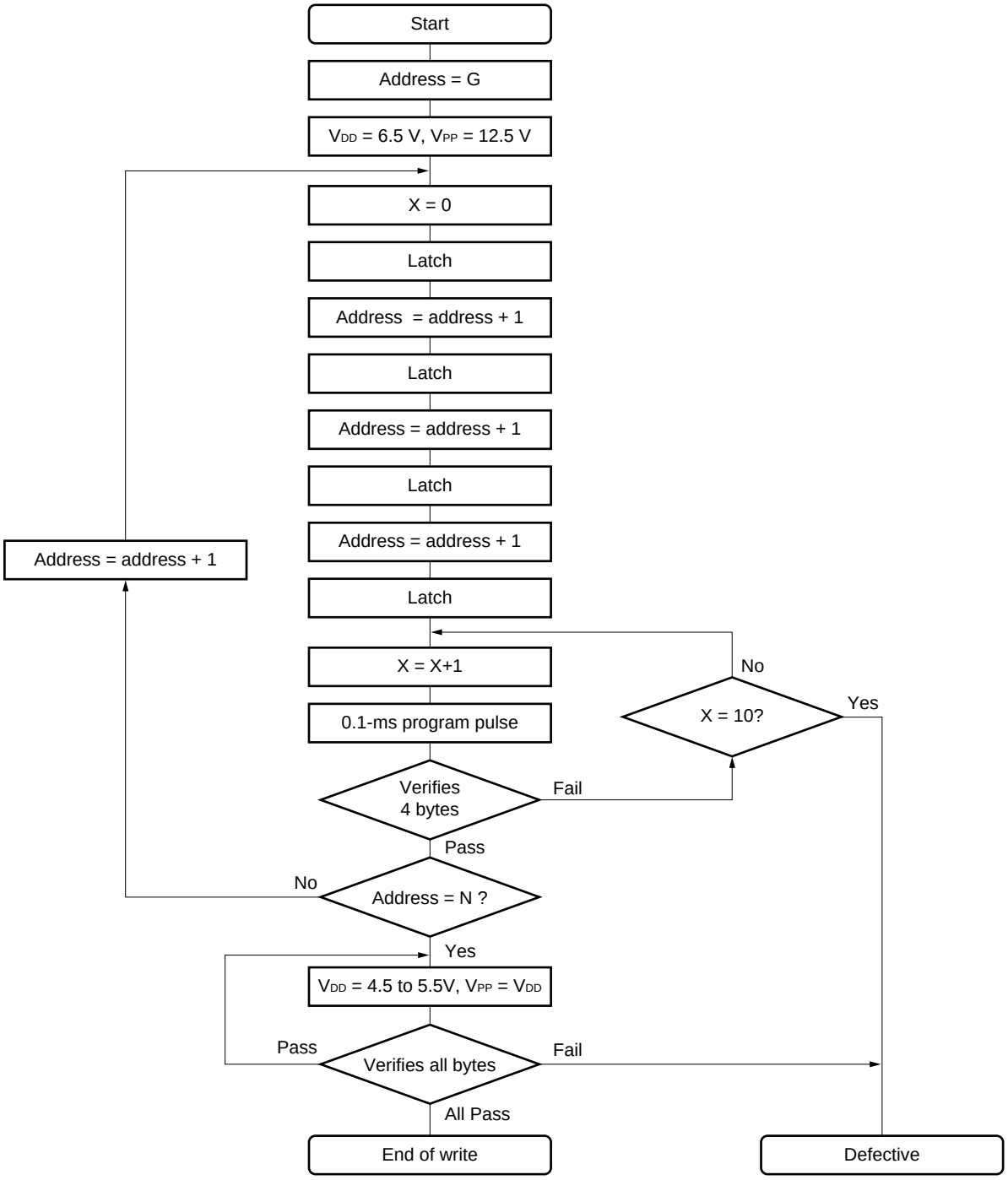
(8) Program inhibit mode

This mode is used to write a program to one of two or more μPD78P098Bs with the $\overline{OE}$, V_{PP}, and D0 through D7 pins connected in parallel.

To write a program, the page write or byte write mode described above is used. At this time, the program is not written to those devices whose $\overline{PGM}$ pin is made high.

5.2 PROM Write Procedure

Figure 5-1. Page Program Mode Flowchart



G = start address

N = end address of program

Figure 5-2. Page Program Mode Timing

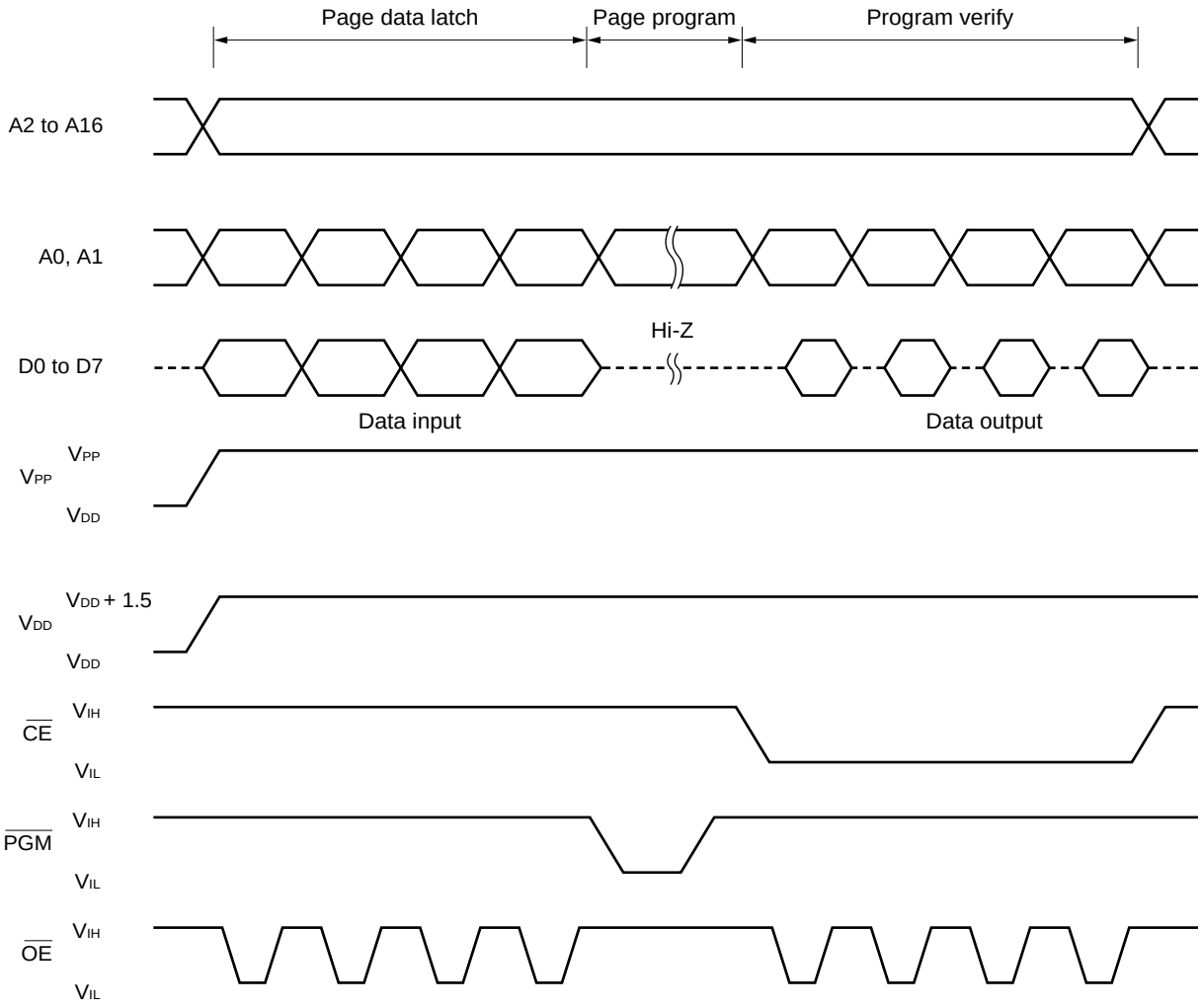
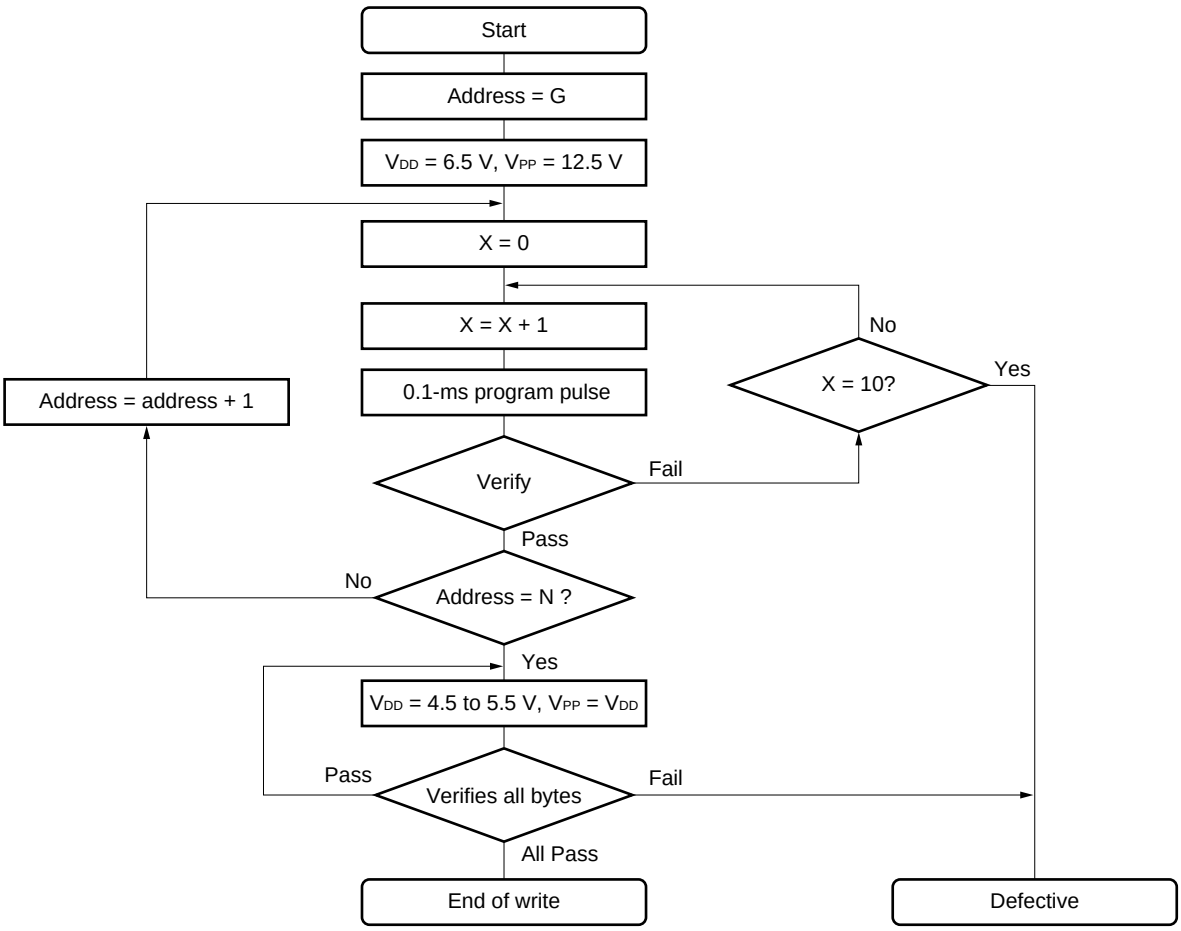


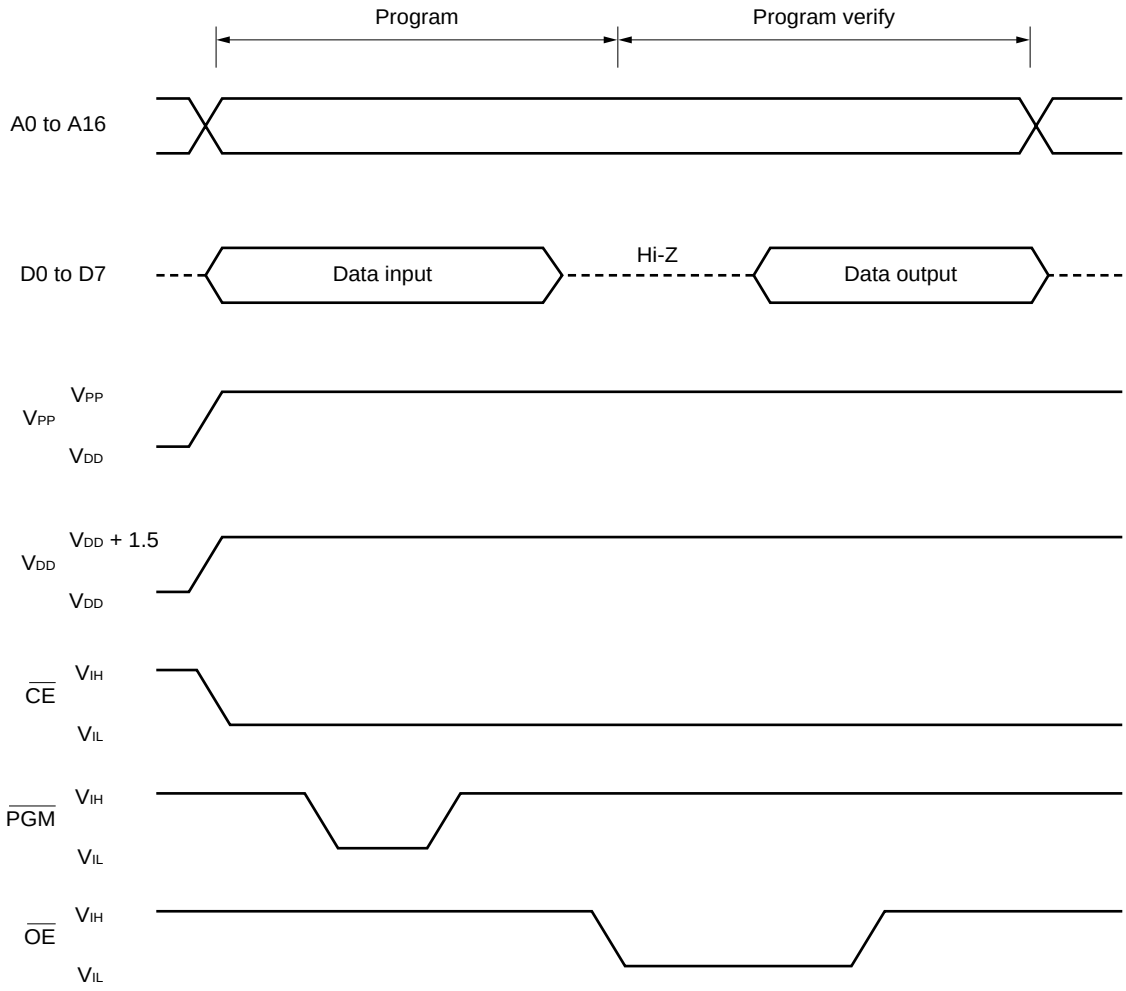
Figure 5-3. Byte Program Mode Flowchart



G = start address

N = end address of program

Figure 5-4. Byte Program Mode Timing



Cautions 1. Apply V_{DD} before V_{PP} and turn off V_{DD} after V_{PP}.

2. Keep V_{PP} from going above +13.5 V, including overshoot.

3. If the device is inserted into or pulled out of the socket while +12.5 V is applied to V_{PP}, the reliability may be adversely affected.

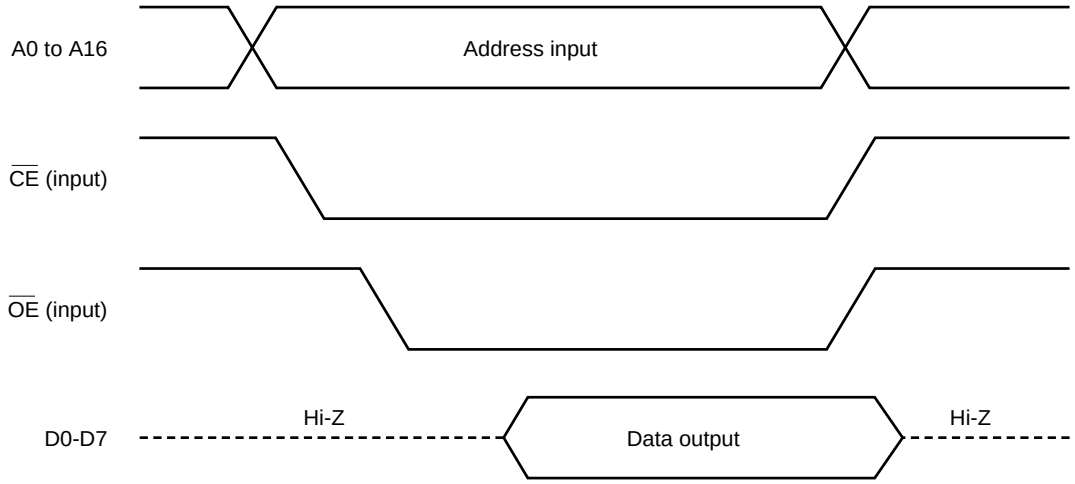
5.3 PROM Read Procedure

The contents of the PROM can be read out to the external data bus (D0 through D7) with the following procedure:

(1) Fix the $\overline{\text{RESET}}$ pin to the low level. Supply +5 V to the V_{PP} pin. Connect the unused pins as described in **(2) PROM programming mode** in **PIN CONFIGURATION (Top View)**.
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) Input the address of the data to be read to the A0 through A16 pins.
(4) The read mode is set.
(5) Data is output to the D0 through D7 pins.

Figure 5-5 shows the timing of steps (2) through (5) above.

Figure 5-5. PROM Read Timing



6. SCREENING OF ONE-TIME PROM VERSION

The one-time PROM version (μPD78P098BGC-3B9) cannot be completely tested by NEC before shipment. It is recommended that screening be implemented to verify the PROM after data has been written to the PROM and the device has been stored under the following conditions:

Storage Temperature	Storage Time
125°C	24 hours

NEC provides a writing, marking, screening, and verifying service for one-time PROMs, called QTOP microcontroller. This service for the μPD78P098B is in preparation. For details, consult NEC.

7. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

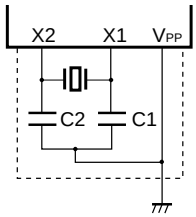
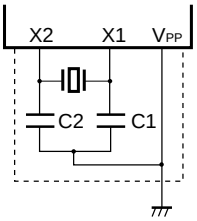
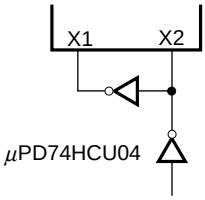
Parameter	Symbol	Test Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to + 7.0	V
	V_{PP}			–0.3 to +13.5	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{REF0}			–0.3 to V_{DD} + 0.3	V
	AV_{REF1}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to 47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131, X1, X2, XT2, $\overline{\text{RESET}}$		–0.3 to V_{DD} +0.3	V
	V_{I2}	P60 to P63	N-ch open drain	–0.3 to +16	V
	V_{I3}	A9	PROM programming mode	–0.3 to +13.5	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pins	AV_{SS} – 0.3 to AV_{REF0} + 0.3	V
Output current high	I_{OH}	1 pin		–10	mA
		Total for P01 to P06, P30 to P37, P56, P57, P60 to P67, P120 to P127		–15	mA
		Total for P10 to P17, P20 to P27, P40 to P47, P50 to P55, P70 to P72, P130, P131		–15	mA
Output current low	I_{OL} Note	1 pin	Peak value	30	mA
			r.m.s. value	15	mA
		Total for P50 to P55	Peak value	100	mA
			r.m.s. value	70	mA
		Total for P56, P57, P60 to P63	Peak value	100	mA
			r.m.s. value	70	mA
		Total for P10 to P17, P20 to P27, P40 to P47, P70 to P72, P130, P131	Peak value	50	mA
			r.m.s. value	20	mA
		Total for P01 to P06, P30 to P37, P64 to P67, P120 to P127	Peak value	50	mA
			r.m.s	20	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C
Total power dissipation	P_d			650	mW

Note The r.m.s. (root mean square) value should be calculated as follows: [r.m.s. value] = [Peak value] x $\sqrt{\text{Duty}}$

Caution **Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter, or even momentarily. In other words, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.**

Remark Unless otherwise specified, alternate function characteristics are the same as port pin characteristics.

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X) Note 1	V_{DD} = Oscillation voltage range	1.0	6.0	6.29	MHz
		Oscillation stabilization time Note 2	After V_{DD} has reached MIN. of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f_X) Note 1		1.0	6.0	6.29	MHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X) Note 1		1.0	6.0	6.29	MHz
		X1 input high-/low-level width (t_{XH}/t_{XL})	When $f_{XX} = f_X$	85		500	ns
			Other than above	72		500	ns

Notes 1. Only the oscillator characteristics are shown. See the AC characteristics for instruction execution times.

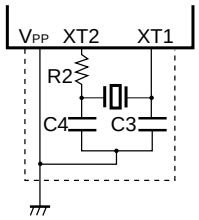
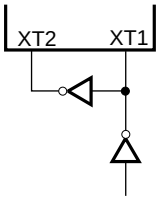
2. This is the time required for oscillation to stabilize after a reset or STOP mode release.

Cautions 1. When the main system clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a broken line to prevent the influence of wiring capacitance, etc.

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as V_{SS}.**
- **Do not connect to a ground pattern carrying a high current.**
- **No signals should be extracted from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT}) Note 1		32	32.768	35	MHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	
External clock		X1 input frequency (f_{XT}) Note 1		32		100	kHz
		X1 input high-/low-level width (t_{XTH}/t_{XTL})		5		15	μs

Notes 1. Only the oscillator characteristics are shown. See the AC characteristics for instruction execution times.

2. This is the time required for oscillation to stabilize after power (V_{DD}) is turned on.

Cautions 1. When the subsystem clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a broken line to prevent the influence of wiring capacitance, etc.

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as V_{SS}.**
- **Do not connect to a ground pattern carrying a high current.**
- **No signals should be extracted from the oscillator.**

2. The subsystem clock oscillator is a low-amplitude circuit in order to achieve a low consumption current, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

CAPACITANCE (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
Input/output capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V.	P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131			15	pF
			P60 to P63			20	pF

Remark Unless otherwise specified, alternate function characteristics are the same as port pin characteristics.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	P60 to P63, N-ch open drain		0.7V_{DD}		15	V
	V_{IH4}	X1, X2		V_{DD} – 0.5		V_{DD}	V
	V_{IH5}	XT1/P07, XT2	4.5 V ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0.9V_{DD}		V_{DD}	V
Input voltage low	V_{IL1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131		0		0.3V_{DD}	V
	V_{IL2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL3}	P60 to P63, N-ch open drain	4.5 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0		0.2V_{DD}	V
	V_{IL4}	X1, X2		0		0.4	V
	V_{IL5}	XT1/P07, XT2	V_{DD} = 4.5 to 5.5 V	0		0.2V_{DD}	V
				0		0.1V_{DD}	V
Output voltage high	V_{OH1}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD} – 1.0			V
		I_{OH} = –100 μA		V_{DD} – 0.5			V
Output voltage low	V_{OL1}	P50 to P57, P60 to P63	V_{DD} = 4.5 to 5.5 V, I_{OL} = 15 mA		0.4	2.0	V
		P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P70 to P72, P120 to P127, P130, P131	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V_{DD} = 4.5 to 5.5 V, Open drain, when pullded up (R = 1 kΩ)			0.2V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V

Remark Unless otherwise specified, alternate function characteristics are the same as port pin characteristics.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P72, P120 to P127, P130, P131, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2, XT1/P07, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P60 to P63			80	μA
Input leakage current low	I_{LIL1}	V_{IN} = 0 V	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P72, P120 to P127, P130, P131, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2, XT1/P07, XT2			–20	μA
	I_{LIL3}		P60 to P63			–3 Note	μA
Output leakage current high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistor	R	V_{IN} = 0 V, P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131	4.5 ≤ V_{DD} ≤ 5.5 V	15	40	90	kΩ
			2.7 ≤ V_{DD} ≤ 4.5 V	20		500	kΩ

Note For P60 to P63, a low-level input leak current of –200 μA (MAX.) flows only during the 1.5 clocks (no-wait time) after an instruction has been executed to read out port 6 (P6) or port mode register 6 (PM6). Outside the period of 1.5 clocks following execution a read-out instruction, the current is –3 μA (MAX.).

Remark Unless otherwise specified, alternate function characteristics are the same as port pin characteristics.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	5.0-MHz crystal oscillation operating mode (f_{XX} = 2.5 MHz) Note 2	V_{DD} = 5.0 V ±10% Note 6		5	15	mA
			V_{DD} = 3.0 V ±10% Note 7		0.7	2.7	mA
		5.0-MHz crystal oscillation operating mode (f_{XX} = 5.0 MHz) Note 3	V_{DD} = 5.0 V ±10% Note 6		9	30	mA
			V_{DD} = 3.0 V ±10% Note 7		1	3.7	mA
		6.29-MHz crystal oscillation operating mode (f_{XX} = 2.1 MHz) Note 4	V_{DD} = 5.0 V ±10% Note 6		4.8	17.4	mA
		6.29-MHz crystal oscillation operating mode (f_{XX} = 4.19 MHz) Note 5	V_{DD} = 5.0 V ±10% Note 6		8.5	28.5	mA

Notes 1. Current flow in V_{DD} and AV_{DD} pins. However this does not include current flow in the A/D converter, D/A converter, and an on-chip pull-up resistor.

2. When bit 0 (IECL10) of clock switching select register 1 (IECL1) is set to 0, bit 0 (IECL20) of clock switching select register 2 (IECL2) is set to 0, and oscillator mode select register (OSMS) is set to 00H.

3. When IECL10 is set to 0, IECL20 to 0, and OSMS is set to 01H.

4. When IECL10 is set to 1, IECL20 to 0, and OSMS is set to 00H. Expresses only power supply characteristics. For IEBus standards refer to the IEBus controller characteristics.

5. When IECL10 is set to 1, IECL20 to 0, and OSMS is set to 01H. Expresses only power supply characteristics. For IEBus standards refer to the IEBus controller characteristics.

6. During high-speed operation (when the processor clock control register (PCC) is set to 00H).

7. During low-speed operation (when PCC is set to 04H).

Remark f_{XX}: Main system clock frequency

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2}	5.0-MHz crystal oscillation HALT mode (f_{XX} = 2.5 MHz) Note 2	V_{DD} = 5.0 V ±10% Note 7		1.5	4.5	mA
			V_{DD} = 3.0 V ±10% Note 8		0.5	1.5	mA
		5.0-MHz crystal oscillation HALT mode (f_{XX} = 5.0 MHz) Note 3	V_{DD} = 5.0 V ±10% Note 7		1.8	5.4	mA
			V_{DD} = 3.0 V ±10% Note 8		0.7	2.1	mA
		6.29-MHz crystal oscillation HALT mode (f_{XX} = 2.1 MHz) Note 4	V_{DD} = 5.0 V ±10% Note 7		1.5	4.5	mA
		6.29-MHz crystal oscillation HALT mode (f_{XX} = 4.19 MHz) Note 5	V_{DD} = 5.0 V ±10% Note 7		1.8	5.4	mA
	I_{DD3}	32.768-kHz crystal oscillation operating mode Note 6	V_{DD} = 5.0 V ±10%		135	270	μA
			V_{DD} = 3.0 V ±10%		95	190	μA
	I_{DD4}	32.768-kHz crystal oscillation HALT mode Note 6	V_{DD} = 5.0 V ±10%		25	55	μA
			V_{DD} = 3.0 V ±10%		5	15	μA
	I_{DD5}	XT1 = 0 V STOP mode Feedback resistor used	V_{DD} = 5.0 V ±10%		1	30	μA
			V_{DD} = 3.0 V ±10%		0.5	10	μA
	I_{DD6}	XT1 = 0 V STOP mode Feedback resistor not used	V_{DD} = 5.0 V ±10%		0.1	30	μA
			V_{DD} = 3.0 V ±10%		0.05	10	μA

Notes 1. Current flow in V_{DD} and AV_{DD} pins. However this does not include current flow in the A/D converter, D/A converter, and an on-chip pull-up resistor.

2. When bit 0 (IECL10) of clock switching select register 1 (IECL1) is set to 0, bit 0 (IECL20) of clock switching select register 2 (IECL2) is set to 0, and oscillator mode select register (OSMS) is set to 00H.

3. When IECL10 is set to 0, IECL20 to 0, and OSMS is set to 01H.

4. When IECL10 is set to 1, IECL20 to 0, and OSMS is set to 00H.
Expresses only power supply characteristics. For IEBus standards refer to the IEBus controller characteristics.

5. When IECL10 is set to 1, IECL20 to 0, and OSMS is set to 01H.
Expresses only power supply characteristics. For IEBus standards refer to the IEBus controller characteristics.

6. When main system clock is stopped.

7. During high-speed operation (when the processor clock control register (PCC) is set to 00H).

8. During low-speed operation (when PCC is set to 04H).

Remark f_{XX} : Main system clock frequency

AC CHARACTERISTICS

(1) Basic Operation (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions			MIN.	TYP.	MAX.	Unit
Cycle time (Minimum instruction execution time)	T_{CY}	Operates with main system clock (MCS = 0 Note 1, fx = 6.29 MHz)	$f_{XX} = f_X/2$	V_{DD} = 4.0 to 5.5 V	0.64		64	μs
					1.27		64	μs
			$f_{XX} = f_X/3$	V_{DD} = 4.0 to 5.5 V	0.95		64	μs
					1.91		64	μs
			$f_{XX} = f_X/6$		1.91		64	μs
			$f_{XX} = f_X/9$		2.86		64	μs
		Operates with main system clock (MCS = 1 Note 2, fx = 6.29 MHz)	$f_{XX} = f_X$	V_{DD} = 4.0 to 5.5 V	0.64		32	μs
					1.27		32	μs
			$f_{XX} = 2f_X/3$	V_{DD} = 4.0 to 5.5 V	0.48		32	μs
					1.91		32	μs
			$f_{XX} = f_X/3$		1.91		32	μs
			$f_{XX} = 2f_X/9$		1.43		32	μs
		Operates with subsystem clock			40 Note 3	122	125	μs
TI00 input frequency	f_{TI00},	$f_{TI00} = t_{TH00} + t_{TIL00}$			0		$1/t_{TI00}$	MHz
TI00 input high-/low-level width	t_{TIH00}, t_{TIL00}				$8/f_{sam}$ **(Note 4)**			μs
TI01, TI1, TI2 input frequency	t_{TI1}	V_{DD} = 4.5 V to 5.5 V			0		4	MHz
					0		275	kHz
TI01, TI1, TI2 input high-/low-level width	t_{TIH1}, t_{TIL1}	V_{DD} = 4.5 V to 5.5 V			100			ns
					1.8			μs
Interrupt request input high-/low-level width	t_{INTH}, t_{INTL}	INTP0			$8/f_{sam}$ Note 4			μs
		INTP1 to INTP6			10			μs
		KR0 to KR7			10			μs
$\overline{\text{RESET}}$ INPUT high-/low-level width	t_{RST}				10			μs

Notes 1. When the oscillation mode select register (OSMS) is set to 00H.

2. When OSMS is set to 01H.

3. Value when an external clock is used. This is 114 μs (MIN.) when using the crystal resonator.

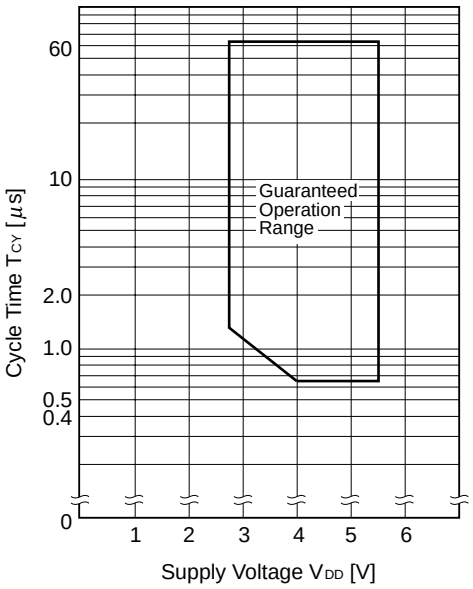
4. By setting the sampling clock select register (SCS) bits 0, 1 (SCS0, SCS1), the following settings can be specified.

$f_{sam} = fxx/2^N$, fxx/32, fxx/64, fxx/128 (N = 0 to 4).

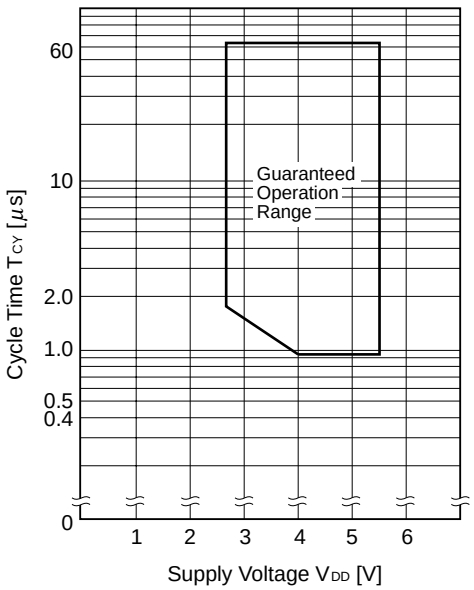
Remarks fxx : Main system clock frequency

fx : Main system clock oscillation frequency

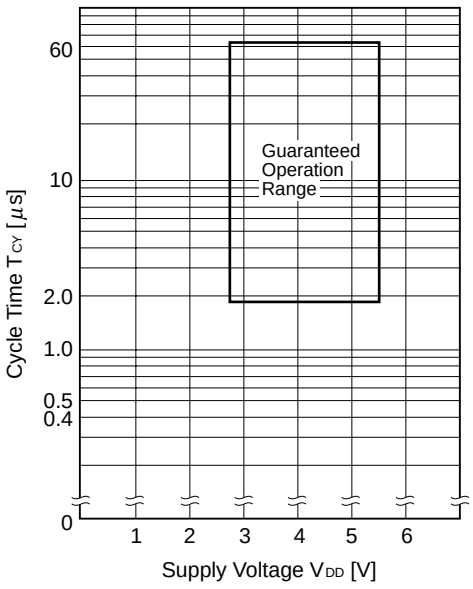
T_{CY} vs V_{DD} (Main System Clock (IECL10 = 0, IECL20 = 0, MCS = 0) Operation)



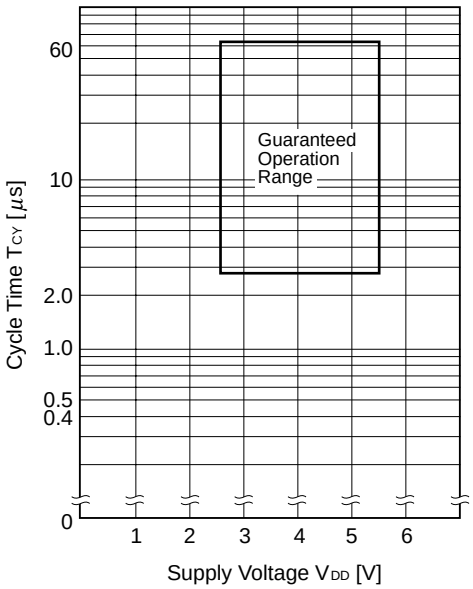
T_{CY} vs V_{DD} (Main System Clock (IECL10 = 1, IECL20 = 0, MCS = 0) Operation)



T_{CY} vs V_{DD} (Main System Clock (IECL10 = 0, IECL20 = 1, MCS = 0) Operation)

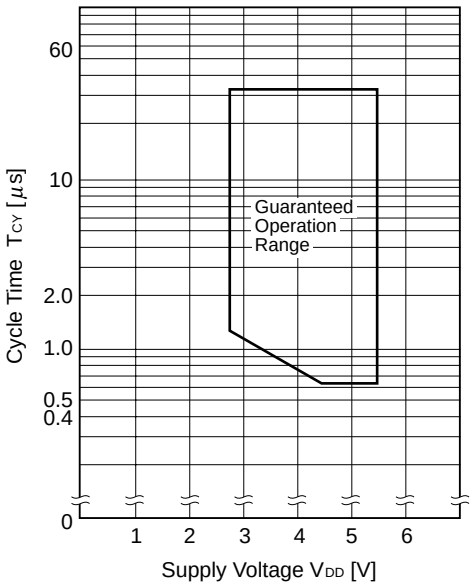


T_{CY} vs V_{DD} (Main System Clock (IECL10 = 1, IECL20 = 1, MCS = 0) Operation)

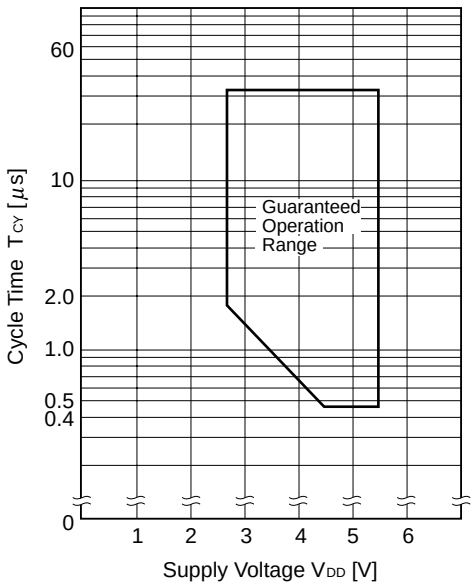


Remarks IECL10 : Bit 0 of clock switching select register 1 (IECL1)
IECL20 : Bit 0 of clock switching select register 2 (IECL2)
MCS : Bit 0 of oscillation mode select register (OSMS)

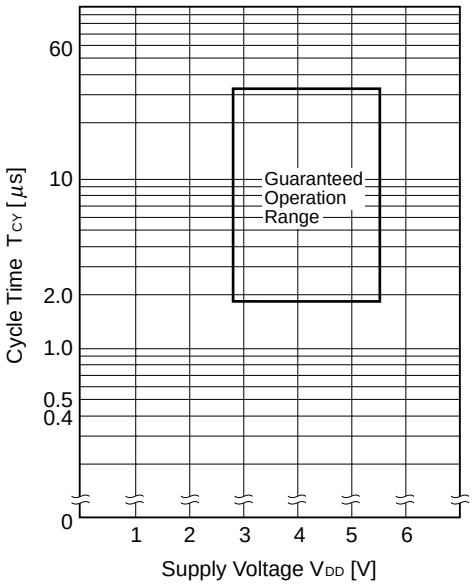
T_{CY} vs V_{DD} (Main System Clock (IECL10 = 0, IECL20 = 0, MCS = 1) Operation)



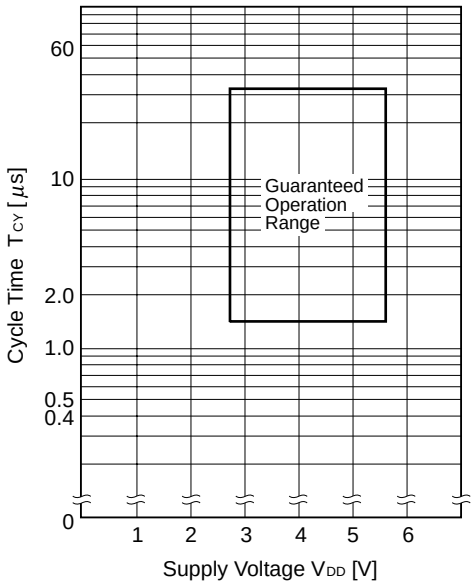
T_{CY} vs V_{DD} (Main System Clock (IECL10 = 1, IECL20 = 0, MCS = 1) Operation)



T_{CY} vs V_{DD} (Main System Clock (IECL10 = 0, IECL20 = 1, MCS = 1) Operation)



T_{CY} vs V_{DD} (Main System Clock (IECL10 = 1, IECL20 = 1, MCS = 1) Operation)



Remarks IECL10 : Bit 0 of clock switching select register 1 (IECL1)
IECL20 : Bit 0 of clock switching select register 2 (IECL2)
MCS : Bit 0 of oscillation mode select register (OSMS)

(2) Read/Write Operations

(a) When MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.85t_{CY}$ – 50		ns
Address setup time	t_{ADS}		$0.85t_{CY}$ – 50		ns
Address hold time	t_{ADH}		50		ns
Data input time from address	t_{ADD1}			$(2.85 + 2n)t_{CY}$ – 80	ns
	t_{ADD2}			$(4 + 2n)t_{CY}$ – 100	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			$(2 + 2n)t_{CY}$ – 100	ns
	t_{RDD2}			$(2.85 + 2n)t_{CY}$ – 100	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(2 + 2n)t_{CY}$ – 60		ns
	t_{RDL2}		$(2.85 + 2n)t_{CY}$ – 60		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t_{RDWT1}			$0.85t_{CY}$ – 50	ns
	t_{RDWT2}			$2t_{CY}$ – 60	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t_{WRWT}			$2t_{CY}$ – 60	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(1.15 + 2n)t_{CY}$	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		$(2.85 + 2n)t_{CY}$ – 100		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(2.85 + 2n)t_{CY}$ – 60		ns
$\overline{RD}\downarrow$ delay time from ASTB↓	t_{ASTRD}		25		ns
$\overline{WR}\downarrow$ delay time from ASTB↓	t_{ASTWR}		$0.85t_{CY}$ + 20		ns
ASTB↑delay time from $\overline{RD}\uparrow$ in external fetch	t_{RDAST}		$0.85t_{CY}$ – 10	$1.15t_{CY}$ + 20	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t_{RDADH}		$0.85t_{CY}$ – 50	$1.15t_{CY}$ + 50	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		0	50	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		$0.85t_{CY}$	$1.15t_{CY}$ + 40	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTRD}		$1.15t_{CY}$ + 40	$3.15t_{CY}$ + 40	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTWR}		$1.15t_{CY}$ + 30	$3.15t_{CY}$ + 30	ns

Remarks **1.** MCS: Bit 0 of the oscillation mode select register (OSMS)

2. PCC2 to PCC0: Bit 2 to 0 of the processor clock control register (PCC)

3. $t_{CY} = T_{CY}/4$

4. n indicates the number of waits.

(b) Except when MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		t_{CY} – 80		ns
Address setup time	t_{ADS}		t_{CY} – 80		ns
Address hold time	t_{ADH}		0.4t_{CY} – 10		ns
Data input time from address	t_{ADD1}			(3 + 2n)t_{CY} – 160	ns
	t_{ADD2}			(4 + 2n)t_{CY} – 200	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			(1.4 + 2n)t_{CY} – 70	ns
	t_{RDD2}			(2.4 + 2n)t_{CY} – 70	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		(1.4 + 2n)t_{CY} – 20		ns
	t_{RDL2}		(2.4 + 2n)t_{CY} – 20		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t_{RDWT1}			t_{CY} – 100	ns
	t_{RDWT2}			2t_{CY} – 100	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t_{WRWT}			2t_{CY} – 100	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(1 + 2n)t_{CY}	(2 + 2n)t_{CY}	ns
Write data setup time	t_{WDS}		(2.4 + 2n)t_{CY} – 60		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL1}		(2.4 + 2n)t_{CY} – 20		ns
$\overline{RD}\downarrow$ delay time from ASTB$\downarrow$	t_{ASTRD}		0.4t_{CY} – 30		ns
$\overline{WR}\downarrow$ delay time from ASTB$\downarrow$	t_{ASTWR}		1.4t_{CY} – 30		ns
ASTB$\uparrow$delay time from $\overline{RD}\uparrow$ in external fetch	t_{RDAST}		t_{CY} – 10	t_{CY} + 20	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t_{RDADH}		t_{CY} – 50	t_{CY} + 50	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		0.4t_{CY} – 20		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		0	60	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		t_{CY}	t_{CY} + 60	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTRD}		0.6t_{CY} + 180	2.6t_{CY} + 180	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTWR}		0.6t_{CY} + 120	2.6t_{CY} + 120	ns

Remarks 1. MCS: Bit 0 of the oscillation mode select register (OSMS)

2. PCC2 to PCC0: Bit 2 to 0 of the processor clock control register (PCC)

3. $t_{CY} = T_{CY}/4$

4. n indicates the number of waits.

(3) Serial Interface (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK0}$ high-/low-level width	t_{KH1},	V_{DD} = 4.5 to 5.5 V	$t_{KCY1}/2$ – 50			ns
	t_{KL1}		$t_{KCY1}/2$ – 100			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK1}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI1}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO1}	C = 100 pF Note			300	ns

Note C is the SO0 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK0}$ high-/low-level width	t_{KH2},	V_{DD} = 4.5 to 5.5 V	400			ns
	t_{KL2}		800			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK2}		100			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI2}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO2}	C = 100 pF Note			300	ns
$\overline{SCK0}$ rise/fall time	t_{R2}, t_{F2}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the SO0 output line load capacitance.

(iii) SBI mode ($\overline{SCK0}$ ... internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH3},	V_{DD} = 4.5 to 5.5 V		$t_{KCY3}/2 - 50$			ns
	t_{KL3}			$t_{KCY3}/2 - 150$			ns
SB0, SB1 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK3}	V_{DD} = 4.5 to 5.5 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI3}			$t_{KCY3}/2$			ns
SB0, SB1 output delay time from	t_{KSO3}	R = 1 kΩ,	V_{DD} = 4.5 to 5.5 V	0		250	ns
$\overline{SCK0}\downarrow$		C = 100 pF [Note]		0		1000	ns
SB0, SB1↓ from $\overline{SCK0}\uparrow$	t_{KSB}			t_{KCY3}			ns
$\overline{SCK0}\downarrow$ from SB0, SB1↓	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R and C are the SB0 and SB1 output line load resistance and load capacitance.

(iv) SBI mode ($\overline{SCK0}$ ... external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH4},	V_{DD} = 4.5 to 5.5 V		400			ns
	t_{KL4}			1600			ns
SB0, SB1 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK4}	V_{DD} = 4.5 to 5.5 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI4}			$t_{KCY4}/2$			ns
SB0, SB1 output delay time from	t_{KSO4}	R = 1 kΩ,	V_{DD} = 4.5 to 5.5 V	0		300	ns
$\overline{SCK0}\downarrow$		C = 100 pF [Note]		0		1000	ns
SB0, SB1↓ from $\overline{SCK0}\uparrow$	t_{KSB}			t_{KCY4}			ns
$\overline{SCK0}\downarrow$ from SB0, SB1↓	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{SCK0}$ rise/fall time	t_{R4}, t_{F4}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note R and C are the SB0 and SB1 output line load resistance and load capacitance.

(v) 2-wire serial I/O mode ($\overline{SCK0}$ ... internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF Note	V_{DD} = 4.5 to 5.5 V	1600			ns
				3200			ns
$\overline{SCK0}$ high-level width	t_{KH5}			$t_{KCY5}/2 - 160$			ns
$\overline{SCK0}$ low-level width	t_{KL5}			$t_{KCY5}/2 - 50$			ns
SB0, SB1 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK5}		V_{DD} = 4.5 to 5.5 V	300			ns
				350			ns
SB0, SB1 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI5}			600			ns
SB0, SB1 output delay time from $\overline{SCK0}\downarrow$	t_{KSO5}			0		300	ns

Note R and C are the $\overline{SCK0}$, SB0 and SB1 output line load resistance and load capacitance.

(vi) 2-wire serial I/O mode ($\overline{SCK0}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}	V_{DD} = 4.5 to 5.5 V	1600			ns
			3200			ns
$\overline{SCK0}$ high-level width	t_{KH6}		650			ns
$\overline{SCK0}$ low-level width	t_{KL6}		800			ns
SB0, SB1 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK6}		100			ns
SB0, SB1 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI6}		$t_{KCY6}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}\downarrow$	t_{KSO6}	R = 1 kΩ, C = 100 pF Note	0		300	ns
$\overline{SCK0}$ rise/fall time	t_{R6}, t_{F6}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note R and C are the $\overline{SCK0}$, SB0 and SB1 output line load resistance and load capacitance.

(b) Serial interface channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY7}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH7},	V_{DD} = 4.5 to 5.5 V	$t_{KCY7}/2 - 50$			ns
	t_{KL7}		$t_{KCY7}/2 - 100$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK7}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI7}		400			ns
SO1 output delay time from $\overline{SCK1}\downarrow$	t_{KSO7}	C = 100 pF Note			300	ns

Note C is the SO1 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY8}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH8},	V_{DD} = 4.5 to 5.5 V	400			ns
	t_{KL8}		800			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK8}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI8}		400			ns
SO1 output delay time from $\overline{SCK1}\downarrow$	t_{KSO8}	C = 100 pF Note			300	ns
$\overline{SCK1}$ rise/fall time	t_{R8}, t_{F8}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the SO1 output line load capacitance.

(iii) Automatic transmission/reception function 3-wire serial I/O mode ($\overline{SCK1}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH9},	V_{DD} = 4.5 to 5.5 V	$t_{KCY9}/2 - 50$			ns
	t_{KL9}		$t_{KCY9}/2 - 100$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK9}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI9}		400			ns
SO1 output delay time from $\overline{SCK1}\downarrow$	t_{KSO9}	C = 100 pF Note, V_{DD} = 4.5 to 5.5 V			300	ns
STB$\uparrow$ from $\overline{SCK1}\uparrow$	t_{SBD}		$t_{KCY9}/2 - 100$		$t_{KCY9}/2 + 100$	ns
Strobe signal high-level width	t_{SBW}		$t_{KCY9} - 30$		$t_{KCY9} + 30$	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
$\overline{SCK1}\downarrow$ from busy inactivation	t_{SPS}				$2t_{KCY9}$	ns

Note C is the SO1 output line load capacitance.

(iv) Automatic transmission/reception function 3-wire serial I/O mode ($\overline{SCK1}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH10},	V_{DD} = 4.5 to 5.5 V	400			ns
	t_{KL10}		800			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK10}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI10}		400			ns
SO1 output delay time from $\overline{SCK1}\downarrow$	t_{KSO10}	C = 100 pF Note			300	ns
$\overline{SCK1}$ rise/fall time	t_{R10}, t_{F10}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the SO1 output line load capacitance.

(c) Serial interface channel 2

(i) 3-wire serial I/O mode ($\overline{SCK2}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY11}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK2}$ high-/low-level width	t_{KH11},	V_{DD} = 4.5 to 5.5 V	$t_{KCY11}/2 - 50$			ns
	t_{KL11}		$t_{KCY11}/2 - 100$			ns
SI2 setup time (to $\overline{SCK2}\uparrow$)	t_{SIK11}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI2 hold time (from $\overline{SCK2}\uparrow$)	t_{KSI11}		400			ns
SO2 output delay time from $\overline{SCK2}\downarrow$	t_{KSO11}	C = 100 pF Note			300	ns

Note C is the SO2 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{SCK2}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY12}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK2}$ high-/low-level width	t_{KH12},	V_{DD} = 4.5 to 5.5 V	400			ns
	t_{KL12}		800			ns
SI2 setup time (to $\overline{SCK2}\uparrow$)	t_{SIK12}		100			ns
SI2 hold time (from $\overline{SCK2}\uparrow$)	t_{KSI12}		400			ns
SO2 output delay time from $\overline{SCK2}\downarrow$	t_{KSO12}	C = 100 pF Note			300	ns
$\overline{SCK2}$ rise/fall time	t_{R12}, t_{F12}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the SO2 output line load capacitance.

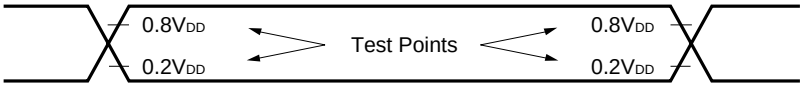
(iii) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 4.5 to 5.5 V			78125	bps
					39063	bps

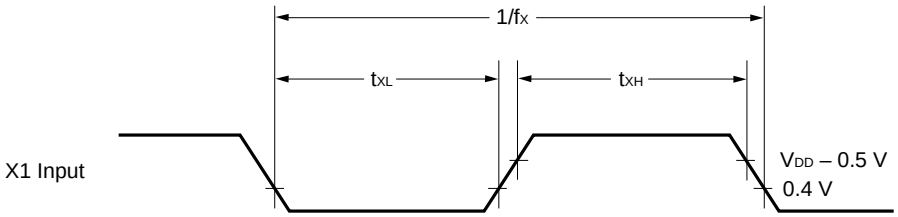
(iv) UART mode (External clock input)

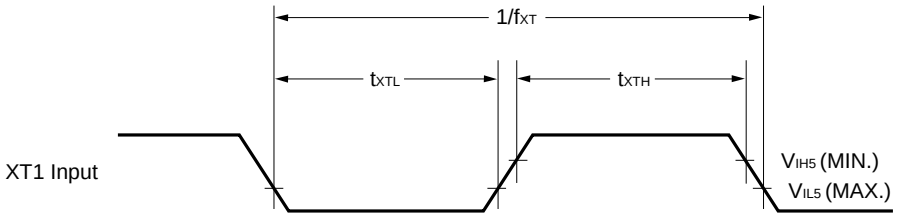
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY13}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
ASCK high-/low-level width	t_{KH13}, t_{KL13}	V_{DD} = 4.5 to 5.5 V	400			ns
			800			ns
Transfer rate		V_{DD} = 4.5 to 5.5 V			39063	bps
					19531	bps
$\overline{SCK}$ rise/fall time	t_{R13}, t_{F13}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

AC Timing Test Point (Excluding X1, XT1 Input)

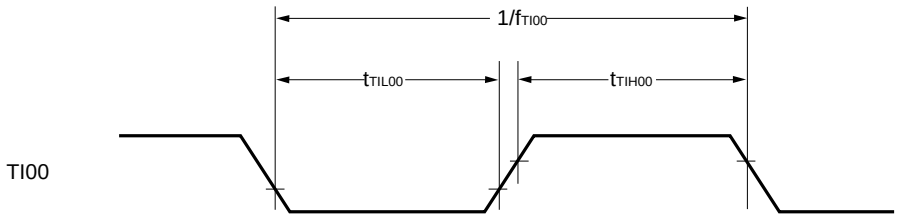


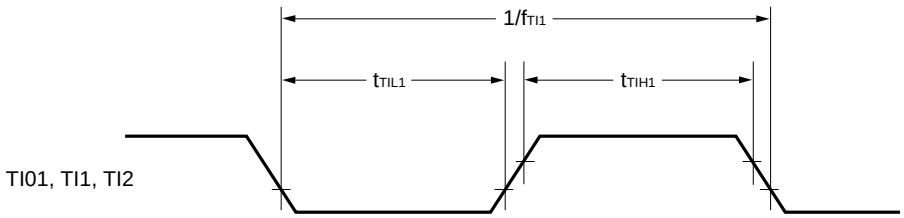
Clock Timing





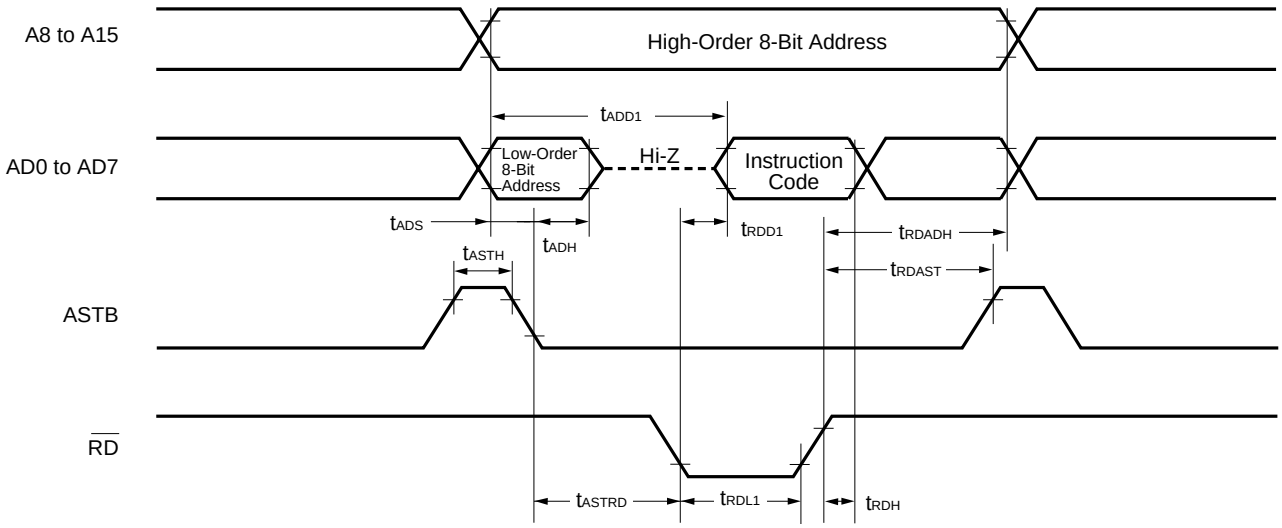
TI Timing



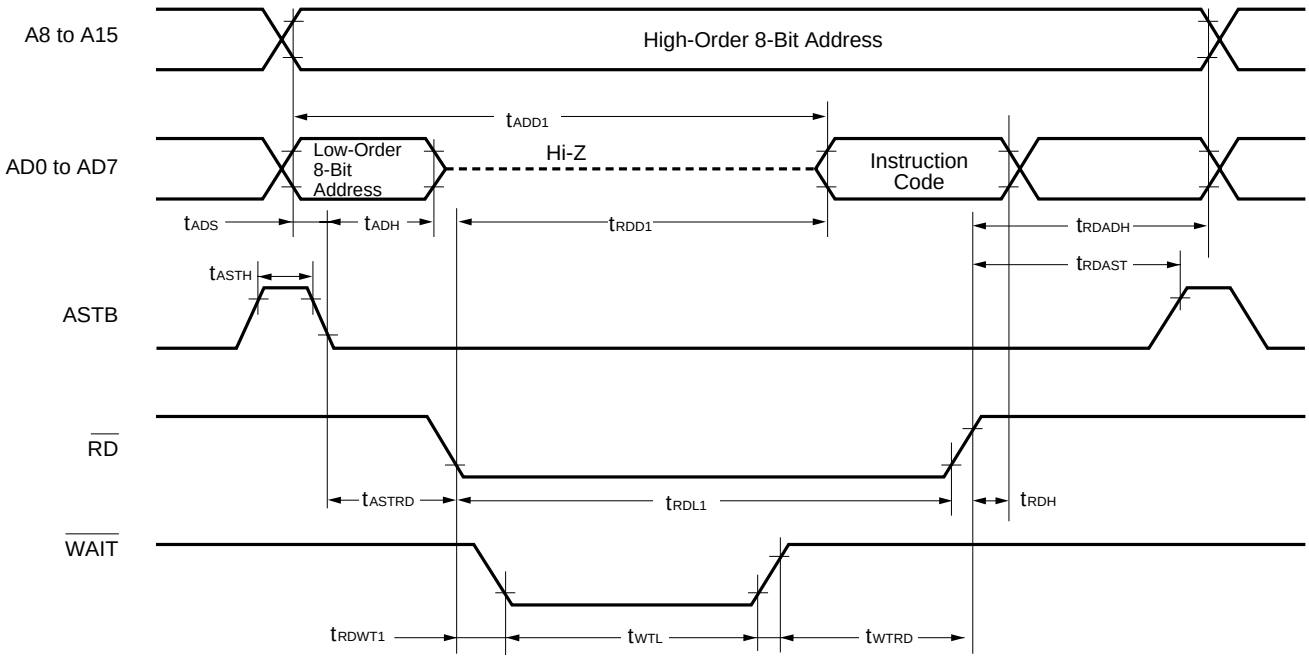


Read/Write Operations

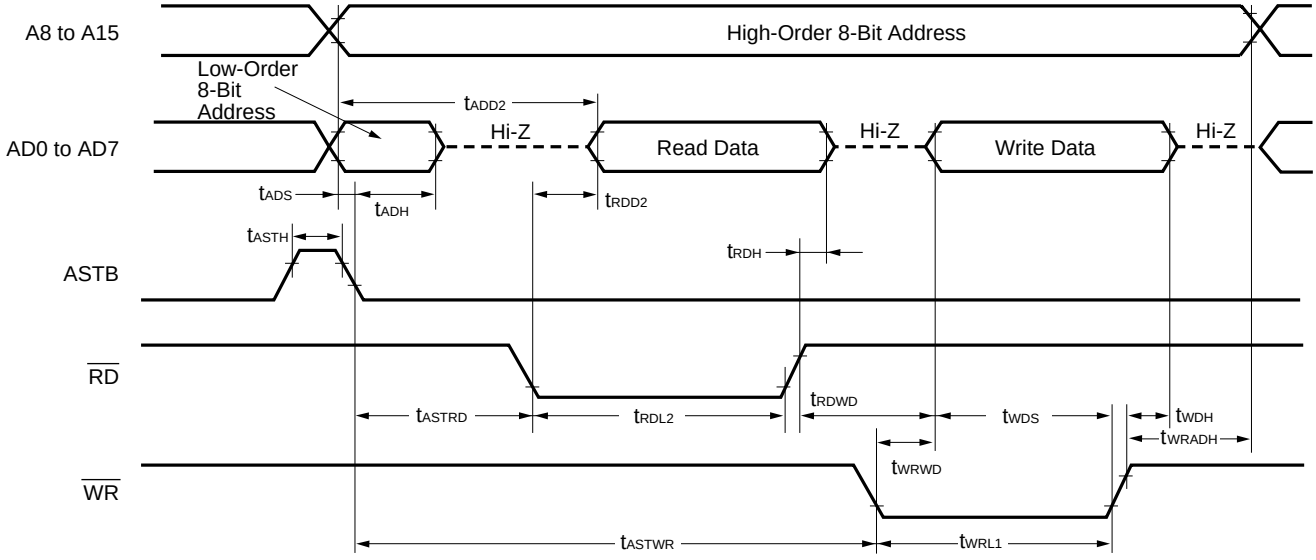
External fetch (no wait):



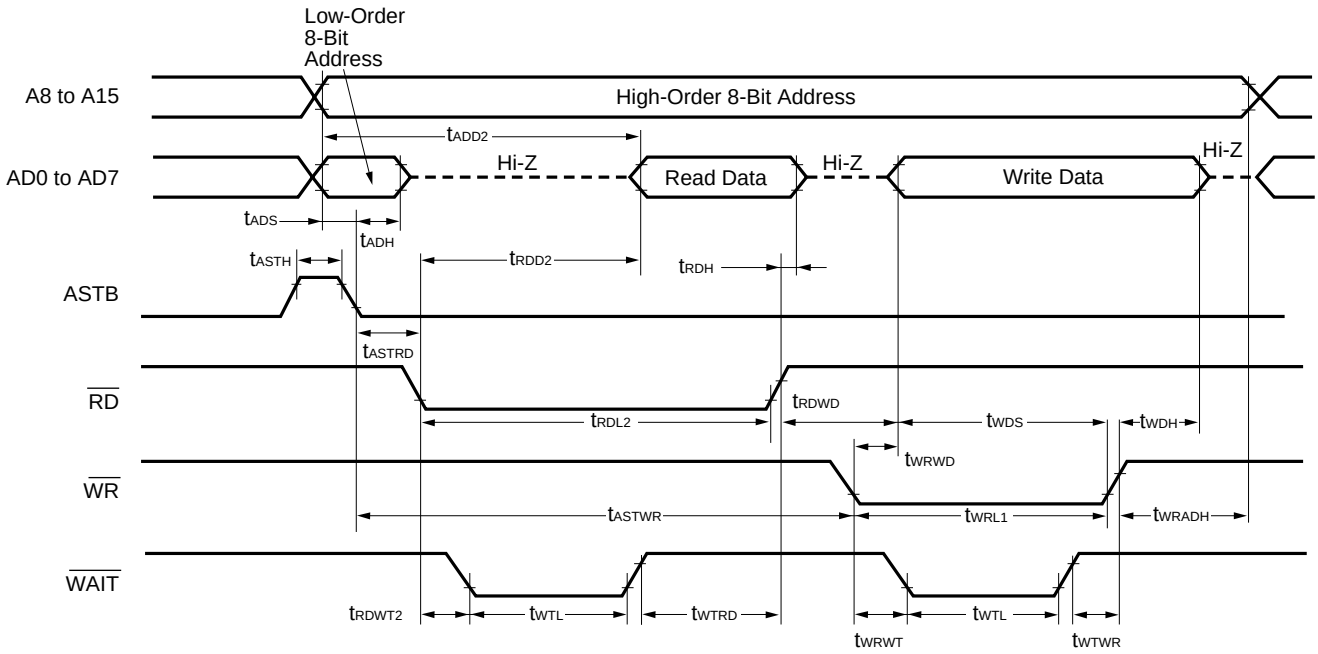
External fetch (wait insertion):



External data access (no wait):

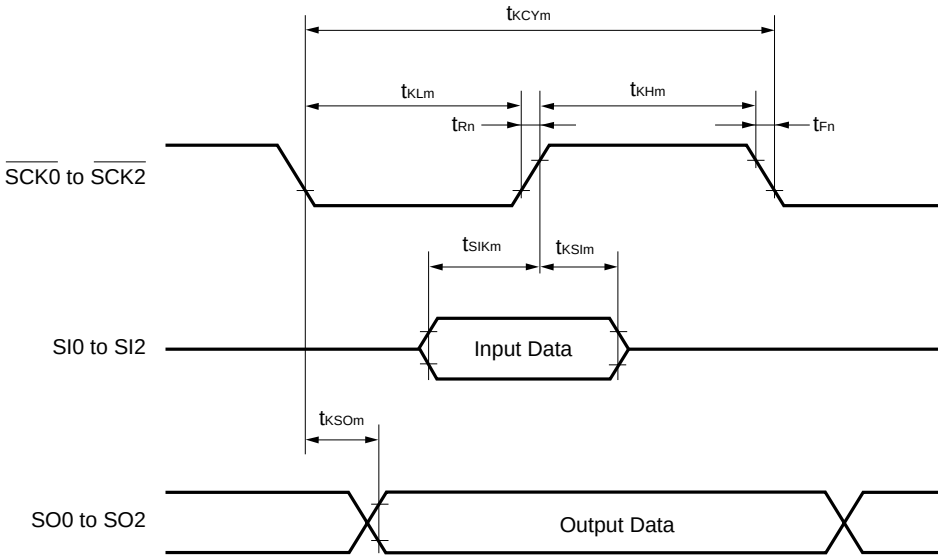


External data access (wait insertion):



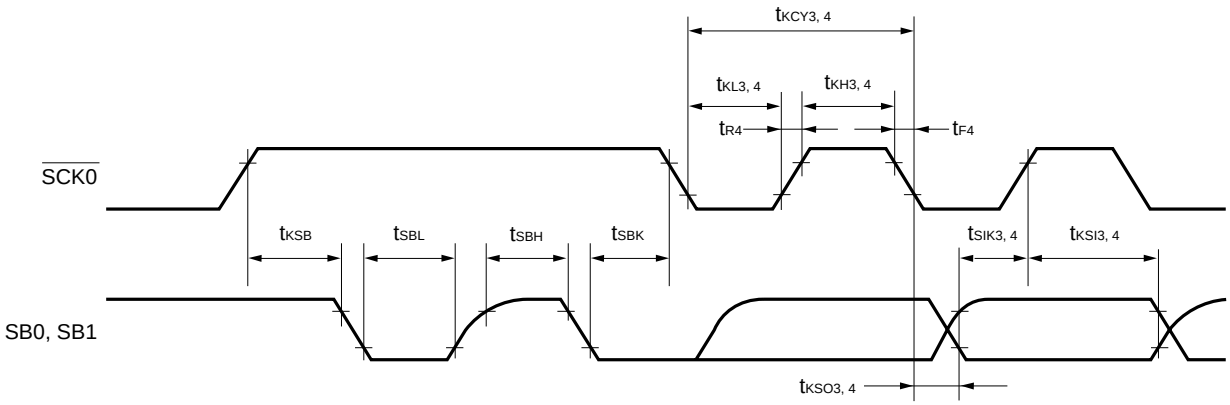
Serial Transfer Timing

3-wire serial I/O mode:

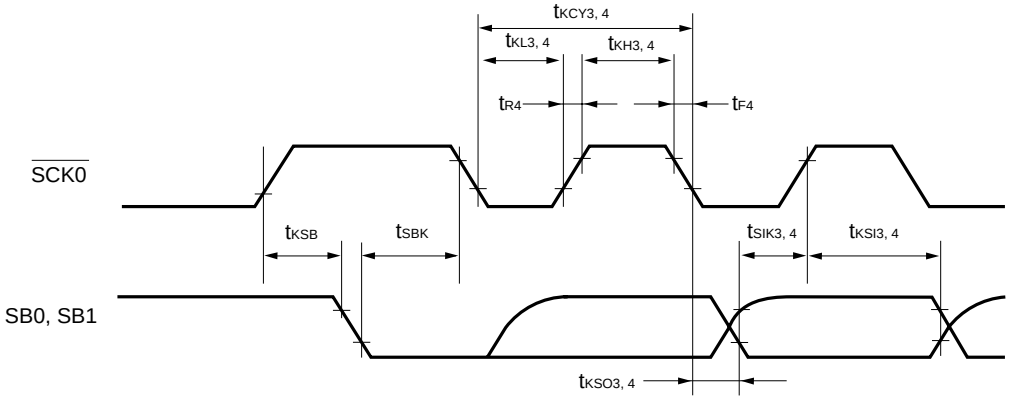


m = 1, 2, 7, 8, 11, 12
n = 2, 8, 12

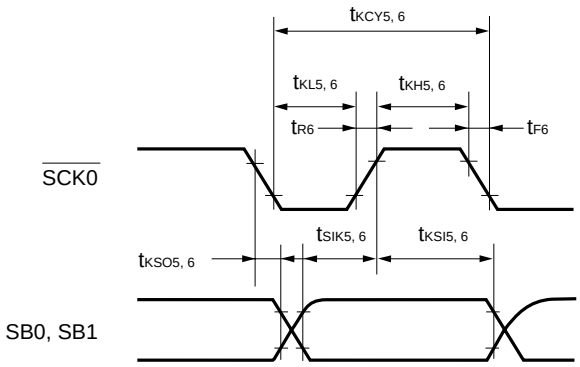
SBI mode (bus release signal transfer):



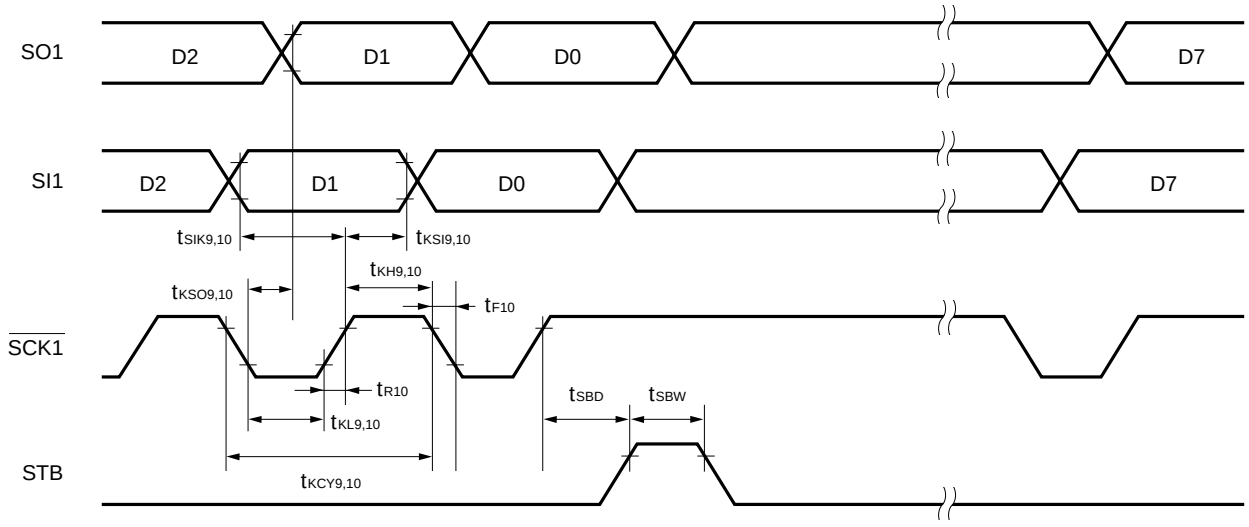
SBI mode (command signal transfer):



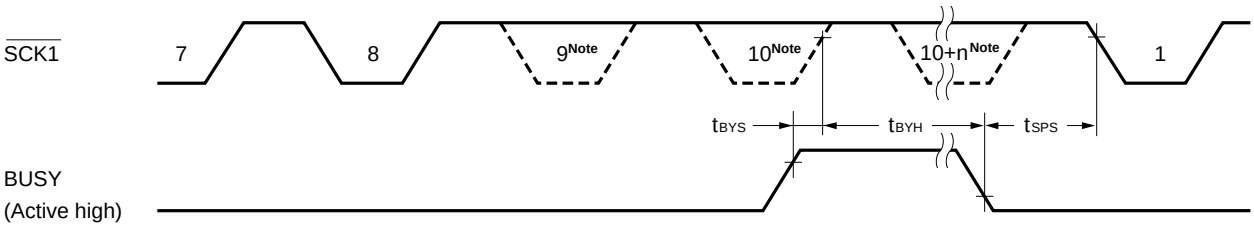
2-wire serial I/O mode:



Automatic transmission/reception function 3-wire serial I/O mode:

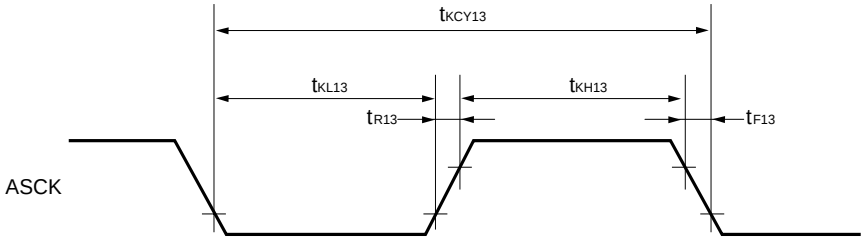


Automatic transmission/reception function 3-wire serial I/O mode (busy processing):



Note The signal is not actually low here, but is represented this way to show the timing.

UART mode (external Clock Input):



A/D Converter Characteristics (T_A = –40 to +85°C, AV_{DD} = V_{DD} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Resolution				8	8	8	bit
Total error Note		IEAD = 00H				1.8	%
		IEAD = 01H	V_{DD} = 4.5 to 5.5 V		2.2	3.4	%
					2.6	3.8	%
Conversion time	t_{CONV}			19.1		200	μs
Sampling time	t_{SAMP}			12/f_{XX}			μs
Analog input voltage	V_{IAN}			AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}			2.7		AV_{DD}	V
AV_{REF0}-AV_{SS} resistance	R_{AIREF0}			4	14		kΩ

Note Excluding quantization error (±1/2 LSB). Shown as a percentage of the full scale value.

Remarks f_{XX} : Main system clock frequency
IEAD : A/D current cut select register

D/A Converter Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Resolution						8	bit
Total error		R = 2 MΩ Note 1				1.2	%
		R = 4 MΩ Note 1				0.8	%
		R = 10 MΩ Note 1				0.6	%
Settling time		C = 30 pF Note 1	AV_{REF} = 4.5 to 5.5 V			10	μs
						15	μs
Output resistance	R_{O0}	DACS0 = 55H			10		kΩ
	R_{O1}	DACS1 = 55H			10		kΩ
Analog reference voltage	AV_{REF1}			2.7		V_{DD}	V
AV_{REF1} current	AI_{REF1}	**Note 2**				1.5	mA

Notes 1. R and C are the D/A converter output pin load resistance and load capacitance.
2. Value for one D/A converter channel.

Remarks DACS0, DACS1 : D/A conversion value setting registers 0, 1

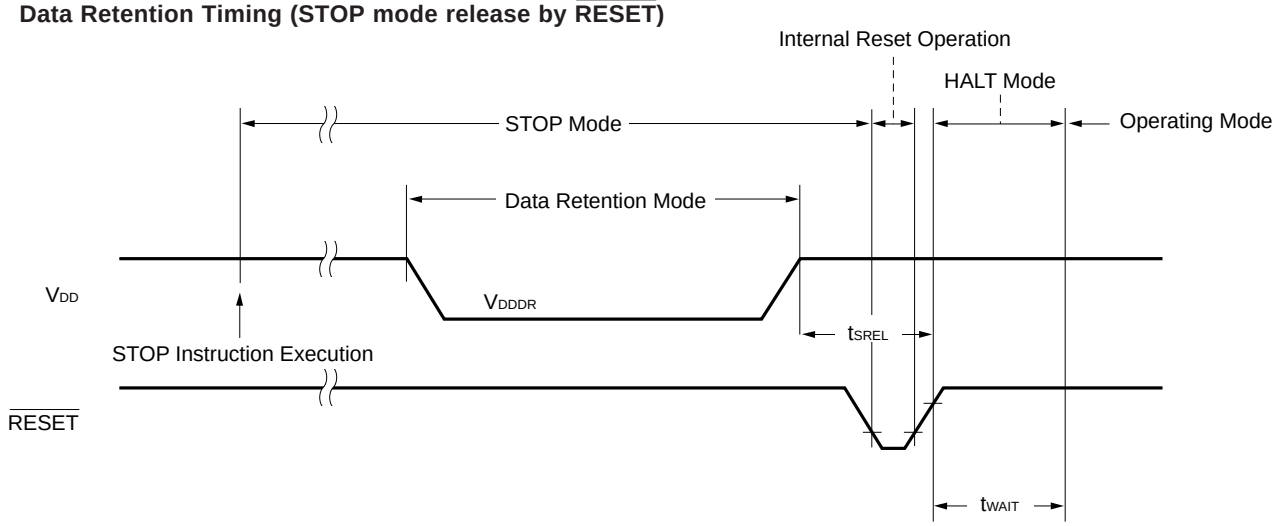
Data Memory STOP Mode Low Power Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.0 V Subsystem clock stopped, feedback resistor disconnected		0.1	10	μA
Release signal setup time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note**		ms

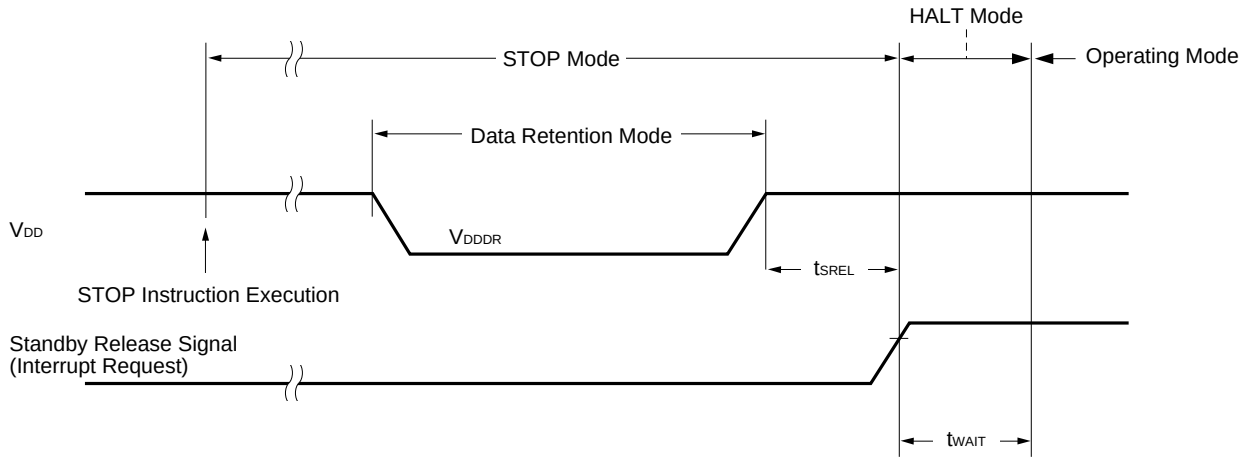
Note $2^{12}/f_{XX}$, or $2^{14}/f_{XX}$ through $2^{17}f_{XX}$ can be selected by bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

Remark f_{XX} : Main system clock frequency
f_X : Main system clock oscillation frequency

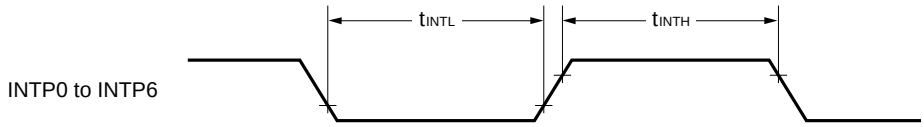
Data Retention Timing (STOP mode release by $\overline{RESET}$)



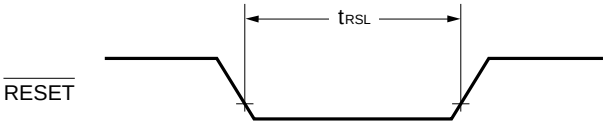
Data Retention Timing (STOP mode release by using standby release signal or interrupt request signal)



Interrupt Request Input Timing



$\overline{\text{RESET}}$ Input Timing



IEBus Controller Characteristics (T_A = –40 to +85°C, V_{DD} = 5 V ±10%)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
IEBus controller system clock frequency	fs	When using mode 0 or 1 Note 1		5.91	6.00	6.09	MHz
				6.20	6.29	6.39	MHz
		When using mode 2		5.97	6.00	6.03	MHz
				6.26	6.29	6.32	MHz
Driver delay time ($\overline{\text{TX}}$ output → bus line)		C = 50 pF Note 2	fs = 6.00 MHz			1.6	μs
			fs = 6.29 MHz			1.5	μs
Receiver delay time (Bus line → $\overline{\text{RX}}$ input)		fs = 6.00 MHz				0.75	μs
		fs = 6.29 MHz				0.7	μs
Propagation delay time on the bus		fs = 6.00 MHz				0.9	μs
		fs = 6.29 MHz				0.85	μs

Notes 1. For the values in the second row, the IEBus standards are not satisfied.

2. C is the $\overline{\text{TX}}$ output line load capacitance.

Remark fs: IEBus controller system clock frequency.

PROM PROGRAMMING CHARACTERISTICS

DC Characteristics

(1) PROM Write Mode (T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol Note	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH}	V_{IH}		0.7V_{DD}		V_{DD}	V
Input voltage low	V_{IL}	V_{IL}		0		0.3V_{DD}	V
Output voltage high	V_{OH}	V_{OH}	I_{OH} = –1 mA	V_{DD} – 1.0			V
Output voltage low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	0 ≤ V_{IN} ≤ V_{DD}	–10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		12.2	12.5	12.8	V
V_{DD} supply voltage	V_{DD}	V_{CC}		6.25	6.5	6.75	V
V_{PP} supply current	I_{PP}	I_{PP}	$\overline{PGM}$ = V_{IL}			50	mA
V_{DD} supply current	I_{DD}	I_{CC}				50	mA

(2) PROM Read Mode (T_A = 25 ±5°C, V_{DD} = 5.0 ±0.5 V, V_{PP} = V_{DD} ±0.6 V)

Parameter	Symbol	Symbol Note	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH}	V_{IH}		0.7V_{DD}		V_{DD}	V
Input voltage low	V_{IL}	V_{IL}		0		0.3V_{DD}	V
Output voltage high	V_{OH1}	V_{OH1}	I_{OH} = –1 mA	V_{DD} – 1.0			V
	V_{OH2}	V_{OH2}	I_{OH} = –100 μA	V_{DD} – 0.5			V
Output voltage low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	0 ≤ V_{IN} ≤ V_{DD}	–10		+10	μA
Output leakage current	I_{LO}	I_{LO}	0 ≤ V_{OUT} ≤ V_{DD}, $\overline{OE}$ = V_{IH}	–10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		V_{DD} – 0.6	V_{DD}	V_{DD} + 0.6	V
V_{DD} supply voltage	V_{DD}	V_{CC}		4.5	5.0	5.5	V
V_{PP} supply current	I_{PP}	I_{PP}	V_{PP} = V_{DD}			100	μA
V_{DD} supply current	I_{DD}	I_{CCA1}	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH}			50	mA

Note Corresponding μPD27C1001A symbol.

AC Characteristics

(1) PROM Write Mode

(a) Page program mode (T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol Note	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{OE}\downarrow$)	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ setup time	t_{OES}	t_{OES}		2			μs
CE setup time (to $\overline{OE}\downarrow$)	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{OE}\downarrow$)	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}\uparrow$)	t_{AH}	t_{AH}		2			μs
	t_{AHL}	t_{AHL}		2			μs
	t_{AHV}	t_{AHV}		0			μs
Input data hold time (from $\overline{OE}\uparrow$)	t_{DH}	t_{DH}		2			μs
Data output float delay time from $\overline{OE}\uparrow$	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{OE}\downarrow$)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{OE}\downarrow$)	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	t_{PW}	t_{PW}		0.095		0.105	ms
Valid data delay time from $\overline{OE}\downarrow$	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ pulse width during data latching	t_{LW}	t_{LW}		1			μs
$\overline{PGM}$ setup time	t_{PGMS}	t_{PGMS}		2			μs
$\overline{CE}$ hold time	t_{CEH}	t_{CEH}		2			μs
$\overline{OE}$ hold time	t_{OEH}	t_{OEH}		2			μs

(b) Byte program mode (T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol Note	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{PGM}\downarrow$)	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ setup time	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (to $\overline{PGM}\downarrow$)	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{PGM}\downarrow$)	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}\uparrow$)	t_{AH}	t_{AH}		2			μs
Input data hold time (from $\overline{PGM}\uparrow$)	t_{DH}	t_{DH}		2			μs
Data output float delay time from $\overline{OE}\uparrow$	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{PGM}\downarrow$)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{PGM}\downarrow$)	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	t_{PW}	t_{PW}		0.095		0.105	ms
Valid data delay time from $\overline{OE}\downarrow$	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ hold time	t_{OEH}	—		2			μs

Note Corresponding μPD27C1001A symbol

(2) PROM Read Mode (T_A = 25 ±5°C, V_{DD} = 5.0 ±0.5 V, V_{PP} = V_{DD} ±0.6 V)

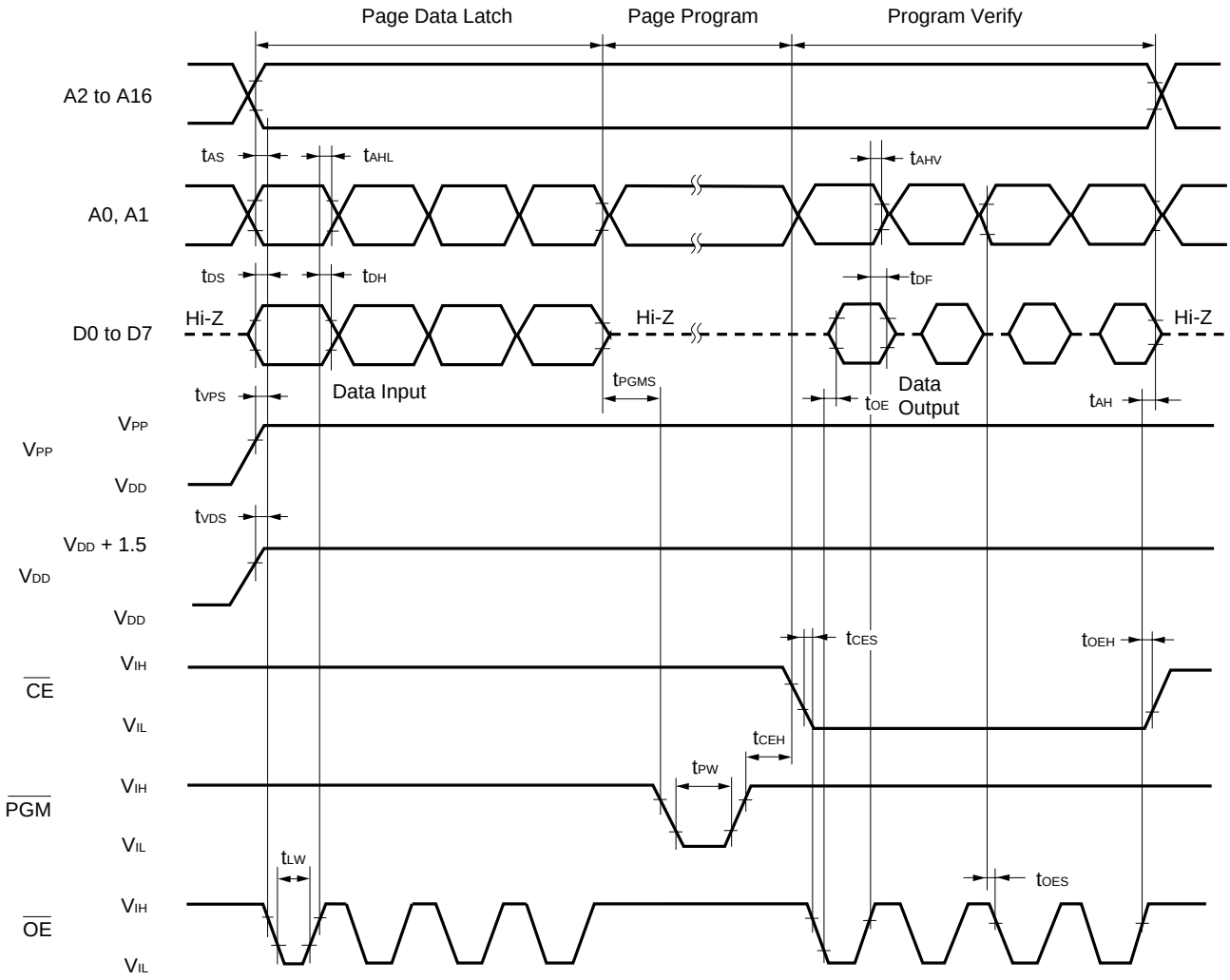
Parameter	Symbol	Symbol Note	Test Conditions	MIN.	TYP.	MAX.	Unit
Data output delay time from address	t_{ACC}	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			800	ns
Data output delay time from $\overline{CE}$↓	t_{CE}	t_{CE}	$\overline{OE}$ = V_{IL}			800	ns
Data output delay time from $\overline{OE}$↓	t_{OE}	t_{OE}	$\overline{CE}$ = V_{IL}			200	ns
Data output float delay time from $\overline{OE}$↑	t_{DF}	t_{DF}	$\overline{CE}$ = V_{IL}	0		60	ns
Data hold time from address	t_{OH}	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0			ns

Note Corresponding μPD27C1001A symbol

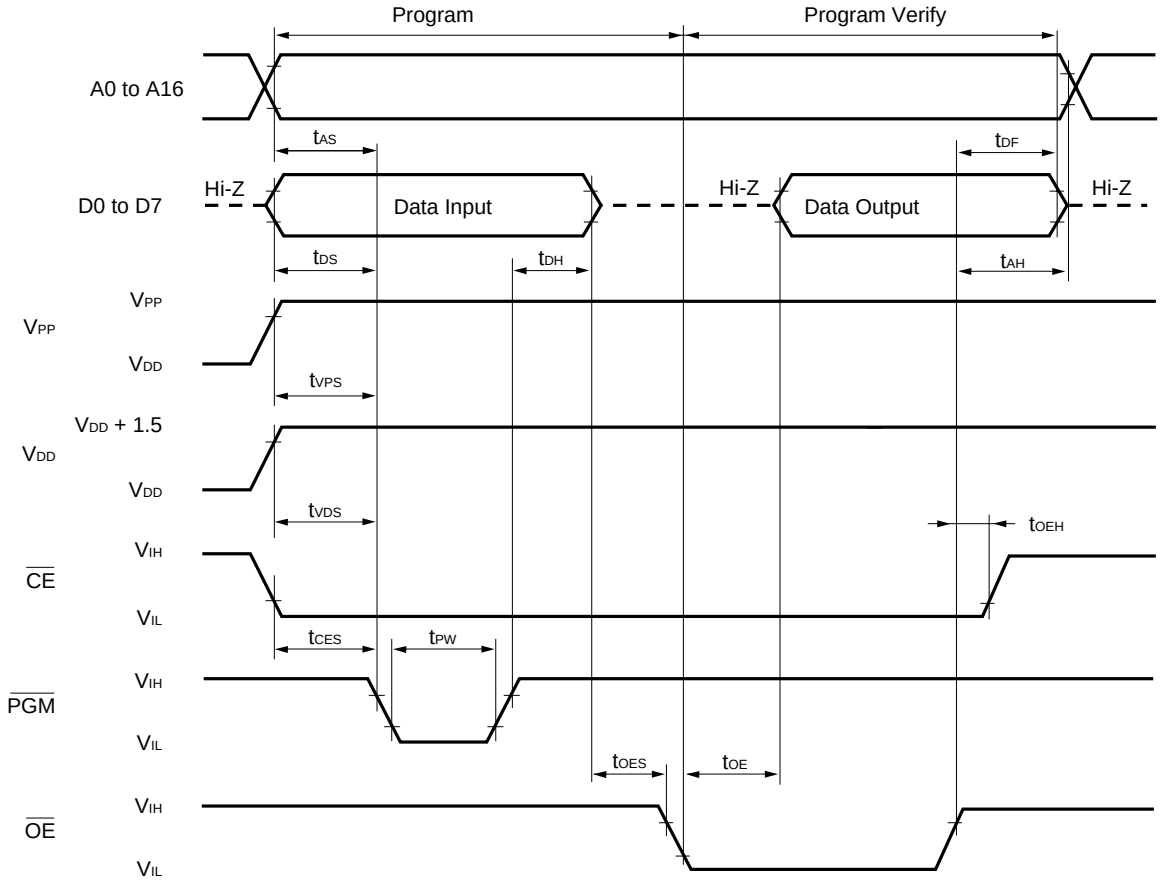
(3) PROM Programming Mode Setting (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
PROM programing mode setup time	t_{SMA}		10			μs

PROM Write Mode Timing (page program mode)



PROM Write Mode Timing (byte program mode)

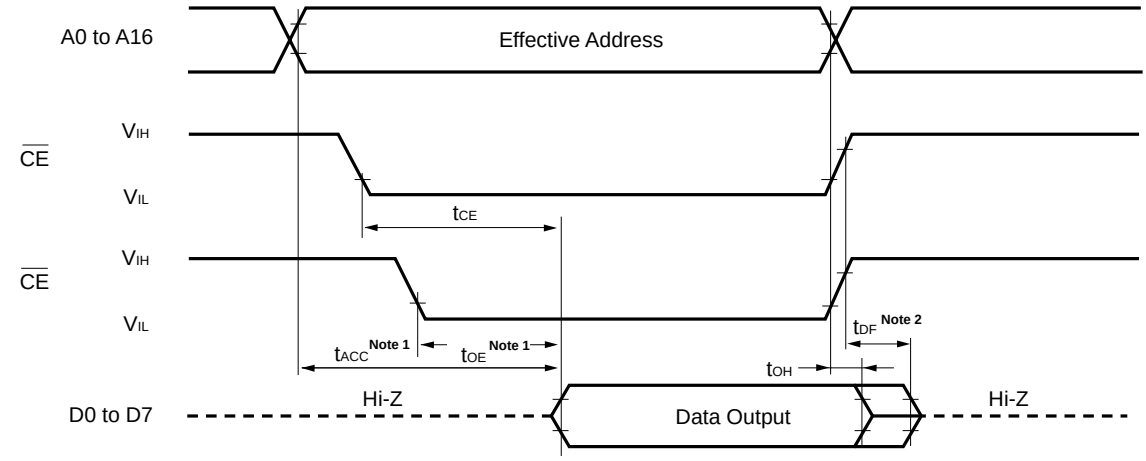


Cautions 1. V_{DD} should be applied before V_{PP}, and cut after V_{PP}.

2. V_{PP} should not exceed +13.5 V including overshoot.

3. Disconnection during application of ±12.5 V to V_{PP} may have an adverse effect on reliability.

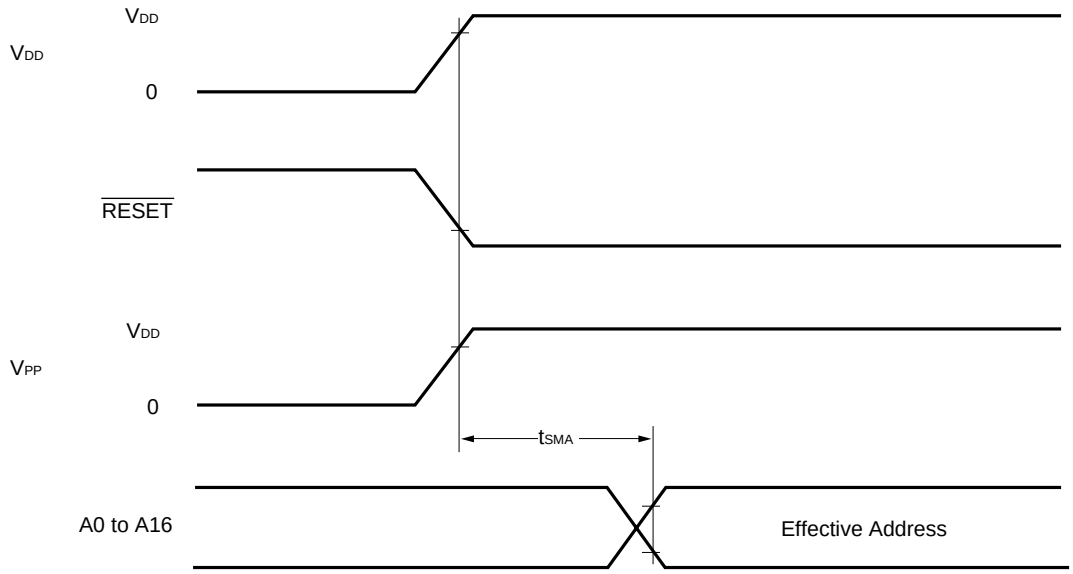
PROM Read Mode Timing



Notes 1. If you want to read within the t_{ACC} range, make the $\overline{OE}$ input delay time from the fall of $\overline{CE}$ the maximum of $t_{ACC} - t_{OE}$.

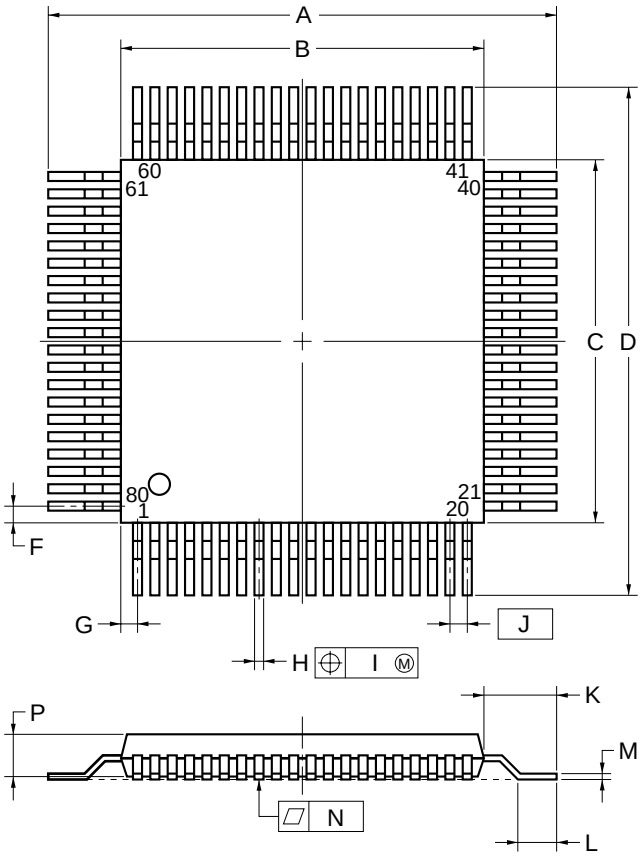
2. t_{DF} is the time from when either $\overline{OE}$ or $\overline{CE}$ first reaches V_{IH}.

PROM Programming Mode Setting Timing

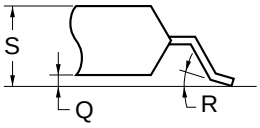


8. PACKAGE DRAWING

80 PIN PLASTIC QFP (14×14)



detail of lead end



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.825	0.032
G	0.825	0.032
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S80GC-65-3B9-4

Remarks The shape and material of ES versions are the same as those of mass-produced versions.

9. RECOMMENDED SOLDERING CONDITIONS

It is recommended that the μPD78P098B be soldered under the following conditions.

For details on the recommended soldering conditions, refer to information document "Semiconductor Device Mounting Technology Manual" (C10535E).

For soldering methods and conditions other than those recommended, please consult an NEC sales representative.

Table 9-1. Surface mounting type soldering conditions

μPD78P098BGC-3B9: 80-pin plastic QFP (14 × 14 mm)

Solder method	Soldering conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Time: within 30 sec. (min. 210°C) Count: 3 times max., Limit on days: 7 day period Note (hereafter 125°C pre-bake time is required)	IR35-207-3
VPS	Package peak temperature: 215°C, Time: within 40 sec. (min. 200°C) Count: 3 times max., Limit on days: 7 day period Note (hereafter 125°C pre-bake time is required)	VP15-207-3
Partial heating	Pin temperature: Max of 300°C, Time: Within 3 sec. (per pin row)	—

Note Exposure limit before soldering after dry-pack package is opened. Storage conditions: 25˚C and relative humidity of 65% or less.

Caution Do not employ more than one soldering method at any one time, except for the partial heating method.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools have been provided for system development using the μPD78P098B.

Language Processing Software

RA78K/0 Notes 1, 2, 3, 4	Assembler package common to 78K/0 Series products
CC78K/0 Notes 1, 2, 3, 4	C compiler package common to 78K/0 Series products
DF78098 Notes 1, 2, 3, 4	Device file common to μPD78098 Subseries products
CC78K/0-L Notes 1, 2, 3, 4	C compiler library source file common to 78K/0 Series products

PROM Write Tools

PG-1500	PROM programmer
PA-78P054GC	Programmer adapter connected to the PG-1500
PG-1500 controller Notes 1, 2	Control program for the PG-1500

Debugging Tools

IE-78000-R	In-circuit emulator common to 78K/0 Series products
IE-78000-R-A	In-circuit emulator common to 78K/0 Series products (for integrated debugger)
IE-78000-R-BK	Break board common to 78K/0 Series products
IE-78098-R-EM Note 8 IE-780908-R-EM	Emulation board common to μPD78098 Subseries products
IE-78000-R-SV3	Interface adapter and cable when an EWS is used as the host machine (IE-78000-R-A)
IE-70000-98-IF-B	Interface adapter when a PC-9800 series (excluding notebook PCs) PC is used as the host machine (for IE-78000-R-A)
IE-70000-98N-IF	Interface adapter and cable when a PC-9800 series (excluding notebook PCs) PC is used as the host machine (for IE-78000-R-A)
IE-70000-PC-IF-B	Interface adapter when an IBM PC/AT™ PC is used as the host machine (for IE-78000-R-A)
EP-78234GC-R	Emulator probe common to μPD78234 Subseries products
EV-9200GC-80 (See Figure A-1)	Socket mounted on target system board made for an 80-pin plastic QFP (GC-3B9 type)
SM78K0 Notes 5, 6, 7	System simulator common to 78K/0 Series products
ID78K0 Notes 4, 5, 6, 7	Integrated debugger for the IE-78000-R-A
SD78K/0 Notes 1, 2	Screen debugger for the IE-78000-R
DF78098 Notes 1, 2, 4, 5, 6, 7	Device file common to μPD78078 Subseries products

Real-Time OS

RX78K/0 Notes 1, 2, 3, 4	Real-time OS used for 78/0 Series products
MX78K0 Notes 1, 2, 3, 4	OS used for 78K/0 Series products

Fuzzy Inference Development Support System

FE9000 Note 1/FE9200 Note 6	Fuzzy knowledge data creation tool
FT9080 Note 1/FT9085 Note 2	Translator
FI78K0 Notes 1, 2	Fuzzy inference module
FD78K0 Notes 1, 2	Fuzzy inference debugger

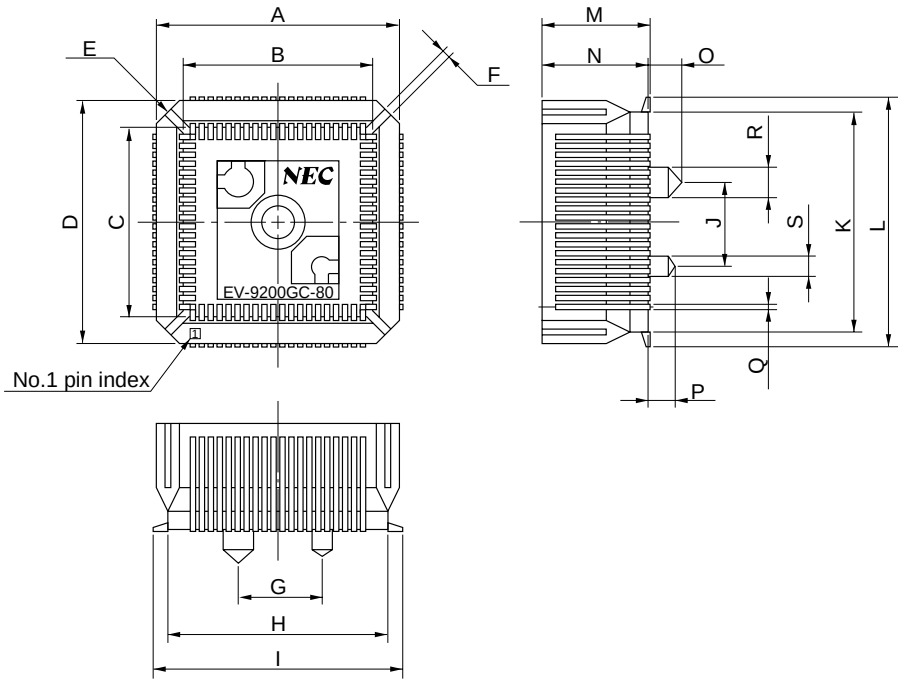
Notes 1. PC-9800 series (MS DOS™) base
2. IBM PC/AT and its compatibles (PC DOS™/IBM DOS™/MS-DOS) base
3. HP9000 series 300™ (HP-UX™) base
4. HP9000 series 700™ (HP-UX) base, SPARCstation™ (SunOS™) base, EWS4800 series (EWS-UX/V) base
5. PC-9800 series (MS-DOS+Windows™) base
6. IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS+Windows) base
7. NEWS™ (NEWS-OS™) base
8. Maintenance only.

Remarks 1. The DF78098 is used in combination with the RA78K/0, CC78K/0, SD78K/0, SM78K0, ID78K0, and RX78K/0.
2. For third party development tools, see **78K/0 Series Selection Guide (U11126E**).

CONVERSION SOCKET DRAWING AND FOOTPRINTS

Figure A-1. Socket Drawing of EV-9200GC-80 (reference)

Based on EV-9200GC-80
(1) Package drawing (in mm)

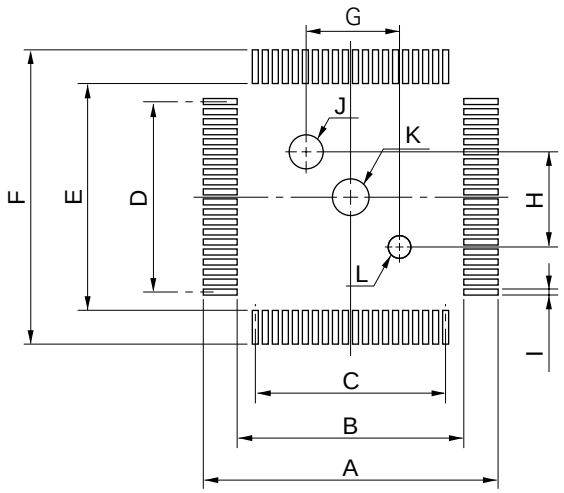


EV-9200GC-80-G0

ITEM	MILLIMETERS	INCHES
A	18.0	0.709
B	14.4	0.567
C	14.4	0.567
D	18.0	0.709
E	4-C 2.0	4-C 0.079
F	0.8	0.031
G	6.0	0.236
H	16.0	0.63
I	18.7	0.736
J	6.0	0.236
K	16.0	0.63
L	18.7	0.736
M	8.2	0.323
O	8.0	0.315
N	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	ϕ2.3	ϕ0.091
S	ϕ1.5	ϕ0.059

Figure A-2. Recommended Footprints of EV-9200GC-80 (reference) (Units : mm)

Based on EV-9200GC-80
(2) Pad drawing (in mm)



EV-9200GC-80-P1E

ITEM	MILLIMETERS	INCHES
A	19.7	0.776
B	15.0	0.591
C	0.65±0.02 × 19=12.35±0.05	$0.026^{+0.001}_{-0.002} \times 0.748 = 0.486^{+0.003}_{-0.002}$
D	0.65±0.02 × 19=12.35±0.05	$0.026^{+0.001}_{-0.002} \times 0.748 = 0.486^{+0.003}_{-0.002}$
E	15.0	0.591
F	19.7	0.776
G	6.0±0.05	$0.236^{+0.003}_{-0.002}$
H	6.0±0.05	$0.236^{+0.003}_{-0.002}$
I	0.35±0.02	$0.014^{+0.001}_{-0.001}$
J	φ2.36±0.03	$\phi 0.093^{+0.001}_{-0.002}$
K	φ2.3	φ0.091
L	φ1.57±0.03	$\phi 0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document Number	
	Japanese	English
μPD78098B Subseries User's Manual	U12761J	To be prepared
μPD78095B, 78096B, 78098B Data Sheet	U12735J	To be prepared
μPD78098B Data Sheet	U12777J	This document
78K/0 Series User's Manual - Instructions	U12326J	U12326E
78K/0 Series Instruction Application Table	U10903J	–
78K/0 Series Instruction Set	U10904J	–
μPD78098B Subseries Special Function Register Application Table	To be prepared	–

Documents Related to Development Tools (User's Manual) (1/2)

Document Name		Document Number	
		Japanese	English
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		U12323J	EEU-1402
RA78K0 Assembler Package	Operation	U11802J	U11802E
	Language	U11801J	U11801E
	Structured Assembly Language	U11789J	U11789E
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K0 C Compiler	Operation	U11517J	U11517E
	Language	U11518J	U11518E
CC78K/0 C Compiler Application Note	Programming Know-how	EEA-618	EEA-1208
CC78K Series Library Source File		U12322J	–
PG-1500 PROM Programmer		U11940J	EEU-1335
PG-1500 Controller PC-9800 Series (MS-DOS) base		EEU-704	EEU-1291
PG-1500 Controller IBM PC Series (PC DOS) base		EEU-5008	U10540E
IE-78000-R		U11376J	U11376E
IE-78000-R-A		U10057J	U10057E
IE-78098-R-BK		EEU-867	EEU-1427
IE-78098-R-EM		To be prepared	To be prepared
EP-78230		EEU-985	EEU-1515
SM78K0 System Simulator - Windows base	Reference	U10181J	U10181E
SM78K Series System Simulator	External Parts User Open Interface Specification	U10092J	U10092E

Caution The contents of the above documents are subject to change without notice. Be sure to use the latest edition for designing.

Documents Related to Development Tools (User's Manual) (2/2)

Document Name		Document Number	
		Japanese	English
ID78K0 Integrated Debugger EWS Base	Reference	U11151J	—
ID78K0 Integrated Debugger PC Base	Reference	U11539J	U11539E
ID78K0 Integrated Debugger Windows Base	Guide	U11649J	U11649E
SD78K/0 Screen Debugger	Introduction	EEU-852	—
PC-9800 Series (MS-DOS) Base	Reference	U10952J	—
SD78K/0 Screen Debugger	Introduction	EEU-5024	U10539E
IBM PC/AT (PC DOS) Base	Reference	U11279J	U11279E

Documents Related to Embedded Software (User's Manual)

Document Name		Document Number	
		Japanese	English
78K/0 Series Real-Time OS	Fundamental	U11537J	U11537E
	Installation	U11536J	U11536E
78K/0 Seies OS MX78K0	Fundamental	U12257J	U12257E
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System - Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System - Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System - Fuzzy Inference Debugger		EEU-921	EEU-1458

Others

Document Name	Document Number	
	Japanese	English
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	–
Guide to Quality Assurance for Semiconductor Devices	C11893J	MEI-1202
Microcomputer Product Series Guide - Third Party Products -	U11416J	–

Caution The contents of the above documents are subject to change without notice. Be sure to use the latest edition for designing.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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