DATA SHEET

MOS INTEGRATED CIRCUIT

μPD78P083

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78P083 is a member of the μPD78083 subseries of the 78K/0 series products. It includes an on-chip, 24-Kbyte, one-time PROM or EPROM.

Because this device can be programmed by users, it is ideally suited for applications involving the evaluation of systems in development stages, small-scale production of many different products, and rapid development and time-to-market of a new product.

Caution The μPD78P083DU does not maintain planned reliability when used in your systems' mass-produced products. Please use only experimentally or for evaluation purposes during trial manufacture.

The details of functions are described in the user's manuals. Be sure to read the following manuals before designing.

μPD78083 Subseries User's Manual : IEU-1407
78K/0 Series User's Manual — Instructions : IEU-1372

FEATURES

- Pin-compatible with mask ROM version (except V_{PP} pin)
- Internal PROM: 24 Kbytes Note
  - μPD78P083DU: Reprogrammable (ideally suited for system evaluation)
  - μPD78P083CU, μPD78P083GB: One-time programmable (ideally suited for small-scale production)
- Internal high-speed RAM: 512 bytes Note
- Can be operated in the same supply voltage as the mask ROM version (V_{DD} = 1.8 to 5.5 V)
- Corresponding to QTOP™ Microcontrollers

Note The internal PROM and internal high-speed RAM capacities can be changed by setting the internal memory size switching register (IMS).

Remark QTOP microcontroller is a general term for microcontrollers which incorporate one-time PROM and are totally supported by NEC's programming service (from programming to marking, screening and verification). *

Differs from the mask ROM version in the following points
The same memory mapping as the mask ROM version is enabled by setting the internal memory size switching register (IMS).

In this document, the term PROM is used in parts common to one-time PROM versions and EPROM versions.

The information in this document is subject to change without notice.

Document No. U11006EJ1V0DS00 (1st edition)
(Previous No. IP-3556)
Date Published June 1996 P
Printed in Japan

The mark * shows major revised points.

ORDERING INFORMATION

Part Number	Package	Internal ROM
μPD78P083CU	42-pin plastic shrink DIP (600 mil)	One-Time PROM
μPD78P083GB-3B4	44-pin plastic QFP (10 x 10 mm)	One-Time PROM
* μPD78P083GB-3BS-MTX	44-pin plastic QFP (10 x 10 mm)	One-Time PROM
μPD78P083DU	42-pin ceramic shrink DIP (with window) (600 mil)	EPROM

Caution μPD78P083GB has two kinds of package. (Refer to 9. PACKAGE DRAWINGS). Please refer an NEC's sales representative for the available package.

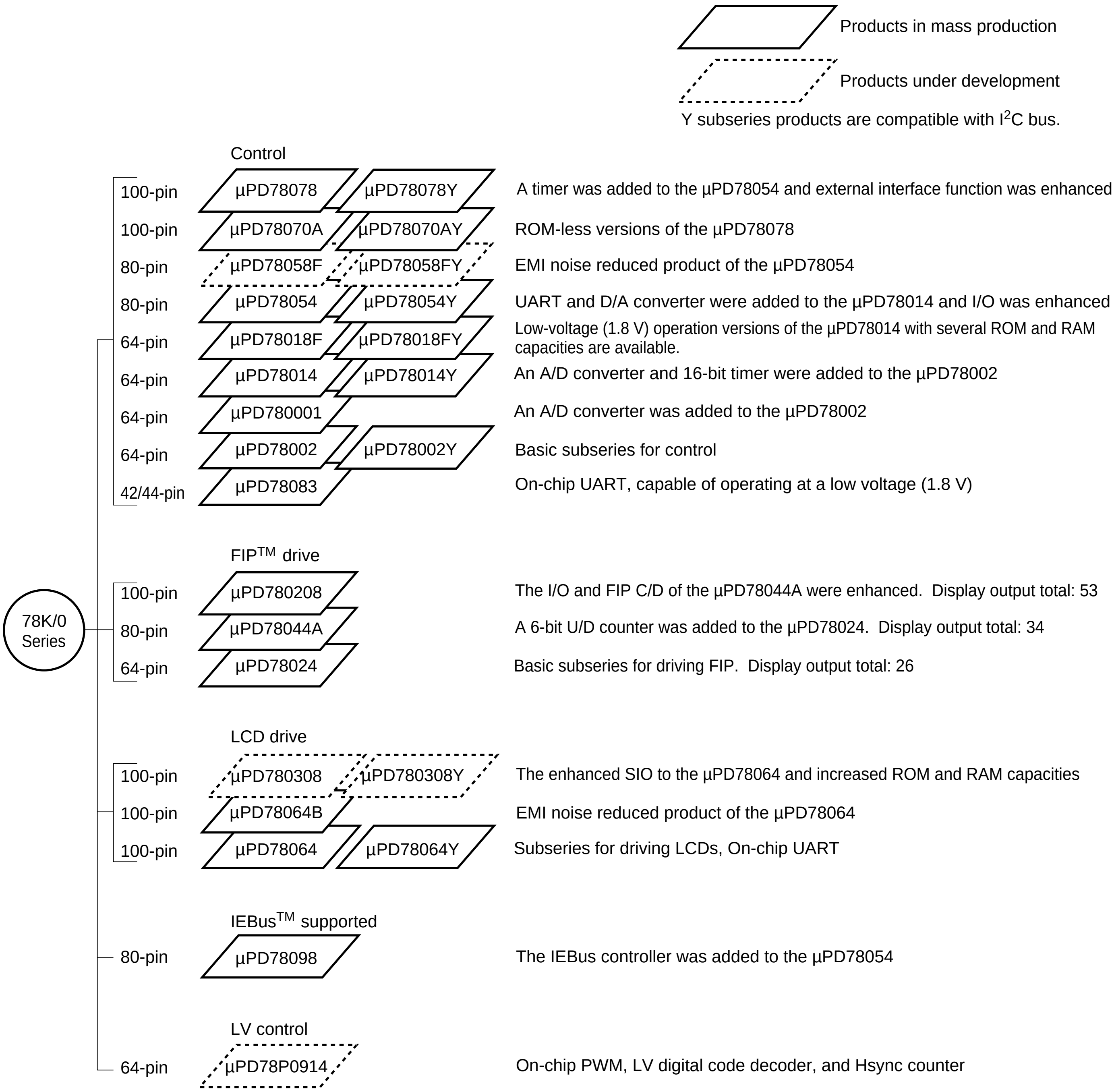
QUALITY GRADE

Part Number	Package	Quality Grades
μPD78P083CU	42-pin plastic shrink DIP (600 mil)	Standard
μPD78P083GB-3B4	44-pin plastic QFP (10 x 10 mm)	Standard
μPD78P083GB-3BS-MTX	44-pin plastic QFP (10 x 10 mm)	Standard
μPD78P083DU	42-pin ceramic shrink DIP (with window) (600 mil)	Not applicable

Please refer to “Quality grades on NEC Semiconductor Devices” (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

78K/0 SERIES DEVELOPMENT

The following shows the 78K/0 series products development. Subseries names are shown inside frames.



The following table shows the differences among subseries functions.

Function / Part Number		ROM Capacity	Timer				8-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-bit	16-bit	Watch	WDT						
Control	μPD78078	32 K to 60 K	4ch	1ch	1ch	1ch	8ch	2ch	3ch (UART: 1ch)	88	1.8 V	Available
	μPD78070A	–								61	2.7 V	
	μPD78058F	48 K to 60 K	2ch							69		
	μPD78054	16 K to 60 K									2.0 V	
	μPD78018F	8 K to 60 K						–	2ch	53	1.8 V	
	μPD78014	8 K to 32 K									2.7 V	
	μPD780001	8 K		–	–				1ch	39		–
	μPD78002	8 K to 16 K			1ch		–			53		Available
	μPD78083				–		8ch		1ch (UART: 1ch)	33	1.8 V	–
FIP drive	μPD780208	32 K to 60 K	2ch	1ch	1ch	1ch	8ch	–	2ch	74	2.7 V	–
	μPD78044A	16 K to 40 K								68		
	μPD78024	24 K to 32 K								54		
LCD drive	μPD780308	48 K to 60 K	2ch	1ch	1ch	1ch	8ch	–	3ch (UART: 1ch)	57	1.8 V	–
	μPD78064B	32 K							2ch (UART: 1ch)		2.0 V	
	μPD78064	16 K to 32 K										
IEBus supported	μPD78098	32 K to 60 K	2ch	1ch	1ch	1ch	8ch	2ch	3ch (UART: 1ch)	69	2.7 V	Available
LV control	μPD78P0914	32 K	6ch	–	–	1ch	8ch	–	2ch	54	4.5 V	Available

FUNCTION DESCRIPTION

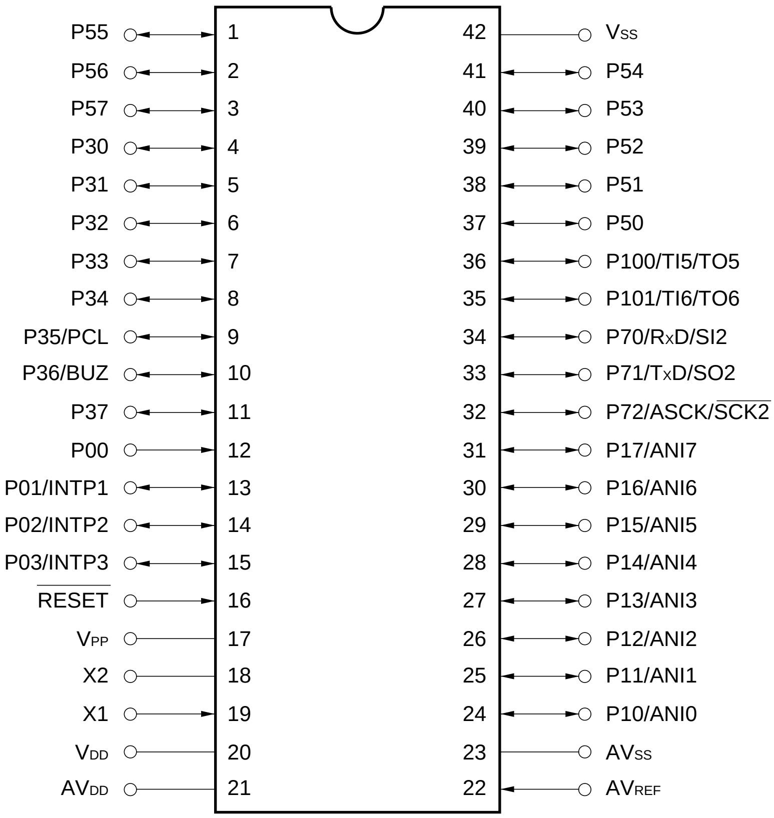
Item		Function
Internal memory		• PROM: 24 Kbytes Note • RAM Internal high-speed RAM: 512 bytes Note
Memory space		64 Kbytes
General register		8 bits x 32 registers (8 bits x 8 registers x 4 banks)
Instruction cycles		Instruction execution time variable function is integrated. 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (@5.0-MHz operation with main system clock)
Instruction set		• 16-bit operation • Multiply/divide (8 bits x 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjust, etc.
I/O ports		Total : 33 • CMOS input : 1 • CMOS input/output : 32
A/D converter		• 8-bit resolution x 8 channels
Serial interface		• 3-wire serial I/O/UART mode selectable: 1 channel
Timer		• 8-bit timer/event counter: 2 channels • Watchdog timer: 1 channel
Timer output		2 pins (8-bit PWM output enable)
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, and 5.0 MHz (@ 5.0-MHz operation with main system clock)
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, and 9.8 kHz (@ 5.0-MHz operation with main system clock)
Vectored interrupts	Maskable interrupts	Internal : 8 external : 3
	Non-maskable interrupt	Internal : 1
	Software interrupt	Internal : 1
Power supply voltage		V_{DD} = 1.8 to 5.5 V
Operating ambient temperature		T_A = –40 to +85°C
Packages		• 42-pin plastic shrink DIP (600 mil) • 44-pin plastic QFP (10 x 10 mm) • 42-pin ceramic shrink DIP (with window) (600 mil)

Note Internal PROM and high-speed RAM capacities can be changed by setting the internal memory size switching register (IMS).

PIN CONFIGURATIONS (Top View)

(1) Normal operating mode

- 42-pin plastic shrink DIP (600 mil) μPD78P083CU
- 42-pin ceramic shrink DIP (with window) (600 mil) μPD78P083DU

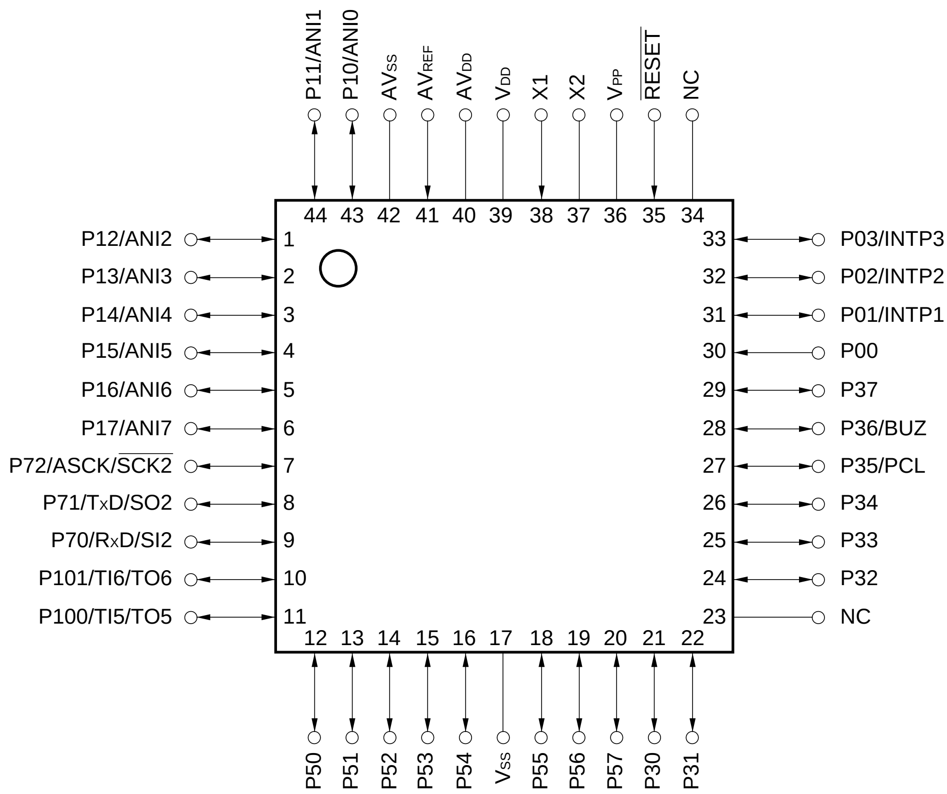


Cautions 1. Connect V_{PP} pin directly to V_{SS}.

2. Connect AV_{DD} pin to V_{DD}.

3. Connect AV_{SS} pin to V_{SS}.

- 44-pin plastic QFP (10 x 10 mm)
  μPD78P083GB-3B4, μPD78P083GB-3BS-MTX



Cautions 1. Connect V_{PP} pin directly to V_{SS}.

2. Connect AV_{DD} pin to V_{DD}.

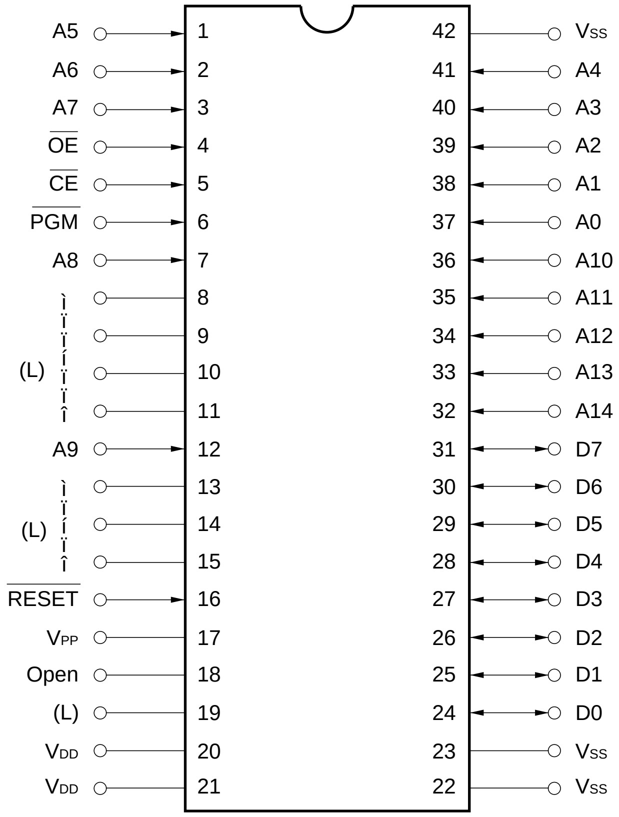
3. Connect AV_{SS} pin to V_{SS}.

4. Connect NC pin to V_{SS} for noise protection (It can be left open).

P00 to P03	:	Port 0
P10 to P17	:	Port 1
P30 to P37	:	Port 3
P50 to P57	:	Port 5
P70 to P72	:	Port 7
P100, P101	:	Port 10
INTP1 to INTP3	:	Interrupt from Peripherals
TI5, TI6	:	Timer Input
TO5, TO6	:	Timer Output
SI2	:	Serial Input
SO2	:	Serial Output
$\overline{\text{SCK2}}$	:	Serial Clock
RxD	:	Receive Data
TxD	:	Transmit Data
ASCK	:	Asynchronous Serial Clock
PCL	:	Programmable Clock
BUZ	:	Buzzer Clock
X1, X2	:	Crystal (Main System Clock)
$\overline{\text{RESET}}$	:	Reset
ANI0-ANI7	:	Analog Input
AV_{DD}	:	Analog Power Supply
AV_{SS}	:	Analog Ground
AV_{REF}	:	Analog Reference Voltage
V_{DD}	:	Power Supply
V_{PP}	:	Programming Power Supply
V_{SS}	:	Ground
NC	:	Non-connection

(2) PROM programming mode

- 42-pin plastic shrink DIP (600 mil) μPD78P083CU
- 42-pin ceramic shrink DIP (with window) (600 mil) μPD78P083DU



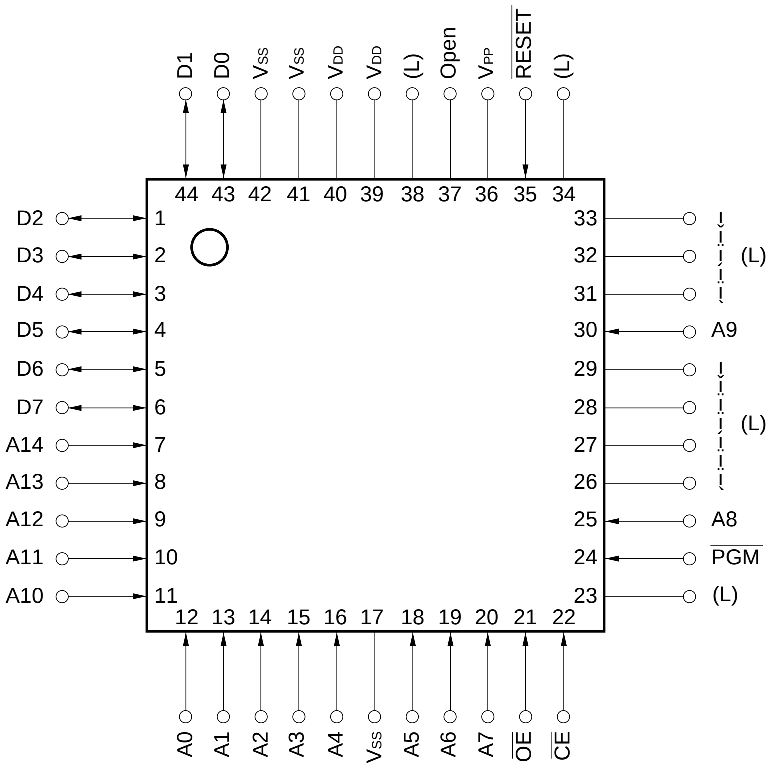
Cautions 1. (L): Individually connect to V_{SS} via a pull-down resistor.

2. V_{SS}: Connect to GND.

3. $\overline{RESET}$: Set to low level.

4. Open: Leave open.

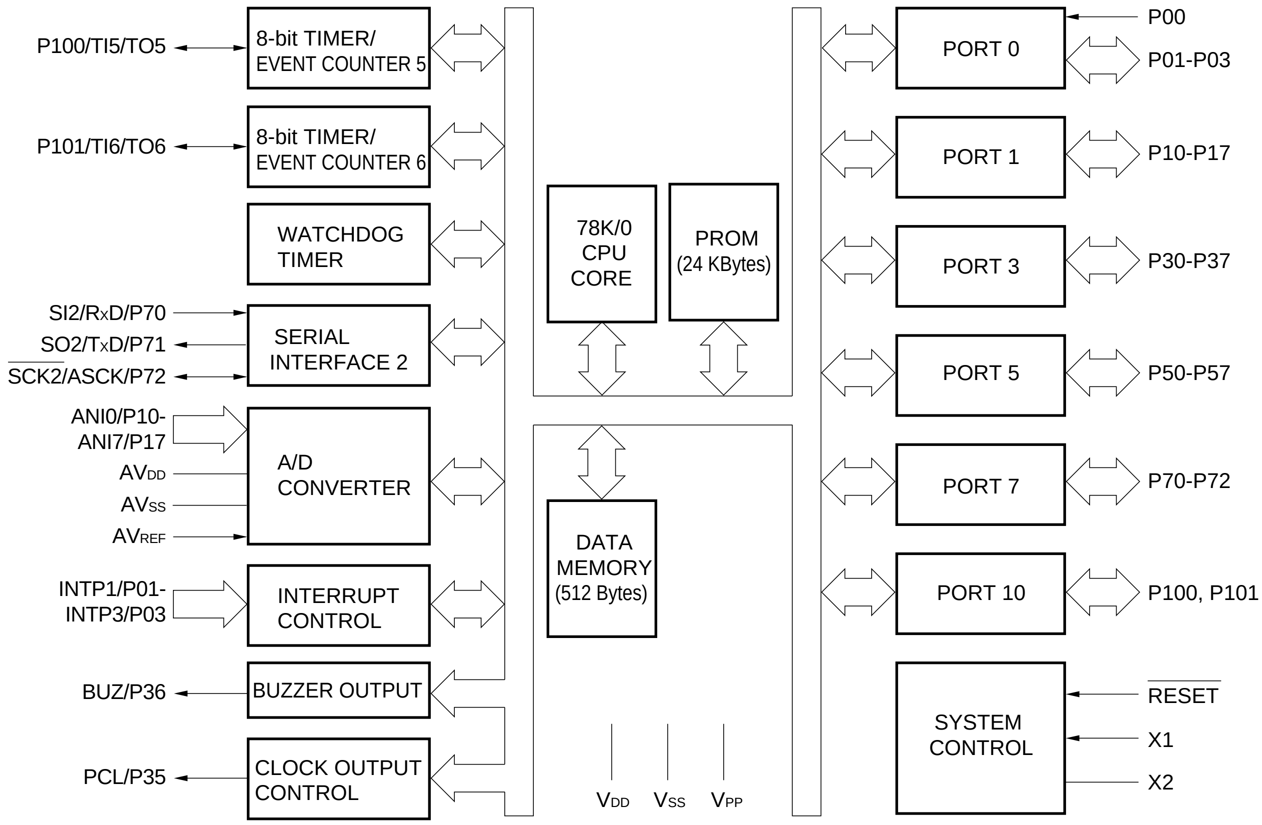
• 44-pin plastic QFP (10 x 10 mm)
μPD78P083GB-3B4, μPD78P083GB-3BS-MTX



Cautions 1. (L): Individually connect to V_{SS} via a pull-down resistor.
2. V_{SS}: Connect to GND.
3. RESET: Set to low level.
4. Open: Leave open.

A0 to A14	:	Address Bus	RESET	:	Reset
D0 to D7	:	Data Bus	V_{DD}	:	Power Supply
CE	:	Chip Enable	V_{PP}	:	Programming Power Supply
OE	:	Output Enable	V_{SS}	:	Ground
PGM	:	Program			

BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN THE μPD78P083 AND MASK ROM VERSIONS

The μPD78P083 is a single-chip microcontroller with an on-chip one-time PROM or with an on-chip EPROM which has program write, erasure and rewrite capability.

Setting the internal memory size switching register (IMS) makes the functions except the PROM specification identical to the mask ROM versions, that is, the μPD78081 and μPD78082.

Differences between the μPD78P083 and mask ROM versions are shown in Table 1-1.

Table 1-1. Differences between the μPD78P083 and Mask ROM Versions

Parameter	μPD78P083	Mask ROM Versions
ROM type	One-time PROM/EPROM	Mask ROM
ROM capacity	24 Kbytes	μPD78081 : 8 Kbytes μPD78082 : 16 Kbytes
Internal high-speed RAM capacity	512 bytes	μPD78081 : 256 bytes μPD78082 : 384 bytes
Internal ROM and internal high-speed RAM capacity change by internal memory size switching register	Can be changed Note	Can not be changed
IC pin	No	Yes
V_{PP} pin	Yes	No
Electrical specifications	Refer to a data sheet of each product	

Note The internal PROM becomes 24 Kbytes and the internal expansion RAM becomes 512 bytes by the $\overline{\text{RESET}}$ input.

2. PIN FUNCTIONS

2.1 Pins in Normal Operating Mode

(1) Port pins

Pin Name	Input/Output	Function		After Reset	Alternate Function
P00	Input	Port 0 4-bit input/output port	Input only	Input	—
P01	Input/output		Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.	Input	INTP1
P02					INTP2
P03					INTP3
P10-P17	Input/output	Port 1 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software. Note		Input	ANI0-ANI7
P30-P34	Input/output	Port 3 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.		Input	—
P35					PCL
P36					BUZ
P37					—
P50-P57	Input/output	Port 5 8-bit input/output port Can drive up to seven LEDs directly. Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.		Input	—
P70	Input/output	Port 7 3-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.		Input	SI2/RxD
P71					SO2/TxD
P72					$\overline{SCK2}$/ASCK
P100	Input/output	Port 10 2-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect a pull-up resistor by software.		Input	TI5/TO5
P101					TI6/TO6

Note When P10/ANI0-P17/ANI7 pins are used as the analog inputs for the A/D converter, set the port 1 to the input mode. The on-chip pull-up resistor is automatically disabled.

(2) Non-port pins

Pin Name	Input/Output	Function	After Reset	Alternate Function
INTP1	Input	External interrupt input by which the active edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P01
INTP2				P02
INTP3				P03
SI2	Input	Serial interface serial data input.	Input	P70/RxD
SO2	Output	Serial interface serial data output.	Input	P71/TxD
$\overline{SCK2}$	Input/Output	Serial interface serial clock input/output.	Input	P72/ASCK
RxD	Input	Asynchronous serial interface serial data input.	Input	P70/SI2
TxD	Output	Asynchronous serial interface serial data output.	Input	P71/SO2
ASCK	Input	Asynchronous serial interface serial clock input.	Input	P72/$\overline{SCK2}$
TI5	Input	External count clock input to 8-bit timer (TM5).	Input	P100/TO5
TI6		External count clock input to 8-bit timer (TM6).		P101/TO6
TO5	Output	8-bit timer output.	Input	P100/TI5
TO6				P101/TI6
PCL	Output	Clock output. (for main system clock trimming)	Input	P35
BUZ	Output	Buzzer output.	Input	P36
ANI0-ANI7	Input	A/D converter analog input.	Input	P10-P17
AV_{REF}	Input	A/D converter reference voltage input.	–	–
AV_{DD}	–	A/D converter analog power supply. Connected to V_{DD}.	–	–
AV_{SS}	–	A/D converter ground potential. Connected to V_{SS}.	–	–
$\overline{RESET}$	Input	System reset input.	–	–
X1	Input	Main system clock oscillation crystal connection.	–	–
X2	–		–	–
V_{DD}	–	Positive power supply.	–	–
V_{PP}	–	High-voltage applied during program write/verification. Connected directly to V_{SS} in normal operating mode.	–	–
V_{SS}	–	Ground potential.	–	–
NC	–	Does not internally connected. Connect to V_{SS}. (It can be left open)	–	–

2.2 Pins in PROM Programming Mode

Pin Name	Input/Output	Function
$\overline{\text{RESET}}$	Input	PROM programming mode setting When +5 V or +12.5 V is applied to the V_{PP} pin and a low-level signal is applied to the $\overline{\text{RESET}}$ pin, this chip is set in the PROM programming mode.
V_{PP}	Input	PROM programming mode setting and high-voltage applied during program write/verification.
A0-A14	Input	Address bus
D0-D7	Input/output	Data bus
$\overline{\text{CE}}$	Input	PROM enable input/program pulse input
$\overline{\text{OE}}$	Input	Read strobe input to PROM
$\overline{\text{PGM}}$	Input	Program/program inhibit input in PROM programming mode.
V_{DD}	—	Positive power supply
V_{SS}	—	Ground potential

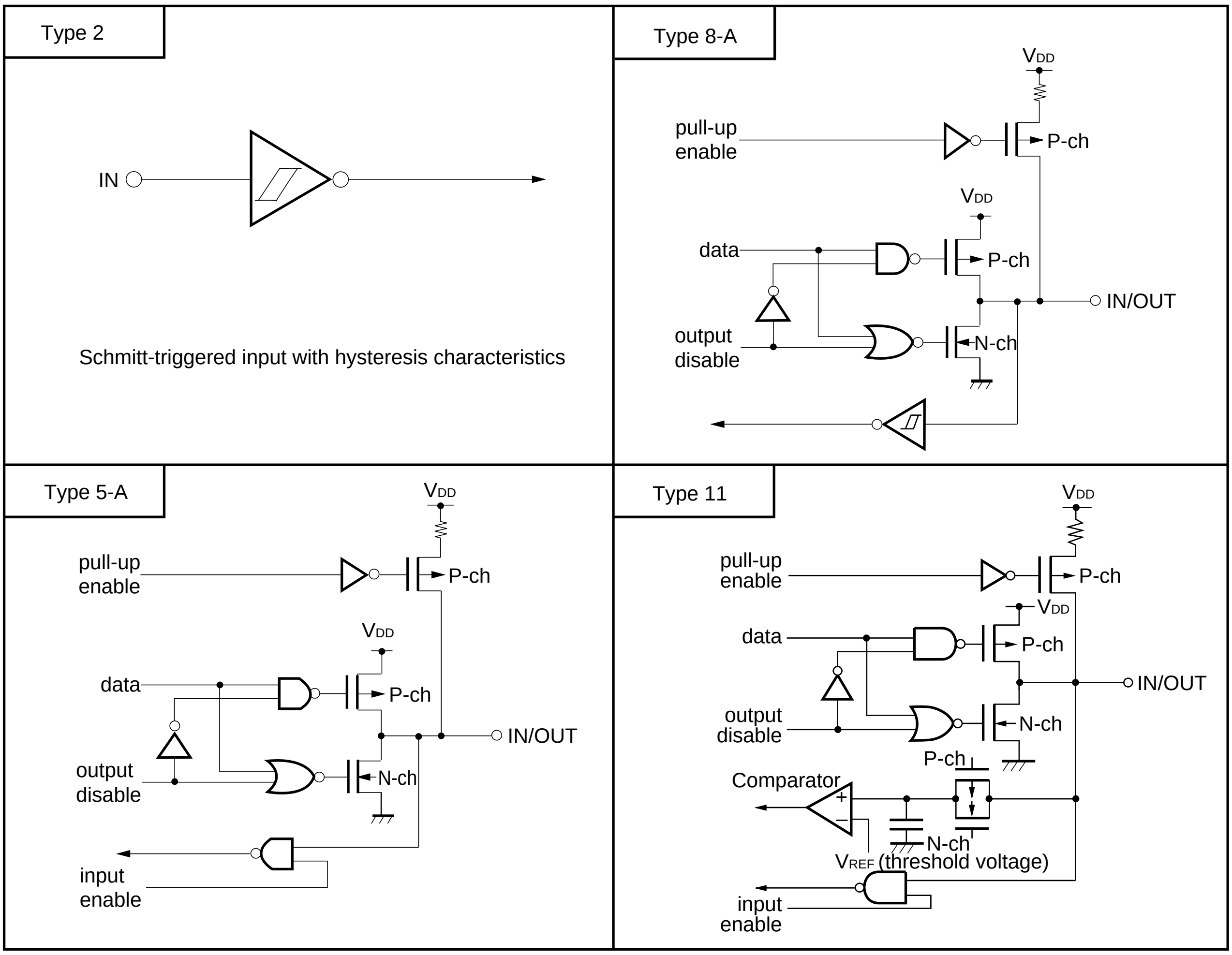
2.3 Pin Input/Output Circuits and Recommended Connection of Unused Pins

Types of input/output circuits of the pins and recommeded connection of unused pins are shown in Table 2-1.
For the configuration of each type of input/output circuit, see Figure 2-1.

Table 2-1. Type of Input/Output Circuit of Each Pin

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connection for Unused Pins
P00	2	Input	Connect to V_{SS}.
P01/INTP1	8-A	Input/Output	Independently connect to V_{SS} via a resistor.
P02/INTP2			
P03/INTP3			
P10/ANI0-P17/ANI7	11	Input/Output	Independently connect to V_{DD} or V_{SS} via a resistor.
P30-P32	5-A		
P33, P34	8-A		
P35/PCL	5-A		
P36/BUZ			
P37			
P50-P57	5-A		
P70/SI2/RxD	8-A		
P71/SO2/TxD	5-A		
P72/$\overline{\text{SCK2}}$/ASCK	8-A		
P100/TI5/TO5	8-A		
P101/TI6/TO6			
$\overline{\text{RESET}}$	2	Input	–
AV_{REF}	–	–	Connect to V_{SS}.
AV_{DD}			Connect to V_{DD}.
AV_{SS}			Connect to V_{SS}.
V_{PP}			Connect directly to V_{SS}.
NC			Connect to V_{SS} (can leave open)

Figure 2-1. Types of Pin Input/Output Circuits



3. INTERNAL MEMORY SIZE SWITCHING REGISTER (IMS)

This is a register to disable use of part of internal memories by software. By setting this internal memory size switching register (IMS), it is possible to get the same memory mapping as that of the mask ROM versions with a different internal memory (ROM, RAM).

IMS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets IMS to 46H.

Figure 3-1. Internal Memory Size Switching Register Format

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	46H	R/W

ROM3	ROM2	ROM1	ROM0	Selection of Internal ROM Capacity
0	0	1	0	8 Kbytes
0	1	0	0	16 Kbytes
0	1	1	0	24 Kbytes
Other than above				Setting prohibited

RAM2	RAM1	RAM0	Selection of Internal High-Speed RAM Capacity
0	1	0	512 bytes
0	1	1	384 bytes
1	0	0	256 bytes
Other than above			Setting prohibited

Table 3-1 shows the setting values of IMS which make the memory mapping the same as that of the mask ROM version.

Table 3-1. Internal Memory Size Switching Register Setting Values

Target Mask ROM Versions	IMS Setting Value
μPD78081	82H
μPD78082	64H

4. PROM PROGRAMMING

The μPD78P083 has an internal 24-Kbyte PROM as a program memory. For programming, set the PROM programming mode with the V_{PP} and $\overline{\text{RESET}}$ pins. For the connection of unused pins, refer to **"PIN CONFIGURATIONS (TOP VIEW) (2) PROM programming mode."**

Caution Programs must be written in addresses 0000H to 5FFFH (The last address 5FFFH must be specified). They cannot be written by a PROM programmer which cannot specify the write address.

4.1 Operating Modes

When +5 V or +12.5 V is applied to the V_{PP} pin and a low-level signal is applied to the $\overline{\text{RESET}}$ pin, the PROM programming mode is set. This mode will become the operating mode as shown in Table 4-1 when the $\overline{\text{CE}}$, $\overline{\text{OE}}$, and $\overline{\text{PGM}}$ pins are set as shown.

Further, when the read mode is set, it is possible to read the contents of the PROM.

Table 4-1. Operating Modes of PROM Programming

Operating Mode \ Pin	$\overline{\text{RESET}}$	V_{PP}	V_{DD}	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{PGM}}$	D0 to D7
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High-impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				x	H	H	High-impedance
				x	L	L	
Read		+5 V	+5 V	L	L	H	Data output
Output disable				L	H	x	High-impedance
Standby				H	x	x	High-impedance

x : L or H

(1) Read mode

Read mode is set if $\overline{CE}$ = L, $\overline{OE}$ = L is set.

(2) Output disable mode

Data output becomes high-impedance, and is in the output disable mode, if $\overline{OE}$ = H is set.

Therefore, it allows data to be read from any device by controlling the $\overline{OE}$ pin, if multiple μPD78P083s are connected to the data bus.

(3) Standby mode

Standby mode is set if $\overline{CE}$ = H is set.

In this mode, data outputs become high-impedance irrespective of the $\overline{OE}$ status.

(4) Page data latch mode

Page data latch mode is set if $\overline{CE}$ = H, $\overline{PGM}$ = H, $\overline{OE}$ = L are set at the beginning of page write mode.

In this mode, 1 page 4-byte data is latched in an internal address/data latch circuit.

(5) Page write mode

After 1 page 4 bytes of addresses and data are latched in the page data latch mode, a page write is executed by applying a 0.1-ms program pulse (active low) to the $\overline{PGM}$ pin with $\overline{CE}$ = H, $\overline{OE}$ = H. Then, program verification can be performed, if $\overline{CE}$ = L, $\overline{OE}$ = L are set.

If programming is not performed by a one-time program pulse, X times (X - 10) write and verification operations should be executed repeatedly.

(6) Byte write mode

Byte write is executed when a 0.1-ms program pulse (active low) is applied to the $\overline{PGM}$ pin with $\overline{CE}$ = L, $\overline{OE}$ = H. Then, program verification can be performed if $\overline{OE}$ = L is set.

If programming is not performed by a one-time program pulse, X times (X - 10) write and verification operations should be executed repeatedly.

(7) Program verify mode

Program verify mode is set if $\overline{CE}$ = L, $\overline{PGM}$ = H, $\overline{OE}$ = L are set.

In this mode, check if a write operation is performed correctly after the write.

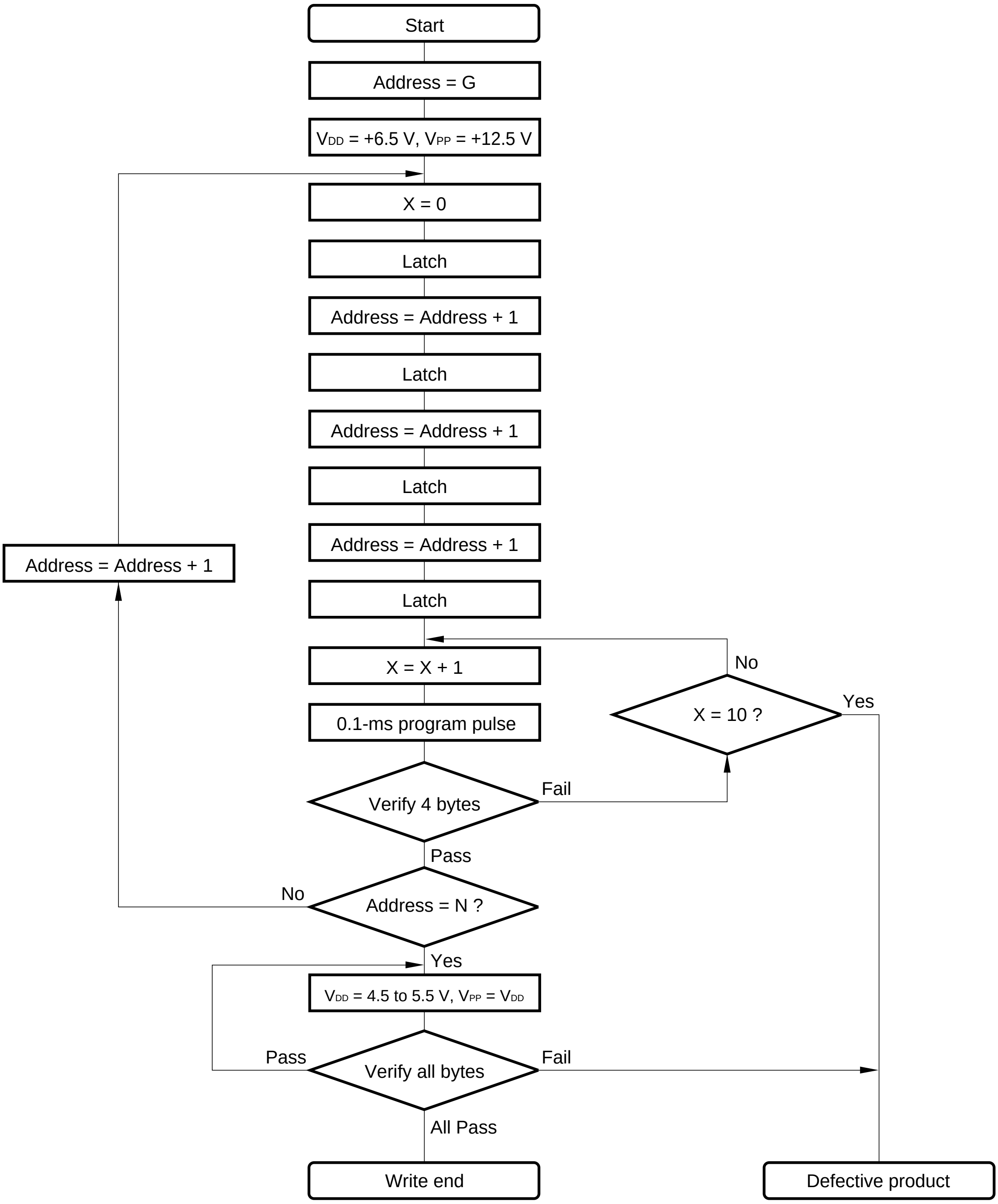
(8) Program inhibit mode

Program inhibit mode is used when the $\overline{OE}$ pin, V_{PP} pin, and D0-D7 pins of multiple μPD78P083s are connected in parallel and a write is performed to one of those devices.

When a write operation is performed, the page write mode or byte write mode described above is used. At this time, a write is not performed to a device which has the $\overline{PGM}$ pin driven high.

4.2 PROM Write Procedure

Figure 4-1. Page Program Mode Flow Chart



G = Start address

N = Program last address

Figure 4-2. Page Program Mode Timing

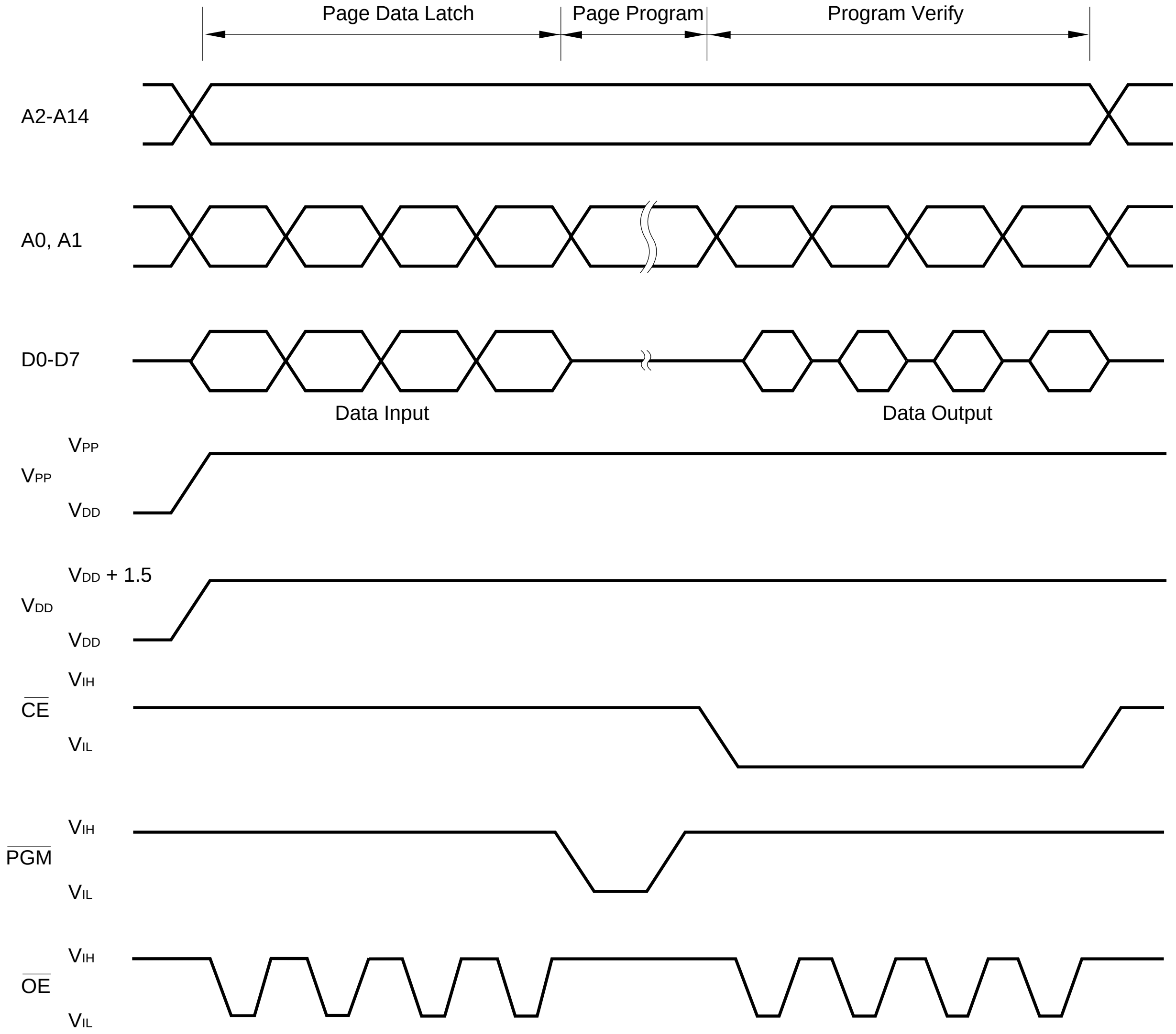
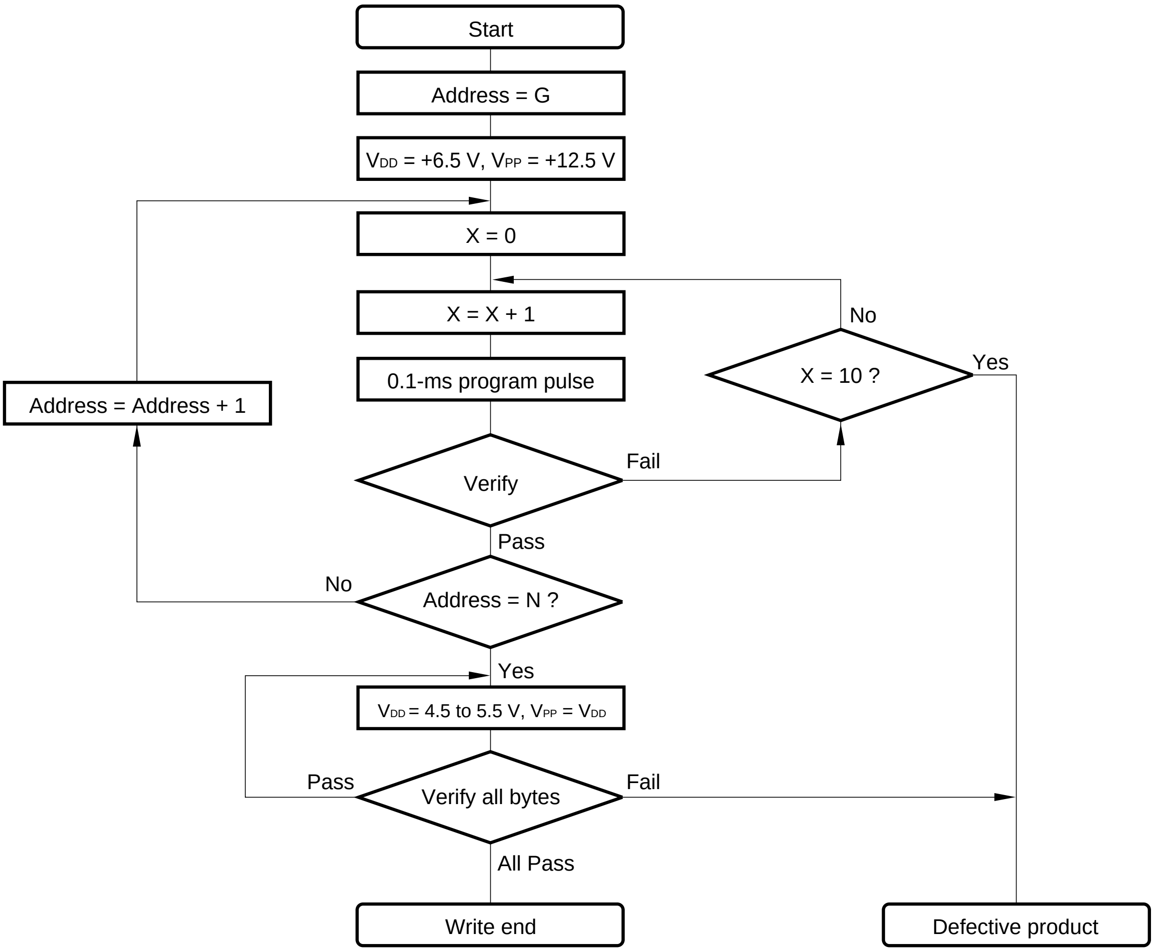
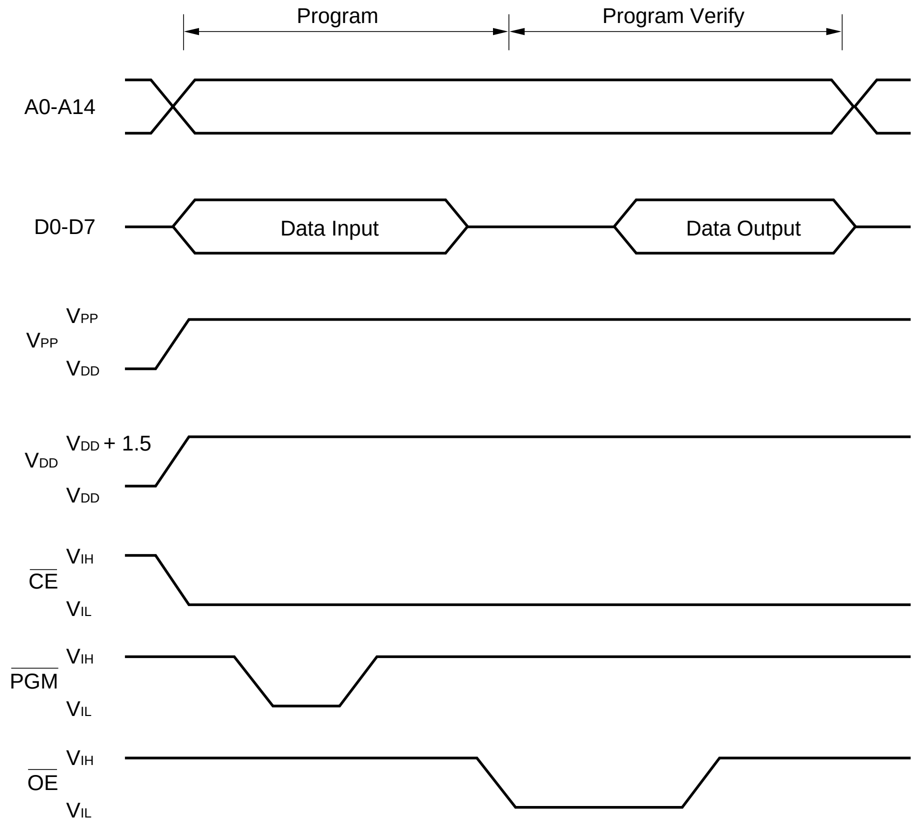


Figure 4-3. Byte Program Mode Flow Chart



G = Start address
N = Program last address

Figure 4-4. Byte Program Mode Timing



Cautions
1. **V_{DD} should be applied before V_{PP} and removed after V_{PP}.**
2. **V_{PP} must not exceed +13.5 V including overshoot.**
3. **Reliability may be adversely affected if removal/reinsertion is performed while +12.5 V is being applied to V_{PP}.**

4.3 PROM Read Procedure

The contents of PROM are readable to the external data bus (D0-D7) according to the read procedure shown below.

(1) Fix the $\overline{RESET}$ pin at low level, supply +5 V to the V_{PP} pin, and connect all other unused pins as shown in **"PIN CONFIGURATIONS (TOP VIEW) (2) PROM programming mode".**

(2) Supply +5 V to the V_{DD} and V_{PP} pins.

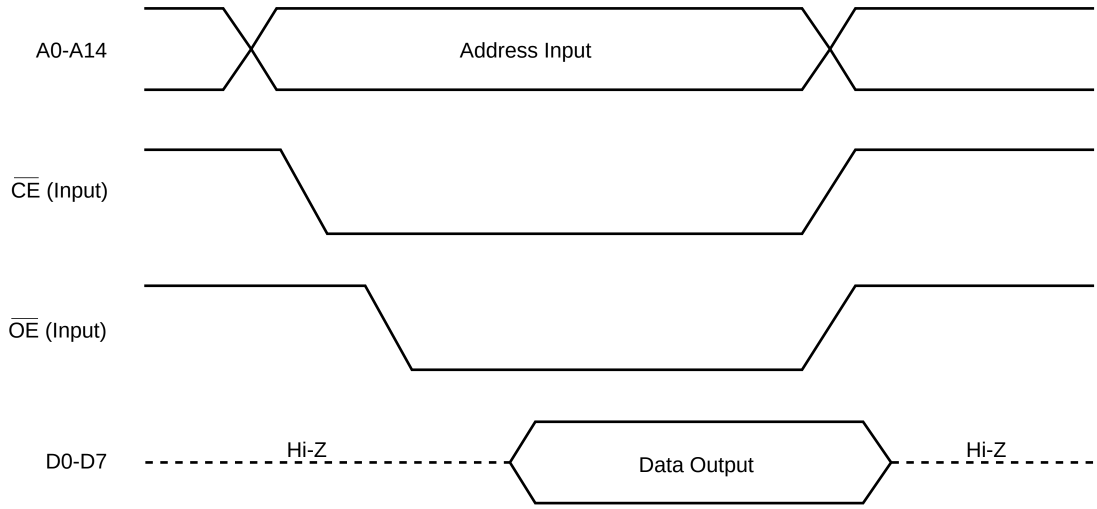
(3) Input address of read data into the A0-A16 pins.

(4) Read mode

(5) Output data to D0-D7 pins.

The timings of the above steps (2) to (5) are shown in Figure 4-5.

Figure 4-5. PROM Read Timings



* **5. PROGRAM ERASURE (μPD78P083DU ONLY)**

The μPD78P083DU is capable of erasing (FFH) the data written in a program memory and rewriting.

To erase the programmed data, expose the erasure window to light having a wavelength shorter than about 400 nm. Normally, irradiate ultraviolet rays of 254-nm wavelength. The amount of exposure required to completely erase the programmed data is as follows:

- UV intensity x erasing time : 30 W•s/cm^2 or more
- Erasure time: 40 min. or more (When a UV lamp of 12,000μW/cm^2 is used. However, a longer time may be needed because of deterioration in performance of the UV lamp, soiled erasure window, etc.)

When erasing the contents of data, set up the UV lamp within 2.5 cm from the erasure window. Further, if a filter is provided for a UV lamp, irradiate the ultraviolet rays after removing the filter.

6. OPAQUE FILM ON ERASURE WINDOW (μPD78P083DU ONLY)

To protect from unintentional erasure by rays other than that of the lamp for erasing EPROM contents, or to protect internal circuit other than EPROM from misoperating by rays, cover the erasure window with an opaque film when EPROM contents erasure is not performed.

7. ONE-TIME PROM VERSION SCREENING

The one-time PROM version (μPD78P083CU, 78P083GB-3B4, 78P083GB-3BS-MTX) cannot be tested completely by NEC before it is shipped, because of its structure. It is recommended to perform screening to verify PROM after writing necessary data and performing high-temperature storage under the condition below.

Storage Temperature	Storage Time
125°C	24 hours

* NEC offers for an additional fee one-time PROM writing to marking, screening, and verify for products designated as "QTOP Microcontroller". Please contact an NEC sales representative for details.

8. ELECTRICAL SPECIFICATIONS

*

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Test Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
	V_{PP}			–0.3 to +13.5	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{REF}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}			–0.3 to V_{DD} + 0.3	V
	V_{I2}	A9	PROM programming mode	–0.3 to +13.5	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10-P17	Analog input pins	AV_{SS} – 0.3 to AV_{REF} + 0.3	V
Output current, high	I_{OH}	Per pin		–10	mA
		Total for P10-P17, P50-P54, P70-P72, P100, P101		–15	mA
		Total for P01-P03, P30-P37, P55-P57		–15	mA
Output current, low	I_{OL} Note	Per pin	Peak value	30	mA
			r.m.s. value	15	mA
		Total for P50-P54	Peak value	100	mA
			r.m.s. value	70	mA
		Total for P55-P57	Peak value	100	mA
			r.m.s. value	70	mA
		Total for P10-P17, P70-P72, P100, P101	Peak value	50	mA
			r.m.s. value	20	mA
		Total for P01-P03, P30-P37	Peak value	50	mA
			r.m.s. value	20	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note The r.m.s. value should be calculated as follows: [r.m.s. value] = [Peak value] x $\sqrt{\text{Duty}}$

Caution If the absolute maximum rating of even one of the above parameters is exceeded, the quality of the product may be degraded. The absolute maximum ratings are therefore the rated values that may, if exceeded, physically damage the product. Be sure to use the product with all the absolute maximum ratings observed.

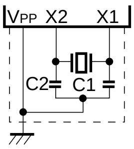
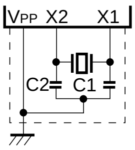
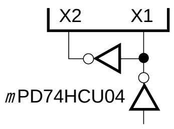
Remark Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz, Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C_{IO}	f = 1 MHz, Unmeasured pins returned to 0 V.	P01-P03, P10-P17, P30-P37, P50-P57, P70-P72, P100, P101			15	pF

Remark Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X) Note 1	V_{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time Note 2	After V_{DD} came to MIN. of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f_X) Note 1		1.0		5.0	MHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X) Note 1		1.0		5.0	MHz
		X1 input high- and low-level widths (t_{XH}, t_{XL})		85		500	ns

Notes 1. Only the oscillator characteristics are shown. For the instruction execution time, refer to **AC Characteristics**.

2. Time required for oscillation to stabilize after a reset or the STOP mode has been released.

Caution When using the oscillation circuit of the main system clock, wire the portion enclosed in broken lines in the figures as follows to avoid adverse influences on the wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring over other signal lines.**
- **Do not route the wiring in the vicinity of lines through which a high fluctuating current flows.**
- **Always keep the ground point of the capacitor of the oscillation circuit at the same potential as V_{SS}.**
- **Do not connect the power source pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10-P17, P30-P32, P35-P37, P50-P57, P71	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				0.8V_{DD}		V_{DD}	V
	V_{IH2}	P00-P03, P33, P34, P70, P72, P100, P101, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
				0.85V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2	V_{DD} = 2.7 to 5.5 V	V_{DD}–0.5		V_{DD}	V
				V_{DD}–0.2		V_{DD}	V
Input voltage, low	V_{IL1}	P10-P17, P30-P32, P35-P37, P50-P57, P71	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				0		0.2V_{DD}	V
	V_{IL2}	P00-P03, P33, P34, P70, P72, P100, P101, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
				0		0.15V_{DD}	V
	V_{IL3}	X1, X2	V_{DD} = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
Output voltage, high	V_{OH}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD}–1.0			V
		I_{OH} = –100 μA		V_{DD}–0.5			V
Output voltage, low	V_{OL}	P50-P57	V_{DD} = 2.0 to 4.5 V, I_{OL} = 10 mA			0.8	V
			V_{DD} = 4.5 to 5.5 V, I_{OL} = 15 mA		0.4	2.0	V
		P01-P03, P10-P17, P30-P37, P70-P72, P100, P101	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
			I_{OL} = 400 μA			0.5	V
Input-leak current, high	I_{LIH1}	V_{IN} = V_{DD}	P00-P03, P10-P17, P30-P37, P50-P57, P70-P72, P100, P101, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2			20	μA
Input-leak current, low	I_{LIL1}	V_{IN} = 0 V	P00-P03, P10-P17, P30-P37, P50-P57, P70-P72, P100, P101, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2			–20	μA
Output leak current, high	I_{LOH}	V_{OUT} = V_{DD}				3	μA
Output leak current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistor	R	V_{IN} = 0 V	P01-P03, P10-P17, P30-P37, P50-P57, P70-P72, P100, P101	15	40	90	k ý

Remark Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	5.0-MHz crystal oscillation operating mode (f_{XX} = 2.5 MHz) Note 2	V_{DD} = 5.0 V ± 10% Note 4		5.4	16.2	mA
			V_{DD} = 3.0 V ± 10% Note 5		0.8	2.4	mA
			V_{DD} = 2.0 V ± 10% Note 5		0.45	1.35	mA
		5.0-MHz crystal oscillation operating mode (f_{XX} = 5.0 MHz) Note 3	V_{DD} = 5.0 V ± 10% Note 4		9.5	28.5	mA
			V_{DD} = 3.0 V ± 10% Note 5		1.0	3.0	mA
	I_{DD2}	5.0-MHz crystal oscillation HALT mode (f_{XX} = 2.5 MHz) Note 2	V_{DD} = 5.0 V ± 10%		1.4	4.2	mA
			V_{DD} = 3.0 V ± 10%		0.5	1.5	mA
			V_{DD} = 2.0 V ± 10%		280	840	μA
		5.0-MHz crystal oscillation HALT mode (f_{XX} = 5.0 MHz) Note 3	V_{DD} = 5.0 V ± 10%		1.6	4.8	mA
			V_{DD} = 3.0 V ± 10%		0.65	1.95	mA
	I_{DD3}	STOP mode	V_{DD} = 5.0 V ± 10%		0.1	30	μA
			V_{DD} = 3.0 V ± 10%		0.05	10	μA
			V_{DD} = 2.0 V ± 10%		0.05	10	μA

Notes 1. Not including AV_{REF}, AV_{DD} currents or port currents (including current flowing into internal pull-up resistors).
2. $f_{XX} = f_X/2$ operation (when oscillation mode selection register (OSMS) is set to 00H).
3. $f_{XX} = f_X$ operation (when oscillation mode selection register (OSMS) is set to 01H).
4. High-speed mode operation (when processor clock control register (PCC) is set to 00H).
5. Low-speed mode operation (when processor clock control register (PCC) is set to 04H).

Remark f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency

AC Characteristics

(1) Basic Operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	$f_{XX} = f_X/2$ Note1	V_{DD} = 2.7 to 5.5 V	0.8		64	μs
				2.0		64	μs
		$f_{XX} = f_X$ Note2	3.5 V - V_{DD} - 5.5 V	0.4		32	μs
			2.7 V - V_{DD} < 3.5 V	0.8		32	μs
TI5, TI6 input frequency	f_{TI}	V_{DD} = 4.5 to 5.5 V		0		4	MHz
				0		275	kHz
TI5, TI6 input high-/low-level widths	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 5.5 V		100			ns
				1.8			μs
Interrupt input high-/low-level widths	t_{INTH}, t_{INTL}	V_{DD} = 2.7 to 5.5 V		10			μs
				20			μs
$\overline{RESET}$ low-level width	t_{RSL}	V_{DD} = 2.7 to 5.5 V		10			μs
				20			μs

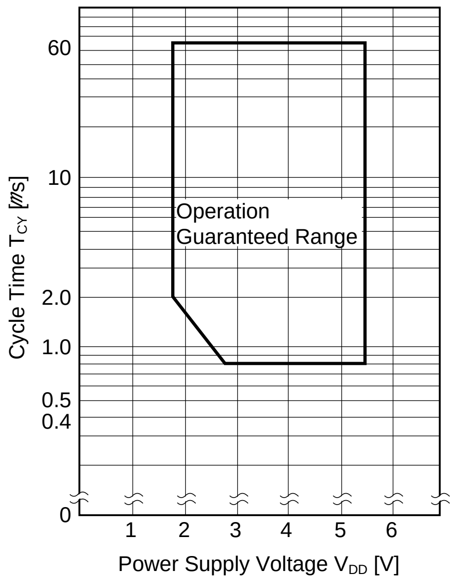
Notes 1. When oscillation mode selection register (OSMS) is set to 00H.

2. When OSMS is set to 01H.

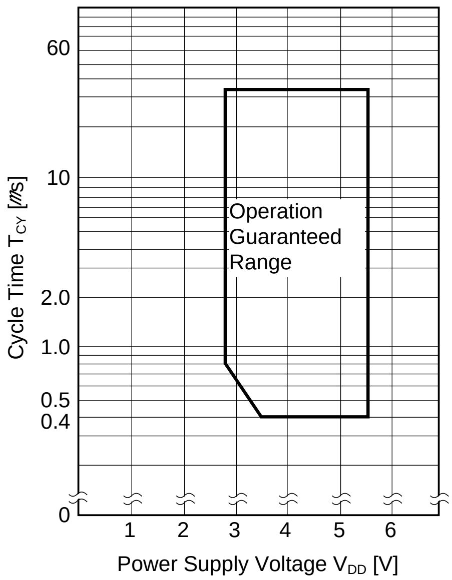
Remark f_{XX}: Main system clock frequency (f_X or $f_X/2$)

f_X: Main system clock oscillation frequency

T_{CY} vs V_{DD} (Main System Clock $f_{XX} = f_X/2$ Operation)



T_{CY} vs V_{DD} (Main System Clock $f_{XX} = f_X$ Operation)



(2) Serial Interface (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode ($\overline{SCK2}$ ··· internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY1}	4.5 V - V_{DD} - 5.5 V	800			ns
		2.7 V - V_{DD} < 4.5 V	1600			ns
		2.0 V - V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK2}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 4.5 to 5.5 V	t_{KCY1}/2–50			ns
			t_{KCY1}/2–100			ns
SI2 setup time (to $\overline{SCK2}$ ↑)	t_{SIK1}	4.5 V - V_{DD} - 5.5 V	100			ns
		2.7 V - V_{DD} < 4.5 V	150			ns
		2.0 V - V_{DD} < 2.7 V	300			ns
			400			ns
SI2 hold time (from $\overline{SCK2}$ ↑)	t_{KSI1}		400			ns
$\overline{SCK2}$ ↓ → SO2 output delay time	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the $\overline{SCK2}$, SO2 output line load capacitance.

(b) 3-wire serial I/O mode ($\overline{SCK2}$ ··· external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY2}	4.5 V - V_{DD} - 5.5 V	800			ns
		2.7 V - V_{DD} < 4.5 V	1600			ns
		2.0 V - V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK2}$ high-/low-level width	t_{KH2}, t_{KL2}	4.5 V - V_{DD} - 5.5 V	400			ns
		2.7 V - V_{DD} < 4.5 V	800			ns
		2.0 V - V_{DD} < 2.7 V	1600			ns
			2400			ns
SI2 setup time (to $\overline{SCK2}$ ↑)	t_{SIK2}	V_{DD} = 2.0 to 5.5 V	100			ns
			150			ns
SI2 hold time (from $\overline{SCK2}$ ↑)	t_{KSI2}		400			ns
$\overline{SCK2}$ ↓ → SO2 output delay time	t_{KSO2}	C = 100 pF[Note], V_{DD} = 2.0 to 5.5 V			300	ns
		C = 100 pF[Note]			500	ns
$\overline{SCK2}$ rise, fall time	t_{R2}, t_{F2}				1000	ns

Note C is the SO2 output line load capacitance.

(c) UART mode (Dedicated baud rate generator output)

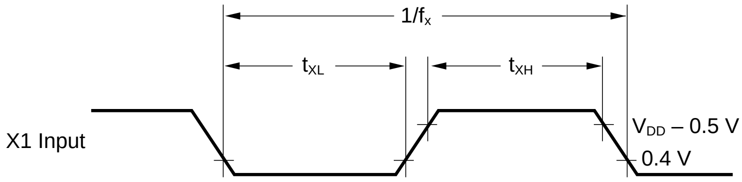
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.5 V - V_{DD} - 5.5 V			78125	bps
		2.7 V - V_{DD} < 4.5 V			39063	bps
		2.0 V - V_{DD} < 2.7 V			19531	bps
					9766	bps

(d) UART mode (External clock input)

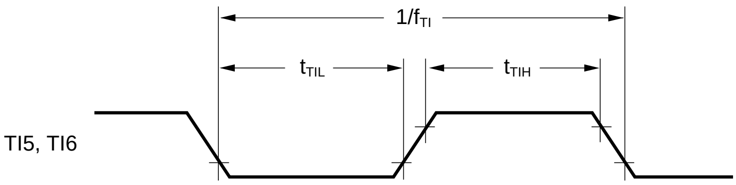
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY3}	4.5 V - V_{DD} - 5.5 V	800			ns
		2.7 V - V_{DD} < 4.5 V	1600			ns
		2.0 V - V_{DD} < 2.7 V	3200			ns
			4800			ns
ASCK high-/low-level width	t_{KH3},	4.5 V - V_{DD} - 5.5 V	400			ns
	t_{KL3}	2.7 V - V_{DD} < 4.5 V	800			ns
		2.0 V - V_{DD} < 2.7 V	1600			ns
			2400			ns
Transfer rate		4.5 V - V_{DD} - 5.5 V			39063	bps
		2.7 V - V_{DD} < 4.5 V			19531	bps
		2.0 V - V_{DD} < 2.7 V			9766	bps
					6510	bps
ASCK rise, fall time	t_{R3}, t_{F3}				1000	ns

AC Timing Test Point (Excluding X1 Input)

Clock Timing

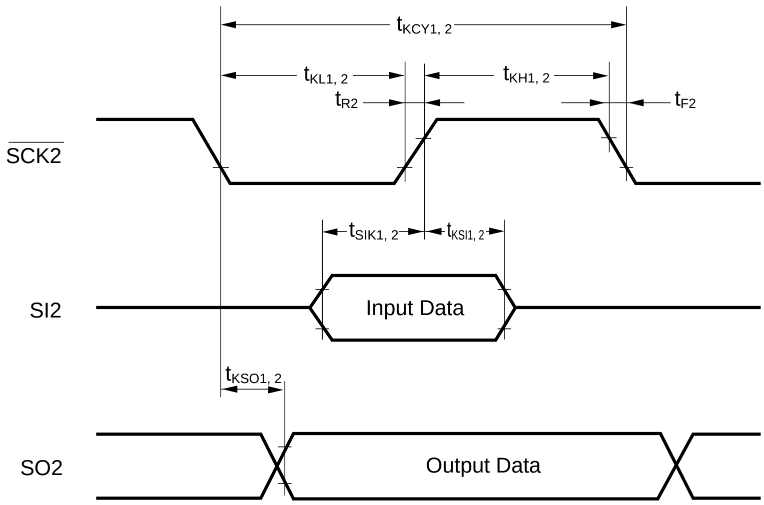


TI Timing

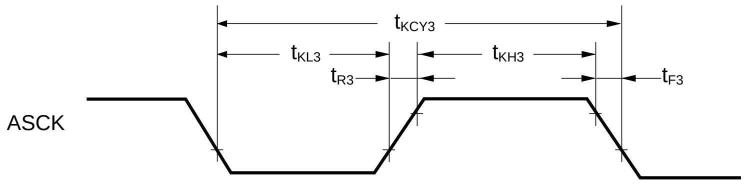


Serial Transfer Timing

3-wire serial I/O mode:



UART mode (external clock input):



A/D Converter Characteristics (T_A = –40 to +85°C, AV_{DD} = V_{DD} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Total error Note		2.7 V - AV_{REF} - AV_{DD}			1.4	%
Conversion time	t_{CONV}		19.1		200	µs
Sampling time	t_{SAMP}		$12/f_{xx}$			µs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		2.7		AV_{DD}	V
AV_{REF}-AV_{SS} resistance	R_{AIREF}		4	14		k ý

Note Excluding quantization error (±1/2 LSB). Shown as a percentage of the full scale value.

Remark f_{xx}: Main system clock frequency (f_x or $f_x/2$)
f_x: Main system clock oscillation frequency

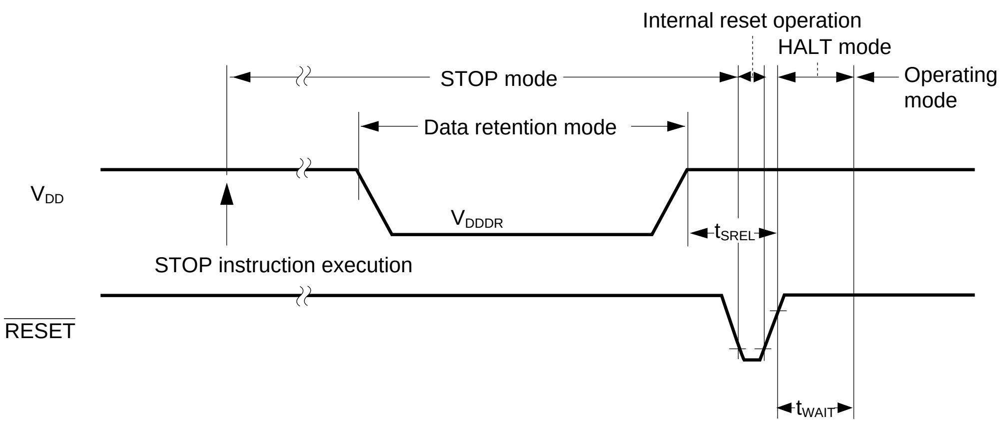
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8 V		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_x$		ms
		Release by interrupt		Note		ms

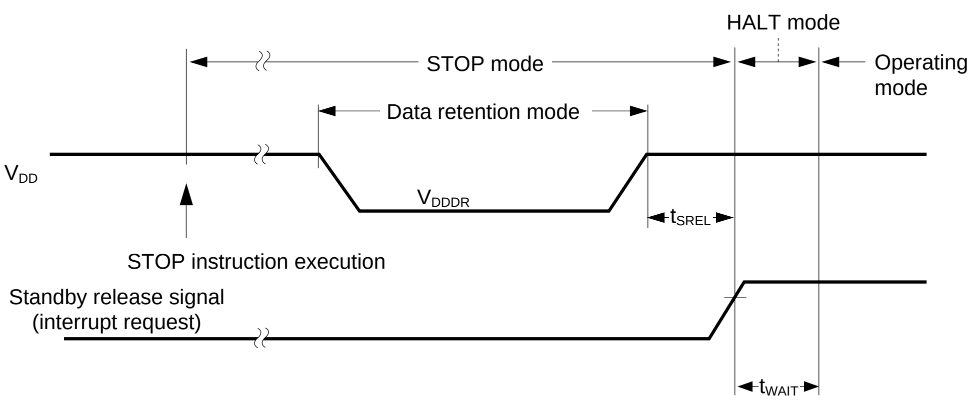
Note $2^{12}/f_{xx}$ or $2^{14}/f_{xx}$-$2^{17}/f_{xx}$ can be selected by bit 0-bit 2 (OSTS0-OSTS2) of oscillation stabilization time selection register (OSTS).

Remark f_{xx}: Main system clock frequency (f_x or $f_x/2$)
f_x: Main system clock oscillation frequency

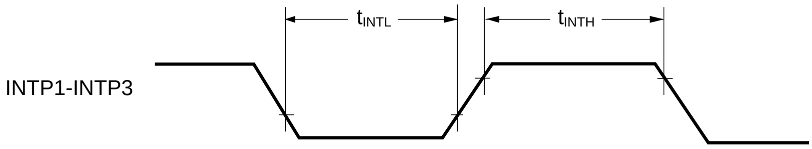
Data Retention Timing (STOP mode released by $\overline{RESET}$)



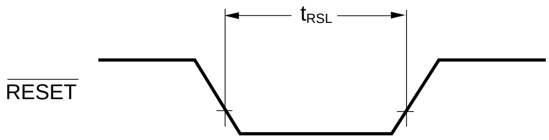
Data Retention Timing (Standby release signal: STOP mode released by interrupt signal)



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



PROM Programming Characteristics

DC Characteristics

(1) PROM Write Mode (T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	V_{IH}		$0.7V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL}	V_{IL}		0		$0.3V_{DD}$	V
Output voltage, high	V_{OH}	V_{OH}	I_{OH} = –1 mA	V_{DD} – 1.0			V
Output voltage, low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	0 - V_{IN} - V_{DD}	–10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		12.2	12.5	12.8	V
V_{DD} supply voltage	V_{DD}	V_{CC}		6.25	6.5	6.75	V
V_{PP} supply current	I_{PP}	I_{PP}	$\overline{PGM}$ = V_{IL}			50	mA
V_{DD} supply current	I_{DD}	I_{CC}				50	mA

(2) PROM Read Mode (T_A = 25 ±5°C, V_{DD} = 5.0 ±0.5 V, V_{PP} = V_{DD} ±0.6 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	V_{IH}		$0.7V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL}	V_{IL}		0		$0.3V_{DD}$	V
Output voltage, high	V_{OH1}	V_{OH1}	I_{OH} = –1 mA	V_{DD} – 1.0			V
	V_{OH2}	V_{OH2}	I_{OH} = –100 μA	V_{DD} – 0.5			V
Output voltage, low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	0 - V_{IN} - V_{DD}	–10		+10	μA
Output leakage current	I_{LO}	I_{LO}	0 - V_{OUT} - V_{DD}, $\overline{OE}$ = V_{IH}	–10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		V_{DD} – 0.6	V_{DD}	V_{DD} + 0.6	V
V_{DD} supply voltage	V_{DD}	V_{CC}		4.5	5.0	5.5	V
V_{PP} supply current	I_{PP}	I_{PP}	V_{PP} = V_{DD}			100	μA
V_{DD} supply current	I_{DD}	I_{CCA1}	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH}			50	mA

Note Corresponding μPD27C1001A symbol.

AC Characteristics

(1) PROM Write Mode

(a) Page program mode (T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol Note	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{OE}$ ↓)	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ setup time	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (to $\overline{OE}$ ↓)	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{OE}$ ↓)	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}$ ↑)	t_{AH}	t_{AH}		2			μs
	t_{AHL}	t_{AHL}		2			μs
	t_{AHV}	t_{AHV}		0			μs
Input data hold time (from $\overline{OE}$ ↑)	t_{DH}	t_{DH}		2			μs
$\overline{OE}$ ↑ → Data output float delay time	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{OE}$ ↓)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{OE}$ ↓)	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	t_{PW}	t_{PW}		0.095	0.1	0.105	ms
$\overline{OE}$ ↓ → Valid data delay time	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ pulse width during data latching	t_{LW}	t_{LW}		1			μs
$\overline{PGM}$ setup time	t_{PGMS}	t_{PGMS}		2			μs
$\overline{CE}$ hold time	t_{CEH}	t_{CEH}		2			μs
$\overline{OE}$ hold time	t_{OEH}	t_{OEH}		2			μs

(b) Byte program mode (T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol Note	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{PGM}$ ↓)	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ set time	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (to $\overline{PGM}$ ↓)	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{PGM}$ ↓)	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}$ ↑)	t_{AH}	t_{AH}		2			μs
Input data hold time (from $\overline{PGM}$ ↑)	t_{DH}	t_{DH}		2			μs
$\overline{OE}$ ↑ → Data output float delay time	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{PGM}$ ↓)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{PGM}$ ↓)	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	t_{PW}	t_{PW}		0.095	0.1	0.105	ms
$\overline{OE}$ ↓ → Valid data delay time	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ hold time	t_{OEH}	—		2			μs

Note Corresponding μPD27C1001A symbol.

(2) PROM Read Mode (T_A = 25 ±5°C, V_{DD} = 5.0 ±0.5 V, V_{PP} = V_{DD} ±0.6 V)

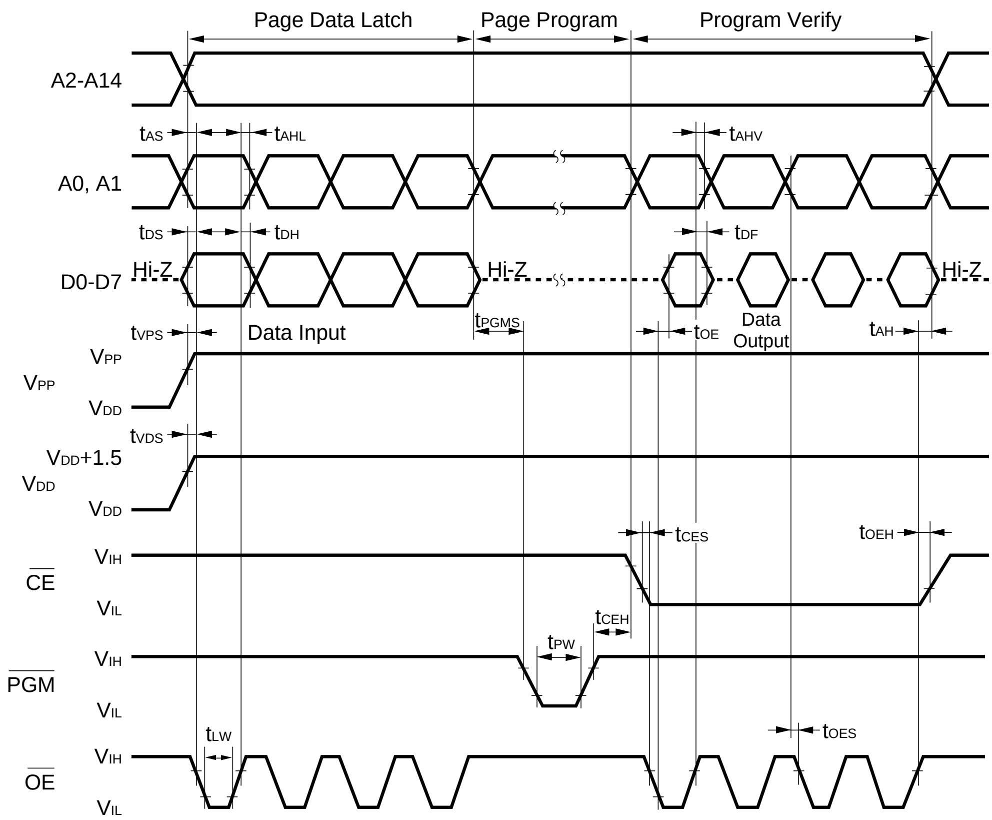
Parameter	Symbol	Symbol Note	Test Conditions	MIN.	TYP.	MAX.	Unit
Address → Data output delay time	t_{ACC}	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$			800	ns
$\overline{CE}$ ↓ → Data output delay time	t_{CE}	t_{CE}	$\overline{OE} = V_{IL}$			800	ns
$\overline{OE}$ ↓ → Data output delay time	t_{OE}	t_{OE}	$\overline{CE} = V_{IL}$			200	ns
$\overline{OE}$ ↑ → Data output float delay time	t_{DF}	t_{DF}	$\overline{CE} = V_{IL}$	0		60	ns
Address → Data hold time	t_{OH}	t_{OH}	$\overline{CE} = \overline{OE} = V_{IL}$	0			ns

Note Corresponding μPD27C1001A symbol.

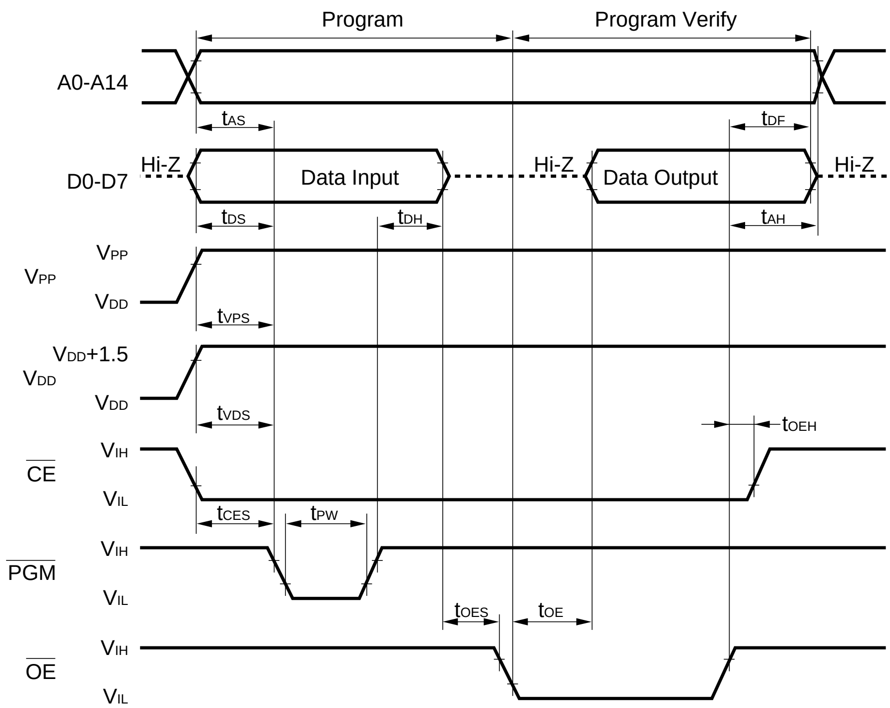
(3) PROM Programming Mode (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
PROM programming mode setup time	t_{SMA}		10			μs

PROM Write Mode Timing (page program mode)



PROM Write Mode Timing (byte program mode)

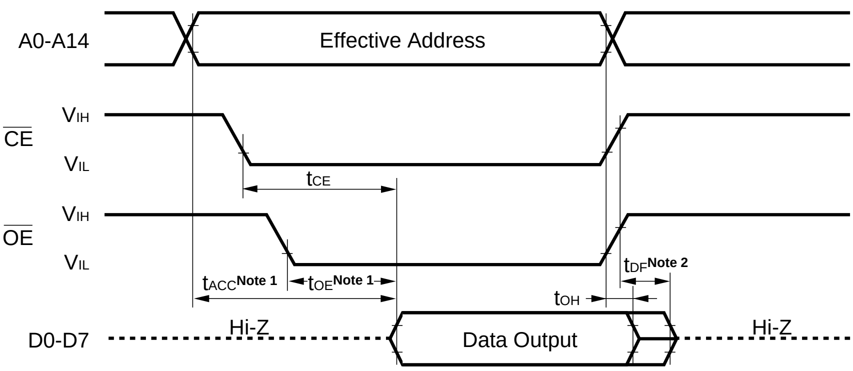


Cautions 1. V_{DD} should be applied before V_{PP}, and removed after V_{PP}.

2. V_{PP} must not exceed +13.5 V including overshoot.

3. Reliability may be adversely affected if removal/reinsertion is performed while + 12.5 V is being applied to V_{PP}.

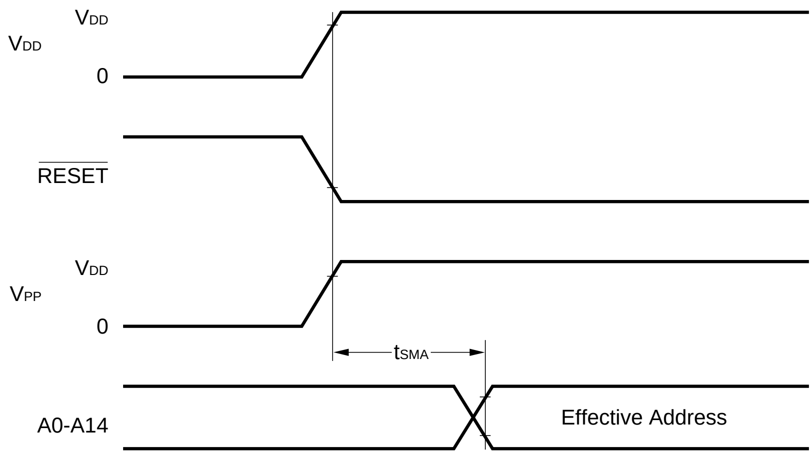
PROM Read Mode Timing



Notes 1. If you want to read within the range of t_{ACC}, make the $\overline{OE}$ input delay time from the fall of $\overline{CE}$ a maximum of t_{ACC}–t_{OE}.

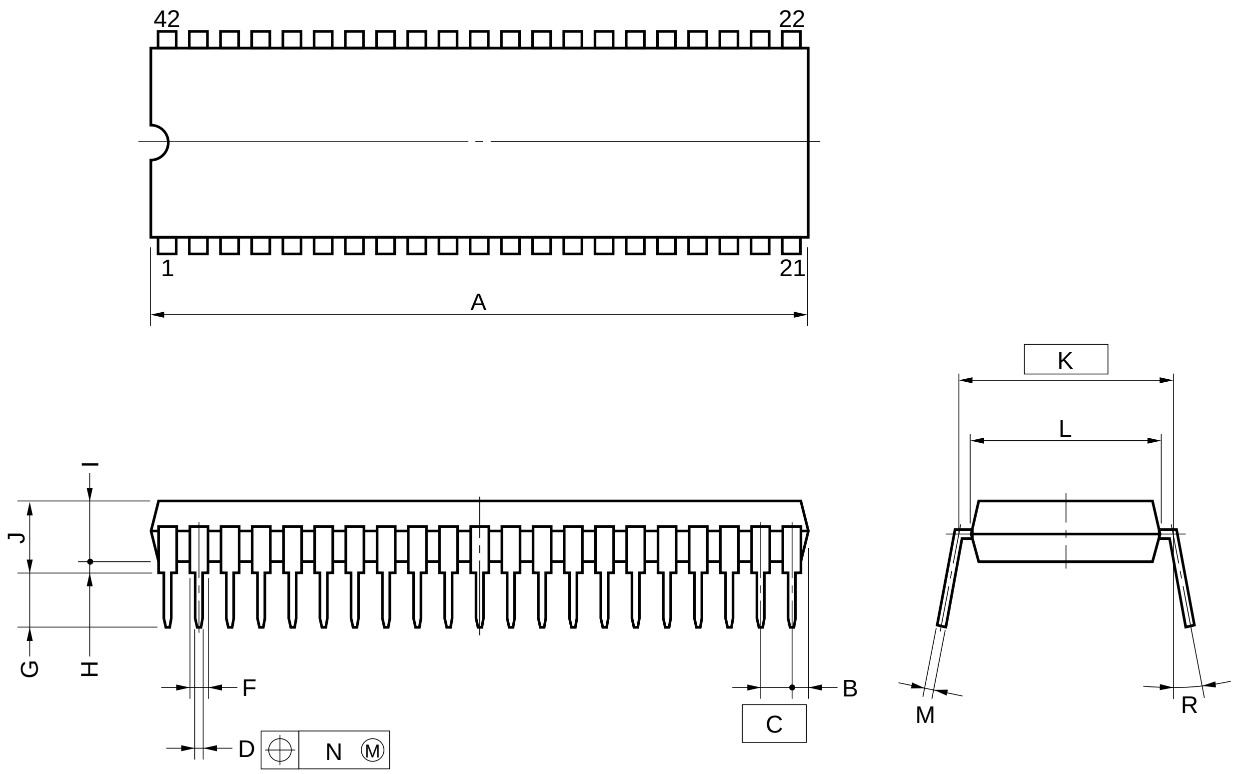
2. t_{DF} is the time from when either $\overline{OE}$ or $\overline{CE}$ first reaches V_{IH}.

PROM Programming Mode Setting Timing



9. PACKAGE DRAWINGS

42PIN PLASTIC SHRINK DIP (600 mil)



NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

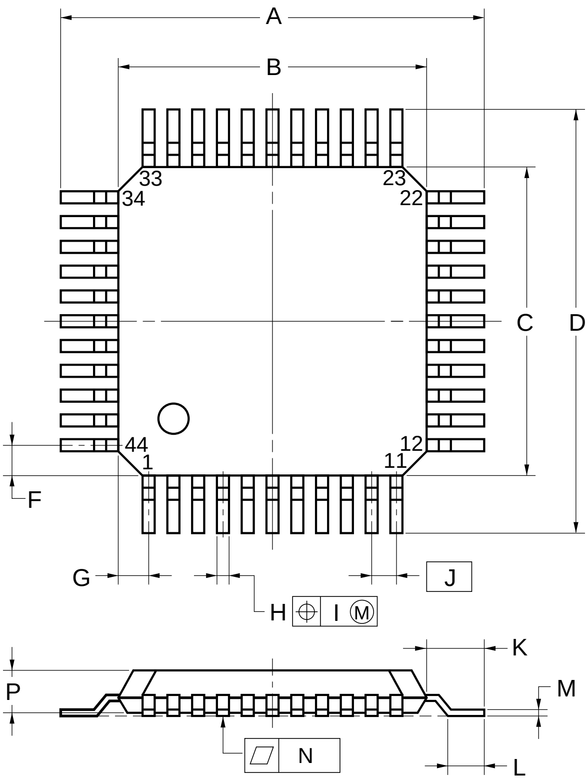
ITEM	MILLIMETERS	INCHES
A	39.13 MAX.	1.541 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	13.2	0.520
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P42C-70-600A-1

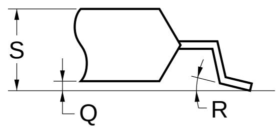
Remark The shape and material of ES versions are the same as those of mass-produced versions.

μPD78P083GB-3B4

44 PIN PLASTIC QFP (□10)



detail of lead end



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

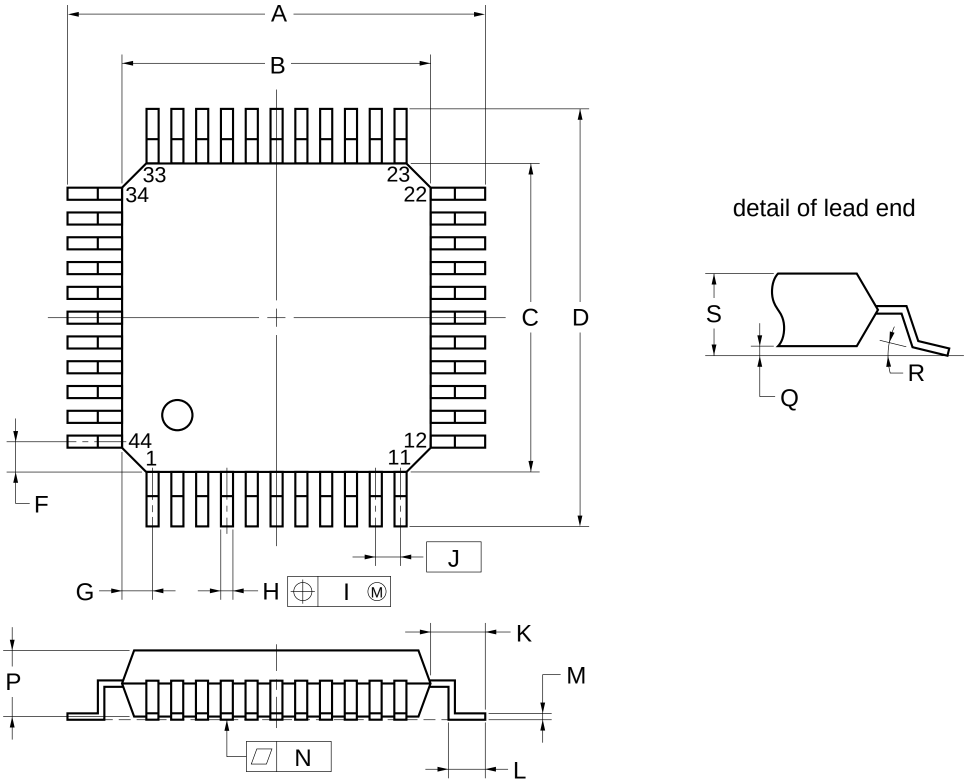
ITEM	MILLIMETERS	INCHES
A	13.6±0.4	$0.535^{+0.017}_{-0.016}$
B	10.0±0.2	$0.394^{+0.008}_{-0.009}$
C	10.0±0.2	$0.394^{+0.008}_{-0.009}$
D	13.6±0.4	$0.535^{+0.017}_{-0.016}$
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P44GB-80-3B4-3

Remark The shape and material of ES versions are the same as those of mass-produced versions.

μPD78P083GB-3BS-MTX

44 PIN PLASTIC QFP (□10)



NOTE

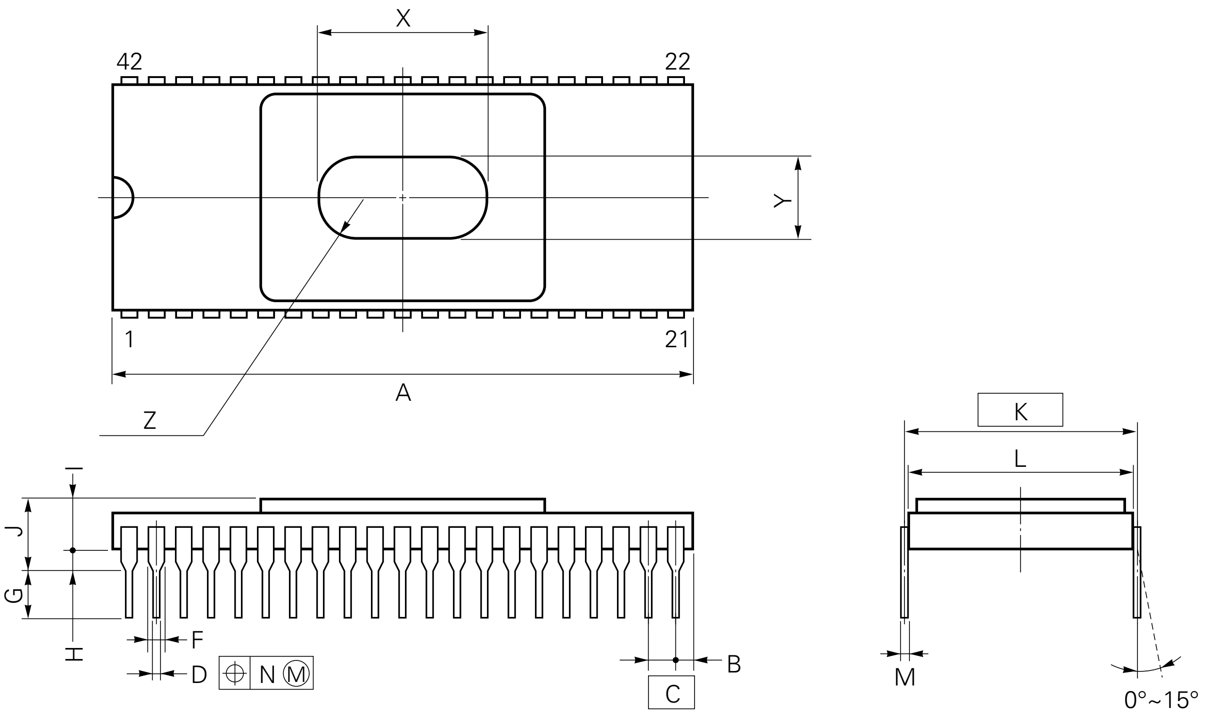
Each lead centerline is located within 0.16 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.2±0.2	$0.520^{+0.008}_{-0.009}$
B	10.0±0.2	$0.394^{+0.008}_{-0.009}$
C	10.0±0.2	$0.394^{+0.008}_{-0.009}$
D	13.2±0.2	$0.520^{+0.008}_{-0.009}$
F	1.0	0.039
G	1.0	0.039
H	$0.37^{+0.08}_{-0.07}$	$0.015^{+0.003}_{-0.004}$
I	0.16	0.007
J	0.8 (T.P.)	0.031 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.06}_{-0.05}$	$0.007^{+0.002}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.125±0.075	0.005±0.003
R	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$
S	3.0 MAX.	0.119 MAX.

S44GB-80-3BS

Remark The shape and material of ES versions are the same as those of mass-produced versions.

42PIN CERAMIC SHRINK DIP (WINDOW) (600 mil)



P42DW-70-600A

NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	38.25 MAX.	1.506 MAX.
B	1.345 MAX.	0.053 MAX.
C	1.778 (T.P.)	0.07 (T.P.)
D	0.46±0.05	0.018±0.002
F	0.85 MIN.	0.033 MIN.
G	3.5±0.3	0.138±0.012
H	1.02 MIN.	0.040 MIN.
I	3.026	0.119
J	5.282 MAX.	0.208 MAX.
K	15.24 (T.P.)	0.600 (T.P.)
L	14.99	0.590
M	0.25±0.05	$0.010^{+0.002}_{-0.003}$
N	0.25	0.01
X	12.0	0.472
Y	6.0	0.236
Z	4-R3.0	4-R0.118

10. RECOMMENDED SOLDERING CONDITIONS

*

It is recommended that the μPD78P083 be soldered under the following conditions.
For details on the recommended soldering conditions, refer to information document **"Semiconductor Device Mounting Technology Manual" (C10535E)**.

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

Table 10-1. Soldering Conditions for Surface Mount Types

μPD78P083GB-3B4 : 44-pin plastic QFP (10 x 10 mm)
μPD78P083GB-3BS-MTX : 44-pin plastic QFP (10 x 10 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared ray reflow	Package peak temperature: 235°C, Reflow time: 30 seconds or less (at 210°C or higher), Number of reflow processes: 2 or less < Cautions > (1) Wait for the device temperature to return to normal after the first reflow before starting the second reflow. (2) Do not perform flux cleaning with water after the first reflow.	IR35-00-2
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds or less (at 200°C or higher), Number of reflow processes: 2 or less < Cautions > (1) Wait for the device temperature to return to normal after the first reflow before starting the second reflow. (2) Do not perform flux cleaning with water after the first reflow.	VP15-00-2
Wave soldering	Solder temperature: 260°C or below, Flow time: 10 seconds or less, Number of flow processes: 1, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C or below, Flow time: 3 seconds or less (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating method).

Table 10-2. Soldering Condition for Hole-Through Types

μPD78P083CU : 42-pin plastic shrink DIP (600 mil)
μPD78P083DU : 42-pin ceramic shrink DIP (with window) (600 mil)

Soldering Method	Soldering Conditions
Wave Soldering (only pins)	Solder temperature: 260°C or below, Flow time: 10 seconds or less
Partial heating	Pin temperature: 300°C or below, Flow time: 3 seconds or less (per pin)

Caution Apply wave soldering only to the pins and be careful so as not to bring solder into direct contact with the package.

* APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available to support development of systems using the μPD78P083.

Language Processing Software

RA78K/0 Notes 1, 2, 3, 4	Assembler package common to the 78K/0 series
CC78K/0 Notes 1, 2, 3, 4	C compiler package common to the 78K/0 series
DF78083 Notes 1, 2, 3, 4	Device file used for the μPD78083 subseries
CC78K/0–L Notes 1, 2, 3, 4	C compiler library source file common to the 78K/0 series

PROM Writing Tools

PG-1500	PROM programmer
PA-78P083CU PA-78P083GB	Programmer adapter connected to the PG-1500
PG-1500 Controller Notes 1, 2	Control program for the PG-1500

Debugging Tools

IE-78000-R	In-circuit emulator common to the 78K/0 series
IE-78000-R-A Note 8	In-circuit emulator common to the 78K/0 series (for integrated debugger)
IE-78000-R-BK	Break board common to the 78K/0 series
IE-78078-R-EM	Emulation board common to the μPD78078 subseries
EP-78083CU-R EP-78083GB-R	Emulation probe for the μPD78083 subseries
EV-9200G-44	Socket mounted on the target system board prepared for 44-pin plastic QFP
SM78K0 Notes 5, 6, 7	System simulator common to the 78K/0 series
ID78K0 Notes 4, 5, 6, 7, 8	Integrated debugger for IE-78000-R-A
SD78K/0 Notes 1, 2	Screen debugger for the IE-78000-R
DF78083 Notes 1, 2, 5, 6, 7	Device file used for the μPD78083 subseries

Notes
1. Based on PC-9800 series (MS-DOS™)
2. Based on IBM PC/AT™ and its compatibles (PC DOS™/IBM DOS™/MS-DOS)
3. Based on HP9000 series 300™ (HP-UX™)
4. Based on HP9000 series 700™ (HP-UX), SPARCstation™ (SunOS™), and EWS4800 series (EWS-UX/V)
5. Based on PC-9800 series (MS-DOS + Windows™)
6. IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS + Windows)
7. Based on NEWS™ (NEWS-OS™)
8. Under development

Remarks
1. Please refer to the **78K/0 Series Selection Guide (U11126E)** for information on the third party development tools.
2. Use the RA78K/0, CC78K/0, SM78K0, ID78K0, and SD78K/0 in combination with the DF78083.

Fuzzy Inference Development Support System

FE9000 Note 1/FE9200 Note 2	Fuzzy knowledge data creation tool
FT9080 Note 1/FT9085 Note 3	Translator
FI78K0 Notes 1, 3	Fuzzy inference module
FD78K0 Notes 1, 3	Fuzzy inference debugger

Notes 1. Based on PC-9800 series (MS-DOS)
2. Based on IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS+Windows)
3. Based on IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS)

Remark Please refer to the **78K/0 Series Selection Guide (U11126E)** for information on the third party development tools.

* APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document Name		Document No.	
		Japanese	English
μPD78083 Subseries User's Manual		IEU-886	IEU-1407
78K/0 Series User's Manual—Instructions		IEU-849	IEU-1372
78K/0 Series Instruction Table		U10903J	—
78K/0 Series Instruction Set		U10904J	—
μPD78083 Subseries Special Function Register Table		IEM-5599	—
78K/0 Series Application Note	Basic (III)	IEA-767	U10182E

Documents Related to Development Tools (User's Manual)

Document Name		Document No.	
		Japanese	English
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K/0 C Compiler Application Note	Programming know-how	EEA-618	EEA-1208
CC78K Series Library Source File		EEU-777	—
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller PC-9800 Series (MS-DOS) Based		EEU-704	EEU-1291
PG-1500 Controller IBM PC Series (PC DOS) Based		EEU-5008	U10540E
IE-78000-R		EEU-810	EEU-1398
IE-78000-R-A		U10057J	U10057E
IE-78000-R-BK		EEU-867	EEU-1427
IE-78078-R-EM		U10775J	EEU-1504
EP-78083		EEU-5003	EEU-1529
SM78K0 System Simulator	Reference	EEU-5002	U10181E
SM78K Series System Simulator	Third party's user open interface specifications	U10092J	U10092E
SD78K/0 Screen Debugger PC-9800 Series (MS-DOS) Based	Introduction	EEU-852	—
	Reference	U10952J	—
SD78K/0 Screen Debugger IBM PC/AT (PC DOS) Based	Introduction	EEU-5024	EEU-1414
	Reference	EEU-993	EEU-1413

Caution The contents of the documents listed above are subject to change without prior notice. Make sure to use the latest edition when starting design.

Documents Related to Embedded Software (User's Manual)

Document Name		Document No.	
		Japanese	English
78K/0 Series OS MX78K0	Basic	EEU-5010	—
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K/0, 78K/II, and 87AD Series Fuzzy Inference Development Support System Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-921	EEU-1458

Other Documents

Document Name	Document No.	
	Japanese	English
Semiconductor Device Package Manual	IEI-635	IEI-1213
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	IEI-620	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	IEI-1201
Guide to Quality Assurance for Semicoductor Devices	MEI-603	MEI-1202
Microcontroller-Related Product Guide – Third Party Products –	MEI-604	—

Caution The contents of the documents listed above are subject to change without prior notice. Be sure to use the latest edition when starting design.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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The customer must judge the need for license
: µPD78P083CU, 78P083GB-3B4, 78P083GB-3BS-MTX