DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD78P078Y

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78P078Y is a member of the μPD78078Y Subseries of the 78K/0 Series, in which the on-chip mask ROM of the μPD78078Y is replaced with a one-time PROM or EPROM.

Because this device can be programmed by users, it is ideally suited for system evaluation, small-lot and multiple-device production, and early development and time-to-market.

The μPD78P078Y can be also used for system evaluation of a μPD78075BY Subseries device.

Cautions 1. The specifications of the μPD78075BY Subseries are not the same as those of the μPD78078Y Subseries. Therefore, if a μPD78P078Y is used to evaluate a μPD78075BY Subseries product, refer to the μPD78075B, 78075BY Subseries User's Manual (U12560E).

2. The reliability of the μPD78P078YKL-T is not guaranteed for use in mass-produced products. Please use only experimentally or for evaluation purposes during trial manufacture.

The details of functions are described in the user's manuals. Be sure to read the following manuals before designing.

μPD78078, 78078Y Subseries User's Manual : U10641E
78K/0 Series User's Manual: Instructions : U12326E

FEATURES

- Pin-compatible with mask ROM version (except V_{PP} pin)
- Internal PROM: 60 Kbytes[Note 1]
  - μPD78P078YKL-T: Reprogrammable (ideally suited for system evaluation)
  - μPD78P078YGC, μPD78P078YGF: One-time programmable (ideally suited for small-lot production)
- Internal high-speed RAM: 1024 bytes
- Internal expansion RAM: 1024 bytes[Note 2]
- Internal buffer RAM: 32 bytes
- Operable in the same supply voltage as the mask ROM version (V_{DD} = 1.8 to 5.5 V)
- Corresponding to QTOP™ Microcontrollers

Notes 1. The internal PROM capacity can be changed by setting the memory size switching register (IMS).

2. The internal expansion RAM capacity can be changed by the internal expansion RAM size switching register (IXS).

Remarks 1. Refer to **1. DIFFERENCES BETWEEN THE μPD78P078Y AND MASK ROM VERSIONS** for the differences between the PROM version and the mask ROM version.

2. QTOP microcontroller is a general term for microcontrollers which incorporate one-time PROM and are totally supported by NEC's programming service (from programming to marking, screening and verification).

In this document, the term PROM is used in parts common to one-time PROM versions and EPROM versions.

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The mark ★ shows major revised points.

ORDERING INFORMATION

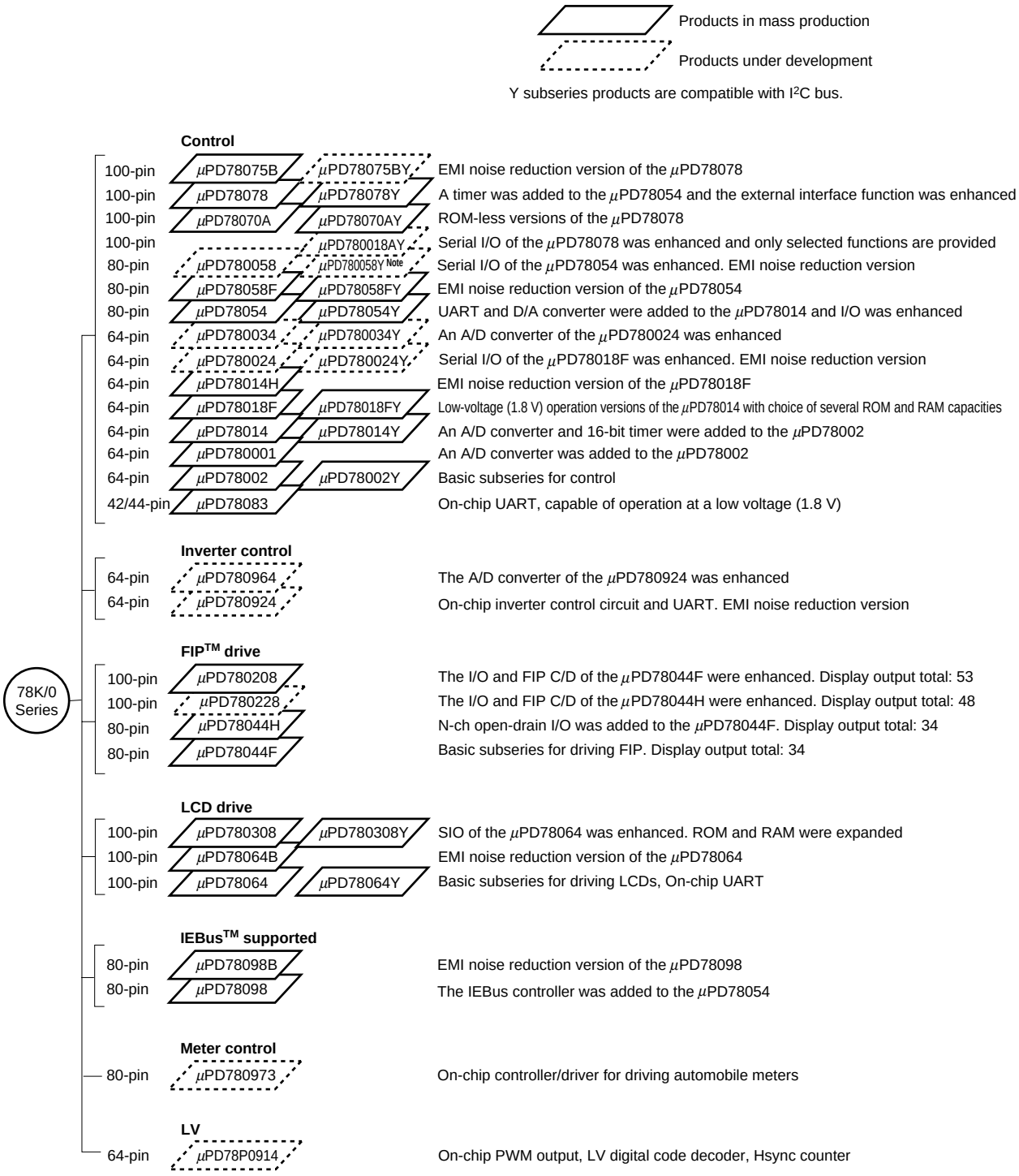
Part Number	Package	Internal ROM	Quality Grades
μPD78P078YGF-3BA	100-pin plastic QFP (14 × 20 mm, resin thickness: 2.7 mm)	One-Time PROM	Standard
μPD78P078YGC-8EU[Note]	100-pin plastic LQFP (fine pitch) (14 × 14 mm, resin thickness: 1.40 mm)	One-Time PROM	Standard
μPD78P078YKL-T	100-pin ceramic WQFN (14 × 20 mm)	EPROM	Not applicable

Note Under development

Please refer to “Quality Grades on NEC Semiconductor Devices” (Document number C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

★ **78K/0 Series Development**

The following shows the 78K/0 Series products development. Subseries names are shown inside frames.



Note Under planning

The following table shows the differences among subseries functions.

Function / Part Number		ROM Capacity	Timer 8-bit	Timer 16-bit	Timer Watch	Timer WDT	8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
Control	μPD78075B	32K to 40K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	88	1.8 V	Available
	μPD78078	48K to 60K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24K to 60K	2 ch						2 ch	3 ch (time division UART: 1 ch)	68	1.8 V	
	μPD78058F	48K to 60K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16K to 60K										2.0 V	
	μPD780034	8K to 32K					–	8 ch	–	3 ch (UART: 1 ch, time division 3-wire: 1 ch)	51	1.8 V	
	μPD780024						8 ch	–					
	μPD78014H									2 ch	53		
	μPD78018F	8K to 60K											
	μPD78014	8K to 32K										2.7 V	
	μPD780001	8K		–	–					1 ch	39		–
	μPD78002	8K to 16K			1 ch		–				53		Available
	μPD78083				–		8 ch			1 ch (UART: 1 ch)	33	1.8 V	–
Inverter control	μPD780964	8K to 32K	3 ch	**Note**	–	1 ch	–	8 ch	–	2 ch (UART: 2 ch)	47	2.7 V	Available
	μPD780924						8 ch	–					
FIP drive	μPD780208	32K to 60K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	2 ch	74	2.7 V	–
	μPD780228	48K to 60K	3 ch	–	–					1 ch	72	4.5 V	
	μPD78044H	32K to 48K	2 ch	1 ch	1 ch						68	2.7 V	
	μPD78044F	16K to 40K								2 ch			
LCD drive	μPD780308	48K to 60K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	3 ch (time division UART: 1 ch)	57	2.0 V	–
	μPD78064B	32K								2 ch (UART: 1 ch)			
	μPD78064	16K to 32K											
IEBus supported	μPD78098B	40K to 60K	2 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	69	2.7 V	Available
	μPD78098	32K to 60K											
Meter control	μPD780973	24K to 32K	3 ch	1 ch	1 ch	1 ch	5 ch	–	–	2 ch (UART: 1 ch)	56	4.5 V	–
LV	μPD78P0914	32K	6 ch	–	–	1 ch	8 ch	–	–	2 ch	54	4.5 V	Available

Note 10-bit timer: 1 channel

FUNCTION DESCRIPTION

Item		Function
Internal memory		• PROM: 60 Kbytes[Note 1] • RAM High-speed RAM: 1024 bytes Expansion RAM: 1024 bytes[Note 2] Buffer RAM: 32 bytes
Memory space		64 Kbytes
General register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Minimum instruction execution time		Minimum instruction execution time variable function is integrated.
	When main system clock is selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (@ 5.0 MHz)
	When subsystem clock is selected	122 μs (@ 32.768 kHz)
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjust, etc.
I/O ports		Total : 88 • CMOS input : 2 • CMOS input/output : 78 • N-ch open-drain input/output : 8
A/D converter		• 8-bit resolution × 8 channels
D/A converter		• 8-bit resolution × 2 channels
Serial interface		• 3-wire serial I/O/2-wire serial I/O/I^2C bus mode selectable: 1 channel • 3-wire serial I/O mode (with max. 32-byte on-chip automatic transmitting/receiving function): 1 channel • 3-wire serial I/O/UART mode selectable: 1 channel
Timer		• 16-bit timer/event counter: 1 channel • 8-bit timer/event counter: 4 channels • Watch timer: 1 channel • Watchdog timer: 1 channel
Timer output		5 pins (14-bit PWM output enable: 1 pin, 8-bit PWM output enable: 2 pins)
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, and 5.0 MHz (@ 5.0 MHz with main system clock) 32.768 kHz (@ 32.768 kHz with subsystem clock)
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz and 9.8 kHz (@ 5.0 MHz with main system clock)

Notes 1. The internal PROM capacity can be changed by using the memory size switching register (IMS).

2. The internal expansion RAM capacity can be changed by using the internal expansion RAM size switching register (IXS).

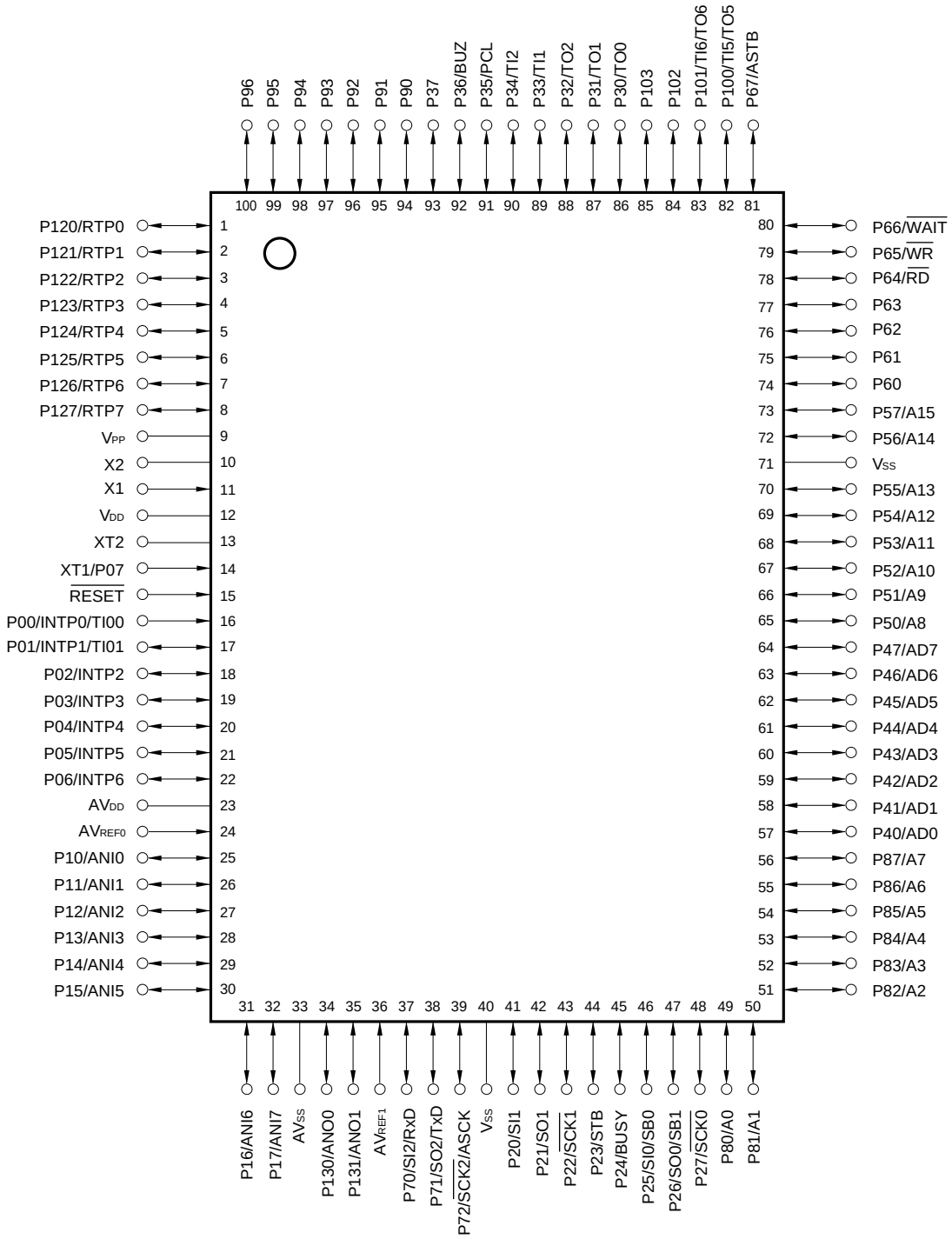
Item		Function
Vectored interrupt sources	Maskable	Internal: 15, External: 7
	Non-maskable	Internal: 1
	Software	1
Test input		Internal: 1, External: 1
Supply voltage		V_{DD} = 1.8 to 5.5 V
Package		• 100-pin plastic QFP (14 × 20 mm, resin thickness: 2.7 mm) • 100-pin plastic LQFP (fine pitch) (14 × 14 mm, resin thickness: 1.40 mm)[Note] • 100-pin ceramic WQFN (14 × 20 mm)

Note Under development

PIN CONFIGURATION (TOP VIEW)

(1) Normal operating mode

- 100-pin plastic QFP (14 × 20 mm, resin thickness: 2.7 mm)
  μPD78P078YGF-3BA
- 100-pin ceramic WQFN
  μPD78P078YKL-T

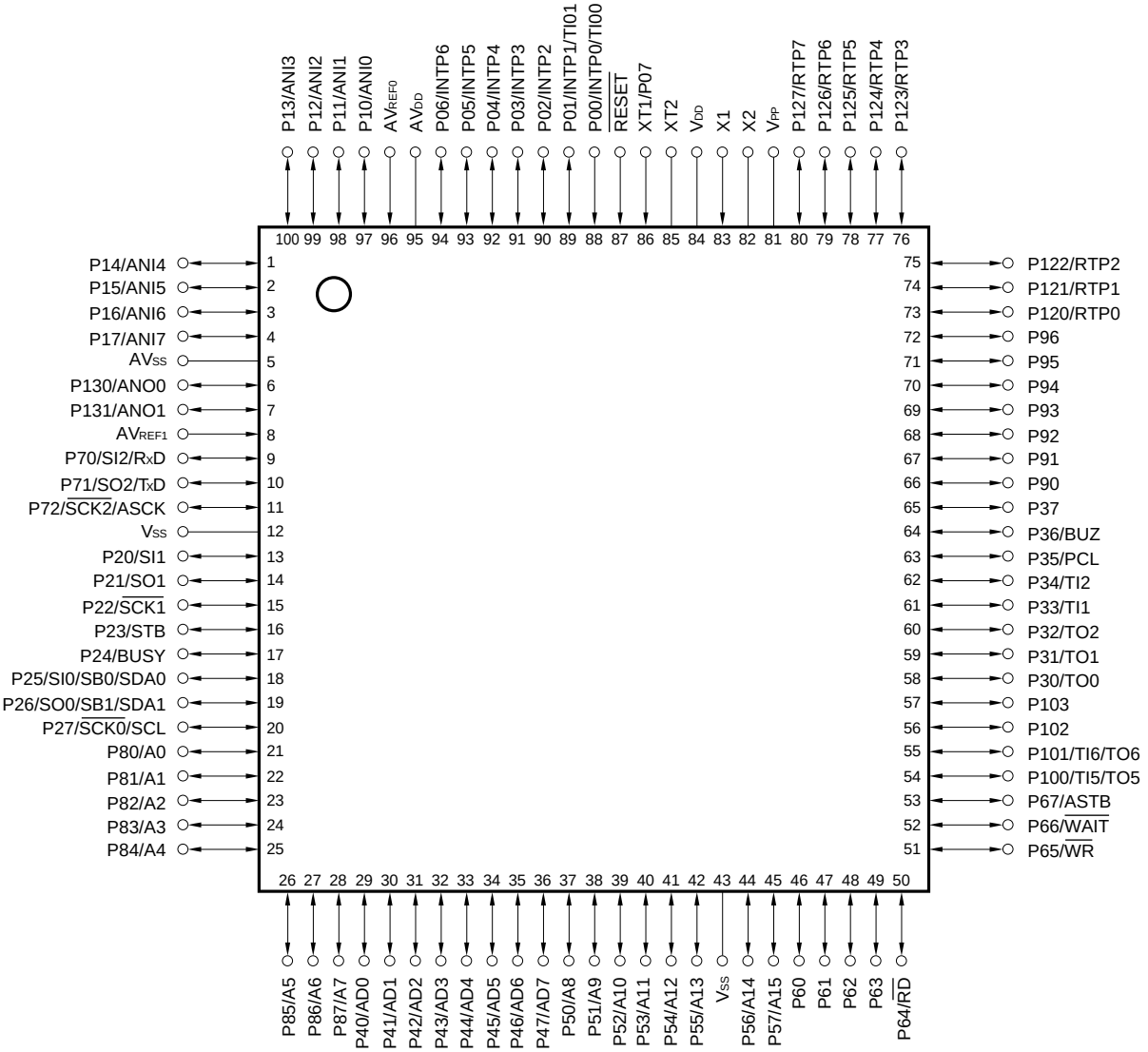


Cautions 1. Connect V_{PP} pin directly to V_{SS}.

2. Connect AV_{DD} pin to V_{DD}.

3. Connect AV_{SS} pin to V_{SS}.

- 100-pin plastic LQFP (fine pitch) (14 × 14 mm, resin thickness: 1.40 mm)
  μPD78P078YGC-8EU[Note]



Note Under development

Cautions 1. Connect V_{PP} pin directly to V_{SS}.

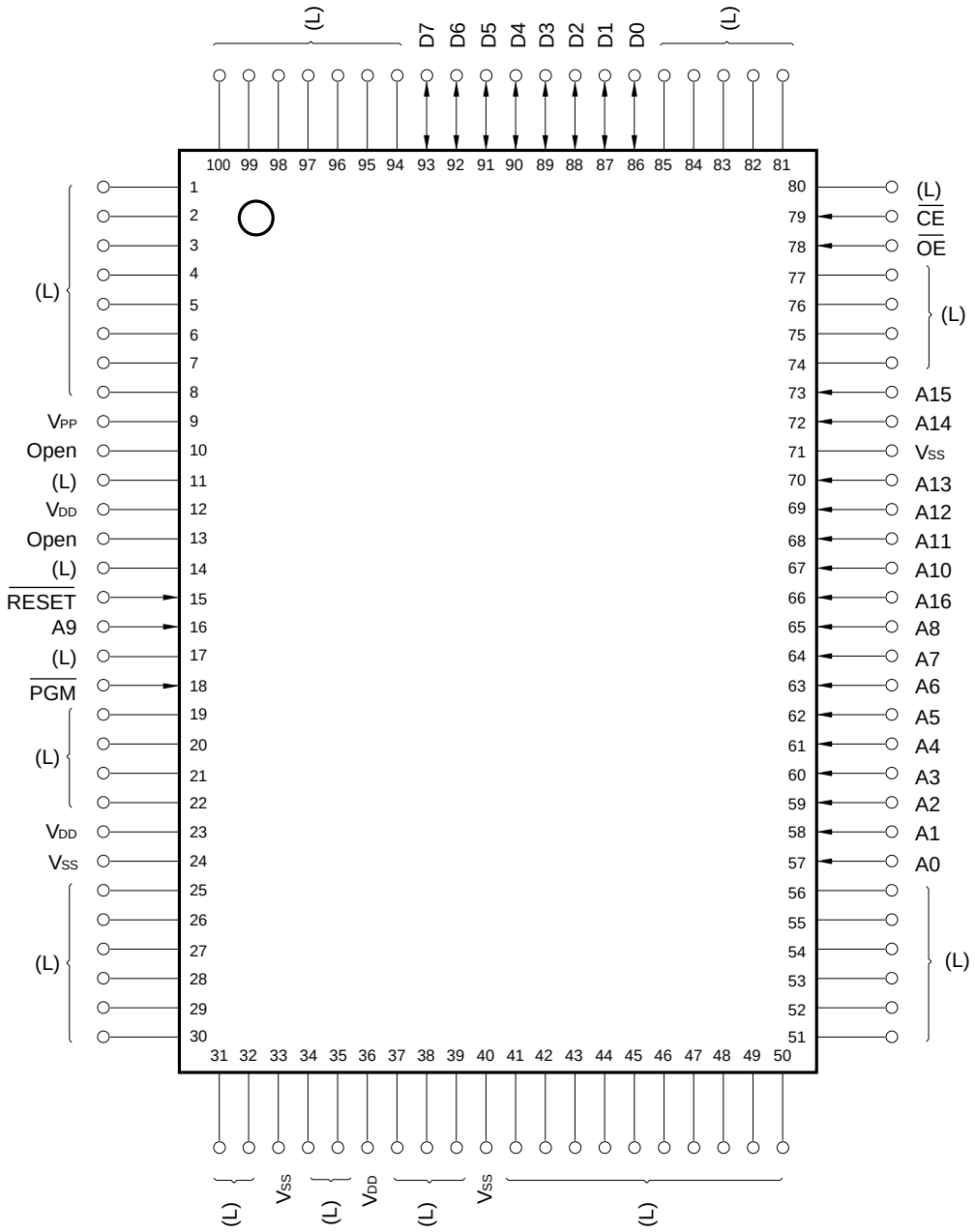
2. Connect AV_{DD} pin to V_{DD}.

3. Connect AV_{SS} pin to V_{SS}.

A0 to A15	: Address Bus
AD0 to AD7	: Address/Data Bus
ANI0 to ANI7	: Analog Input
ANO0, ANO1	: Analog Output
ASCK	: Asynchronous Serial Clock
ASTB	: Address Strobe
AV_{DD}	: Analog Power Supply
AV_{REF0}, AV_{REF1}	: Analog Reference Voltage
AV_{SS}	: Analog Ground
BUSY	: Busy
BUZ	: Buzzer Clock
INTP0 to INTP6	: Interrupt from Peripherals
P00 to P07	: Port 0
P10 to P17	: Port 1
P20 to P27	: Port 2
P30 to P37	: Port 3
P40 to P47	: Port 4
P50 to P57	: Port 5
P60 to P67	: Port 6
P70 to P72	: Port 7
P80 to P87	: Port 8
P90 to P96	: Port 9
P100 to P103	: Port 10
P120 to P127	: Port 12
P130, P131	: Port 13
PCL	: Programmable Clock
$\overline{RD}$	: Read Strobe
$\overline{RESET}$	: Reset
RTP0 to RTP7	: Real-Time Output Port
RxD	: Receive Data
TxD	: Transmit Data
SB0, SB1	: Serial Bus
$\overline{SCK0}$ to $\overline{SCK2}$	: Serial Clock
SCL	: Serial Clock
SDA0, SDA1	: Serial Data
SI0 to SI2	: Serial Input
SO0 to SO2	: Serial Output
STB	: Strobe
TI00, TI01	: Timer Input
TI1, TI2, TI5, TI6	: Timer Input
TO0 to TO2, TO5, TO6	: Timer Output
V_{DD}	: Power Supply
V_{PP}	: Programming Power Supply
V_{SS}	: Ground
$\overline{WAIT}$	: Wait
$\overline{WR}$	: Write Strobe
X1, X2	: Crystal (Main System Clock)
XT1, XT2	: Crystal (Subsystem Clock)

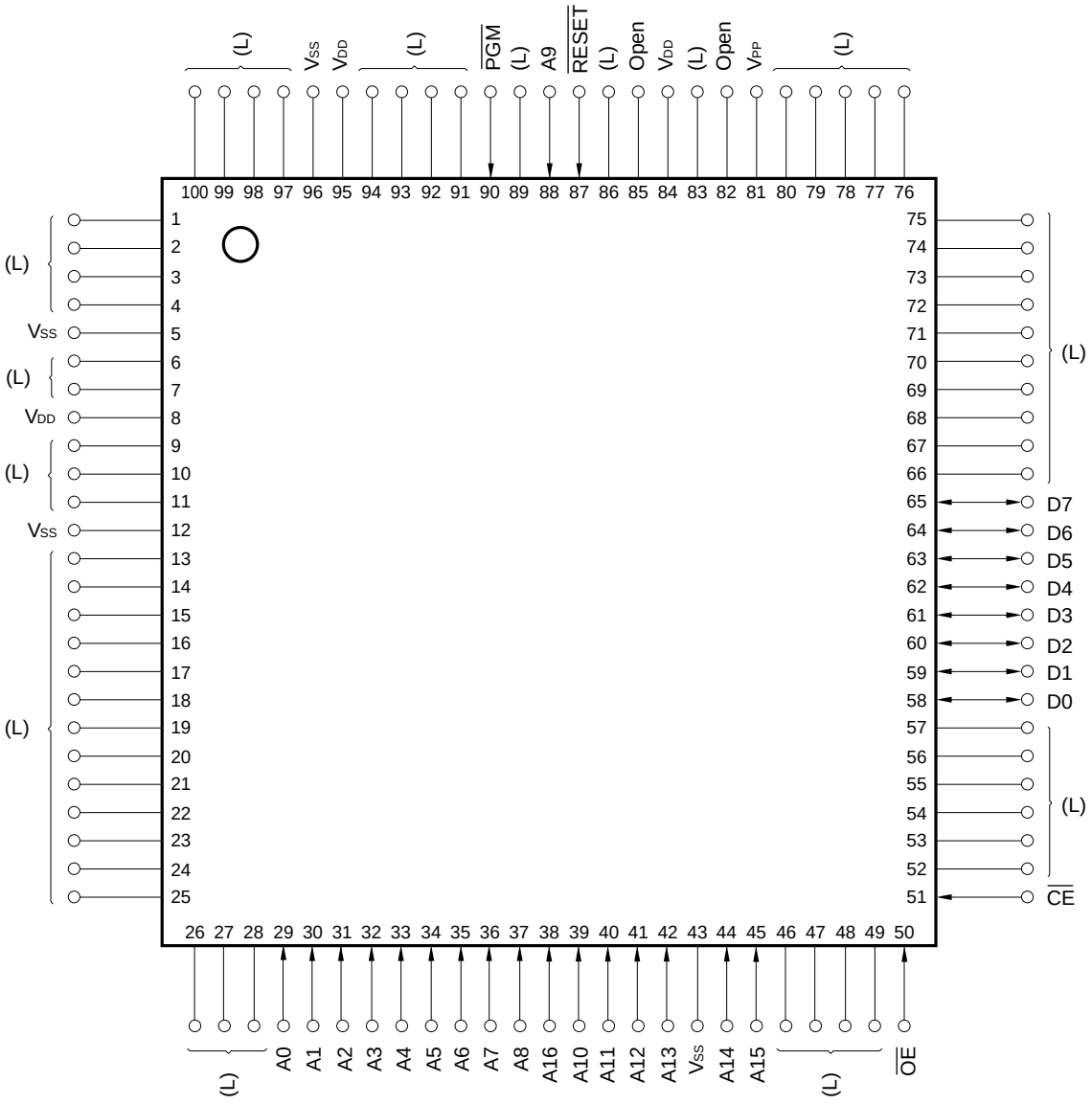
(2) PROM programming mode

- 100-pin plastic QFP (14 × 20 mm, resin thickness: 2.7 mm)
  μPD78P078YGF-3BA
- 100-pin ceramic WQFN
  μPD78P078YKL-T



Cautions 1. (L): Individually connect to V_{SS} via a pull-down resistor.
2. V_{SS}: Connect to GND.
3. $\overline{RESET}$: Set to low level.
4. Open: No connection.

- 100-pin plastic LQFP (fine pitch) (14 × 14 mm, resin thickness: 1.40 mm)
  μPD78P078YGC-8EU[Note]

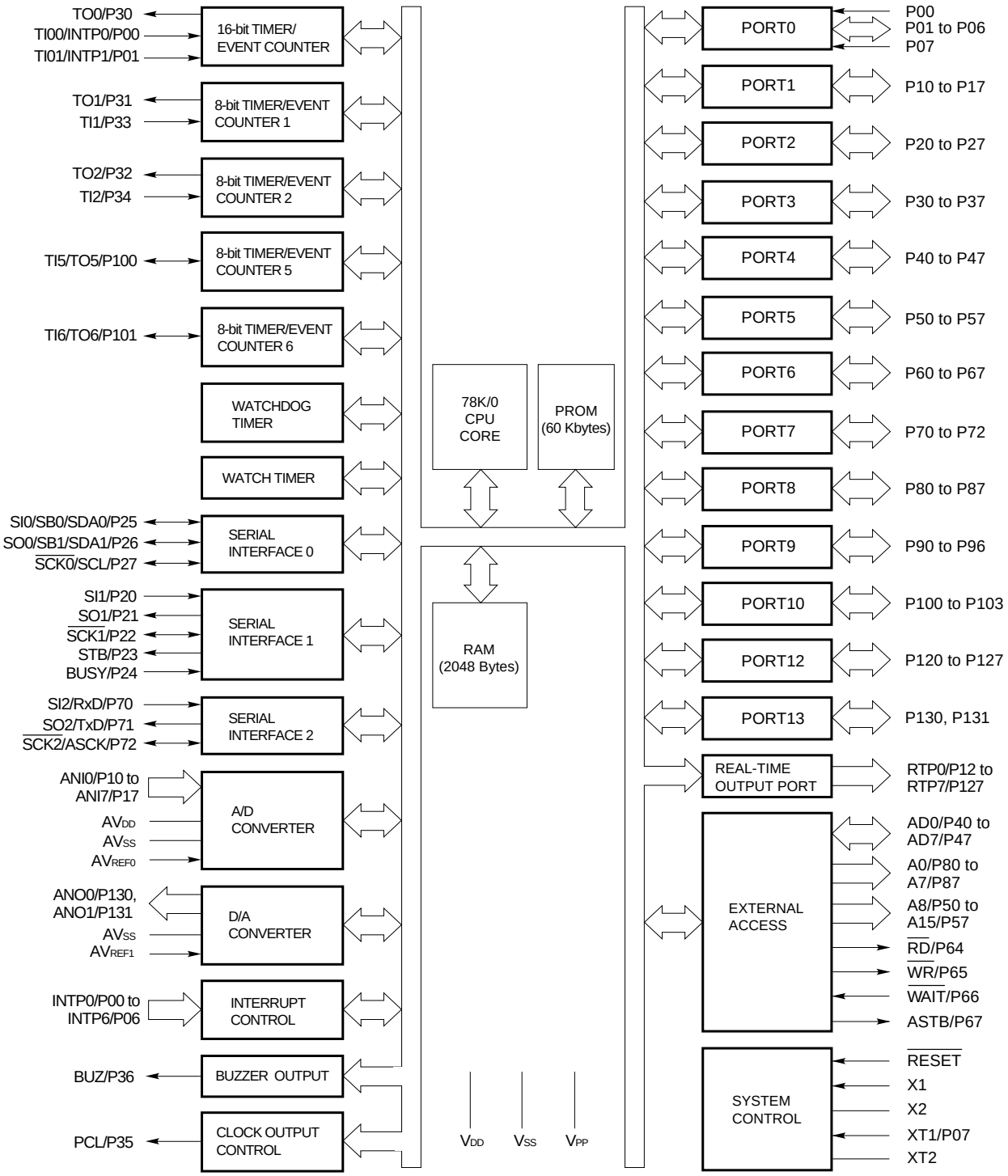


Note Under development

Cautions 1. (L): Individually connect to V_{SS} via a pull-down resistor.
2. V_{SS}: Connect to GND.
3. $\overline{RESET}$: Set to low level.
4. Open: No connection.

A0 to A16	:	Address Bus	$\overline{RESET}$	:	Reset
$\overline{CE}$	:	Chip Enable	V_{DD}	:	Power Supply
D0 to D7	:	Data Bus	V_{PP}	:	Programming Power Supply
$\overline{OE}$	:	Output Enable	V_{SS}	:	Ground
$\overline{PGM}$	:	Program			

BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN THE μPD78P078Y AND MASK ROM VERSIONS

The μPD78P078Y is a single-chip microcontroller with an on-chip one-time PROM or with an on-chip EPROM which has program write, erasure and rewrite capability.

It is possible to make all the functions, except for PROM specification and mask option of the P60 to P63 and P90 to P93 pins, the same as those of the mask ROM versions by setting the memory size switching register (IMS) and internal expanded RAM size switching register (IXS).

Differences between the PROM version (μPD78P078Y) and mask ROM versions (μPD78074BY, 78075BY, 78076Y, 78078Y) are shown in Table 1-1.

Table 1-1. Differences between the μPD78P078 and Mask ROM Versions

Parameter	μPD78P078	Mask ROM Versions
Internal ROM type	One-time PROM/EPROM	Mask ROM
Internal ROM capacity	60 Kbytes	μPD78074BY : 32 Kbytes μPD78075BY : 40 Kbytes μPD78076Y : 48 Kbytes μPD78078Y : 60 Kbytes
Internal expanded RAM capacity	1024 bytes	μPD78074BY : none μPD78075BY : none μPD78076Y : 1024 bytes μPD78078Y : 1024 bytes
Internal ROM capacity selection with memory size switching register (IMS)	Possible[Note 1]	Not possible
Internal expanded RAM capacity selection with internal expanded RAM size switching register (IXS)	Possible[Note 2]	Not possible
IC pin	No	Yes
V_{PP} pin	Yes	No
On-chip pull-up resistor mask option of P60 to P63 and P90 to P93 pins	No	Yes
Electrical specifications	Refer to the Data Sheet for each version.	

Notes 1. The internal PROM becomes 60 Kbytes and the internal high-speed RAM becomes 1024 bytes by $\overline{\text{RESET}}$ input.

2. The internal expansion RAM becomes 1024 bytes by $\overline{\text{RESET}}$ input.

★ **Caution There are differences in noise immunity and noise radiation between the PROM and mask ROM versions. When pre-producing an application set with the PROM version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the set using consumer samples (not engineering samples) of the mask ROM version.**

2. PIN FUNCTIONS

2.1 Pins in Normal Operating Mode

(1) Port pins (1/3)

Pin Name	Input/Output	Function		After Reset	Alternate Function
P00	Input	Port 0	Input only	Input	INTP0/TI00
P01	Input/output	8-bit input/output port	Input/output is specifiable bit-wise. When used as the input port, it is possible to connect an on-chip pull-up resistor by software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P06					INTP6
P07[Note 1]	Input		Input only	Input	XT1
P10 to P17	Input/output	Port 1 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect an on-chip pull-up resistor by software.[Note 2]		Input	ANI0 to ANI7
P20	Input/output	Port 2 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect an on-chip pull-up resistor by software.		Input	SI1
P21					SO1
P22					$\overline{SCK1}$
P23					STB
P24					BUSY
P25					SI0/SB0
P26					SO0/SB1
P27					$\overline{SCK0}$
P30	Input/output	Port 3 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect an on-chip pull-up resistor by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—

Notes 1. When the P07/XT1 pin is used as an input port, set the processor clock control register (PCC) bit 6 (FRC) to 1 (Be sure not to use the feedback resistor of the subsystem clock oscillator).

2. When the P10/ANI0 to P17/ANI7 pins are used as the analog inputs for the A/D converter, the pull-up resistor is automatically disabled.

(1) Port pins (2/3)

Pin Name	Input/Output	Function		After Reset	Alternate Function
P40 to P47	Input/output	Port 4 8-bit input/output port Input/output is specifiable in 8-bit units. When used as the input port, it is possible to connect an on-chip pull-up resistor by software. Set test input flag (KRIF) to 1 by falling edge detection.		Input	AD0 to AD7
P50 to P57	Input/output	Port 5 8-bit input/output port It is possible to directly drive LEDs. Input/output is specifiable bit-wise. When used as the input port, it is possible to connect an on-chip pull-up resistor by software.		Input	A8 to A15
P60	Input/output	Port 6 8-bit input/output port Input/output is specifiable bit-wise.	N-ch open-drain input/output port. It is possible to directly drive LEDs.	Input	—
P61					
P62					
P63					
P64			When used as the input port, it is possible to connect an on-chip pull-up resistor by software.	Input	$\overline{RD}$
P65					$\overline{WR}$
P66					$\overline{WAIT}$
P67					ASTB
P70	Input/output	Port 7 3-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect an on-chip pull-up resistor by software.		Input	SI2/RxD
P71					SO2/TxD
P72					$\overline{SCK2}$/ASCK
P80 to P87	Input/output	Port 8 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect an on-chip pull-up resistor by software.		Input	A0 to A7
P90	Input/output	Port 9 7-bit input/output port Input/output is specifiable bit-wise.	N-ch open-drain input/output port. It is possible to directly drive LEDs.	Input	—
P91					
P92					
P93					
P94			When used as the input port, it is possible to connect an on-chip pull-up resistor by software.		
P95					
P96					

(1) Port pins (3/3)

Pin Name	Input/Output	Function	After Reset	Alternate Function
P100	Input/output	Port 10 4-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect an on-chip pull-up resistor by software.	Input	TI5/TO5
P101				TI6/TO6
P102, P103				—
P120 to P127	Input/output	Port 12 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect an on-chip pull-up resistor by software.	Input	RTP0 to RTP7
P130, P131	Input/output	Port 13 2-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to connect an on-chip pull-up resistor by software.	Input	ANO0, ANO1

(2) Non-port pins (1/2)

Pin Name	Input/Output	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input by which the active edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
INTP6				P06
SI0	Input	Serial interface serial data input.	Input	P25/SB0/SDA0
SI1				P20
SI2				P70/RxD
SO0	Output	Serial interface serial data output.	Input	P26/SB1/SDA1
SO1				P21
SO2				P71/TxD
SB0	Input/Output	Serial interface serial data input/output.	Input	P25/SI0/SDA0
SB1				P26/SO0/SDA1
SDA0				P25/S10/SB0
SDA1				P26/SO0/SB1
$\overline{SCK0}$	Input/Output	Serial interface serial clock input/output.	Input	P27/SCL
$\overline{SCK1}$				P22
$\overline{SCK2}$				P72/ASCK
SCL				P27/$\overline{SCK0}$
STB	Output	Serial interface automatic transmit/receive strobe output.	Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input.	Input	P24
RxD	Input	Asynchronous serial interface serial data input.	Input	P70/SI2
TxD	Output	Asynchronous serial interface serial data output.	Input	P71/SO2
ASCK	Input	Asynchronous serial interface serial clock input.	Input	P72/SCK2
TI00	Input	External count clock input to 16-bit timer (TM0).	Input	P00/INTP0
TI01		Capture trigger signal input to capture register (CR00).		P01/INTP1
TI1		External count clock input to 8-bit timer (TM1).		P33
TI2		External count clock input to 8-bit timer (TM2).		P34
TI5		External count clock input to 8-bit timer (TM5).		P100/TO5
TI6		External count clock input to 8-bit timer (TM6).		P101/TO6
TO0	Output	16-bit timer (TM0) output (also used for 14-bit PWM output).	Input	P30
TO1		8-bit timer (TM1) output.		P31
TO2		8-bit timer (TM2) output.		P32
TO5		8-bit timer (TM5) output (also used for 8-bit PWM output).		P100/TI5
TO6		8-bit timer (TM6) output (also used for 8-bit PWM output).		P101/TI6
PCL	Output	Clock output (for main system clock, subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
RTP0 to RTP7	Output	Real-time output port by which data is output in synchronization with a trigger.	Input	P120 to P127
AD0 to AD7	Input/Output	Low-order address/data bus at external memory expansion.	Input	P40 to P47

(2) Non-port pins (2/2)

Pin Name	Input/Output	Function	After Reset	Alternate Function
A0 to A7	Output	Low-order address bus at external memory expansion.	Input	P80 to P87
A8 to A15	Output	High-order address bus at external memory expansion.	Input	P50 to P57
$\overline{RD}$	Output	External memory read operation strobe signal output.	Input	P64
$\overline{WR}$		External memory write operation strobe signal output.	Input	P65
$\overline{WAIT}$	Input	Wait insertion at external memory access.	Input	P66
ASTB	Output	Strobe output which latches the address data output for ports 4, 5 and 8 to access external memory.	Input	P67
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
ANO0, ANO1	Output	D/A converter analog output.	Input	P130, P131
AV_{REF0}	Input	A/D converter reference voltage input.	—	—
AV_{REF1}	Input	D/A converter reference voltage input.	—	—
AV_{DD}	—	A/D converter analog power supply. Connected to V_{DD}.	—	—
AV_{SS}	—	A/D and D/A converters ground potential. Connected to V_{SS}.	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection.	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection.	Input	P07
XT2	—		—	—
V_{DD}	—	Positive power supply.	—	—
V_{PP}	—	High-voltage applied during program write/verification. Connected directly to V_{SS} in normal operating mode.	—	—
V_{SS}	—	Ground potential.	—	—

2.2 Pins in PROM Programming Mode

Pin Name	Input/Output	Function
$\overline{RESET}$	Input	PROM programming mode setting When +5 V or +12.5 V is applied to the V_{PP} pin and a low level signal is applied to the $\overline{RESET}$ pin, this chip is set in the PROM programming mode.
V_{PP}	Input	PROM programming mode setting and high-voltage applied during program write/verification.
A0 to A16	Input	Address bus
D0 to D7	Input/output	Data bus
$\overline{CE}$	Input	PROM enable input/program pulse input
$\overline{OE}$	Input	Read strobe input to PROM
$\overline{PGM}$	Input	Program/program inhibit input in PROM programming mode.
V_{DD}	—	Positive power supply
V_{SS}	—	Ground potential

2.3 Pin Input/Output Circuits and Recommended Connection of Unused Pins

Types of input/output circuits of the pins and recommended connection of unused pins are shown in Table 2-1. For the configuration of each type of input/output circuit, see Figure 2-1.

Table 2-1. Type of Input/Output Circuit of Each Pin (1/2)

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connection for Unused Pins
P00/INTP0/TI00	2	Input	Connect to V_{SS}.
P01/INTP1/TI01	8-A	Input/Output	Independently connect to V_{SS} via a resistor.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P06/INTP6			
P07/XT1	16	Input	Connect to V_{DD}.
P10/ANI0 to P17/ANI7	11	Input/Output	Independently connect to V_{DD} or V_{SS} via a resistor.
P20/SI1	8-A		
P21/SO1	5-A		
P22/$\overline{SCK1}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0/SDA0	10-A		
P26/SO0/SB1/SDA1			
P27/$\overline{SCK0}$/SCL			
P30/TO0	5-A		
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0 to P47/AD7	5-E	Input/Output	Independently connect to V_{DD} via a resistor.
P50/A8 to P57/A15	5-A	Input/Output	Independently connect to V_{DD} or V_{SS} via a resistor.
P60 to P63	13-D	Input/Output	Independently connect to V_{DD} via a resistor.
P64/$\overline{RD}$	5-A	Input/Output	Independently connect to V_{DD} or V_{SS} via a resistor.
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			

Table 2-1. Type of Input/Output Circuit of Each Pin (2/2)

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connection for Unused Pins
P70/SI2/RxD	8-A	Input/Output	Independently connect to V_{DD} or V_{SS} via a resistor.
P71/SO2/TxD	5-A		
P72/$\overline{SCK2}$/ASCK	8-A		
P80/A0 to P87/A7	5-A		
P90 to P93	13-D	Input/Output	Independently connect to V_{DD} via a resistor.
P94 to P96	5-A	Input/Output	Independently connect to V_{DD} or V_{SS} via a resistor.
P100/TI5/TO5	8-A		
P101/TI6/TO6			
P102, P103	5-A		
P120/RTP0 to P127/RTP7	5-A		
P130/ANO0, P131/ANO1	12-A	Input/Output	Independently connect to V_{SS} via a resistor.
$\overline{RESET}$	2	Input	—
XT2	16	—	Leave open.
AV_{REF0}	—		Connect to V_{SS}.
AV_{REF1}			Connect to V_{DD}.
AV_{DD}			
AV_{SS}			Connect to V_{SS}.
V_{PP}			Connect directly to V_{SS}.

Figure 2-1. List of Pin Input/Output Circuits (1/2)

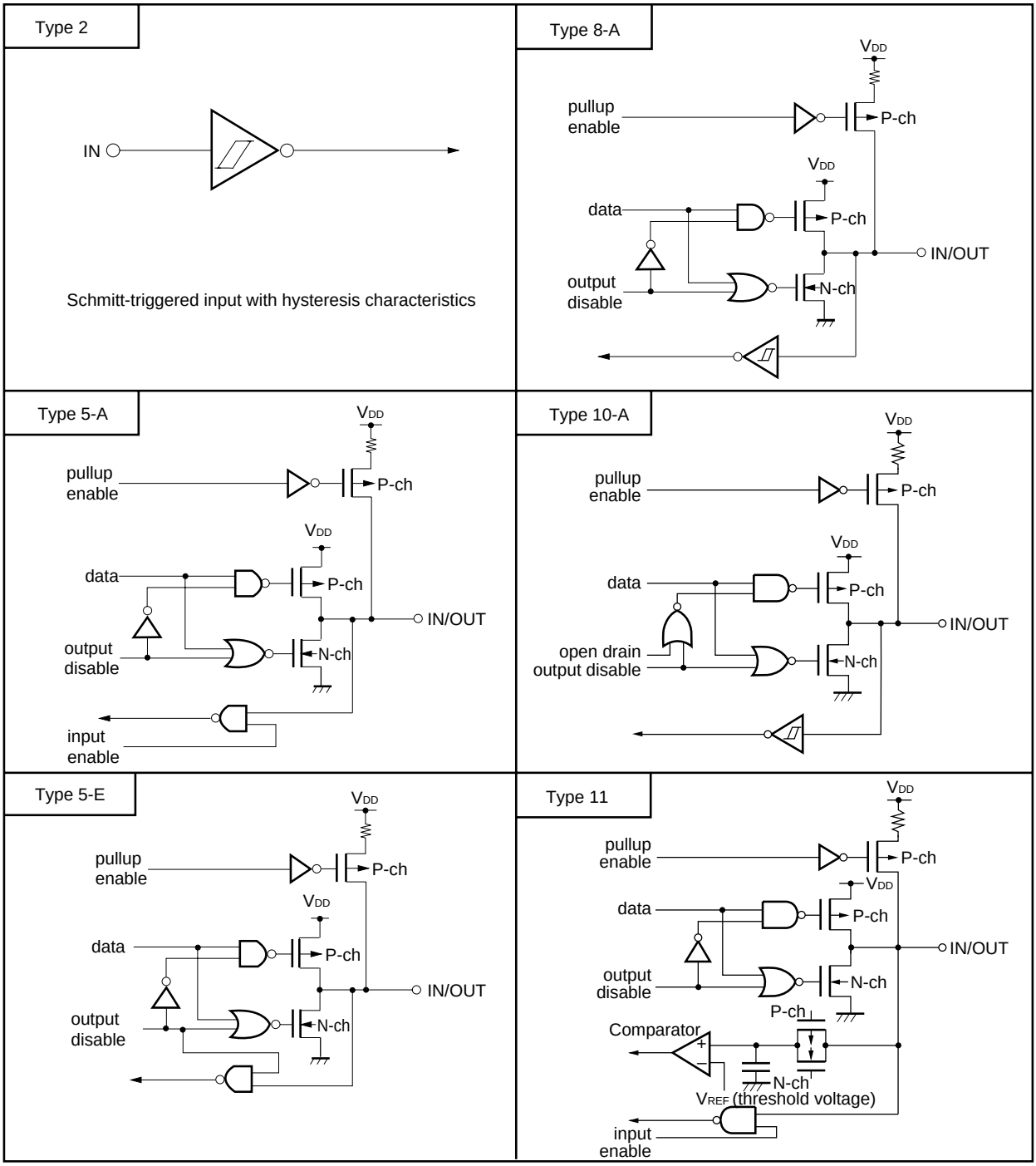
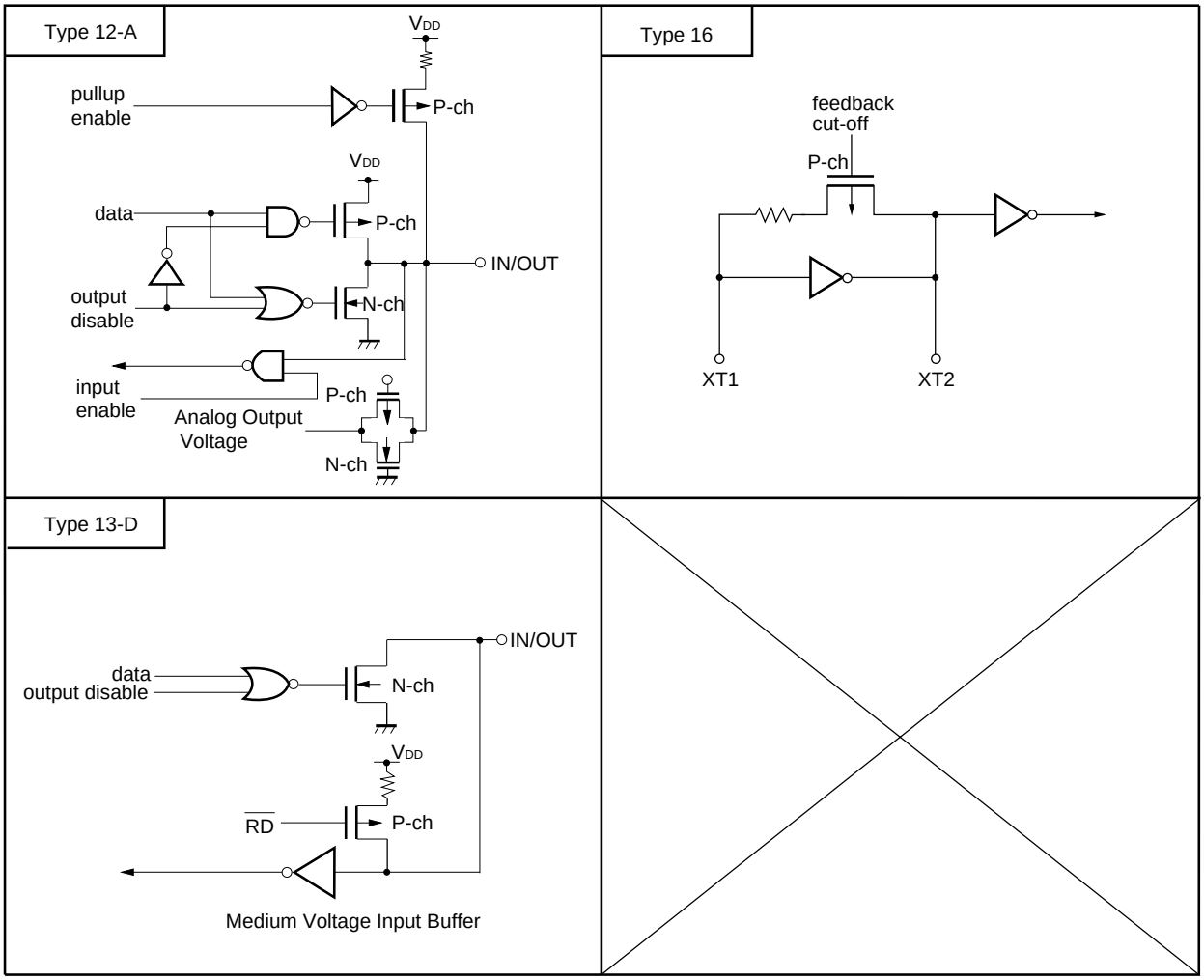


Figure 2-1. List of Pin Input/Output Circuits (2/2)



3. MEMORY SIZE SWITCHING REGISTER (IMS)

This is a register to disable use of part of internal memories by software. By setting this memory size switching register (IMS), it is possible to get the same memory mapping as that of the mask ROM versions with a different internal memory (ROM).

IMS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets IMS to CFH.

Figure 3-1. Memory Size Switching Register Format

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

ROM3	ROM2	ROM1	ROM0	Selection of internal ROM Capacity
1	0	0	0	32 Kbytes
1	0	1	0	40 Kbytes
1	1	0	0	48 Kbytes
1	1	1	0	56 Kbytes[Note]
1	1	1	1	60 Kbytes
Other than above				Setting prohibited

RAM2	RAM1	RAM0	Selection of Internal High-Speed RAM Capacity
1	1	0	1024 bytes
Other than above			Setting prohibited

Note When the external device expansion function is used, the internal ROM capacity should be set to 56 Kbytes or less.

Table 3-1 shows the setting values of IMS which make the memory mapping the same as that of the mask ROM version.

Table 3-1. Memory Size Switching Register Setting Values

Target Mask ROM Versions	IMS Setting Value
μPD78074BY	C8H
μPD78075BY	CAH
μPD78076Y	CCH
μPD78078Y	CFH

4. INTERNAL EXPANSION RAM SIZE SWITCHING REGISTER (IXS)

This register is used to set the internal expansion RAM capacity by software. By setting this internal expansion RAM size switching register (IXS), it is possible to get the same memory mapping as that of the mask ROM versions with a different internal expansion RAM.

IXS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets 0AH.

Figure 4-1. Internal Expansion RAM Size Switching Register Format

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IXS	0	0	0	0	IXRAM3	IXRAM2	IXRAM1	IXRAM0	FFF4H	0AH	W

IXRAM3	IXRAM2	IXRAM1	IXRAM0	Internal expansion RAM capacity selection
1	1	0	0	0 bytes
1	0	1	0	1024 bytes
Other than above				Setting prohibited

Table 4-1 shows the setting values of IXS which make the memory mapping the same as that of the mask ROM versions.

Table 4-1. Internal Expansion RAM Size Switching Register Setting Values

Target Mask ROM Versions	IXS Setting Value
μPD78074BY	0CH[Note]
μPD78075BY	
μPD78076Y	0AH
μPD78078Y	

Note If a program for the μPD78P078 in which "MOV IXS, #0CH" is written is executed in the μPD78074BY and μPD78075BY, the operations are not affected.

5. PROM PROGRAMMING

The μPD78P078Y has an on-chip 60-Kbyte PROM as a program memory. For programming, set the PROM programming mode with the V_{PP} and $\overline{RESET}$ pins. For the connection of unused pins, refer to **"PIN CONFIGURATIONS (2) PROM programming mode."**

Caution Programs must be written in addresses 0000H to EFFFH (The last address EFFFH must be specified). They cannot be written by a PROM programmer which cannot specify the write address.

5.1 Operating Modes

When +5 V or +12.5 V is applied to the V_{PP} pin and a low-level signal is applied to the $\overline{RESET}$ pin, the PROM programming mode is set. This mode will become the operating mode as shown in Table 5-1 when the $\overline{CE}$, $\overline{OE}$ and $\overline{PGM}$ pins are set as shown.

Further, when the read mode is set, it is possible to read the contents of the PROM.

Table 5-1. Operating Modes of PROM Programming

Pin / Operating Mode	$\overline{RESET}$	V_{PP}	V_{DD}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	D0 to D7
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High-impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				×	H	H	High-impedance
				×	L	L	
Read		+5 V	+5 V	L	L	H	Data output
Output disable				L	H	×	High-impedance
Standby				H	×	×	High-impedance

× : L or H

(1) Read mode

Read mode is set by setting $\overline{CE}$ = L, $\overline{OE}$ = L.

(2) Output disable mode

Data output becomes high-impedance and is placed in the output disable mode by setting $\overline{OE}$ = H.

Therefore, if multiple μPD78P078Ys are connected to the data bus, data can be read from any device by controlling the $\overline{OE}$ pin.

(3) Standby mode

Standby mode is set by setting $\overline{CE}$ = H.

In this mode, data outputs become high-impedance irrespective of the $\overline{OE}$ status.

(4) Page data latch mode

Page data latch mode is set by setting $\overline{CE}$ = H, $\overline{PGM}$ = H, $\overline{OE}$ = L at the beginning of page write mode.

In this mode, 1 page 4-byte data is latched in an internal address/data latch circuit.

(5) Page write mode

After 1 page 4 bytes of addresses and data are latched in the page data latch mode, a page write is executed by applying a 0.1-ms program pulse (active low) to the $\overline{PGM}$ pin with $\overline{CE}$ = H, $\overline{OE}$ = H. Then, program verification can be performed by setting $\overline{CE}$ = L, $\overline{OE}$ = L.

If programming is not performed by a one-time program pulse, X times ($X \leq 10$) write and verification operations should be executed repeatedly.

(6) Byte write mode

Byte write is executed when a 0.1-ms program pulse (active low) is applied to the $\overline{PGM}$ pin with $\overline{CE}$ = L, $\overline{OE}$ = H. Then, program verification can be performed by setting $\overline{OE}$ = L.

If programming is not performed by a one-time program pulse, X times ($X \leq 10$) write and verification operations should be executed repeatedly.

(7) Program verify mode

Program verify mode is set by setting $\overline{CE}$ = L, $\overline{PGM}$ = H, $\overline{OE}$ = L.

In this mode, check if a write operation is performed correctly after the write.

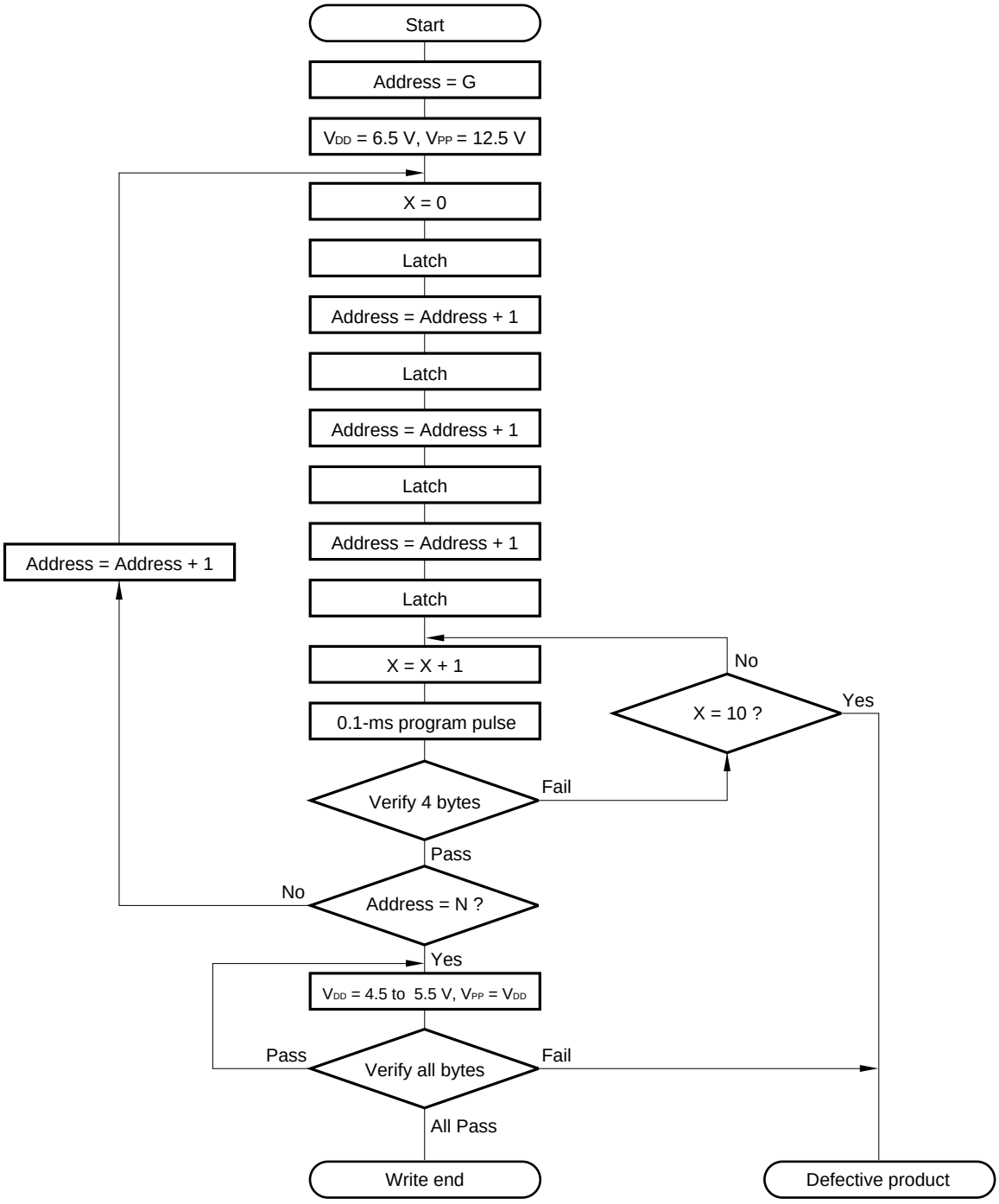
(8) Program inhibit mode

Program inhibit mode is used when the $\overline{OE}$ pin, V_{PP} pin and D0 to D7 pins of multiple μPD78P078Ys are connected in parallel and a write is performed to one of those devices.

When a write operation is performed, the page write mode or byte write mode described above is used. At this time, a write is not performed to a device which has the $\overline{PGM}$ pin driven high.

5.2 PROM Write Procedure

Figure 5-1. Page Program Mode Flow Chart



G = Start address
N = Program last address

Figure 5-2. Page Program Mode Timing

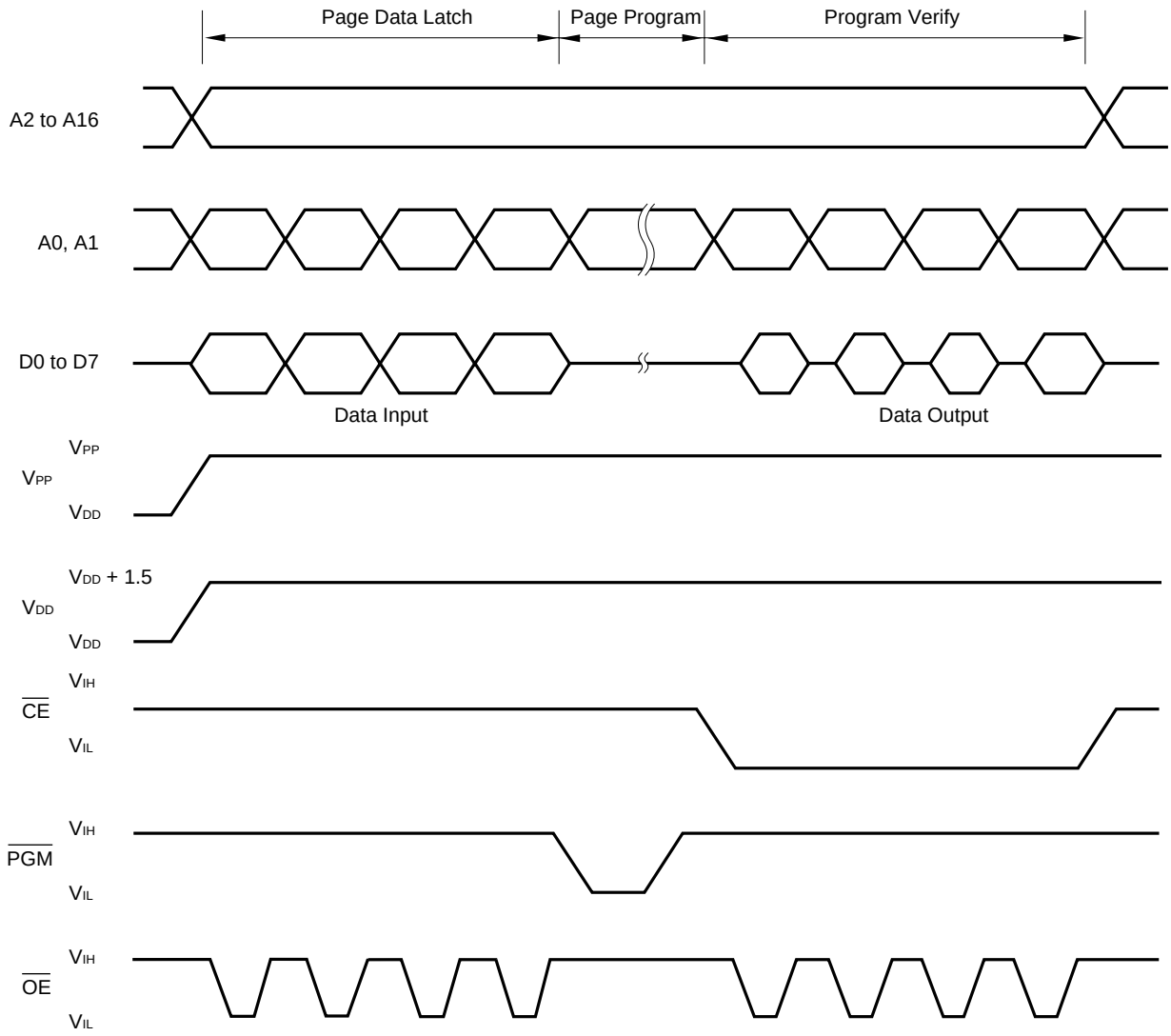
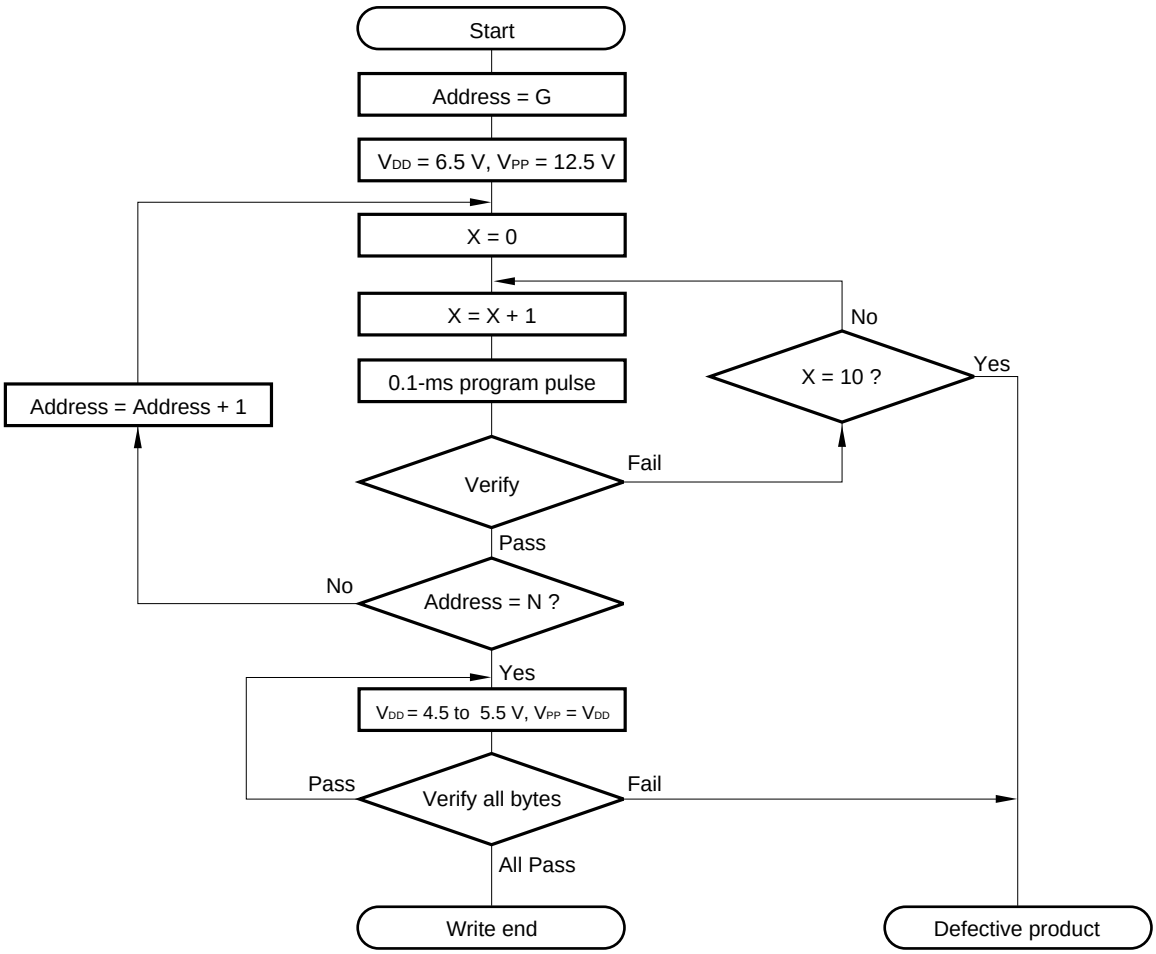


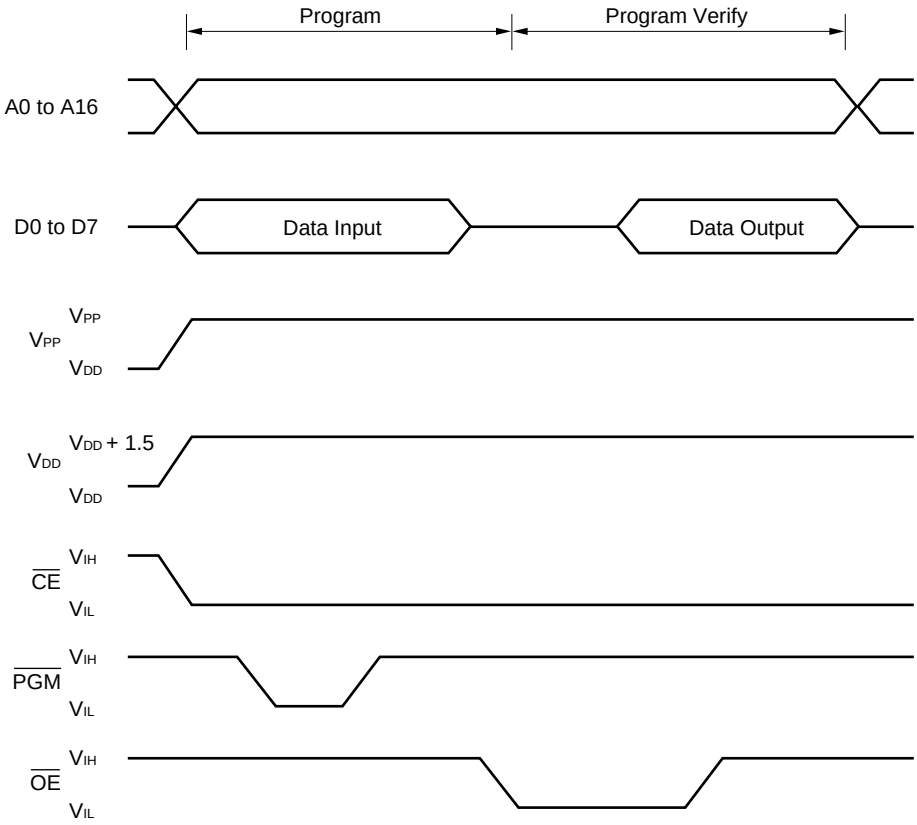
Figure 5-3. Byte Program Mode Flow Chart



G = Start address

N = Program last address

Figure 5-4. Byte Program Mode Timing



Cautions 1. V_{DD} should be applied before V_{PP} and removed after V_{PP}.

2. V_{PP} must not exceed +13.5 V including overshoot.

3. Reliability may be adversely affected if removal/reinsertion is performed while +12.5 V is being applied to V_{PP}.

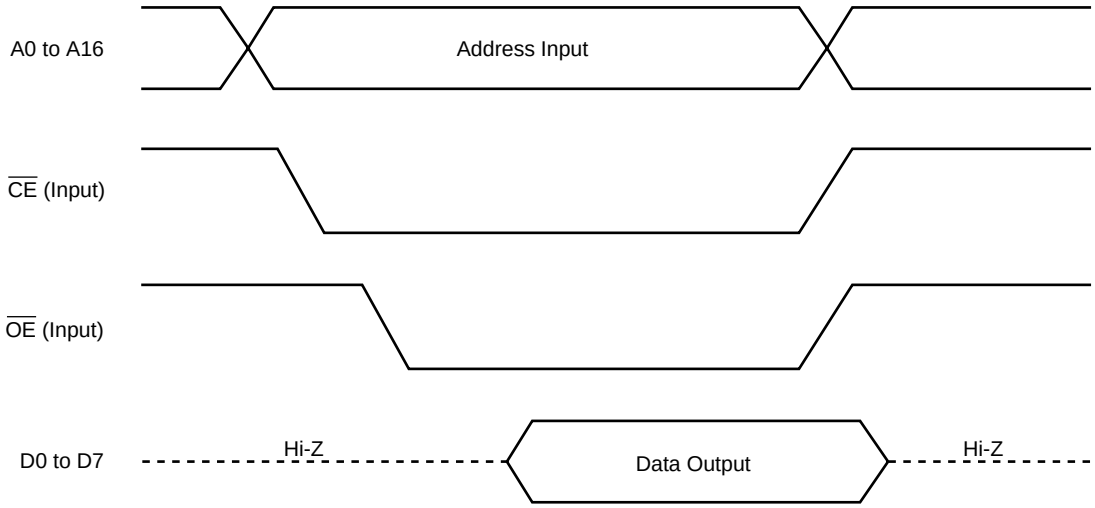
5.3 PROM Read Procedure

The contents of PROM are readable to the external data bus (D0 to D7) according to the read procedure shown below.

(1) Fix the $\overline{\text{RESET}}$ pin at low level, supply +5 V to the V_{PP} pin, and connect all other unused pins as shown in **"PIN CONFIGURATIONS (2) PROM programming mode".**
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) Input address of read data into the A0 to A16 pins.
(4) Read mode
(5) Output data to D0 to D7 pins.

The timings of the above steps (2) to (5) are shown in Figure 5-5.

Figure 5-5. PROM Read Timings



6. PROGRAM ERASURE (μPD78P078YKL-T ONLY)

The μPD78P078YKL-T is capable of erasing the data written in a program memory (to FFH) and rewriting.

To erase the programmed data, expose the erasure window to light having a wavelength shorter than about 400 nm. Normally, irradiate ultraviolet rays of 254-nm wavelength. The amount of exposure required to completely erase the programmed data is as follows:

- UV intensity × erasing time: 30 W • s/cm^2 or more
- Erasure time: 40 min. or more (When a UV lamp of 12,000 μW/cm^2 is used. However, a longer time may be needed because of deterioration in performance of the UV lamp, soiled erasure window, etc.)

When erasing the contents of data, set up the UV lamp within 2.5 cm from the erasure window. Further, if a filter is provided for a UV lamp, irradiate the ultraviolet rays after removing the filter.

7. OPAQUE FILM ON ERASURE WINDOW (μPD78P078YKL-T ONLY)

To protect from unintentional erasure by rays other than that of the lamp for erasing EPROM contents, or to protect internal circuits other than EPROM from misoperating by rays, cover the erasure window with an opaque film when EPROM contents erasure is not performed.

8. ONE-TIME PROM VERSION SCREENING

The one-time PROM version (μPD78P078YGC-8EU, 78P078YGF-3BA) cannot be tested completely by NEC before it is shipped, because of its structure. It is recommended to perform screening to verify PROM after writing necessary data and performing high-temperature storage under the condition below.

Storage Temperature	Storage Time
125°C	24 hours

NEC offers for an additional fee services from one-time PROM writing to marking, screening, and verify for products designated as “QTOP Microcontroller”. For details, contact an NEC sales representative.

9. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Test Conditions			Ratings	Unit
Supply voltage	V_{DD}				–0.3 to +7.0	V
	V_{PP}				–0.3 to +13.5	V
	AV_{DD}				–0.3 to V_{DD} + 0.3	V
	AV_{REF0}				–0.3 to V_{DD} + 0.3	V
	AV_{REF1}				–0.3 to V_{DD} + 0.3	V
	AV_{SS}				–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131, X1, X2, XT2, $\overline{\text{RESET}}$			–0.3 to V_{DD} + 0.3	V
	V_{I2}	P60 to P63, P90 to 93	N-ch open-drain		–0.3 to +16	V
	V_{I3}	A9	PROM programming mode		–0.3 to +13.5	V
Output voltage	V_O				–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pins		AV_{SS} – 0.3 to AV_{REF0} + 0.3	V
Output current, high	I_{OH}	Per pin			–10	mA
		Total for P30 to P37, P56, P57, P60 to P67, P90 to P96, P100 to P103, P120 to P127			–15	mA
		Total for P01 to P06, P10 to P17, P20 to P27, P40 to P47, P50 to P55, P70 to P72, P80 to P87, P130, P131			–15	mA
Output current, low	I_{OL}[Note]	Per pin		Peak value	30	mA
				r.m.s. value	15	mA
		Total for P50 to P55		Peak value	100	mA
				r.m.s. value	70	mA
		Total for P56, P57, P60 to P63		Peak value	100	mA
				r.m.s. value	70	mA
		Total for P30 to P37, P64 to P67, P90 to P96, P100 to P103, P120 to P127		Peak value	100	mA
				r.m.s. value	70	mA
		Total for P20 to P27, P40 to P47, P80 to P87		Peak value	50	mA
				r.m.s. value	20	mA
		Total for P01 to P06, P10 to P17, P70 to P72, P130, P131		Peak value	50	mA
				r.m.s. value	20	mA
Operating ambient temperature	T_A				–40 to +85	°C
Storage temperature	T_{stg}				–65 to +150	°C

Note The r.m.s. (root mean square) value should be calculated as follows: [r.m.s. value] = [Peak value] $\times\sqrt{\text{Duty}}$

Caution Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.

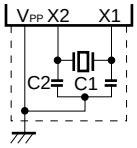
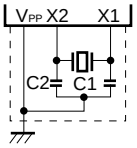
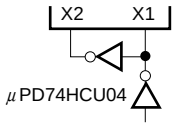
Remark Unless otherwise specified, alternate-function pin characteristics are the same as port pin characteristics.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz, Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C_{IO}	f = 1 MHz, Unmeasured pins returned to 0 V.	P01 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131			15	pF
			P60 to P63, P90 to P93			20	pF

Remark Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1	V_{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization timeNote 2	After V_{DD} came to MIN. of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f_X)Note 1		1.0		5.0	MHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X)Note 1		1.0		5.0	MHz
		X1 input high- and low-level widths (t_{XH}, t_{XL})		85		500	ns

Notes 1. Only the oscillator characteristics are shown. For the instruction execution time, refer to **AC Characteristics**.

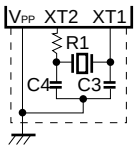
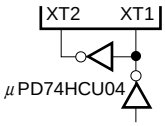
2. Time required for oscillation to stabilize after a reset or the STOP mode has been released.

Cautions 1. When using the oscillation circuit of the main system clock, wire the portion enclosed in broken lines in the figures as follows to avoid adverse influences on the wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring over other signal lines.**
- **Do not route the wiring in the vicinity of lines through which a high fluctuating current flows.**
- **Always keep the ground point of the capacitor of the oscillation circuit at the same potential as V_{SS}.**
- **Do not connect the power source pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT})Note 1		32		100	kHz
		XT1 input high-, low-level widths (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Only the oscillator characteristics are shown. For the instruction execution time, refer to **AC Characteristics**.

2. Time required for oscillation to stabilize after V_{DD} reaches the minimum value of the oscillation voltage range.

Cautions 1. When using the oscillation circuit of the subsystem clock, wire the portion enclosed in broken lines in the figures as follows to avoid adverse influences on the wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring over other signal lines.**
- **Do not route the wiring in the vicinity of lines through which a high fluctuating current flows.**
- **Always keep the ground point of the capacitor of the oscillation circuit at the same potential as V_{SS}.**
- **Do not connect the power source pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

2. The amplification factor of the subsystem clock oscillator is designed to be low to reduce the current consumption and therefore, the subsystem clock oscillator is influenced by noise more easily than the main system clock oscillator. When using the subsystem clock, therefore, exercise utmost care in wiring the circuit.

Recommended Oscillator Constant

Main System Clock : Ceramic Resonator (T_A = –40 to +85°C)

Manufacturer	Part number	Frequency	Recommended circuit constant			Oscillation voltage range		Remarks
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)	
TDK	CCR1000K2	1.00 MHz	150	150	0	2.0	5.5	On-chip capacitor
	CCR2.0MC3	2.00 MHz	On-chip	On-chip	0	2.0	5.5	On-chip capacitor surface mount type
	CCR4.0MC3	4.00 MHz	On-chip	On-chip	0	2.0	5.5	On-chip capacitor surface mount type
	FCR4.0MC5	4.00 MHz	On-chip	On-chip	0	2.0	5.5	On-chip capacitor insertion type
Murata Mfg. Corporation	CSB1000J	1.00 MHz	100	100	5.6	1.8	5.5	Insertion type
	CSA2.00MG040	2.00 MHz	100	100	0	1.8	5.5	Insertion type
	CST2.00MG040	2.00 MHz	On-chip	On-chip	0	1.8	5.5	On-chip capacitor insertion type
	CSA4.00MG	4.00 MHz	30	30	0	1.8	5.5	Insertion type
	CST4.00MGW	4.00 MHz	On-chip	On-chip	0	1.8	5.5	On-chip capacitor insertion type
	CSA4.00MGU	4.00 MHz	30	30	0	1.8	5.5	Insertion type
	CST4.00MGWU	4.00 MHz	On-chip	On-chip	0	1.8	5.5	On-chip capacitor insertion type

Main System Clock : Ceramic Resonator (T_A = –20 to +80°C)

Manufacturer	Part number	Frequency	Recommended circuit constant			Oscillation voltage range		Remarks
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)	
Kyocera Corporation	KFR-1000F	1.00 MHz	220	220	0	1.8	5.5	Insertion type
	PBR-1000Y	1.00 MHz	220	220	0	1.8	5.5	Surface mount type
	KBR-2.0MS	2.00 MHz	82	82	0	1.8	5.5	Insertion type
	KBR-4.0MKC	4.00 MHz	On-chip	On-chip	0	1.8	5.5	On-chip capacitor insertion type
	KBR-4.0MSB	4.00 MHz	33	33	0	1.8	5.5	Insertion type
	PBRC4.00B	4.00 MHz	On-chip	On-chip	0	1.8	5.5	On-chip capacitor surface mount type
	PBRC4.00A	4.00 MHz	33	33	0	1.8	5.5	Surface mount type

Caution The oscillator constant and oscillation voltage range indicate conditions for stable oscillation. The oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation frequency must be adjusted on the implementation circuit. For details, please contact directly the manufacturer of the resonator you will use.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P80 to P87, P94 to P96, P102, P103, P120 to P127, P130, P131	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				0.8V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, P100, P101, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
				0.85V_{DD}		V_{DD}	V
	V_{IH3}	P60 to P63, P90 to P93 (N-ch open-drain)	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		15	V
				0.8V_{DD}		15	V
	V_{IH4}	X1, X2	V_{DD} = 2.7 to 5.5 V	V_{DD}–0.5		V_{DD}	V
				V_{DD}–0.2		V_{DD}	V
	V_{IH5}	XT1/P07, XT2	4.5 V ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0.9V_{DD}		V_{DD}	V
			Note	0.9V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P80 to P87, P94 to P96, P102, P103, P120 to P127, P130, P131	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				0		0.2V_{DD}	V
	V_{IL2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, P100, P101, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
				0		0.15V_{DD}	V
	V_{IL3}	P60 to P63, P90 to P93 (N-ch open-drain)	4.5 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0		0.2V_{DD}	V
				0		0.1V_{DD}	V
	V_{IL4}	X1, X2	V_{DD} = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
	V_{IL5}	XT1/P07, XT2	4.5 V ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0		0.1V_{DD}	V
			Note	0		0.1V_{DD}	V
Output voltage, high	V_{OH}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD}–1.0			V
		I_{OH} = –100 μA		V_{DD}–0.5			V

Note When used as P07, the reverse phase of P07 should be input to XT2 pin using an inverter.

Remark Unless otherwise specified, alternate-function pin characteristics are the same as port pin characteristics.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, low	V_{OL1}	P50 to P57, P60 to P63, P90 to P93	V_{DD} = 4.5 to 5.5 V, I_{OL} = 15 mA		0.4	2.0	V
		P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{SCK0}$	V_{DD} = 4.5 to 5.5 V, open-drain, pulled up (R = 1 kΩ)			$0.2V_{DD}$	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V
Input leakage current, high	I_{LIH1}	V_{IN} = V_{DD}	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131, $\overline{RESET}$			3	μA
	I_{LIH2}		X1, X2, XT1/P07, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P60 to P63, P90 to P93			80	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131, $\overline{RESET}$			–3	μA
	I_{LIL2}		X1, X2, XT1/P07, XT2			–20	μA
	I_{LIL3}		P60 to P63, P90 to P93			–3[Note]	μA
Output leakage current, high	I_{LOH}	V_{OUT} = V_{DD}				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA

Note The value is –200 μA (MAX.) only for 1.5 clock cycles (no wait) when read-out instruction is executed to port 6 (P6), port mode register 6 (PM6), port 9 (P9) and port mode register 9 (PM9). For cases other than the 1.5 clock cycles of read-out instruction execution, the value is –3 μA (MAX.).

Remark Unless otherwise specified, alternate-function pin characteristics are the same as port pin characteristics.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Software pull-up resistor[Note 1]	R	V_{IN} = 0 V, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P80 to P87, P94 to P96, P100 to P103, P120 to P127, P130, P131	4.5 V ≤ V_{DD} ≤ 5.5 V	15	40	90	kΩ
			2.7 V ≤ V_{DD} < 4.5 V	20		500	kΩ
Supply current[Note 2]	I_{DD1}	5.0-MHz crystal oscillation operating mode (f_{XX} = 2.5 MHz)[Note 3]	V_{DD} = 5.0 V ± 10%[Note 6]		5.4	16.2	mA
			V_{DD} = 3.0 V ± 10%[Note 7]		0.8	2.4	mA
			V_{DD} = 2.2 V ± 10%[Note 7]		0.45	1.35	mA
		5.0-MHz crystal oscillation operating mode (f_{XX} = 5.0 MHz)[Note 4]	V_{DD} = 5.0 V ± 10%[Note 6]		9.5	28.5	mA
			V_{DD} = 3.0 V ± 10%[Note 7]		1.0	3.0	mA
	I_{DD2}	5.0 MHz crystal oscillation HALT mode (f_{XX} = 2.5 MHz)[Note 3]	V_{DD} = 5.0 V ± 10%		1.4	4.2	mA
			V_{DD} = 3.0 V ± 10%		0.5	1.5	mA
			V_{DD} = 2.0 V ± 10%		280	840	μA
		5.0 MHz crystal oscillation HALT mode (f_{XX} = 5.0 MHz)[Note 4]	V_{DD} = 5.0 V ± 10%		1.6	4.8	mA
			V_{DD} = 3.0 V ± 10%		0.65	1.95	mA
★	I_{DD3}	32.768-kHz crystal oscillation operating mode[Note 5]	V_{DD} = 5.0 V ± 10%		135	270	μA
★			V_{DD} = 3.0 V ± 10%		95	190	μA
★			V_{DD} = 2.0 V ± 10%		70	140	μA
	I_{DD4}	32.768-kHz crystal oscillation HALT mode[Note 5]	V_{DD} = 5.0 V ± 10%		25	55	μA
			V_{DD} = 3.0 V ± 10%		5	15	μA
			V_{DD} = 2.0 V ± 10%		2.5	12.5	μA
	I_{DD5}	XT1 = V_{DD} STOP mode Feedback resistor used	V_{DD} = 5.0 V ± 10%		1	30	μA
			V_{DD} = 3.0 V ± 10%		0.5	10	μA
			V_{DD} = 2.0 V ± 10%		0.3	10	μA
	I_{DD6}	XT1 = V_{DD} STOP mode Feedback resistor not used	V_{DD} = 5.0 V ± 10%		0.1	30	μA
			V_{DD} = 3.0 V ± 10%		0.05	10	μA
			V_{DD} = 2.0 V ± 10%		0.05	10	μA

Notes 1. Software pull-up resistor can be used only within a range of V_{DD} = 2.7 to 5.5 V.

2. Supply current flowing to the V_{DD} pin. It excludes the current flowing to the A/D, D/A converters and on-chip pull-up resistors.

3. $f_{XX} = f_X/2$ operation (when oscillation mode selection register (OSMS) is set to 00H).

4. $f_{XX} = f_X$ operation (when OSMS is set to 01H).

5. When the main system clock is stopped.

6. High-speed mode operation (when processor clock control register (PCC) is set to 00H).

7. Low-speed mode operation (when PCC is set to 04H).

Remarks 1. Unless otherwise specified, alternate-function pin characteristics are the same as port pin characteristics.

2. f_{XX}: Main system clock frequency (f_X or $f_X/2$)

3. f_X: Main system clock oscillation frequency

AC Characteristics

(1) Basic Operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions			MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operating on main system clock	$f_{XX} = f_X/2$ (Note 1)	V_{DD} = 2.7 to 5.5 V	0.8		64	μs
					2.0		64	μs
			$f_{XX} = f_X$ (Note 2)	3.5 V ≤ V_{DD} ≤ 5.5 V	0.4		32	μs
				2.7 V ≤ V_{DD} < 3.5 V	0.8		32	μs
		Operating on subsystem clock			40	122	125	μs
TI00 input high-/low-level widths	t_{TIH00}, t_{TIL00}	3.5 V ≤ V_{DD} ≤ 5.5 V			2/fsam+0.1 (Note 3)			μs
		2.7 V ≤ V_{DD} < 3.5 V			2/fsam+0.2 (Note 3)			μs
					2/fsam+0.5 (Note 3)			μs
TI01 input high-/low-level widths	t_{TIH01}, t_{TIL01}	V_{DD} = 2.7 to 5.5 V			10			μs
					20			μs
TI1, TI2, TI5, TI6 input frequency	f_{TI1}	V_{DD} = 4.5 to 5.5 V			0		4	MHz
					0		275	kHz
TI1, TI2, TI5, TI6 input high-/low-level widths	t_{TIH1}, t_{TIL1}	V_{DD} = 4.5 to 5.5 V			100			ns
					1.8			μs
Interrupt request input high-/low-level widths	t_{INTH}, t_{INTL}	INTP0		3.5 V ≤ V_{DD} ≤ 5.5 V	2/fsam+0.1 (Note 3)			μs
				2.7 V ≤ V_{DD} < 3.5 V	2/fsam+0.2 (Note 3)			μs
					2/fsam+0.5 (Note 3)			μs
		INTP1 to INTP6, P40 to P47		V_{DD} = 2.7 to 5.5 V	10			μs
					20			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}	V_{DD} = 2.7 to 5.5 V			10			μs
					20			μs

Notes 1. When oscillation mode selection register (OSMS) is set to 00H.

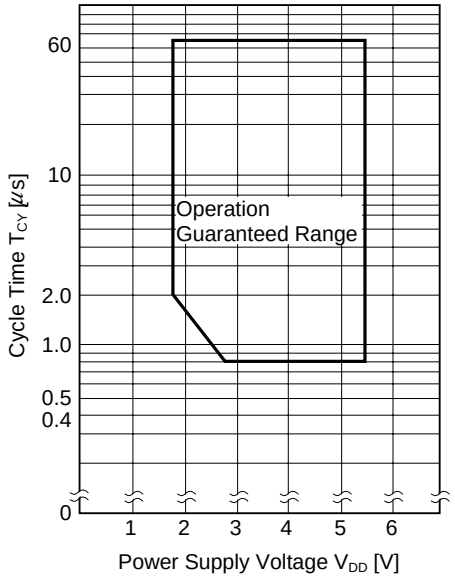
2. When OSMS is set to 01H.

3. f_{sam} can be selected as $f_{XX}/2^N$, $f_{XX}/32$, $f_{XX}/64$ or $f_{XX}/128$ (N = 0 to 4) by bits 0 and 1 (SCS0, SCS1) of the sampling clock selection register (SCS).

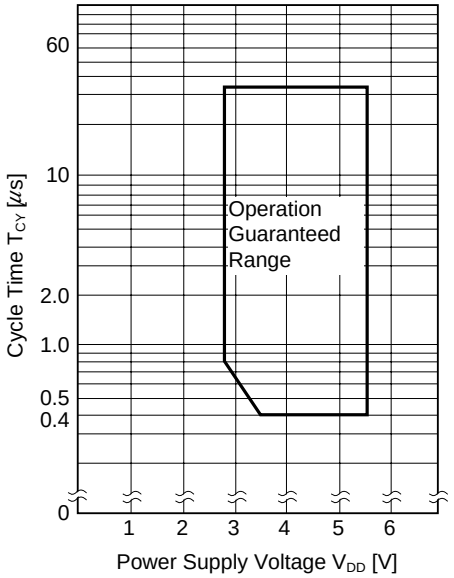
Remark f_{XX}: Main system clock frequency (f_X or $f_X/2$)

f_X: Main system clock oscillation frequency

T_{CY} vs. V_{DD}
(Main System Clock $f_{XX} = f_X/2$ Operation)



T_{CY} vs. V_{DD}
(Main System Clock $f_{XX} = f_X$ Operation)



(2) Read/Write Operation

(a) When MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.85t_{CY}$ – 50		ns
Address setup time	t_{ADS}		$0.85t_{CY}$ – 50		ns
Address hold time	t_{ADH}		50		ns
Address → Data input time	t_{ADD1}			(2.85 + 2n) t_{CY} – 80	ns
	t_{ADD2}			(4 + 2n) t_{CY} – 100	ns
$\overline{RD}$ ↓ → Data input time	t_{RDD1}			(2 + 2n) t_{CY} – 100	ns
	t_{RDD2}			(2.85 + 2n) t_{CY} – 100	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		(2 + 2n) t_{CY} – 60		ns
	t_{RDL2}		(2.85 + 2n) t_{CY} – 60		ns
$\overline{RD}$ ↓ → $\overline{WAIT}$ ↓ input time	t_{RDWT1}			$0.85t_{CY}$ – 50	ns
	t_{RDWT2}			$2t_{CY}$ – 60	ns
$\overline{WR}$ ↓ → $\overline{WAIT}$ ↓ input time	t_{WRWT}			$2t_{CY}$ – 60	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(1.15 + 2n) t_{CY}	(2 + 2n) t_{CY}	ns
Write data setup time	t_{WDS}		(2.85 + 2n) t_{CY} – 100		ns
Write data hold time	t_{WDH}	load resistance ≥ 5 kΩ	20		ns
$\overline{WR}$ low-level width	t_{WRL}		(2.85 + 2n) t_{CY} – 60		ns
ASTB ↓ → $\overline{RD}$ ↓ delay time	t_{ASTRD}		25		ns
ASTB ↓ → $\overline{WR}$ ↓ delay time	t_{ASTWR}		$0.85t_{CY}$ + 20		ns
In external fetch $\overline{RD}$ ↑ → ASTB ↑ delay time	t_{RDAST}		$0.85t_{CY}$ – 10	$1.15t_{CY}$ + 20	ns
In external fetch $\overline{RD}$ ↑ → address hold time	t_{RDADH}		$0.85t_{CY}$ – 50	$1.15t_{CY}$ + 50	ns
$\overline{RD}$ ↑ → write data output time	t_{RDWD}		40		ns
$\overline{WR}$ ↓ → write data output time	t_{WRWD}		0	50	ns
$\overline{WR}$ ↑ → address hold time	t_{WRADH}		$0.85t_{CY}$ – 20	$1.15t_{CY}$ + 40	ns
$\overline{WAIT}$↑ → $\overline{RD}$ ↑ delay time	t_{WTRD}		$1.15t_{CY}$ + 40	$3.15t_{CY}$ + 40	ns
$\overline{WAIT}$↑ → $\overline{WR}$ ↑ delay time	t_{WTWR}		$1.15t_{CY}$ + 30	$3.15t_{CY}$ + 30	ns

Remarks 1. MCS: Bit 0 of the oscillation mode selection register (OSMS)

2. PCC2 to PCC0: Bit 2 to bit 0 of the processor clock control register (PCC)

3. $t_{CY} = T_{CY}/4$

4. n indicates the number of waits.

(b) Except When MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		t_{CY} – 80		ns
Address setup time	t_{ADS}		t_{CY} – 80		ns
Address hold time	t_{ADH}		0.4t_{CY} – 10		ns
Address → Data input time	t_{ADD1}			(3 + 2n) t_{CY} – 160	ns
	t_{ADD2}			(4 + 2n) t_{CY} – 200	ns
$\overline{RD}$ ↓ → Data input time	t_{RDD1}			(1.4 + 2n) t_{CY} – 70	ns
	t_{RDD2}			(2.4 + 2n) t_{CY} – 70	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		(1.4 + 2n) t_{CY} – 20		ns
	t_{RDL2}		(2.4 + 2n) t_{CY} – 20		ns
$\overline{RD}$ ↓ → $\overline{WAIT}$ ↓ input time	t_{RDWT1}			t_{CY} – 100	ns
	t_{RDWT2}			2t_{CY} – 100	ns
$\overline{WR}$ ↓ → $\overline{WAIT}$ ↓ input time	t_{WRWT}			2t_{CY} – 100	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(1 + 2n) t_{CY}	(2 + 2n) t_{CY}	ns
Write data setup time	t_{WDS}		(2.4 + 2n) t_{CY} – 60		ns
Write data hold time	t_{WDH}	load resistance ≥ 5 kΩ	20		ns
$\overline{WR}$ low-level width	t_{WRL}		(2.4 + 2n) t_{CY} – 20		ns
ASTB ↓ → $\overline{RD}$ ↓ delay time	t_{ASTRD}		0.4t_{CY} – 30		ns
ASTB ↓ → $\overline{WR}$ ↓ delay time	t_{ASTWR}		1.4t_{CY} – 30		ns
In external fetch $\overline{RD}$ ↑ → ASTB ↑ delay time	t_{RDAST}		t_{CY} – 10	t_{CY} + 20	ns
In external fetch $\overline{RD}$ ↑ → address hold time	t_{RDADH}		t_{CY} – 80	t_{CY} + 50	ns
$\overline{RD}$ ↑ → write data output time	t_{RDWD}		0.4t_{CY} – 30		ns
$\overline{WR}$ ↓ → write data output time	t_{WRWD}		0	60	ns
$\overline{WR}$ ↑ → address hold time	t_{WRADH}		t_{CY} – 60	t_{CY} + 60	ns
$\overline{WAIT}$↑ → $\overline{RD}$ ↑ delay time	t_{WTRD}		0.6t_{CY} + 180	2.6t_{CY} + 180	ns
$\overline{WAIT}$↑ → $\overline{WR}$ ↑ delay time	t_{WTWR}		0.6t_{CY} + 120	2.6t_{CY} + 120	ns

Remarks 1. MCS: Bit 0 of the oscillation mode selection register (OSMS)

2. PCC2 to PCC0: Bit 2 to bit 0 of the processor clock control register (PCC)

3. $t_{CY} = T_{CY}/4$

4. n indicates the number of waits.

(3) Serial Interface (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) Serial Interface Channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$ ··· internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK0}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 4.5 to 5.5 V	t_{KCY1}/2–50			ns
			t_{KCY1}/2–100			ns
SI0 setup time (to $\overline{SCK0}$ ↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI0 hold time (from $\overline{SCK0}$ ↑)	t_{KSI1}		400			ns
$\overline{SCK0}$ ↓ → SO0 output delay time	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the SO0 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$ ··· external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK0}$ high-/low-level width	t_{KH2}, t_{KL2}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SI0 setup time (to $\overline{SCK0}$ ↑)	t_{SIK2}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI0 hold time (from $\overline{SCK0}$ ↑)	t_{KSI2}			400			ns
$\overline{SCK0}$ ↓ → SO0 output delay time	t_{KSO2}	C = 100 pF[Note]	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK0}$ rise, fall time	t_{R2}, t_{F2}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note C is the SO0 output line load capacitance.

(iii) 2-wire serial I/O mode ($\overline{SCK0}$ ··· internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	R = 1 kΩ, C = 100 pF[Note]	2.7 V ≤ V_{DD} ≤ 5.5 V	1600			ns
			2.0 V ≤ V_{DD} < 2.7 V	3200			ns
				4800			ns
$\overline{SCK0}$ high-level width	t_{KH3}		V_{DD} = 2.7 to 5.5 V	t_{KCY3}/2–160			ns
				t_{KCY3}/2–190			ns
$\overline{SCK0}$ low-level width	t_{KL3}		V_{DD} = 4.5 to 5.5 V	t_{KCY3}/2–50			ns
				t_{KCY3}/2–100			ns
SB0, SB1 setup time (to $\overline{SCK0}$ ↑)	t_{SIK3}		4.5 V ≤ V_{DD} ≤ 5.5 V	300			ns
			2.7 V ≤ V_{DD} < 4.5 V	350			ns
			2.0 V ≤ V_{DD} < 2.7 V	400			ns
				500			ns
SB0, SB1 hold time (from $\overline{SCK0}$ ↑)	t_{KSI3}			600			ns
$\overline{SCK0}$ ↓ → SB0, SB1 output delay time	t_{KSO3}			0		300	ns

Note R and C are the $\overline{SCK0}$, SB0, SB1 output line load resistance and load capacitance.

(iv) 2-wire serial I/O mode ($\overline{SCK0}$ ··· external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	2.7 V ≤ V_{DD} ≤ 5.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK0}$ high-level width	t_{KH4}	2.7 V ≤ V_{DD} ≤ 5.5 V		650			ns
		2.0 V ≤ V_{DD} < 2.7 V		1300			ns
				2100			ns
$\overline{SCK0}$ low-level width	t_{KL4}	2.7 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SB0, SB1 setup time (to $\overline{SCK0}$ ↑)	t_{SIK4}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SB0, SB1 hold time (from $\overline{SCK0}$ ↑)	t_{KSI4}			t_{KCY4}/2			ns
$\overline{SCK0}$ ↓ → SB0, SB1 output delay time	t_{KSO4}	R = 1 kΩ, C = 100 pF[Note]	4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
			2.0 V ≤ V_{DD} < 4.5 V	0		500	ns
						800	ns
$\overline{SCK0}$ rise, fall time	t_{R4}, t_{F4}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note R and C are the SB0, SB1 output line load resistance and load capacitance.

(v) I^2C bus mode (SCL ... internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF[Note]	2.7 V ≤ V_{DD} ≤ 5.5 V	10			μs
			2.0 V ≤ V_{DD} < 2.7 V	20			μs
				30			μs
SCL high-level width	t_{KH5}		V_{DD} = 2.7 to 5.5 V	t_{KCY5}–160			ns
				t_{KCY5}–190			ns
SCL low-level width	t_{KL5}		V_{DD} = 4.5 to 5.5 V	t_{KCY5}–50			ns
				t_{KCY5}–100			ns
SDA0, SDA1 setup time (to SCL↑)	t_{SIK5}		2.7 V ≤ V_{DD} ≤ 5.5 V	200			ns
			2.0 V ≤ V_{DD} < 2.7 V	300			ns
				400			ns
SDA0, SDA1 hold time (from SCL↓)	t_{KSI5}			0			ns
SCL↓→SDA0, SDA1 output delay time	t_{KS05}		4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
			2.0 V ≤ V_{DD} < 4.5 V	0		500	ns
				0		600	ns
SCL↑→SDA0, SDA1↓ or SCL↑→ SDA0, SDA1↑	t_{KSB}			200			ns
SDA0, SDA1↓→SCL↓	t_{SBK}		V_{DD} = 2.0 to 5.5 V	400			ns
				500			ns
SDA0, SDA1 high level width	t_{SBH}			500			ns

Note R and C are the SCL, SDA0, SDA1 output line load resistance and load capacitance.

(vi) I^2C bus mode (SCL ... external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY6}			1000			ns
SCL high-/low-level width	t_{KH6},	V_{DD} = 2.0 to 5.5 V		400			ns
	t_{KL6}			600			ns
SDA0, SDA1 setup time (to SCL↑)	t_{SIK6}	V_{DD} = 2.0 to 5.5 V		200			ns
				300			ns
SDA0, SDA1 hold time (from SCL↓)	t_{KSI6}			0			ns
SCL↓→SDA0, SDA1 output delay time	t_{KSO6}	R = 1 kΩ, C = 100 pF[Note]	4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
			2.0 V ≤ V_{DD} < 4.5 V	0		500	ns
				0		600	ns
SCL↑→SDA0, SDA1↓ or SCL↑→SDA0, SDA1↑	t_{KSB}			200			ns
SDA0, SDA1↓→SCL↓	t_{SBK}	V_{DD} = 2.0 to 5.5 V		400			ns
				500			ns
SDA0, SDA1 high-level width	t_{SBH}	V_{DD} = 2.0 to 5.5 V		500			ns
				800			ns
SCL rise, fall time	t_{R6},	When using external device expansion function				160	ns
	t_{F6}	When not using external device expansion function				1000	ns

Note R and C are the SDA0, SDA1 output line load resistance and load capacitance.

(b) Serial Interface Channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$ ··· internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY7}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK1}$ high-/low-level width	t_{KH7}, t_{KL7}	V_{DD} = 4.5 to 5.5 V	t_{KCY7}/2–50			ns
			t_{KCY7}/2–100			ns
SI1 setup time (to $\overline{SCK1}$ ↑)	t_{SIK7}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI1 hold time (from $\overline{SCK1}$ ↑)	t_{KSI7}		400			ns
$\overline{SCK1}$ ↓ → SO1 output delay time	t_{KSO7}	C = 100 pF[Note]			300	ns

Note C is the SO1 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$ ··· external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY8}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK1}$ high-/low-level width	t_{KH8}, t_{KL8}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SI1 setup time (to $\overline{SCK1}$ ↑)	t_{SIK8}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI1 hold time (from $\overline{SCK1}$ ↑)	t_{KSI8}			400			ns
$\overline{SCK1}$ ↓ → SO1 output delay time	t_{KSO8}	C = 100 pF[Note]	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK1}$ rise, fall time	t_{R8}, t_{F8}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note C is the SO1 output line load capacitance.

(iii) 3-wire serial I/O mode with automatic transmission/reception function ($\overline{SCK1}$ ··· internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK1}$ high-/low-level width	t_{KH9}, t_{KL9}	V_{DD} = 4.5 to 5.5 V	t_{KCY9}/2–50			ns
			t_{KCY9}/2–100			ns
SI1 setup time (to $\overline{SCK1}$ ↑)	t_{SIK9}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI1 hold time (from $\overline{SCK1}$ ↑)	t_{KSI9}		400			ns
$\overline{SCK1}$ ↓ → SO1 output delay time	t_{KSO9}	C = 100 pF[Note]			300	ns
$\overline{SCK1}$ ↑ → STB ↑	t_{SBD}		t_{KCY9}/2–100		t_{KCY9}/2+100	ns
Strobe signal high-level width	t_{SBW}	2.7 V ≤ V_{DD} ≤ 5.5 V	t_{KCY9}–30		t_{KCY9}+30	ns
		2.0 V ≤ V_{DD} < 2.7 V	t_{KCY9}–60		t_{KCY9}+60	ns
			t_{KCY9}–90		t_{KCY9}+90	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	200			ns
			300			ns
Busy inactive → $\overline{SCK1}$ ↓	t_{SPS}				2t_{KCY9}	ns

Note C is the SO1 output line load capacitance.

(iv) 3-wire serial I/O mode with automatic transmission/reception function ($\overline{SCK1}$ ··· external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK1}$ high-/low-level width	t_{KH10}, t_{KL10}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SI1 setup time (to $\overline{SCK1}$ ↑)	t_{SIK10}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI1 hold time (from $\overline{SCK1}$ ↑)	t_{KSI10}			400			ns
$\overline{SCK1}$ ↓ → SO1 output delay time	t_{KSO10}	C = 100 pF[Note]	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK1}$ rise, fall time	t_{R10}, t_{F10}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note C is the SO1 output line load capacitance.

(c) Serial Interface Channel 2

(i) 3-wire serial I/O mode ($\overline{SCK2}$ ··· internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY11}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
$\overline{SCK2}$ high-/low-level width	t_{KH11}, t_{KL11}	V_{DD} = 4.5 to 5.5 V	t_{KCY11}/2–50			ns
			t_{KCY11}/2–100			ns
SI2 setup time (to $\overline{SCK2}$ ↑)	t_{SIK11}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
		2.0 V ≤ V_{DD} < 2.7 V	300			ns
			400			ns
SI2 hold time (from $\overline{SCK2}$ ↑)	t_{KSI11}		400			ns
$\overline{SCK2}$ ↓ → SO2 output delay time	t_{KSO11}	C = 100 pF[Note]			300	ns

Note C is the SO2 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{SCK2}$ ··· external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY12}	4.5 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.7 V ≤ V_{DD} < 4.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{SCK2}$ high-/low-level width	t_{KH12}, t_{KL12}	4.5 V ≤ V_{DD} ≤ 5.5 V		400			ns
		2.7 V ≤ V_{DD} < 4.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SI2 setup time (to $\overline{SCK2}$ ↑)	t_{SIK12}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SI2 hold time (from $\overline{SCK2}$ ↑)	t_{KSI12}			400			ns
$\overline{SCK2}$ ↓ → SO2 output delay time	t_{KSO12}	C = 100 pF[Note]	V_{DD} = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{SCK2}$ rise, fall time	t_{R12}, t_{F12}	V_{DD} = 4.5 to 5.5 V When not using external device expansion function				1000	ns
						160	ns

Note C is the SO2 output line load capacitance.

(iii) UART mode (Dedicated baud rate generator output)

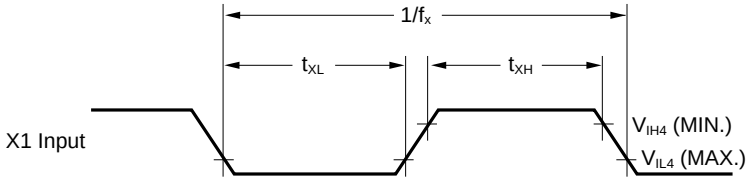
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.5 V ≤ V_{DD} ≤ 5.5 V			78125	bps
		2.7 V ≤ V_{DD} < 4.5 V			39063	bps
		2.0 V ≤ V_{DD} < 2.7 V			19531	bps
					9766	bps

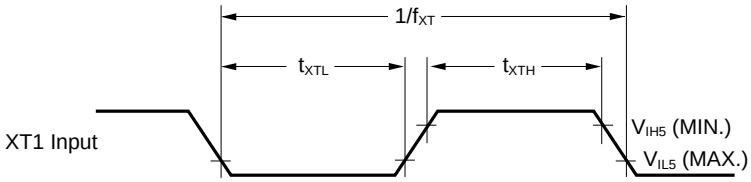
(iv) UART mode (External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY13}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
		2.0 V ≤ V_{DD} < 2.7 V	3200			ns
			4800			ns
ASCK high-/low-level width	t_{KH13}, t_{KL13}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
		2.0 V ≤ V_{DD} < 2.7 V	1600			ns
			2400			ns
Transfer rate		4.5 V ≤ V_{DD} ≤ 5.5 V			39063	bps
		2.7 V ≤ V_{DD} < 4.5 V			19531	bps
		2.0 V ≤ V_{DD} < 2.7 V			9766	bps
					6510	bps
ASCK rise, fall time	t_{R13}, t_{F13}	V_{DD} = 4.5 to 5.5 V When not using external device expansion function			1000	ns
					160	ns

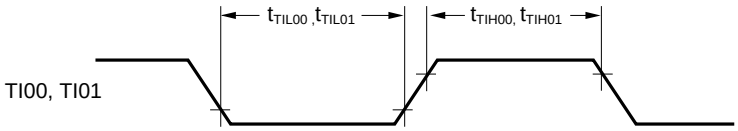
AC Timing Test Point (Excluding X1, XT1 Input)

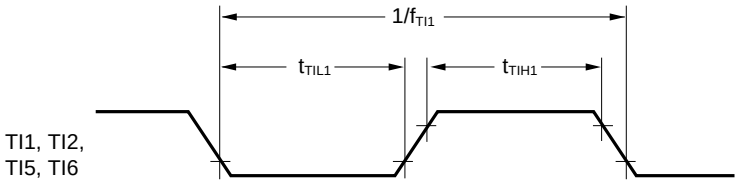
Clock Timing





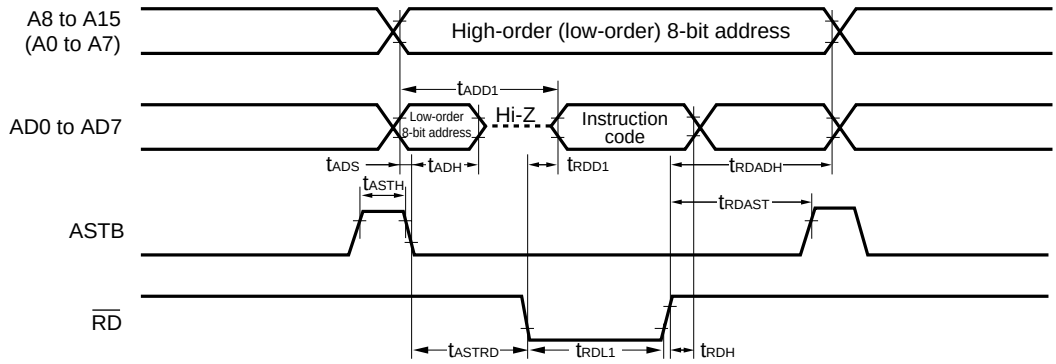
TI Timing





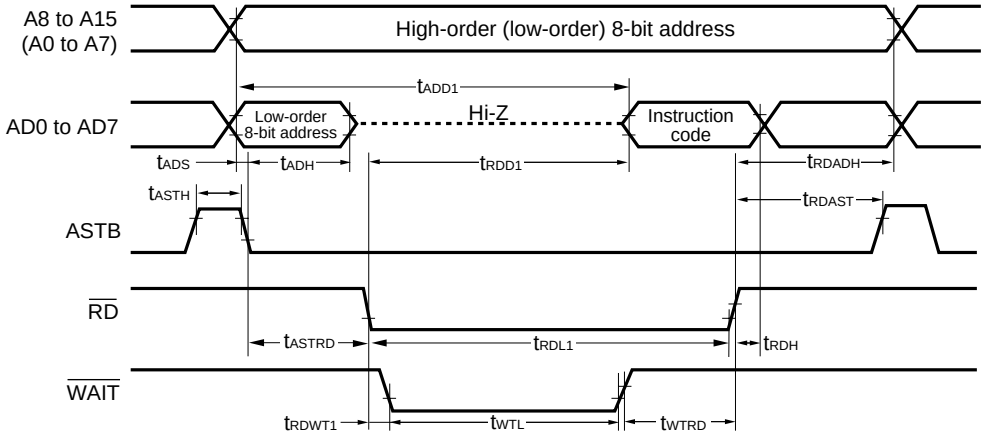
Read/Write Operation

External fetch (no wait):



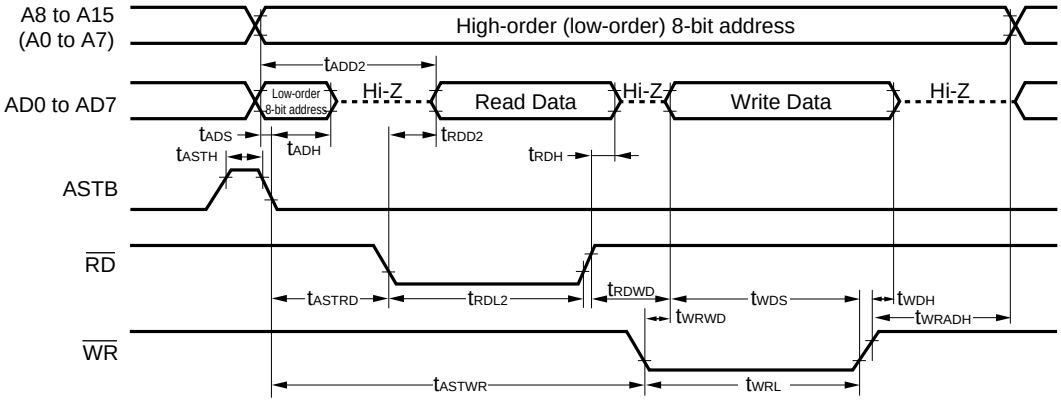
Remark ( ) is effective only in separate bus mode.

External fetch (wait insertion):



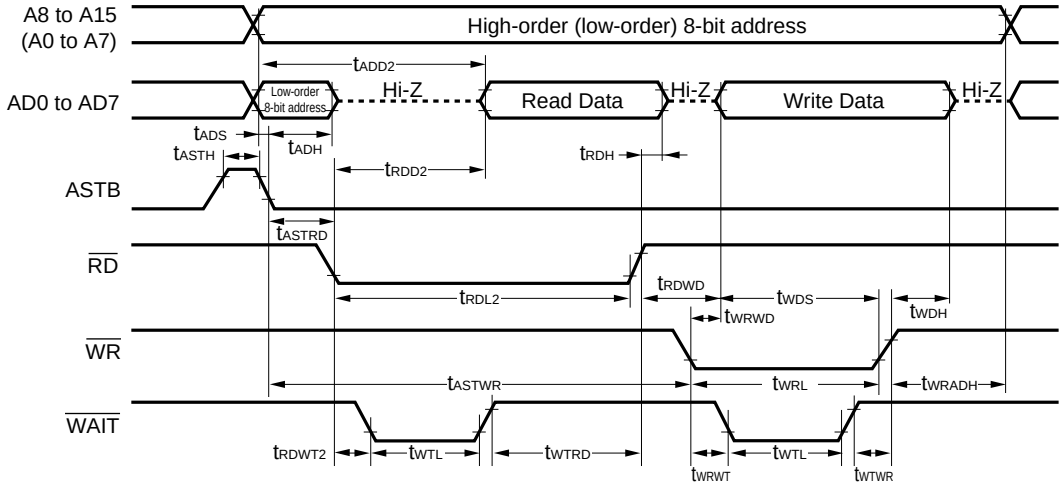
Remark ( ) is effective only in separate bus mode.

External data access (no wait):



Remark ( ) is effective only in separate bus mode.

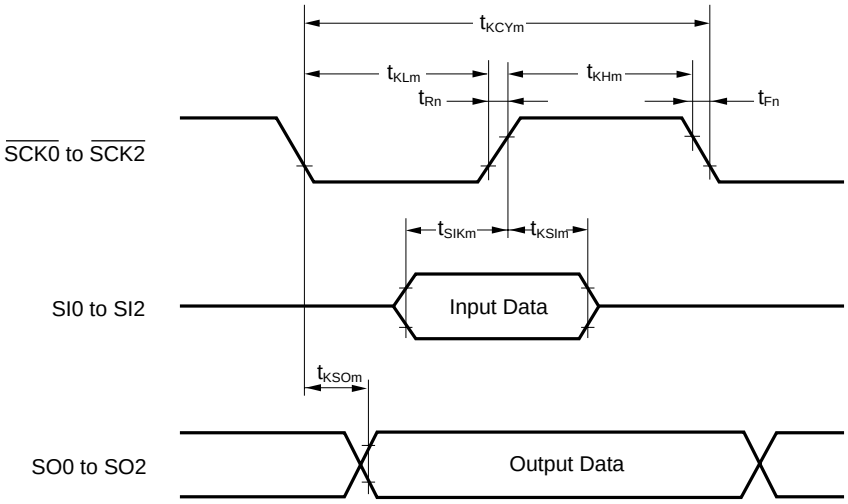
External data access (wait insertion):



Remark ( ) is effective only in separate bus mode.

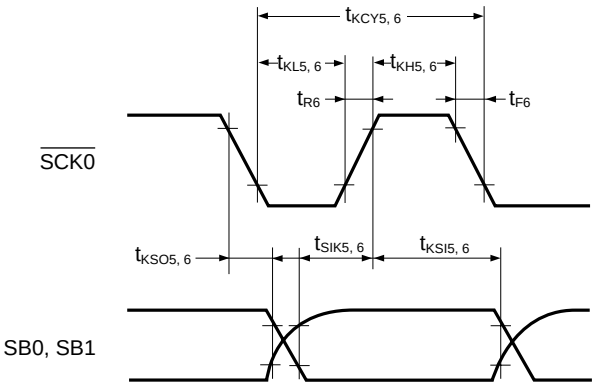
Serial Transfer Timing

3-wire serial I/O mode:

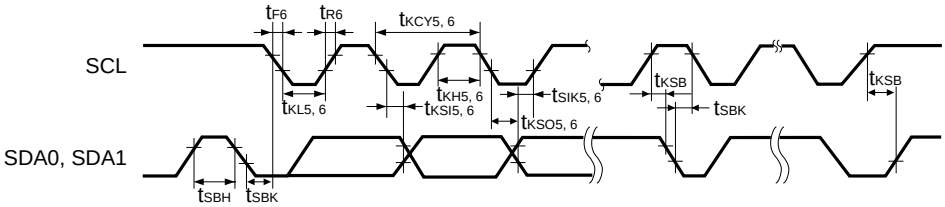


Remark m = 1, 2, 7, 8, 11, 12
n = 2, 8, 12

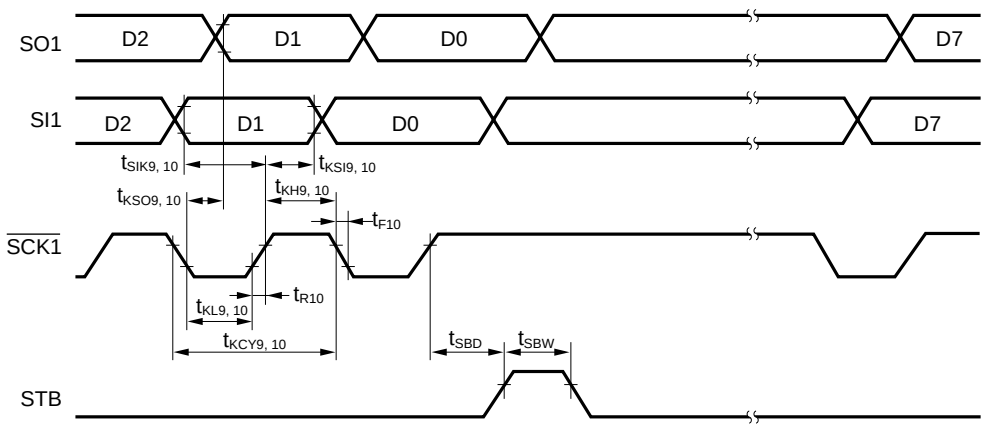
2-wire serial I/O mode:



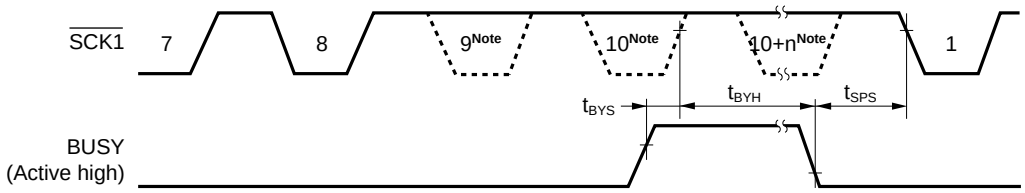
I²C bus mode



3-wire serial I/O mode with automatic transmission/reception function:

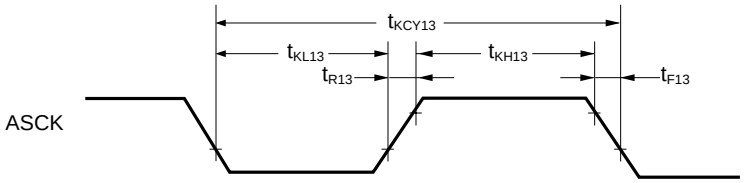


3-wire serial I/O mode with automatic transmission/reception function (busy processing):



Note The signal is not actually low here, but is represented in this way to show the timing.

UART mode (external clock input):



A/D Converter Characteristics (T_A = –40 to +85°C, AV_{DD} = V_{DD} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Total error[Note]		2.7 V ≤ AV_{REF0} ≤ AV_{DD}			1.4	%
Conversion time	t_{CONV}		19.1		200	μs
Sampling time	t_{SAMP}		12/f_{XX}			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}		2.7		AV_{DD}	V
AV_{REF0} to AV_{SS} resistance	R_{AIREF0}		4			kΩ

Note Excluding quantization error (±1/2 LSB). Shown as a percentage of the full scale value.

Remark f_{XX}: Main system clock frequency (f_X or f_X/2)
f_X: Main system clock oscillation frequency

D/A Converter Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Resolution						8	bit
Total error		R = 2 MΩ[Note 1]				1.2	%
		R = 4 MΩ[Note 1]				0.8	%
		R = 10 MΩ[Note 1]				0.6	%
Settling time		C = 30 pF[Note 1]	4.5 V ≤ AV_{REF1} ≤ 5.5 V			10	μs
			2.7 V ≤ AV_{REF1} < 4.5 V			15	μs
			1.8 V ≤ AV_{REF1} < 2.7 V			20	μs
Output resistor	R_O	**Note 2**			10		kΩ
Analog reference voltage	AV_{REF1}			1.8		V_{DD}	V
AV_{REF1} to AV_{SS} resistance	R_{AIREF1}	DACS0, DACS1 = 55H[Note 2]		4	8		kΩ

Notes 1. R and C are the D/A converter output pin load resistance and load capacitance.
2. Value for one D/A converter channel.

Remark DACS0, DACS1 : D/A conversion value setting register 0, 1

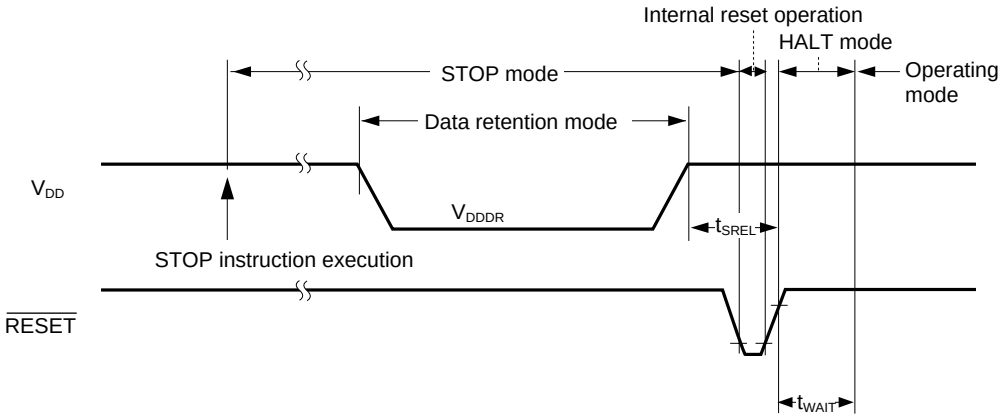
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8 V When subsystem clock stopped and feedback resistor disconnected		0.1	10	μA
Release signal setup time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_x$		ms
		Release by interrupt		**Note**		ms

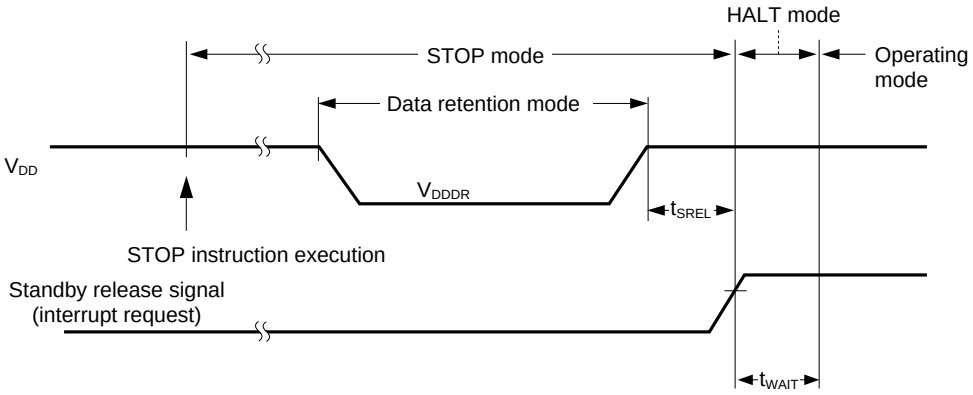
Note $2^{12}/f_{XX}$ or $2^{14}/f_{XX}$ to $2^{17}/f_{XX}$ can be selected by bit 0 to bit 2 (OSTS0 to OSTS2) of oscillation stabilization time selection register.

Remark f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency

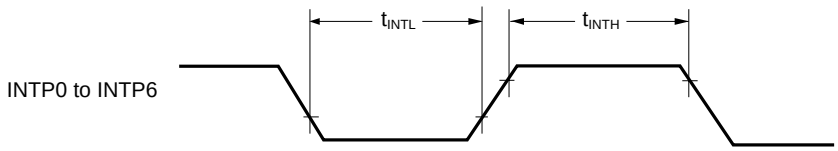
Data Retention Timing (STOP mode released by $\overline{RESET}$)



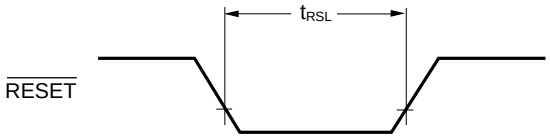
Data Retention Timing (Standby release signal: STOP mode released by interrupt signal)



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



PROM Programming Characteristics

DC Characteristics

(1) PROM Write Mode (T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	V_{IH}		0.7V_{DD}		V_{DD}	V
Input voltage, low	V_{IL}	V_{IL}		0		0.3V_{DD}	V
Output voltage, high	V_{OH}	V_{OH}	I_{OH} = –1 mA	V_{DD} – 1.0			V
Output voltage, low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	0 ≤ V_{IN} ≤ V_{DD}	–10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		12.2	12.5	12.8	V
V_{DD} supply voltage	V_{DD}	V_{CC}		6.25	6.5	6.75	V
V_{PP} supply current	I_{PP}	I_{PP}	$\overline{PGM}$ = V_{IL}			50	mA
V_{DD} supply current	I_{DD}	I_{CC}				50	mA

(2) PROM Read Mode (T_A = 25 ±5°C, V_{DD} = 5.0 ±0.5 V, V_{PP} = V_{DD} ±0.6 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	V_{IH}		0.7V_{DD}		V_{DD}	V
Input voltage, low	V_{IL}	V_{IL}		0		0.3V_{DD}	V
Output voltage, high	V_{OH1}	V_{OH1}	I_{OH} = –1 mA	V_{DD} – 1.0			V
	V_{OH2}	V_{OH2}	I_{OH} = –100 μA	V_{DD} – 0.5			V
Output voltage, low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	0 ≤ V_{IN} ≤ V_{DD}	–10		+10	μA
Output leakage current	I_{LO}	I_{LO}	0 ≤ V_{OUT} ≤ V_{DD}, $\overline{OE}$ = V_{IH}	–10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		V_{DD} – 0.6	V_{DD}	V_{DD} + 0.6	V
V_{DD} supply voltage	V_{DD}	V_{CC}		4.5	5.0	5.5	V
V_{PP} supply current	I_{PP}	I_{PP}	V_{PP} = V_{DD}			100	μA
V_{DD} supply current	I_{DD}	I_{CCA1}	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH}			50	mA

Note Corresponding μPD27C1001A symbol.

AC Characteristics

(1) PROM Write Mode

(a) Page program mode (T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{OE}$ ↓)	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ setup time	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (to $\overline{OE}$ ↓)	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{OE}$ ↓)	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}$ ↑)	t_{AH}	t_{AH}		2			μs
	t_{AHL}	t_{AHL}		2			μs
	t_{AHV}	t_{AHV}		0			μs
Input data hold time (from $\overline{OE}$ ↑)	t_{DH}	t_{DH}		2			μs
$\overline{OE}$ ↑ → Data output float delay time	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{OE}$ ↓)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{OE}$ ↓)	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	t_{PW}	t_{PW}		0.095	0.1	0.105	ms
$\overline{OE}$ ↓ → Valid data delay time	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ pulse width during data latching	t_{LW}	t_{LW}		1			μs
$\overline{PGM}$ setup time	t_{PGMS}	t_{PGMS}		2			μs
$\overline{CE}$ hold time	t_{CEH}	t_{CEH}		2			μs
$\overline{OE}$ hold time	t_{OEH}	t_{OEH}		2			μs

(b) Byte program mode (T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{PGM}$ ↓)	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ setup time	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (to $\overline{PGM}$ ↓)	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{PGM}$ ↓)	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}$ ↑)	t_{AH}	t_{AH}		2			μs
Input data hold time (from $\overline{PGM}$ ↑)	t_{DH}	t_{DH}		2			μs
$\overline{OE}$ ↑ → Data output float delay time	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{PGM}$ ↓)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{PGM}$ ↓)	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	t_{PW}	t_{PW}		0.095	0.1	0.105	ms
$\overline{OE}$ ↓ → Valid data delay time	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ hold time	t_{OEH}	—		2			μs

Note Corresponding μPD27C1001A symbol.

(2) PROM Read Mode (T_A = 25 ±5°C, V_{DD} = 5.0 ±0.5 V, V_{PP} = V_{DD} ±0.6 V)

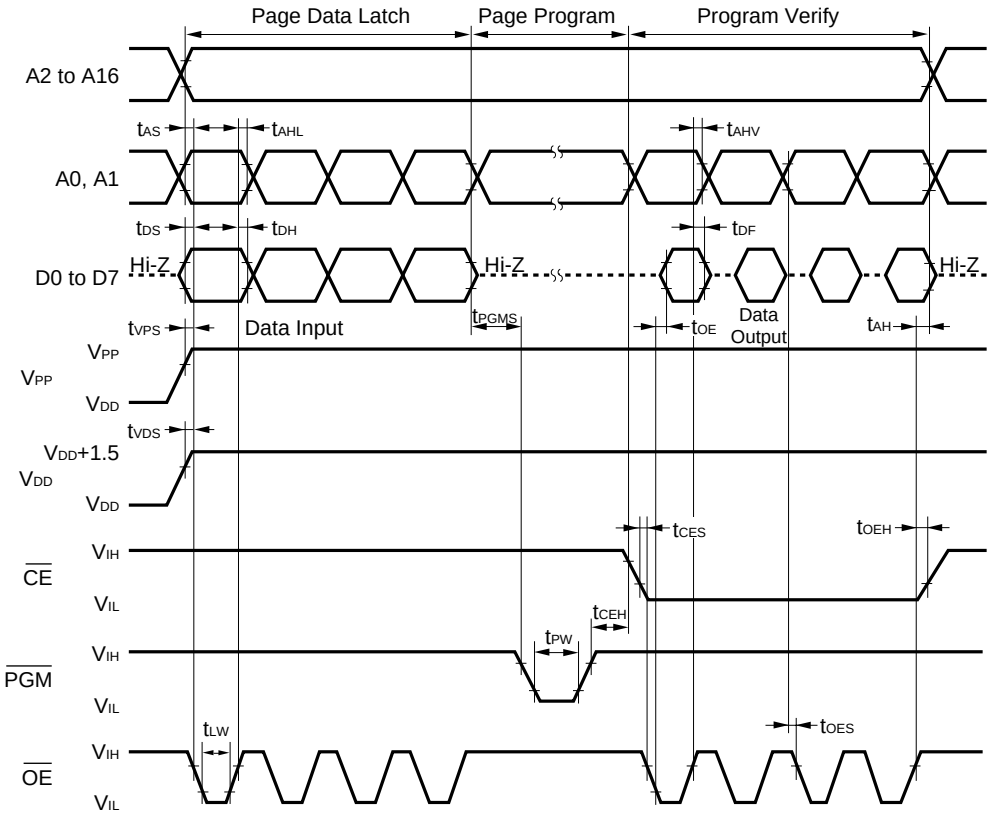
Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Address → Data output delay time	t_{ACC}	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			800	ns
$\overline{CE}$ ↓ → Data output delay time	t_{CE}	t_{CE}	$\overline{OE}$ = V_{IL}			800	ns
$\overline{OE}$ ↓ → Data output delay time	t_{OE}	t_{OE}	$\overline{CE}$ = V_{IL}			200	ns
$\overline{OE}$ ↑ → Data output float delay time	t_{DF}	t_{DF}	$\overline{CE}$ = V_{IL}	0		60	ns
Address → Data hold time	t_{OH}	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0			ns

Note Corresponding μPD27C1001A symbol.

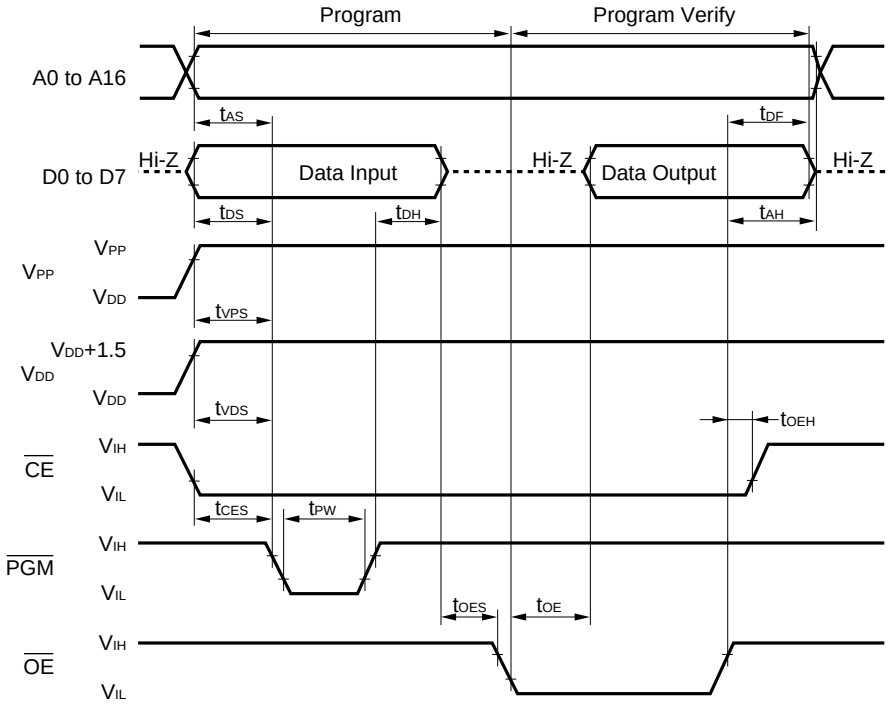
(3) PROM Programming Mode (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
PROM programming mode setup time	t_{SMA}		10			μs

PROM Write Mode Timing (page program mode)



PROM Write Mode Timing (byte program mode)

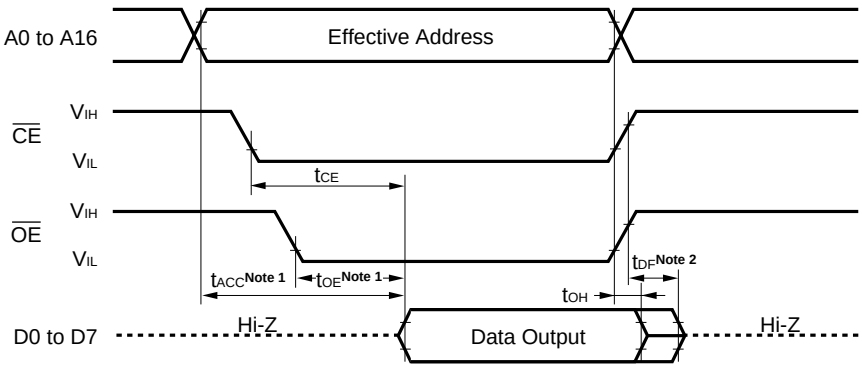


Cautions 1. V_{DD} should be applied before V_{PP}, and removed after V_{PP}.

2. V_{PP} must not exceed +13.5 V including overshoot.

3. Reliability may be adversely affected if removal/reinsertion is performed while +12.5 V is being applied to V_{PP}.

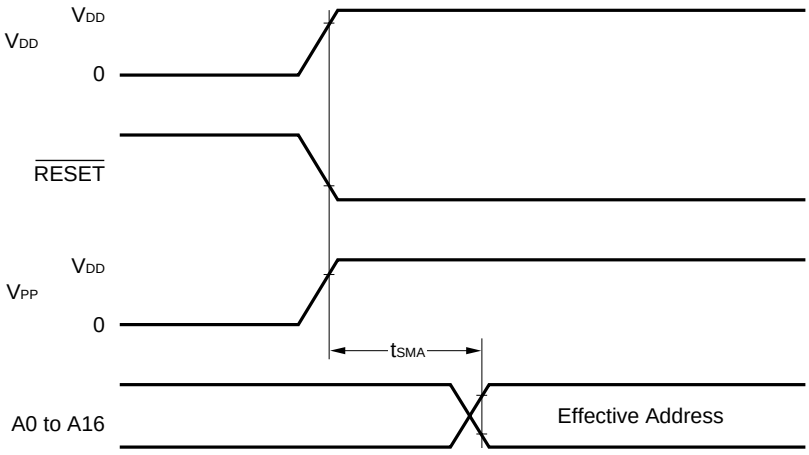
PROM Read Mode Timing



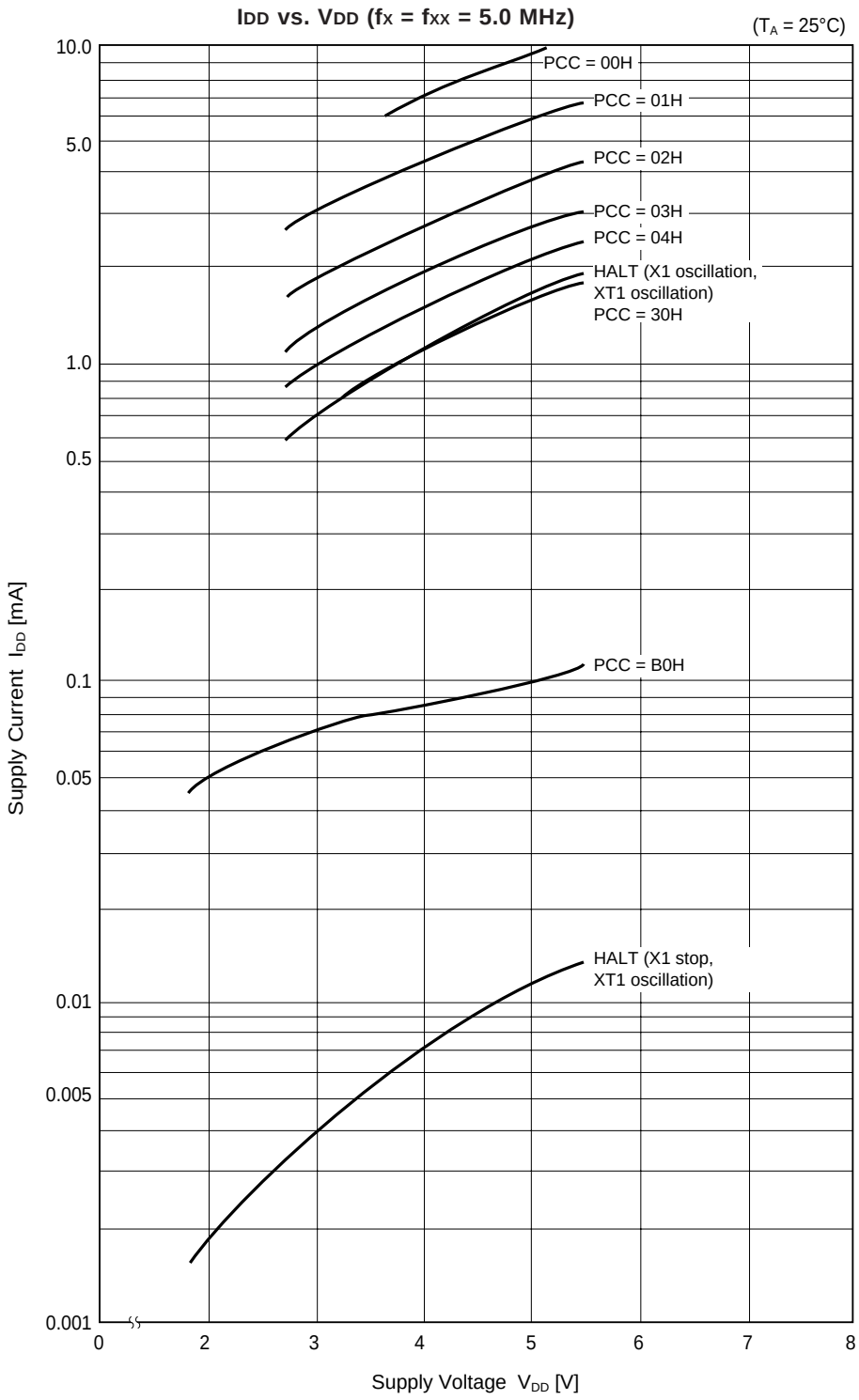
Notes 1. If you want to read within the range of t_{ACC}, make the $\overline{OE}$ input delay time from the fall of $\overline{CE}$ a maximum of $t_{ACC}-t_{OE}$.

2. t_{DF} is the time from when either $\overline{OE}$ or $\overline{CE}$ first reaches V_{IH}.

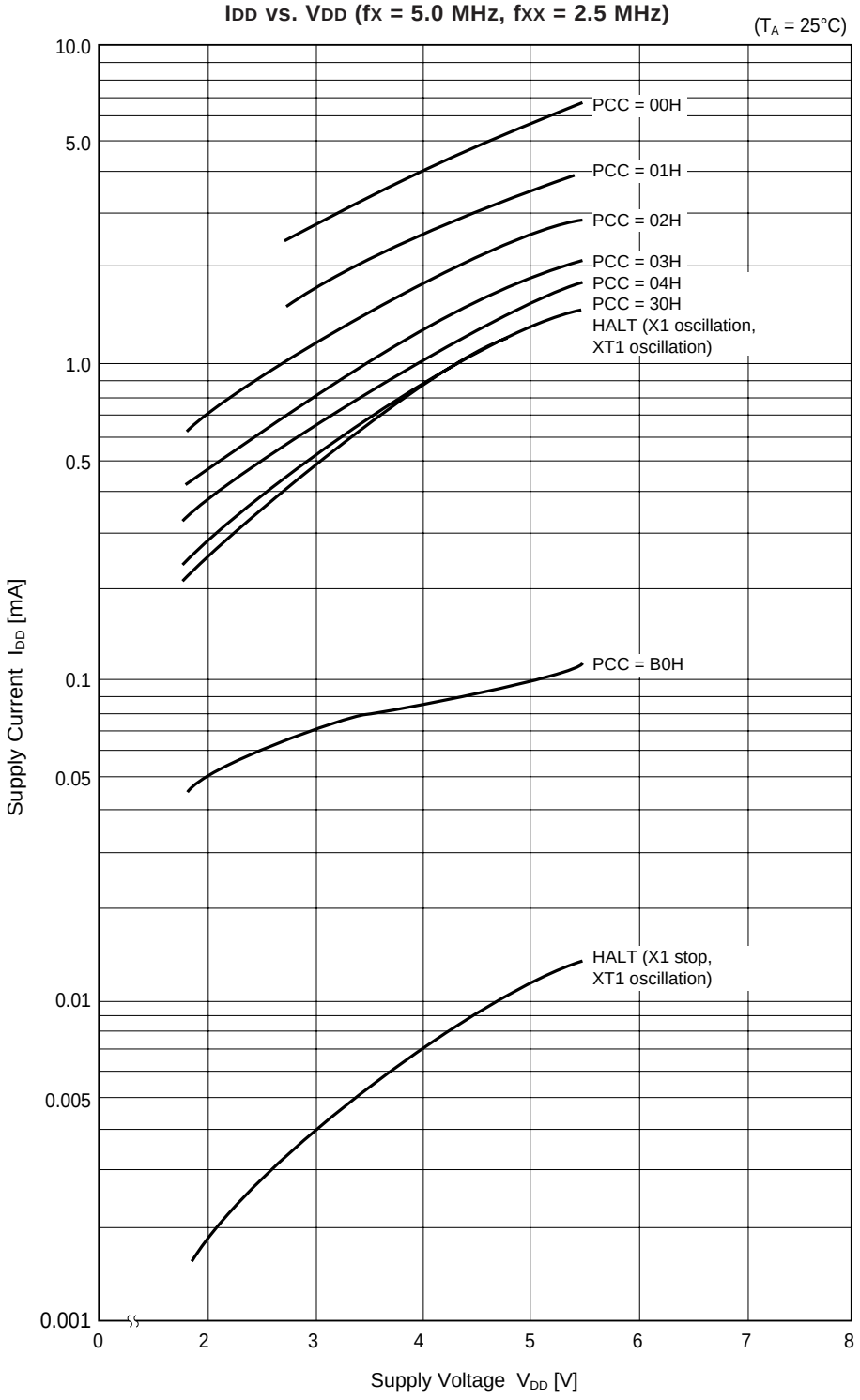
PROM Programming Mode Setting Timing



10. CHARACTERISTIC CURVES (REFERENCE VALUES)

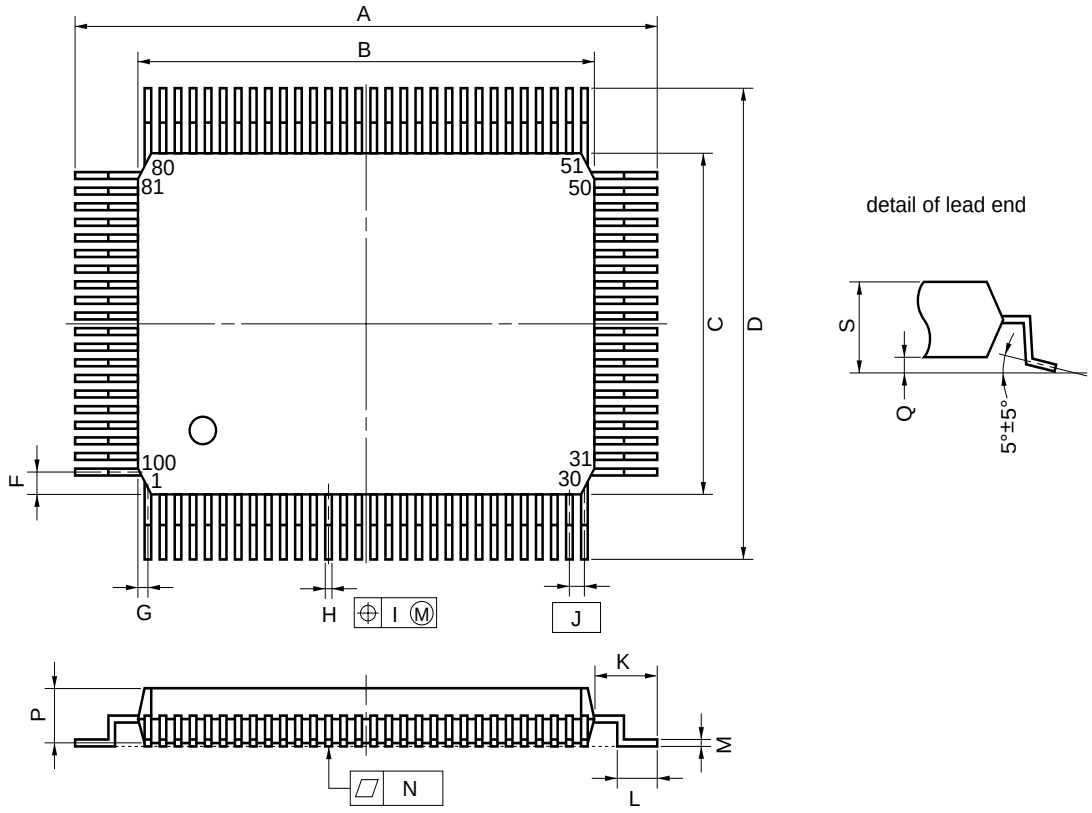


IDD vs. VDD (fX = 5.0 MHz, fXX = 2.5 MHz)



11. PACKAGE DRAWINGS

100 PIN PLASTIC QFP (14 × 20)



P100GF-65-3BA1-2

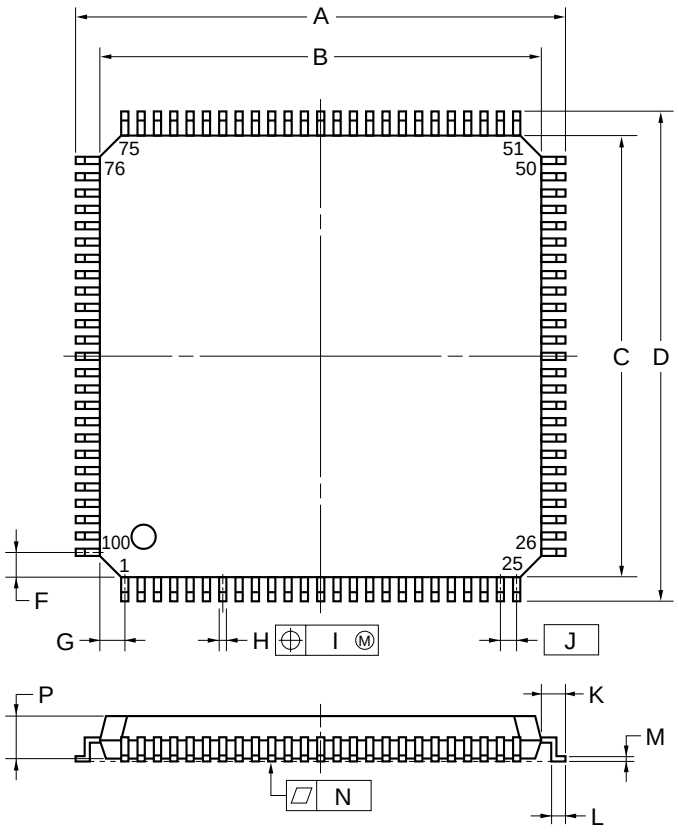
NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

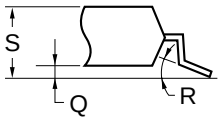
ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

Remark The shape and material of ES versions are the same as those of mass-produced versions.

100 PIN PLASTIC LQFP (FINE PITCH) (14 × 14)



detail of lead end



NOTE

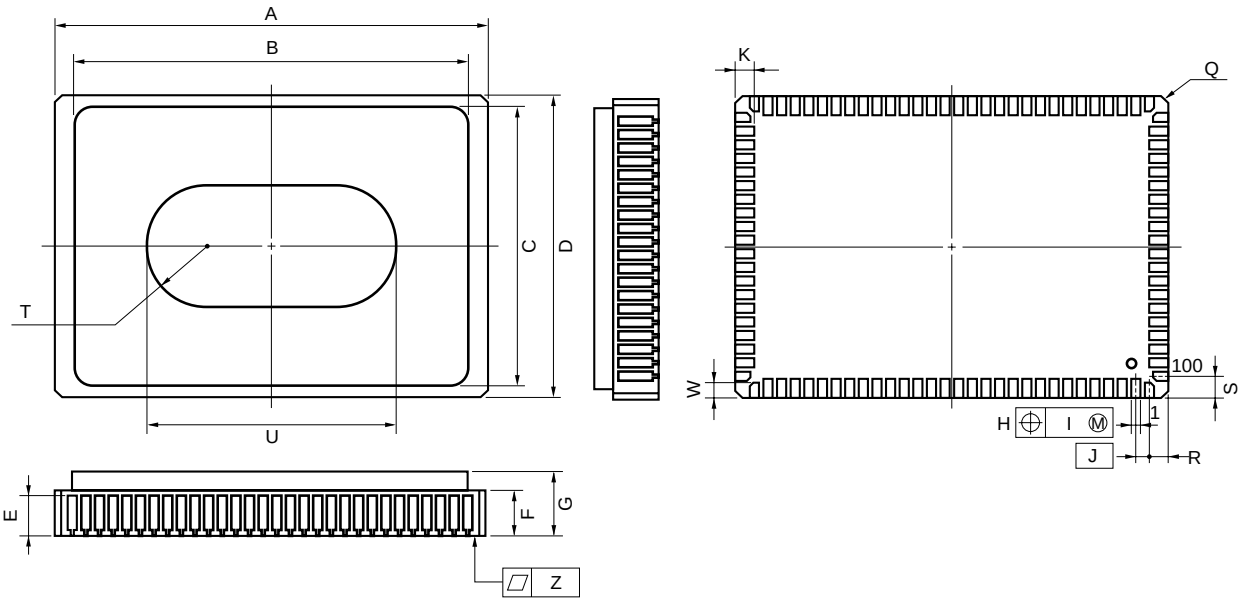
Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.00±0.20	0.630±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	16.00±0.20	0.630±0.008
F	1.00	0.039
G	1.00	0.039
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.08	0.003
J	0.50 (T.P.)	0.020 (T.P.)
K	1.00±0.20	$0.039^{+0.009}_{-0.008}$
L	0.50±0.20	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.08	0.003
P	1.40±0.05	0.055±0.002
Q	0.10±0.05	0.004±0.002
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.60 MAX.	0.063 MAX.

S100GC-50-8EU

Remark The shape and material of ES versions are the same as those of mass-produced versions.

100 PIN CERAMIC WQFN



X100KW-65A-1

ITEM	MILLIMETERS	INCHES
A	20.6±0.4	0.811±0.016
B	19.0	0.748
C	13.8	0.543
D	14.6±0.4	0.575±0.016
E	1.94	0.076
F	2.14	0.084
G	3.5 MAX,	0.138 MAX.
H	0.45±0.10	$0.018^{+0.004}_{-0.005}$
I	0.06	0.003
J	0.65	0.026
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
Q	C 0.3	C 0.012
R	0.875	0.034
S	1.125	0.044
T	R 3.17	R 0.125
U	12.0	0.472
W	0.75±0.2	$0.030^{+0.008}_{-0.009}$
Z	0.10	0.004

NOTE

Each lead centerline is located within 0.06 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

12. RECOMMENDED SOLDERING CONDITIONS

It is recommended that the μPD78P078Y be soldered under the following conditions.
For details on the recommended soldering conditions, refer to information document **"Semiconductor Device Mounting Technology Manual" (C10535E)**.

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

Table 12-1. Soldering Conditions for Surface Mount Devices

μPD78P078YGF-3BA: 100-pin plastic QFP (14 × 20 mm, resin thickness: 2.7 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared ray reflow	Package peak temperature: 235°C, Reflow time: 30 seconds or less (at 210°C or higher), Number of reflow processes: 3 or less	IR35-00-3
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds or less (at 200°C or higher), Number of reflow processes: 3 or less	VP15-00-3
Wave soldering	Solder temperature: 260°C or below, Flow time: 10 seconds or less, Number of flow processes: 1, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C or below, Flow time: 3 seconds or less (per pin row)	—

Cautions 1. Do not use different soldering methods together (except for partial heating method).

2. Soldering conditions have not been fixed because the μPD78P078YGC-8EU is still under development.

APPENDIX A. DEVELOPMENT TOOLS

The following dvelopment tools are available to support development of systems using the μPD78P078Y.

Language Processing Software

RA78K/0[Notes 1, 2, 3, 4]	Assembler package common to the 78K/0 Series
CC78K/0[Notes 1, 2, 3, 4]	C compiler package common to the 78K/0 Series
DF78078[Notes 1, 2, 3, 4]	Device file common to the μPD78078 Subseries
CC78K/0–L[Notes 1, 2, 3, 4]	C compiler library source file common to the 78K/0 Series

PROM Writing Tools

PG-1500	PROM programmer
PA-78P078GC PA-78P078GF PA-78P078KL-T	Programmer adapter connected to the PG-1500
PG-1500 Controller [Notes 1, 2]	Control program for the PG-1500

Debugging Tools

IE-78000-R	In-circuit emulator common to the 78K/0 Series
★ IE-78000-R-A	In-circuit emulator common to the 78K/0 Series (for integrated debugger)
IE-78000-R-BK	Break board common to the 78K/0 Series
IE-78078-R-EM	Emulation board for evaluation of the μPD78078 Subseries
EP-78064GC-R EP-78064GF-R	Emulation probe common to the μPD78064 Subseries
EV-9200GF-100	Socket mounted on the target system board prepared for 100-pin plastic QFP (GF-3BA type)
★ TGC-100SDW	Adapter mounted on the target system board prepared for 100-pin plastic LQFP (GC-8EU type) This is a product of TOKYO ELETECH Corporation (Tokyo (03) 5295-1661). Consult an NEC sales representative for purchase.
EV-9900	Tool used for removing the μPD78P078YKL-T from the EV-9200GF-100.
SM78K0[Notes 5, 6, 7]	System simulator common to the 78K/0 Series
ID78K0[Notes 4, 5, 6, 7]	Integrated debugger for the IE-78000-R-A
SD78K/0[Notes 1, 2]	Screen debugger for the IE-78000-R
DF78078[Notes 1, 2, 4, 5, 6, 7]	Device file common to the μPD78078 Subseries

Real-Time OS

RX78K/0[Notes 1, 2, 3, 4]	Real-time OS used for the 78K/0 Series
MX78K0[Notes 1, 2, 3, 4]	OS used for the 78K/0 Series

Fuzzy Inference Development Support System

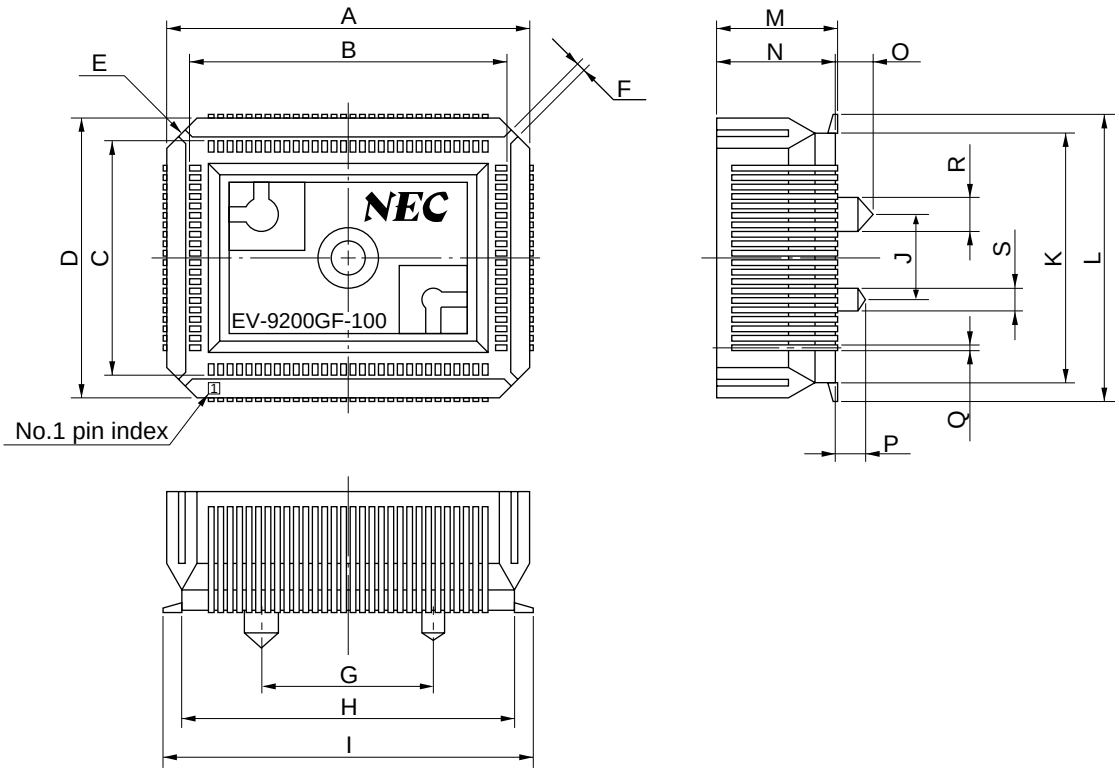
FE9000[Note 1]/FE9200[Note 3]	Fuzzy knowledge data creation tool
FT9080[Note 1]/FT9085[Note 2]	Translator
FI78K0[Notes 1, 2]	Fuzzy inference module
FD78K0[Notes 1, 2]	Fuzzy inference debugger

Notes 1. PC-9800 Series (MS-DOS™) based
2. IBM PC/AT™ and its compatibles (PC DOS™/IBM DOS™/MS-DOS) based
3. HP9000 Series 300™(HP-UX™) based
4. HP9000 Series 700™ (HP-UX), SPARCstation™ (SunOS™), and EWS4800 Series (EWS-UX/V) based
5. PC-9800 Series (MS-DOS + Windows™) based
6. IBM PC/AT and its compatibles (PC DOS/IBM DOS/MS-DOS + Windows) based
7. NEWS™ (NEWS-OS™) based

Remarks 1. Refer to the **78K/0 Series Selection Guide (U11126E)** for information on third party development tools.
2. Use the RA78K/0, CC78K/0, SM78K/0, ID78K0, SD78K/0, and RX78K/0 in combination with the DF78078.

DRAWINGS OF CONVERSION SOCKET (EV-9200GF-100) AND RECOMMENDED FOOTPRINT

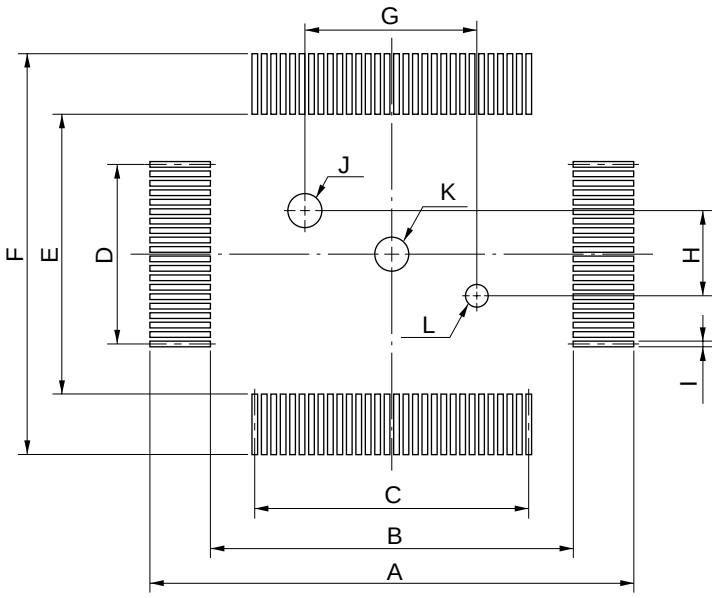
Figure A-1. Drawing of EV-9200GF-100 (for reference only)



EV-9200GF-100-G0

ITEM	MILLIMETERS	INCHES
A	24.6	0.969
B	21	0.827
C	15	0.591
D	18.6	0.732
E	4-C 2	4-C 0.079
F	0.8	0.031
G	12.0	0.472
H	22.6	0.89
I	25.3	0.996
J	6.0	0.236
K	16.6	0.654
L	19.3	076
M	8.2	0.323
N	8.0	0.315
O	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	φ2.3	φ0.091
S	φ1.5	φ0.059

Figure A-2. Recommended Footprint of EV-9200GF-100 (for reference only)



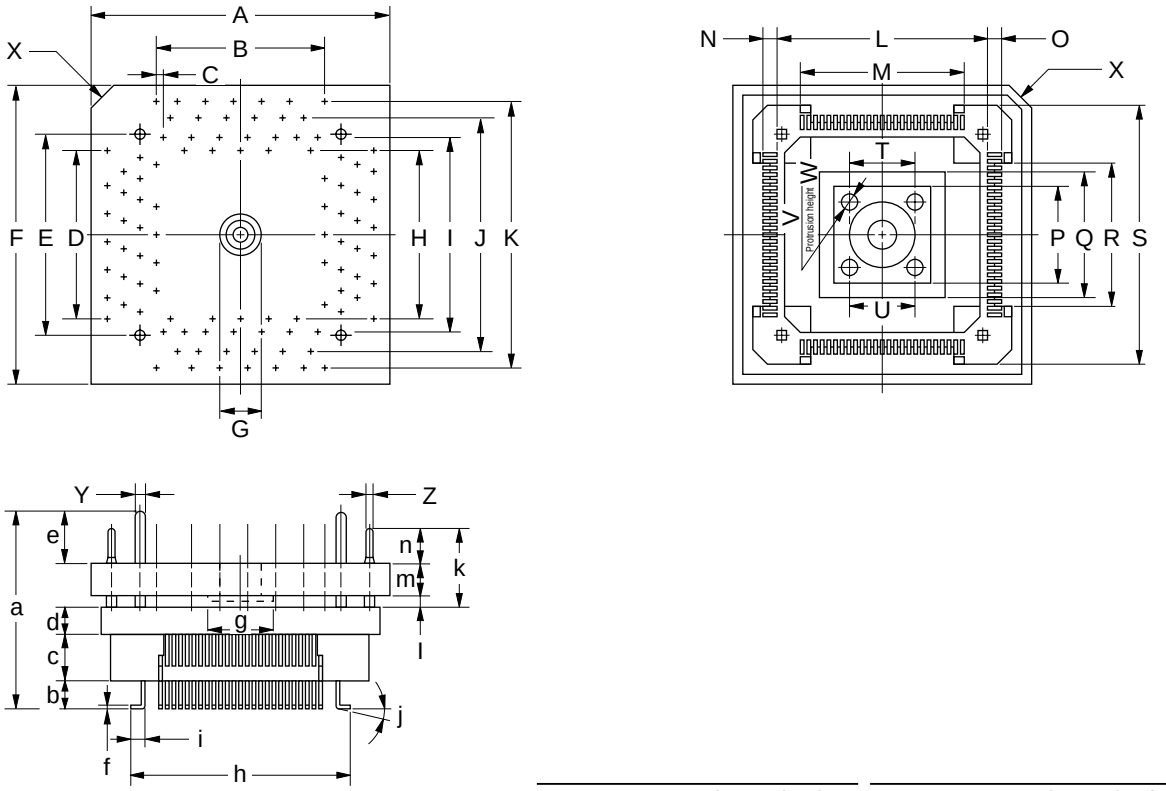
EV-9200GF-100-P1

ITEM	MILLIMETERS	INCHES
A	26.3	1.035
B	21.6	0.85
C	0.65±0.02 x 29=18.85±0.05	$0.026^{+0.001}_{-0.002}$ x 1.142=$0.742^{+0.002}_{-0.002}$
D	0.65±0.02 x 19=12.35±0.05	$0.026^{+0.001}_{-0.002}$ x 0.748=$0.486^{+0.003}_{-0.002}$
E	15.6	0.614
F	20.3	0.799
G	12±0.05	$0.472^{+0.003}_{-0.002}$
H	6±0.05	$0.236^{+0.003}_{-0.002}$
I	0.35±0.02	$0.014^{+0.001}_{-0.001}$
J	φ2.36±0.03	$\phi 0.093^{+0.001}_{-0.002}$
K	φ2.3	φ0.091
L	φ1.57±0.03	$\phi 0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to “SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL” (C10535E).

★ DRAWINGS OF CONVERSION ADAPTER (TGC-100SDW)

Figure A-3. Drawings of TGC-100SDW (for reference only) (Unit: mm)



ITEM	MILLIMETERS	INCHES
A	21.55	0.848
B	0.5x24=12	0.020x0.945=0.472
C	0.5	0.020
D	0.5x24=12	0.020x0.945=0.472
E	15.0	0.591
F	21.55	0.848
G	ϕ3.55	ϕ0.140
H	10.9	0.429
I	13.3	0.524
J	15.7	0.618
K	18.1	0.713
L	13.75	0.541
M	0.5x24=12.0	0.020x0.945=0.472
N	1.125±0.3	0.044±0.012
O	1.125±0.2	0.044±0.008
P	7.5	0.295
Q	10.0	0.394
R	11.3	0.445
S	18.1	0.713
T	ϕ5.0	ϕ0.197
U	5.0	0.197
V	4-ϕ1.3	4-ϕ0.051
W	1.8	0.071
X	C 2.0	C 0.079
Y	ϕ0.9	ϕ0.035
Z	ϕ0.3	ϕ0.012

ITEM	MILLIMETERS	INCHES
a	14.45	0.569
b	1.85±0.25	0.073±0.010
c	3.5	0.138
d	2.0	0.079
e	3.9	0.154
f	0.25	0.010
g	ϕ4.5	ϕ0.177
h	16.0	0.630
i	1.125±0.3	0.044±0.012
j	0~5°	0.000~0.197°
k	5.9	0.232
l	0.8	0.031
m	2.4	0.094
n	2.7	0.106

TGC-100SDW-G0E

Note Product by TOKYO ELETECH CORPORATION.

★ APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document No.	
	Japanese	English
μPD78078, 78078Y Subseries User's Manual	U10641J	U10641E
μPD78076Y, 78078Y Data Sheet	U10605J	U10605E
μPD78P078Y Data Sheet	U10606J	This document
μPD78074BY, 78075BY Data Sheet	Planned	Planned
μPD78075B, 78075BY Subseries User's Manual	U12560J	Planned
78K/0 Series User's Manual—Instructions	U12326J	U12326E
78K/0 Series Instruction Table	U10903J	—
78K/0 Series Instruction Set	U10904J	—
μPD78078Y Subseries Special Function Register Table	IEM-5601	—
78K/0 Series Application Note—Basics (III)	IEA-767	U10182E

Documents Related to Development Tools (User's Manual) (1/2)

Document Name		Document No.	
		Japanese	English
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
RA78K0 Assembler Package	Operation	U11802J	U11802E
	Assembly language	U11801J	U11801E
	Structured assembly language	U11789J	U11789E
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K0 C Compiler	Operation	U11517J	U11517E
	Language	U11518J	U11518E
CC78K/0 C Compiler Application Note	Programming know-how	EEA-618	EEA-1208
CC78K Series Library Source File		U12322J	—
PG-1500 PROM Programmer		U11940J	EEU-1335
PG-1500 Controller PC-9800 Series (MS-DOS) Based		EEU-704	EEU-1291
PG-1500 Controller IBM PC Series (PC DOS) Based		EEU-5008	U10540E
IE-78000-R		U11376J	U11376E
IE-78000-R-BK		EEU-867	EEU-1427
IE-78000-R-A		U10057J	U10057E
IE-78078-R-EM		U10775J	U10775E
EP-78064		EEU-934	EEU-1522

Caution The contents of the documents listed above are subject to change without prior notice. Make sure to use the latest edition when starting design.

Documents Related to Development Tools (User's Manual) (2/2)

Document Name		Document No.	
		Japanese	English
SM78K0 System Simulator Windows Based	Reference	U10181J	U10181E
SM78K Series System Simulator	External parts user open interface specification	U10092J	U10092E
ID78K0 Integrated Debugger EWS Based	Reference	U11151J	—
ID78K0 Integrated Debugger PC Based	Reference	U11539J	U11539E
ID78K0 Integrated Debugger Windows Based	Guides	U11649J	U11649E
SD78K/0 Screen Debugger	Introduction	EEU-852	U10539E
PC-9800 Series (MS-DOS) Based	Reference	U10952J	—
SD78K/0 Screen Debugger	Introduction	EEU-5024	EEU-1414
IBM PC/AT (PC DOS) Based	Reference	U11279J	U11279E

Documents Related to Embedded Software (User's Manual)

Document Name		Document No.	
		Japanese	English
78K/0 Series Real-time OS	Basics	U11537J	—
	Installation	U11536J	—
78K/0 Series OS MX78K0	Basics	U12257J	—
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K/0, 78K/II, and 87AD Series Fuzzy Inference Development Support System Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-921	EEU-1458

Other Documents

Document Name	Document No.	
	Japanese	English
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	—
Guide to Quality Assurance for Semiconductor Devices	C11893J	MEI-1202
Microcomputer Product Series Guide – Third Party Products –	U11416J	—

Caution The contents of the documents listed above are subject to change without prior notice. Be sure to use the latest edition when starting design.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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