NEC

MOS INTEGRATED CIRCUIT

μPD78P0308

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78P0308 is a member of the μPD780308 Subseries of the 78K/0 Series, in which the on-chip mask ROM of the μPD780308 is replaced with a one-time PROM or EPROM.

Because this device can be programmed by users, it is ideally suited for system evaluation, small-scale and multiple-device production, and early development and time-to-market.

Caution The μPD78P0308KL-T does not maintain planned reliability when used in your systems' mass-produced products. Please use only experimentally or for evaluation purposes during trial manufacture.

The details of functions are described in the user's manuals. Be sure to read the following manuals before designing.

μPD780308, 780308Y Subseries User's Manual	**: U11377E**
78K/0 Series User's Manual Instructions	**: U12326E**

FEATURES

- Pin-compatible with mask ROM version (except V_{PP} pin)
- Internal PROM: 60 Kbytes[Note]
  - μPD78P0308KL-T : Reprogrammable (ideally suited for system evaluation)
  - μPD78P0308GC, μPD78P0308GF : One-time programmable (ideally suited for small-scale production)
- Internal high-speed RAM : 1024 bytes
- Internal expansion RAM : 1024 bytes
- LCD display RAM : 40 x 4 bits
- ★ Supply voltage : V_{DD} = 2.7 to 5.5 V
- Corresponding to QTOP™ Microcontrollers (under planning)

Note The internal PROM capacity can be changed by setting the memory size switching register (IMS).

Remarks 1. QTOP microcontroller is a general term for microcontrollers that incorporate one-time PROM and are totally supported by NEC's programming service (from programming to marking, screening, and verification).

2. Refer to **1. DIFFERENCES BETWEEN THE μPD78P0308 AND MASK ROM VERSIONS** for the difference between the PROM and mask ROM versions.

In this document, the term PROM is used in parts common to one-time PROM versions and EPROM versions.

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The mark ★ shows major revised points

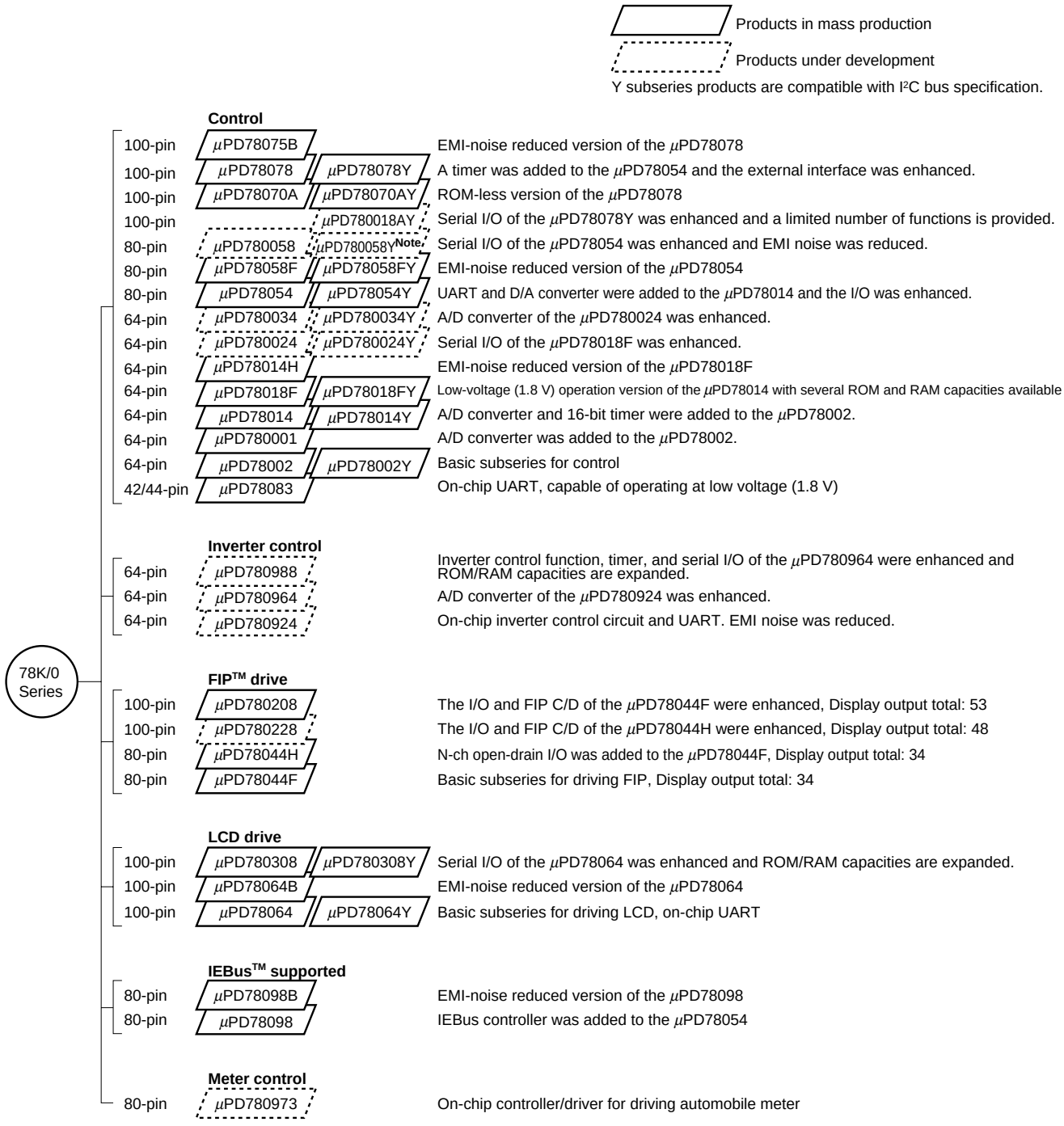
ORDERING INFORMATION

	Part Number	Package	Internal ROM	Quality Grades
★	μPD78P0308GC-8EU	100-pin plastic LQFP (fine pitch) (14 × 14 mm)	One-Time PROM	Standard
	μPD78P0308GF-3BA	100-pin plastic QFP (14 × 20 mm)	One-Time PROM	Standard
	μPD78P0308KL-T	100-pin ceramic WQFN (14 × 20 mm)	EPROM	Not applicable (for evaluation)

Please refer to “Quality Grades on NEC Semiconductor Devices” (Document number C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

78K/0 SERIES DEVELOPMENT

The following shows the 78K/0 Series product lineup. Subseries names are shown inside frames.



Note Under planning

The following lists the main functional differences between subseries products.

Subseries Name \ Function		ROM Capacity	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-bit	16-bit	Watch	WDT							
Control	μPD78075B	32K-40K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	88	1.8 V	A
	μPD78078	48K-60K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24K-60K	2 ch							3 ch (time division UART: 1 ch)	68	1.8 V	
	μPD78058F	48K-60K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16K-60K										2.0 V	
	μPD780034	8K-32K					–	8 ch	–	3 ch (UART: 1 ch, time division 3-wire: 1 ch)	51	1.8 V	
	μPD780024						8 ch	–					
	μPD78014H									2 ch	53		
	μPD78018F	8K-60K											
	μPD78014	8K-32K										2.7 V	
	μPD780001	8K		–	–					1 ch	39		N/A
	μPD78002	8K-16K			1 ch		–				53		A
	μPD78083				–		8 ch			1 ch (UART: 1 ch)	33	1.8 V	N/A
Inverter control	μPD780988	8K-60K	3 ch	Note1	–	1 ch	–	8 ch	–	3 ch (UART: 2 ch)	47	2.7 V	A
	μPD780964	8K-32K		Note2						2 ch (UART: 2 ch)		4.0 V	
	μPD780924						8 ch	–					
FIP drive	μPD780208	32K-60K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	2 ch	74	2.7 V	N/A
	μPD780228	48K-60K	3 ch	–	–					1 ch	72	4.5 V	
	μPD78044H	32K-48K	2 ch	1 ch	1 ch						68	2.7 V	
	μPD78044F	16K-40K								2 ch			
LCD drive	μPD780308	48K-60K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	3 ch (time division UART: 1 ch)	57	2.0 V	N/A
	μPD78064B	32K								2 ch (UART: 1 ch)			
	μPD78064	16K-32K											
IEBus supported	μPD78098B	40K-60K	2 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	69	2.7 V	A
	μPD78098	32K-60K											
Meter	μPD780973	24K-32K	3 ch	1 ch	1 ch	1 ch	5 ch	–	–	2 ch (UART: 1 ch)	56	4.5 V	N/A

Notes 1. 16-bit timer: 2 channels
10-bit timer: 1 channel

2. 10-bit timer: 1 channel

Remark A : Available
N/A : Not available

FUNCTION DESCRIPTION

Item		Function
Internal memory		• PROM: 60 Kbytes[Note] • RAM High-speed RAM: 1024 bytes Expansion RAM: 1024 bytes LCD display RAM: 40 x 4 bits
General register		8 bits x 32 registers (8 bits x 8 registers x 4 banks)
Minimum instruction execution time		Minimum instruction execution time variable function is integrated.
	When main system clock is selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (@ 5.0-MHz operation)
	When subsystem clock is selected	122 μs (@ 32.768-kHz operation)
Instruction set		• 16-bit operation • Multiply/divide (8 bits x 8 bits, 16 bits ÷ 8 bits) • Bit manipulate (set, reset, test, Boolean operation) • BCD adjust, etc.
I/O ports (Segment signal output pin included)		Total : 57 • CMOS input : 2 • CMOS input/output : 55
A/D converter		• 8-bit resolution x 8 channels • Supply voltage : $V_{DD0} = V_{DD1} = AV_{REF}$ = 4.0 to 5.5 V
LCD Controller/driver		• Segment signal output : 40 pins maximum • Common signal output : 4 pins maximum • Bias : 1/2,1/3 bias convertible
Serial interface		• 3-wire serial I/O/SBI/2-wire serial I/O mode selectable : 1 channel • 3-wire serial I/O/UART mode selectable : 1 channel • 3-wire serial I/O mode : 1 channel
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel
Timer output		3 pins (14-bit PWM output enable: 1 pin)
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, and 5.0 MHz (@ 5.0-MHz operation with main system clock) 32.768 kHz (@ 32.768-kHz operation with subsystem clock)
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, and 9.8 kHz (@ 5.0-MHz operation with main system clock)

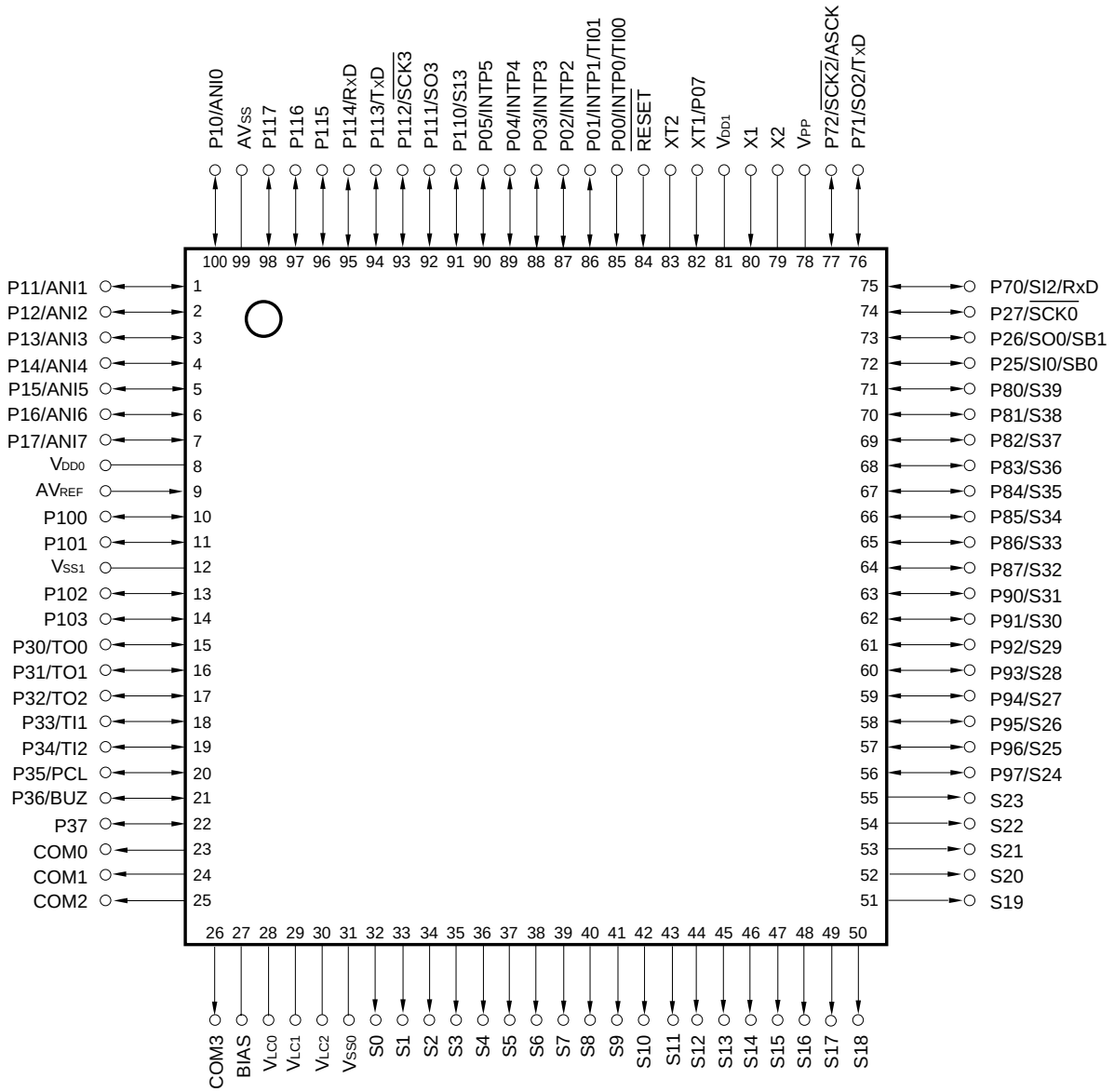
Note Internal PROM capacity can be changed with the memory size switching register (IMS).

Item		Function
Vectored interrupt sources	Maskable	Internal: 13, External: 6
	Non-maskable	Internal: 1
	Software	1
Test input		Internal: 1, External: 1
★ Supply voltage		V_{DD} = 2.7 to 5.5 V
★ Package		• 100-pin plastic LQFP (fine pitch) (14 × 14 mm) • 100-pin plastic QFP (14 × 20 mm) • 100-pin ceramic WQFN (14 × 20 mm)

PIN CONFIGURATIONS (Top View)

(1) Normal operating mode

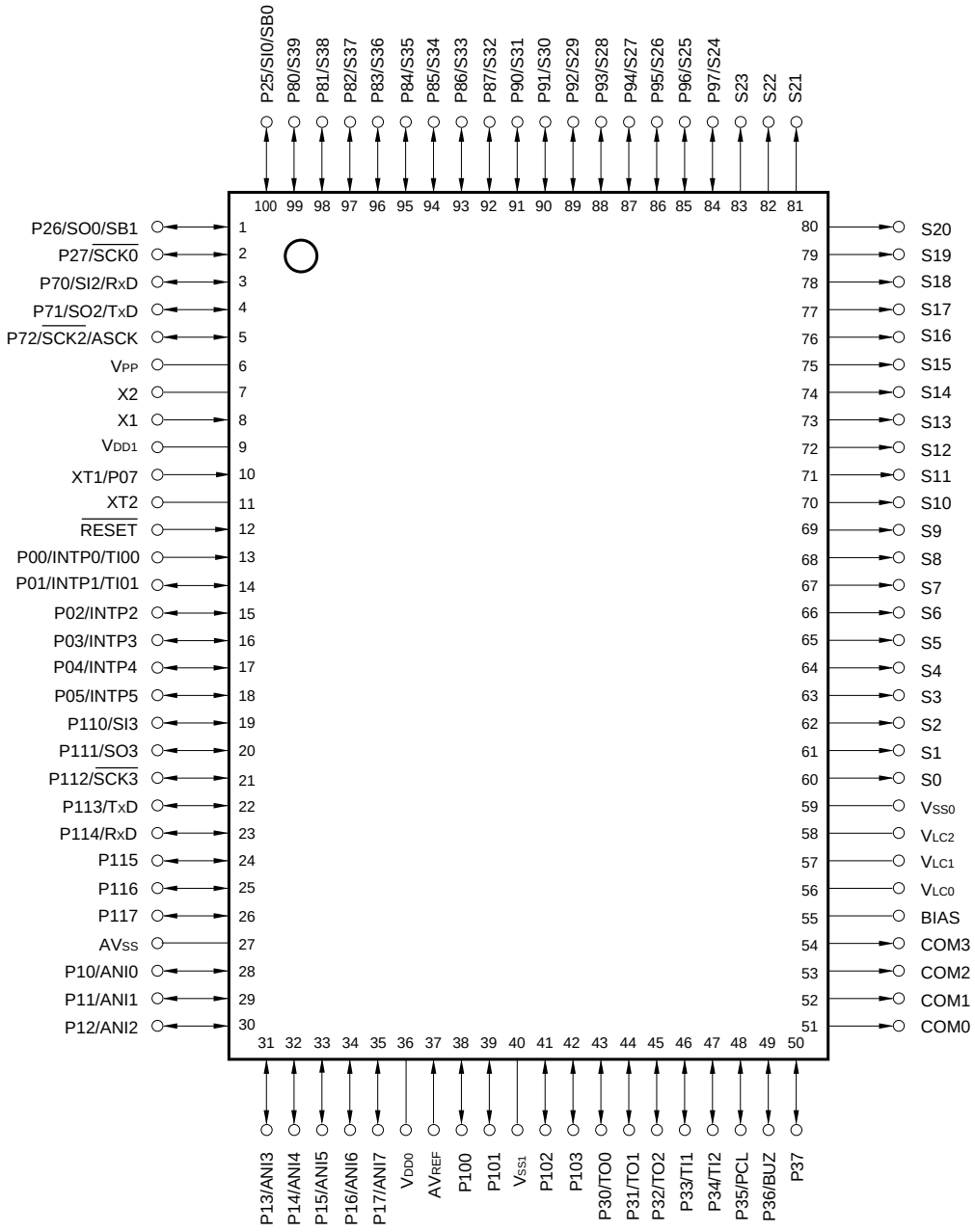
★ • 100-pin plastic LQFP (fine pitch) (14 × 14 mm)
μPD78P0308GC-8EU



★ **Cautions 1. Connect V_{PP} pin directly to V_{SS0} or V_{SS1}.**
2. Connect AV_{SS} pin to V_{SS0}.

Remark When this device is used in applications where noise generated from the microcontroller should be reduced, V_{DD0} and V_{DD1} should be powered separately, and noise reduction measures should be implemented, such as connecting V_{SS0} and V_{SS1} to separate ground lines.

- 100-pin plastic QFP (14 × 20 mm)
  μPD78P0308GF-3BA
- 100-pin ceramic WQFN (14 × 20 mm)
  μPD78P0308KL-T



Cautions 1. Connect V_{PP} pin directly to V_{SS0} or V_{SS1}.

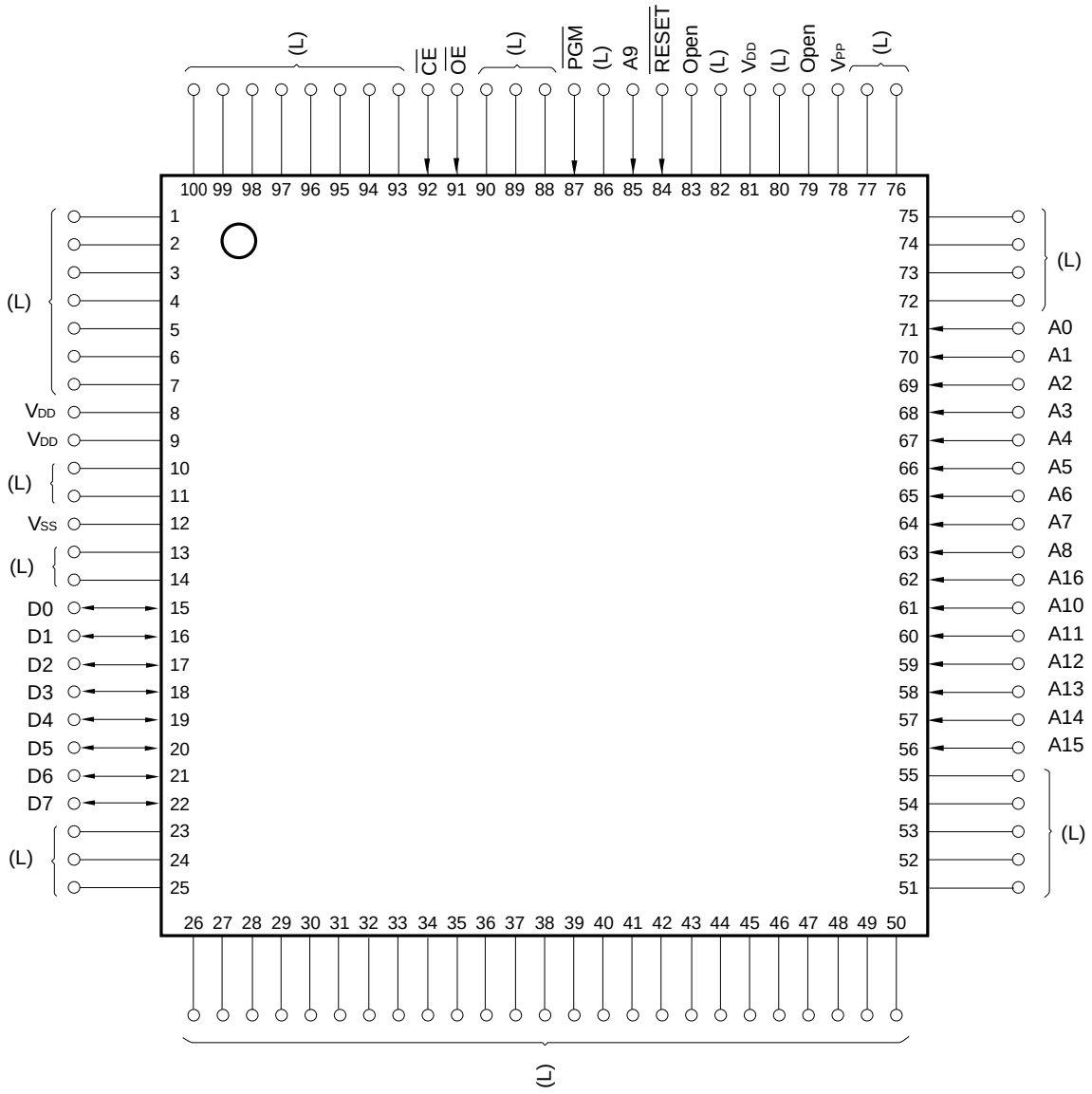
2. Connect AV_{SS} pin to V_{SS0}.

Remark When this device is used in applications where noise generated from the microcontroller should be reduced, V_{DD0} and V_{DD1} should be powered separately, and noise reduction measures should be implemented, such as connecting V_{SS0} and V_{SS1} to separate ground lines.

ANI0-ANI7	:	Analog Input	PCL	: Programmable Clock
ASCK	:	Asynchronous Serial Clock	$\overline{\text{RESET}}$	: Reset
AV_{REF}	:	Analog Reference Voltage	RxD	: Receive Data
AV_{SS}	:	Analog Ground	S0-S39	: Segment Output
BIAS	:	LCD Power Supply Bias Control	SB0, SB1	: Serial Bus
BUZ	:	Buzzer Clock	$\overline{\text{SCK0}}$, $\overline{\text{SCK2}}$, $\overline{\text{SCK3}}$	: Serial Clock
COM0-COM3	:	Common Output	SI0, SI2, SI3	: Serial Input
INTP0-INTP5	:	Interrupt from Peripherals	SO0, SO2, SO3	: Serial Output
P00-P05, P07	:	Port 0	TI00, TI01, TI1,TI2	: Timer Input
P10-P17	:	Port 1	TO0-TO2	: Timer Output
P25-P27	:	Port 2	TxD	: Transmit Data
P30-P37	:	Port 3	V_{DD0}, V_{DD1}	: Power Supply
P70-P72	:	Port 7	V_{LC0}-V_{LC2}	: LCD Power Supply
P80-P87	:	Port 8	V_{PP}	: Programming Power Supply
P90-P97	:	Port 9	V_{SS0}, V_{SS1}	: Ground
P100-P103	:	Port 10	X1, X2	: Crystal (Main System Clock)
P110-P117	:	Port 11	XT1, XT2	: Crystal (Subsystem Clock)

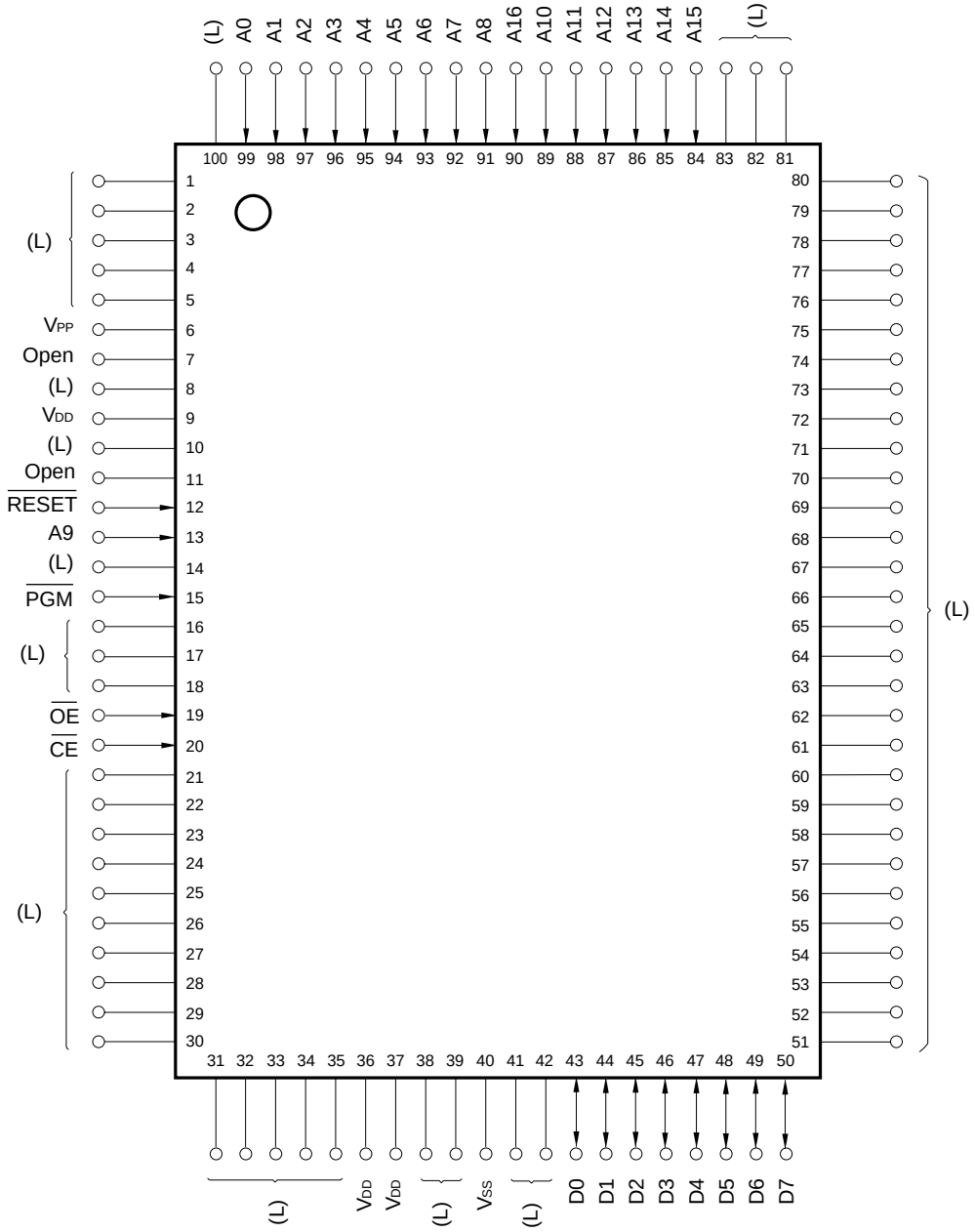
(2) PROM programming mode

★ • 100-pin plastic LQFP (fine pitch) (14 × 14 mm)
μPD78P0308GC-8EU



Cautions 1. (L): Independently connect to V_{SS} via a pull-down resistor.
2. V_{SS}: Connect to GND.
3. $\overline{RESET}$: Set to low level.
4. Open: Leave open.

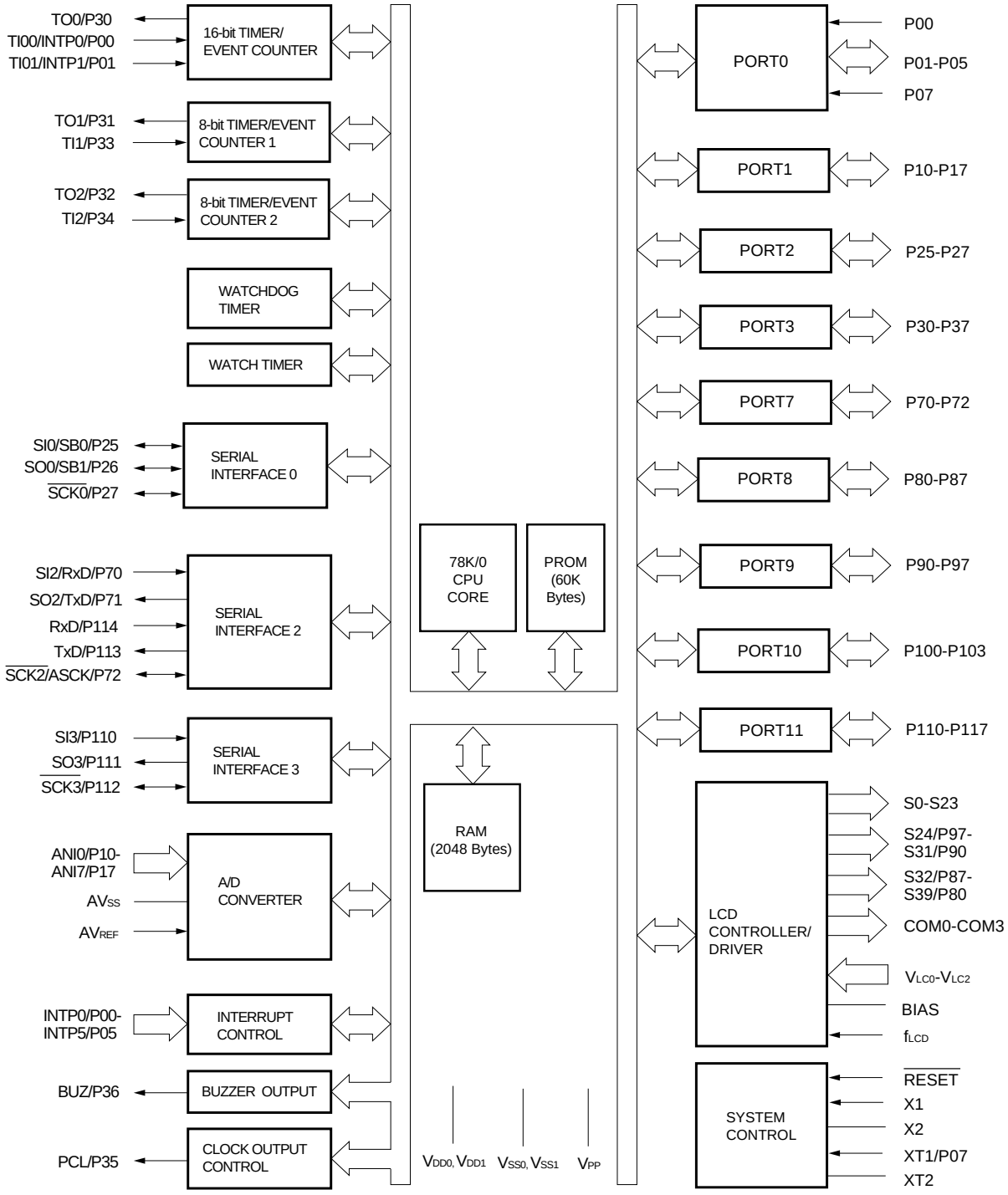
- 100-pin plastic QFP (14 × 20 mm)
  μPD78P0308GF-3BA
- 100-pin ceramic WQFN
  μPD78P0308KL-T



Cautions 1. (L): Independently connect to V_{SS} via a pull-down resistor.
2. V_{SS}: Connect to GND.
3. $\overline{RESET}$: Set to low level.
4. Open: Leave open.

A0 to A16	: Address Bus	$\overline{RESET}$	: Reset
$\overline{CE}$	: Chip Enable	V_{DD}	: Power Supply
D0 to D7	: Data Bus	V_{PP}	: Programming Power Supply
$\overline{OE}$	: Output Enable	V_{SS}	: Ground
$\overline{PGM}$	: Program		

BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN THE μPD78P0308 AND MASK ROM VERSIONS

The μPD78P0308 is a single-chip microcontroller with an on-chip one-time PROM or with an on-chip EPROM, which has program write, erasure, and rewrite capability.

It is possible to make all the functions except for PROM specification, and mask option of LCD drive power supply split resistor, the same as those of mask ROM versions by setting the memory size switching register (IMS).

Difference between the PROM version (μPD78P0308) and mask ROM versions (μPD780306, 780308) are shown in Table 1-1.

Table 1-1. Differences between the μPD78P0308 and Mask ROM Versions

Item	μPD78P0308	Mask ROM Versions
Internal ROM configuration	One-time PROM/EPROM	Mask ROM
Internal ROM capacity	60 Kbytes	μPD780306: 48 Kbytes μPD780308: 60 Kbytes
Internal ROM capacity change by the memory size switching register (IMS)	Possible[Note]	Impossible
IC pin	No	Yes
V_{PP} pin	Yes	No
Mask options of LCD drive power supply split resistor	None	Available
Electrical specifications, recommended soldering conditions	Refer to data sheet of the individual product.	

Note The internal PROM capacity is set to 60 Kbytes by $\overline{\text{RESET}}$ input.

★ **Caution There are differences in noise immunity and noise radiation between the PROM and mask ROM versions. When pre-producing an application set with the PROM version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the set using consumer samples (not engineering samples) of the mask ROM version.**

2. PIN FUNCTIONS

2.1 Pins in Normal Operating Mode

(1) Port pins (1/2)

Pin Name	Input/Output	Function		After Reset	Alternate Function
P00	Input	Port 0	Input only	Input	INTP0/TI00
P01	Input/output	7-bit input/output port	Input/output is specifiable bit-wise. When used as the input port, on-chip pull-up resistor connection can be specified by means of software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P07[Note 1]	Input		Input only	Input	XT1
P10-P17	Input/output	Port 1 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, on-chip pull-up resistor connection can be specified by means of software. [Note 2]		Input	ANI0-ANI7
P25	Input/output	Port 2 3-bit input/output port Input/output is specifiable bit-wise. When used as the input port, on-chip pull-up resistor connection can be specified by means of software.		Input	SI0/SB0
P26					SO0/SB1
P27					$\overline{\text{SCK0}}$
P30	Input/output	Port 3 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, on-chip pull-up resistor connection can be specified by means of software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—

Notes 1. When P07/XT1 pins are used as the input ports, set bit 6 (FRC) of the processor clock control register (PCC) to 1, and be sure not to use the feedback resistor of the subsystem clock oscillator.

2. When P10/ANI0-P17/ANI7 pins are used as the analog inputs for the A/D converter, shift port 1 to input mode. The on-chip pull-up resistor is automatically disabled.

(1) Port pins (2/2)

Pin Name	Input/Output	Function	After Reset	Alternate Function
P70	Input/output	Port 7 3-bit input/output port Input/output is specifiable bit-wise. When used as the input port, on-chip pull-up resistor connection can be specified by means of software.	Input	SI2/RxD
P71				SO2/TxD
P72				$\overline{\text{SCK2}}$/ASCK
P80-P87	Input/output	Port 8 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, on-chip pull-up resistor connection can be specified by means of software. Input/output port/segment signal output function is specifiable in 2-bit units by the LCD display control register (LCDC).	Input	S39-S32
P90-P97	Input/output	Port 9 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, on-chip pull-up resistor connection can be specified by means of software. Input/output port/segment signal output function is specifiable in 2-bit units by the LCD display control register (LCDC).	Input	S31-S24
P100-P103	Input/output	Port 10 4-bit input/output port Input/output is specifiable bit-wise. When used as the input port, on-chip pull-up resistor connection can be specified by means of software. It is possible to directly drive LEDs.	Input	—
P110	Input/output	Port 11 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, on-chip pull-up resistor connection can be specified by means of software. Falling edge detection is possible.	Input	SI3
P111				SO3
P112				$\overline{\text{SCK3}}$
P113				TxD
P114				RxD
P115-P117				—

(2) Non-port pins (1/2)

Pin Name	Input/Output	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input for which the active edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
SI0	Input	Serial interface serial data input.	Input	P25/SB0
SI2				P70/RxD
SI3				P110
SO0	Output	Serial interface serial data output.	Input	P26/SB1
SO2				P71/TxD
SO3				P111
SB0	Input/output	Serial interface serial data input/output.	Input	P25/SI0
SB1				P26/SO0
$\overline{SCK0}$	Input/output	Serial interface serial clock input/output.	Input	P27
$\overline{SCK2}$				P72/ASCK
$\overline{SCK3}$				P112
RxD	Input	Asynchronous serial interface serial data input.	Input	P70/SI2, P114
TxD	Output	Asynchronous serial interface serial data output.	Input	P71/SO2, P113
ASCK	Input	Asynchronous serial interface serial clock input.	Input	P72/$\overline{SCK2}$
TI00	Input	External count clock input to 16-bit timer (TM0).	Input	P00/INTP0
TI01		Capture trigger signal input to capture register (CR00).		P01/INTP1
TI1		External count clock input to 8-bit timer (TM1).		P33
TI2		External count clock input to 8-bit timer (TM2).		P34
TO0	Output	16-bit timer (TM0) output (also used for 14-bit PWM output).	Input	P30
TO1		8-bit timer (TM1) output.		P31
TO2		8-bit timer (TM2) output.		P32
PCL	Output	Clock output (for main system clock, subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
S0-S23	Output	LCD controller/driver segment signal output.	Output	—
S24-S31			Input	P97-P90
S32-S39				P87-P80
COM0-COM3	Output	LCD controller/driver common signal output.	Output	—
V_{LC0}-V_{LC2}	—	LCD drive voltage.	—	—
BIAS	—	LCD drive power supply.	—	—

(2) Non-port pins (2/2)

Pin Name	Input/Output	Function	After Reset	Alternate Function
ANI0-ANI7	Input	A/D converter analog input.	Input	P10-P17
AV_{REF}	Input	A/D converter reference voltage input (also used for analog input).	—	—
AV_{SS}	—	A/D converter ground potential. Set to the same potential as V_{SS0}.	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Crystal resonator connection for main system clock oscillation.	—	—
X2	—		—	—
XT1	Input	Crystal resonator connection for subsystem clock oscillation.	Input	P07
XT2	—		—	—
V_{DD0}	—	Positive power supply for ports.	—	—
V_{SS0}	—	Ground potential for ports.	—	—
V_{DD1}	—	Positive power supply (except for ports and analog).	—	—
V_{SS1}	—	Ground potential (except for ports and analog).	—	—
★ V_{PP}	—	High voltage application in program write/verify mode. Connect directly to V_{SS0} or V_{SS1} in normal operating mode.	—	—

2.2 Pins in PROM Programming Mode

Pin Name	Input/Output	Function
$\overline{RESET}$	Input	PROM programming mode setting. When +5 V or +12.5 V is applied to the V_{PP} pin and a low-level signal is applied to the $\overline{RESET}$ pin, this chip is set in the PROM programming mode.
V_{PP}	Input	PROM programming mode setting and high voltage application during program write/verification.
A0-A16	Input	Address bus.
D0-D7	Input/output	Data bus.
$\overline{CE}$	Input	PROM enable input/program pulse input.
$\overline{OE}$	Input	Read strobe input to PROM.
$\overline{PGM}$	Input	Program/program inhibit input in PROM programming mode.
V_{DD}	—	Positive power supply.
V_{SS}	—	Ground potential.

2.3 Pin Input/Output Circuits and Recommended Connection of Unused Pins

Types of input/output circuits of the pins and recommended connection of unused pins are shown in Table 2-1. For the configuration of each type of input/output circuit, see Figure 2-1.

Table 2-1. Type of Input/Output Circuit of Each Pin (1/2)

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connection for Unused Pins
P00/INTP0/TI00	2	Input	Connect to V_{SS0}.
P01/INTP1/TI01	8-C	Input/output	Independently connect to V_{SS0} via a resistor.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P07/XT1	16	Input	Connect to V_{DD0}.
P10/ANI0-P17/ANI7	11-B	Input/output	Independently connect to V_{DD0} or V_{SS0} via a resistor.
P25/SI0/SB0	10-B		
P26/SO0/SB1			
P27/$\overline{SCK0}$			
P30/TO0	5-H		
P31/TO1			
P32/TO2			
P33/TI1	8-C		
P34/TI2			
P35/PCL	5-H		
P36/BUZ			
P37			
P70/SI2/RxD	8-C		
P71/SO2/TxD	5-H		
P72/$\overline{SCK2}$/ASCK	8-C		
P80/S39-P87/S32	17-C		
P90/S31-P97/S24			
P100-P103	5-H		
P110/SI3	8-C		Independently connect to V_{DD0} via a resistor.
P111/SO3			
P112/$\overline{SCK3}$			
P113/TxD			
P114/RxD			
P115-P117			
S0-S23	17-B	Output	Leave open.
COM0-COM3	18-A		

Table 2-1. Type of Input/Output Circuit of Each Pin (2/2)

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connection for Unused Pins
V_{LC0}-V_{LC2}	—	—	Leave open.
BIAS			
$\overline{RESET}$	2	Input	—
XT2	16	—	Leave open.
AV_{REF}	—	—	Connect to V_{SS0}.
AV_{SS}			
★ V_{PP}			Connect directly to V_{SS0} or V_{SS1}.

Figure 2-1. List of Pin Input/Output Circuits (1/2)

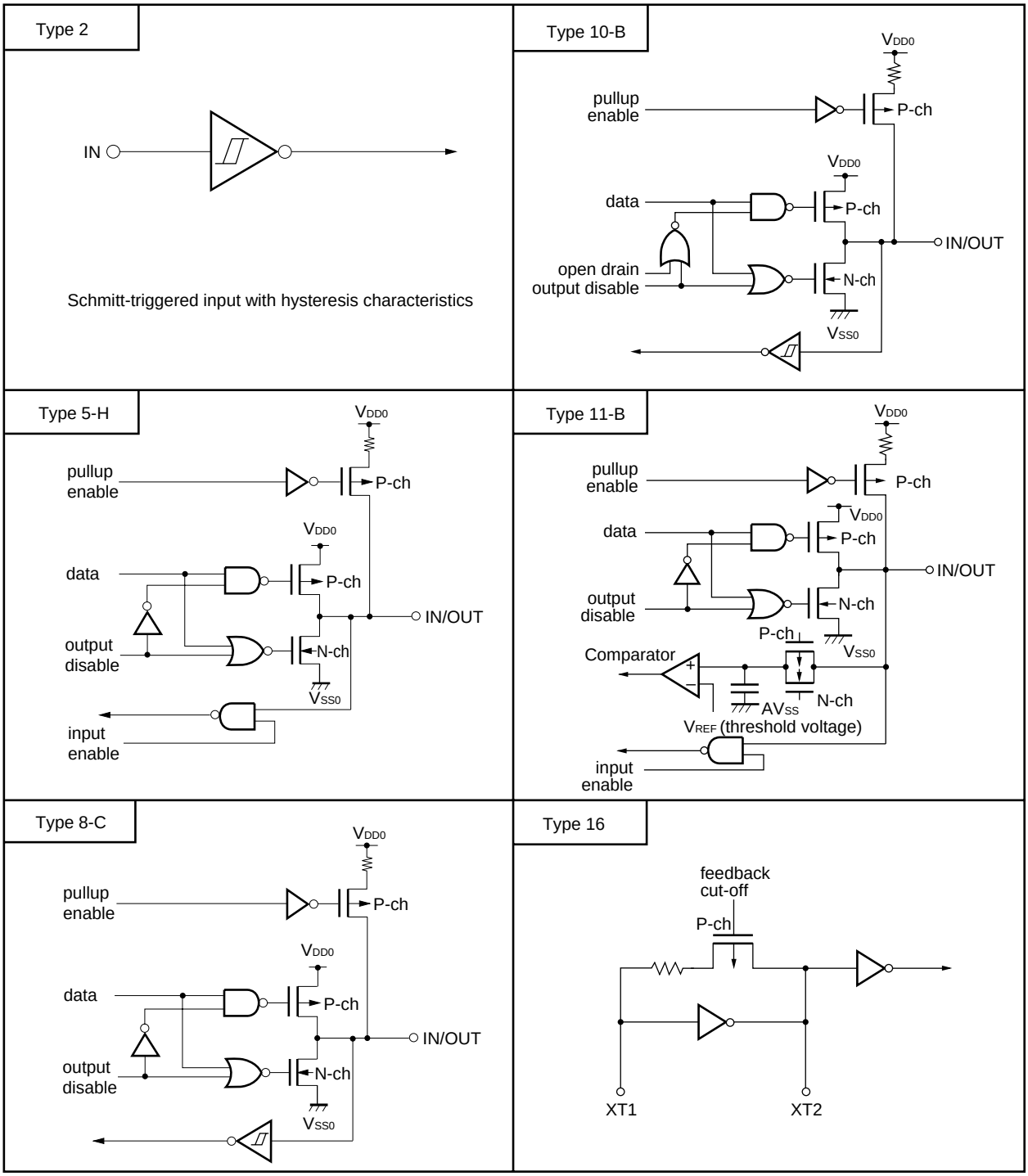
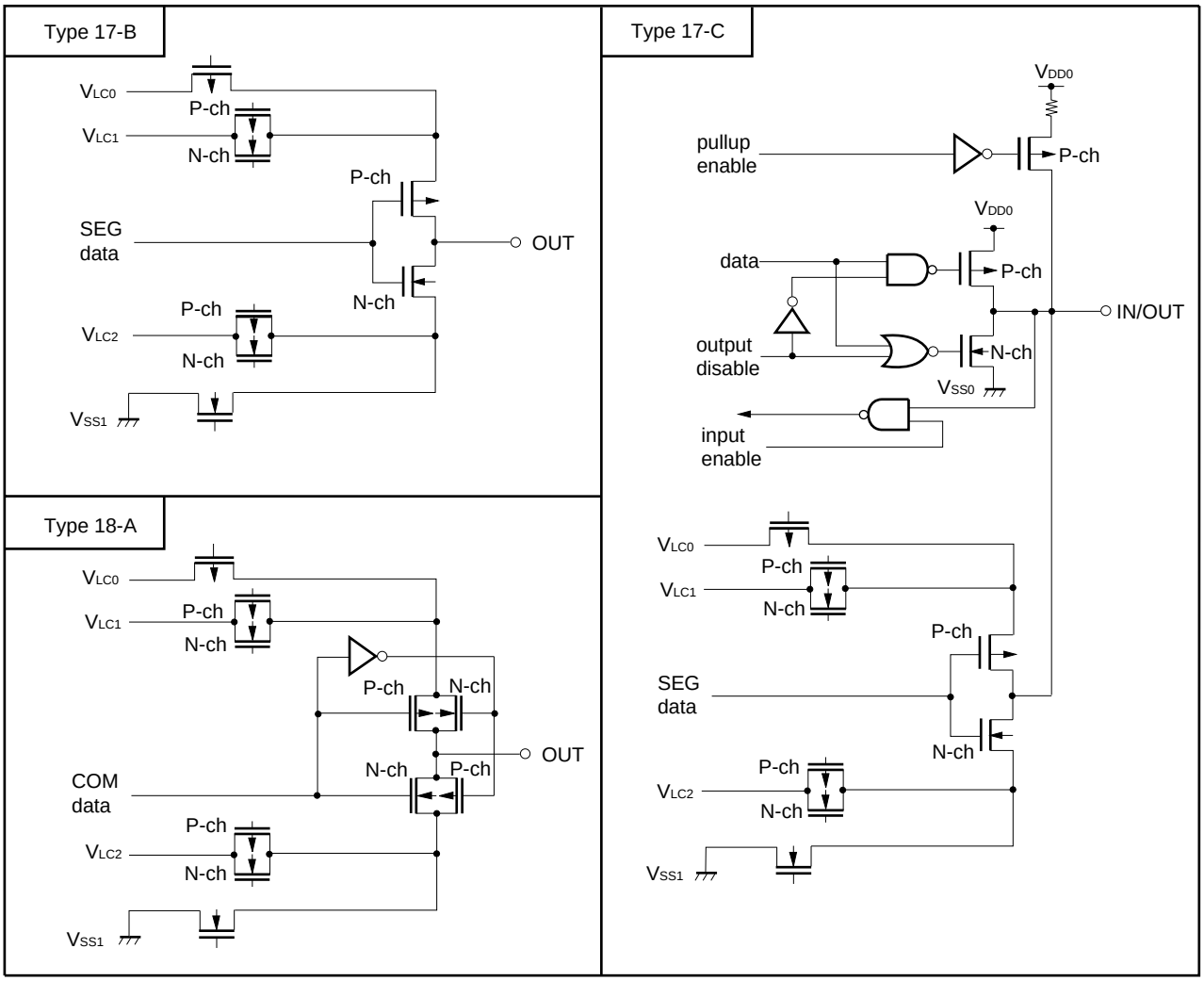


Figure 2-1. List of Pin Input/Output Circuits (2/2)



3. MEMORY SIZE SWITCHING REGISTER (IMS)

This is a register to disable use of part of internal memories by software. By setting this memory size switching register (IMS), it is possible to get the same memory map as that of the mask ROM versions with a different internal memory (ROM) capacity.

IMS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets IMS to CFH.

Figure 3-1. Memory Size Switching Register Format

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

ROM3	ROM2	ROM1	ROM0	Internal ROM Capacity Selection
1	1	0	0	48 Kbytes
1	1	1	1	60 Kbytes
Other than above				Setting prohibited

RAM2	RAM1	RAM0	Internal High-Speed RAM Capacity Selection
1	1	0	1024 bytes
Other than above			Setting prohibited

Table 3-1 shows the setting values of IMS that make the memory mapping the same as that of the mask ROM version.

Table 3-1. Memory Size Switching Register Setting Values

Target Mask ROM Versions	IMS Setting Value
μPD780306	CCH
μPD780308	CFH

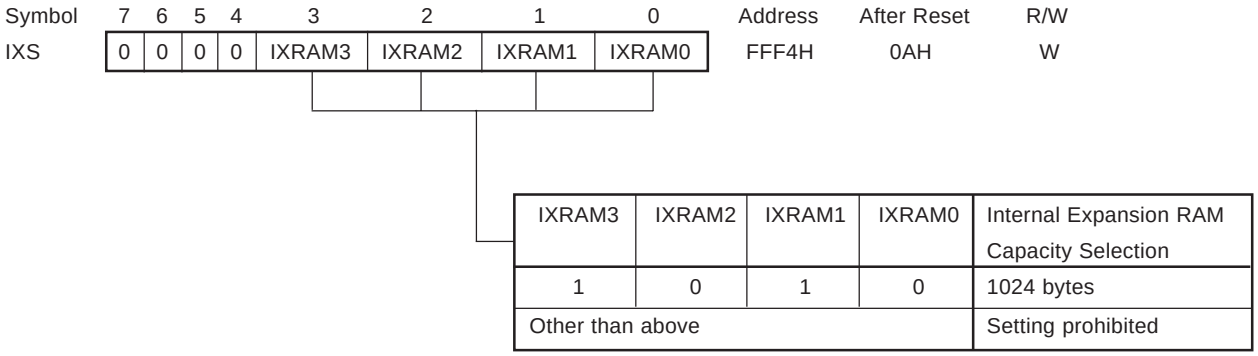
4. INTERNAL EXPANSION RAM SIZE SWITCHING REGISTER (IXS)

This register is used to set the internal expansion RAM capacity by software. By setting this internal expansion RAM size switching register (IXS), it is possible to get the same memory map as that of the mask ROM versions with a different internal expansion RAM capacity.

IXS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets IXS to 0AH.

Figure 4-1. Internal Expansion RAM Size Switching Register Format



IXRAM3	IXRAM2	IXRAM1	IXRAM0	Internal Expansion RAM Capacity Selection
1	0	1	0	1024 bytes
Other than above				Setting prohibited

Table 4-1 shows the setting values of IXS that make the memory mapping the same as that of the mask ROM versions.

Table 4-1. Internal Expansion RAM Size Switching Register Setting Values

Target Mask ROM Versions	IXS Setting Value
μPD780306	0AH
μPD780308	

5. PROM PROGRAMMING

The μPD78P0308 has an on-chip 60-Kbyte PROM as a program memory. For programming, set the PROM programming mode with the V_{PP} and $\overline{RESET}$ pins. For the connection of unused pins, refer to **"PIN CONFIGURATIONS (2) PROM programming mode."**

Caution Programs must be written in addresses 0000H to EFFFH (The last address EFFFH must be specified).
They cannot be written by a PROM programmer that cannot specify the write address.

5.1 Operating Modes

When +5 V or +12.5 V is applied to the V_{PP} pin and a low-level signal is applied to the $\overline{RESET}$ pin, the PROM programming mode is set. This mode will become the operating mode as shown in Table 5-1 when the $\overline{CE}$, $\overline{OE}$ and $\overline{PGM}$ pins are set as shown.

Further, when the read mode is set, it is possible to read the contents of the PROM.

Table 5-1. Operating Modes of PROM Programming

Pin / Operating Mode	$\overline{RESET}$	V_{PP}	V_{DD}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	D0-D7
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High-impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				×	H	H	High-impedance
				×	L	L	
Read		+5 V	+5 V	L	L	H	Data output
Output disable				L	H	×	High-impedance
Standby				H	×	×	High-impedance

× : L or H

(1) Read mode

Read mode is set if $\overline{CE}$ = L, $\overline{OE}$ = L is set.

(2) Output disable mode

Data output becomes high-impedance, and is in the output disable mode, if $\overline{OE}$ = H is set.

Therefore, it allows data to be read from any device by controlling the $\overline{OE}$ pin, if multiple μPD78P0308s are connected to the data bus.

(3) Standby mode

Standby mode is set if $\overline{CE}$ = H is set.

In this mode, data outputs become high-impedance irrespective of the $\overline{OE}$ status.

(4) Page data latch mode

Page data latch mode is set if $\overline{CE}$ = H, $\overline{PGM}$ = H, $\overline{OE}$ = L are set at the beginning of page write mode.

In this mode, 1 page 4-byte data is latched in an internal address/data latch circuit.

(5) Page write mode

After 1 page 4 bytes of addresses and data are latched in the page data latch mode, a page write is executed by applying a 0.1-ms program pulse (active low) to the $\overline{PGM}$ pin with $\overline{CE}$ = H, $\overline{OE}$ = H. Then, program verification can be performed, if $\overline{CE}$ = L, $\overline{OE}$ = L are set.

If programming is not performed by a one-time program pulse, X times (X ≤ 10) write and verification operations should be executed repeatedly.

(6) Byte write mode

Byte write is executed when a 0.1-ms program pulse (active low) is applied to the $\overline{PGM}$ pin with $\overline{CE}$ = L, $\overline{OE}$ = H. Then, program verification can be performed if $\overline{OE}$ = L is set.

If programming is not performed by a one-time program pulse, X times (X ≤ 10) write and verification operations should be executed repeatedly.

(7) Program verify mode

Program verify mode is set if $\overline{CE}$ = L, $\overline{PGM}$ = H, $\overline{OE}$ = L are set.

In this mode, check if a write operation is performed correctly after the write.

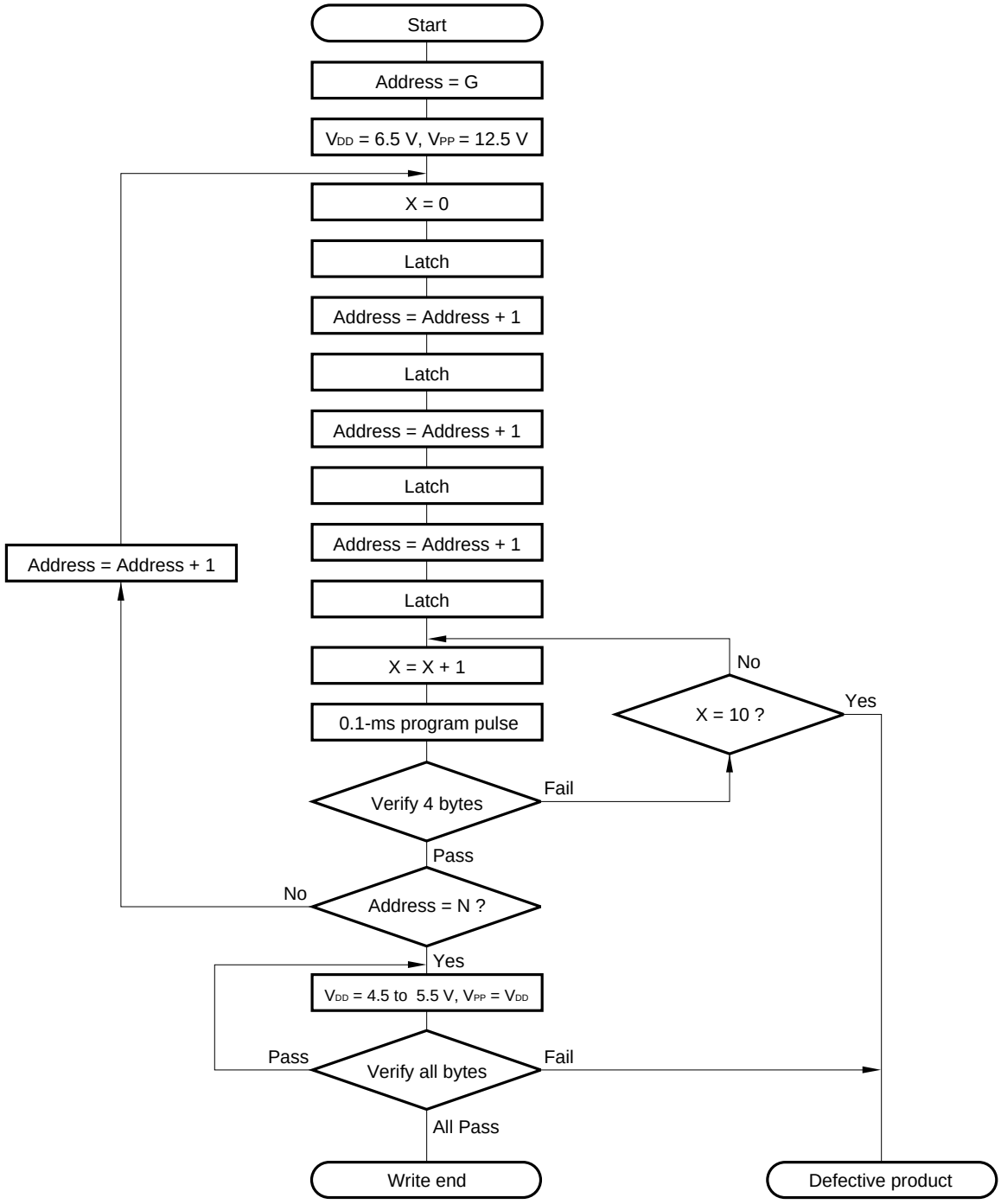
(8) Program inhibit mode

Program inhibit mode is used when the $\overline{OE}$ pin, V_{PP} pin, and D0-D7 pins of multiple μPD78P0308s are connected in parallel and a write is performed to one of those devices.

When a write operation is performed, the page write mode or byte write mode described above is used. At this time, a write is not performed to a device whose $\overline{PGM}$ pin is driven high.

5.2 PROM Write Procedure

Figure 5-1. Page Program Mode Flow Chart



G = Start address

N = Program last address

Figure 5-2. Page Program Mode Timing

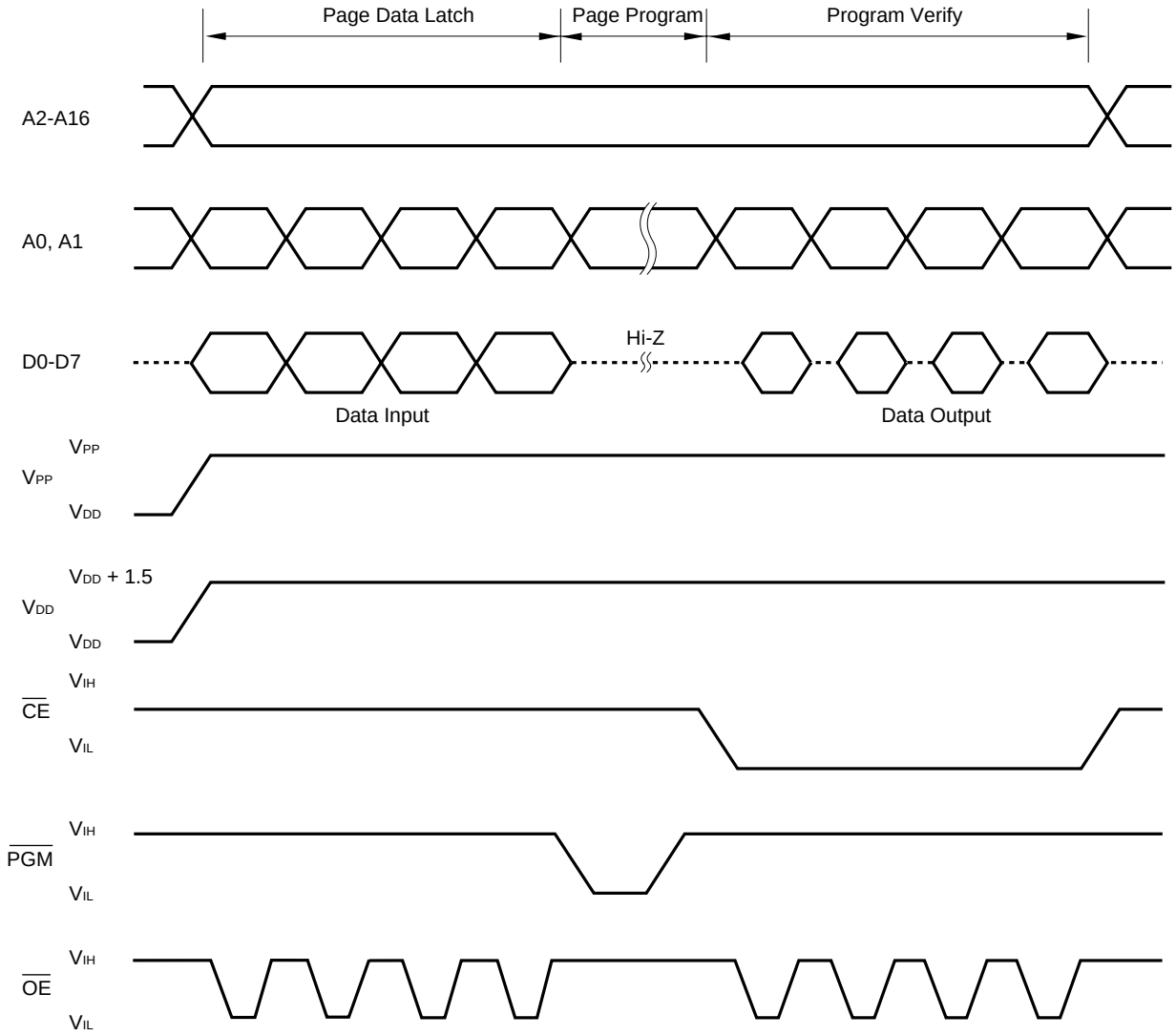
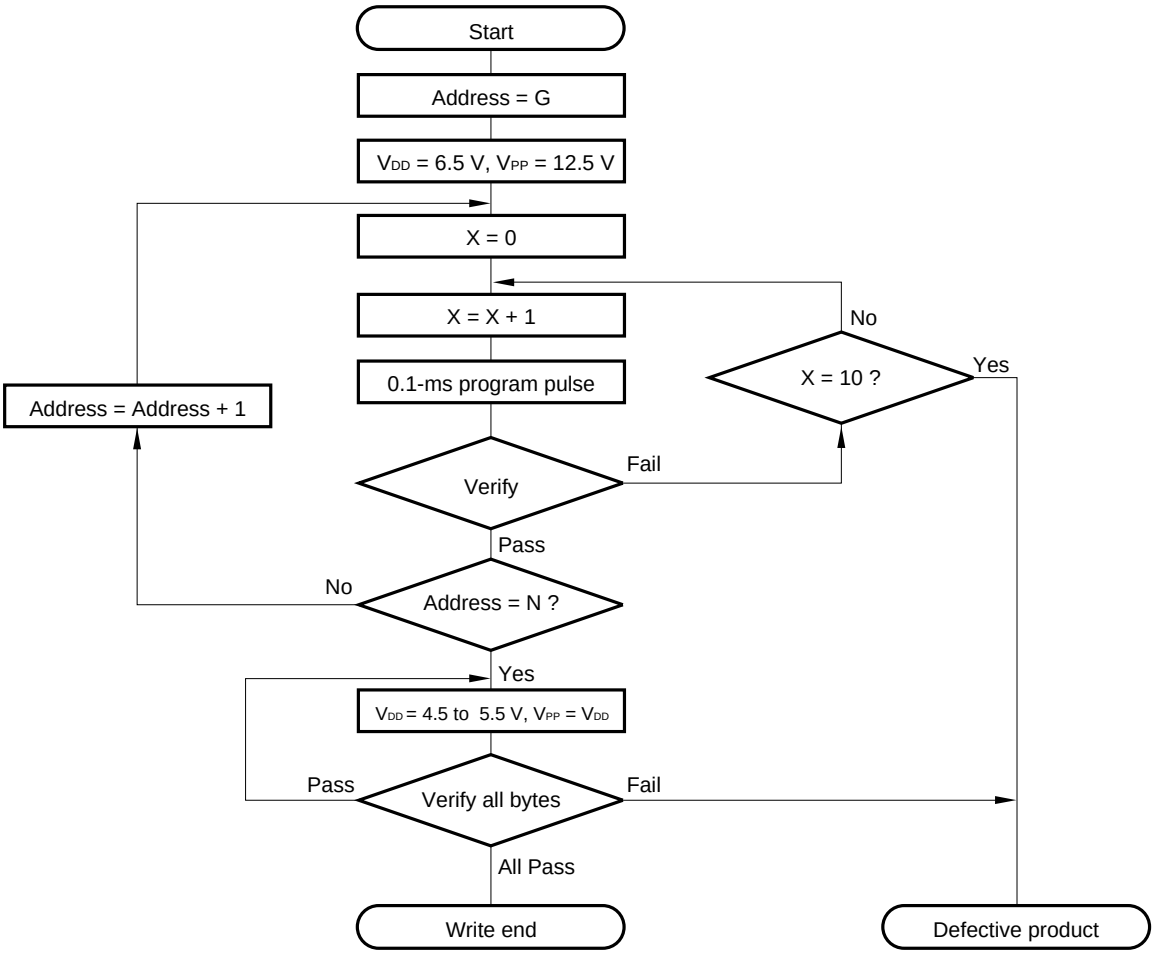


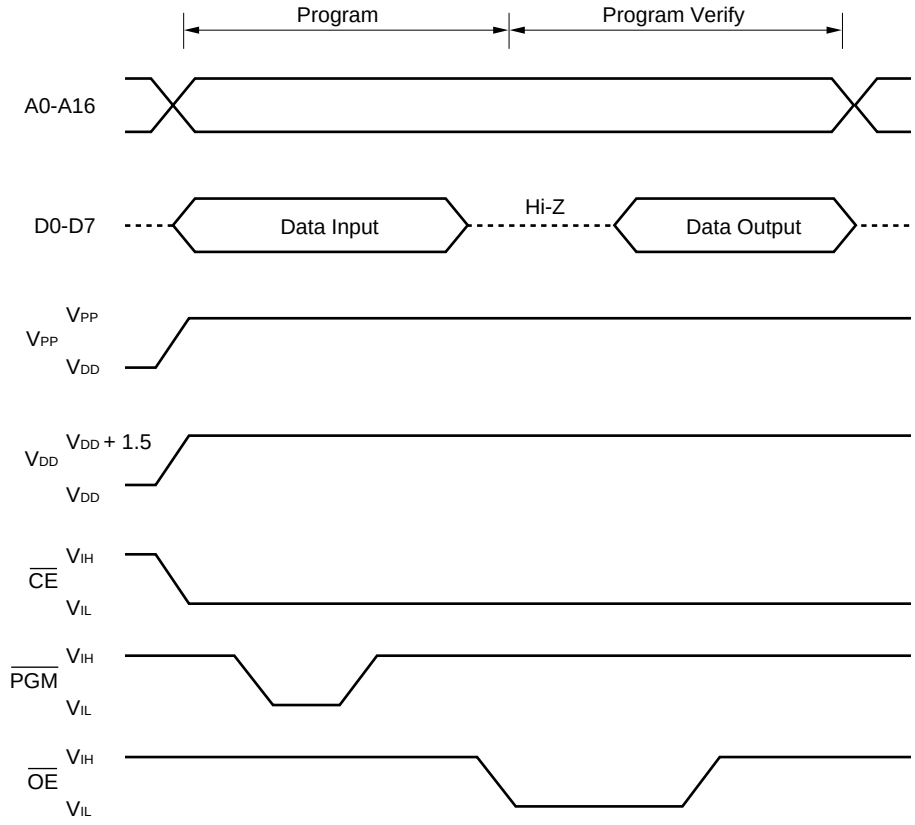
Figure 5-3. Byte Program Mode Flow Chart



G = Start address

N = Program last address

Figure 5-4. Byte Program Mode Timing



Cautions 1. V_{DD} should be applied before V_{PP}, and cut after V_{PP}.

2. V_{PP} should not exceed +13.5 V including overshoot.

3. Disconnection during application of ±12.5 V to V_{PP} may have an adverse effect on reliability.

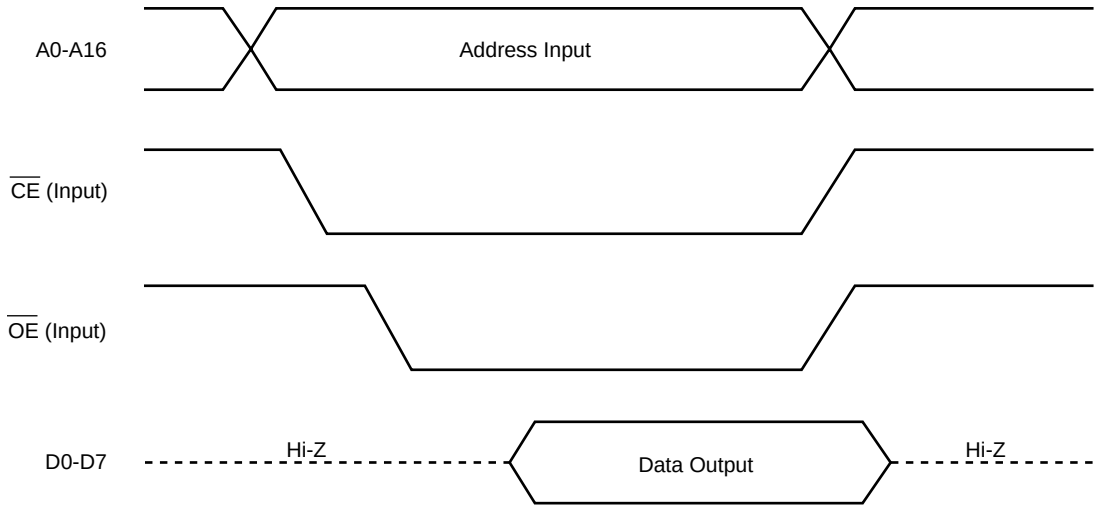
5.3 PROM Read Procedure

The contents of PROM are readable to the external data bus (D0-D7) according to the read procedure shown below.

(1) Fix the $\overline{\text{RESET}}$ pin at low level, supply +5 V to the V_{PP} pin, and connect all other unused pins as shown in **"PIN CONFIGURATIONS (2) PROM programming mode".**
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) Input address of data to be read into the A0-A16 pins.
(4) Read mode
(5) Output data to D0-D7 pins.

The timings of the above steps (2) to (5) are shown in Figure 5-5.

Figure 5-5. PROM Read Timings



6. PROGRAM ERASURE (μPD78P0308YKL-T ONLY)

The μPD78P0308KL-T is capable of erasing (FFH) the data written in a program memory and rewriting.

To erase the programmed data, expose the erasure window to light having a wavelength shorter than about 400 nm. Normally, irradiate ultraviolet rays of 254-nm wavelength. The amount of exposure required to completely erase the programmed data is as follows:

- UV intensity × erasing time : 30 W • s/cm^2 or more
- Erasure time: 40 min. or more (When a UV lamp of 12 mW/cm^2 is used. However, a longer time may be needed because of deterioration in performance of the UV lamp, soiled erasure window, etc.)

When erasing the contents of data, set up the UV lamp within 2.5 cm from the erasure window. Further, if a filter is provided for a UV lamp, irradiate the ultraviolet rays after removing the filter.

7. OPAQUE FILM ON ERASURE WINDOW (μPD78P0308KL-T ONLY)

To protect from unintentional erasure by rays other than that of the lamp for erasing EPROM contents, or to protect internal circuit other than EPROM from misoperating by rays, cover the erasure window with an opaque film when EPROM contents erasure is not performed.

8. ONE-TIME PROM VERSION SCREENING

The one-time PROM version (μPD78P0308GC-8EU and 78P0308GF-3BA) cannot be tested completely by NEC before it is shipped, because of its structure. It is recommended to perform screening to verify PROM after writing necessary data and performing high-temperature storage under the condition below.

Storage Temperature	Storage Time
125°C	24 hours

NEC offers for an additional fee service from one-time PROM writing to marking, screening, and verify for products designated as "QTOP microcontroller". This additional fee service is being planned for μPD78P0308. Please contact an NEC sales representative for details.

★ 9. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Test Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
	V_{PP}			–0.3 to +13.5	V
	AV_{REF}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00-P05, P07, P10-P17, P25-P27, P30-P37, P70-P72, P80-P87, P90-P97, P100-P103, P110-P117, X1, X2, XT2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	A9	PROM Programing mode	–0.3 to +13.5	V
Output Voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10-P17	Analog input pin	AV_{SS} – 0.3 to AV_{REF} + 0.3	V
Output current, high	I_{OH}	1 pin		–10	mA
		Total for P01-P05, P10-P17, P25-P27, P70-P72, P110-P117		–15	mA
		Total for P30-P37, P80-P87, P90-P97, P100-P117		–15	mA
Output current, low	I_{OL}	1 pin	Peak value	30	mA
			r.m.s. value	15[Note]	mA
		Total for P01-P05, P10-P17, P110-P117	Peak value	60	mA
			r.m.s. value	40[Note]	mA
		Total for P30-P37, P100-P103	Peak value	140	mA
			r.m.s. value	100[Note]	mA
		Total for P25-P27, P70-P72, P80-P87, P90-P97	Peak value	50	mA
			r.m.s. value	20[Note]	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note The root mean square (r.m.s.) value should be calculated as follows: [r.m.s. value] = [Peak value] $\times\sqrt{\text{Duty}}$

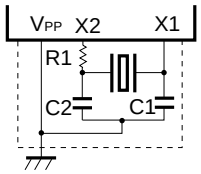
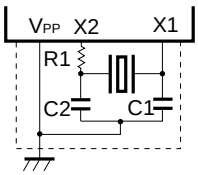
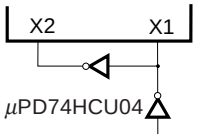
Caution The product quality may be damaged even if a value of only one of the above parameters exceeds the absolute maximum rating or any value exceeds the absolute maximum rating for an instant. That is, the absolute maximum rating is a rating value which may cause a product to be damaged physically. The absolute maximum rating values must therefore be observed in using the product.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

CAPACITANCE (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz			15	pF
Output capacitance	C_{OUT}	Unmeasured pins returned			15	pF
I/O capacitance	C_{IO}	to 0 V.			15	pF

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended circuit	Parameter	Test conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1	V_{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization timeNote 2	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)Note 1		1.0		5.0	MHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X)Note 1		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

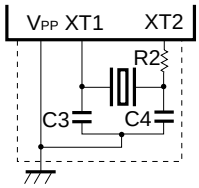
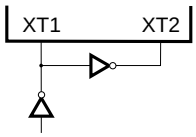
2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wiring in the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground it to the ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. If the main system clock oscillator is operated by the subsystem clock when the main system clock is stopped, reswitching to the main system clock should be performed after the oscillation stabilization time has been obtained by the program.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT})Note 1		32		100	kHz
		XT1 input high-/low-level width (t_{XTH}/t_{XTL})		5		15	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} has reached the minimum oscillation voltage range.

Cautions 1. When using the subsystem clock oscillator, wiring in the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground it to the ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplification circuit to provide low consumption current, causing misoperation due to noise more frequently than the main system clock oscillator. Special care should therefore be taken regarding the wiring method when the subsystem clock is used.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10-P17, P30-P32, P35-P37, P80-P87, P90-P97, P100-P103		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00-P05, P25-P27, P33, P34, P70-P72, P110-P117, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2		V_{DD} – 0.5		V_{DD}	V
	V_{IH4}	XT1/P07, XT2	4.5 ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			2.7 ≤ V_{DD} < 4.5 V	0.9V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10-P17, P30-P32, P35-P37, P80-P87, P90-P97, P100-P103		0		0.3V_{DD}	V
	V_{IL2}	P00-P05, P25-P27, P33, P34, P70-P72, P110-P117, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL3}	X1, X2		0		0.4	V
	V_{IL4}	XT1/P07, XT2	4.5 ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
			2.7 ≤ V_{DD} < 4.5 V	0		0.1V_{DD}	V
Output voltage, high	V_{OH}	V_{DD} = 4.5 to 5.5 V I_{OH} = –1 mA		V_{DD} – 1.0		V_{DD}	V
		I_{OH} = –100 μA		V_{DD} – 0.5		V_{DD}	V
Output voltage, low	V_{OL1}	P100-P103	V_{DD} = 4.5 to 5.5 V, I_{OL} = 15 mA		0.4	2.0	V
		P01-P05, P10-P17, P25-P27, P30-P37, P70-P72, P80-P87, P90-P97, P110-P117	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V_{DD} = 4.5 to 5.5 V, open-drain, pulled up (R = 1 kΩ)			0.2V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as the those of port pins.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00-P05, P10-P17, P25-P27, P30-P37, P70-P72, P80-P87, P90-P97, P100-P103, P110-P117			3	μA
	I_{LIH2}		X1, X2, XT1/P07, XT2			20	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00-P05, P10-P17, P25-P27, P30-P37, P70-P72, P80-P87, P90-P97, P100-P103, P110-P117			–3	μA
	I_{LIH2}		X1, X2, XT1/P07, XT2			–20	μA
Output leakage current, high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistor	R	V_{IN} = 0 V	P01-P05, P10-P17, P25-P27, P30-P37, P70-P72, P80-P87, P90-P97, P100-P103, P110-P117	15	40	90	kΩ
Supply current[Note 1]	I_{DD1}	5.00-MHz crystal oscillation (f_{XX} = 2.5 MHz)[Note 2] operating mode	V_{DD} = 5.0 V ±10%[Note 5]		5	15	mA
			V_{DD} = 3.0 V ±10%[Note 6]		0.7	2.1	mA
		5.00-MHz crystal oscillation (f_{XX} = 5.0 MHz)[Note 3] operating mode	V_{DD} = 5.0 V ±10%[Note 5]		9	27	mA
			V_{DD} = 3.0 V ±10%[Note 6]		1	3	mA
	I_{DD2}	5.00-MHz crystal oscillation (f_{XX} = 2.5 MHz)[Note 2] HALT mode	V_{DD} = 5.0 V ±10%		1.4	4.2	mA
			V_{DD} = 3.0 V ±10%		500	1500	μA
		5.00-MHz crystal oscillation (f_{XX} = 5.0 MHz)[Note 3] HALT mode	V_{DD} = 5.0 V ±10%		1.6	4.8	mA
			V_{DD} = 3.0 V ±10%		650	1950	μA
	I_{DD3}	32.768-kHz crystal oscillation operating mode[Note 4]	V_{DD} = 5.0 V ±10%		135	270	μA
			V_{DD} = 3.0 V ±10%		95	190	μA
	I_{DD4}	32.768-kHz crystal oscillation HALT mode[Note 4]	V_{DD} = 5.0 V ±10%		25	55	μA
			V_{DD} = 3.0 V ±10%		5	15	μA
	I_{DD5}	XT1 = V_{DD} STOP mode When feedback resistor is connected	V_{DD} = 5.0 V ±10%		1	30	μA
			V_{DD} = 3.0 V ±10%		0.5	10	μA
	I_{DD6}	XT1 = V_{DD} STOP mode When feedback resistor is disconnected	V_{DD} = 5.0 V ±10%		0.1	30	μA
			V_{DD} = 3.0 V ±10%		0.05	10	μA

Notes 1. Current flowing into V_{DD} pin. Not including the current flowing into A/D converter, on-chip pull-up resistors, or LCD split resistors.

2. Main system clock $f_{XX} = f_X/2$ operation (when oscillation mode selection register (OSMS) is set to 00H)

3. Main system clock $f_{XX} = f_X$ operation (when OSMS is set to 01H)

4. When the main system clock is stopped.

5. High-speed mode operation (when processor clock control register (PCC) is set to 00H)

6. Low-speed mode operation (when PCC is set to 04H)

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as the those of port pins.

LCD CONTROLLER/DRIVER CHARACTERISTICS (AT NORMAL OPERATION)

(1) Static Display Mode (T_A = –10 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}			2.7		V_{DD}	V
LCD output voltage deviation[Note] (common)	V_{ODC}	I_O = ±5 μA	$V_{LCD0} = V_{LCD}$	0		±0.2	V
LCD output voltage deviation[Note] (segment)	V_{ODS}	I_O = ±1 μA		0		±0.2	V

Note The voltage deviation is the difference between the output voltage and the corresponding ideal value of the segment or common output (V_{LCDn}; n = 0, 1, 2).

(2) 1/3 Bias Method (T_A = –10 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}			2.7		V_{DD}	V
LCD output voltage deviation[Note] (common)	V_{ODC}	I_O = ±5 μA	$V_{LCD0} = V_{LCD}$ $V_{LCD1} = V_{LCD} \times 2/3$	0		±0.2	V
LCD output voltage deviation[Note] (segment)	V_{ODS}	I_O = ±1 μA	$V_{LCD2} = V_{LCD} \times 1/3$	0		±0.2	V

Note The voltage deviation is the difference between the output voltage and the corresponding ideal value of the segment or common output (V_{LCDn}; n = 0, 1, 2).

(3) 1/2 Bias Method (T_A = –10 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}			2.7		V_{DD}	V
LCD output voltage deviation[Note] (common)	V_{ODC}	I_O = ±5 μA	$V_{LCD0} = V_{LCD}$ $V_{LCD1} = V_{LCD} \times 1/2$	0		±0.2	V
LCD output voltage deviation[Note] (segment)	V_{ODS}	I_O = ±1 μA	$V_{LCD2} = V_{LCD1}$	0		±0.2	V

Note The voltage deviation is the difference between the output voltage and the corresponding ideal value of the segment or common output (V_{LCDn}; n = 0, 1, 2).

Caution Characteristics at low-voltage operation are undecided.

AC CHARACTERISTICS

(1) Basic Operation (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating on main system clock (f_{XX} = 2.5 MHz)Note 1		0.8		64	μs
		Operating on main system clock (f_{XX} = 5.0 MHz)Note 2	4.5 ≤ V_{DD} ≤ 5.5 V	0.4		32	μs
			2.7 ≤ V_{DD} < 4.5 V	0.8		32	μs
		Operating on subsystem clock		40Note 3	122	125	μs
TI00 input high/low-level width	t_{TIH00}, t_{TIL00}	4.5 V ≤ V_{DD} ≤ 5.5 V		$2/f_{sam}$+0.1Note 4			μs
		2.7 V ≤ V_{DD} < 4.5 V		$2/f_{sam}$+0.2Note 4			μs
TI01 input high/low-level width	t_{TIH01}, t_{TIL01}			10			μs
TI1, TI2 input frequency	f_{TI1}	V_{DD} = 4.5 to 5.5 V		0		4	MHz
				0		275	kHz
TI1, TI2 input high/low-level width	t_{TIH1}, t_{TIL1}	V_{DD} = 4.5 to 5.5 V		100			ns
				1.8			μs
Interrupt request input high/low-level width	t_{INTH}, t_{INTL}	INTP0	4.5 V ≤ V_{DD} ≤ 5.5 V	$2/f_{sam}$+0.1Note 4			μs
			2.7 V ≤ V_{DD} < 4.5 V	$2/f_{sam}$+0.2Note 4			μs
		INTP1-INTP5, P110-P117		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

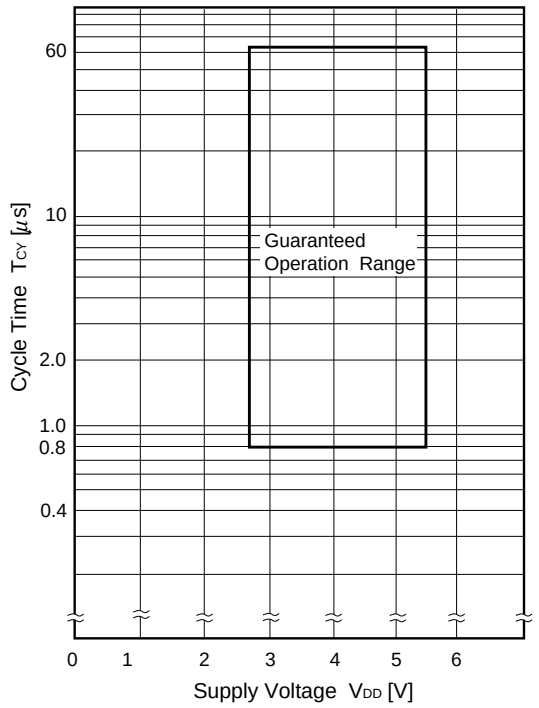
Notes 1. Main system clock $f_{XX} = f_X/2$ operation (when oscillation mode selection register (OSMS) is set to 00H)

2. Main system clock $f_{XX} = f_X$ operation (when OSMS is set to 01H)

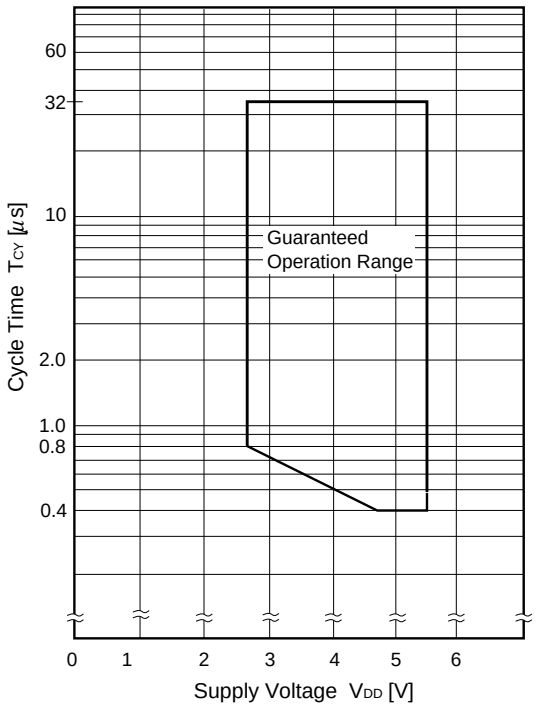
3. This is the value when the external clock is used. The value is 114 μs (min.) when the crystal resonator is used.

4. In combination with bits 0 (SCS0) and 1 (SCS1) of the sampling clock select register (SCS), selection of f_{sam} is possible between $f_{XX}/2^{N+1}$, $f_{XX}/32$, $f_{XX}/64$, and $f_{XX}/128$ (when N = 0 to 4).

T_{CY} vs V_{DD} (At main system clock $f_{XX} = f_X/2$ operation)



T_{CY} vs V_{DD} (At main system clock $f_{XX} = f_X$ operation)



(2) Serial Interface (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
$\overline{SCK0}$ high/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 4.5 to 5.5 V	t_{KCY1}/2 – 50			ns
			t_{KCY1}/2 – 100			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI1}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK0}$ and SO0 output lines.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
$\overline{SCK0}$ high/low-level width	t_{KH2}, t_{KL2}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK2}		100			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI2}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO2}	C = 100 pF[Note]			300	ns
$\overline{SCK0}$ rise, fall time	t_{R2}, t_{F2}				1000	ns

Note C is the load capacitance of the SO0 output line.

(iii) SBI mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH3},	V_{DD} = 4.5 to 5.5 V		$t_{KCY3}/2 - 50$			ns
	t_{KL3}			$t_{KCY3}/2 - 150$			ns
SB0, SB1 setup time	t_{SIK3}	V_{DD} = 4.5 to 5.5 V		100			ns
(to $\overline{SCK0}$↑)				300			ns
SB0, SB1 hold time	t_{KSI3}			$t_{KCY3}/2$			ns
(from $\overline{SCK0}$↑)							
SB0, SB1 output delay	t_{KSO3}	R = 1 kΩ,	V_{DD} = 4.5 to 5.5 V	0		250	ns
time from $\overline{SCK0}$↓		C = 100 pF[Note]		0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R and C are the load resistance and load capacitance of the $\overline{SCK0}$, SB0, and SB1 output lines.

(iv) SBI mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH4},	V_{DD} = 4.5 to 5.5 V		400			ns
	t_{KL4}			1600			ns
SB0, SB1 setup time	t_{SIK4}	V_{DD} = 4.5 to 5.5 V		100			ns
(to $\overline{SCK0}$↑)				300			ns
SB0, SB1 hold time	t_{KSI4}			$t_{KCY4}/2$			ns
(from $\overline{SCK0}$↑)							
SB0, SB1 output delay	t_{KSO4}	R = 1 kΩ,	V_{DD} = 4.5 to 5.5 V	0		300	ns
time from $\overline{SCK0}$↓		C = 100 pF[Note]		0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{SCK0}$ rising/falling time	t_{R4},					1000	ns
	t_{F4}						

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output lines.

(v) 2-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF[Note]		1600			ns
$\overline{SCK0}$ high-level width	t_{KH5}			$t_{KCY5}/2 - 160$			ns
$\overline{SCK0}$ low-level width	t_{KL5}		V_{DD} = 4.5 to 5.5 V	$t_{KCY5}/2 - 50$			ns
				$t_{KCY5}/2 - 100$			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK5}		4.5 V ≤ V_{DD} ≤ 5.5 V	300			ns
			2.7 V ≤ V_{DD} < 4.5 V	350			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI5}			600			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO5}					300	ns

Note R and C are the load resistance and load capacitance of the $\overline{SCK0}$, SB0, and SB1 output lines.

(vi) 2-wire serial I/O mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}			1600			ns
$\overline{SCK0}$ high-level width	t_{KH6}			650			ns
$\overline{SCK0}$ low-level width	t_{KL6}			800			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK6}			100			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI6}			$t_{KCY6}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO6}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	0		300	ns
				0		500	ns
$\overline{SCK0}$ rise, fall time	t_{R6}, t_{F6}					1000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output lines.

(b) Serial interface channel 2

(i) 3-wire serial I/O mode ($\overline{SCK2}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY7}	$4.5\ V \le V_{DD} \le 5.5\ V$	800			ns
		$2.7\ V \le V_{DD} < 4.5\ V$	1600			ns
$\overline{SCK2}$ high/low-level width	t_{KH7},	V_{DD} = 4.5 to 5.5 V	$t_{KCY7}/2 - 50$			ns
	t_{KL7}		$t_{KCY7}/2 - 100$			ns
SI2 setup time (to $\overline{SCK2}\uparrow$)	t_{SIK7}	$4.5\ V \le V_{DD} \le 5.5\ V$	100			ns
		$2.7\ V \le V_{DD} < 4.5\ V$	150			ns
SI2 hold time (from $\overline{SCK2}\uparrow$)	t_{KSI7}		400			ns
SO2 output delay time from $\overline{SCK2}\downarrow$	t_{KSO7}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK2}$ and SO2 output lines.

(ii) 3-wire serial I/O mode ($\overline{SCK2}$... External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY8}	$4.5\ V \le V_{DD} \le 5.5\ V$	800			ns
		$2.7\ V \le V_{DD} < 4.5\ V$	1600			ns
$\overline{SCK2}$ high/low-level width	t_{KH8},	$4.5\ V \le V_{DD} \le 5.5\ V$	400			ns
	t_{KL8}	$2.7\ V \le V_{DD} < 4.5\ V$	800			ns
SI2 setup time (to $\overline{SCK2}\uparrow$)	t_{SIK8}		100			ns
SI2 hold time (from $\overline{SCK2}\uparrow$)	t_{KSI8}		400			ns
SO2 output delay time from $\overline{SCK2}\downarrow$	t_{KSO8}	C = 100 pF[Note]			300	ns
$\overline{SCK2}$ rise, fall time	t_{R8}, t_{F8}				1000	ns

Note C is the load capacitance of the SO2 output line.

(iii) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.5 V ≤ V_{DD} ≤ 5.5 V			78125	bps
		2.7 V ≤ V_{DD} < 4.5 V			39063	bps

(iv) UART mode (External clock input)

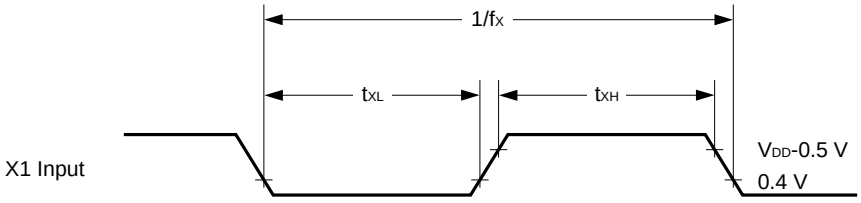
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY9}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
ASCK high/low-level width	t_{KH9}, t_{KL9}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
Transfer rate		4.5 V ≤ V_{DD} ≤ 5.5 V			39063	bps
		2.7 V ≤ V_{DD} < 4.5 V			19531	bps
ASCK rise, fall time	t_{R9}, t_{F9}				1000	ns

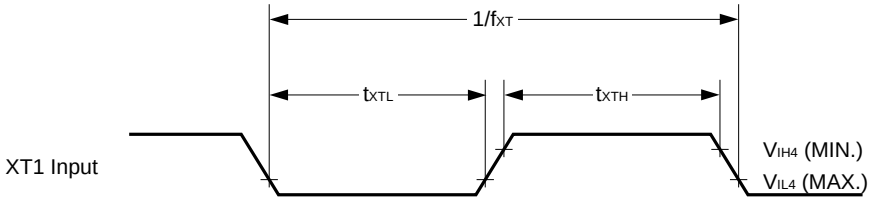
(c) Serial interface channel 3

Undecided

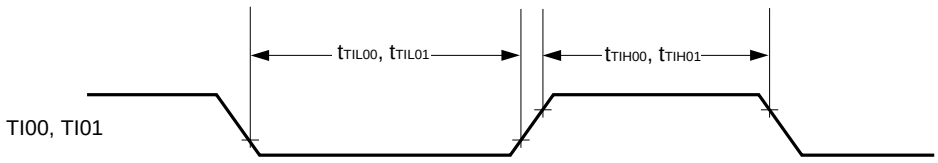
AC Timing Test Point (Excluding X1, XT1 Inputs)

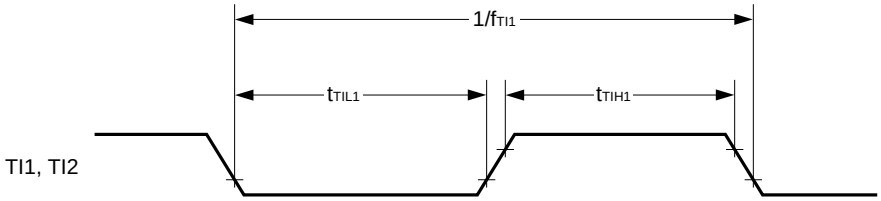
Clock Timing





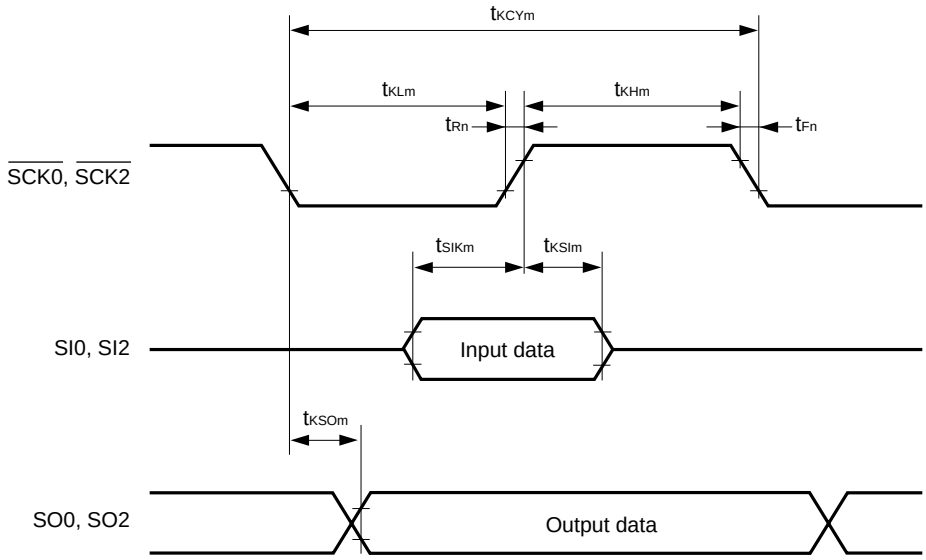
TI Timing





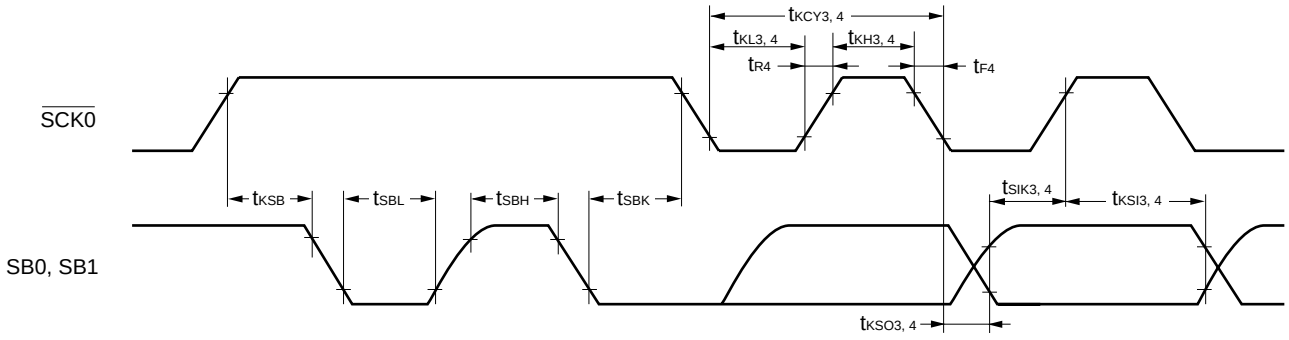
Serial Transfer Timing

3-wire serial I/O mode:

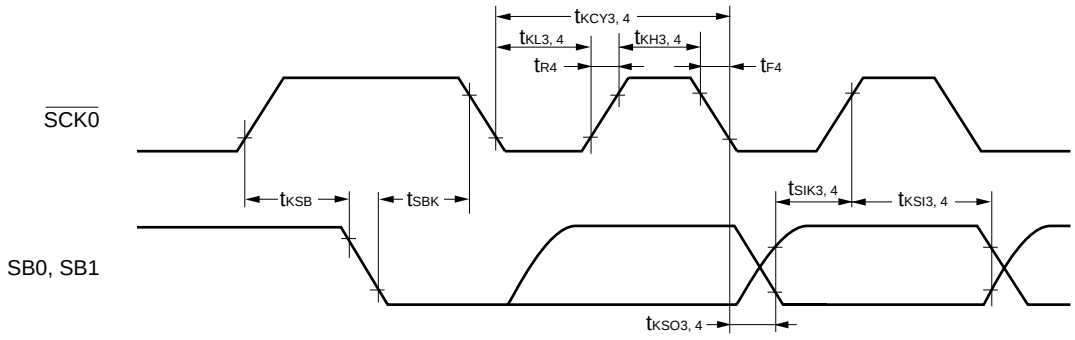


m = 1, 2, 7, 8
n = 2, 8

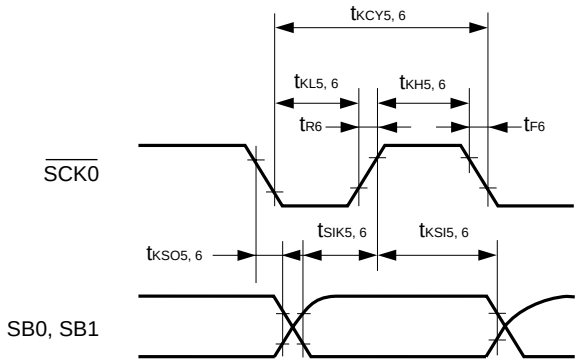
SBI mode (bus release signal transfer):



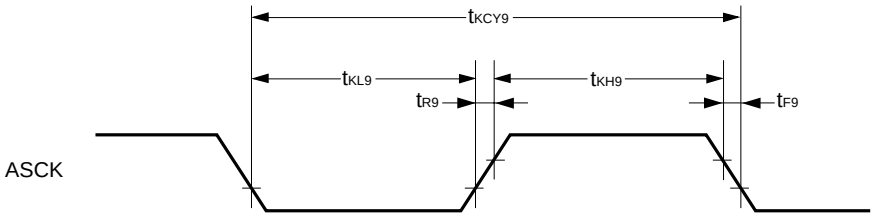
SBI mode (command signal transfer):



2-wire serial I/O mode:



UART mode:



A/D Converter (T_A = –40 to +85°C, AV_{DD} = V_{DD} = AV_{REF} = 4.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note 1]					±0.6	%
Conversion time	t_{CONV}		19.1		200	μs
Sampling time	t_{SAMP}		12/f_{XX}			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		4.0		AV_{DD}	V
AV_{REF}-AV_{SS} resistance	R_{REF}	When not operating A/D conversion	4	14		kΩ
AV_{REF} current	AI_{REF}	When operating A/D conversion[Note 2]		2.0	4.0	mA
		When not operating A/D conversion[Note 3]		0.5	1.5	mA

Notes 1. Quantization error (±1/2 LSB) is not included. This is expressed in proportion to the full-scale value.

2. Indicates current flowing to AV_{REF} pin when the CS bit of the A/D converter mode register (ADM) is 1.

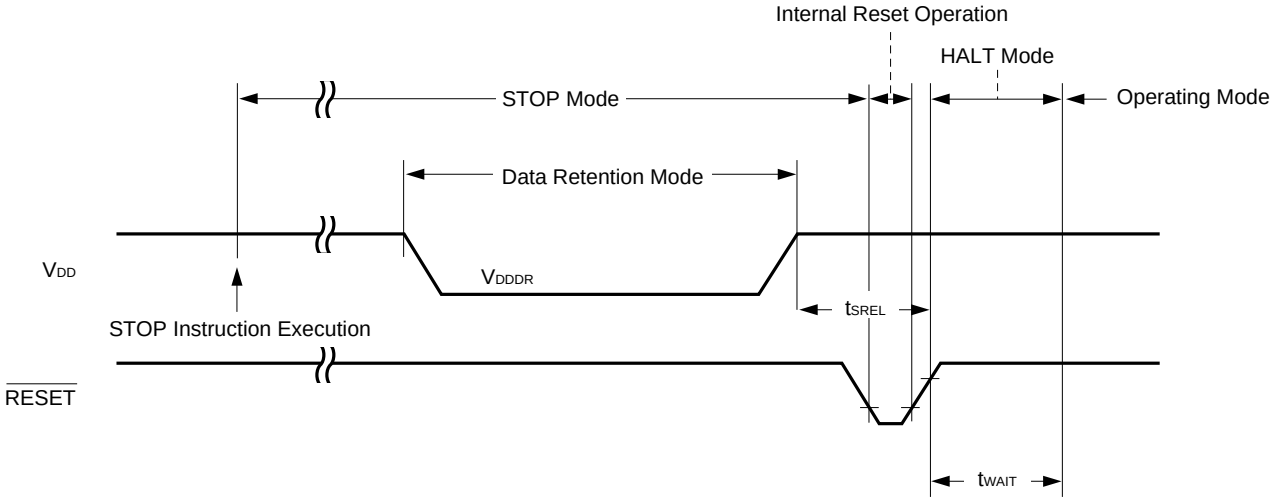
3. Indicates current flowing to AV_{REF} pin when the CS bit of ADM is 0.

DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (T_A = –40 to +85°C)

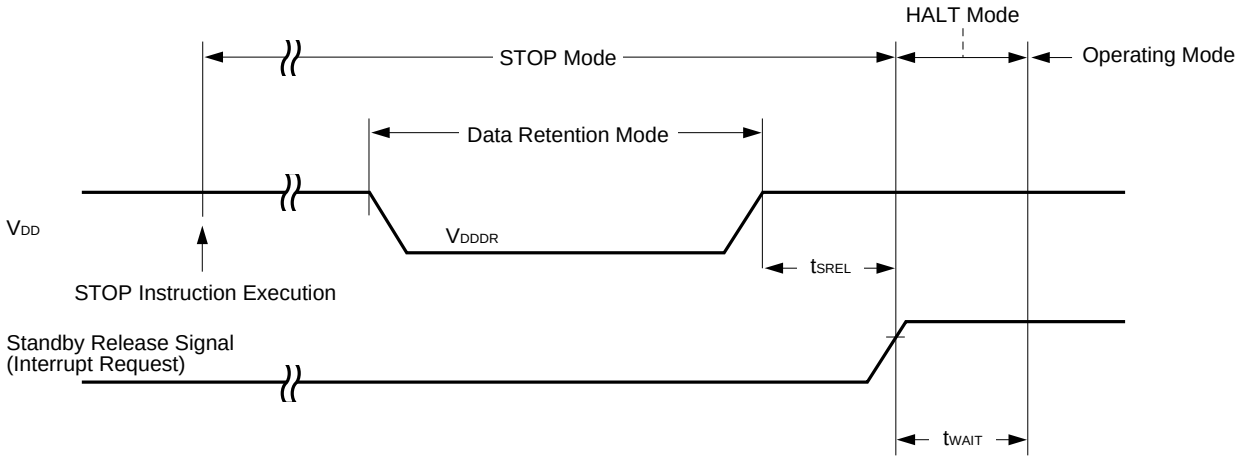
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Data retention power supply current	I_{DDDR}	VDDDR = 1.8 V Subsystem clock stop and feed-back resistor disconnected.		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		2^{17}/fx		ms
		Release by interrupt request		**Note**		ms

Note In combination with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS), selection of 2^{12}/fxx and 2^{14}/fxx to 2^{17}/fxx is possible.

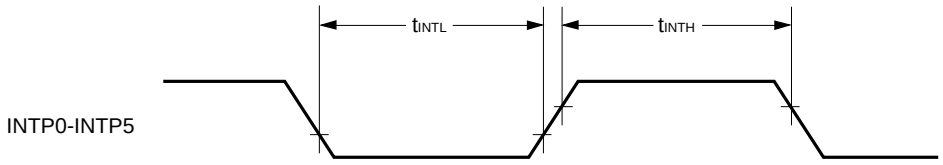
Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



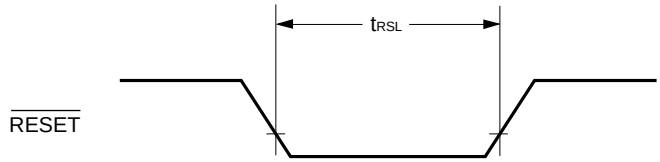
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



Interrupt Request Input Timing



$\overline{\text{RESET}}$ Input Timing



PROM PROGRAMMING CHARACTERISTICS

DC Characteristics

(1) PROM Write Mode (T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol Note	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH}	V_{IH}		0.7V_{DD}		V_{DD}	V
Input voltage low	V_{IL}	V_{IL}		0		0.3V_{DD}	V
Output voltage high	V_{OH}	V_{OH}	I_{OH} = –1 mA	V_{DD} – 1.0			V
Output voltage low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	0 ≤ V_{IN} ≤ V_{DD}	–10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		12.2	12.5	12.8	V
V_{DD} supply voltage	V_{DD}	V_{CC}		6.25	6.5	6.75	V
V_{PP} supply current	I_{PP}	I_{PP}	$\overline{PGM}$ = V_{IL}			50	mA
V_{DD} supply current	I_{DD}	I_{CC}				50	mA

(2) PROM Read Mode (T_A = 25 ±5°C, V_{DD} = 5.0 ±0.5 V, V_{PP} = V_{DD} ±0.6 V)

Parameter	Symbol	Symbol Note	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH}	V_{IH}		0.7V_{DD}		V_{DD}	V
Input voltage low	V_{IL}	V_{IL}		0		0.3V_{DD}	V
Output voltage high	V_{OH1}	V_{OH1}	I_{OH} = –1 mA	V_{DD} – 1.0			V
	V_{OH2}	V_{OH2}	I_{OH} = –100 μA	V_{DD} – 0.5			V
Output voltage low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	0 ≤ V_{IN} ≤ V_{DD}	–10		+10	μA
Output leakage current	I_{LO}	I_{LO}	0 ≤ V_{OUT} ≤ V_{DD}, $\overline{OE}$ = V_{IH}	–10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		V_{DD} – 0.6	V_{DD}	V_{DD} + 0.6	V
V_{DD} supply voltage	V_{DD}	V_{CC}		4.5	5.0	5.5	V
V_{PP} supply current	I_{PP}	I_{PP}	V_{PP} = V_{DD}			100	μA
V_{DD} supply current	I_{DD}	I_{CCA1}	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH}			50	mA

Note Corresponding μPD27C1001A symbol.

AC Characteristics

(1) PROM Write Mode

(a) Page program mode (T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol Note	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{OE}\downarrow$)	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ setup time	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (to $\overline{OE}\downarrow$)	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{OE}\downarrow$)	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}\uparrow$)	t_{AH}	t_{AH}		2			μs
	t_{AHL}	t_{AHL}		2			μs
	t_{AHV}	t_{AHV}		0			μs
Input data hold time (from $\overline{OE}\uparrow$)	t_{DH}	t_{DH}		2			μs
Data output float delay time from $\overline{OE}\uparrow$	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{OE}\downarrow$)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{OE}\downarrow$)	t_{VDS}	t_{VCS}		1.0		250	ms
Program pulse width	t_{PW}	t_{PW}		0.095		0.105	ms
Valid data delay time from $\overline{OE}\downarrow$	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ pulse width during data latching	t_{LW}	t_{LW}		1			μs
$\overline{PGM}$ setup time	t_{PGMS}	t_{PGMS}		2			μs
$\overline{CE}$ hold time	t_{CEH}	t_{CEH}		2			μs
$\overline{OE}$ hold time	t_{OEH}	t_{OEH}		2			μs

(b) Byte program mode (T_A = 25 ±5°C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol Note	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{PGM}\downarrow$)	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ setup time	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (to $\overline{PGM}\downarrow$)	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{PGM}\downarrow$)	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}\uparrow$)	t_{AH}	t_{AH}		2			μs
Input data hold time (from $\overline{PGM}\uparrow$)	t_{DH}	t_{DH}		2			μs
Data output float delay time from $\overline{OE}\uparrow$	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{PGM}\downarrow$)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{PGM}\downarrow$)	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	t_{PW}	t_{PW}		0.095		0.105	ms
Valid data delay time from $\overline{OE}\downarrow$	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ hold time	t_{OEH}	—		2			μs

Note Corresponding μPD27C1001A symbol

(2) PROM Read Mode (T_A = 25 ±5°C, V_{DD} = 5.0 ±0.5 V, V_{PP} = V_{DD} ±0.6 V)

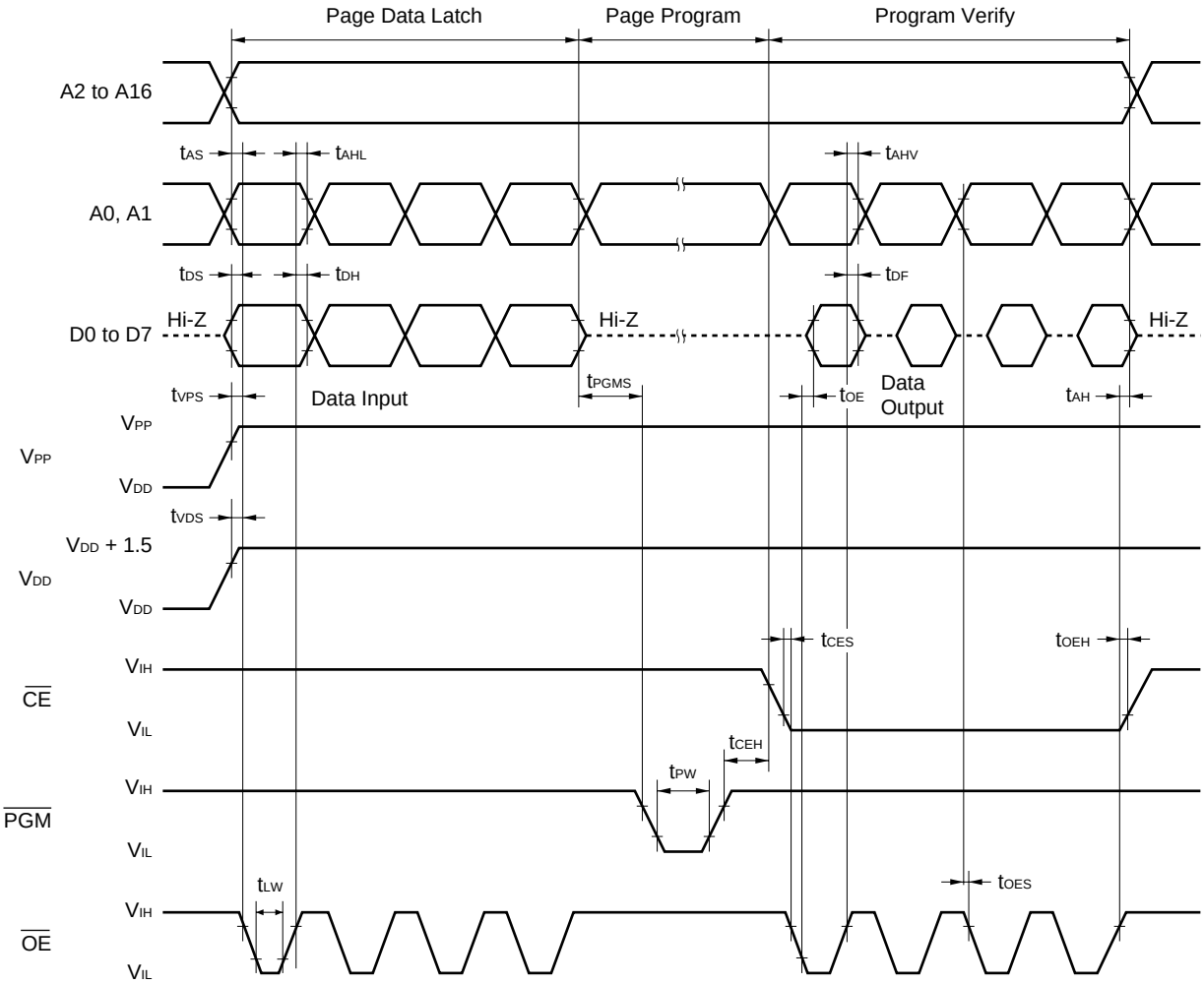
Parameter	Symbol	Symbol Note	Test Conditions	MIN.	TYP.	MAX.	Unit
Data output delay time from address	t_{ACC}	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			800	ns
Data output delay time from $\overline{CE}$↓	t_{CE}	t_{CE}	$\overline{OE}$ = V_{IL}			800	ns
Data output delay time from $\overline{OE}$↓	t_{OE}	t_{OE}	$\overline{CE}$ = V_{IL}			200	ns
Data output float delay time from $\overline{OE}$↑	t_{DF}	t_{DF}	$\overline{CE}$ = V_{IL}	0		60	ns
Data hold time from address	t_{OH}	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0			ns

Note Corresponding μPD27C1001A symbol

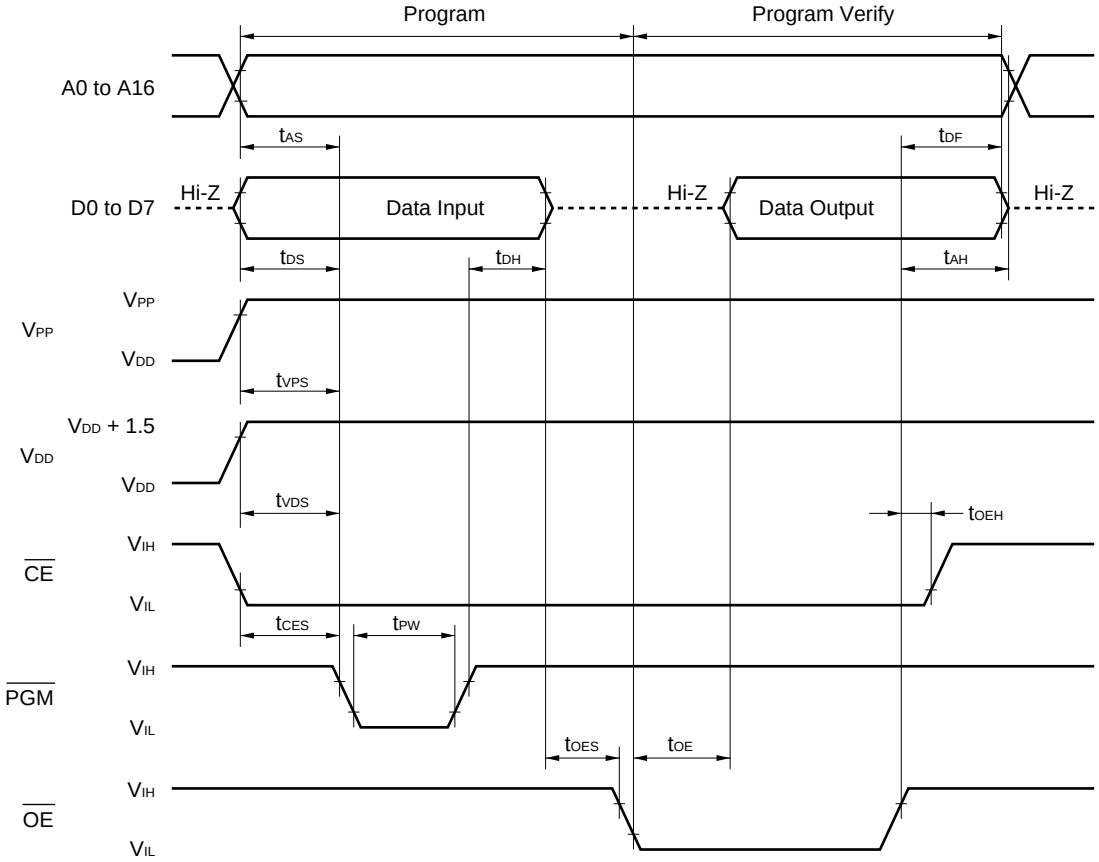
(3) PROM Programming Mode Setting (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
PROM programing mode setup time	t_{SMA}		10			μs

PROM Write Mode Timing (Page Program Mode)



PROM Write Mode Timing (Byte Program Mode)

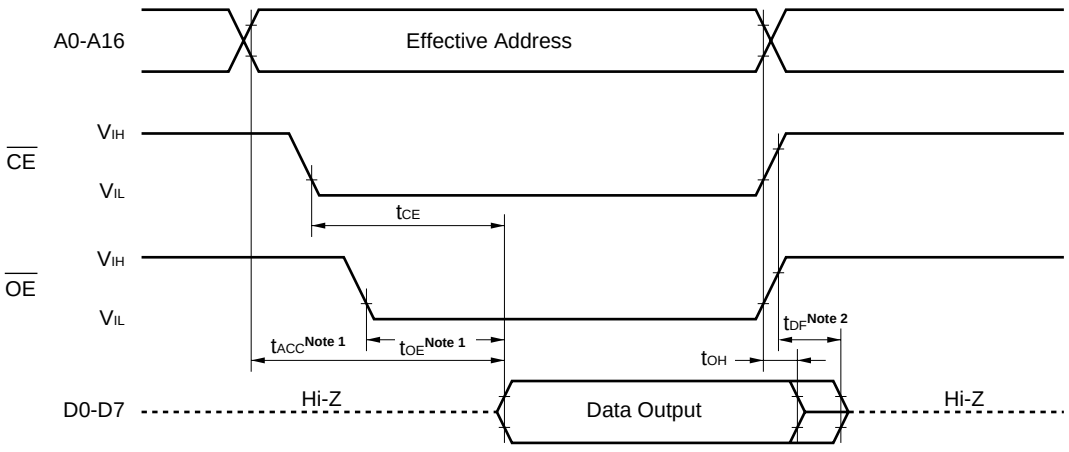


Cautions 1. V_{DD} should be applied before V_{PP}, and cut after V_{PP}.

2. V_{PP} should not exceed +13.5 V including overshoot.

3. Disconnection during application of ±12.5 V to V_{PP} may have an adverse effect on reliability.

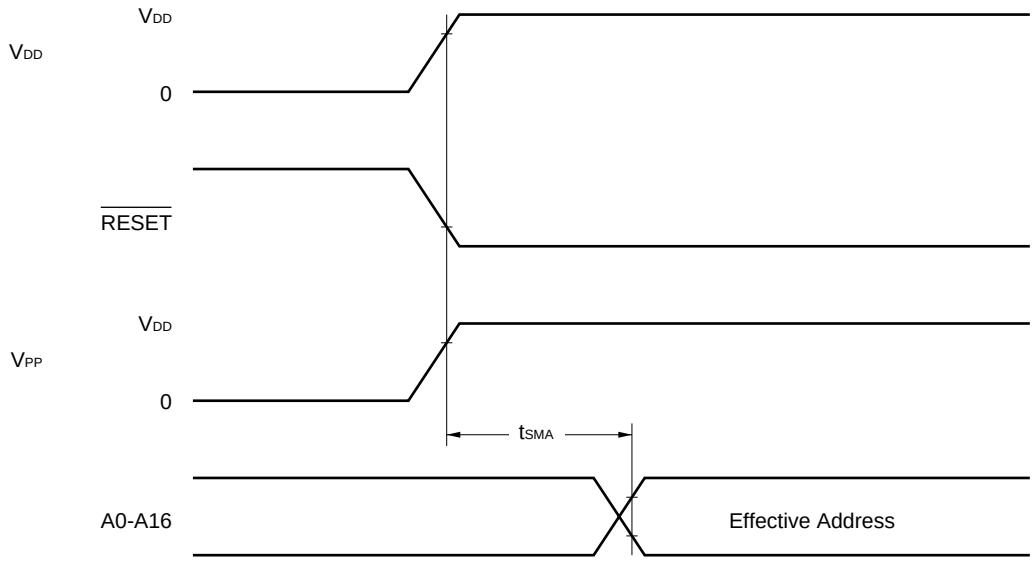
PROM Read Mode Timing



Notes 1. If you want to read within the t_{ACC} range, make the $\overline{OE}$ input delay time from the fall of $\overline{CE}$ the maximum of $t_{ACC} - t_{OE}$.

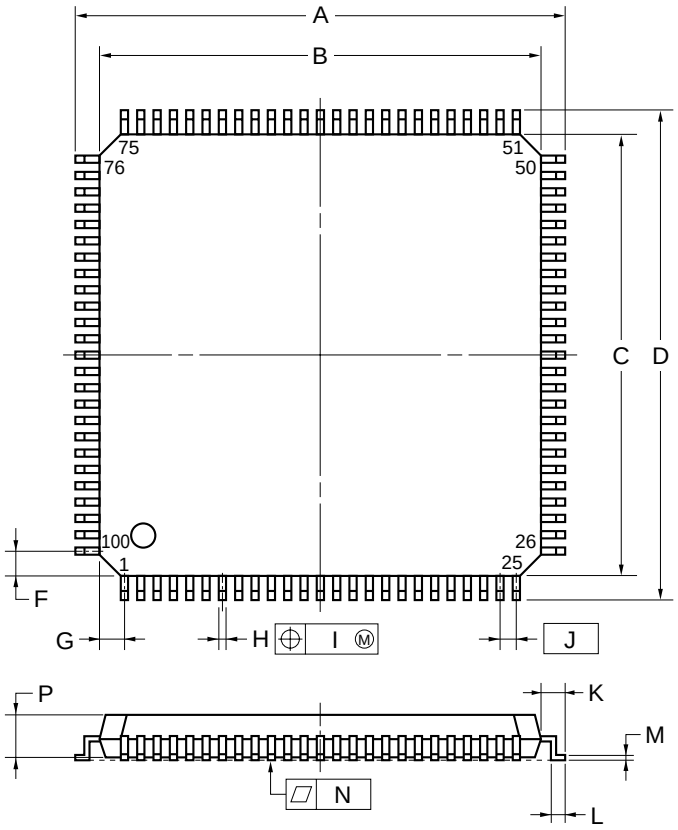
2. t_{DF} is the time from when either $\overline{OE}$ or $\overline{CE}$ first reaches V_{IH}.

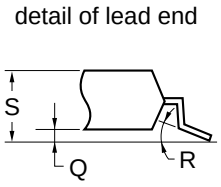
PROM Programming Mode Setting Timing



10. PACKAGE DRAWINGS

★ 100 PIN PLASTIC LQFP (FINE PITCH) (14×14)





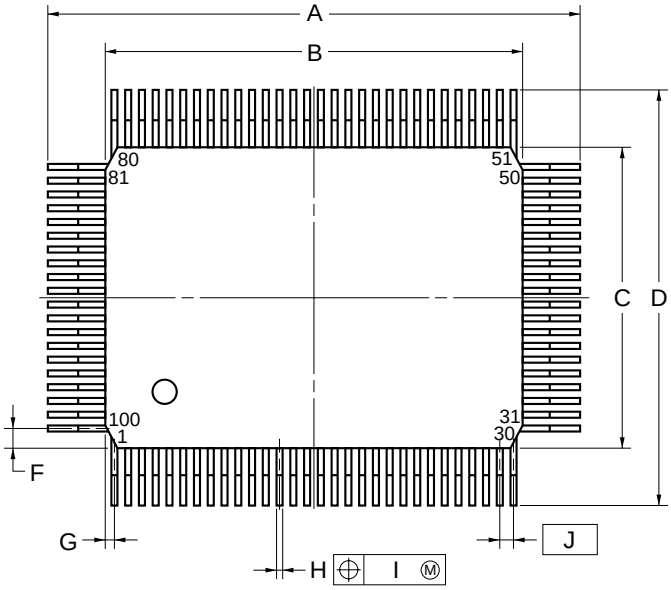
NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

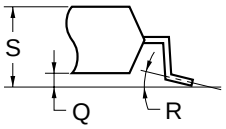
ITEM	MILLIMETERS	INCHES
A	16.00±0.20	0.630±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	16.00±0.20	0.630±0.008
F	1.00	0.039
G	1.00	0.039
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.08	0.003
J	0.50 (T.P.)	0.020 (T.P.)
K	1.00±0.20	$0.039^{+0.009}_{-0.008}$
L	0.50±0.20	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.08	0.003
P	1.40±0.05	0.055±0.002
Q	0.10±0.05	0.004±0.002
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.60 MAX.	0.063 MAX.

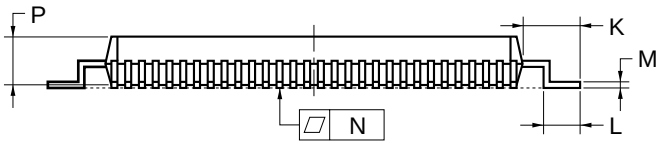
S100GC-50-8EU

100PIN PLASTIC QFP (14x20)



detail of lead end





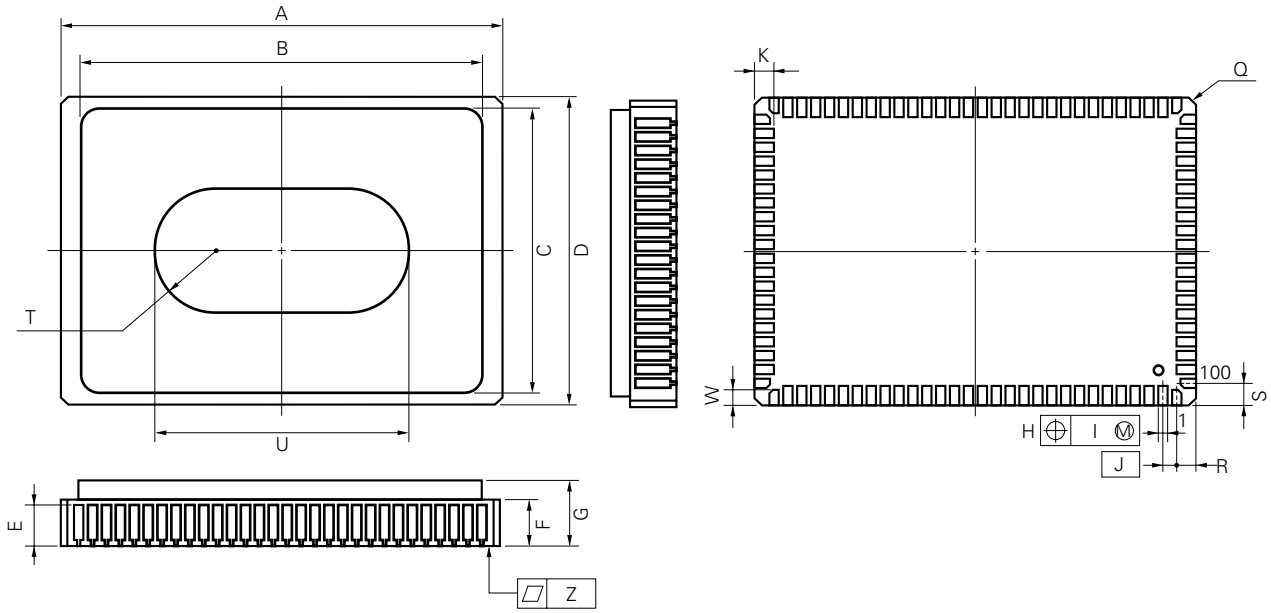
NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7±0.1	$0.106^{+0.005}_{-0.004}$
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P100GF-65-3BA1-3

100 PIN CERAMIC WQFN



NOTE

Each lead centerline is located within 0.06 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

X100KW-65A-1

ITEM	MILLIMETERS	INCHES
A	20.6−0.4	0.811−0.016
B	19.0	0.748
C	13.8	0.543
D	14.6−0.4	0.575−0.016
E	1.94	0.076
F	2.14	0.084
G	3.5 MAX,	0.138 MAX.
H	0.45−0.10	$0.018^{+0.004}_{-0.005}$
I	0.06	0.003
J	0.65	0.026
K	1.0−0.2	$0.039^{+0.009}_{-0.008}$
Q	C 0.3	C 0.012
R	0.875	0.034
S	1.125	0.044
T	R 3.17	R 0.125
U	12.0	0.472
W	0.75−0.2	$0.030^{+0.008}_{-0.009}$
Z	0.10	0.004

★ APPENDIX A. DEVELOPMENT TOOLS

The following development tools are provided for system development using the μPD78P0308.

Also refer to **(5) Precautions in Using Development Tools**.

(1) Language Processing Software

RA78K/0	Assembler package common to 78K/0 Series products
CC78K/0	C compiler package common to 78K/0 Series products
DF780308	Device file common to μPD780308 Subseries products (part number: μSxxxxDF78064)
CC78K/0–L	C compiler library source file common to 78K/0 Series products

(2) PROM Write Tools

PG-1500	PROM programmer
PA-78P0308GC PA-78P0308GF PA-78P0308KL-T	Programmer adapter connected to the PG-1500
PG-1500 Controller	Control program for the PG-1500

(3) Debugging Tools

- **When using the IE-78K0-NS as an in-circuit emulator**

IE-78K0-NS[Note]	In-circuit emulator common to 78K/0 Series products
IE-70000-MC-PS-B	Power supply unit for the IE-78K0-NS
IE-70000-98-IF-C[Note]	Interface adapter when a PC-9800 series PC (excluding notebook-type PCs) is used as the host machine
IE-70000-CD-IF[Note]	PC card and interface cable when a PC-9800 series notebook-type PC is used as the host machine
IE-70000-PC-IF-C[Note]	Interface adapter when an IBM PC/AT™ or its compatible is used as the host machine
IE-780308-NS-EM1[Note]	Emulation board common to μPD780308 Subseries products
NP-100GC	Emulation probe for 100-pin plastic LQFP (GC-8EU type)
NP-100GF	Emulation probe for 100-pin plastic QFP (GF-3BA type)
TGC-100SDW	Conversion adapter to connect the NP-100GC with the target system board prepared for mounting a 100-pin plastic LQFP (GC-8EU type)
EV-9200GF-100	Socket to be mounted on the target system board prepared for 100-pin plastic QFP (GF-3BA type)
ID78K0-NS[Note]	Integrated debugger for the IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series products
DF780308	Device file common to μPD780308 Subseries products (part number: μSxxxxDF78064)

Note Under development

- **When using the IE-78001-R-A as an in-circuit emulator**

IE-78001-R-A[Note]	In-circuit emulator common to 78K/0 Series products
IE-70000-98-IF-B IE-70000-98-IF-C[Note]	Interface adapter when a PC-9800 series PC (excluding notebook-type PCs) is used as the host machine
IE-70000-PC-IF-B IE-70000-PC-IF-C[Note]	Interface adapter when an IBM PC/AT™ or its compatible is used as the host machine
IE-78000-R-SV3	Interface adapter and cable when an EWS is used as the host machine
IE-780308-NS-EM1[Note] IE-780308-R-EM	Emulation board common to μPD780308 Subseries products
IE-78K0-R-EX1[Note]	Emulation probe conversion board required when the IE-780308-NS-EM1 is used in the IE-78001-R-A
EP-78064GC-R	Emulation probe for 100-pin plastic LQFP (GC-8EU type)
EP-78064GF-R	Emulation probe for 100-pin plastic QFP (GF-3BA type)
TGC-100SDW	Conversion adapter to connect the EP-78064GC-R with the target system board prepared for mounting a 100-pin plastic LQFP (GC-8EU type)
EV-9200GF-100	Socket to be mounted on the target system board prepared for 100-pin plastic QFP (GF-3BA type)
ID78K0	Integrated debugger for the IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series products
DF780308	Device file common to μPD780308 Subseries products (part number: μSxxxxDF78064)

Note Under development

(4) Real-Time OS

RX78K/0	Real-time OS for 78K/0 Series products
MX78K0	OS for 78K/0 Series products

(5) Precautions in Using Development Tools

- The package name of the DF780308 is DF78064.
- Use the ID78K0-NS, ID78K0, and SM78K0 in combination with the DF780308.
- Use the CC78K/0 and RX78K/0 in combination with the RA78K/0 and DF780308.
- The NP-100GC and NP-100GF are products of Naitou Densei Machidaseisakusho Co., Ltd. (tel: (044) 822-3813). Contact an NEC dealer to purchase these products.
- The TGC-100SDW is a product of TOKYO ELETECH Corporation.

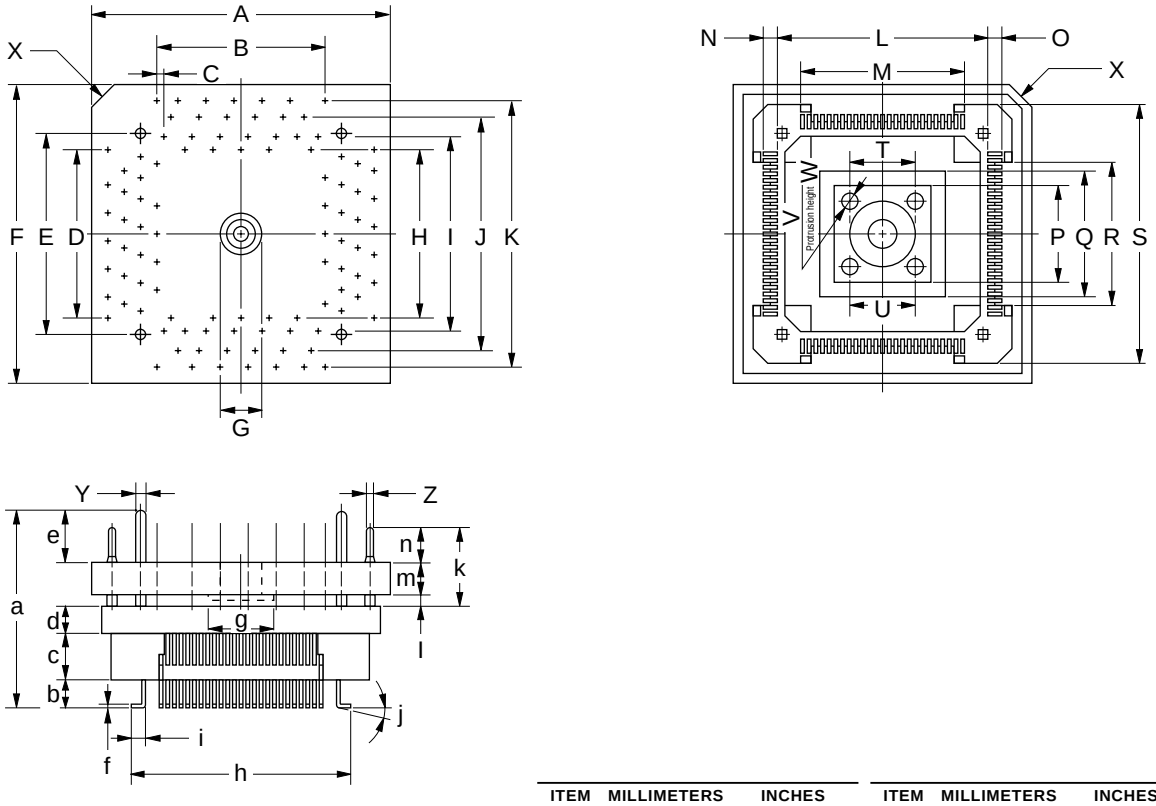
  Contact: Daimaru Kogyo Co., Ltd. Tokyo Electronic Component Department (tel: (03) 3820-7112)
  Osaka Electronic Component Department (tel: (06) 244-6672)
- Please refer to **78K/0 Series Selection Guide (U11126E)** for information on the third party development tools.
- The following table shows what host machine and OS support each software.

Host machine / [OS] / Software	PC	EWS
	PC-9800 series [Windows™] IBM PC/AT and its compatibles [Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™] NEWS™ (RISC) [NEWS-OS™]
RA78K/0	√Note	√
CC78K/0	√Note	√
PG-1500 controller	√Note	—
ID78K0-NS	√	—
ID78K0	√	√
SM78K0	√	—
RX78K/0	√Note	√
MX78K0	√Note	√

Note DOS-based software.

DRAWING OF CONVERSION ADAPTER (TGC-100SDW)

Figure A-1. Drawing of TGC-100SDW (for reference only) (unit: mm)



ITEM	MILLIMETERS	INCHES
A	21.55	0.848
B	0.5x24=12	0.020x0.945=0.472
C	0.5	0.020
D	0.5x24=12	0.020x0.945=0.472
E	15.0	0.591
F	21.55	0.848
G	ϕ3.55	ϕ0.140
H	10.9	0.429
I	13.3	0.524
J	15.7	0.618
K	18.1	0.713
L	13.75	0.541
M	0.5x24=12.0	0.020x0.945=0.472
N	1.125±0.3	0.044±0.012
O	1.125±0.2	0.044±0.008
P	7.5	0.295
Q	10.0	0.394
R	11.3	0.445
S	18.1	0.713
T	ϕ5.0	ϕ0.197
U	5.0	0.197
V	4-ϕ1.3	4-ϕ0.051
W	1.8	0.071
X	C 2.0	C 0.079
Y	ϕ0.9	ϕ0.035
Z	ϕ0.3	ϕ0.012

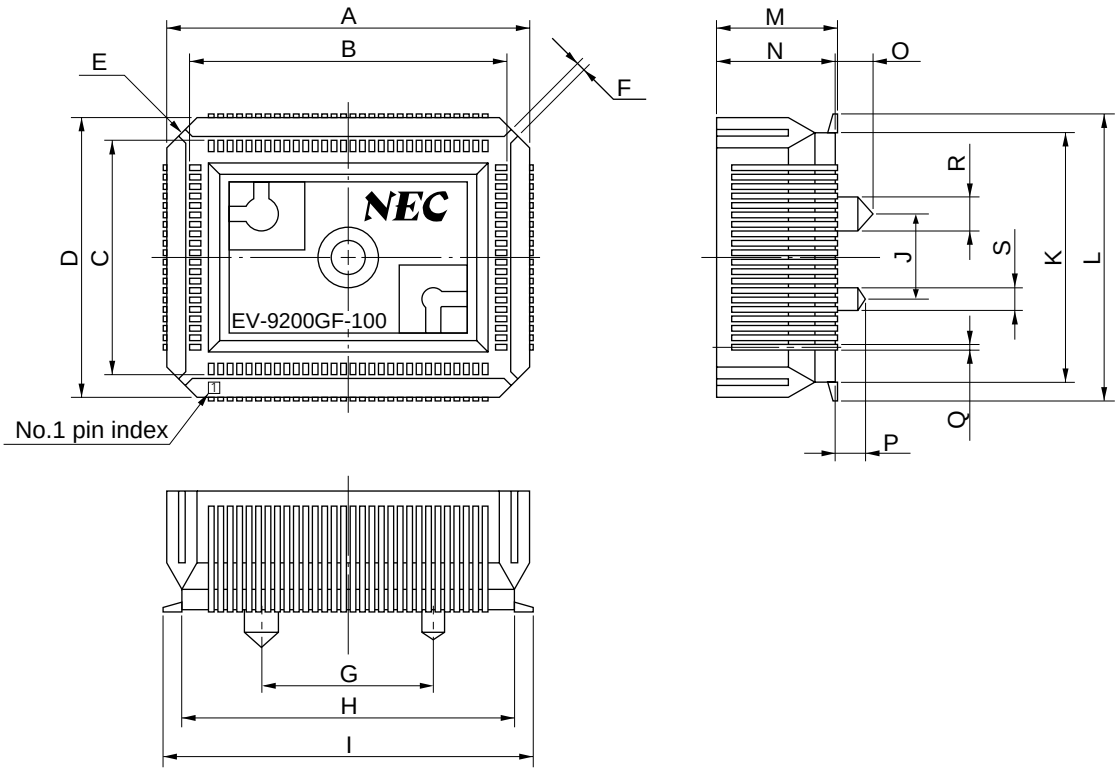
ITEM	MILLIMETERS	INCHES
a	14.45	0.569
b	1.85±0.25	0.073±0.010
c	3.5	0.138
d	2.0	0.079
e	3.9	0.154
f	0.25	0.010
g	ϕ4.5	ϕ0.177
h	16.0	0.630
i	1.125±0.3	0.044±0.012
j	0~5°	0.000~0.197°
k	5.9	0.232
l	0.8	0.031
m	2.4	0.094
n	2.7	0.106

TGC-100SDW-G1E

note: Product of TOKYO ELETECH CORPORATION.

DRAWINGS OF CONVERSION SOCKET (EV-9200GF-100) AND RECOMMENDED FOOTPRINTS

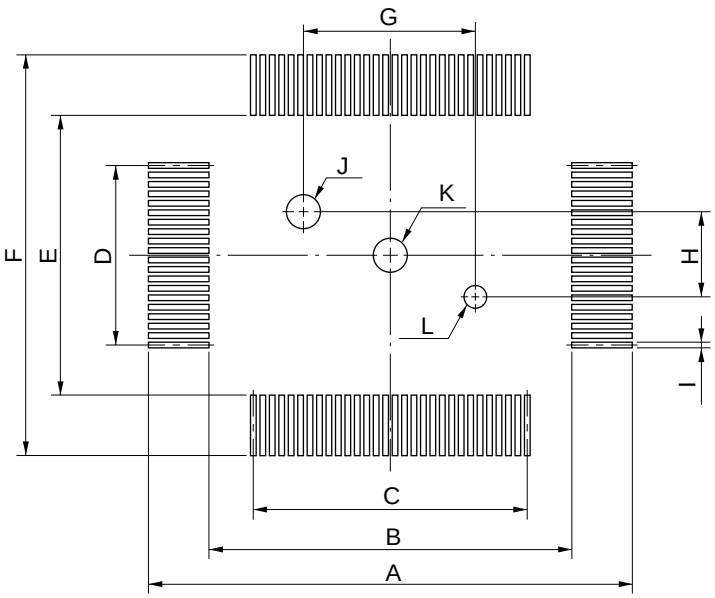
Figure A-2. Drawing of EV-9200GF-100 (for reference only)



EV-9200GF-100-G0E

ITEM	MILLIMETERS	INCHES
A	24.6	0.969
B	21	0.827
C	15	0.591
D	18.6	0.732
E	4-C 2	4-C 0.079
F	0.8	0.031
G	12.0	0.472
H	22.6	0.89
I	25.3	0.996
J	6.0	0.236
K	16.6	0.654
L	19.3	0.76
M	8.2	0.323
N	8.0	0.315
O	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	φ2.3	φ0.091
S	φ1.5	φ0.059

Figure A-3. Recommended Footprints of EV-9200GF-100 (for reference only)



EV-9200GF-100-P1E

ITEM	MILLIMETERS	INCHES
A	26.3	1.035
B	21.6	0.85
C	0.65±0.02 × 29=18.85±0.05	$0.026^{+0.001}_{-0.002} \times 1.142 = 0.742^{+0.002}_{-0.002}$
D	0.65±0.02 × 19=12.35±0.05	$0.026^{+0.001}_{-0.002} \times 0.748 = 0.486^{+0.003}_{-0.002}$
E	15.6	0.614
F	20.3	0.799
G	12±0.05	$0.472^{+0.003}_{-0.002}$
H	6±0.05	$0.236^{+0.003}_{-0.002}$
I	0.35±0.02	$0.014^{+0.001}_{-0.001}$
J	φ2.36±0.03	$\phi 0.093^{+0.001}_{-0.002}$
K	φ2.3	φ0.091
L	φ1.57±0.03	$\phi 0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

★ APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document Number	
	English	Japanese
μPD780308, 780308Y Subseries User's Manual	U11377E	U11377J
μPD780306, 780308 Data Sheet	U11105E	U11105J
μPD78P0308 Data Sheet	This document	U11776J
78K/0 Series User's Manual Instructions	U12326E	U12326J
78K/0 Series Instruction Application Table	—	U10903J
78K/0 Series Instruction Set	—	U10904J
μPD780308 Subseries Special Function Register Table	—	To be prepared
78K/0 Series Application Note — Basics III	U10182E	U10182J

Documents Related to Development Tools (User's Manual)

Document Name		Document Number	
		English	Japanese
RA78K0 Assembler Package	Operation	U11802E	U11802J
	Assembly Language	U11801E	U11801J
	Structured Assembly Language	U11789E	U11789J
RA78K Series Structured Assembler Preprocessor		EEU-1402	U12323J
CC78K0 C Compiler	Operation	U11517E	U11517J
	Language	U11518E	U11518J
CC78K0 C Compiler Application Note	Programming Know-how	EEA-1208	EEA-618
CC78K Series Library Source File		—	U12322J
PG-1500 PROM Programmer		U11940E	U11940J
PG-1500 Controller PC-9800 series (MS-DOS™) based		EEU-1291	EEU-704
PG-1500 Controller IBM PC series (PC DOS™) based		U10540E	EEU-5008
IE-78K0-NS		To be prepared	To be prepared
IE-78001-R-A		To be prepared	To be prepared
IE-78K0-R-EX1		To be prepared	To be prepared
IE-780308-NS-EM1		To be prepared	To be prepared
IE-780308-R-EM		U11362E	U11362J
EP-78064		EEU-1469	EEU-934
SM78K0 System Simulator Windows based	Reference	U10181E	U10181J
SM78K Series System Simulator	External Parts User's Open Interface Specifications	U10092E	U10092J
ID78K0-NS Integrated Debugger	Reference	To be prepared	U12900J
ID78K0 Integrated Debugger EWS-based	Reference	—	U11151J
ID78K0 Integrated Debugger PC-based	Reference	U11539E	U11539J
ID78K0 Integrated Debugger Windows-based	Guide	U11649E	U11649J

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Documents Related to Embedded Software (User's Manuals)

Document Name		Document Number	
		English	Japanese
78K/0 Series Real-Time OS	Basics	U11537E	U11537J
	Installation	U11536E	U11536J
78K/0 Series OS MX78K0	Basics	U12257E	U12257J

Others

Document Name	Document No.	
	English	Japanese
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E	C11892J
Guide to Quality Assurance for Semiconductor Devices	MEI-1202	—
Microcomputer Product Series Guide	—	U11416J

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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