DATA SHEET

NEC

MOS INTEGRATED CIRCUIT
µPD78P018FY

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The µPD78P018FY is a member of the µPD78018FY Subseries of 78K/0 Series products. The internal mask ROM of the µPD78018FY is replaced with one-time PROM or EPROM.

Because the µPD78P018FY can be programmed by users, it is ideally suited for applications involving the evaluation of systems in development stages, small-scale production of many different products, and rapid development and time-to-market of new products.

Caution   The µPD78P018FYDW and 78P018FYKK-S are not guaranteed to maintain the reliability level required for mass production of the customer's devices. Please use only experimentally or for evaluation purposes during trial manufacture.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.
µPD78018F, 78018FY Subseries User's Manual: U10659E
78K/0 Series User's Manual – Instructions: U12326E

FEATURES

- Pin compatible with mask ROM version (except V_{PP} pin)
- Internal PROM: 60 Kbytes **Note 1**
  µPD78P018FYDW, 78P018FYKK-S: Re-programmable (suited for system evaluation)
  µPD78P018FYCW, 78P018FYGC-AB8: Programmable only once (suited for small-scale production)
- Internal high-speed RAM: 1024 bytes **Note 1**
- Internal expansion RAM: 1024 bytes **Note 2**
- Internal buffer RAM: 32 bytes
- Supports the I^2C bus interface
- Operable over same supply voltage range as mask ROM version: V_{DD} = 1.8 to 5.5 V (except an A/D converter)
- QTOP™ microcontroller supported

Notes 1. The capacities of internal PROM and internal high-speed RAM can be changed by means of the internal memory size switching register (IMS).
2. The capacity of the internal expansion RAM can be changed by means of the internal expansion RAM size switching register (IXS).

Remarks 1. QTOP Microcontroller is a general term for microcontrollers which incorporate one-time PROM and are totally supported by NEC's programming service (from programming to marking, screening, and verification).
2. For the differences between the PROM version and mask ROM versions, refer to **1. DIFFERENCES BETWEEN THE µPD78P018FY AND MASK ROM VERSIONS**.

In this document, the term PROM is used in parts common to one-time PROM versions and EPROM versions.
The information in this document is subject to change without notice.

The mark ★ shows major revised points.

ORDERING INFORMATION

Part Number	Package	Internal ROM
μPD78P018FYCW	64-pin plastic shrink DIP (750 mils)	One-time PROM
μPD78P018FYDW	64-pin ceramic shrink DIP (with window) (750 mils)	EPROM
μPD78P018FYGC-AB8	64-pin plastic QFP (14 × 14 mm)	One-time PROM
μPD78P018FYKK-S	64-pin ceramic WQFN (14 × 14 mm)	EPROM

QUALITY GRADE

Part Number	Package	Quality Grades
μPD78P018FYCW	64-pin plastic shrink DIP (750 mils)	Standard
μPD78P018FYDW	64-pin ceramic shrink DIP (with window) (750 mils)	Not applicable (for function evaluation)
μPD78P018FYGC-AB8	64-pin plastic QFP (14 × 14 mm)	Standard
μPD78P018FYKK-S	64-pin ceramic WQFN (14 × 14 mm)	Not applicable (for function evaluation)

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

★   **78K/0 SERIES PRODUCT LINEUP**

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.

Products in mass production
Products under development
Y subseries products are compatible with I2C bus.

78K/0 Series

Control

Pin	Product	Y version	Description
100-pin	μPD78075B		EMI-noise reduced version of the μPD78078
100-pin	μPD78078	μPD78078Y	Timer was added to the μPD78054 and external interface was enhanced
100-pin	μPD78070A	μPD78070AY	ROM-less version of the μPD78078
100-pin		μPD780018AY	Serial I/O of the μPD78078Y was enhanced and the function is limited
80-pin	μPD780058	μPD780058Y[Note]	Serial I/O of the μPD78054 was enhanced and EMI-noise was reduced
80-pin	μPD78058F	μPD78058FY	EMI-noise reduced version of the μPD78054
80-pin	μPD78054	μPD78054Y	UART and D/A converter were added to the μPD78018F and I/O was enhanced
80-pin	μPD780065		RAM capacity of μPD780024 was expanded
64-pin	μPD780034	μPD780034Y	A/D converter of the μPD780024 was enhanced
64-pin	μPD780024	μPD780024Y	Serial I/O of the μPD78018F was enhanced
64-pin	μPD78014H		EMI-noise reduced version of the μPD78018F
64-pin	μPD78018F	μPD78018FY	Basic subseries for control
42/44-pin	μPD78083		On-chip UART, capable of operating at low voltage (1.8 V)

Inverter control

Pin	Product	Description
64-pin	μPD780988	On-chip inverter control circuit and UART. EMI-noise was reduced

FIP™ drive

Pin	Product	Description
100-pin	μPD780208	I/O and FIP C/D of the μPD78044F were enhanced, Display output total: 53
100-pin	μPD780228	I/O and FIP C/D of the μPD78044H were enhanced, Display output total: 48
80-pin	μPD780232	For panel control. On-chip FIP C/D. Display output total: 53
80-pin	μPD78044H	N-ch open drain was added to the μPD78044F, Display output total: 34
80-pin	μPD78044F	Basic subseries for driving FIP, Display output total: 34

LCD drive

Pin	Product	Y version	Description
100-pin	μPD780308	μPD780308Y	SIO of the μPD78064 was enhanced and ROM, RAM capacity expanded
100-pin	μPD78064B		EMI-noise reduced version of the μPD78064
100-pin	μPD78064	μPD78064Y	Basic subseries for driving LCDs, On-chip UART

Bus interface supported

Pin	Product	Description
80-pin	μPD78098B	IEBus™ controller is added to μPD78054. EMI-noise was reduced.
80-pin	μPD780948	On-chip DCAN controller
80-pin	μPD780701Y	On-chip DCAN/IEBus controller
80-pin	μPD780833Y	On-chip J1850 (CLASS2) controller

Meter control

Pin	Product	Description
80-pin	μPD780973	On-chip controller/driver for automotive meter drive
80-pin	μPD780955	Ultra-low power consumption and on-chip UART
100-pin	μPD780958	For industrial meter control

Note   Under planning

The major functional differences among the Y subseries are shown below.

Function / Subseries Name		ROM Capacity	Configuration of Serial Interface	I/O	V_{DD} MIN. Value
Control	μPD78078Y	48 K to 60 K	3-wire/2-wire/I²C: 1 ch 3-wire with automatic transmit/receive function: 1 ch 3-wire/UART: 1 ch	88	1.8 V
	μPD78070AY	–		61	2.7 V
	μPD780018AY	48 K to 60 K	3-wire with automatic transmit/receive function: 1 ch Time-division 3-wire: 1 ch I²C bus (multimaster supported): 1 ch	88	2.7 V
	μPD780058Y	24 K to 60 K	3-wire/2-wire/I²C: 1 ch 3-wire with automatic transmit/receive function: 1 ch 3-wire/time-division UART: 1 ch	68	1.8 V
	μPD78058FY	48 K to 60 K	3-wire/2-wire/I²C: 1 ch 3-wire with automatic transmit/receive function: 1 ch 3-wire/UART: 1 ch	69	2.7 V
	μPD78054Y	16 K to 60 K			2.0 V
	μPD780034Y	8 K to 32 K	UART: 1 ch 3-wire: 1 ch I²C bus (multimaster supported): 1 ch	51	1.8 V
	μPD780024Y				
	μPD78018FY	8 K to 60 K	3-wire/2-wire/I²C: 1 ch 3-wire with automatic transmit/receive function: 1 ch	53	
LCD drive	μPD780308Y	48 K to 60 K	3-wire/2-wire/I²C: 1 ch 3-wire/time-division UART: 1 ch 3-wire: 1 ch	57	2.0 V
	μPD78064Y	16 K to 32 K	3-wire/2-wire/I²C: 1 ch 3-wire/UART: 1 ch		

Remark The functions other than the serial interface are common to the Subseries without Y.

FUNCTION OVERVIEW (1/2)

Item		Function
Internal memory	PROM	60 Kbytes Note 1
	High-speed RAM	1024 bytes Note 1
	Expansion RAM	1024 bytes Note 2
	Buffer RAM	32 bytes
Memory space		64 Kbytes
General-purpose registers		8 bits $\times$ 32 registers (8 bits $\times$ 8 registers $\times$ 4 banks)
Minimum instruction execution time		Minimum instruction execution time cycle modification function provided.
	When main system clock selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (@ 10.0-MHz operation)
	When subsystem clock selected	122 μs (@ 32.768-kHz operation)
Instruction set		• 16-bit operation • Multiply/divide (8 bits $\times$ 8 bits, 16 bits $\div$ 8 bits) • Bit manipulate (set, reset, test, Boolean operation) • BCD adjust, etc.
I/O ports		Total: 53 • CMOS input: 2 • CMOS I/O: 47 • N-channel open-drain I/O (15-V withstand voltage): 4
A/D converter		• 8-bit resolution $\times$ 8 channels • Operable over a wide power supply voltage range: V_{DD} = 2.2 to 5.5 V
Serial interface		• 3-wire serial I/O mode/2-wire serial I/O mode/I²C bus mode selectable: 1 channel • 3-wire serial I/O mode (on-chip max. 32 bytes automatic data transmit/receive function): 1 channel
Timer		• 16-bit timer/event counter: 1 channel • 8-bit timer/event counter: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel
Timer output		3 (14-bit PWM output $\times$ 1)
Clock output		39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz (@ 10.0-MHz operation with main system clock), 32.768 kHz (@ 32.768-kHz operation with subsystem clock)
Buzzer output		2.4 kHz, 4.9 kHz, 9.8 kHz (@ 10.0-MHz operation with main system clock)
Vectored interrupt sources	Maskable	Internal: 8 External: 4
	Non-maskable	Internal: 1
	Software	1

Notes 1. The internal PROM and internal high-speed RAM capacities can be changed with the internal memory size switching register (IMS).

 2. The internal expansion RAM capacity can be changed with the internal expansion RAM size switching register (IXS).

FUNCTION OVERVIEW (2/2)

Item	Function
Test input	Internal: 1 External: 1
Supply voltage	V_{DD} = 1.8 to 5.5 V
Operating ambient temperature	T_A = −40 to +85°C
Package	• 64-pin plastic shrink DIP (750 mils) • 64-pin ceramic shrink DIP (with window) (750 mils) • 64-pin plastic QFP (14 × 14 mm) • 64-pin ceramic WQFN (750 mils)

PIN CONFIGURATION (Top View)

(1) Normal operating mode

- **64-pin Plastic Shrink DIP (750 mils)**
  μPD78P018FYCW
- **64-pin Ceramic Shrink DIP (with window) (750 mils)**
  μPD78P018FYDW

Left pin	No.		No.	Right pin
P20/SI1	1		64	AV$_{REF}$
P21/SO1	2		63	AV$_{DD}$
P22/$\overline{SCK1}$	3		62	P17/ANI7
P23/STB	4		61	P16/ANI6
P24/BUSY	5		60	P15/ANI5
P25/SI0/SB0/SDA0	6		59	P14/ANI4
P26/SO0/SB1/SDA1	7		58	P13/ANI3
P27/$\overline{SCK0}$/SCL	8		57	P12/ANI2
P30/TO0	9		56	P11/ANI1
P31/TO1	10		55	P10/ANI0
P32/TO2	11		54	AV$_{SS}$
P33/TI1	12		53	P04/XT1
P34/TI2	13		52	XT2
P35/PCL	14		51	V$_{PP}$
P36/BUZ	15		50	X1
P37	16		49	X2
V$_{SS}$	17		48	V$_{DD}$
P40/AD0	18		47	P03/INTP3
P41/AD1	19		46	P02/INTP2
P42/AD2	20		45	P01/INTP1
P43/AD3	21		44	P00/INTP0/TI0
P44/AD4	22		43	$\overline{RESET}$
P45/AD5	23		42	P67/ASTB
P46/AD6	24		41	P66/$\overline{WAIT}$
P47/AD7	25		40	P65/$\overline{WR}$
P50/A8	26		39	P64/$\overline{RD}$
P51/A9	27		38	P63
P52/A10	28		37	P62
P53/A11	29		36	P61
P54/A12	30		35	P60
P55/A13	31		34	P57/A15
V$_{SS}$	32		33	P56/A14

Cautions 1. Connect the V$_{PP}$ pin directly to V$_{SS}$.
2. Connect the AV$_{DD}$ pin to V$_{DD}$.
3. Connect the AV$_{SS}$ pin to V$_{SS}$.

- **64-pin Plastic QFP (14 × 14 mm)**
  μPD78P018FYGC-AB8
- **64-pin Ceramic WQFN (14 × 14 mm)**
  μPD78P018FYKK-S

Top pins (left to right):
P27/$\overline{\text{SCK0}}$/SCL, P26/SO0/SB1/SDA1, P25/SI0/SB0/SDA0, P24/BUSY, P23/STB, P22/$\overline{\text{SCK1}}$, P21/SO1, P20/SI1, AV$_{REF}$, AV$_{DD}$, P17/ANI7, P16/ANI6, P15/ANI5, P14/ANI4, P13/ANI3, P12/ANI2

Top pin numbers: 64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49

Left side pins:
- P30/TO0 — 1
- P31/TO1 — 2
- P32/TO2 — 3
- P33/TI1 — 4
- P34/TI2 — 5
- P35/PCL — 6
- P36/BUZ — 7
- P37 — 8
- V$_{SS}$ — 9
- P40/AD0 — 10
- P41/AD1 — 11
- P42/AD2 — 12
- P43/AD3 — 13
- P44/AD4 — 14
- P45/AD5 — 15
- P46/AD6 — 16

Right side pins:
- 48 — P11/ANI1
- 47 — P10/ANI0
- 46 — AV$_{SS}$
- 45 — P04/XT1
- 44 — XT2
- 43 — V$_{PP}$
- 42 — X1
- 41 — X2
- 40 — V$_{DD}$
- 39 — P03/INTP3
- 38 — P02/INTP2
- 37 — P01/INTP1
- 36 — P00/INTP0/TI0
- 35 — $\overline{\text{RESET}}$
- 34 — P67/ASTB
- 33 — P66/$\overline{\text{WAIT}}$

Bottom pin numbers: 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32

Bottom pins (left to right):
P47/AD7, P50/A8, P51/A9, P52/A10, P53/A11, P54/A12, P55/A13, V$_{SS}$, P56/A14, P57/A15, P60, P61, P62, P63, P64/$\overline{\text{RD}}$, P65/$\overline{\text{WR}}$

Cautions 1. Connect the V$_{PP}$ pin directly to V$_{SS}$.
2. Connect the AV$_{DD}$ pin to V$_{DD}$.
3. Connect the AV$_{SS}$ pin to V$_{SS}$.

A8 to A15:   Address Bus
AD0 to AD7:   Address/Data Bus
ANI0 to ANI7:   Analog Input
ASTB: Address Strobe
AV_{DD}:   Analog Power Supply
AV_{REF}:   Analog Reference Voltage
AV_{SS}:   Analog Ground
BUSY: Busy
BUZ: Buzzer Clock
INTP0 to INTP3:   Interrupt from Peripherals
P00 to P04:   Port 0
P10 to P17:   Port 1
P20 to P27:   Port 2
P30 to P37:   Port 3
P40 to P47:   Port 4
P50 to P57:   Port 5
P60 to P67:   Port 6
PCL: Programmable Clock

$\overline{\text{RESET}}$:   Reset
$\overline{\text{RD}}$:   Read Strobe
SB0, SB1:   Serial Bus
$\overline{\text{SCK0}}$, $\overline{\text{SCK1}}$:   Serial Clock
SCL: Serial Clock
SDA0, SDA1:   Serial Data
SI0, SI1:   Serial Input
SO0, SO1:   Serial Output
STB: Strobe
TI0 to TI2:   Timer Input
TO0 to TO2:   Timer Output
V_{DD}:   Power Supply
V_{PP}:   Programming Power Supply
V_{SS}:   Ground
$\overline{\text{WAIT}}$:   Wait
$\overline{\text{WR}}$:   Write Strobe
X1, X2:   Crystal (Main System Clock)
XT1, XT2:   Crystal (Subsystem Clock)

(2) PROM programming mode

- **64-pin Plastic Shrink DIP (750 mils)**
  μPD78P018FYCW
- **64-pin Ceramic Shrink DIP (with window) (750 mils)**
  μPD78P018FYDW

Pin (left)	No.		No.	Pin (right)
(L)	1		64	Vss
	2		63	VDD
	3		62	(L)
	4		61	
	5		60	
	6		59	
	7		58	(L)
	8		57	
D0	9		56	
D1	10		55	
D2	11		54	Vss
D3	12		53	(L)
D4	13		52	Open
D5	14		51	VPP
D6	15		50	(L)
D7	16		49	Open
Vss	17		48	VDD
A0	18		47	(L)
A1	19		46	$\overline{\text{PGM}}$
A2	20		45	(L)
A3	21		44	A9
A4	22		43	$\overline{\text{RESET}}$
A5	23		42	(L)
A6	24		41	(L)
A7	25		40	$\overline{\text{CE}}$
A8	26		39	$\overline{\text{OE}}$
A16	27		38	(L)
A10	28		37	(L)
A11	29		36	(L)
A12	30		35	(L)
A13	31		34	A15
Vss	32		33	A14
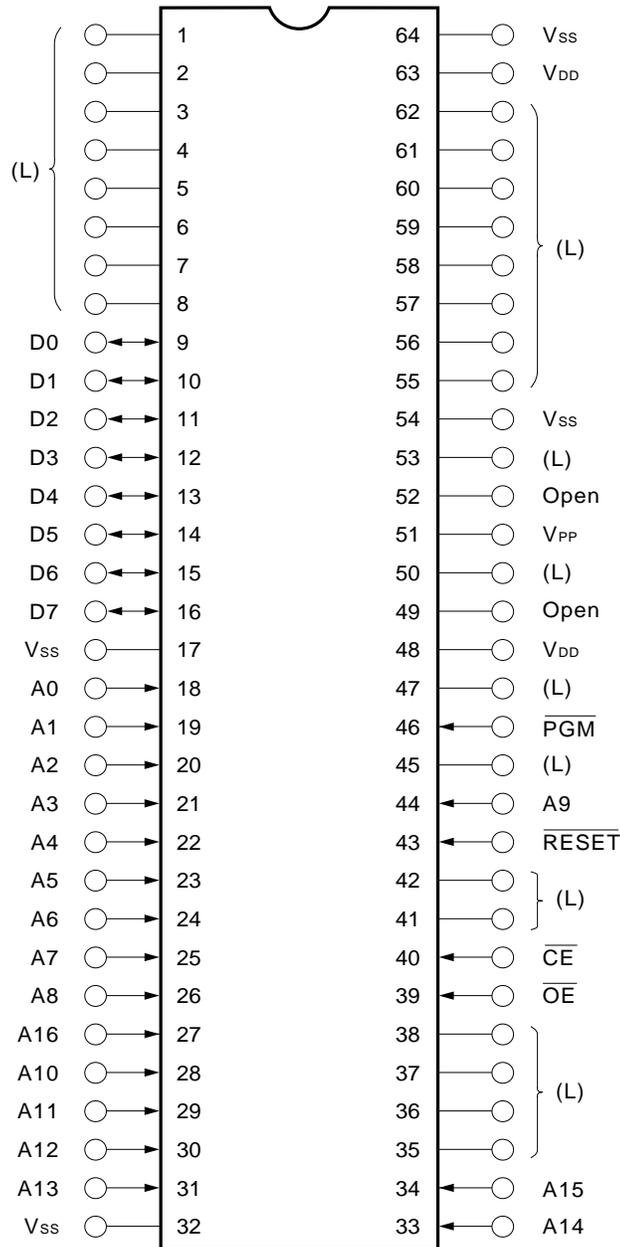
Cautions 1. (L): Independently connect to Vss via a pull-down resistor.
2. Vss: Connect to GND.
3. $\overline{\text{RESET}}$: Set to low level.
4. Open: Leave open.

- **64-pin Plastic QFP (14 × 14 mm)**
  μPD78P018FYGC-AB8
- **64-pin Ceramic WQFN (14 × 14 mm)**
  μPD78P018FYKK-S
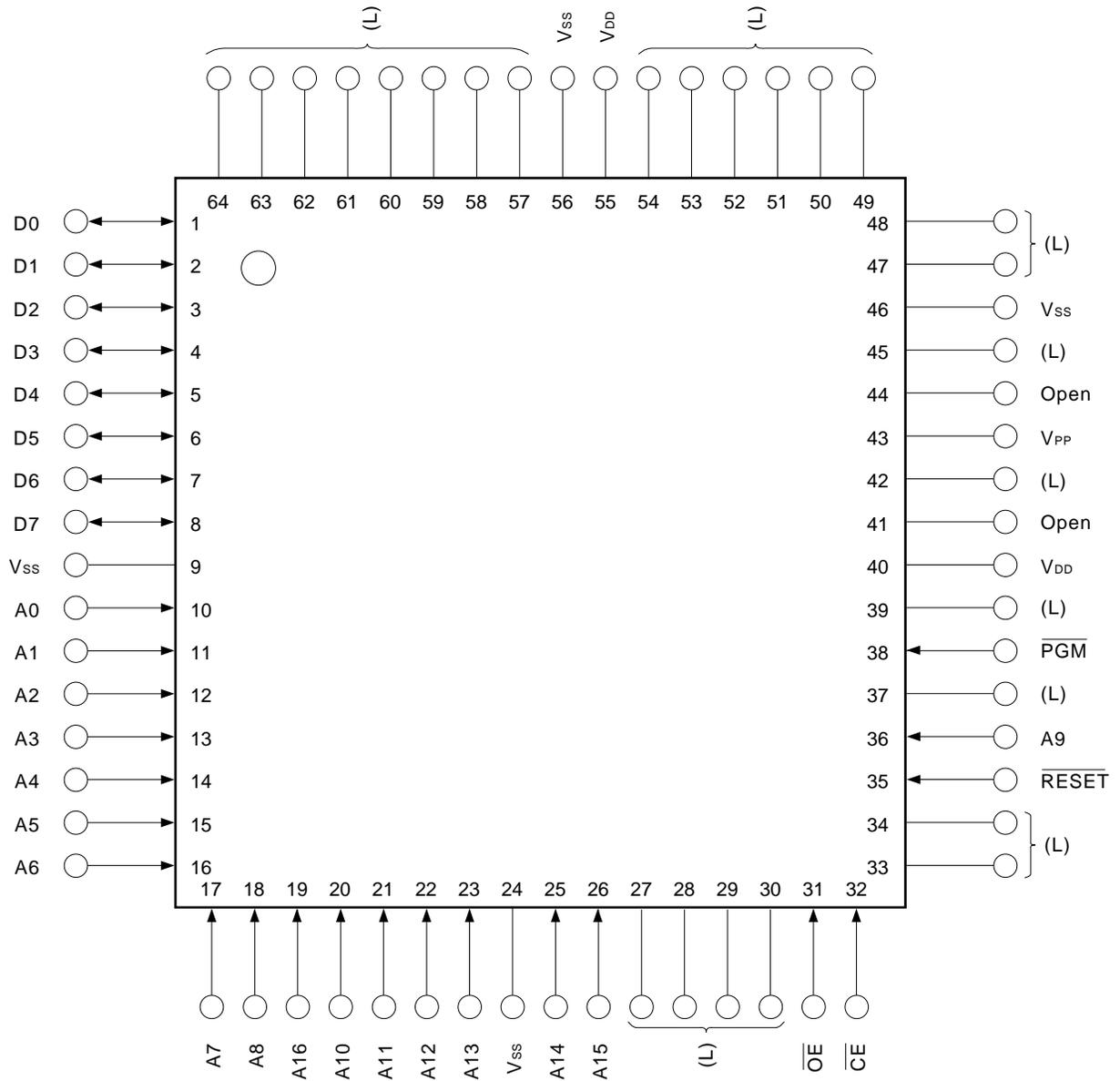
Cautions 1. (L):   **Independently connect to Vss via a pull-down resistor.**
         2. Vss: **Connect to GND.**
         3. RESET: **Set to low level.**
         4. Open: **Leave open.**

A0 to A16:   Address   RESET: Reset
CE: Chip Enable   VDD: Power Supply
D0 to D7:   Data Bus   VPP: Programming Power Supply
OE: Output Enable   Vss: Ground
PGM: Program

BLOCK DIAGRAM

TO0/P30 — 16-bit TIMER/EVENT COUNTER
TI0/INTP0/P00 —

TO1/P31 — 8-bit TIMER/EVENT COUNTER 1
TI1/P33 —

TO2/P32 — 8-bit TIMER/EVENT COUNTER 2
TI2/P34 —

WATCHDOG TIMER

WATCH TIMER

SI0/SB0/SDA0/P25 — SERIAL INTERFACE 0
SO0/SB1/SDA1/P26 —
$\overline{SCK0}$/SCL/P27 —

SI1/P20 — SERIAL INTERFACE 1
SO1/P21 —
$\overline{SCK1}$/P22 —
STB/P23 —
BUSY/P24 —

ANI0/P10-ANI7/P17 — A/D CONVERTER
AV_{DD} —
AV_{SS} —
AV_{REF} —

INTP0/P00-INTP3/P03 — INTERRUPT CONTROL

BUZ/P36 — BUZZER OUTPUT

PCL/P35 — CLOCK OUTPUT CONTROL

78K/0 CPU CORE

PROM (60 Kbytes)

RAM (2048 bytes)

V_{DD} V_{SS} V_{PP}

PORT0 — P00 / P01 to P03 / P04

PORT1 — P10 to P17

PORT2 — P20 to P27

PORT3 — P30 to P37

PORT4 — P40 to P47

PORT5 — P50 to P57

PORT6 — P60 to P67

EXTERNAL ACCESS — AD0/P40 to AD7/P47 / A8/P50 to A15/P57 / $\overline{RD}$/P64 / $\overline{WR}$/P65 / $\overline{WAIT}$/P66 / ASTB/P67

SYSTEM CONTROL — $\overline{RESET}$ / X1 / X2 / XT1/P04 / XT2

CONTENTS

1. DIFFERENCES BETWEEN THE μPD78P018FY AND MASK ROM VERSIONS

The μPD78P018FY is a single-chip microcontroller with an on-chip one-time PROM or EPROM that has program write, erase, and rewrite capability.

It is possible to make all the functions except for PROM specification and mask option of P60 to P63 pins, the same as those of mask ROM versions (μPD78011FY, 78012FY, 78013FY, 78014FY, 78015FY, 78016FY, and 78018FY) by setting the internal memory size switching register (IMS) and the internal expansion RAM size switching register (IXS).

Differences between the μPD78P018FY and mask ROM versions are shown in Table 1-1.

Table 1-1. Differences Between μPD78P018FY and Mask ROM Version

Item	μPD78P018FY	Mask ROM Versions
Internal ROM type	One-time PROM or EPROM	Mask ROM
Internal ROM capacity	60 Kbytes	μPD78011FY: 8 Kbytes μPD78012FY: 16 Kbytes μPD78013FY: 24 Kbytes μPD78014FY: 32 Kbytes μPD78015FY: 40 Kbytes μPD78016FY: 48 Kbytes μPD78018FY: 60 Kbytes
Internal high-speed RAM capacity	1024 bytes	μPD78011FY: 512 bytes μPD78012FY: 512 bytes μPD78013FY: 1024 bytes μPD78014FY: 1024 bytes μPD78015FY: 1024 bytes μPD78016FY: 1024 bytes μPD78018FY: 1024 bytes
Internal expansion RAM capacity	1024 byte	μPD78011FY: No μPD78012FY: No μPD78013FY: No μPD78014FY: No μPD78015FY: 512 bytes μPD78016FY: 512 bytes μPD78018FY: 1024 bytes
Internal ROM, internal high-speed RAM capacity changeable with internal memory size switching register (IMS)	Yes **Note 1**	No
Internal expansion RAM capacity changeable with internal expansion RAM size switching register (IXS)	Yes **Note 2**	No
IC pin	No	Yes
V$_{PP}$ pin	Yes	No
On-chip pull-up resistor mask option of P60 to P63 pins	No	Yes
Electrical specifications Recommended soldering conditions	See respective data sheet of individual products.	

Notes 1. The internal PROM capacity becomes 60 Kbytes and the internal high-speed RAM capacity becomes 1024 bytes by the $\overline{\text{RESET}}$ input.

   2. The internal expansion RAM capacity becomes 1024 bytes by the $\overline{\text{RESET}}$ input.

Caution There are differences in noise immunity and noise radiation between the PROM and mask ROM versions. When pre-producing an application set with the PROM version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the commercial samples (not engineering samples) of the mask ROM version.

2. PIN FUNCTIONS

2.1　Pins During Normal Operating Mode

(1)　Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P00	Input	Port 0 5-bit input/ output port	Input only	Input	INTP0/TI0
P01	Input/ output		Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	INTP1
P02					INTP2
P03					INTP3
P04 **Note1**	Input		Input only	Input	XT1
P10 to P17	Input/ output	Port 1 8-bit input/output port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. **Note 2**		Input	ANI0 to ANI7
P20	Input/ output	Port 2 8-bit input/output port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.		Input	SI1
P21					SO1
P22					$\overline{\text{SCK1}}$
P23					STB
P24					BUSY
P25					SI0/SB0/SDA0
P26					SO0/SB1/SDA1
P27					$\overline{\text{SCK0}}$/SCL
P30	Input/ output	Port 3 8-bit input/output port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—
P40 to P47	Input/ output	Port 4 8-bit input/output port. Input/output can be specified in 8-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software. Test input flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7

Notes 1. When using the P04/XT1 pin as an input port, set bit 6 (FRC) of the processor clock control register (PCC) to 1 (Do not use the on-chip feedback resistor of the subsystem clock oscillator).

2. When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input pins, set port 1 to the input mode. At this time, on-chip pull-up resistors are automatically disconnected.

(1) Port Pins (2/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P50 to P57	Input/ output	Port 5 8-bit input/output port. LEDs can be driven directly. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.		Input	A8 to A15
P60	Input/ output	Port 6 8-bit input/output port. Input/output can be specified in 1-bit units.	N-ch open-drain input/ output port. LEDs can be driven directly.	Input	—
P61					
P62					
P63					
P64			When used as an input port, an on-chip pull-up resistor can be specified by means of software.		$\overline{RD}$
P65					$\overline{WR}$
P66					$\overline{WAIT}$
P67					ASTB

(2) Non-port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input for which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.	Input	P00/TI0
INTP1				P01
INTP2				P02
INTP3		Falling edge detection external interrupt request input.		P03
SI0	Input	Serial interface serial data input.	Input	P25/SB0/SDA0
SI1				P20
SO0	Output	Serial interface serial data output.	Input	P26/SB1/SDA1
SO1				P21
SB0	Input/ output	Serial interface serial data input/output.	Input	P25/SI0/SDA0
SB1				P26/SO0/SDA1
SDA0				P25/SI0/SB0
SDA1				P26/SO0/SB1
$\overline{SCK0}$	Input/ output	Serial interface serial clock input/output.	Input	P27/SCL
$\overline{SCK1}$				P22
SCL				P27/$\overline{SCK0}$
STB	Output	Serial interface automatic transmit/receive strobe output.	Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input.	Input	P24

(2) Non-port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
TI0	Input	External count clock input to 16-bit timer (TM0).	Input	P00/INTP0
TI1		External count clock input to 8-bit timer (TM1).		P33
TI2		External count clock input to 8-bit timer (TM2).		P34
TO0	Output	16-bit timer (TM0) output (shared as 14-bit PWM output).	Input	P30
TO1		8-bit timer (TM1) output.		P31
TO2		8-bit timer (TM2) output.		P32
PCL	Output	Clock output (for main system clock, subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.		P36
AD0 to AD7	Input/output	Lower address/data bus for expanding memory externally.	Input	P40 to P47
A8 to A15	Output	Higher address bus for expanding memory externally.	Input	P50 to P57
$\overline{\text{RD}}$	Output	Strobe signal output for read from external memory.	Input	P64
$\overline{\text{WR}}$		Strobe signal output for writing to external memory.		P65
$\overline{\text{WAIT}}$	Input	Wait insertion at external memory access.	Input	P66
ASTB	Output	Strobe output that externally latches address information output to port 4 and port 5 to access external memory.	Input	P67
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
AV$_{REF}$	Input	A/D converter reference voltage input.	—	—
AV$_{DD}$	—	A/D converter analog power supply. Connect to V$_{DD}$.	—	—
AV$_{SS}$	—	A/D converter ground potential. Connect to V$_{SS}$.	—	—
$\overline{\text{RESET}}$	Input	System reset input.	—	—
X1	Input	Connecting crystal resonator for main system clock oscillation.	—	—
X2	—		—	—
XT1	Input	Connecting crystal resonator for subsystem clock oscillation.	Input	P04
XT2	—		—	—
V$_{DD}$	—	Positive power supply.	—	—
V$_{PP}$	—	High voltage applied during program write/verify. In normal operating mode, connect to V$_{SS}$ directly.	—	—
V$_{SS}$	—	Ground potential.	—	—

2.2 Pins During PROM Programming Mode

Pin	I/O	Function
$\overline{\text{RESET}}$	Input	Sets PROM programming mode. When +5 V or +12.5 V is applied to the V_{PP} and low level is applied to $\overline{\text{RESET}}$ pin, microcontroller is shifted to PROM programming mode.
V_{PP}	Input	Applies high voltage during PROM programming mode setting and program write/verify.
A0 to A16	Input	Address bus
D0 to D7	Input/output	Data bus
$\overline{\text{CE}}$	Input	PROM enable input/program pulse input.
$\overline{\text{OE}}$	Input	Read strobe input to PROM.
$\overline{\text{PGM}}$	Input	Program/program inhibit input in PROM programming mode.
V_{DD}	—	Positive power supply
V_{SS}	—	Ground potential

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 2-1. For the input/output circuit configuration of each type, see Figure 2-1.

Table 2-1. Types of Pin I/O Circuits

Pin Name	Input/output Circuit Type	I/O	Recommended Connection when Not Used
P00/INTP0/TI0	2	Input	Connect to V_{SS}.
P01/INTP1	8-A	Input/output	Independently connect to V_{SS} via a resistor.
P02/INTP2			
P03/INTP3			
P04/XT1	16	Input	Connect to V_{DD}.
P10/ANI0 to P17/ANI7	11	Input/output	Independently connect to V_{DD} or V_{SS} via a resistor.
P20/SI1	8-A		
P21/SO1	5-A		
P22/$\overline{SCK1}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0/SDA0	10-A		
P26/SO0/SB1/SDA1			
P27/$\overline{SCK0}$/SCL			
P30/TO0	5-A		
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0 to P47/AD7	5-E		Independently connect to V_{DD} via a resistor.
P50/A8 to P57/A15	5-A		Independently connect to V_{DD} or V_{SS} via a resistor.
P60 to P63	13-D		Independently connect to V_{DD} via a resistor.
P64/$\overline{RD}$	5-A		Independently connect to V_{DD} or V_{SS} via a resistor.
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
$\overline{RESET}$	2	Input	—
XT2	16	—	Leave open.
AV$_{REF}$	—		Connect to V_{SS}.
AV$_{DD}$			Connect to V_{DD}.
AV$_{SS}$			Connect to V_{SS}.
V$_{PP}$			Connect directly to V_{SS}.

Figure 2-1. Pin Input/Output Circuits
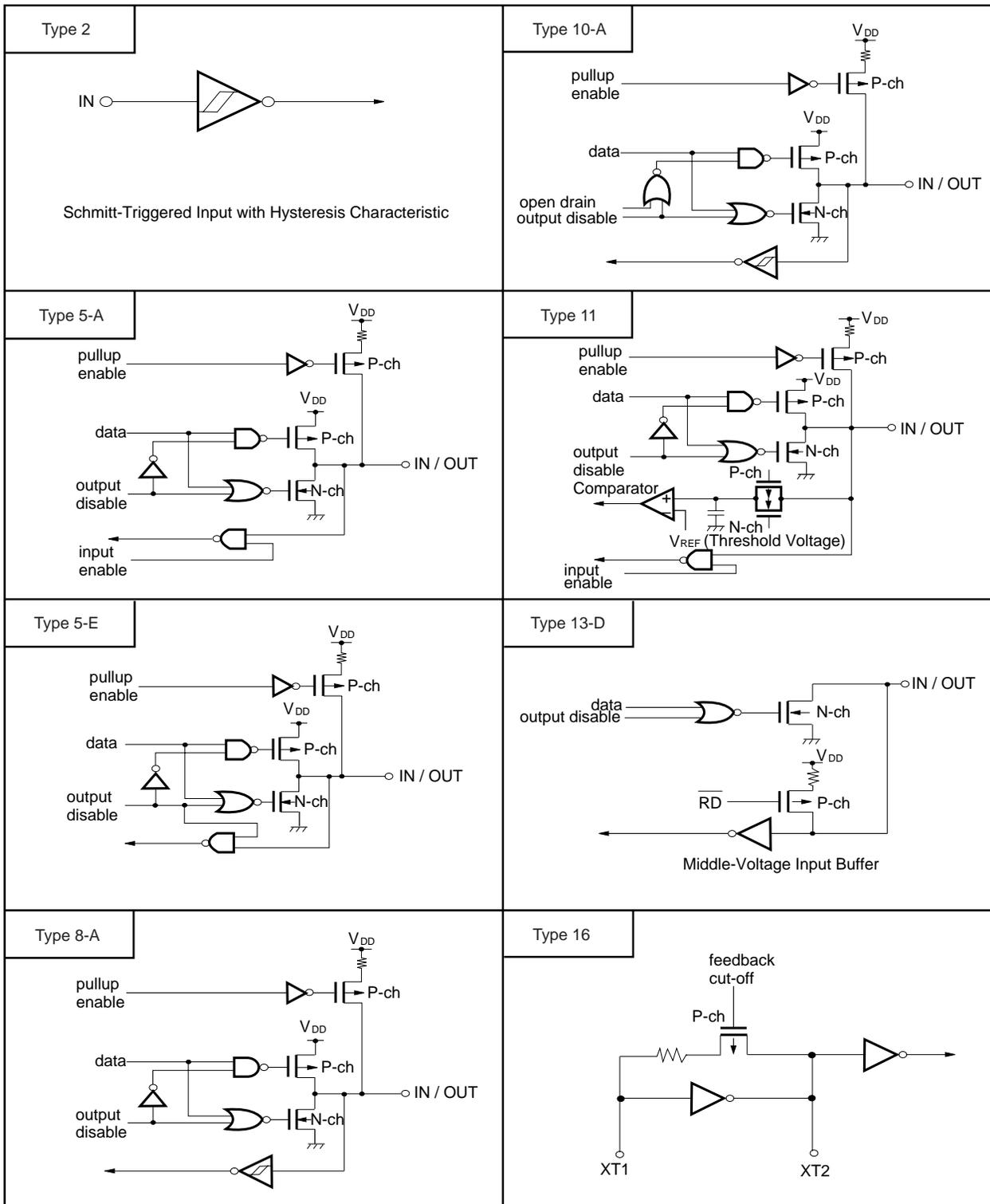
3. INTERNAL MEMORY SIZE SWITCHING REGISTER (IMS)

This register is used to disable the use of part of the internal memory by software. By setting this register (IMS), it is possible to get the same memory map as that of the mask ROM versions with a different internal memory (ROM, RAM).

IMS is set with an 8-bit memory manipulate instruction.

$\overline{\text{RESET}}$ input sets IMS to CFH.

Figure 3-1. Internal Memory Size Switching Register Format

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	W

ROM3	ROM2	ROM1	ROM0	Selection of Internal ROM Capacity
0	0	1	0	8 Kbytes
0	1	0	0	16 Kbytes
0	1	1	0	24 Kbytes
1	0	0	0	32 Kbytes
1	0	1	0	40 Kbytes
1	1	0	0	48 Kbytes
1	1	1	0	56 Kbytes **Note**
1	1	1	1	60 Kbytes
Other than above				Setting prohibited

RAM2	RAM1	RAM0	Selection of Internal High-Speed RAM Capacity
0	1	0	512 bytes
1	1	0	1024 bytes
Other than above			Setting prohibited

Note If external device expansion functions are to be employed for the μPD78P018FY, set the size of the internal ROM to 56 Kbytes or below using the internal memory size switching register (IMS).

Table 3-1 shows the setting values of IMS which make the memory map the same as that of the mask ROM versions.

Table 3-1. Internal Memory Size Switching Register Setting Values

Target Mask ROM Versions	IMS Setting Value
μPD78011FY	42H
μPD78012FY	44H
μPD78013FY	C6H
μPD78014FY	C8H
μPD78015FY	CAH
μPD78016FY	CCH
μPD78018FY	CFH

4. INTERNAL EXPANSION RAM SIZE SWITCHING REGISTER (IXS)

This register is used to disable the use of part of the internal expansion RAM capacity by software. By setting this register (IXS), it is possible to get the same memory map as that of the mask ROM versions with a different internal expansion RAM.

IXS is set with an 8-bit memory manipulate instruction.

$\overline{\text{RESET}}$ input sets IXS to 0AH.

Figure 4-1. Internal Expansion RAM Size Switching Register Format

	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IXS	0	0	0	0	IX RAM3	IX RAM2	IX RAM1	IX RAM0	FFF4H	0AH	W

IX RAM3	IX RAM2	IX RAM1	IX RAM0	Selection of Internal Expansion RAM Capacity
1	0	1	0	1024 bytes (F400H to F7FFH)
1	0	1	1	512 bytes (F600H to F7FFH)
1	1	0	0	0 bytes
Other than above				Setting prohibited
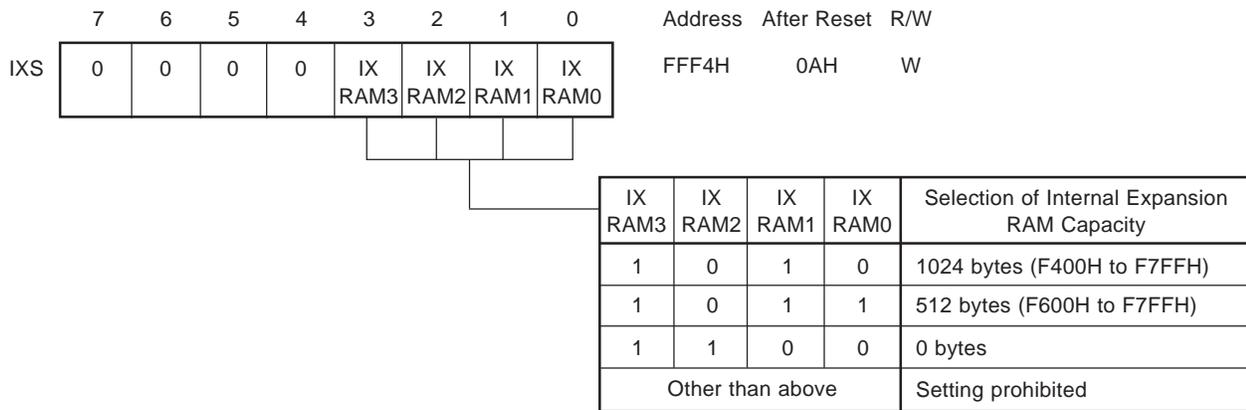
Table 4-1 shows the setting values of IXS which make the memory map the same as that of the mask ROM versions.

Table 4-1. Internal Expansion RAM Size Switching Register Setting Values

Target Mask ROM Versions	IXS Setting Value
μPD78011FY	0CH **Note**
μPD78012FY	
μPD78013FY	
μPD78014FY	
μPD78015FY	0BH
μPD78016FY	
μPD78018FY	0AH

Note   Even if a program for the μPD78P018FY in which "MOV IXS, #0CH"
is written is executed in the μPD78011FY, 78012FY, 78013FY, and
78014FY, the operations are not affected.

5. PROM PROGRAMMING

The μPD78P018FY has an internal 60-Kbyte PROM as a program memory. For programming, set the PROM programming mode by setting the V_{PP} and $\overline{RESET}$ pins. For unused pin connection, refer to "**PIN CONFIGURATION (Top View) (2) PROM programming mode**."

Caution   When writing in a program, use locations 0000H-EFFFH (specify the last address as EFFFH). You cannot write in using a PROM programmer that cannot specify the addresses to write.

5.1 Operating Modes

When +5 V or +12.5 V is applied to the V_{PP} pin and the low-level signal is applied to the $\overline{RESET}$ pin, the PROM programming mode is set. This mode will become the operating mode as shown in Table 5-1 when the $\overline{CE}$, $\overline{OE}$, and $\overline{PGM}$ pins are set as shown.

Further, when the read mode is set, it is possible to read the contents of the PROM.

Table 5-1. Operating Modes of PROM Programming

Pin \ Operating Mode	$\overline{RESET}$	V_{PP}	V_{DD}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	D0 to D7
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High-impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				×	H	H	High-impedance
				×	L	L	
Read		+5 V	+5 V	L	L	H	Data output
Output disable				L	H	×	High-impedance
Standby				H	×	×	High-impedance

× : L or H

(1) Read mode

Read mode is set if $\overline{CE}$ = L, $\overline{OE}$ = L is set.

(2) Output disable mode

Data output becomes high-impedance, and is in the output disable mode, if $\overline{OE}$ = H is set.

Therefore, it allows data to be read from any device by controlling the $\overline{OE}$ pin, if multiple μPD78P018FYs are connected to the data bus.

(3) Standby mode

Standby mode is set if $\overline{CE}$ = H is set.

In this mode, data outputs become high-impedance irrespective of the $\overline{OE}$ status.

(4) Page data latch mode

Page data latch mode is set if $\overline{CE}$ = H, $\overline{PGM}$ = H, $\overline{OE}$ = L are set at the beginning of page write mode.

In this mode, 1 page 4-byte data is latched in an internal address/data latch circuit.

(5) Page write mode

After 1 page 4 bytes of addresses and data are latched in the page data latch mode, a page write is executed by applying a 0.1-ms program pulse (active low) to the $\overline{PGM}$ pin with $\overline{CE}$ = H, $\overline{OE}$ = H. Then, program verification can be performed, if $\overline{CE}$ = L, $\overline{OE}$ = L are set.

If programming is not performed by a one-time program pulse, X (X $\leq$ 10) write and verification operations should be executed repeatedly.

(6) Byte write mode

Byte write is executed when a 0.1-ms program pulse (active low) is applied to the $\overline{PGM}$ pin with $\overline{CE}$ = L, $\overline{OE}$ = H. Then, program verification can be performed if $\overline{OE}$ = L is set.

If programming is not performed by a one-time program pulse, X (X $\leq$ 10) write and verification operations should be executed repeatedly.

(7) Program verify mode

Program verify mode is set if $\overline{CE}$ = L, $\overline{PGM}$ = H, $\overline{OE}$ = L are set. In this mode, check if a write operation is performed correctly, after the write.

(8) Program inhibit mode

Program inhibit mode is used when the $\overline{OE}$ pin, V$_{PP}$ pin, and D0 to D7 pins of multiple μPD78P018FYs are connected in parallel and a write is performed to one of those devices.

When a write operation is performed, the page write mode or byte write mode described above is used. At this time, a write is not performed to a device which has the $\overline{PGM}$ pin driven high.

5.2 PROM Write Procedure

Figure 5-1. Page Program Mode Flow Chart

```
                        ┌──────────────────────┐
                        │        Start         │
                        └──────────────────────┘
                                   │
                        ┌──────────────────────┐
                        │     Address = G      │
                        └──────────────────────┘
                                   │
                        ┌──────────────────────┐
                        │ VDD = 6.5 V, VPP = 12.5 V │
                        └──────────────────────┘
                                   │
                        ┌──────────────────────┐
                        │        X = 0         │
                        └──────────────────────┘
                                   │
                        ┌──────────────────────┐
                        │        Latch         │
                        └──────────────────────┘
                                   │
                        ┌──────────────────────┐
                        │ Address = Address + 1│
                        └──────────────────────┘
                                   │
                        ┌──────────────────────┐
                        │        Latch         │
                        └──────────────────────┘
                                   │
                        ┌──────────────────────┐
                        │ Address = Address + 1│
                        └──────────────────────┘
                                   │
                        ┌──────────────────────┐
                        │        Latch         │
                        └──────────────────────┘
                                   │
    ┌──────────────────────┐      ┌──────────────────────┐
    │ Address = Address + 1│      │ Address = Address + 1│
    └──────────────────────┘      └──────────────────────┘
                                   │
                        ┌──────────────────────┐
                        │        Latch         │
                        └──────────────────────┘
                                   │
                        ┌──────────────────────┐         No
                        │      X = X + 1       │◄──────────────┐
                        └──────────────────────┘               │
                                   │                   Yes     │
                        ┌──────────────────────┐    ◄─── X = 10 ?
                        │  0.1-ms program pulse│               │
                        └──────────────────────┘               │
                                   │             Fail          │
                              Verify 4 bytes ──────────────────┘
                                   │ Pass
              No              Address = N ?
        ◄──────────────────
                                   │ Yes
                        ┌──────────────────────┐
                        │ VDD = 4.5 to 5.5 V, VPP = VDD │
                        └──────────────────────┘
                                   │
              Pass         Verify all bytes       Fail
        ◄──────────────                      ──────────────►
                                   │ All Pass
                        ┌──────────────────────┐      ┌──────────────────────┐
                        │      Write end       │      │  Defective product   │
                        └──────────────────────┘      └──────────────────────┘
```
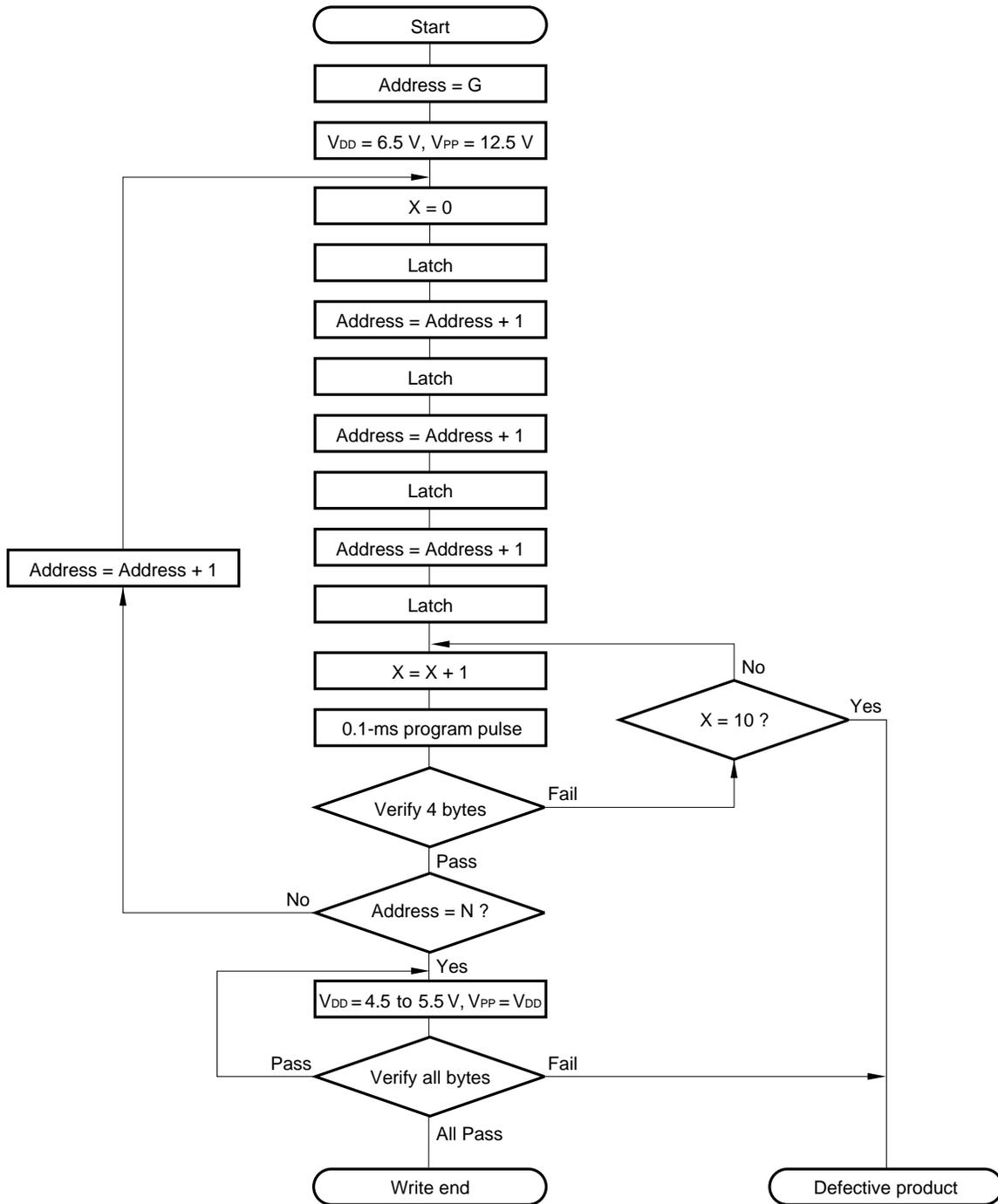
G = Start address

N = Program last address

Figure 5-2. Page Program Mode Timing

Page Data Latch	Page Program	Program Verify

A2 to A16

A0, A1

D0 to D7

Hi-Z

Data Input   Data Output

V$_{PP}$
V$_{PP}$
V$_{DD}$

V$_{DD}$
V$_{DD}$ + 1.5
V$_{DD}$

$\overline{CE}$
V$_{IH}$
V$_{IL}$

$\overline{PGM}$
V$_{IH}$
V$_{IL}$

$\overline{OE}$
V$_{IH}$
V$_{IL}$
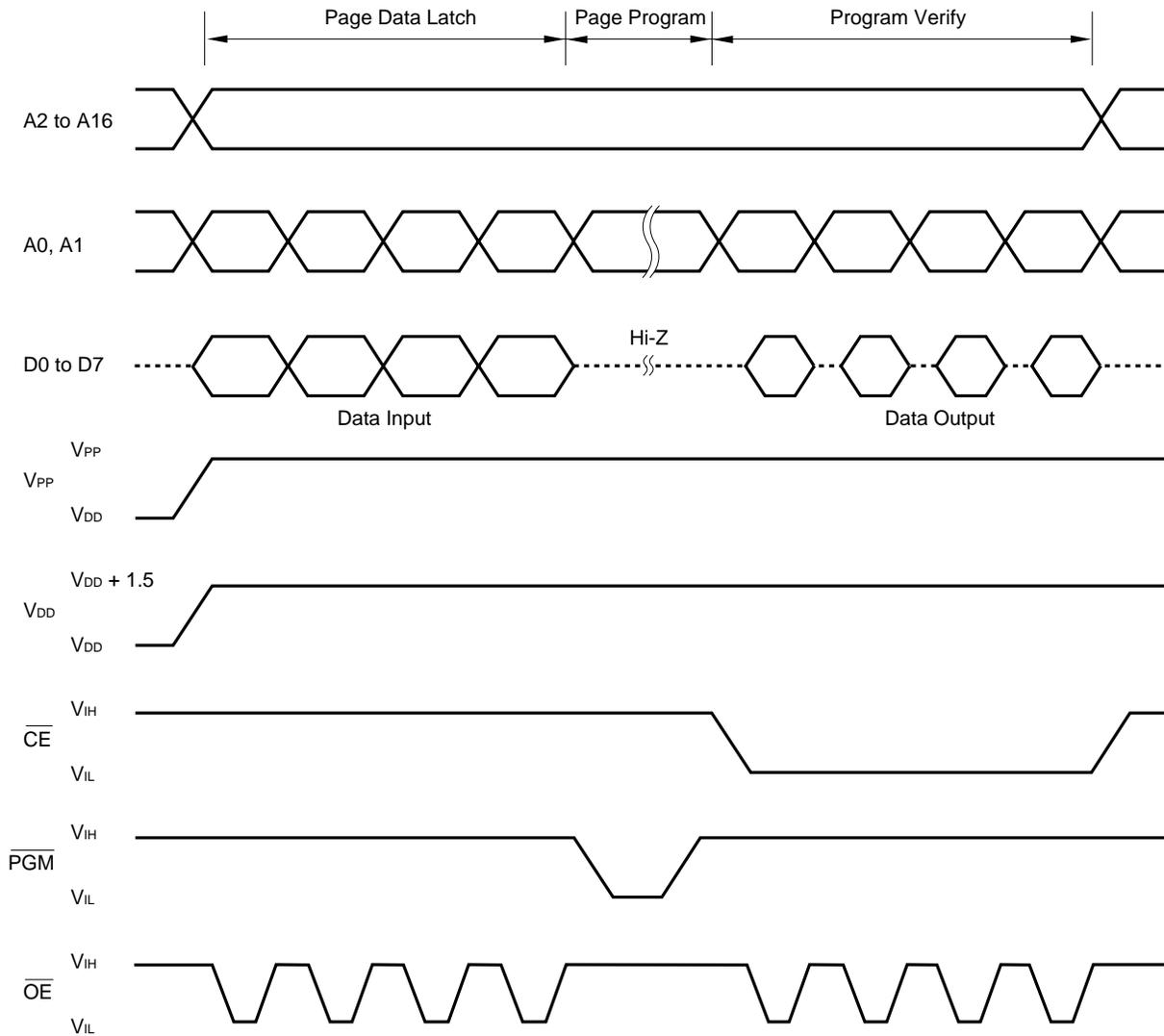
Figure 5-3. Byte Program Mode Flow Chart

```
                            ┌──────────────┐
                            │    Start     │
                            └──────┬───────┘
                            ┌──────┴───────┐
                            │ Address = G  │
                            └──────┬───────┘
                    ┌────────────────────────────────┐
                    │ VDD = 6.5 V, VPP = 12.5 V       │
                    └──────┬─────────────────────────┘
                    ┌──────┴───────┐
                    │    X = 0     │
                    └──────┬───────┘
                    ┌──────┴───────┐                  No
                    │  X = X + 1   │
                    └──────┬───────┘          ◇ X = 10 ?  ◇  Yes
                    │ 0.1-ms program pulse │
                    └──────┬───────┘              Fail
   ┌──────────────────┐   ◇  Verify  ◇ ──────────┘
   │ Address=Address+1│       │
   └──────────────────┘     Pass
          No      ◇ Address = N ? ◇
                          │
                        Yes
              │ VDD = 4.5 to 5.5 V, VPP = VDD │
      Pass   ◇  Verify all bytes  ◇   Fail
                    All Pass
          ┌──────────────┐        ┌───────────────────┐
          │  Write end   │        │ Defective product │
          └──────────────┘        └───────────────────┘
```
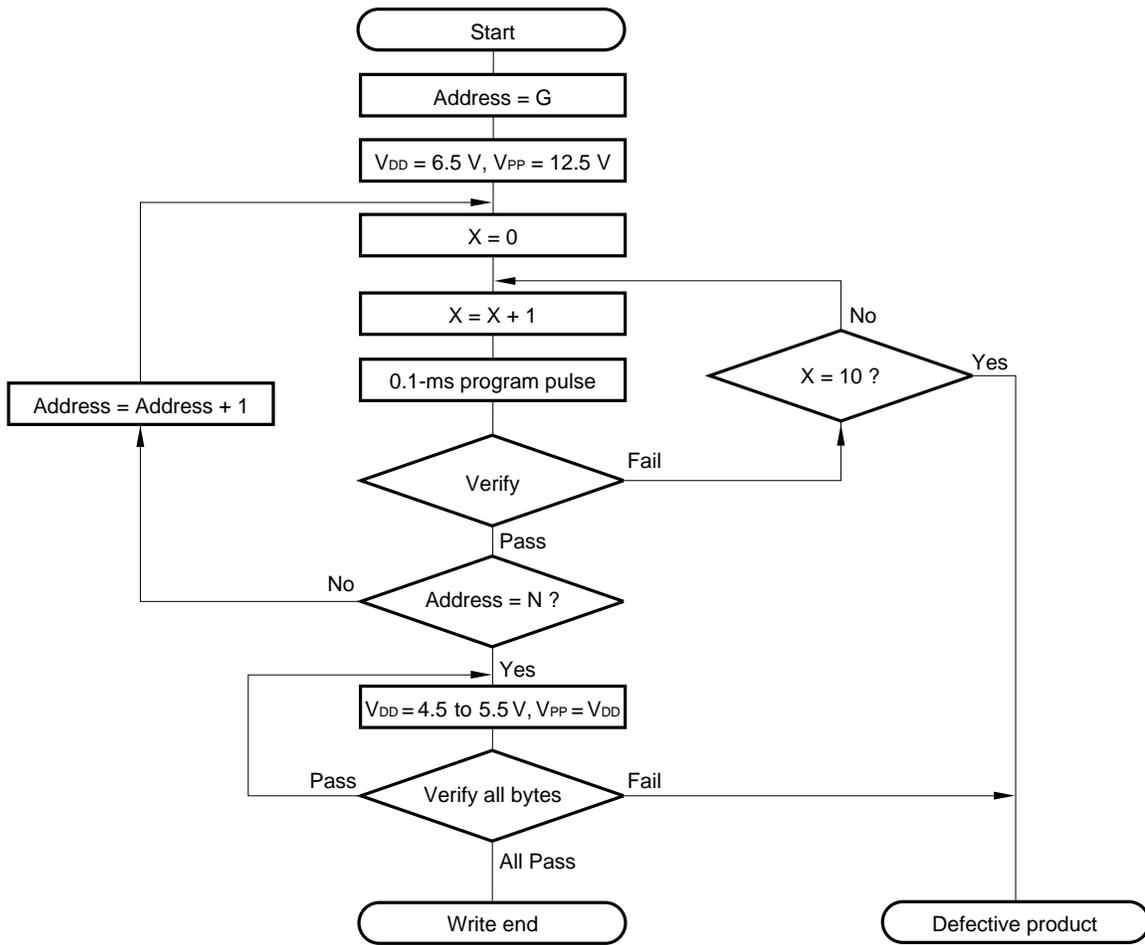
G = Start address
N = Program last address

Figure 5-4. Byte Program Mode Timing

| Program | Program Verify |

A0 to A16

D0 to D7 — Data Input — Hi-Z — Data Output —

V_{PP}
V_{PP}
V_{DD}

V_{DD}
V_{DD} + 1.5
V_{DD}

$\overline{CE}$
V_{IH}
V_{IL}

$\overline{PGM}$
V_{IH}
V_{IL}

$\overline{OE}$
V_{IH}
V_{IL}
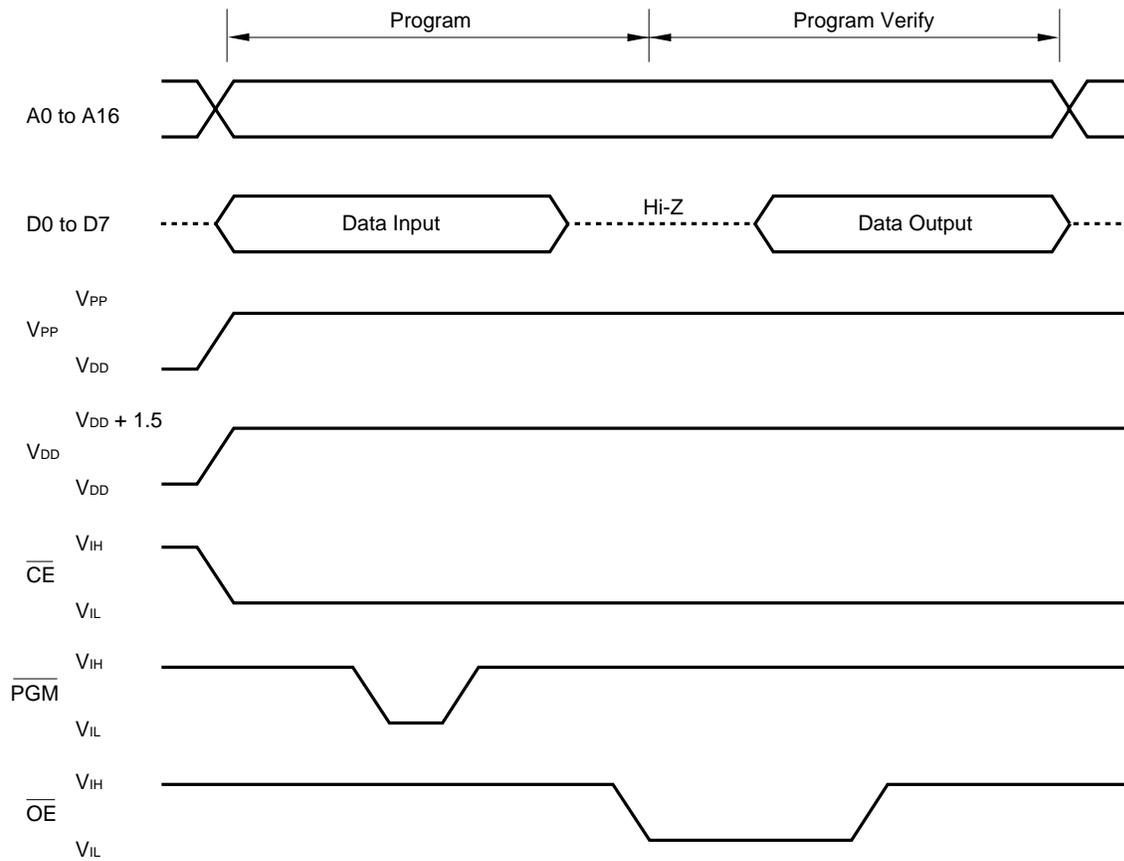
Cautions 1. V$_{DD}$ should be applied before V$_{PP}$ and cut after V$_{PP}$.

2. V$_{PP}$ must not exceed +13.5 V including overshoot.

3. Removing and reinserting while +12.5 V is applied to V$_{PP}$ may adversely affect reliability.

5.3 PROM Read Procedure

The contents of PROM are readable to the external data bus (D0 to D7) according to the read procedure shown below.

(1) Fix the $\overline{\text{RESET}}$ pin at low level, supply +5 V to the V$_{PP}$ pin, and connect all other unused pins as shown in **"PIN CONFIGURATION (Top View) (2) PROM programming mode".**

(2) Supply +5 V to the V$_{DD}$ and V$_{PP}$ pins.

(3) Input address of read data into the A0 to A16 pins.

(4) Read mode

(5) Output data to D0 to D7 pins.

The timings of the above steps (2) to (5) are shown in Figure 5-5.

Figure 5-5. PROM Read Timings
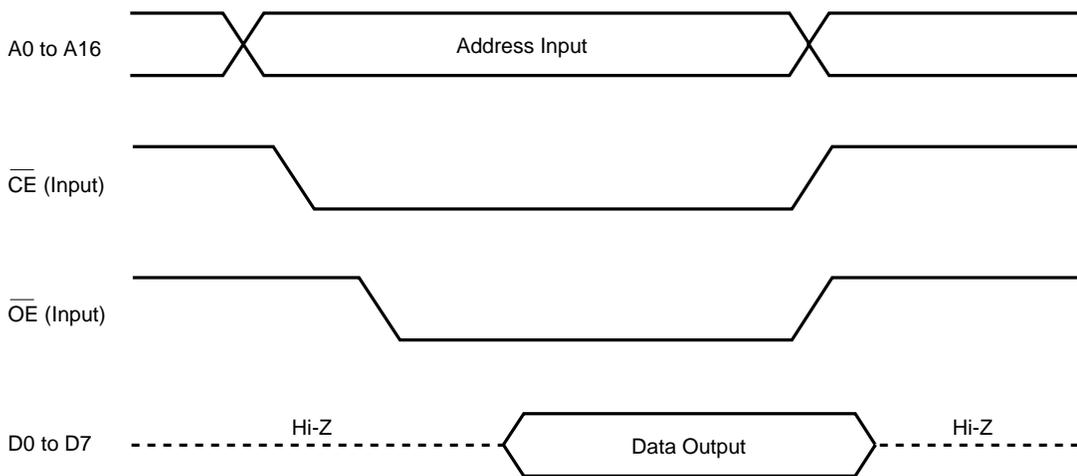
6.   PROGRAM ERASURE (FOR _μ_PD78P018FYDW, 78P018FYKK-S)

The _μ_PD78P018FYDW, 78P018FYKK-S are capable of erasing (FFH) the contents of data written in a program memory and rewriting.

When erasing the contents of data, irradiate light having a wavelength of less than about 400 nm to the erasure window. Normally, irradiate ultraviolet rays of 254 nm wavelength. Volume of irradiation required to completely erase the contents of data is as follows:

- UV intensity × erasing time: 30 W • s/cm^2 or more
- Erasing time: 40 min. or longer (When a UV lamp of 12 mW/cm^2 is used. However, a longer time may be needed because of deterioration in performance of the UV lamp, contamination of the erasure window, etc.)

When erasing the contents of data, set up the UV lamp within 2.5 cm from the erasing window. Further, if a filter is provided for a UV lamp, irradiate the ultraviolet rays after removing the filter.

7.   OPAQUE FILM ON ERASURE WINDOW (FOR _μ_PD78P018FYDW, 78P018FYKK-S)

To protect from unintentional erasure by rays other than that of the lamp for erasing EPROM contents, or to protect internal circuit other than EPROM from misoperating by rays, cover the erasure window with an opaque film when EPROM contents erasure is not performed.

8.   ONE-TIME PROM VERSION SCREENING

The one-time PROM versions (_μ_PD78P018FYCW, 78P018FYGC-AB8) cannot be tested completely by NEC before it is shipped, because of its structure. It is recommended to perform screening to verify PROM after writing necessary data and performing high-temperature storage under the condition below.

Storage Temperature	Storage Time
125°C	24 hours

NEC provides for a fee one-time PROM writing, marking, screening, and verify service for products designated as "QTOP Microcontrollers." For details, contact an NEC sales representative.

9. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T$_A$ = 25°C)

Parameter	Symbol	Test Conditions		Ratings	Unit
Supply voltage	V$_{DD}$			−0.3 to +7.0	V
	V$_{PP}$			−0.3 to +13.5	V
	AV$_{DD}$			−0.3 to V$_{DD}$ + 0.3	V
	AV$_{REF}$			−0.3 to V$_{DD}$ + 0.3	V
	AV$_{SS}$			−0.3 to +0.3	V
Input voltage	V$_{I1}$	P00 to P04, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, X1, X2, XT2, $\overline{RESET}$		−0.3 to V$_{DD}$ + 0.3	V
	V$_{I2}$	P60 to P63	Open-drain	−0.3 to +16	V
	V$_{I3}$	A9	PROM programming mode	−0.3 to +13.5	V
Output voltage	V$_O$			−0.3 to V$_{DD}$ + 0.3	V
Analog input voltage	V$_{AN}$	P10 to P17	Analog input pin	AV$_{SS}$ − 0.3 to AV$_{REF}$ + 0.3	V
Output current, high	I$_{OH}$	1 pin		−10	mA
		Total for P10 to P17, P20 to P27, P30 to P37		−15	mA
		Total for P01 to P03, P40 to P47, P50 to P57, P60 to P67		−15	mA
Output current, low	I$_{OL}$**Note**	1 pin	Peak value	30	mA
			rms value	15	mA
		Total for P40 to P47, P50 to P55	Peak value	100	mA
			rms value	70	mA
		Total for P01 to P03, P56, P57, P60 to P67	Peak value	100	mA
			rms value	70	mA
		Total for P01 to P03, P64 to P67	Peak value	50	mA
			rms value	20	mA
		Total for P10 to P17, P20 to P27, P30 to P37	Peak value	50	mA
			rms value	20	mA
Operating ambient temperature	T$_A$			−40 to +85	°C
Storage temperature	T$_{stg}$			−65 to +150	°C

Note   The rms value should be calculated as follows: [rms value] = [Peak value] $\times \sqrt{\text{Duty}}$

Caution   Product quality may suffer if the absolute maximum rating is exceed even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Capacitance (T$_A$ = 25°C, V$_{DD}$ = V$_{SS}$ = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C$_{IN}$	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C$_{IO}$	f = 1 MHz Unmeasured pins returned to 0 V.	P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67			15	pF
			P60 to P63			20	pF

Remark   Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port functions.

Main System Clock Oscillator Characteristics (T$_A$ = −40 to +85°C, V$_{DD}$ = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator	X2 X1 V$_{PP}$ C2 C1	Oscillation frequency (f$_X$) **Note 1**	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	1		10	MHz
			1.8 V ≤ V$_{DD}$ < 2.7 V	1		5	
		Oscillation stabilization time **Note 2**	After V$_{DD}$ reaches oscillator voltage range MIN.			4	ms
Crystal resonator	X2 X1 V$_{PP}$ C2 C1	Oscillation frequency (f$_X$) **Note 1**	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	1		10	MHz
			1.8 V ≤ V$_{DD}$ < 2.7 V	1		5	
		Oscillation stabilization time **Note 2**	V$_{DD}$ = 4.5 to 5.5 V			10	ms
						30	
External clock	X2 X1 μPD74HCU04	X1 input frequency (f$_X$) **Note 1**		1.0		10.0	MHz
		X1 input high-/low-level width (t$_{XH}$, t$_{XL}$)		45		500	ns
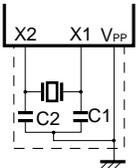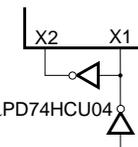
Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.
     2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wire the area enclosed by the broken line in the above figures as follows to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always keep the ground point of the oscillator capacitor to the same potential as V$_{SS}$.**
- **Do not ground the capacitor to a ground pattern in which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

Subsystem Clock Oscillator Characteristics (T$_A$ = –40 to +85°C, V$_{DD}$ = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator	V$_{PP}$ XT2 XT1 R1 C4 C3	Oscillation frequency (f$_{XT}$) **Note 1**		32	32.768	35	kHz
		Oscillation stabilization time **Note 2**	V$_{DD}$ = 4.5 to 5.5 V		1.2	2	s
						10	
External clock	XT2 XT1 μPD74HCU04	XT1 input frequency (f$_{XT}$) **Note 1**		32		100	kHz
		XT1 input high-/low-level width (t$_{XTH}$, t$_{XTL}$)		5		15	μs
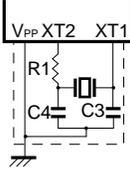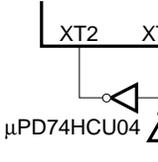
Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.
   2. Time required to stabilize oscillation after V$_{DD}$ reaches oscillator voltage MIN.

Cautions 1. When using the subsystem clock oscillator, wire the area enclosed by the broken line in the above figures as follows to avoid an adverse effect from wiring capacitance.

    • **Keep the wiring length as short as possible.**
    • **Do not cross the wiring with the other signal lines.**
    • **Do not route the wiring near a signal line through which a high fluctuating current flows.**
    • **Always keep the ground point of the oscillator capacitor to the same potential as V$_{SS}$.**
    • **Do not ground the capacitor to a ground pattern in which a high current flows.**
    • **Do not fetch signals from the oscillator.**

   2. The subsystem clock oscillator is a low-amplitude circuit in order to achieve a low consumption current, and is more prone to malfunction due to noise than the main system clock oscillator.
    Particular care is therefore required with the wiring method when the subsystem clock is used.

RECOMMENDED OSCILLATOR CONSTANTS

Main system clock: Ceramic resonator (T$_A$ = –40 to +85°C)

Manufacturer	Name	Frequency (MHz)	Recommended Oscillator Constants		Oscillation Voltage Range		Remarks
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
TDK	CCR4.0MC3	4.00	On-Chip	On-Chip	1.8	5.5	On-chip capacitor, surface mounting type
	FCR4.0MC5	4.00	On-Chip	On-Chip	1.8	5.5	On-chip capacitor, insertion type
	CCR4.19MC3	4.19	On-Chip	On-Chip	1.8	5.5	On-chip capacitor, surface mounting type
	FCR4.19MC5	4.19	On-Chip	On-Chip	1.8	5.5	On-chip capacitor, insertion type
	CCR5.00MC3	5.00	On-Chip	On-Chip	1.8	5.5	On-chip capacitor, surface mounting type
	FCR5.00MC5	5.00	On-Chip	On-Chip	1.8	5.5	On-chip capacitor, insertion type
	CCR8.00MC	8.00	On-Chip	On-Chip	2.7	5.5	On-chip capacitor, surface mounting type
	FCR8.00MC5	8.00	On-Chip	On-Chip	2.7	5.5	On-chip capacitor, insertion type
	CCR8.38MC	8.38	On-Chip	On-Chip	2.7	5.5	On-chip capacitor, surface mounting type
	FCR8.38MC5	8.38	On-Chip	On-Chip	2.7	5.5	On-chip capacitor, insertion type
	CCR10.00MC	10.00	On-Chip	On-Chip	2.7	5.5	On-chip capacitor, surface mounting type
	FCR10.00MC5	10.00	On-Chip	On-Chip	2.7	5.5	On-chip capacitor, insertion type
Murata Mfg. Co., Ltd.	CSA4.00MG	4.00	30	30	1.8	5.5	Insertion type
	CST4.00MGW	4.00	On-Chip	On-Chip	1.8	5.5	On-chip capacitor, insertion type
	CSA4.19MG	4.19	30	30	1.8	5.5	Insertion type
	CST4.19MGW	4.19	On-Chip	On-Chip	1.8	5.5	On-chip capacitor, insertion type
	CSA5.00MG	5.00	30	30	1.8	5.5	Insertion type
	CST5.00MGW	5.00	On-Chip	On-Chip	1.8	5.5	On-chip capacitor, insertion type
	CSA8.00MTZ	8.00	30	30	2.7	5.5	Insertion type
	CST8.00MTW	8.00	On-Chip	On-Chip	2.7	5.5	On-chip capacitor, insertion type
	CSA8.38MTZ	8.38	30	30	2.7	5.5	Insertion type
	CST8.38MTW	8.38	On-Chip	On-Chip	2.7	5.5	On-chip capacitor, insertion type
	CSA10.00MTZ	10.00	30	30	2.7	5.5	Insertion type
	CST10.00MTW	10.00	On-Chip	On-Chip	2.7	5.5	On-chip capacitor, insertion type

Caution   The oscillator constants and oscillation voltage range indicate conditions for stable oscillation, but do not guarantee oscillation frequency accuracy. If oscillation frequency accuracy is required for actual circuits, it is necessary to adjust the oscillation frequency of the oscillator in the actual circuit. Please contact directly the manufacturer of the resonator to be used.

Main system clock: Ceramic resonator (T$_A$ = −20 to +80°C)

Manufacturer	Name	Frequency (MHz)	Recommended Oscillator Constants		Oscillation Voltage Range		Remarks
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
Kyocera Corporation	PBRC4.00A	4.00	33	33	1.8	5.5	Surface mounting type
	PBRC4.00B	4.00	On-Chip	On-Chip	1.8	5.5	On-chip capacitor, surface mounting type
	KBR-4.00MSA	4.00	33	33	1.8	5.5	Insertion type
	KBR-4.00MKS	4.00	On-Chip	On-Chip	1.8	5.5	On-chip capacitor, insertion type
	PBRC5.00A	5.00	33	33	1.8	5.5	Surface mounting type
	PBRC5.00B	5.00	On-Chip	On-Chip	1.8	5.5	On-chip capacitor, surface mounting type
	KBR-5.00MSA	5.00	33	33	1.8	5.5	Insertion type
	KBR-5.00MKS	5.00	On-Chip	On-Chip	1.8	5.5	On-chip capacitor, insertion type
	KBR-8M	8.00	33	33	2.7	5.5	Insertion type
	KBR-10M	10.00	33	33	2.7	5.5	Insertion type

Caution   The oscillator constants and oscillation voltage range indicate conditions for stable oscillation. The oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation frequency must be adjusted on the implementation circuit. For details, please contact directly the manufacturer of the resonator you will use.

DC Characteristics (T$_A$ = –40 to +85°C, V$_{DD}$ = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V$_{IH1}$	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67	V$_{DD}$ = 2.7 to 5.5 V	0.7V$_{DD}$		V$_{DD}$	V
				0.8V$_{DD}$		V$_{DD}$	V
	V$_{IH2}$	P00 to P03, P20, P22, P24 to P27, P33, P34, $\overline{\text{RESET}}$	V$_{DD}$ = 2.7 to 5.5 V	0.8V$_{DD}$		V$_{DD}$	V
				0.85V$_{DD}$		V$_{DD}$	V
	V$_{IH3}$	P60 to P63 (N-ch open-drain)	V$_{DD}$ = 2.7 to 5.5 V	0.7V$_{DD}$		15	V
				0.8V$_{DD}$		15	V
	V$_{IH4}$	X1, X2	V$_{DD}$ = 2.7 to 5.5 V	V$_{DD}$ – 0.5		V$_{DD}$	V
				V$_{DD}$ – 0.2		V$_{DD}$	V
	V$_{IH5}$	XT1/P04, XT2	4.5 V ≤ V$_{DD}$ ≤ 5.5 V	0.8V$_{DD}$		V$_{DD}$	V
			2.7 V ≤ V$_{DD}$ < 4.5 V	0.9V$_{DD}$		V$_{DD}$	V
			1.8 V ≤ V$_{DD}$ < 2.7 V **Note**	0.9V$_{DD}$		V$_{DD}$	V
Input voltage, low	V$_{IL1}$	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67	V$_{DD}$ = 2.7 to 5.5 V	0		0.3V$_{DD}$	V
				0		0.2V$_{DD}$	V
	V$_{IL2}$	P00 to P03, P20, P22, P24 to P27, P33, P34, $\overline{\text{RESET}}$	V$_{DD}$ = 2.7 to 5.5 V	0		0.2V$_{DD}$	V
				0		0.15V$_{DD}$	V
	V$_{IL3}$	P60 to P63	4.5 V ≤ V$_{DD}$ ≤ 5.5 V	0		0.3V$_{DD}$	V
			2.7 V ≤ V$_{DD}$ < 4.5 V	0		0.2V$_{DD}$	V
				0		0.1V$_{DD}$	V
	V$_{IL4}$	X1, X2	V$_{DD}$ = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
	V$_{IL5}$	XT1/P04, XT2	4.5 V ≤ V$_{DD}$ ≤ 5.5 V	0		0.2V$_{DD}$	V
			2.7 V ≤ V$_{DD}$ < 4.5 V	0		0.1V$_{DD}$	V
			1.8 V ≤ V$_{DD}$ < 2.7 V **Note**	0		0.1V$_{DD}$	V
Output voltage, high	V$_{OH1}$	V$_{DD}$ = 4.5 to 5.5 V, I$_{OH}$ = –1 mA		V$_{DD}$ – 1.0			V
		I$_{OH}$ = –100 μA		V$_{DD}$ – 0.5			V
Output voltage, low	V$_{OL1}$	P50 to P57, P60 to P63	V$_{DD}$ = 4.5 to 5.5 V, I$_{OL}$ = 15 mA		0.4	2.0	V
		P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67	V$_{DD}$ = 4.5 to 5.5 V, I$_{OL}$ = 1.6 mA			0.4	V
	V$_{OL2}$	SB0, SB1, $\overline{\text{SCK0}}$	V$_{DD}$ = 4.5 to 5.5 V, open-drain pulled-up (R = 1 kΩ)			0.2V$_{DD}$	V
	V$_{OL3}$	I$_{OL}$ = 400 μA				0.5	V

Note When using XT1/P04 as P04, input the inverse phase of P04 should be input to XT2 using an inverter.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T$_A$ = −40 to +85°C, V$_{DD}$ = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I$_{LIH1}$	V$_{IN}$ = V$_{DD}$	P00 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, $\overline{RESET}$			3	μA
	I$_{LIH2}$		X1, X2, XT1/P04, XT2			20	μA
	I$_{LIH3}$	V$_{IN}$ = 15 V	P60 to P63			80	μA
Input leakage current, low	I$_{LIL1}$	V$_{IN}$ = 0 V	P00 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, $\overline{RESET}$			−3	μA
	I$_{LIL2}$		X1, X2, XT1/P04, XT2			−20	μA
	I$_{LIL3}$		P60 to P63			−3 **Note**	μA
Output leakage current, high	I$_{LOH}$	V$_{OUT}$ = V$_{DD}$				3	μA
Output leakage current, low	I$_{LOL}$	V$_{OUT}$ = 0 V				−3	μA
Software pull-up resistor	R	V$_{IN}$ = 0 V, P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67		15	40	90	kΩ

Note For pins P60 to P63, a low-level input leak current of −200 μA (MAX.) flows only during the 3 clocks (no-wait time) after an instruction has been executed to read out port 6 (P6) or port mode register 6 (PM6). Outside the period of 3 clocks following execution a read-out instruction, the current is −3 μA (MAX.).

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T$_A$ = –40 to +85°C, V$_{DD}$ = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Supply current Note 1	I$_{DD1}$	10.00-MHz crystal oscillation operation mode	V$_{DD}$ = 5.0 V ± 10 % Note 2		12.0	24.0	mA
			V$_{DD}$ = 3.0 V ± 10 % Note 3		1.4	2.8	mA
	I$_{DD2}$	10.00-MHz crystal oscillation HALT mode	V$_{DD}$ = 5.0 V ± 10 % Note 2		4.0	8.0	mA
			V$_{DD}$ = 3.0 V ± 10 % Note 3		1.4	2.8	mA
	I$_{DD3}$	32.768-kHz crystal oscillation operation mode Note 4	V$_{DD}$ = 5.0 V ± 10 %		150	300	μA
			V$_{DD}$ = 3.0 V ± 10 %		100	200	μA
			V$_{DD}$ = 2.0 V ± 10 %		60	120	μA
	I$_{DD4}$	32.768-kHz crystal oscillation HALT mode Note 4	V$_{DD}$ = 5.0 V ± 10 %		25	50	μA
			V$_{DD}$ = 3.0 V ± 10 %		5	15	μA
			V$_{DD}$ = 2.0 V ± 10 %		2.5	10	μA
	I$_{DD5}$	XT1 = V$_{DD}$ STOP mode when using feedback resistor	V$_{DD}$ = 5.0 V ± 10 %		2.0	30	μA
			V$_{DD}$ = 3.0 V ± 10 %		1.0	10	μA
			V$_{DD}$ = 2.0 V ± 10 %		0.5	10	μA
	I$_{DD6}$	XT1 = V$_{DD}$ STOP mode when not using feedback resistor	V$_{DD}$ = 5.0 V ± 10 %		0.1	30	μA
			V$_{DD}$ = 3.0 V ± 10 %		0.05	10	μA
			V$_{DD}$ = 2.0 V ± 10 %		0.05	10	μA

Notes 1. Refers to the current flowing to the V$_{DD}$ pin. The current flowing to the on-chip pull-up resistors, ports, and A/D converter is not included.

2. When operating at high-speed mode (when the processor clock control register (PCC) is set to 00H)

3. When operating at low-speed mode (when PCC is set to 04H)

4. When main system clock operation stopped.

AC Characteristics

(1) Basic Operation (T$_A$ = –40 to +85°C, V$_{DD}$ = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T$_{CY}$	Operating with main system clock	3.5 V ≤ V$_{DD}$ ≤ 5.5 V	0.4		64	μs
			2.7 V ≤ V$_{DD}$ < 3.5 V	0.8		64	μs
			1.8 V ≤ V$_{DD}$ < 2.7 V	2.0		64	μs
		Operating with subsystem clock		40 **Note 1**	122	125	μs
TI0 input high-/low-level width	t$_{TIH0}$, t$_{TIL0}$	3.5 V ≤ V$_{DD}$ ≤ 5.5 V		2/f$_{sam}$+0.1 **Note 2**			μs
		2.7 V ≤ V$_{DD}$ < 3.5 V		2/f$_{sam}$+0.2 **Note 2**			μs
		1.8 V ≤ V$_{DD}$ < 2.7 V		2/f$_{sam}$+0.5 **Note 2**			μs
TI1, TI2 input frequency	f$_{TI1}$	V$_{DD}$ = 4.5 to 5.5 V		0		4	MHz
				0		275	kHz
TI1, TI2 input high-/low-level width	t$_{TIH1}$, t$_{TIL1}$	V$_{DD}$ = 4.5 to 5.5 V		100			ns
				1.8			μs
Interrupt request input high-/low-level width	t$_{INTH}$, t$_{INTL}$	INTP0	3.5 V ≤ V$_{DD}$ ≤ 5.5 V	2/f$_{sam}$+0.1 **Note 2**			μs
			2.7 V ≤ V$_{DD}$ < 3.5 V	2/f$_{sam}$+0.2 **Note 2**			μs
			1.8 V ≤ V$_{DD}$ < 2.7 V	2/f$_{sam}$+0.5 **Note 2**			μs
		INTP1 to INTP3, KR0 to KR7	V$_{DD}$ = 2.7 to 5.5 V	10			μs
				20			μs
$\overline{\text{RESET}}$ low-level width	t$_{RSL}$	V$_{DD}$ = 2.7 to 5.5 V		10			μs
				20			μs

Notes 1. Value when an external clock is used. This value is 114 μs (MIN.) when a crystal resonator is used.

2. In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register (SCS), selection of f$_{sam}$ is possible between f$_X$/2^{N+1}, f$_X$/64, and f$_X$/128 (when N= 0 to 4).

T$_{CY}$ vs. V$_{DD}$ (At main system clock operation)
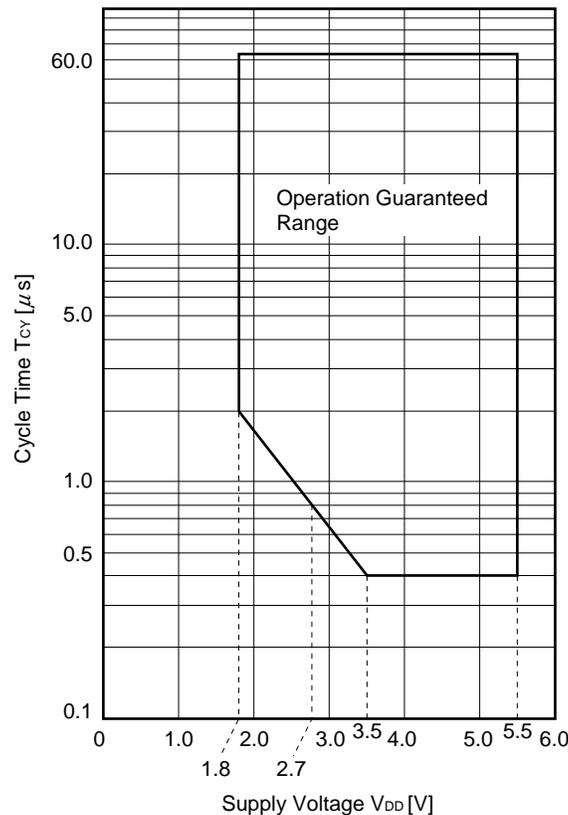
(2) Read/Write Operation (T$_A$ = –40 to +85°C, V$_{DD}$ = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t$_{ASTH}$		0.5t$_{CY}$		ns
Address setup time	t$_{ADS}$		0.5t$_{CY}$–30		ns
Address hold time	t$_{ADH}$		50		ns
Data input time from address	t$_{ADD1}$			(2.5+2n)t$_{CY}$–50	ns
	t$_{ADD2}$			(3+2n)t$_{CY}$–100	ns
Data input time from $\overline{RD}$↓	t$_{RDD1}$			(1+2n)t$_{CY}$–25	ns
	t$_{RDD2}$			(2.5+2n)t$_{CY}$–100	ns
Read data hold time	t$_{RDH}$		0		ns
$\overline{RD}$ low-level width	t$_{RDL1}$		(1.5+2n)t$_{CY}$–20		ns
	t$_{RDL2}$		(2.5+2n)t$_{CY}$–20		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t$_{RDWT1}$			0.5t$_{CY}$	ns
	t$_{RDWT2}$			1.5t$_{CY}$	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t$_{WRWT}$			0.5t$_{CY}$	ns
$\overline{WAIT}$ low-level width	t$_{WTL}$		(0.5+2n)t$_{CY}$+10	(2+2n)t$_{CY}$	ns
Write data setup time	t$_{WDS}$		100		ns
Write data hold time	t$_{WDH}$	Load resistance ≥ 5 kΩ	20		ns
$\overline{WR}$ low-level width	t$_{WRL}$		(2.5+2n)t$_{CY}$ –20		ns
$\overline{RD}$↓ delay time from ASTB↓	t$_{ASTRD}$		0.5t$_{CY}$–30		ns
$\overline{WR}$↓ delay time from ASTB↓	t$_{ASTWR}$		1.5t$_{CY}$–30		ns
ASTB↑ delay time from $\overline{RD}$↑ in external fetch	t$_{RDAST}$		t$_{CY}$–10	t$_{CY}$+40	ns
Address hold time from $\overline{RD}$↑ in external fetch	t$_{RDADH}$		t$_{CY}$	t$_{CY}$+50	ns
Write data output time from $\overline{RD}$↑	t$_{RDWD}$	V$_{DD}$ = 4.5 to 5.5 V	0.5t$_{CY}$+5	0.5t$_{CY}$+30	ns
			0.5t$_{CY}$+15	0.5t$_{CY}$+90	ns
Write data output time from $\overline{WR}$↓	t$_{WRWD}$	V$_{DD}$ = 4.5 to 5.5 V	5	30	ns
			15	90	ns
Address hold time from $\overline{WR}$↑	t$_{WRADH}$	V$_{DD}$ = 4.5 to 5.5 V	t$_{CY}$	t$_{CY}$+60	ns
			t$_{CY}$	t$_{CY}$+100	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t$_{WTRD}$		0.5t$_{CY}$	2.5t$_{CY}$+80	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t$_{WTWR}$		0.5t$_{CY}$	2.5t$_{CY}$+80	ns

Remarks 1. t$_{CY}$ = T$_{CY}$/4

2. n indicates the number of waits.

(3) Serial Interface (T$_A$ = –40 to +85°C, V$_{DD}$ = 1.8 to 5.5 V)

    (a) Serial Interface Channel 0

        (i) 3-wire serial I/O mode ($\overline{\text{SCK0}}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t$_{KCY1}$	4.5 V ≤ V$_{DD}$ ≤ 5.5 V	800			ns
		2.7 V ≤ V$_{DD}$ < 4.5 V	1600			ns
		2.0 V ≤ V$_{DD}$ < 2.7 V	3200			ns
			4800			ns
$\overline{\text{SCK0}}$ high-/low-level width	t$_{KH1}$, t$_{KL1}$	V$_{DD}$ = 4.5 to 5.5 V	t$_{KCY1}$/2–50			ns
			t$_{KCY1}$/2–100			ns
SI0 setup time (to $\overline{\text{SCK0}}$↑)	t$_{SIK1}$	4.5 V ≤ V$_{DD}$ ≤ 5.5 V	100			ns
		2.7 V ≤ V$_{DD}$ < 4.5 V	150			ns
		2.0 V ≤ V$_{DD}$ < 2.7 V	300			ns
			400			ns
SI0 hold time (from $\overline{\text{SCK0}}$↑)	t$_{KSI1}$		400			ns
SO0 output delay time from $\overline{\text{SCK0}}$↓	t$_{KSO1}$	C = 100 pF **Note**			300	ns

Note C is the load capacitance of $\overline{\text{SCK0}}$ and SO0 output lines.

        (ii) 3-wire serial I/O mode ($\overline{\text{SCK0}}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t$_{KCY2}$	4.5 V ≤ V$_{DD}$ ≤ 5.5 V		800			ns
		2.7 V ≤ V$_{DD}$ < 4.5 V		1600			ns
		2.0 V ≤ V$_{DD}$ < 2.7 V		3200			ns
				4800			ns
$\overline{\text{SCK0}}$ high-/low-level width	t$_{KH2}$, t$_{KL2}$	4.5 V ≤ V$_{DD}$ ≤ 5.5 V		400			ns
		2.7 V ≤ V$_{DD}$ < 4.5 V		800			ns
		2.0 V ≤ V$_{DD}$ < 2.7 V		1600			ns
				2400			ns
SI0 setup time (to $\overline{\text{SCK0}}$↑)	t$_{SIK2}$	V$_{DD}$ = 2.0 to 5.5 V		100			ns
				150			ns
SI0 hold time (from $\overline{\text{SCK0}}$↑)	t$_{KSI2}$			400			ns
SO0 output delay time from $\overline{\text{SCK0}}$↓	t$_{KSO2}$	C = 100 pF **Note**	V$_{DD}$ = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{\text{SCK0}}$ rise/fall time	t$_{R2}$, t$_{F2}$	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note C is the load capacitance of SO0 output line.

(iii) 2-wire serial I/O mode ($\overline{\text{SCK0}}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{KCY3}	R = 1 kΩ, C = 100 pF **Note**	2.7 V ≤ V_{DD} ≤ 5.5 V	1600			ns
			2.0 V ≤ V_{DD} < 2.7 V	3200			ns
				4800			ns
$\overline{\text{SCK0}}$ high-level width	t_{KH3}		V_{DD} = 2.7 to 5.5 V	t_{KCY3}/2−160			ns
				t_{KCY3}/2−190			ns
$\overline{\text{SCK0}}$ low-level width	t_{KL3}		V_{DD} = 4.5 to 5.5 V	t_{KCY3}/2−50			ns
				t_{KCY3}/2−100			ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}$↑)	t_{SIK3}		4.5 V ≤ V_{DD} ≤ 5.5 V	300			ns
			2.7 V ≤ V_{DD} < 4.5 V	350			ns
			2.0 V ≤ V_{DD} < 2.7 V	400			ns
				500			ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}$↑)	t_{KSI3}			600			ns
SB0, SB1 output delay time from $\overline{\text{SCK0}}$↓	t_{KSO3}			0		300	ns

Note R and C are the load resistance and load capacitance of the $\overline{\text{SCK0}}$, SB0, and SB1 output lines.

(iv) 2-wire serial I/O mode ($\overline{\text{SCK0}}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{KCY4}	2.7 V ≤ V_{DD} ≤ 5.5 V		1600			ns
		2.0 V ≤ V_{DD} < 2.7 V		3200			ns
				4800			ns
$\overline{\text{SCK0}}$ high-level width	t_{KH4}	2.7 V ≤ V_{DD} ≤ 5.5 V		650			ns
		2.0 V ≤ V_{DD} < 2.7 V		1300			ns
				2100			ns
$\overline{\text{SCK0}}$ low-level width	t_{KL4}	2.7 V ≤ V_{DD} ≤ 5.5 V		800			ns
		2.0 V ≤ V_{DD} < 2.7 V		1600			ns
				2400			ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}$↑)	t_{SIK4}	V_{DD} = 2.0 to 5.5 V		100			ns
				150			ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}$↑)	t_{KSI4}			t_{KCY4}/2			ns
SB0, SB1 output delay time from $\overline{\text{SCK0}}$↓	t_{KSO4}	R = 1 kΩ, C = 100 pF **Note**	4.5 V ≤ V_{DD} ≤ 5.5 V	0		300	ns
			2.0 V ≤ V_{DD} < 4.5 V	0		500	ns
				0		800	ns
$\overline{\text{SCK0}}$ rise/fall time	t_{R4}, t_{F4}	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output lines.

(v) I²C bus mode (SCL... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t$_{KCY5}$	R = 1 kΩ, C = 100 pF **Note**	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	10			μs
			2.0 V ≤ V$_{DD}$ < 2.7 V	20			μs
				30			μs
SCL high-level width	t$_{KH5}$		V$_{DD}$ = 2.7 to 5.5 V	t$_{KCY5}$–160			ns
				t$_{KCY5}$–190			ns
SCL low-level width	t$_{KL5}$		V$_{DD}$ = 4.5 to 5.5 V	t$_{KCY5}$–50			ns
				t$_{KCY5}$–100			ns
SDA0, SDA1 setup time (to SCL↑)	t$_{SIK5}$		2.7 V ≤ V$_{DD}$ ≤ 5.5 V	200			ns
			2.0 V ≤ V$_{DD}$ < 2.7 V	300			ns
				400			ns
SDA0, SDA1 hold time (from SCL↓)	t$_{KSI5}$			0			ns
SDA0, SDA1 output delay time from SCL↓	t$_{KSO5}$		4.5 V ≤ V$_{DD}$ ≤ 5.5 V	0		300	ns
			2.0 V ≤ V$_{DD}$ < 4.5 V	0		500	ns
				0		600	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL↑	t$_{KSB}$			200			ns
SCL↓ from SDA0, SDA1↓	t$_{SBK}$		V$_{DD}$ = 2.0 to 5.5 V	400			ns
				500			ns
SDA0, SDA1 high-level width	t$_{SBH}$			500			ns

Note R and C are the load resistance and load capacitance of the SCL, SDA0, and SDA1 output lines.

(vi) I²C bus mode (SCL... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t$_{KCY6}$			1000			ns
SCL high-/low-level width	t$_{KH6}$, t$_{KL6}$	V$_{DD}$ = 2.0 to 5.5 V		400			ns
				600			ns
SDA0, SDA1 setup time (to SCL↑)	t$_{SIK6}$	V$_{DD}$ = 2.0 to 5.5 V		200			ns
				300			ns
SDA0, SDA1 hold time (from SCL↓)	t$_{KSI6}$			0			ns
SDA0, SDA1 output delay time from SCL↓	t$_{KSO6}$	R = 1 kΩ, C = 100 pF **Note**	4.5 V ≤ V$_{DD}$ ≤ 5.5 V	0		300	ns
			2.0 V ≤ V$_{DD}$ < 4.5 V	0		500	ns
				0		600	ns
SDA0, SDA1↓ from SCL↑ or SDA0, SDA1↑ from SCL↑	t$_{KSB}$			200			ns
SCL↓ from SDA0, SDA1↓	t$_{SBK}$	V$_{DD}$ = 2.0 to 5.5 V		400			ns
				500			ns
SDA0, SDA1 high-level width	t$_{SBH}$	V$_{DD}$ = 2.0 to 5.5 V		500			ns
				800			ns
SCL rise/fall time	t$_{R6}$, t$_{F6}$	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note R and C are the load resistance and load capacitance of the SDA0 and SDA1 output lines.

(b) Serial Interface Channel 1

(i) 3-wire serial I/O mode ($\overline{\text{SCK1}}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY7}	4.5 V ≤ V_DD ≤ 5.5 V		800			ns
		2.7 V ≤ V_DD < 4.5 V		1600			ns
		2.0 V ≤ V_DD < 2.7 V		3200			ns
				4800			ns
$\overline{\text{SCK1}}$ high-/low-level width	t_{KH7}, t_{KL7}	V_DD = 4.5 to 5.5 V		$t_{KCY7}/2-50$			ns
				$t_{KCY7}/2-100$			ns
SI1 setup time (to $\overline{\text{SCK1}}\uparrow$)	t_{SIK7}	4.5 V ≤ V_DD ≤ 5.5 V		100			ns
		2.7 V ≤ V_DD < 4.5 V		150			ns
		2.0 V ≤ V_DD < 2.7 V		300			ns
				400			ns
SI1 hold time (from $\overline{\text{SCK1}}\uparrow$)	t_{KSI7}			400			ns
SO1 output delay time from $\overline{\text{SCK1}}\downarrow$	t_{KSO7}	C = 100 pF **Note**				300	ns

Note   C is the load capacitance of $\overline{\text{SCK1}}$ and SO1 output lines.

(ii) 3-wire serial I/O mode ($\overline{\text{SCK1}}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY8}	4.5 V ≤ V_DD ≤ 5.5 V		800			ns
		2.7 V ≤ V_DD < 4.5 V		1600			ns
		2.0 V ≤ V_DD < 2.7 V		3200			ns
				4800			ns
$\overline{\text{SCK1}}$ high-/low-level width	t_{KH8}, t_{KL8}	4.5 V ≤ V_DD ≤ 5.5 V		400			ns
		2.7 V ≤ V_DD < 4.5 V		800			ns
		2.0 V ≤ V_DD < 2.7 V		1600			ns
				2400			ns
SI1 setup time (to $\overline{\text{SCK1}}\uparrow$)	t_{SIK8}	V_DD = 2.0 to 5.5 V		100			ns
				150			ns
SI1 hold time (from $\overline{\text{SCK1}}\uparrow$)	t_{KSI8}			400			ns
SO1 output delay time from $\overline{\text{SCK1}}\downarrow$	t_{KSO8}	C = 100 pF **Note**	V_DD = 2.0 to 5.5 V			300	ns
						500	ns
$\overline{\text{SCK1}}$ rise/fall time	t_{R8}, t_{F8}	When external device expansion function is used				160	ns
		When external device expansion function is not used	When 16-bit timer output function is used			700	ns
			When 16-bit timer output function is not used			1000	ns

Note   C is the load capacitance of the SO1 output line.

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{\text{SCK1}}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY9}	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	800			ns
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$	1600			ns
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$	3200			ns
			4800			ns
$\overline{\text{SCK1}}$ high-/low-level width	t_{KH9}, t_{KL9}	$V_{DD} = 4.5$ to 5.5 V	$t_{KCY9}/2{-}50$			ns
			$t_{KCY9}/2{-}100$			ns
SI1 setup time (to $\overline{\text{SCK1}}\uparrow$)	t_{SIK9}	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	100			ns
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$	150			ns
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$	300			ns
			400			ns
SI1 hold time (from $\overline{\text{SCK1}}\uparrow$)	t_{KSI9}		400			ns
SO1 output delay time from $\overline{\text{SCK1}}\downarrow$	t_{KSO9}	$C = 100\text{ pF}$ **Note**			300	ns
$\overline{\text{STB}}\uparrow$ from $\overline{\text{SCK1}}\uparrow$	t_{SBD}		$t_{KCY9}/2{-}100$		$t_{KCY9}/2{+}100$	ns
Strobe signal high-level width	t_{SBW}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$t_{KCY9}{-}30$		$t_{KCY9}{+}30$	ns
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$	$t_{KCY9}{-}60$		$t_{KCY9}{+}60$	ns
			$t_{KCY9}{-}90$		$t_{KCY9}{+}90$	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	$4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	100			ns
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$	150			ns
		$2.0\text{ V} \leq V_{DD} < 2.7\text{ V}$	200			ns
			300			ns
$\overline{\text{SCK1}}\downarrow$ from busy inactive	t_{SPS}				$2t_{KCY9}$	ns

Note   C is the load capacitance of the $\overline{\text{SCK1}}$ and SO1 output lines.

(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{\text{SCK1}}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY10}	$4.5 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$		800			ns
		$2.7 \text{ V} \leq V_{DD} < 4.5 \text{ V}$		1600			ns
		$2.0 \text{ V} \leq V_{DD} < 2.7 \text{ V}$		3200			ns
				4800			ns
$\overline{\text{SCK1}}$ high-/low-level width	t_{KH10}, t_{KL10}	$4.5 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$		400			ns
		$2.7 \text{ V} \leq V_{DD} < 4.5 \text{ V}$		800			ns
		$2.0 \text{ V} \leq V_{DD} < 2.7 \text{ V}$		1600			ns
				2400			ns
SI1 setup time (to $\overline{\text{SCK1}}\uparrow$)	t_{SIK10}	$V_{DD} = 2.0 \text{ to } 5.5 \text{ V}$		100			ns
				150			ns
SI1 hold time (from $\overline{\text{SCK1}}\uparrow$)	t_{KSI10}			400			ns
SO1 output delay time from $\overline{\text{SCK1}}\downarrow$	t_{KSO10}	$C = 100 \text{ pF }$ **Note**	$V_{DD} = 2.0 \text{ to } 5.5 \text{ V}$			300	ns
						500	ns
$\overline{\text{SCK1}}$ rise/fall time	t_{R10}, t_{F10}	When external device expansion function is used				160	ns
		When external device expansion function is not used				1000	ns

Note   C is the load capacitance of the SO1 output line.

AC Timing Test Point (Excluding X1, XT1 Input)

```
        0.8 V_DD                          0.8 V_DD
                    Test Points
        0.2 V_DD                          0.2 V_DD
```

Clock Timing

X1 Input

$1/f_X$

t_{XL} t_{XH}

V_{IH4} (MIN.)
V_{IL4} (MAX.)

XT1 Input

$1/f_{XT}$

t_{XTL} t_{XTH}

V_{IH5} (MIN.)
V_{IL5} (MAX.)

TI Timing

TI0

t_{TIL0} t_{TIH0}

TI1,TI2

$1/f_{TI1}$

t_{TIL1} t_{TIH1}
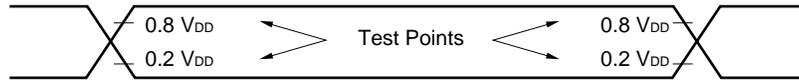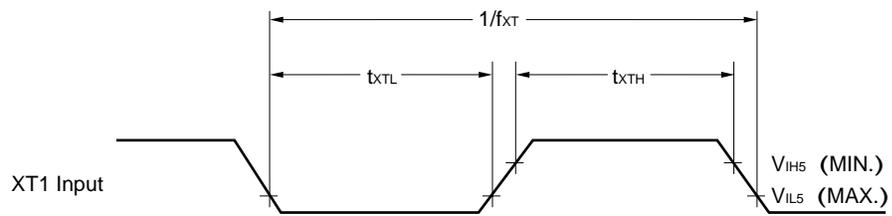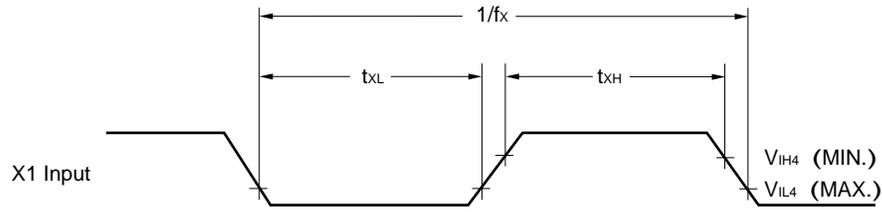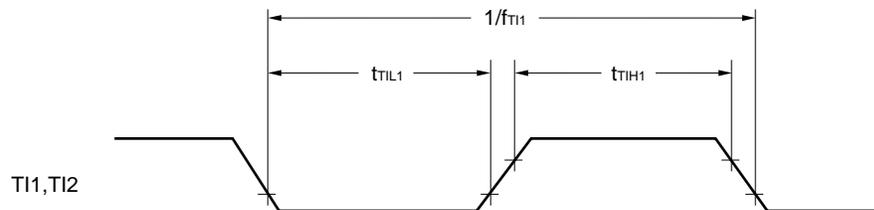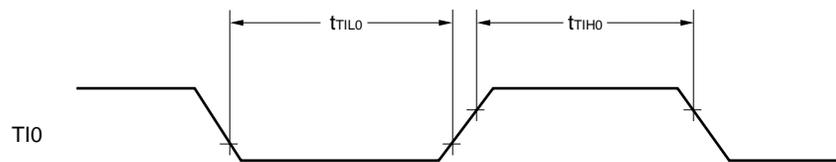
Read/Write Operation

External fetch (No wait):

A8 to A15 — Higher 8-Bit Address

t$_{ADD1}$

AD0 to AD7 — Lower 8-Bit Address — Hi-Z — Operation Code

t$_{ADS}$ t$_{ADH}$ t$_{RDD1}$ t$_{RDADH}$

t$_{ASTH}$ t$_{RDAST}$

ASTB

$\overline{RD}$

t$_{ASTRD}$ t$_{RDL1}$ t$_{RDH}$
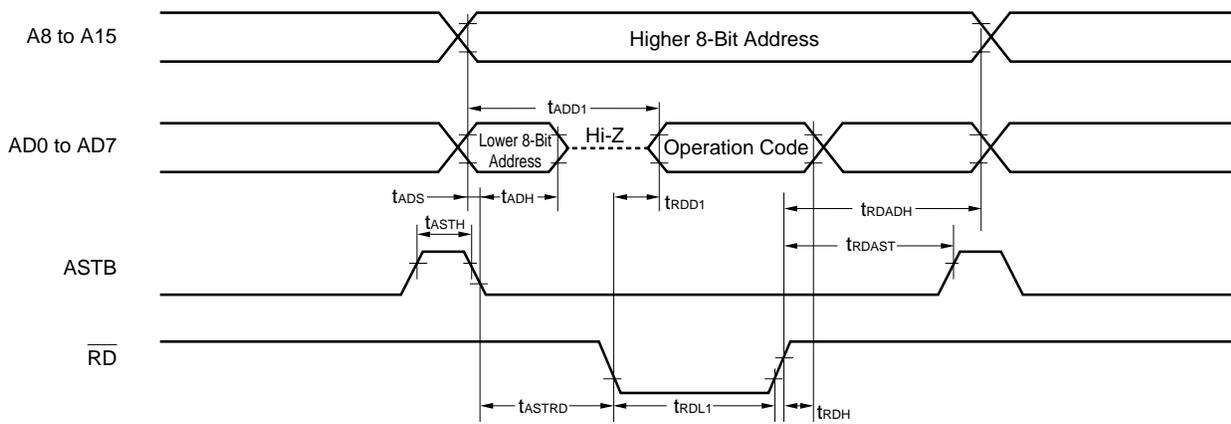
External fetch (Wait insertion):

A8 to A15 — Higher 8-Bit Address

t$_{ADD1}$

AD0 to AD7 — Lower 8-Bit Address — Hi-Z — Operation Code

t$_{ADS}$ t$_{ADH}$ t$_{RDD1}$ t$_{RDADH}$

t$_{ASTH}$ t$_{RDAST}$

ASTB

$\overline{RD}$

t$_{ASTRD}$ t$_{RDL1}$ t$_{RDH}$

$\overline{WAIT}$

t$_{RDWT1}$ t$_{WTL}$ t$_{WTRD}$
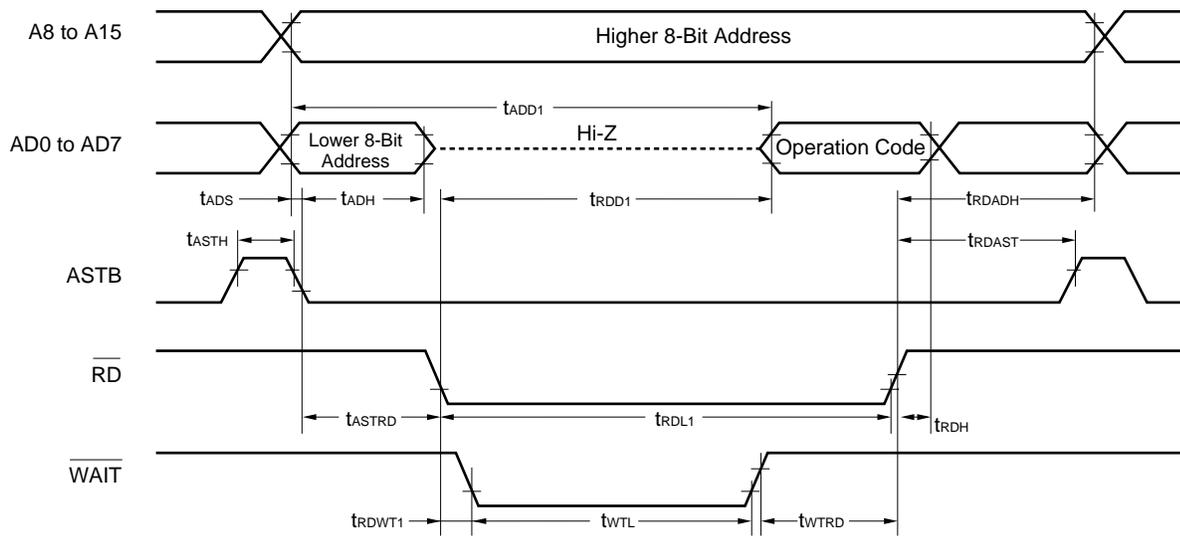
External data access (No wait):

A8 to A15 — Higher 8-Bit Address

AD0 to AD7 — Lower 8-Bit Address / Hi-Z / Read Data / Hi-Z / Write Data / Hi-Z

t_{ADD2}

t_{ADS} t_{ADH} t_{RDD2}

ASTB

t_{ASTH} t_{RDH}

RD

t_{ASTRD} t_{RDL2} t_{RDWD} t_{WDS} t_{WDH}

t_{WRWD} t_{WRADH}

WR

t_{ASTWR} t_{WRL}
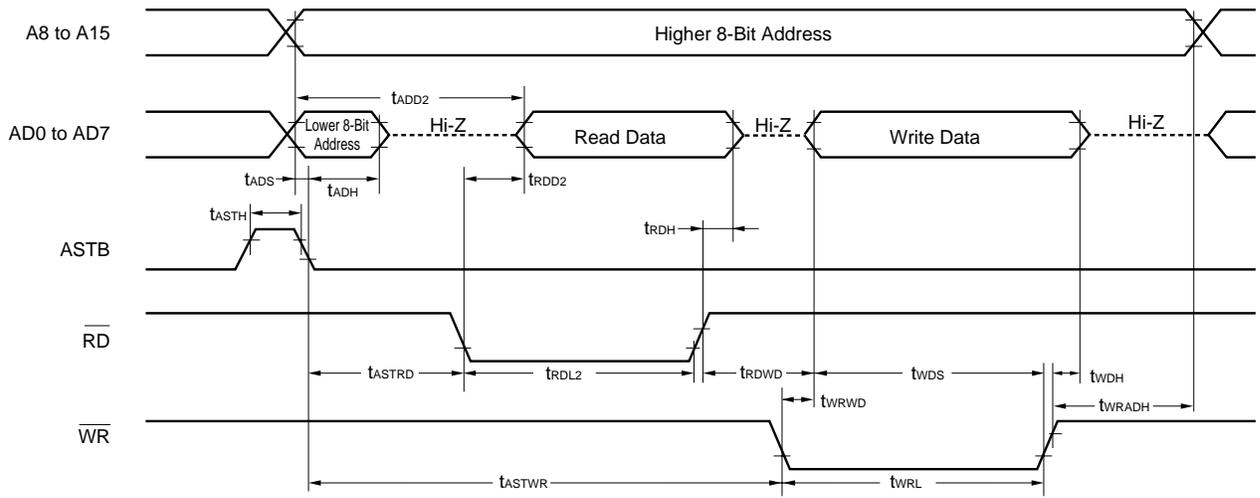
External data access (Wait insertion):

A8 to A15 — Higher 8-Bit Address

AD0 to AD7 — Lower 8-Bit Address / Hi-Z / Read Data / Hi-Z / Write Data / Hi-Z

t_{ADD2}

t_{ADS} t_{ADH} t_{RDD2} t_{RDH}

ASTB

t_{ASTH}

t_{ASTRD}

RD

t_{RDL2} t_{RDWD} t_{WDS} t_{WDH}

t_{WRWD}

WR

t_{ASTWR} t_{WRL} t_{WRADH}

WAIT

t_{RDWT2} t_{WTL} t_{WTRD} t_{WTL} t_{WTWR}

t_{WRWT}
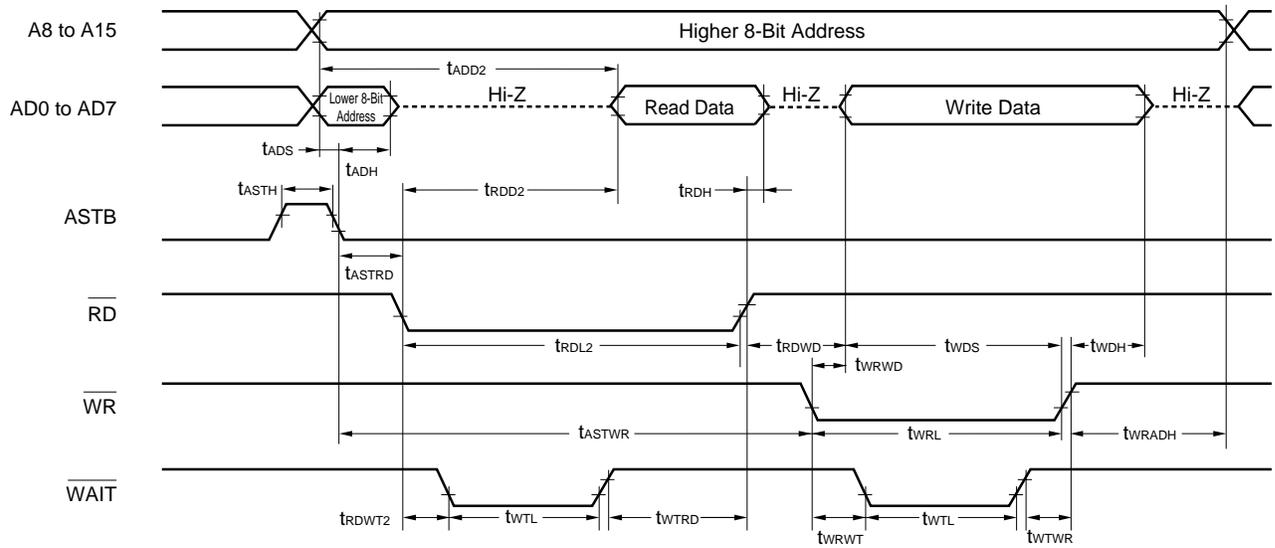
Serial Transfer Timing

3-wire serial I/O mode:
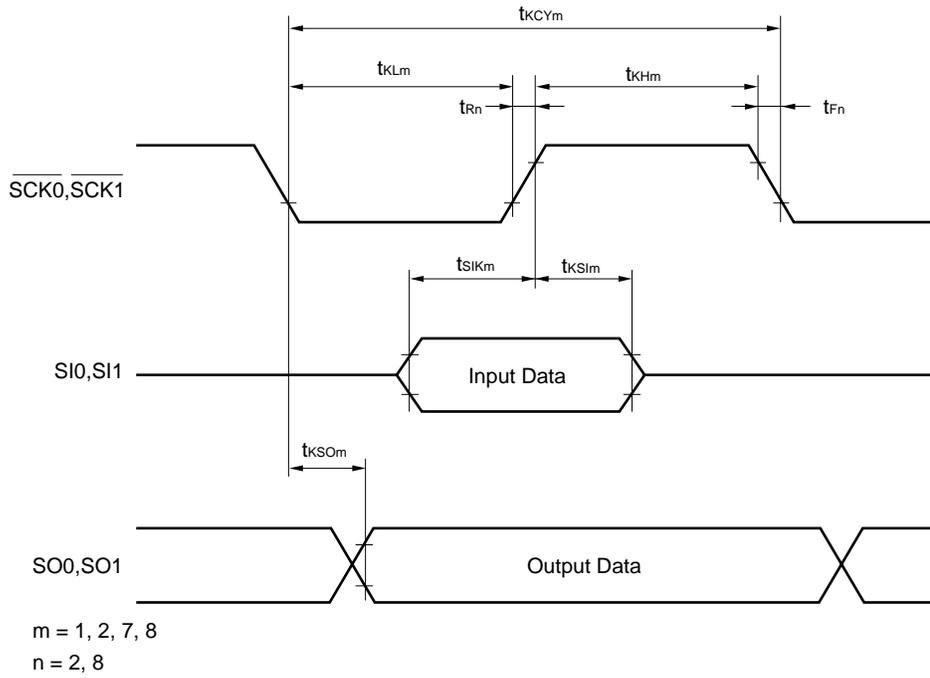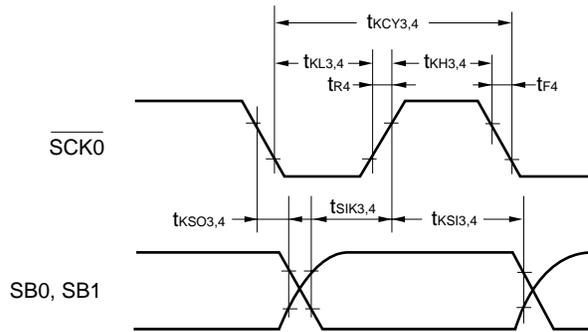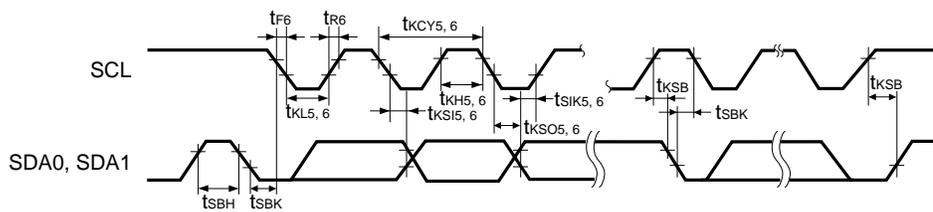
t_{KCYm}

t_{KLm}

t_{KHm}

t_{Rn}

t_{Fn}

$\overline{SCK0}, \overline{SCK1}$

t_{SIKm}

t_{KSIm}

SI0, SI1

Input Data

t_{KSOm}

SO0, SO1

Output Data

m = 1, 2, 7, 8
n = 2, 8

2-wire serial I/O mode:

$t_{KCY3,4}$

$t_{KL3,4}$

$t_{KH3,4}$

t_{R4}

t_{F4}

$\overline{SCK0}$

$t_{KSO3,4}$

$t_{SIK3,4}$

$t_{KSI3,4}$

SB0, SB1

I^{2}C bus mode:

t_{F6}

t_{R6}

$t_{KCY5,6}$

SCL

$t_{KH5,6}$

$t_{SIK5,6}$

t_{KSB}

t_{KSB}

$t_{KL5,6}$

$t_{KSI5,6}$

$t_{KSO5,6}$

t_{SBK}

SDA0, SDA1

t_{SBH}

t_{SBK}

3-wire serial I/O mode with automatic transmit/receive function:

SO1 D2 D1 D0 D7

SI1 D2 D1 D0 D7

$t_{SIK9,10}$ $t_{KSI9,10}$

$t_{KSO9,10}$ $t_{KH9,10}$ t_{F10}

SCK1

$t_{KL9,10}$ t_{R10} t_{SBD} t_{SBW}

$t_{KCY9,10}$

STB
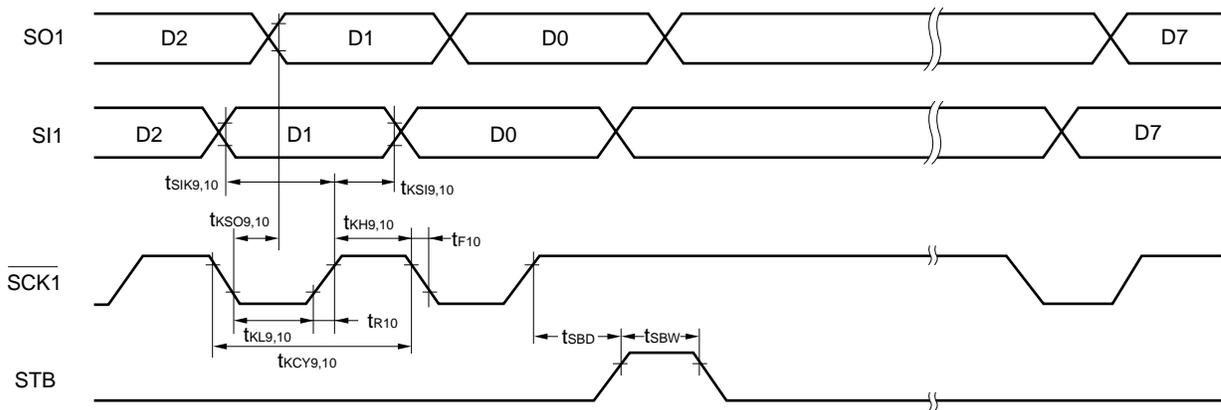
3-wire serial I/O mode with automatic transmit/receive function (busy processing):

SCK1 7 8 9[Note] 10[Note] 10 + n[Note] 1

t_{BYS} t_{BYH} t_{SPS}

BUSY
(Active High)
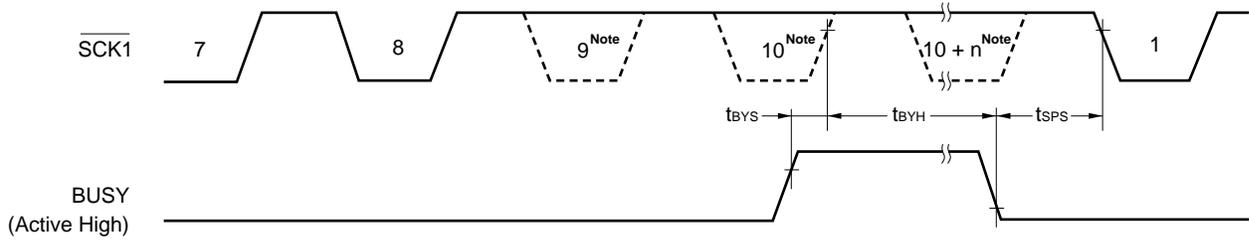
Note The signal is not actually driven low here; it is shown as such to indicate the timing.

A/D Converter Characteristics (T_A = −40 to +85°C, AV_{DD} = V_{DD} = 2.2 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error **Note**		$2.7 \text{ V} \leq AV_{REF} \leq AV_{DD}$			0.6	%
		$2.2 \text{ V} \leq AV_{REF} < 2.7 \text{ V}$			1.4	%
Conversion time	t_{CONV}	$2.7 \text{ V} \leq AV_{REF} \leq AV_{DD}$	19.1		200	μs
		$2.2 \text{ V} \leq AV_{REF} < 2.7 \text{ V}$	38.2		200	μs
Sampling time	t_{SAMP}		$24/f_X$			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		2.2		AV_{DD}	V
AV_{REF} resistance	R_{AIREF}		4	14		kΩ

★

Note Overall error excluding quantization error (±1/2 LSB). It is indicated as a ratio to the full-scale value.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = −40 to +85°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8 V Subsystem clock stops and feedback resistor disconnected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{18}/f_X$		ms
		Release by interrupt request		**Note**		ms

Note In combination with bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS), selection of $2^{13}/f_X$ and $2^{15}/f_X$ to $2^{18}/f_X$ is possible.

Data Retention Timing (STOP Mode Release by $\overline{RESET}$)
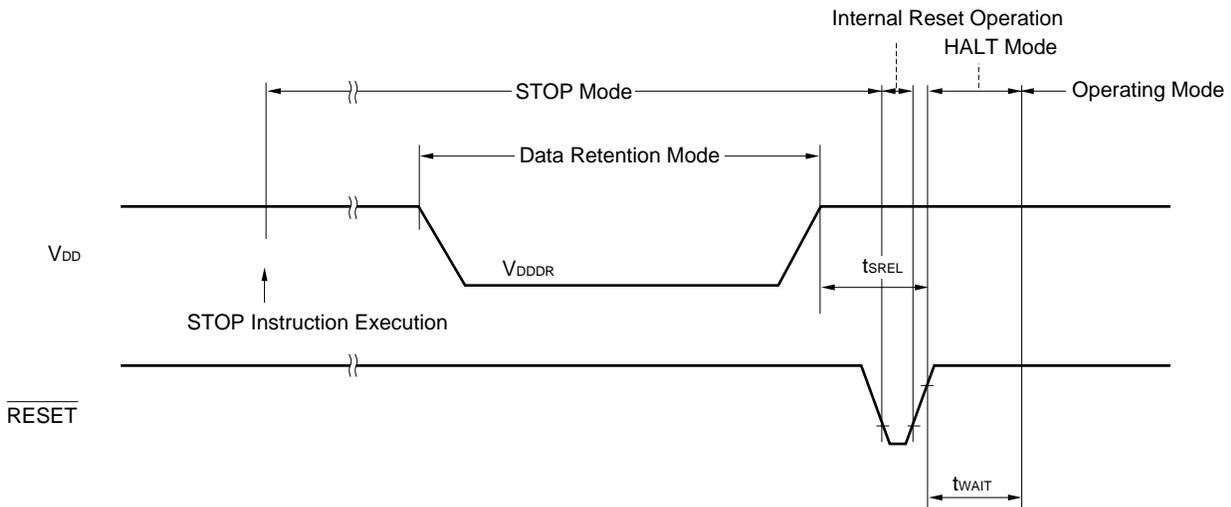
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)
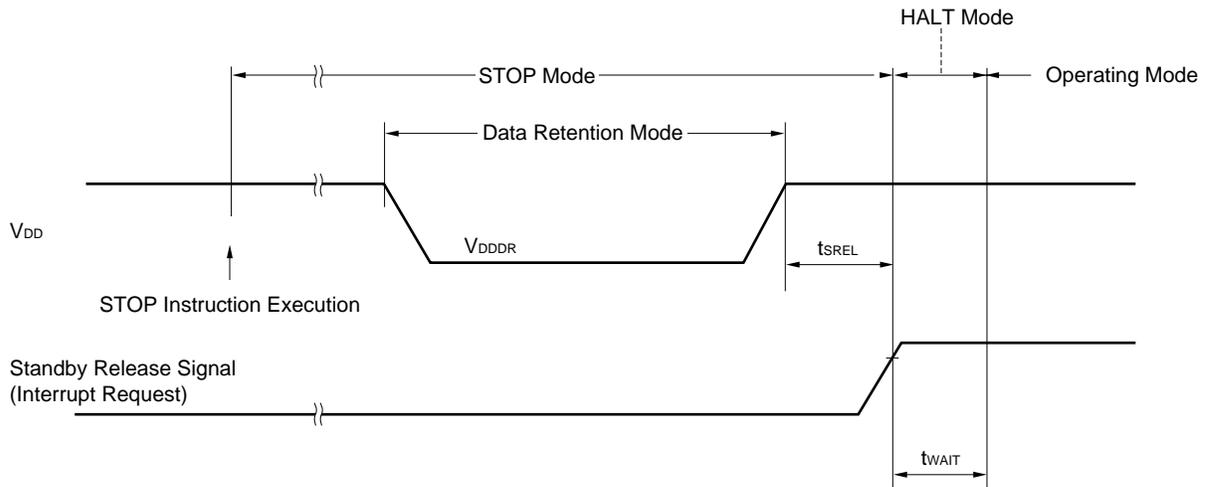
Interrupt Input Request Timing

INTP0 to INTP2

INTP3
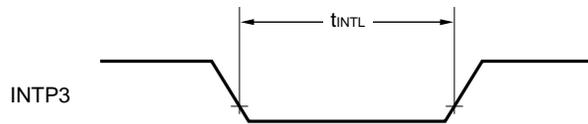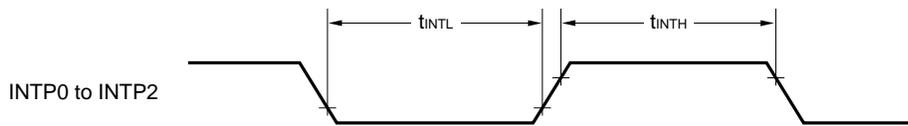
RESET Input Timing

RESET
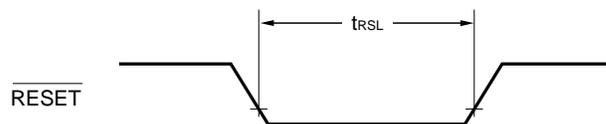
PROM PROGRAMMING CHARACTERISTICS

DC Characteristics

(1) PROM Write Mode (T$_A$ = 25 $\pm$ 5°C, V$_{DD}$ = 6.5 $\pm$ 0.25 V, V$_{PP}$ = 12.5 $\pm$ 0.3 V)

Parameter	Symbol	Symbol [Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V$_{IH}$	V$_{IH}$		0.7V$_{DD}$		V$_{DD}$	V
Input voltage, low	V$_{IL}$	V$_{IL}$		0		0.3V$_{DD}$	V
Output voltage, high	V$_{OH}$	V$_{OH}$	I$_{OH}$ = −1 mA	V$_{DD}$ − 1.0			V
Output voltage, low	V$_{OL}$	V$_{OL}$	I$_{OL}$ = 1.6 mA			0.4	V
Input leakage current	I$_{LI}$	I$_{LI}$	0 $\leq$ V$_{IN}$ $\leq$ V$_{DD}$	−10		+10	μA
V$_{PP}$ supply voltage	V$_{PP}$	V$_{PP}$		12.2	12.5	12.8	V
V$_{DD}$ supply voltage	V$_{DD}$	V$_{CC}$		6.25	6.5	6.75	V
V$_{PP}$ supply current	I$_{PP}$	I$_{PP}$	$\overline{PGM}$ = V$_{IL}$			50	mA
V$_{DD}$ supply current	I$_{DD}$	I$_{CC}$				50	mA

Note Corresponding μPD27C1001A symbol

(2) PROM Read Mode (T$_A$ = 25 $\pm$ 5°C, V$_{DD}$ = 5.0 $\pm$ 0.5 V, V$_{PP}$ = V$_{DD}$ $\pm$ 0.6 V)

Parameter	Symbol	Symbol [Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V$_{IH}$	V$_{IH}$		0.7V$_{DD}$		V$_{DD}$	V
Input voltage, low	V$_{IL}$	V$_{IL}$		0		0.3V$_{DD}$	V
Output voltage, high	V$_{OH1}$	V$_{OH1}$	I$_{OH}$ = −1 mA	V$_{DD}$ − 1.0			V
	V$_{OH2}$	V$_{OH2}$	I$_{OH}$ = −100 μA	V$_{DD}$ − 0.5			V
Output voltage, low	V$_{OL}$	V$_{OL}$	I$_{OL}$ = 1.6 mA			0.4	V
Input leakage current	I$_{LI}$	I$_{LI}$	0 $\leq$ V$_{IN}$ $\leq$ V$_{DD}$	−10		+10	μA
Output leakage current	I$_{LO}$	I$_{LO}$	0 $\leq$ V$_{OUT}$ $\leq$ V$_{DD}$, $\overline{OE}$ = V$_{IH}$	−10		+10	μA
V$_{PP}$ supply voltage	V$_{PP}$	V$_{PP}$		V$_{DD}$ − 0.6	V$_{DD}$	V$_{DD}$ + 0.6	V
V$_{DD}$ supply voltage	V$_{DD}$	V$_{CC}$		4.5	5.0	5.5	V
V$_{PP}$ supply current	I$_{PP}$	I$_{PP}$	V$_{PP}$ = V$_{DD}$			100	μA
V$_{DD}$ supply current	I$_{DD}$	I$_{CCA1}$	$\overline{CE}$ = V$_{IL}$, V$_{IN}$ = V$_{IH}$			50	mA

Note Corresponding μPD27C1001A symbol

AC Characteristics

(1) PROM Write Mode

(a) Page program mode (T$_A$ = 25 $\pm$ 5°C, V$_{DD}$ = 6.5 $\pm$ 0.25 V, V$_{PP}$ = 12.5 $\pm$ 0.3 V)

Parameter	Symbol	Symbol Note	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{OE}\downarrow$)	t$_{AS}$	t$_{AS}$		2			μs
$\overline{OE}$ setup time	t$_{OES}$	t$_{OES}$		2			μs
$\overline{CE}$ setup time (to $\overline{OE}\downarrow$)	t$_{CES}$	t$_{CES}$		2			μs
Input data setup time (to $\overline{OE}\downarrow$)	t$_{DS}$	t$_{DS}$		2			μs
Address hold time (from $\overline{OE}\uparrow$)	t$_{AH}$	t$_{AH}$		2			μs
	t$_{AHL}$	t$_{AHL}$		2			μs
	t$_{AHV}$	t$_{AHV}$		0			μs
Input data hold time (from $\overline{OE}\uparrow$)	t$_{DH}$	t$_{DH}$		2			μs
Data output float delay time from $\overline{OE}\uparrow$	t$_{DF}$	t$_{DF}$		0		250	ns
V$_{PP}$ setup time (to $\overline{OE}\downarrow$)	t$_{VPS}$	t$_{VPS}$		1.0			ms
V$_{DD}$ setup time (to $\overline{OE}\downarrow$)	t$_{VDS}$	t$_{VCS}$		1.0			ms
Program pulse width	t$_{PW}$	t$_{PW}$		0.095	0.1	0.105	ms
Valid data delay time from $\overline{OE}\downarrow$	t$_{OE}$	t$_{OE}$				1	μs
$\overline{OE}$ pulse width during data latching	t$_{LW}$	t$_{LW}$		1			μs
$\overline{PGM}$ setup time	t$_{PGMS}$	t$_{PGMS}$		2			μs
$\overline{CE}$ hold time	t$_{CEH}$	t$_{CEH}$		2			μs
$\overline{OE}$ hold time	t$_{OEH}$	t$_{OEH}$		2			μs

Note   Corresponding μPD27C1001A symbol

(b) Byte program mode (T$_A$ = 25 $\pm$ 5°C, V$_{DD}$ = 6.5 $\pm$ 0.25 V, V$_{PP}$ = 12.5 $\pm$ 0.3 V)

Parameter	Symbol	Symbol Note	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{PGM}\downarrow$)	t$_{AS}$	t$_{AS}$		2			μs
$\overline{OE}$ setup time	t$_{OES}$	t$_{OES}$		2			μs
$\overline{CE}$ setup time (to $\overline{PGM}\downarrow$)	t$_{CES}$	t$_{CES}$		2			μs
Input data setup time (to $\overline{PGM}\downarrow$)	t$_{DS}$	t$_{DS}$		2			μs
Address hold time (from $\overline{OE}\uparrow$)	t$_{AH}$	t$_{AH}$		2			μs
Input data hold time (from $\overline{PGM}\uparrow$)	t$_{DH}$	t$_{DH}$		2			μs
Data output float delay time from $\overline{OE}\uparrow$	t$_{DF}$	t$_{DF}$		0		250	ns
V$_{PP}$ setup time (to $\overline{PGM}\downarrow$)	t$_{VPS}$	t$_{VPS}$		1.0			ms
V$_{DD}$ setup time (to $\overline{PGM}\downarrow$)	t$_{VDS}$	t$_{VCS}$		1.0			ms
Program pulse width	t$_{PW}$	t$_{PW}$		0.095	0.1	0.105	ms
Valid data delay time from $\overline{OE}\downarrow$	t$_{OE}$	t$_{OE}$				1	μs
$\overline{OE}$ hold time	t$_{OEH}$	—		2			μs

Note   Corresponding μPD27C1001A symbol

(2) PROM Read Mode (T$_A$ = 25 $\pm$ 5°C, V$_{DD}$ = 5.0 $\pm$ 0.5 V, V$_{PP}$ = V$_{DD}$ $\pm$ 0.6 V)

Parameter	Symbol	Symbol Note	Test Conditions	MIN.	TYP.	MAX.	Unit
Data output time from address	t$_{ACC}$	t$_{ACC}$	$\overline{CE}$ = $\overline{OE}$ = V$_{IL}$			800	ns
Data output delay time from $\overline{CE}$↓	t$_{CE}$	t$_{CE}$	$\overline{OE}$ = V$_{IL}$			800	ns
Data output delay time from $\overline{OE}$↓	t$_{OE}$	t$_{OE}$	$\overline{CE}$ = V$_{IL}$			200	ns
Data output float delay time from $\overline{OE}$↑	t$_{DF}$	t$_{DF}$	$\overline{CE}$ = V$_{IL}$	0		60	ns
Data hold time from address	t$_{OH}$	t$_{OH}$	$\overline{CE}$ = $\overline{OE}$ = V$_{IL}$	0			ns

Note Corresponding μPD27C1001A symbol

(3) PROM Programming Mode Setting (T$_A$ = 25°C, V$_{SS}$ = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
PROM programming mode setup time	t$_{SMA}$		10			μs

PROM Write Mode Timing (Page program mode)
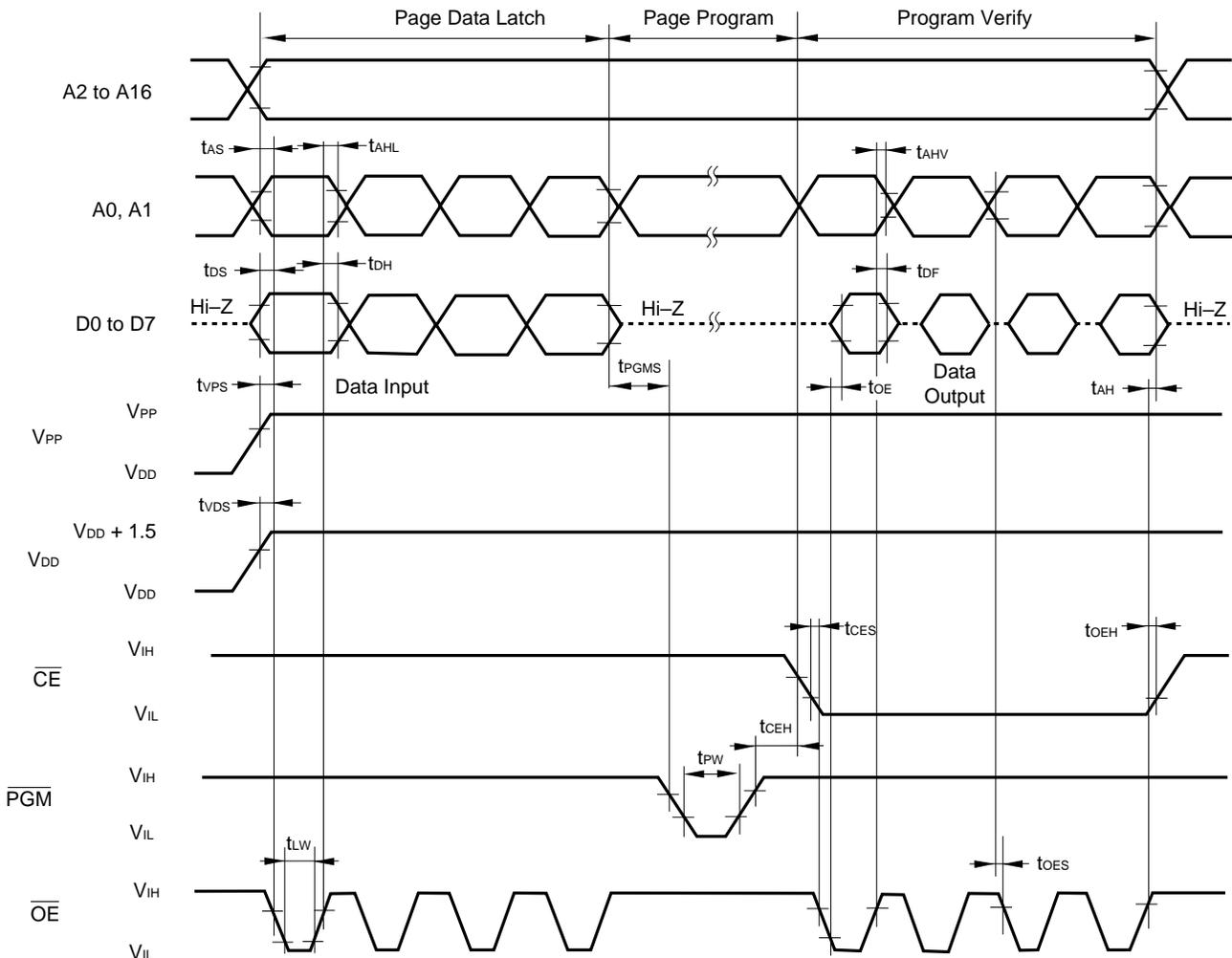
PROM Write Mode Timing (Byte program mode)

Program | Program Verify

A0 to A16

t_{AS} t_{DF}

D0 to D7   Hi-Z   Data Input   Hi-Z   Data Output   Hi-Z

t_{DS} t_{DH} t_{AH}

V_{PP} V_{PP} / V_{DD}

t_{VPS}

V_{DD} V_{DD} + 1.5 / V_{DD}

t_{VDS} t_{OEH}

$\overline{CE}$ V_{IH} / V_{IL}

t_{CES} t_{PW}

$\overline{PGM}$ V_{IH} / V_{IL}

t_{OES} t_{OE}

$\overline{OE}$ V_{IH} / V_{IL}
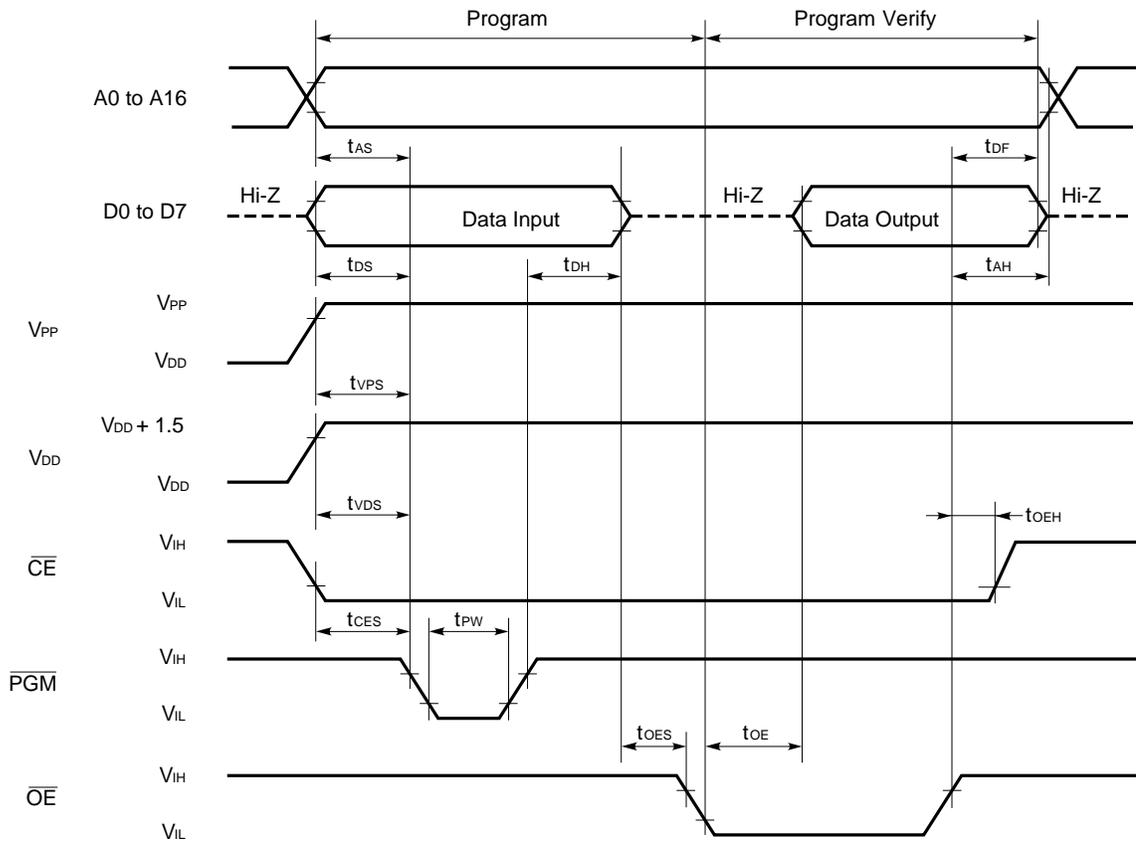
Cautions 1. V_DD must be applied before V_PP and cut off after V_PP.
2. V_PP must not exceed +13.5 V including overshoot.
3. Removing and reinserting while +12.5 V is applied to V_PP may adversely affect reliability.

PROM Read Mode Timing

A0 to A16   Effective Address

$\overline{CE}$ V_{IH} / V_{IL}

t_{CE}

$\overline{OE}$ V_{IH} / V_{IL}

Note 1   Note 1   Note 2

t_{ACC} t_{OE} t_{OH} t_{DF}

D0 to D7   Hi-Z   Data Output   Hi-Z
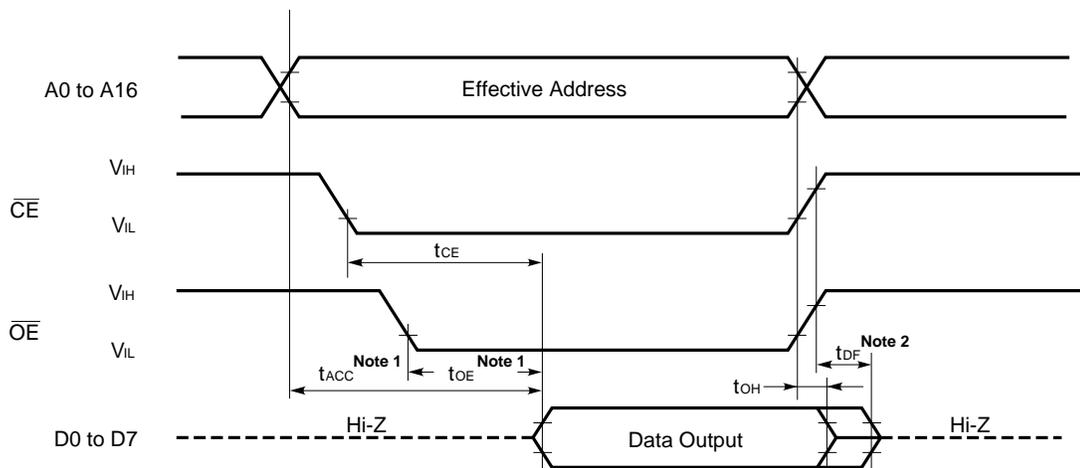
Notes 1. When reading within the t_{ACC} range, the $\overline{OE}$ input delay time from the $\overline{CE}$ fall time must be maximum of
$t_{ACC} - t_{OE}$.

2. t_{DF} is the time from the point at which either $\overline{OE}$ or $\overline{CE}$ (whichever is first) reaches V_{IH}.

PROM Programming Mode Setting Timing

Signal	Levels
V$_{DD}$	V$_{DD}$ / 0
$\overline{RESET}$	
V$_{PP}$	V$_{DD}$ / 0
A0 to A16	Effective Address

t$_{SMA}$
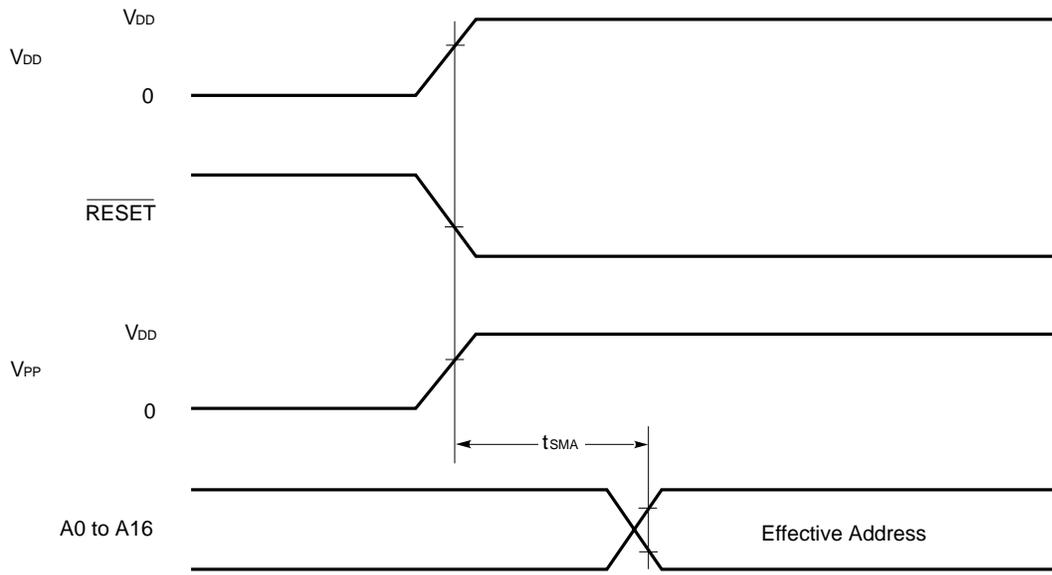
★ **8. CHARACTERISTIC CURVE (REFERENCE VALUE)**

I_DD vs. V_DD (Main System Clock: 10.0 MHz)
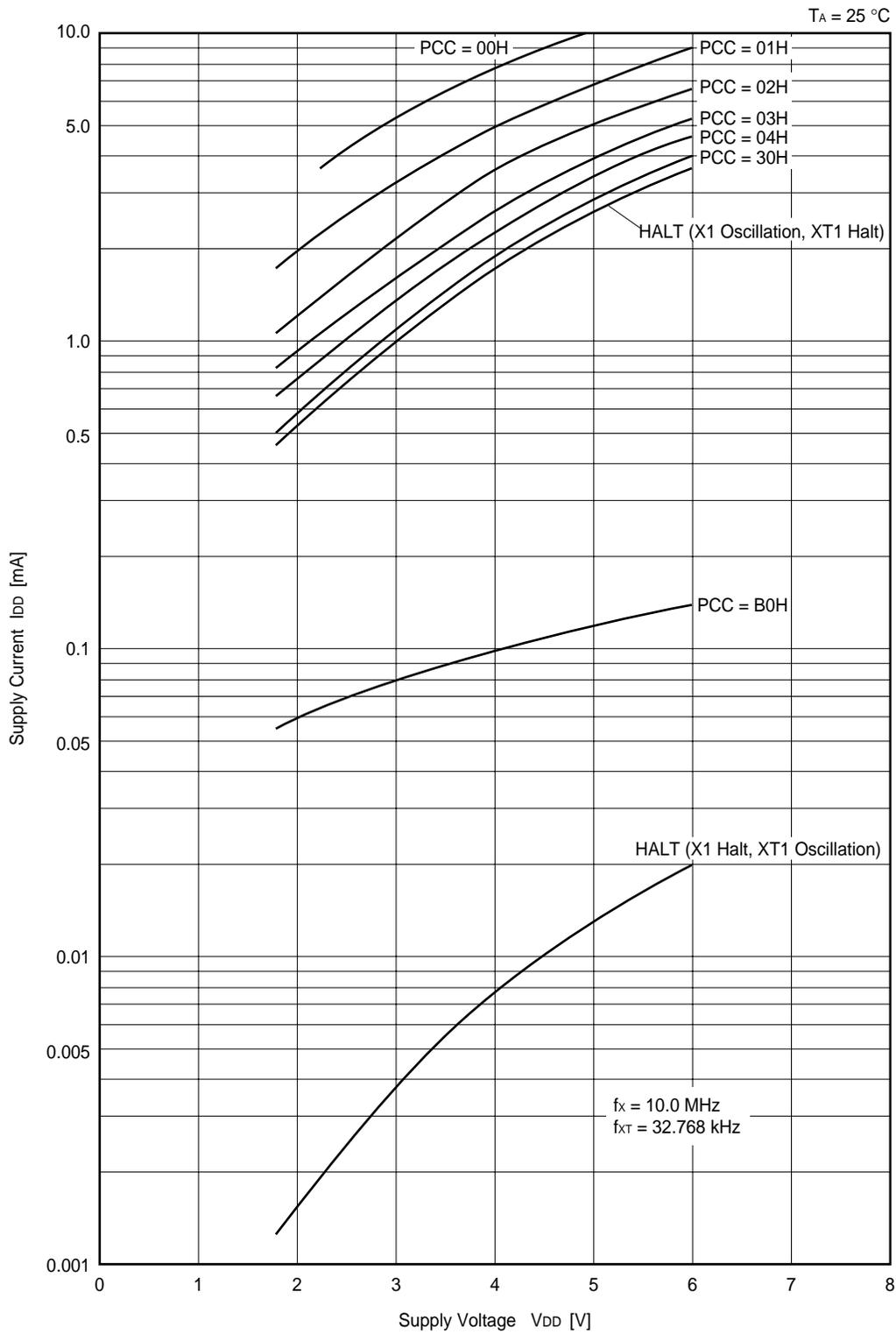
11. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mils)
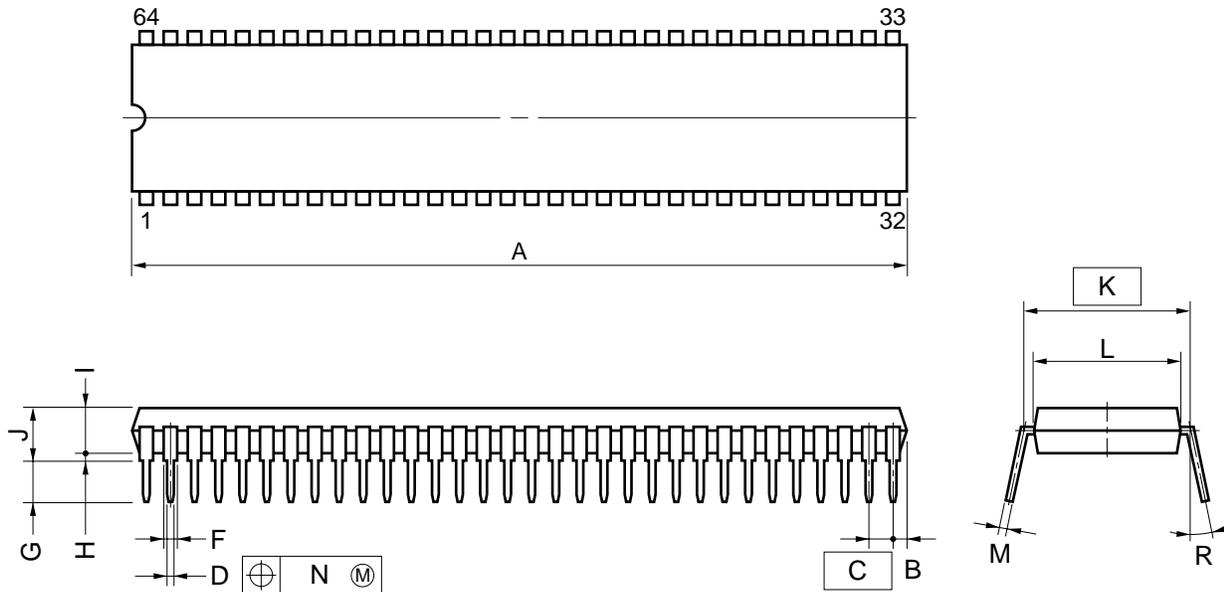
NOTE

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

Remark The dimensions and materials of ES (Engineering Sample) versions are the same as those of mass-produced versions.

64 PIN CERAMIC SHRINK DIP (750 mils)
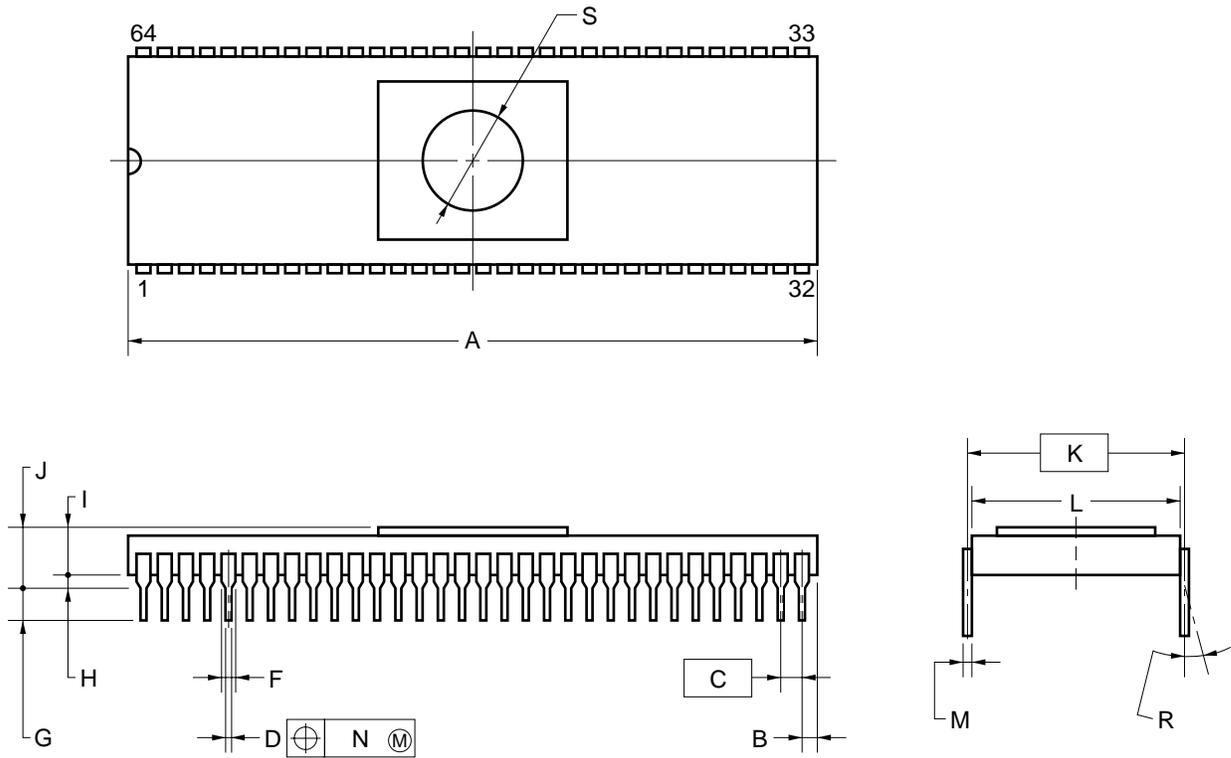
NOTES

1) Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.310 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.46±0.05	0.018±0.002
F	0.8 MIN.	0.031 MIN.
G	3.5±0.3	0.138±0.012
H	1.0 MIN.	0.039 MIN.
I	3.0	0.118
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	18.8	0.740
M	0.25±0.05	$0.010^{+0.002}_{-0.003}$
N	0.25	0.010
R	0~15°	0~15°
S	φ8.89	φ0.350

P64DW-70-750A-1

64 PIN PLASTIC QFP (14x14)

detail of lead end
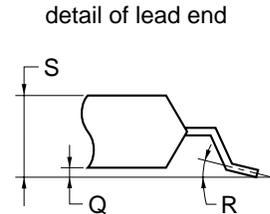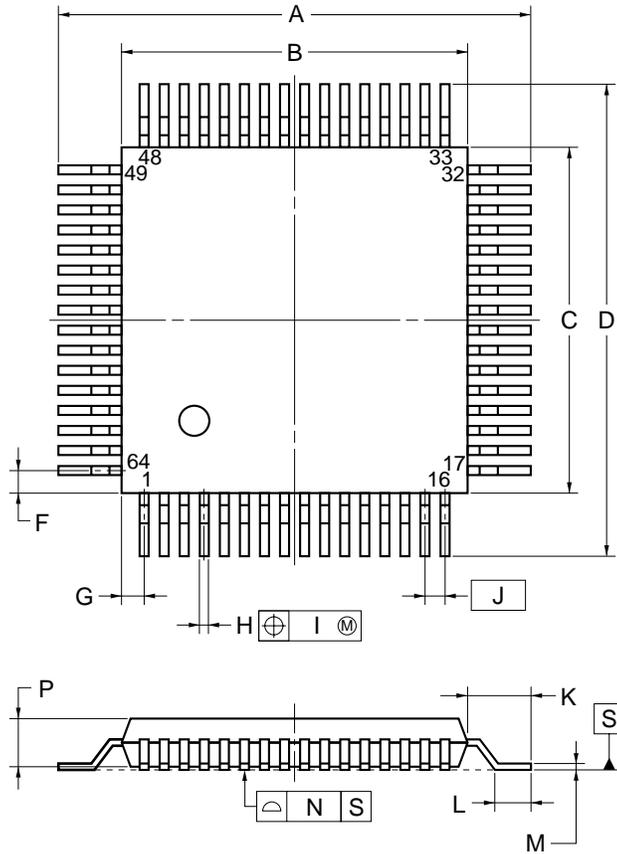
NOTE

1. Controlling dimension —— millimeter.

2. Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	$0.37^{+0.08}_{-0.07}$	$0.015^{+0.003}_{-0.004}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.08}_{-0.07}$	$0.007^{+0.003}_{-0.004}$
N	0.10	0.004
P	2.55±0.1	0.100±0.004
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	2.85 MAX.	0.113 MAX.

P64GC-80-AB8-4

Remark The dimensions and materials of ES (Engineering Sample) versions are the same as those of mass-produced versions.

64 PIN CERAMIC WQFN
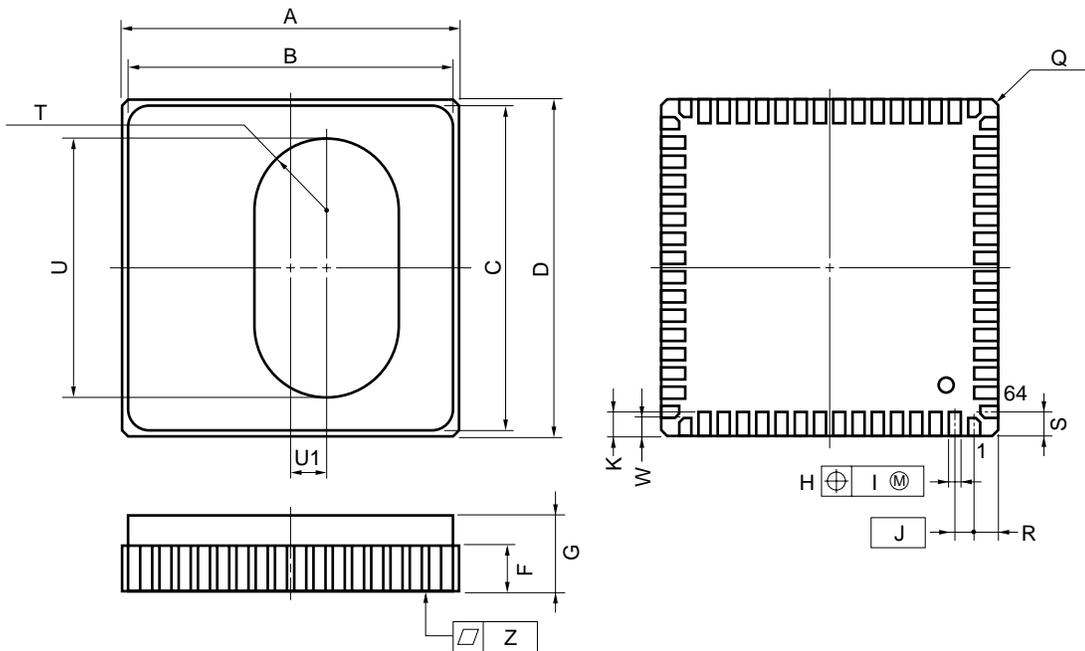
NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

X64KW-80A1

ITEM	MILLIMETERS	INCHES
A	14.0±0.18	0.551±0.007
B	13.4	0.528
C	13.4	0.528
D	14.0±0.18	0.551±0.007
F	1.84	0.072
G	3.56 MAX.	0.141 MAX.
H	0.51±0.1	0.02±0.004
I	0.08	0.003
J	0.8 (T.P.)	0.031 (T.P.)
K	1.0±0.15	$0.039^{+0.007}_{-0.006}$
Q	C 0.3	C 0.012
R	1.0	0.039
S	1.0	0.039
T	R 3.0	R 0.118
U	10.8	0.425
U1	1.4	0.055
W	0.75±0.15	$0.03^{+0.006}_{-0.007}$
Z	0.10	0.004

12. RECOMMENDED SOLDERING CONDITIONS

The μPD78P018FY should be soldered and mounted under the following recommended conditions.

For the recommended soldering conditions, refer to the document **"Semiconductor Device Mounting Technology Manual" (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 12-1. Surface Mounting Type Soldering Conditions

μ**PD78P018FYGC-AB8: 64-pin Plastic QFP (14 $\times$ 14 mm)**

Soldering Method	Soldering Conditions	Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds Max. (at 210°C or higher), Count: Three times or less	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 seconds Max. (at 200°C or higher), Count: Three times or less	VP15-00-3
Wave soldering	Solder bath temperature: 260°C, Time: 10 seconds Max., Count: Once, Preheating temperature: 120°C Max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C Max., Time: 3 seconds Max. (per pin row)	—

Caution   Do not use different soldering methods together (except for partial heating).

Table 12-2. Insertion Type Soldering Conditions

μ**PD78P018FYCW: 64-pin Plastic Shrink DIP (750 mils)**
μ**PD78P018FYDW: 64-pin Ceramic Shrink DIP (with window) (750 mils)**

Soldering Method	Soldering Conditions
Wave soldering (pin only)	Solder temperature: 260°C Max., Time: 10 seconds Max.
Partial heating	Pin temperature: 300°C Max., Time: 3 seconds Max. (per pin)

Caution   Apply wave soldering only to the pins and be careful not to bring solder into direct contact with the package.

★ **APPENDIX A. DEVELOPMENT TOOLS**

The following development tools are available for system development using the μPD78P018FY.
Read **(5) Cautions on using developing tools** for reference.

(1) Language Processing Software

RA78K/0	Assembler package common to 78K/0 Series
CC78K/0	C compiler package common to 78K/0 Series
DF78014	Device file common to μPD78018F Subseries
CC78K/0-L	C compiler library source file common to 78K/0 Series

(2) PROM Writing Tools

PG-1500	PROM programmer
PA-78P018CW PA-78P018GC PA-78P018KK-S	Programmer adapter connected to PG-1500
PG-1500 controller	PG-1500 control program

(3) Debugging Tool

 • **When using in-circuit emulator IE-78K0-NS**

IE-78K0-NS	In-circuit emulator common to 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-70000-98-IF-C	Interface adapter required when using PC-9800 series as host machine (excluding notebook PCs, C bus supported)
IE-70000-CD-IF-A	PC card and interface cable required when using notebook PC of PC-9800 series as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT™ compatible as host machine (ISA bus supported)
IE-70000-PCI-IF	Adapter when using PC that incorporates PCI bus as host machine
IE-78018-NS-EM1	Emulation board common to μPD78018F Subseries
NP-64CW	Emulation probe for 64-pin plastic shrink DIP (CW type)
NP-64GC	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
EV-9200GC-64	Socket to be mounted on a target system board made for 64-pin plastic QFP (GC-AB8 type)
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
DF78014	Device file common to μPD78018F Subseries

• **When using in-circuit emulator IE-78001-R-A**

IE-78001-R-A	In-circuit emulator common to 78K/0 Series
IE-70000-98-IF-C	Interface adapter required when using PC-9800 series as host machine (excluding notebook PCs, C bus supported)
IE-70000-PC-IF-C	Interface adapter required when using IBM PC/AT compatible as host machine (ISA bus supported)
IE-78000-R-SV3	Interface adapter and cable when using EWS as host machine
IE-70000-PCI-IF	Adapter when using PC that incorporates PCI bus as host machine
IE-78018-NS-EM1	Emulation board common to μPD78018F Subseries
IE-78K0-R-EX1	Emulation probe conversion board necessary to use IE-78018-NS-EM1 on IE-78001-R-A
EP-78240CW-R	Emulation probe for 64-pin plastic shrink DIP (CW type)
EP-78240GC-R	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
EV-9200GC-64	Socket to be mounted on a target system board made for 64-pin plastic QFP (GC-AB8 type)
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
DF78014	Device file common to μPD78018F Subseries

(4) Real-time OS

RX78K/0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series

(5) Cautions on using development tools
- The ID-78K0-NS, ID78K0, and SM78K0 are used in combination with the DF78014.
- The CC78K/0 and RX78K/0 are used in combination with the RA78K/0 and the DF78014.
- NP-64CW and NP-64GC are products made by Naitou Densei Machidaseisakusho (TEL: +81-44-822-3813).
  Contact an NEC distributor regarding the purchase of these products.
- For third party development tools, see the **78K/0 Series Selection Guide (U11126E)**.
- The host machine and OS suitable for each software are as follows:

Software / Host Machine [OS]	PC PC-9800 series [Windows™] IBM PC/AT compatible [Japanese/English Windows]	EWS HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K/0	√ Note	√
CC78K/0	√ Note	√
PG-1500 Controller	√ Note	—
ID78K0-NS	√	—
ID78K0	√	√
SM78K0	√	—
RX78K/0	√ Note	√
MX78K0	√ Note	√

Note   DOS-based software

Drawing of Conversion Socket (EV-9200GC-64) and Recommended Footprint

Figure A-1. Drawing of EV-9200GC-64 (for reference only)

No.1 pin index
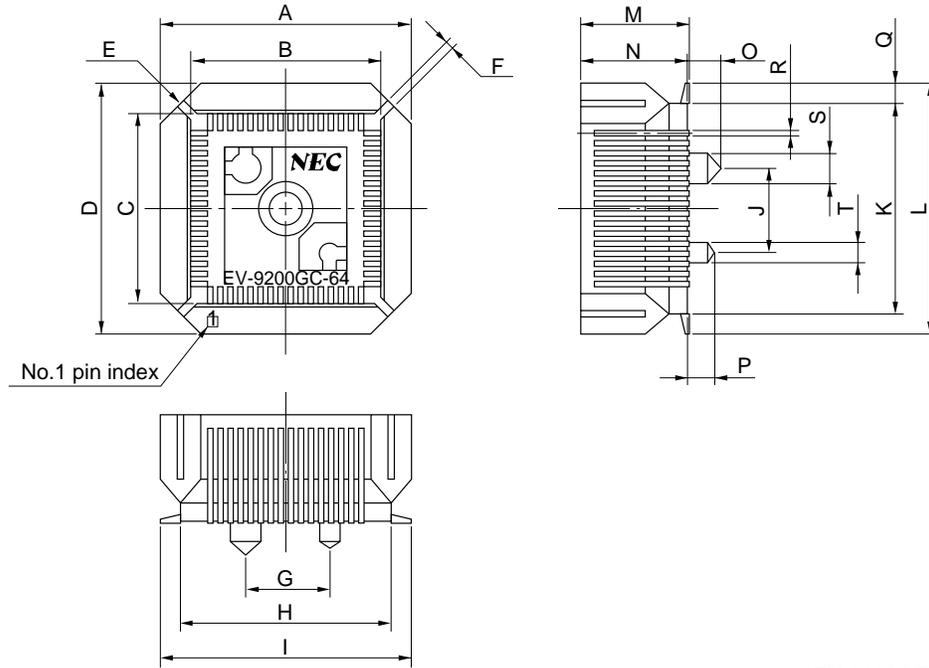
EV-9200GC-64

EV-9200GC-64-G0E

ITEM	MILLIMETERS	INCHES
A	18.8	0.74
B	14.1	0.555
C	14.1	0.555
D	18.8	0.74
E	4-C 3.0	4-C 0.118
F	0.8	0.031
G	6.0	0.236
H	15.8	0.622
I	18.5	0.728
J	6.0	0.236
K	15.8	0.622
L	18.5	0.728
M	8.0	0.315
N	7.8	0.307
O	2.5	0.098
P	2.0	0.079
Q	1.35	0.053
R	0.35±0.1	$0.014^{+0.004}_{-0.005}$
S	ϕ2.3	ϕ0.091
T	ϕ1.5	ϕ0.059

Figure A-2. Recommended Footprint of EV-9200GC-64 (for reference only)
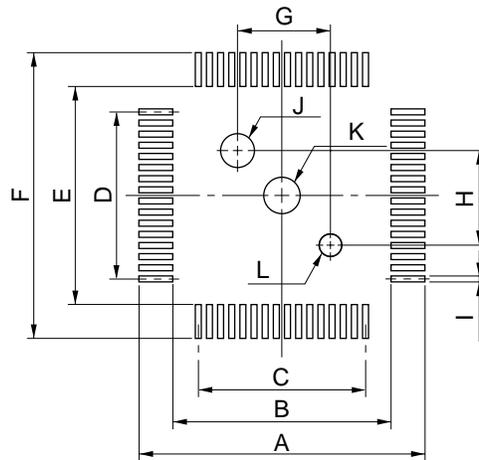
EV-9200GC-64-P1E

ITEM	MILLIMETERS	INCHES
A	19.5	0.768
B	14.8	0.583
C	$0.8\pm0.02 \times 15=12.0\pm0.05$	$0.031^{+0.002}_{-0.001} \times 0.591=0.472^{+0.003}_{-0.002}$
D	$0.8\pm0.02 \times 15=12.0\pm0.05$	$0.031^{+0.002}_{-0.001} \times 0.591=0.472^{+0.003}_{-0.002}$
E	14.8	0.583
F	19.5	0.768
G	6.00 ± 0.08	$0.236^{+0.004}_{-0.003}$
H	6.00 ± 0.08	$0.236^{+0.004}_{-0.003}$
I	0.5 ± 0.02	$0.197^{+0.001}_{-0.002}$
J	$\phi2.36\pm0.03$	$\phi0.093^{+0.001}_{-0.002}$
K	$\phi2.2\pm0.1$	$\phi0.087^{+0.004}_{-0.005}$
L	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

★ **APPENDIX B. RELATED DOCUMENTS**

Device Related Documents

Document Name		Document No.	
		Japanese	English
μPD78011FY, 78012FY, 78013FY, 78014FY, 78015FY, 78016FY, 78018FY Data Sheet		U10281J	U10281E
μPD78P018FY Data Sheet		U10989J	This document
μPD78018F, 78018FY Subseries User's Manual		U10659J	U10659E
78K/0 Series User's Manual - Instructions		U12326J	U12326E
78K/0 Series Instruction List		U10903J	—
78K/0 Series Instruction Set		U10904J	—
μPD78018FY Subseries Special Function Register List		U10287J	—
78K/0 Series Application Note	Basics (I)	U12704J	U12704E
	Floating-Point Arithmetic Programs	U13482J	IEA-1289

Development Tool Documents (User's Manual) (1/2)

Document Name		Document No.	
		Japanese	English
RA78K0 Assembler Package	Operation	U11802J	U11802E
	Assembly Language	U11801J	U11801E
	Structured Assembly Language	U11789J	U11789E
RA78K Series Structured Assembler Preprocessor		U12323J	EEU-1402
CC78K0 C Compiler	Operation	U11517J	U11517E
	Language	U11518J	U11518E
CC78K/0 C Compiler Application Note	Programming Know-How	U13034J	U13034E
PG-1500 PROM Programmer		U11940J	U11940E
PG-1500 Controller PC-9800 Series (MS-DOS™) Based		EEU-704	EEU-1291
PG-1500 Controller IBM PC Series (PC DOS™) Based		EEU-5008	U10540E
IE-78K0-NS		To be prepared	To be prepared
IE-78001-R-A		To be prepared	To be prepared
IE-78K0-R-EX1		To be prepared	To be prepared
IE-78018-NS-EM1		U13289J	To be prepared
EP-78240		EEU-986	U10332E

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Development Tool Documents (User's Manual) (2/2)

Document Name		Document No.	
		Japanese	English
SM78K0 System Simulator Windows Based	Reference	U10181J	U10181E
SM78K Series System Simulator	External Part User Open Interface Specification	U10092J	U10092E
ID78K0-NS Integrated Debugger Windows Based	Reference	U12900J	U12900E
ID78K0 Integrated Debugger EWS based	Reference	U11151J	—
ID78K0 Integrated Debugger PC based	Reference	U11539J	U11539E
ID78K0 Integrated Debugger Windows based	Guide	U11649J	U11649E

Embedded Software Documents (User's Manual)

Document Name		Document No.	
		Japanese	English
78K/0 Series Real-Time OS	Basic	U11537J	U11537E
	Installation	U11536J	U11536E
78K/0 Series OS MX78K0	Basic	U12257J	U12257E

Other Documents

Document Name	Document No.	
	Japanese	English
NEC IC Package Manual (CD-ROM)	—	C13388E
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damages for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Guide to Quality Assurance for Semiconductor Devices	—	MEI-1202
Microcomputer – Related Product Guide – Third Parties	U11416J	—

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[MEMO]

NOTES FOR CMOS DEVICES

① **PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② **HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V$_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ **STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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• Availability of related technical literature

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