NEC

MOS INTEGRATED CIRCUIT

# μPD78P018F(A)

## 8-BIT SINGLE-CHIP MICROCONTROLLER

### DESCRIPTION

The μPD78P018F(A) comes under a more severe quality assurance program than the μPD78P018F (standard grade), so it is classified as special grade in NEC's quality grade classification.

The μPD78P018F(A) is a member of the μPD78018F Subseries within 78K/0 Series. The internal mask ROM of the μPD78018F(A) is replaced with one-time PROM.

Because the μPD78P018F(A) can be programmed by users, it is ideally suited for applications involving the evaluation of systems in the development stage, small-scale production of many different products, and rapid development and time-to-market of new products.

**Detailed descriptions of functions are provided in the following documents. Be sure to read them before designing.**

**μPD78018F, 78018FY Subseries User's Manual: U10659E**
**78K/0 Series User's Manual—Instructions: U12326E**

### FEATURES

- Higher reliability compared to the μPD78P018F (refer to "Quality Grades on NEC Semiconductor Devices" (C11531E))
- Pin compatible with mask ROM version (except $V_{PP}$ pin)
- Internal PROM: 60 Kbytes **Note 1**
  μPD78P018FCW(A), 78P018FGC(A)-AB8: Programmable only once (suited for small-scale production)
- Internal high-speed RAM: 1024 bytes **Note 1**
- Internal expansion RAM: 1024 bytes **Note 2**
- Internal buffer RAM: 32 bytes
- Operable over same supply voltage range as mask ROM version (1.8 to 5.5 V)
- QTOP™ microcontroller supported

**Notes 1.** The capacities of internal PROM and internal high-speed RAM can be changed by means of the internal memory size switching register (IMS).

**2.** The capacity of the internal expansion RAM can be changed by means of the internal expansion RAM size switching register (IXS).

**Remarks 1.** QTOP Microcontroller is a general term for microcontrollers which incorporate one-time PROM and are totally supported by NEC's programming service (from programming to marking, screening and verification).

**2.** For the differences between the PROM version and mask ROM versions, refer to **1. DIFFERENCES BETWEEN THE μPD78P018F(A) AND MASK ROM VERSIONS**.



Document No. U12132EJ2V0DS00 (2nd edition)
Date Published December 1998 N CP(K)
Printed in Japan

**The mark ★ shows major revised points.**

## ORDERING INFORMATION

| Part Number | Package | Internal ROM |
|---|---|---|
| μPD78P018FCW(A) | 64-pin plastic shrink DIP (750 mil) | One-time PROM |
| μPD78P018FGC(A)-AB8 | 64-pin plastic QFP (14 × 14 mm) | One-time PROM |

## QUALITY GRADE

| Part Number | Package | Quality Grade |
|---|---|---|
| μPD78P018FCW(A) | 64-pin plastic shrink DIP (750 mil) | Special |
| μPD78P018FGC(A)-AB8 | 64-pin plastic QFP (14 × 14 mm) | Special |

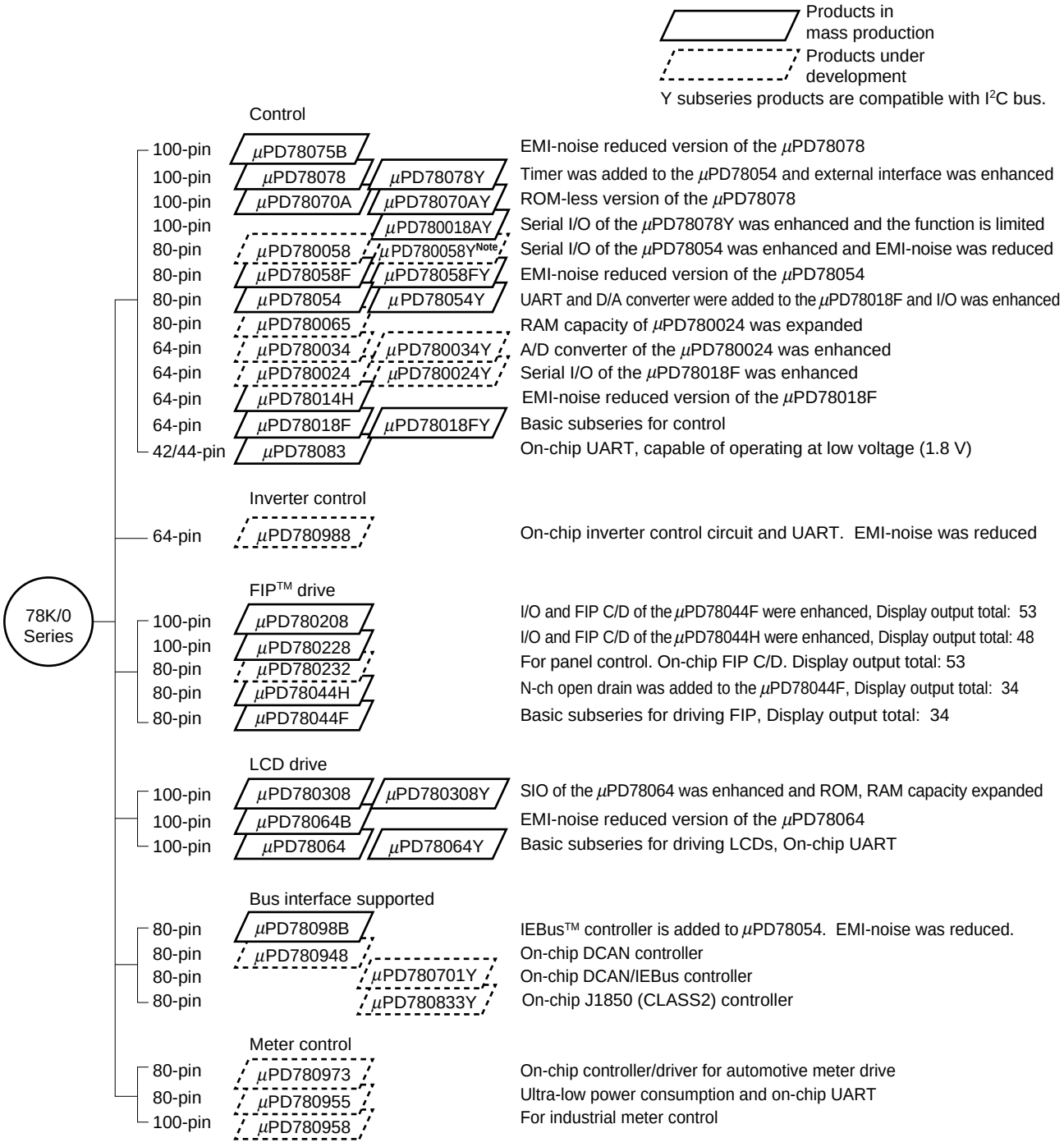
Refer to "Quality Grades on NEC Semiconductor Devices" (Document number C11531E) published by NEC Corporation for detailed information on the quality grades and recommended applications of devices.

The following table shows the differences between the μPD78P018F(A) and the standard product (μPD78P018F).

| Item \ Part Number | μPD78P018F(A) | μPD78P018F |
|---|---|---|
| Packages | • 64-pin plastic shrink DIP (750 mil)<br>• 64-pin plastic QFP (14 x 14 mm) | • 64-pin plastic shrink DIP (750 mil)<br>• 64-pin plastic QFP (14 x 14 mm)<br>• 64-pin plastic LQFP (12 x 12 mm)<br>• 64-pin ceramic shrink DIP (with a window) (750 mil)<br>• 64-pin ceramic WQFN (14 x 14 mm) |
| Quality Grade | Special | Standard |

## ★ 78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.




**Note** Under planning

The major functional differences among subseries are shown below.

| Subseries Name \ Function | | ROM Capacity | Timer | | | | 8-bit A/D | 10-bit A/D | 8-bit D/A | Serial Interface | I/O | $V_{DD}$ MIN. Value | External Expansion |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 8-bit | 16-bit | Watch | WDT | | | | | | | |
| Control | μPD78075B | 32 K to 40 K | 4 ch | 1 ch | 1 ch | 1 ch | 8 ch | — | 2 ch | 3 ch (UART: 1 ch) | 88 | 1.8 V | Available |
| | μPD78078 | 48 K to 60 K | | | | | | | | | | | |
| | μPD78070A | — | | | | | | | | | 61 | 2.7 V | |
| | μPD780058 | 24 K to 60 K | 2 ch | | | | | | | 3 ch (time-division UART: 1 ch) | 68 | 1.8 V | |
| | μPD78058F | 48 K to 60 K | | | | | | | | 3 ch (UART: 1 ch) | 69 | 2.7 V | |
| | μPD78054 | 16 K to 60 K | | | | | | | | | | 2.0 V | |
| | μPD780065 | 40 K to 48 K | | | | | | | — | 4 ch (UART: 1 ch) | 60 | 2.7 V | |
| | μPD780034 | 8 K to 32 K | | | | | — | 8 ch | | 3 ch (UART: 1 ch, time-division 3-wire: 1 ch) | 51 | 1.8 V | |
| | μPD780024 | | | | | | 8 ch | — | | | | | |
| | μPD78014H | | | | | | | | | 2 ch | 53 | | |
| | μPD78018F | 8 K to 60 K | | | | | | | | | | | |
| | μPD78083 | 8 K to 16 K | | — | — | | | | | 1 ch (UART: 1 ch) | 33 | | — |
| Inverter control | μPD780988 | 16 K to 60 K | 3 ch | **Note** | — | 1 ch | — | 8 ch | — | 3 ch (UART: 2 ch) | 47 | 4.0 V | Available |
| FIP drive | μPD780208 | 32 K to 60 K | 2 ch | 1 ch | 1 ch | 1 ch | 8 ch | — | — | 2 ch | 74 | 2.7 V | — |
| | μPD780228 | 48 K to 60 K | 3 ch | — | — | | | | | 1 ch | 72 | 4.5 V | |
| | μPD780232 | 16 K to 24 K | | | | | 4 ch | | | 2 ch | 40 | | |
| | μPD78044H | 32 K to 48 K | 2 ch | 1 ch | 1 ch | | 8 ch | | | 1 ch | 68 | 2.7 V | |
| | μPD78044F | 16 K to 40 K | | | | | | | | 2 ch | | | |
| LCD drive | μPD780308 | 48 K to 60 K | 2 ch | 1 ch | 1 ch | 1 ch | 8 ch | — | — | 3 ch (time-division UART: 1 ch) | 57 | 2.0 V | — |
| | μPD78064B | 32 K | | | | | | | | 2 ch (UART: 1 ch) | | | |
| | μPD78064 | 16 K to 32 K | | | | | | | | | | | |
| Bus interface supported | μPD78098B | 40 K to 60 K | 2 ch | 1 ch | 1 ch | 1 ch | 8 ch | — | 2 ch | 3 ch (UART: 1 ch) | 69 | 2.7 V | — |
| | μPD780948 | 60 K | | 2 ch | | | | | — | | 79 | 4.0 V | |
| Meter control | μPD780973 | 24 K to 32 K | 3 ch | 1 ch | 1 ch | 1 ch | 5 ch | — | — | 2 ch (UART: 1 ch) | 56 | 4.5 V | — |
| | μPD780955 | 40 K | 6 ch | | — | | 1 ch | | | 2 ch (UART: 2 ch) | 50 | 2.2 V | |
| | μPD780958 | 48 K to 60 K | 4 ch | 2 ch | | | — | | | 2 ch (UART: 1 ch) | 69 | | |

**Note** 16-bit timer: 2 channels
10-bit timer: 1 channel

## FUNCTION OVERVIEW

| Item | | Function |
|---|---|---|
| Internal memory | PROM | 60 Kbytes Note 1 |
| | High-speed RAM | 1024 bytes Note 1 |
| | Expansion RAM | 1024 bytes Note 2 |
| | Buffer RAM | 32 bytes |
| Memory space | | 64 Kbytes |
| General-purpose registers | | 8 bits × 32 registers (8 bits × 8 registers × 4 banks) |
| Minimum instruction execution time | | Minimum instruction execution time modification function provided. |
| | When main system clock selected | 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (@10.0-MHz operation) |
| | When subsystem clock selected | 122 μs (@32.768-kHz operation) |
| Instruction set | | • 16-bit operation<br>• Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits)<br>• Bit manipulate (set, reset, test, boolean operation)<br>• BCD adjust, etc. |
| I/O ports | | Total: 53<br>• CMOS input: 2<br>• CMOS I/O: 47<br>• N-channel open-drain I/O (15-V withstand voltage): 4 |
| A/D converter | | • 8-bit resolution × 8 channels<br>• Operable over a wide power supply voltage range: $AV_{DD}$ = 2.2 to 5.5 V |
| Serial interface | | • 3-wire serial I/O/SBI/2-wire serial I/O mode selectable: 1 channel<br>• 3-wire serial I/O mode (automatic data transmit/receive function for up to 32 bytes is provided on chip): 1 channel |
| Timer | | • 16-bit timer/event counter: 1 channel<br>• 8-bit timer/event counter: 2 channels<br>• Watch timer: 1 channel<br>• Watchdog timer: 1 channel |
| Timer output | | 3 (14-bit PWM output × 1) |
| Clock output | | 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz (@10.0-MHz operation with main system clock), 32.768 kHz (@32.768-kHz operation with subsystem clock) |
| Buzzer output | | 2.4 kHz, 4.9 kHz, 9.8 kHz (@10.0-MHz operation with main system clock) |
| Vectored interrupt sources | Maskable | Internal: 8<br>External: 4 |
| | Non-maskable | Internal: 1 |
| | Software | 1 |
| Test input | | Internal: 1<br>External: 1 |
| Supply voltage | | $V_{DD}$ = 1.8 to 5.5 V |
| Operating ambient temperature | | $T_A$ = –40 to +85°C |
| Package | | • 64-pin plastic shrink DIP (750 mil)<br>• 64-pin plastic QFP (14 × 14 mm) |

★

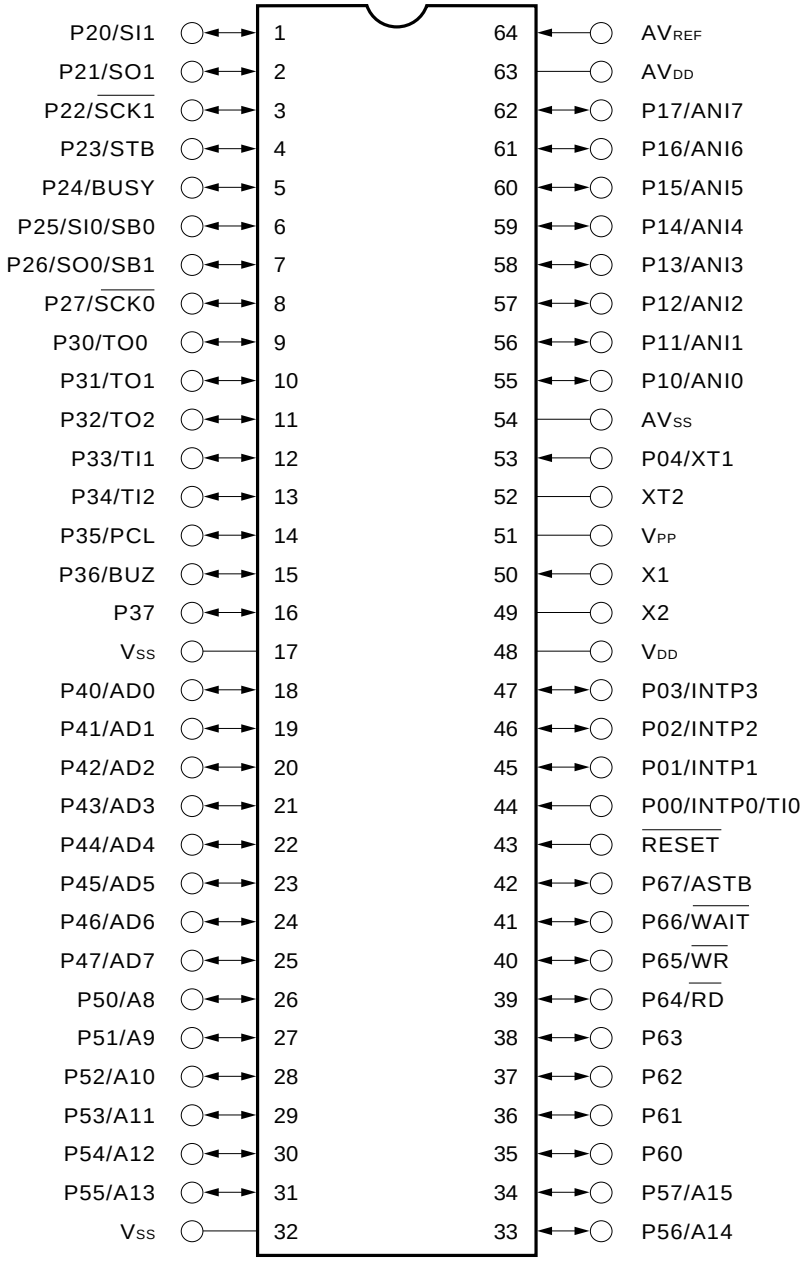
**Notes 1.** The internal PROM and internal high-speed RAM capacities can be changed with the internal memory size switching register (IMS).

**2.** The internal expansion RAM capacity can be changed with the internal expansion RAM size switching register (IXS).

## PIN CONFIGURATION (Top View)

**(1) Normal operating mode**

- **64-pin Plastic Shrink DIP (750 mil)**
  μPD78P018FCW(A)

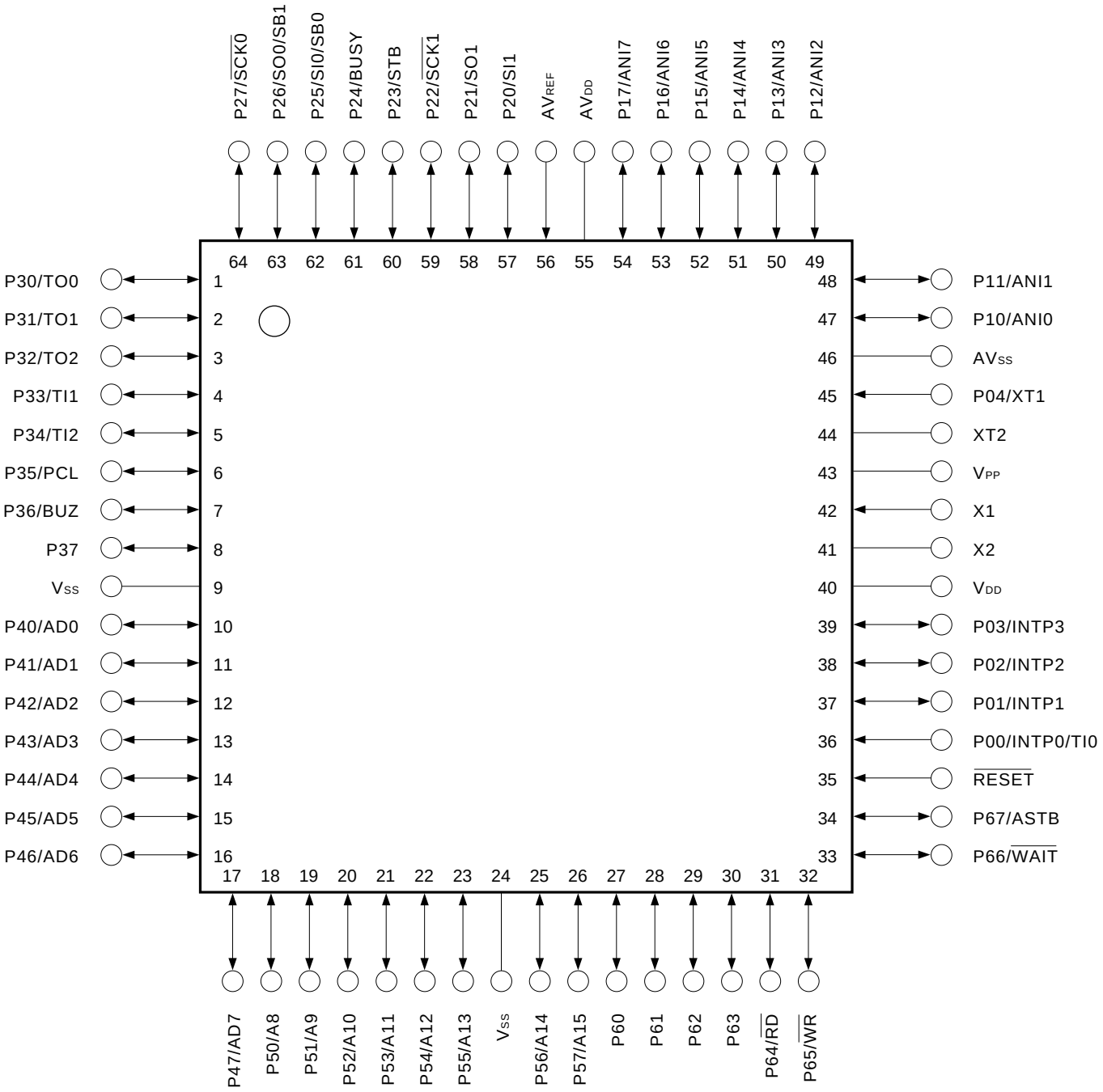



**Cautions 1. Connect the $V_{PP}$ pin directly to $V_{SS}$.**

**2. Connect the $AV_{DD}$ pin to $V_{DD}$.**

**3. Connect the $AV_{SS}$ pin to $V_{SS}$.**

- **64-pin Plastic QFP (14 × 14 mm)**
  μPD78P018FGC(A)-AB8




**Cautions 1. Connect the $V_{PP}$ pin directly to $V_{SS}$.**

**2. Connect the $AV_{DD}$ pin to $V_{DD}$.**

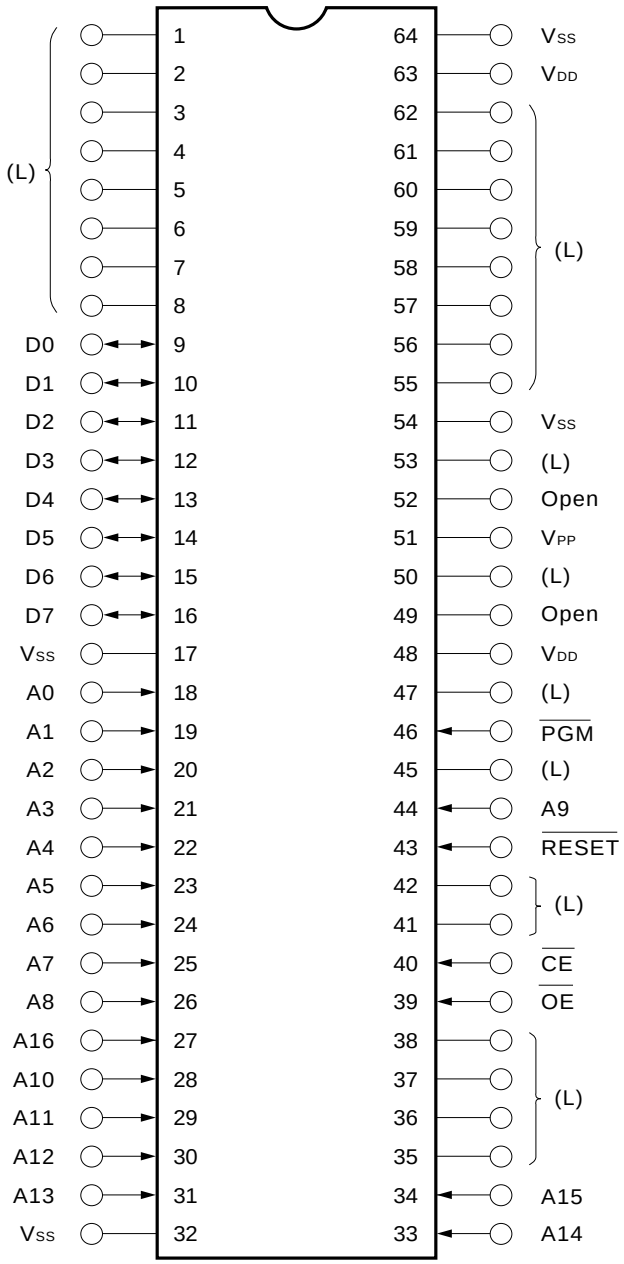
**3. Connect the $AV_{SS}$ pin to $V_{SS}$.**

| | |
|---|---|
| A8 to A15: | Address Bus |
| AD0 to AD7: | Address/Data Bus |
| ANI0 to ANI7: | Analog Input |
| ASTB: | Address Strobe |
| $AV_{DD}$: | Analog Power Supply |
| $AV_{REF}$: | Analog Reference Voltage |
| $AV_{SS}$ : | Analog Ground |
| BUSY: | Busy |
| BUZ: | Buzzer Clock |
| INTP0 to INTP3: | Interrupt from Peripherals |
| P00 to P04: | Port 0 |
| P10 to P17: | Port 1 |
| P20 to P27: | Port 2 |
| P30 to P37: | Port 3 |
| P40 to P47: | Port 4 |
| P50 to P57: | Port 5 |
| P60 to P67: | Port 6 |
| PCL: | Programmable Clock |
| $\overline{RD}$: | Read Strobe |
| $\overline{RESET}$: | Reset |
| SB0, SB1: | Serial Bus |
| $\overline{SCK0}$, $\overline{SCK1}$: | Serial Clock |
| SI0, SI1: | Serial Input |
| SO0, SO1: | Serial Output |
| STB: | Strobe |
| TI0 to TI2: | Timer Input |
| TO0 to TO2: | Timer Output |
| $V_{DD}$: | Power Supply |
| $V_{PP}$: | Programming Power Supply |
| $V_{SS}$: | Ground |
| $\overline{WAIT}$: | Wait |
| $\overline{WR}$: | Write Strobe |
| X1 and X2: | Crystal (Main System Clock) |
| XT1 and XT2: | Crystal (Subsystem Clock) |

**(2) PROM programming mode**

- **64-pin Plastic Shrink DIP (750 mil)**

  μPD78P018FCW(A)



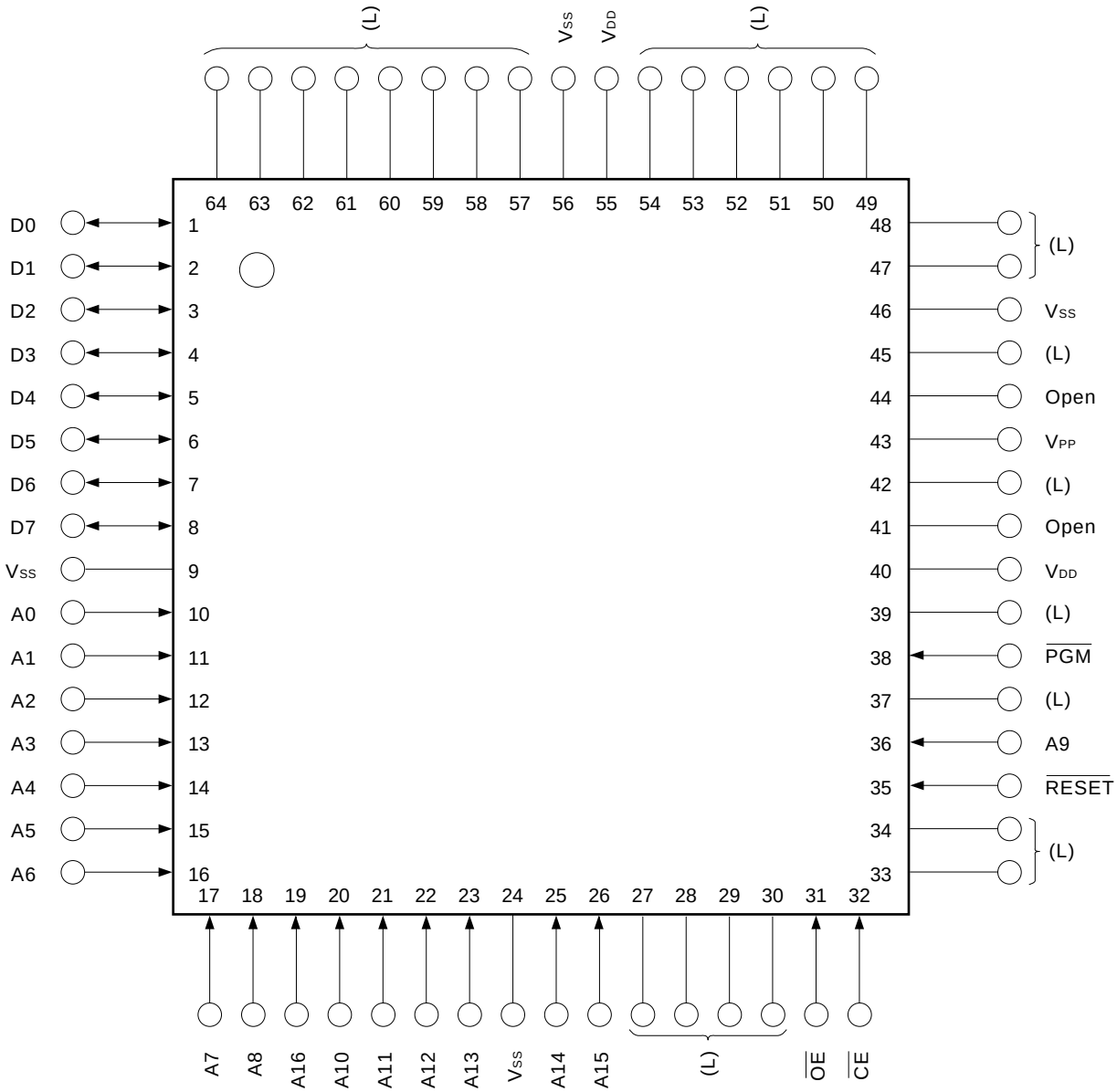

**Cautions 1. (L): Independently connect to $V_{SS}$ via a pull-down resistor.**

**2. $V_{SS}$: Connect to GND.**

**3. $\overline{\text{RESET}}$: Set to low level.**

**4. Open: Leave open.**

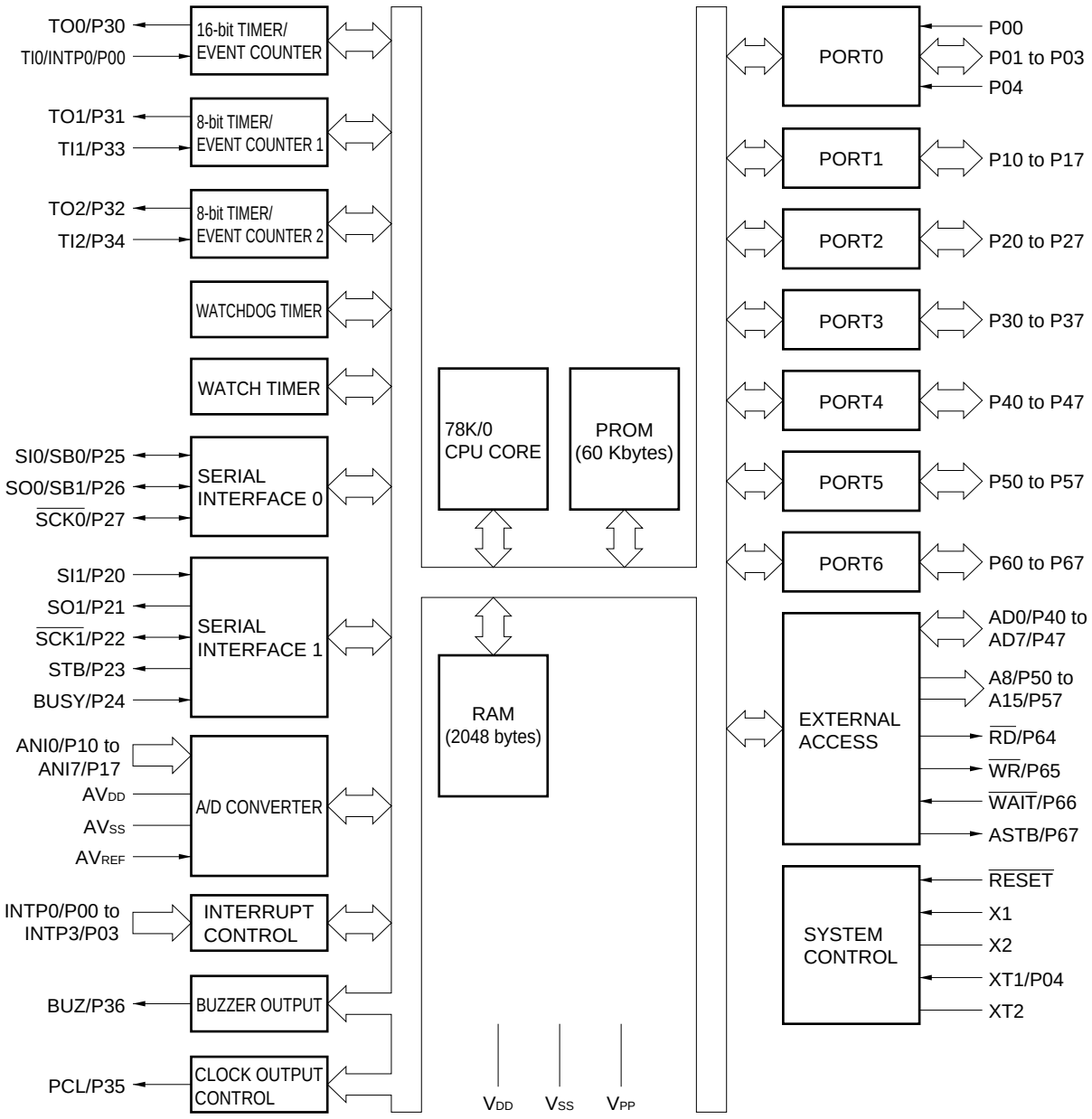
- **64-pin Plastic QFP (14 × 14 mm)**
  μPD78P018FGC(A)-AB8




**Cautions 1. (L): Independently connect to $V_{SS}$ via a pull-down resistor.**
**2. $V_{SS}$: Connect to GND.**
**3. $\overline{RESET}$: Set to low level.**
**4. Open: Leave open.**

| | | | |
|---|---|---|---|
| A0 to A16: | Address | $\overline{RESET}$: | Reset |
| $\overline{CE}$: | Chip Enable | $V_{DD}$: | Power Supply |
| D0 to D7: | Data Bus | $V_{PP}$: | Programming Power Supply |
| $\overline{OE}$: | Output Enable | $V_{SS}$: | Ground |
| $\overline{PGM}$: | Program | | |

## BLOCK DIAGRAM



CONTENTS

## 1. DIFFERENCES BETWEEN THE μPD78P018F(A) AND MASK ROM VERSIONS

The μPD78P018F(A) is a single-chip microcontroller with an on-chip one-time PROM which can be rewritten only once.

It is possible to make all the functions, except for PROM specification and mask option of the P60 to P63 pins, the same as those of mask ROM versions (μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), and 78018F(A)) by setting the internal memory size switching register (IMS) and the internal expansion RAM size switching register (IXS).

Differences between the μPD78P018F(A) and mask ROM versions are shown in Table 1-1.

**Table 1-1. Differences between μPD78P018F(A) and Mask ROM Version**

| Parameter | μPD78P018F(A) | Mask ROM Versions |
|---|---|---|
| Internal ROM type | One-time PROM | Mask ROM |
| Internal ROM capacity | 60 Kbytes | μPD78011F(A): 8 Kbytes<br>μPD78012F(A): 16 Kbytes<br>μPD78013F(A): 24 Kbytes<br>μPD78014F(A): 32 Kbytes<br>μPD78015F(A): 40 Kbytes<br>μPD78016F(A): 48 Kbytes<br>μPD78018F(A): 60 Kbytes |
| Internal high-speed RAM capacity | 1024 bytes | μPD78011F(A): 512 bytes<br>μPD78012F(A): 512 bytes<br>μPD78013F(A): 1024 bytes<br>μPD78014F(A): 1024 bytes<br>μPD78015F(A): 1024 bytes<br>μPD78016F(A): 1024 bytes<br>μPD78018F(A): 1024 bytes |
| Internal expansion RAM capacity | 1024 bytes | μPD78011F(A): No<br>μPD78012F(A): No<br>μPD78013F(A): No<br>μPD78014F(A): No<br>μPD78015F(A): 512 bytes<br>μPD78016F(A): 512 bytes<br>μPD78018F(A): 1024 bytes |
| Internal ROM, internal high-speed RAM capacity changeable with internal memory size switching register | Yes **Note 1** | No |
| Internal expansion RAM capacity changeable with internal expansion RAM size switching register | Yes **Note 2** | No |
| IC pin | No | Yes |
| $V_{PP}$ pin | Yes | No |
| On-chip pull-up resistor mask option of P60 to P63 pins | No | Yes |
| Electrical specifications, recommended soldering conditions | See respective data sheet of individual products. | |

**Notes 1.** The internal PROM capacity becomes 60 Kbytes and the internal high-speed RAM capacity becomes 1024 bytes by $\overline{\text{RESET}}$ input.

**2.** The internal expansion RAM capacity becomes 1024 bytes by $\overline{\text{RESET}}$ input.

★ **Caution There are differences in noise immunity and noise radiation between the PROM and mask ROM versions. When pre-producing an application set with the PROM version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the commercial samples (not engineering samples) of the mask ROM version.**

## 2. PIN FUNCTIONS

### 2.1 Pins During Normal Operating Mode

#### (1) Port pins (1/2)

| Pin Name | I/O | Function | | After Reset | Alternate Function |
|---|---|---|---|---|---|
| P00 | Input | Port 0<br>5-bit input/output port | Input only | Input | INTP0/TI0 |
| P01 | Input/output | | Input/output can be specified in 1-bit units.<br>When used as an input port, an on-chip pull-up resistor can be specified by means of software. | Input | INTP1 |
| P02 | | | | | INTP2 |
| P03 | | | | | INTP3 |
| P04 Note 1 | Input | | Input only | Input | XT1 |
| P10 to P17 | Input/output | Port 1<br>8-bit input/output port<br>Input/output can be specified in 1-bit units.<br>When used as an input port, an on-chip pull-up resistor can be specified by means of software. Note 2 | | Input | ANI0 to ANI7 |
| P20 | Input/output | Port 2<br>8-bit input/output port<br>Input/output can be specified in 1-bit units.<br>When used as an input port, an on-chip pull-up resistor can be specified by means of software. | | Input | SI1 |
| P21 | | | | | SO1 |
| P22 | | | | | $\overline{\text{SCK1}}$ |
| P23 | | | | | STB |
| P24 | | | | | BUSY |
| P25 | | | | | SI0/SB0 |
| P26 | | | | | SO0/SB1 |
| P27 | | | | | $\overline{\text{SCK0}}$ |
| P30 | Input/output | Port 3<br>8-bit input/output port<br>Input/output can be specified in 1-bit units.<br>When used as an input port, an on-chip pull-up resistor can be specified by means of software. | | Input | TO0 |
| P31 | | | | | TO1 |
| P32 | | | | | TO2 |
| P33 | | | | | TI1 |
| P34 | | | | | TI2 |
| P35 | | | | | PCL |
| P36 | | | | | BUZ |
| P37 | | | | | — |
| P40 to P47 | Input/output | Port 4<br>8-bit input/output port<br>Input/output can be specified in 8-bit units.<br>When used as an input port, an on-chip pull-up resistor can be specified by means of software.<br>Test input flag (KRIF) is set to 1 by falling edge detection. | | Input | AD0 to AD7 |

**Notes 1.** When using the P04/XT1 pin as an input port, set bit 6 (FRC) of the processor clock control register (PCC) to 1 (Do not use the internal feedback resistor of the subsystem clock oscillator).

**2.** When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input, the internal pull-up resistor is automatically disabled.

**(1) Port pins (2/2)**

| Pin Name | I/O | Function | | After Reset | Alternate Function |
|---|---|---|---|---|---|
| P50 to P57 | Input/ output | Port 5<br>8-bit input/output port<br>LEDs can be driven directly.<br>Input/output can be specified in 1-bit units.<br>When used as an input port, an on-chip pull-up resistor can be specified by means of software. | | Input | A8 to A15 |
| P60 | Input/ output | Port 6<br>8-bit input/output port<br>Input/output can be specified in 1-bit units. | N-ch open-drain input/output port<br>LEDs can be driven directly. | Input | — |
| P61 | | | | | |
| P62 | | | | | |
| P63 | | | | | |
| P64 | | | When used as an input port, an on-chip pull-up resistor can be specified by means of software. | | $\overline{RD}$ |
| P65 | | | | | $\overline{WR}$ |
| P66 | | | | | $\overline{WAIT}$ |
| P67 | | | | | ASTB |

**(2) Non-port pins (1/2)**

| Pin Name | I/O | Function | After Reset | Alternate Function |
|---|---|---|---|---|
| INTP0 | Input | External interrupt request input by which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified. | Input | P00/TI0 |
| INTP1 | | | | P01 |
| INTP2 | | | | P02 |
| INTP3 | | Falling edge detection external interrupt request input | | P03 |
| SI0 | Input | Serial interface serial data input | Input | P25/SB0 |
| SI1 | | | | P20 |
| SO0 | Output | Serial interface serial data output | Input | P26/SB1 |
| SO1 | | | | P21 |
| SB0 | Input/ output | Serial interface serial data input/output | Input | P25/SI0 |
| SB1 | | | | P26/SO0 |
| $\overline{SCK0}$ | Input/ output | Serial interface serial clock input/output | Input | P27 |
| $\overline{SCK1}$ | | | | P22 |
| STB | Output | Serial interface automatic transmit/receive strobe output | Input | P23 |
| BUSY | Input | Serial interface automatic transmit/receive busy input | Input | P24 |

**(2) Non-port pins (2/2)**

| Pin Name | I/O | Function | After Reset | Alternate Function |
|---|---|---|---|---|
| TI0 | Input | External count clock input to 16-bit timer (TM0) | Input | P00/INTP0 |
| TI1 | | External count clock input to 8-bit timer (TM1) | | P33 |
| TI2 | | External count clock input to 8-bit timer (TM2) | | P34 |
| TO0 | Output | 16-bit timer (TM0) output (shared as 14-bit PWM output) | Input | P30 |
| TO1 | | 8-bit timer (TM1) output | | P31 |
| TO2 | | 8-bit timer (TM2) output | | P32 |
| PCL | Output | Clock output (for main system clock, subsystem clock trimming) | Input | P35 |
| BUZ | Output | Buzzer output | Input | P36 |
| AD0 to AD7 | Input/ output | Lower address/data bus for expanding memory externally | Input | P40 to P47 |
| A8 to A15 | Output | Higher address bus for expanding memory externally | Input | P50 to P57 |
| $\overline{RD}$ | Output | Strobe signal output for read from external memory | Input | P64 |
| $\overline{WR}$ | | Strobe signal output for writing to external memory | | P65 |
| $\overline{WAIT}$ | Input | Wait insertion at external memory access | Input | P66 |
| ASTB | Output | Strobe output which latches the address information output at port 4 and port 5 to access external memory | Input | P67 |
| ANI0 to ANI7 | Input | A/D converter analog input | Input | P10 to P17 |
| $AV_{REF}$ | Input | A/D converter reference voltage input | — | — |
| $AV_{DD}$ | — | A/D converter analog power supply. Connect to $V_{DD}$. | — | — |
| $AV_{SS}$ | — | A/D converter ground potential. Connect to $V_{SS}$. | — | — |
| $\overline{RESET}$ | Input | System reset input | — | — |
| X1 | Input | Connecting crystal resonator for main system clock oscillation | — | — |
| X2 | — | | — | — |
| XT1 | Input | Connecting crystal resonator for subsystem clock oscillation | Input | P04 |
| XT2 | — | | — | — |
| $V_{DD}$ | — | Positive power supply | — | — |
| $V_{PP}$ | — | High voltage supply during program write/verify. In normal operating mode, connect directly to $V_{SS}$. | — | — |
| $V_{SS}$ | — | Ground potential | — | — |

### 2.2 Pins During PROM Programming Mode

| Pin | I/O | Function |
|---|---|---|
| $\overline{\text{RESET}}$ | Input | Sets PROM programming mode.<br>When +5 V or +12.5 V is applied to the $V_{PP}$ and low level is applied to $\overline{\text{RESET}}$ pin, microcontroller is shifted to PROM programming mode. |
| $V_{PP}$ | Input | High voltage supply during PROM programming mode setting and program write/verify |
| A0 to A16 | Input | Address bus |
| D0 to D7 | Input/ output | Data bus |
| $\overline{\text{CE}}$ | Input | PROM enable input/program pulse input |
| $\overline{\text{OE}}$ | Input | Read strobe input to PROM |
| $\overline{\text{PGM}}$ | Input | Program/program inhibit input in PROM programming mode |
| $V_{DD}$ | — | Positive power supply |
| $V_{SS}$ | — | Ground potential |

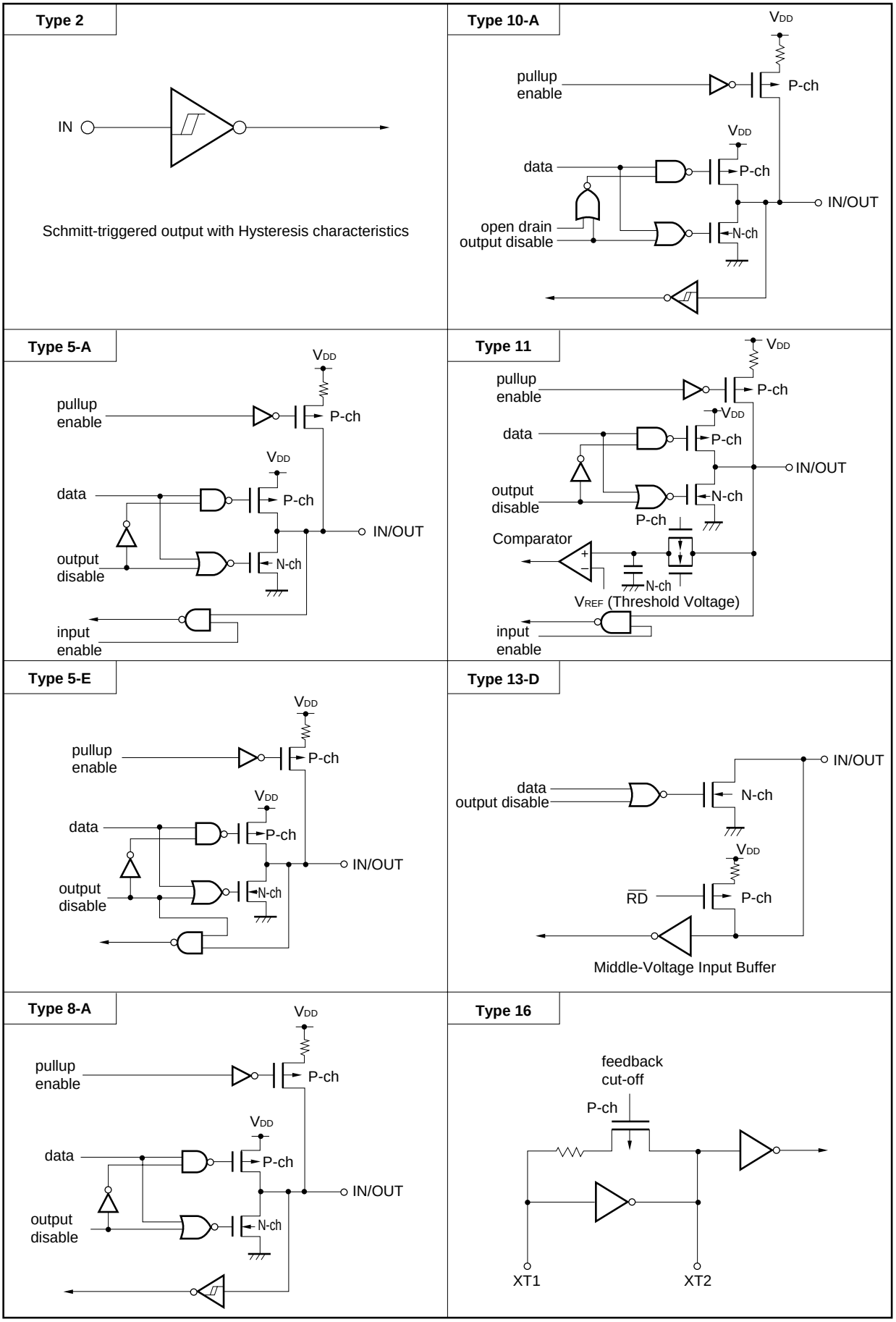
### 2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 2-1. For the input/output circuit configuration of each type, see Figure 2-1.

**Table 2-1. Types of Pin I/O Circuits**

| Pin Name | Input/output Circuit Type | I/O | Recommended Connection when Not Used |
|---|---|---|---|
| P00/INTP0/TI0 | 2 | Input | Connect to $V_{SS}$. |
| P01/INTP1 | 8-A | Input/output | Independently connect to $V_{SS}$ via a resistor. |
| P02/INTP2 | | | |
| P03/INTP3 | | | |
| P04/XT1 | 16 | Input | Connect to $V_{DD}$. |
| P10/ANI0 to P17/ANI7 | 11 | Input/output | Independently connect to $V_{DD}$ or $V_{SS}$ via a resistor. |
| P20/SI1 | 8-A | | |
| P21/SO1 | 5-A | | |
| P22/$\overline{\text{SCK1}}$ | 8-A | | |
| P23/STB | 5-A | | |
| P24/BUSY | 8-A | | |
| P25/SI0/SB0 | 10-A | | |
| P26/SO0/SB1 | | | |
| P27/$\overline{\text{SCK0}}$ | | | |
| P30/TO0 | 5-A | | |
| P31/TO1 | | | |
| P32/TO2 | | | |
| P33/TI1 | 8-A | | |
| P34/TI2 | | | |
| P35/PCL | 5-A | | |
| P36/BUZ | | | |
| P37 | | | |
| P40/AD0 to P47/AD7 | 5-E | | Independently connect to $V_{DD}$ via a resistor. |
| P50/A8 to P57/A15 | 5-A | | Independently connect to $V_{DD}$ or $V_{SS}$ via a resistor. |
| P60 to P63 | 13-D | | Independently connect to $V_{DD}$ via a resistor. |
| P64/$\overline{\text{RD}}$ | 5-A | | Independently connect to $V_{DD}$ or $V_{SS}$ via a resistor. |
| P65/$\overline{\text{WR}}$ | | | |
| P66/$\overline{\text{WAIT}}$ | | | |
| P67/ASTB | | | |
| $\overline{\text{RESET}}$ | 2 | Input | — |
| XT2 | 16 | — | Leave open. |
| $AV_{REF}$ | — | | Connect to $V_{SS}$. |
| $AV_{DD}$ | | | Connect to $V_{DD}$. |
| $AV_{SS}$ | | | Connect to $V_{SS}$. |
| $V_{PP}$ | | | Connect directly to $V_{SS}$. |

**Figure 2-1. Pin Input/Output Circuits**



## 3. INTERNAL MEMORY SIZE SWITCHING REGISTER (IMS)

This register is used to disable the use of part of the internal memory by software. By setting this register (IMS), it is possible to get the same memory map as that of the mask ROM versions with a different internal memory (ROM, RAM).

IMS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets IMS to CFH.

**Figure 3-1. Internal Memory Size Switching Register Format**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| IMS | RAM2 | RAM1 | RAM0 | 0 | ROM3 | ROM2 | ROM1 | ROM0 | FFF0H | CFH | W |

| ROM3 | ROM2 | ROM1 | ROM0 | Selection of Internal ROM Capacity |
|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 8 Kbytes |
| 0 | 1 | 0 | 0 | 16 Kbytes |
| 0 | 1 | 1 | 0 | 24 Kbytes |
| 1 | 0 | 0 | 0 | 32 Kbytes |
| 1 | 0 | 1 | 0 | 40 Kbytes |
| 1 | 1 | 0 | 0 | 48 Kbytes |
| 1 | 1 | 1 | 0 | 56 Kbytes[Note] |
| 1 | 1 | 1 | 1 | 60 Kbytes |
| Other than above | | | | Setting prohibited |

| RAM2 | RAM1 | RAM0 | Selection of Internal High-Speed RAM Capacity |
|---|---|---|---|
| 0 | 1 | 0 | 512 bytes |
| 1 | 1 | 0 | 1024 bytes |
| Other than above | | | Setting prohibited |

**Note** When the external device expansion function is used, the internal ROM capacity should be set to 56 Kbytes or less.

Table 3-1 shows the setting values of IMS which make the memory map the same as that of the mask ROM versions.

**Table 3-1. Internal Memory Size Switching Register Setting Values**

| Target Mask ROM Versions | IMS Setting Value |
|---|---|
| μPD78011F(A) | 42H |
| μPD78012F(A) | 44H |
| μPD78013F(A) | C6H |
| μPD78014F(A) | C8H |
| μPD78015F(A) | CAH |
| μPD78016F(A) | CCH |
| μPD78018F(A) | CFH |

## 4. INTERNAL EXPANSION RAM SIZE SWITCHING REGISTER (IXS)

This register is used to disable the use of part of the internal expansion RAM capacity by software. By setting this register (IXS), it is possible to get the same memory map as that of the mask ROM versions with a different internal expansion RAM.

IXS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets IXS to 0AH.

**Figure 4-1. Internal Expansion RAM Size Switching Register Format**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| IXS | 0 | 0 | 0 | 0 | IXRAM3 | IXRAM2 | IXRAM1 | IXRAM0 | FFF4H | 0AH | W |

| IXRAM3 | IXRAM2 | IXRAM1 | IXRAM0 | Selection of Internal Expansion RAM Capacity |
|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 1024 bytes (F400H to F7FFH) |
| 1 | 0 | 1 | 1 | 512 bytes (F600H to F7FFH) |
| 1 | 1 | 0 | 0 | 0 bytes |
| Other than above | | | | Setting prohibited |

Table 4-1 shows the setting values of IXS which make the memory map the same as that of the mask ROM versions.

**Table 4-1. Internal Expansion RAM Size Switching Register Setting Values**

| Target Mask ROM Versions | IXS Setting Value |
|---|---|
| μPD78011F(A) | 0CH **Note** |
| μPD78012F(A) | |
| μPD78013F(A) | |
| μPD78014F(A) | |
| μPD78015F(A) | 0BH |
| μPD78016F(A) | |
| μPD78018F(A) | 0AH |

**Note** Even if a program for the μPD78P018F(A) in which "MOV IXS, #0CH" is written is executed in the μPD78011F(A), 78012F(A), 78013F(A), and 78014F(A), the operations are not affected.

## 5. PROM PROGRAMMING

The μPD78P018F(A) has an internal 60-Kbyte PROM as a program memory. For programming, set the PROM programming mode by setting the $V_{PP}$ and $\overline{RESET}$ pins. For handling unused pins, refer to "**PIN CONFIGURATION (Top View) (2) PROM programming mode**."

**Caution When writing a program, use locations 0000H-EFFFH (Specify the last address as EFFFH). You cannot write a program using a PROM programmer that cannot specify the addresses to write.**

### 5.1 Operating Modes

When +5 V or +12.5 V is applied to the $V_{PP}$ pin and the low-level signal is applied to the $\overline{RESET}$ pin, the PROM programming mode is set. This mode will become the operating mode as shown in Table 5-1 when the $\overline{CE}$, $\overline{OE}$, and $\overline{PGM}$ pins are set as shown.

Further, when the read mode is set, it is possible to read the contents of the PROM.

**Table 5-1. Operating Modes of PROM Programming**

| Pin / Operating Mode | $\overline{RESET}$ | $V_{PP}$ | $V_{DD}$ | $\overline{CE}$ | $\overline{OE}$ | $\overline{PGM}$ | D0 to D7 |
|---|---|---|---|---|---|---|---|
| Page data latch | L | +12.5 V | +6.5 V | H | L | H | Data input |
| Page write | | | | H | H | L | High-impedance |
| Byte write | | | | L | H | L | Data input |
| Program verify | | | | L | L | H | Data output |
| Program inhibit | | | | × | H | H | High-impedance |
| | | | | × | L | L | |
| Read | | +5 V | +5 V | L | L | H | Data output |
| Output disable | | | | L | H | × | High-impedance |
| Standby | | | | H | × | × | High-impedance |

× : L or H

**(1) Read mode**

Read mode is set if $\overline{CE}$ = L, $\overline{OE}$ = L is set.

**(2) Output disable mode**

Data output becomes high-impedance, and is in the output disable mode, if $\overline{OE}$ = H is set.

Therefore, it allows data to be read from any device by controlling the $\overline{OE}$ pin, if multiple μPD78P018F(A)s are connected to the data bus.

**(3) Standby mode**

Standby mode is set if $\overline{CE}$ = H is set.

In this mode, data outputs become high-impedance irrespective of the $\overline{OE}$ status.

**(4) Page data latch mode**

Page data latch mode is set if $\overline{CE}$ = H, $\overline{PGM}$ = H, $\overline{OE}$ = L are set at the beginning of page write mode.

In this mode, 1 page 4-byte data is latched in an internal address/data latch circuit.

**(5) Page write mode**

After 1 page 4 bytes of addresses and data are latched in the page data latch mode, a page write is executed by applying a 0.1-ms program pulse (active low) to the $\overline{PGM}$ pin with $\overline{CE}$ = H, $\overline{OE}$ = H. Then, program verification can be performed, if $\overline{CE}$ = L, $\overline{OE}$ = L are set.

If programming is not performed by a one-time program pulse, X (X ≤ 10) write and verification operations should be executed repeatedly.

**(6) Byte write mode**

Byte write is executed when a 0.1-ms program pulse (active low) is applied to the $\overline{PGM}$ pin with $\overline{CE}$ = L, $\overline{OE}$ = H. Then, program verification can be performed if $\overline{OE}$ = L is set.

If programming is not performed by a one-time program pulse, X (X ≤ 10) write and verification operations should be executed repeatedly.

**(7) Program verify mode**

Program verify mode is set if $\overline{CE}$ = L, $\overline{PGM}$ = H, $\overline{OE}$ = L are set. In this mode, check if the write operation was performed correctly, after the write.

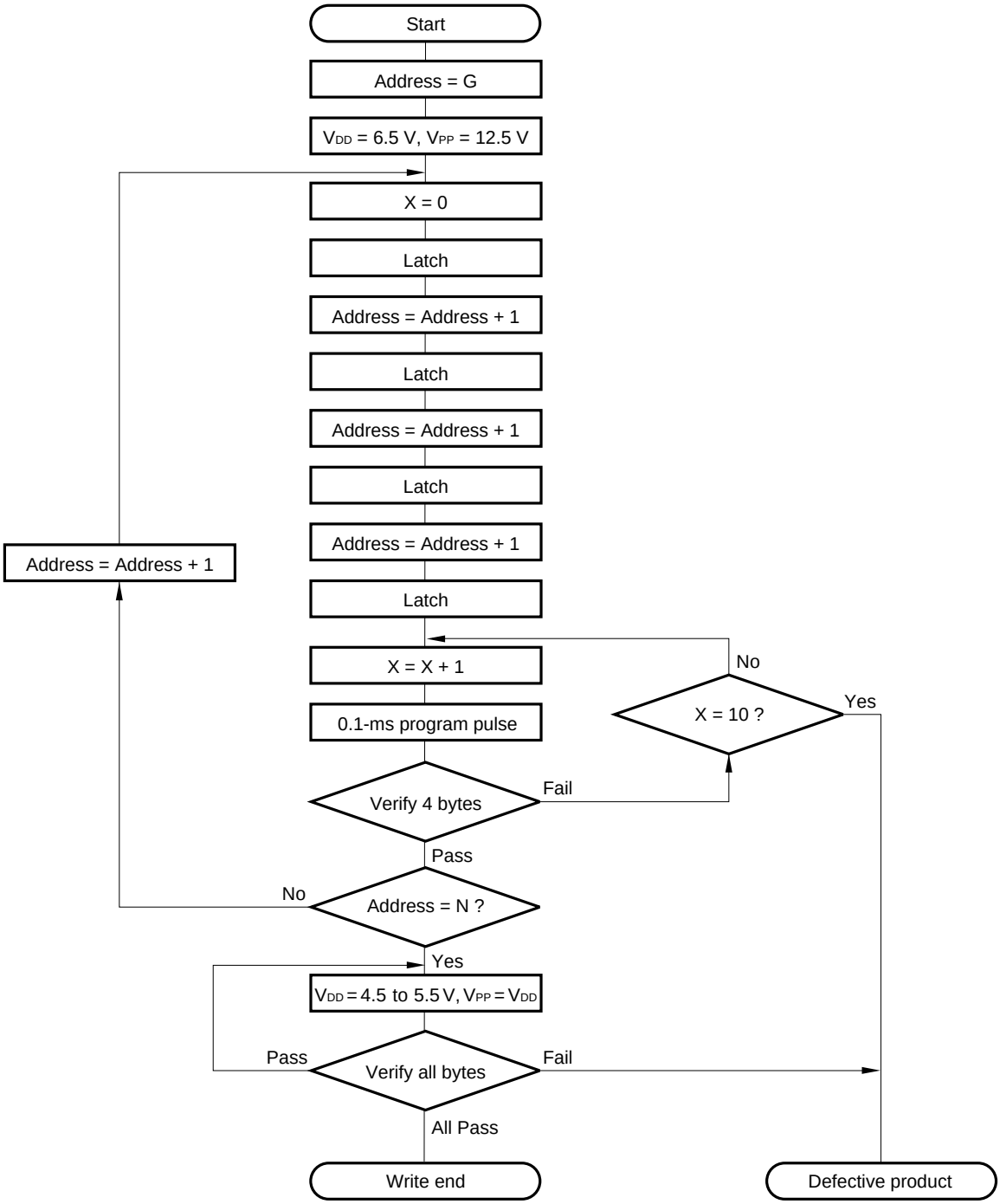
**(8) Program inhibit mode**

Program inhibit mode is used when the $\overline{OE}$ pin, $V_{PP}$ pin, and D0 to D7 pins of multiple μPD78P018F(A)s are connected in parallel and a write is performed to one of those devices.

When a write operation is performed, the page write mode or byte write mode described above is used. At this time, a write is not performed to a device which has the $\overline{PGM}$ pin driven high.

### 5.2 PROM Write Procedure

**Figure 5-1. Page Program Mode Flow Chart**




G = Start address

N = Program last address

**Figure 5-2. Page Program Mode Timing**

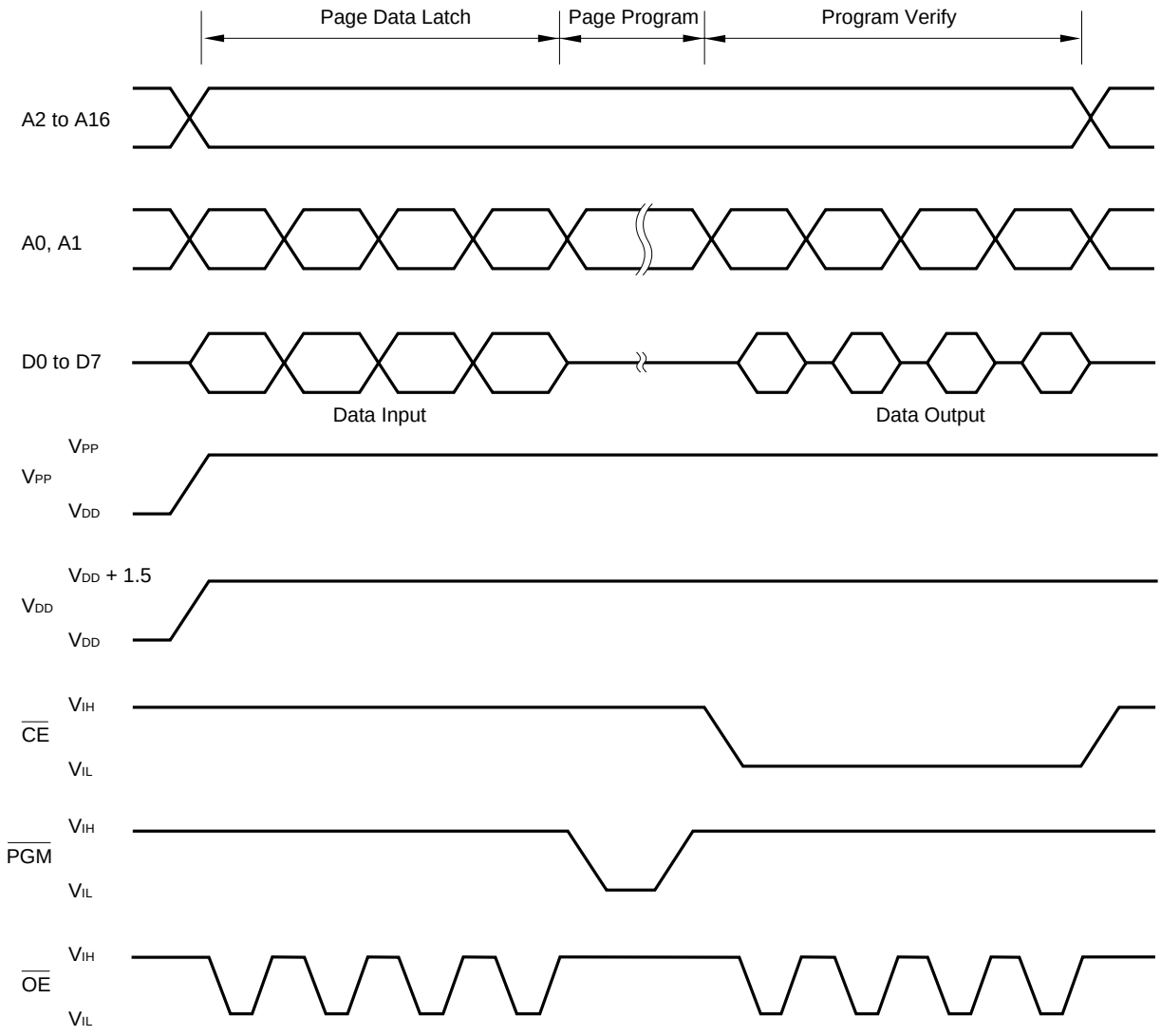
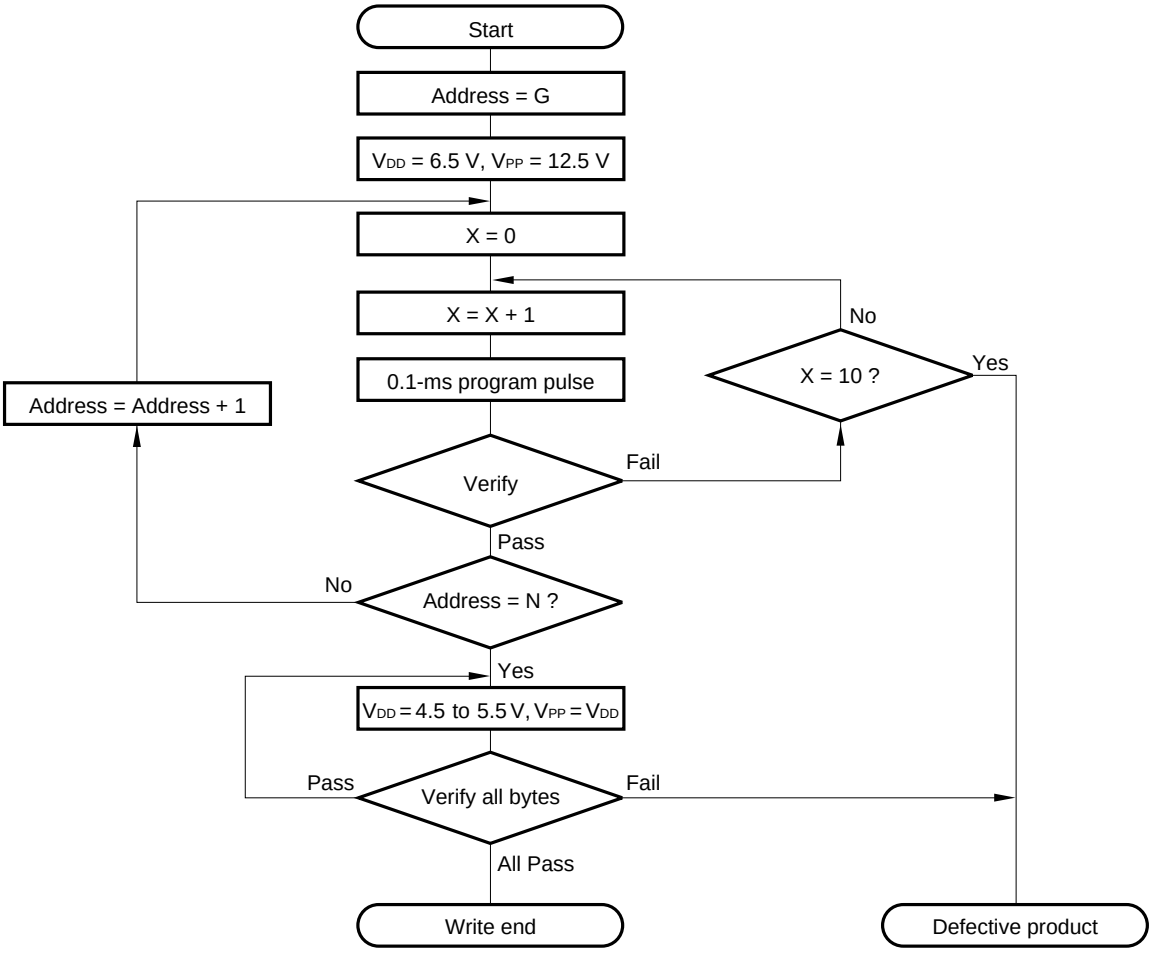


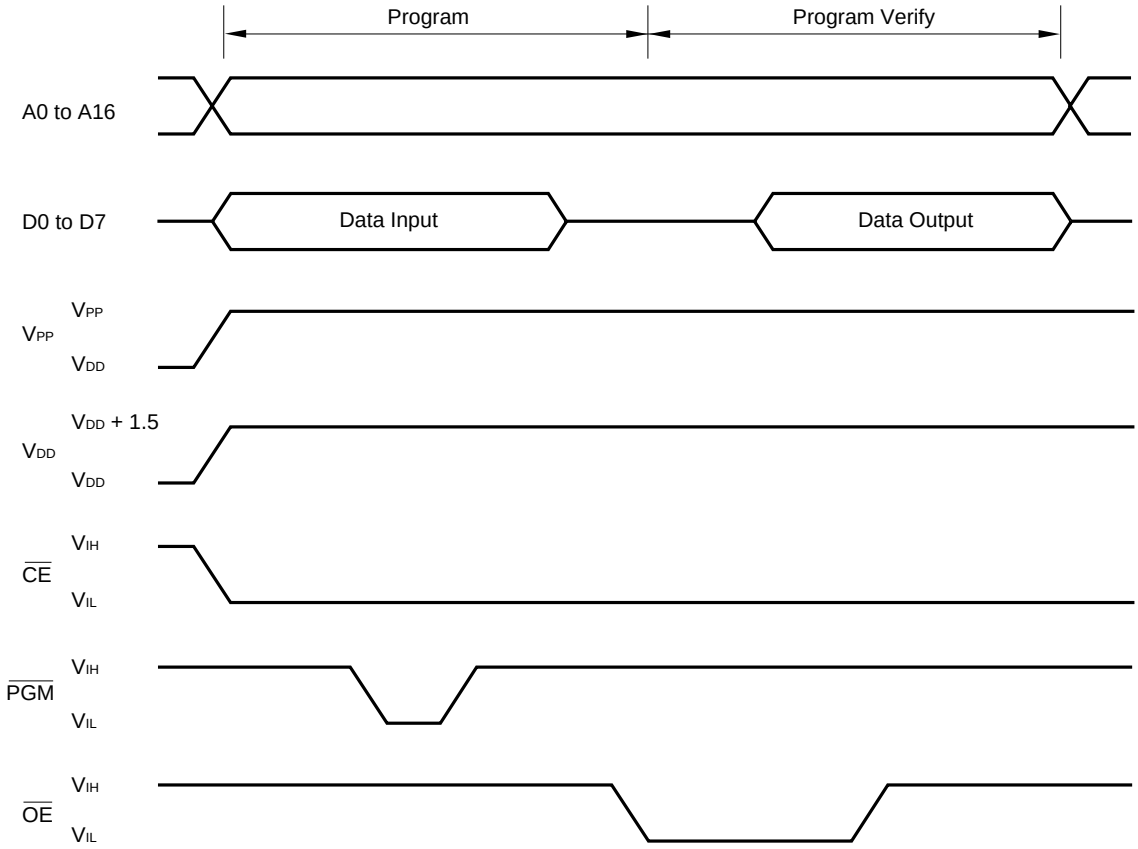
**Figure 5-3. Byte Program Mode Flow Chart**




G = Start address

N = Program last address

**Figure 5-4. Byte Program Mode Timing**




**Cautions 1. $V_{DD}$ should be applied before $V_{PP}$ and cut after $V_{PP}$.**

**2. $V_{PP}$ must not exceed +13.5 V including overshoot.**

**3. Removing and reinserting while +12.5 V is applied to $V_{PP}$ may adversely affect reliability.**

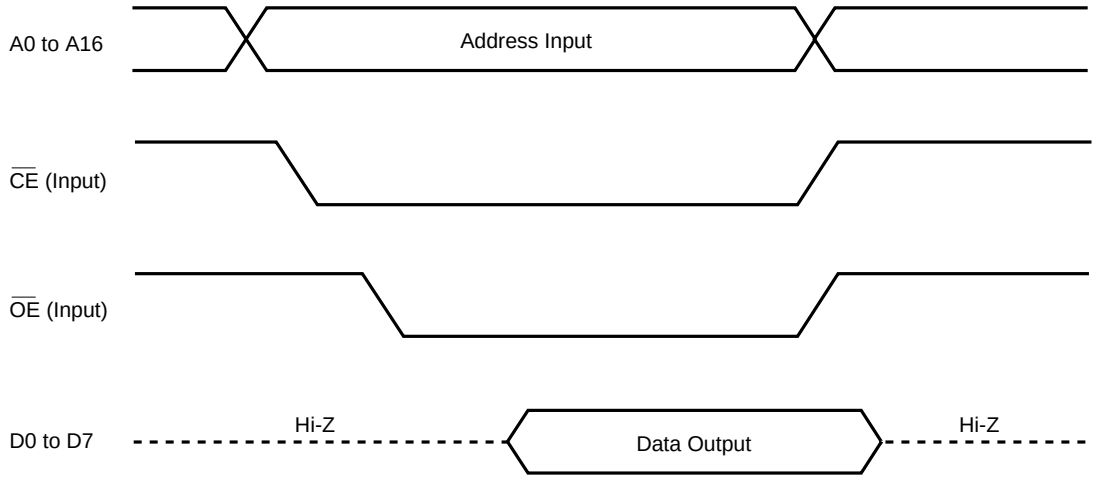
### 5.3 PROM Read Procedure

The contents of PROM are readable to the external data bus (D0 to D7) according to the read procedure shown below.

(1) Fix the $\overline{\text{RESET}}$ pin at low level, supply +5 V to the $V_{PP}$ pin, and handle all other unused pins as shown in "**PIN CONFIGURATION (Top View) (2) PROM programming mode**".
(2) Supply +5 V to the $V_{DD}$ and $V_{PP}$ pins.
(3) Input address of read data into the A0 to A16 pins.
(4) Read mode
(5) Output data to D0 to D7 pins.

The timings of the above steps (2) to (5) are shown in Figure 5-5.

**Figure 5-5. PROM Read Timings**



## 6. ONE-TIME PROM VERSION SCREENING

The one-time PROM versions (μPD78P018FCW(A), 78P018FGC(A)-AB8) cannot be tested completely by NEC before it is shipped, because of their structure. It is recommended to perform screening to verify PROM after writing necessary data and performing high-temperature storage under the conditions below.

| Storage Temperature | Storage Time |
|---|---|
| 125°C | 24 hours |

NEC provides for a fee one-time PROM writing, marking, screening, and verify service for products designated as "QTOP Microcontrollers." For details, contact an NEC sales representative.

## 7. ELECTRICAL SPECIFICATIONS

**Absolute Maximum Ratings ($T_A$ = 25°C)**

| Parameter | Symbol | Test Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | | –0.3 to +7.0 | V |
| | $V_{PP}$ | | | –0.3 to +13.5 | V |
| | $AV_{DD}$ | | | –0.3 to $V_{DD}$ + 0.3 | V |
| | $AV_{REF}$ | | | –0.3 to $V_{DD}$ + 0.3 | V |
| | $AV_{SS}$ | | | –0.3 to +0.3 | V |
| Input voltage | $V_{I1}$ | P00 to P04, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, X1, X2, XT2, $\overline{RESET}$ | | –0.3 to $V_{DD}$ + 0.3 | V |
| | $V_{I2}$ | P60 to P63 | Open-drain | –0.3 to +16 | V |
| | $V_{I3}$ | A9 | PROM programming mode | –0.3 to +13.5 | V |
| Output voltage | $V_O$ | | | –0.3 to $V_{DD}$ + 0.3 | V |
| Analog input voltage | $V_{AN}$ | P10 to P17 | Analog input pin | $AV_{SS}$ – 0.3 to $AV_{REF}$ + 0.3 | V |
| Output current, high | $I_{OH}$ | 1 pin | | –10 | mA |
| | | Total for P10 to P17, P20 to P27, P30 to P37 | | –15 | mA |
| | | Total for P01 to P03, P40 to P47, P50 to P57, P60 to P67 | | –15 | mA |
| Output current, low | $I_{OL}$ **Note** | 1 pin | Peak value | 30 | mA |
| | | | rms value | 15 | mA |
| | | Total for P40 to P47, P50 to P55 | Peak value | 100 | mA |
| | | | rms value | 70 | mA |
| | | Total for P01 to P03, P56, P57, P60 to P67 | Peak value | 100 | mA |
| | | | rms value | 70 | mA |
| | | Total for P01 to P03, P64 to P67 | Peak value | 50 | mA |
| | | | rms value | 20 | mA |
| | | Total for P10 to P17, P20 to P27, P30 to P37 | Peak value | 50 | mA |
| | | | rms value | 20 | mA |
| Operating ambient temperature | $T_A$ | | | –40 to +85 | °C |
| Storage temperature | $T_{stg}$ | | | –65 to +150 | °C |

**Note** The rms value should be calculated as follows: [rms value] = [Peak value] × $\sqrt{Duty}$

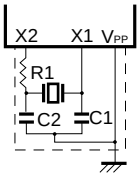
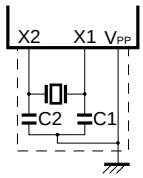
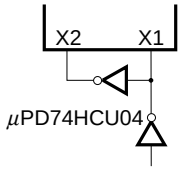
**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Capacitance ($T_A$ = 25°C, $V_{DD}$ = $V_{SS}$ = 0 V )**

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | f = 1 MHz Unmeasured pins returned to 0 V | | | | 15 | pF |
| I/O capacitance | $C_{IO}$ | f = 1 MHz Unmeasured pins returned to 0 V | P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67 | | | 15 | pF |
| | | | P60 to P63 | | | 20 | pF |

**Remark** Unless specified otherwise, the characteristics of an alternate-function pins are the same as those of port pins.

**Main System Clock Oscillator Characteristics ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Resonator | Recommended Circuit | Parameter | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Ceramic resonator |  | Oscillation frequency ($f_X$) **Note 1** | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1 | | 10 | MHz |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | 1 | | 5 | |
| | | Oscillation stabilization time **Note 2** | After $V_{DD}$ reaches oscillation voltage range MIN. | | | 4 | ms |
| Crystal resonator |  | Oscillation frequency ($f_X$) **Note 1** | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1 | | 10 | MHz |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | 1 | | 5 | |
| | | Oscillation stabilization time **Note 2** | $V_{DD}$ = 4.5 to 5.5 V | | | 10 | ms |
| | | | | | | 30 | |
| External clock |  | X1 input frequency ($f_X$) **Note 1** | | 1.0 | | 10.0 | MHz |
| | | X1 input high-/low-level width ($t_{XH}$ , $t_{XL}$) | | 45 | | 500 | ns |

**Notes 1.** Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

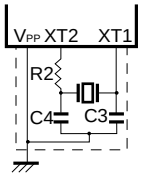
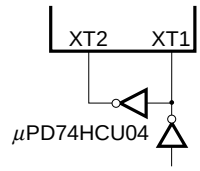
**2.** Time required to stabilize oscillation after reset or STOP mode release.

**Cautions 1. When using the main system clock oscillator, wire the area enclosed by the broken line in the above figures as follows to avoid an adverse effect from wiring capacitance.**

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always keep the ground point of the oscillator capacitor to the same potential as $V_{SS}$.**
- **Do not ground the capacitor to a ground pattern in which a high current flows.**
- **Do not fetch signals from the oscillator.**

**2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.**

**Subsystem Clock Oscillator Characteristics ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Resonator | Recommended Circuit | Parameter | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Crystal resonator |  | Oscillation frequency ($f_{XT}$) **Note 1** | | 32 | 32.768 | 35 | kHz |
| | | Oscillation stabilization time **Note 2** | $V_{DD}$ = 4.5 to 5.5 V | | 1.2 | 2 | s |
| | | | | | | 10 | |
| External clock |  | X1 input frequency ($f_{XT}$) **Note 1** | | 32 | | 100 | kHz |
| | | X1 input high-/low-level width ($t_{XTH}$, $t_{XTL}$) | | 5 | | 15 | μs |

**Notes 1.** Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

**2.** Time required to stabilize oscillation after $V_{DD}$ reaches oscillator voltage MIN.

**Cautions 1. When using the subsystem clock oscillator, wire the area enclosed by the broken line in the above figures as follows to avoid an adverse effect from wiring capacitance.**

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always keep the ground point of the oscillator capacitor to the same potential as $V_{SS}$.**
- **Do not ground the capacitor to a ground pattern in which a high current flows.**
- **Do not fetch signals from the oscillator.**

**2. The subsystem clock oscillator is a low-amplitude circuit in order to achieve a low consumption current, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.**

## RECOMMENDED OSCILLATOR CONSTANTS

**Main system clock: Ceramic resonator ($T_A$ = –40 to +85°C)**

| Manufacturer | Name | Frequency (MHz) | Recommended Oscillator Constants | | Oscillation Voltage Range | | Remarks |
|---|---|---|---|---|---|---|---|
| | | | C1 (pF) | C2 (pF) | MIN. (V) | MAX. (V) | |
| TDK | CCR4.0MC3 | 4.00 | On-Chip | On-Chip | 1.8 | 5.5 | On-chip capacitor, surface mounting type |
| | FCR4.0MC5 | 4.00 | On-Chip | On-Chip | 1.8 | 5.5 | On-chip capacitor, insertion type |
| | CCR4.19MC3 | 4.19 | On-Chip | On-Chip | 1.8 | 5.5 | On-chip capacitor, surface mounting type |
| | FCR4.19MC5 | 4.19 | On-Chip | On-Chip | 1.8 | 5.5 | On-chip capacitor, insertion type |
| | CCR5.00MC3 | 5.00 | On-Chip | On-Chip | 1.8 | 5.5 | On-chip capacitor, surface mounting type |
| | FCR5.00MC5 | 5.00 | On-Chip | On-Chip | 1.8 | 5.5 | On-chip capacitor, insertion type |
| | CCR8.00MC | 8.00 | On-Chip | On-Chip | 2.7 | 5.5 | On-chip capacitor, surface mounting type |
| | FCR8.00MC5 | 8.00 | On-Chip | On-Chip | 2.7 | 5.5 | On-chip capacitor, insertion type |
| | CCR8.38MC | 8.38 | On-Chip | On-Chip | 2.7 | 5.5 | On-chip capacitor, surface mounting type |
| | FCR8.38MC5 | 8.38 | On-Chip | On-Chip | 2.7 | 5.5 | On-chip capacitor, insertion type |
| | CCR10.00MC | 10.00 | On-Chip | On-Chip | 2.7 | 5.5 | On-chip capacitor, surface mounting type |
| | FCR10.00MC5 | 10.00 | On-Chip | On-Chip | 2.7 | 5.5 | On-chip capacitor, insertion type |
| Murata Mfg. Co., Ltd. | CSA4.00MG | 4.00 | 30 | 30 | 1.8 | 5.5 | Insertion type |
| | CST4.00MGW | 4.00 | On-Chip | On-Chip | 1.8 | 5.5 | On-chip capacitor, insertion type |
| | CSA4.19MG | 4.19 | 30 | 30 | 1.8 | 5.5 | Insertion type |
| | CST4.19MGW | 4.19 | On-Chip | On-Chip | 1.8 | 5.5 | On-chip capacitor, insertion type |
| | CSA5.00MG | 5.00 | 30 | 30 | 1.8 | 5.5 | Insertion type |
| | CST5.00MGW | 5.00 | On-Chip | On-Chip | 1.8 | 5.5 | On-chip capacitor, insertion type |
| | CSA8.00MTZ | 8.00 | 30 | 30 | 2.7 | 5.5 | Insertion type |
| | CST8.00MTW | 8.00 | On-Chip | On-Chip | 2.7 | 5.5 | On-chip capacitor, insertion type |
| | CSA8.38MTZ | 8.38 | 30 | 30 | 2.7 | 5.5 | Insertion type |
| | CST8.38MTW | 8.38 | On-Chip | On-Chip | 2.7 | 5.5 | On-chip capacitor, insertion type |
| | CSA10.00MTZ | 10.00 | 30 | 30 | 2.7 | 5.5 | Insertion type |
| | CST10.00MTW | 10.00 | On-Chip | On-Chip | 2.7 | 5.5 | On-chip capacitor, insertion type |

**Caution The oscillator constants and oscillation voltage range indicate conditions for stable oscillation, but do not guarantee oscillation frequency accuracy. If oscillation frequency accuracy is required for actual circuits, it is necessary to adjust the oscillation frequency of the oscillator in the actual circuit. Please contact directly the manufacturer of the resonator to be used.**

**Main system clock: Ceramic resonator ($T_A$ = –20 to +80°C)**

| Manufacturer | Name | Frequency (MHz) | Recommended Oscillator Constants | | Oscillation Voltage Range | | Remarks |
|---|---|---|---|---|---|---|---|
| | | | C1 (pF) | C2 (pF) | MIN. (V) | MAX. (V) | |
| Kyocera Corporation | PBRC4.00A | 4.00 | 33 | 33 | 1.8 | 5.5 | Surface mounting type |
| | PBRC4.00B | 4.00 | On-Chip | On-Chip | 1.8 | 5.5 | On-chip capacitor, surface mounting type |
| | KBR-4.00MSA | 4.00 | 33 | 33 | 1.8 | 5.5 | Insertion type |
| | KBR-4.00MKS | 4.00 | On-Chip | On-Chip | 1.8 | 5.5 | On-chip capacitor, insertion type |
| | PBRC5.00A | 5.00 | 33 | 33 | 1.8 | 5.5 | Surface mounting type |
| | PBRC5.00B | 5.00 | On-Chip | On-Chip | 1.8 | 5.5 | On-chip capacitor, surface mounting type |
| | KBR-5.00MSA | 5.00 | 33 | 33 | 1.8 | 5.5 | Insertion type |
| | KBR-5.00MKS | 5.00 | On-Chip | On-Chip | 1.8 | 5.5 | On-chip capacitor, insertion type |
| | KBR-8M | 8.00 | 33 | 33 | 2.7 | 5.5 | Insertion type |
| | KBR-10M | 10.00 | 33 | 33 | 2.7 | 5.5 | Insertion type |

**Caution The oscillator constants and oscillation voltage range indicate conditions for stable oscillation, but do not guarantee oscillation frequency accuracy. If oscillation frequency accuracy is required for actual circuits, it is necessary to adjust the oscillation frequency of the oscillator in the actual circuit. Please contact directly the manufacturer of the resonator to be used.**

**DC Characteristics ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH1}$ | P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67 | $V_{DD}$ = 2.7 to 5.5 V | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| | | | | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH2}$ | P00 to P03, P20, P22, P24 to P27, P33, P34, $\overline{RESET}$ | $V_{DD}$ = 2.7 to 5.5 V | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| | | | | 0.85$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH3}$ | P60 to P63 (N-ch open-drain) | $V_{DD}$ = 2.7 to 5.5 V | 0.7$V_{DD}$ | | 15 | V |
| | | | | 0.8$V_{DD}$ | | 15 | V |
| | $V_{IH4}$ | X1, X2 | $V_{DD}$ = 2.7 to 5.5 V | $V_{DD}$ – 0.5 | | $V_{DD}$ | V |
| | | | | $V_{DD}$ – 0.2 | | $V_{DD}$ | V |
| | $V_{IH5}$ | XT1/P04, XT2 | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| | | | 2.7 V ≤ $V_{DD}$ < 4.5 V | 0.9$V_{DD}$ | | $V_{DD}$ | V |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V **Note** | 0.9$V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67 | $V_{DD}$ = 2.7 to 5.5 V | 0 | | 0.3$V_{DD}$ | V |
| | | | | 0 | | 0.2$V_{DD}$ | V |
| | $V_{IL2}$ | P00 to P03, P20, P22, P24 to P27, P33, P34, $\overline{RESET}$ | $V_{DD}$ = 2.7 to 5.5 V | 0 | | 0.2$V_{DD}$ | V |
| | | | | 0 | | 0.15$V_{DD}$ | V |
| | $V_{IL3}$ | P60 to P63 | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | 0 | | 0.3$V_{DD}$ | V |
| | | | 2.7 V ≤ $V_{DD}$ < 4.5 V | 0 | | 0.2$V_{DD}$ | V |
| | | | | 0 | | 0.1$V_{DD}$ | V |
| | $V_{IL4}$ | X1, X2 | $V_{DD}$ = 2.7 to 5.5 V | 0 | | 0.4 | V |
| | | | | 0 | | 0.2 | V |
| | $V_{IL5}$ | XT1/P04, XT2 | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | 0 | | 0.2$V_{DD}$ | V |
| | | | 2.7 V ≤ $V_{DD}$ < 4.5 V | 0 | | 0.1$V_{DD}$ | V |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V **Note** | 0 | | 0.1$V_{DD}$ | V |
| Output voltage, high | $V_{OH1}$ | $V_{DD}$ = 4.5 to 5.5 V, $I_{OH}$ = –1 mA | | $V_{DD}$ – 1.0 | | | V |
| | | $I_{OH}$ = –100 μA | | $V_{DD}$ – 0.5 | | | V |
| Output voltage, low | $V_{OL1}$ | P50 to P57, P60 to P63 | $V_{DD}$ = 4.5 to 5.5 V, $I_{OL}$ = 15 mA | | 0.4 | 2.0 | V |
| | | P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67 | $V_{DD}$ = 4.5 to 5.5 V, $I_{OL}$ = 1.6 mA | | | 0.4 | V |
| | $V_{OL2}$ | SB0, SB1, $\overline{SCK0}$ | $V_{DD}$ = 4.5 to 5.5 V, open-drain pulled-up (R = 1 kΩ) | | | 0.2$V_{DD}$ | V |
| | $V_{OL3}$ | $I_{OL}$ = 400 μA | | | | 0.5 | V |

**Note** When using XT1/P04 as P04, the inverse phase of P04 should be input to XT2 using an inverter.

**Remark** Unless specified otherwise, the characteristics of an alternate-function pins are the same as those of port pins.

**DC Characteristics ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input leakage current, high | $I_{LIH1}$ | $V_{IN} = V_{DD}$ | P00 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, $\overline{RESET}$ | | | 3 | μA |
| | $I_{LIH2}$ | | X1, X2, XT1/P04, XT2 | | | 20 | μA |
| | $I_{LIH3}$ | $V_{IN}$ = 15 V | P60 to P63 | | | 80 | μA |
| Input leakage current, low | $I_{LIL1}$ | $V_{IN}$ = 0 V | P00 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, $\overline{RESET}$ | | | –3 | μA |
| | $I_{LIL2}$ | | X1, X2, XT1/P04, XT2 | | | –20 | μA |
| | $I_{LIL3}$ | | P60 to P63 | | | –3 Note | μA |
| Output leakage current, high | $I_{LOH}$ | $V_{OUT} = V_{DD}$ | | | | 3 | μA |
| Output leakage current, low | $I_{LOL}$ | $V_{OUT}$ = 0 V | | | | –3 | μA |
| Software pull-up resistor | R | $V_{IN}$ = 0 V, P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67 | | 15 | 40 | 90 | kΩ |

**Note** For P60 to P63, a low-level input leak current of –200 μA (MAX.) flows only during the 3 clocks (no-wait time) after an instruction has been executed to read out port 6 (P6) or port mode register 6 (PM6). Outside the period of 3 clocks following execution a read-out instruction, the current is –3 μA (MAX.).

**Remark** Unless specified otherwise, the characteristics of an alternate-function pins are the same as those of port pins.

**DC Characteristics ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | 10.00-MHz crystal oscillation operation mode | $V_{DD}$ = 5.0 V ±10 % Note 2 | | 12.0 | 24.0 | mA |
| | | | $V_{DD}$ = 3.0 V ±10 % Note 3 | | 1.4 | 2.8 | mA |
| | $I_{DD2}$ | 10.00-MHz crystal oscillation HALT mode | $V_{DD}$ = 5.0 V ±10 % Note 2 | | 4.0 | 8.0 | mA |
| | | | $V_{DD}$ = 3.0 V ±10 % Note 3 | | 1.4 | 2.8 | mA |
| | $I_{DD3}$ | 32.768-kHz crystal oscillation operation mode Note 4 | $V_{DD}$ = 5.0 V ±10 % | | 150 | 300 | μA |
| | | | $V_{DD}$ = 3.0 V ±10 % | | 100 | 200 | μA |
| | | | $V_{DD}$ = 2.0 V ±10 % | | 60 | 120 | μA |
| | $I_{DD4}$ | 32.768-kHz crystal oscillation HALT mode Note 4 | $V_{DD}$ = 5.0 V ±10 % | | 25 | 50 | μA |
| | | | $V_{DD}$ = 3.0 V ±10 % | | 5 | 15 | μA |
| | | | $V_{DD}$ = 2.0 V ±10 % | | 2.5 | 10 | μA |
| | $I_{DD5}$ | XT1 = $V_{DD}$ STOP mode when using feedback resistor | $V_{DD}$ = 5.0 V ±10 % | | 2.0 | 30 | μA |
| | | | $V_{DD}$ = 3.0 V ±10 % | | 1.0 | 10 | μA |
| | | | $V_{DD}$ = 2.0 V ±10 % | | 0.5 | 10 | μA |
| | $I_{DD6}$ | XT1 = $V_{DD}$ STOP mode when not using feedback resistor | $V_{DD}$ = 5.0 V ±10 % | | 0.1 | 30 | μA |
| | | | $V_{DD}$ = 3.0 V ±10 % | | 0.05 | 10 | μA |
| | | | $V_{DD}$ = 2.0 V ±10 % | | 0.05 | 10 | μA |

**Notes 1.** Refers to the current flowing to the $V_{DD}$ pin. The current flowing to the on-chip pull-up resistors, ports, and A/D converter is not included.

**2.** When operating at high-speed mode (when the processor clock control register (PCC) is set to 00H)

**3.** When operating at low-speed mode (when PCC is set to 04H)

**4.** When main system clock stopped.

### AC Characteristics

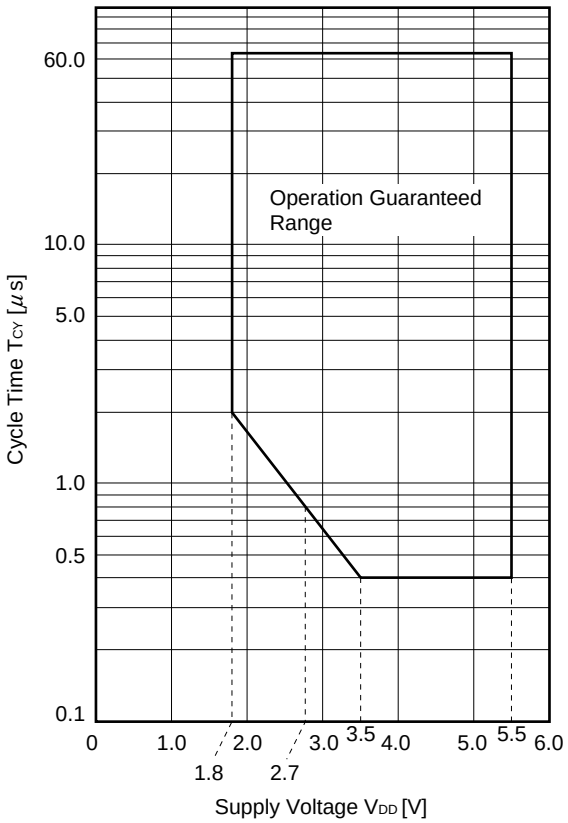
**(1) Basic Operation ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Cycle time (Min. instruction execution time) | $T_{CY}$ | Operating on main system clock | 3.5 V ≤ $V_{DD}$ ≤ 5.5 V | 0.4 | | 64 | μs |
| | | | 2.7 V ≤ $V_{DD}$ < 3.5 V | 0.8 | | 64 | μs |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | 2.0 | | 64 | μs |
| ★ | | Operating on subsystem clock | | 40 Note 1 | 122 | 125 | μs |
| TI0 input high-/low-level width | $t_{TIH0}$, $t_{TIL0}$ | 3.5 V ≤ $V_{DD}$ ≤ 5.5 V | | $2/f_{sam}$ + 0.1 Note 2 | | | μs |
| | | 2.7 V ≤ $V_{DD}$ < 3.5 V | | $2/f_{sam}$ + 0.2 Note 2 | | | μs |
| | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | $2/f_{sam}$ + 0.5 Note 2 | | | μs |
| TI1, TI2 input frequency | $f_{TI1}$ | $V_{DD}$ = 4.5 to 5.5 V | | 0 | | 4 | MHz |
| | | | | 0 | | 275 | kHz |
| TI1, TI2 input high-/low-level width | $t_{TIH1}$, $t_{TIL1}$ | $V_{DD}$ = 4.5 to 5.5 V | | 100 | | | ns |
| | | | | 1.8 | | | μs |
| Interrupt input high-/low-level width | $t_{INTH}$, $t_{INTL}$ | INTP0 | 3.5 V ≤ $V_{DD}$ ≤ 5.5 V | $2/f_{sam}$ + 0.1 Note 2 | | | μs |
| | | | 2.7 V ≤ $V_{DD}$ < 3.5 V | $2/f_{sam}$ + 0.2 Note 2 | | | μs |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | $2/f_{sam}$ + 0.5 Note 2 | | | μs |
| | | INTP1 to INTP3, KR0 to KR7 | $V_{DD}$ = 2.7 to 5.5 V | 10 | | | μs |
| | | | | 20 | | | μs |
| $\overline{\text{RESET}}$ low-level width | $t_{RSL}$ | $V_{DD}$ = 2.7 to 5.5 V | | 10 | | | μs |
| | | | | 20 | | | μs |

**Notes 1.** Value when external clock is used. When a crystal resonator is used, it is 114 μs (MIN.).

**2.** In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register (SCS), selection of $f_{sam}$ is possible between $f_X/2^{N+1}$, $f_X$/64, and $f_X$/128 (when N = 0 to 4).

**$T_{CY}$ vs. $V_{DD}$ (At main system clock operation)**



**(2) Read/Write Operation ($T_A$ = –40 to +85°C, $V_{DD}$ = 2.7 to 5.5 V)**

| Parameter | Symbol | Test Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| ASTB high-level width | $t_{ASTH}$ | | $0.5t_{CY}$ | | ns |
| Address setup time | $t_{ADS}$ | | $0.5t_{CY}$ – 30 | | ns |
| Address hold time | $t_{ADH}$ | | 50 | | ns |
| Data input time from address | $t_{ADD1}$ | | | $(2.5 + 2n)t_{CY}$ – 50 | ns |
| | $t_{ADD2}$ | | | $(3 + 2n)t_{CY}$ – 100 | ns |
| Data input time from $\overline{RD}\downarrow$ | $t_{RDD1}$ | | | $(1 + 2n)t_{CY}$ – 25 | ns |
| | $t_{RDD2}$ | | | $(2.5 + 2n)t_{CY}$ – 100 | ns |
| Read data hold time | $t_{RDH}$ | | 0 | | ns |
| $\overline{RD}$ low-level width | $t_{RDL1}$ | | $(1.5+2n)t_{CY}$ – 20 | | ns |
| | $t_{RDL2}$ | | $(2.5+2n)t_{CY}$ – 20 | | ns |
| $\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$ | $t_{RDWT1}$ | | | $0.5t_{CY}$ | ns |
| | $t_{RDWT2}$ | | | $1.5t_{CY}$ | ns |
| $\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$ | $t_{WRWT}$ | | | $0.5t_{CY}$ | ns |
| $\overline{WAIT}$ low-level width | $t_{WTL}$ | | $(0.5 + 2n)t_{CY}$ + 10 | $(2 + 2n)t_{CY}$ | ns |
| Write data setup time | $t_{WDS}$ | | 100 | | ns |
| Write data hold time | $t_{WDH}$ | Load resistance ≥ 5 kΩ | 20 | | ns |
| $\overline{WR}$ low-level width | $t_{WRL}$ | | $(2.5 + 2n)t_{CY}$ – 20 | | ns |
| $\overline{RD}\downarrow$ delay time from ASTB↓ | $t_{ASTRD}$ | | $0.5t_{CY}$ – 30 | | ns |
| $\overline{WR}\downarrow$ delay time from ASTB↓ | $t_{ASTWR}$ | | $1.5t_{CY}$ – 30 | | ns |
| ASTB↑ delay time from $\overline{RD}\uparrow$ in external fetch | $t_{RDAST}$ | | $t_{CY}$ – 10 | $t_{CY}$ + 40 | ns |
| Address hold time from $\overline{RD}\uparrow$ in external fetch | $t_{RDADH}$ | | $t_{CY}$ | $t_{CY}$ + 50 | ns |
| Write data output time from $\overline{RD}\uparrow$ | $t_{RDWD}$ | $V_{DD}$ = 4.5 to 5.5 V | $0.5t_{CY}$ + 5 | $0.5t_{CY}$ + 30 | ns |
| | | | $0.5t_{CY}$ + 15 | $0.5t_{CY}$ + 90 | ns |
| Write data output time from $\overline{WR}\downarrow$ | $t_{WRWD}$ | $V_{DD}$ = 4.5 to 5.5 V | 5 | 30 | ns |
| | | | 15 | 90 | ns |
| Address hold time from $\overline{WR}\uparrow$ | $t_{WRADH}$ | $V_{DD}$ = 4.5 to 5.5 V | $t_{CY}$ | $t_{CY}$ + 60 | ns |
| | | | $t_{CY}$ | $t_{CY}$ + 100 | ns |
| $\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$ | $t_{WTRD}$ | | $0.5t_{CY}$ | $2.5t_{CY}$ + 80 | ns |
| $\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$ | $t_{WTWR}$ | | $0.5t_{CY}$ | $2.5t_{CY}$ + 80 | ns |

**Remarks 1.** $t_{CY} = T_{CY}/4$

**2.** n indicates the number of waits.

### (3) Serial Interface ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)

#### (a) Serial Interface Channel 0

##### (i) 3-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $\overline{SCK0}$ cycle time | $t_{KCY1}$ | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | 800 | | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.5 V | 1600 | | | ns |
| | | 2.0 V ≤ $V_{DD}$ < 2.7 V | 3200 | | | ns |
| | | | 4800 | | | ns |
| $\overline{SCK0}$ high-/low-level width | $t_{KH1}$, $t_{KL1}$ | $V_{DD}$ = 4.5 to 5.5 V | $t_{KCY1}/2$ – 50 | | | ns |
| | | | $t_{KCY1}/2$ – 100 | | | ns |
| SI0 setup time (to $\overline{SCK0}$↑) | $t_{SIK1}$ | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | 100 | | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.5 V | 150 | | | ns |
| | | 2.0 V ≤ $V_{DD}$ < 2.7 V | 300 | | | ns |
| | | | 400 | | | ns |
| SI0 hold time (from $\overline{SCK0}$↑) | $t_{KSI1}$ | | 400 | | | ns |
| SO0 output delay time from $\overline{SCK0}$↓ | $t_{KSO1}$ | C = 100 pF **Note** | | | 300 | ns |

**Note** C is the load capacitance of $\overline{SCK0}$ and SO0 output lines.

##### (ii) 3-wire serial I/O mode ($\overline{SCK0}$... External clock input)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK0}$ cycle time | $t_{KCY2}$ | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | | 800 | | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.5 V | | 1600 | | | ns |
| | | 2.0 V ≤ $V_{DD}$ < 2.7 V | | 3200 | | | ns |
| | | | | 4800 | | | ns |
| $\overline{SCK0}$ high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | | 400 | | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.5 V | | 800 | | | ns |
| | | 2.0 V ≤ $V_{DD}$ < 2.7 V | | 1600 | | | ns |
| | | | | 2400 | | | ns |
| SI0 setup time (to $\overline{SCK0}$↑) | $t_{SIK2}$ | $V_{DD}$ = 2.0 to 5.5 V | | 100 | | | ns |
| | | | | 150 | | | ns |
| SI0 hold time (from $\overline{SCK0}$↑) | $t_{KSI2}$ | | | 400 | | | ns |
| SO0 output delay time from $\overline{SCK0}$↓ | $t_{KSO2}$ | C = 100 pF **Note** | $V_{DD}$ = 2.0 to 5.5 V | | | 300 | ns |
| | | | | | | 500 | ns |
| $\overline{SCK0}$ rise, fall time | $t_{R2}$, $t_{F2}$ | When external device expansion function is used | | | | 160 | ns |
| | | When external device expansion function is not used | When 16-bit timer output function is used | | | 700 | ns |
| | | | When 16-bit timer output function is not used | | | 1000 | ns |

**Note** C is the load capacitance of SO0 output line.

### (iii) SBI mode ($\overline{SCK0}$... Internal clock output)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK0}$ cycle time | $t_{KCY3}$ | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | | 800 | | | ns |
| | | 2.0 V ≤ $V_{DD}$ < 4.5 V | | 3200 | | | ns |
| | | | | 4800 | | | ns |
| $\overline{SCK0}$ high-/low-level width | $t_{KH3}$, $t_{KL3}$ | $V_{DD}$ = 4.5 to 5.5 V | | $t_{KCY3}$/2 – 50 | | | ns |
| | | | | $t_{KCY3}$/2 – 150 | | | ns |
| SB0, SB1 setup time (to $\overline{SCK0}$↑) | $t_{SIK3}$ | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | | 100 | | | ns |
| | | 2.0 V ≤ $V_{DD}$ < 4.5 V | | 300 | | | ns |
| | | | | 400 | | | ns |
| SB0, SB1 hold time (from $\overline{SCK0}$↑) | $t_{KSI3}$ | | | $t_{KCY3}$/2 | | | ns |
| SB0, SB1 output delay time from $\overline{SCK0}$↓ | $t_{KSO3}$ | R = 1 kΩ, C = 100 pF **Note** | $V_{DD}$ = 4.5 to 5.5 V | 0 | | 250 | ns |
| | | | | 0 | | 1000 | ns |
| SB0, SB1↓ from $\overline{SCK0}$↑ | $t_{KSB}$ | | | $t_{KCY3}$ | | | ns |
| $\overline{SCK0}$↓ from SB0, SB1↓ | $t_{SBK}$ | | | $t_{KCY3}$ | | | ns |
| SB0, SB1 high-level width | $t_{SBH}$ | | | $t_{KCY3}$ | | | ns |
| SB0, SB1 low-level width | $t_{SBL}$ | | | $t_{KCY3}$ | | | ns |

**Note** R and C are the load resistance and load capacitance of the SB0, SB1 and $\overline{SCK0}$ output lines.

### (iv) SBI mode ($\overline{SCK0}$... External clock input)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK0}$ cycle time | $t_{KCY4}$ | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | | 800 | | | ns |
| | | 2.0 V ≤ $V_{DD}$ < 4.5 V | | 3200 | | | ns |
| | | | | 4800 | | | ns |
| $\overline{SCK0}$ high-/low-level width | $t_{KH4}$, $t_{KL4}$ | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | | 400 | | | ns |
| | | 2.0 V ≤ $V_{DD}$ < 4.5 V | | 1600 | | | ns |
| | | | | 2400 | | | ns |
| SB0, SB1 setup time (to $\overline{SCK0}$↑) | $t_{SIK4}$ | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | | 100 | | | ns |
| | | 2.0 V ≤ $V_{DD}$ < 4.5 V | | 300 | | | ns |
| | | | | 400 | | | ns |
| SB0, SB1 hold time (from $\overline{SCK0}$↑) | $t_{KSI4}$ | | | $t_{KCY4}$/2 | | | ns |
| SB0, SB1 output delay time from $\overline{SCK0}$↓ | $t_{KSO4}$ | R = 1 kΩ, C = 100 pF **Note** | $V_{DD}$ = 4.5 to 5.5 V | 0 | | 300 | ns |
| | | | | 0 | | 1000 | ns |
| SB0, SB1↓ from $\overline{SCK0}$↑ | $t_{KSB}$ | | | $t_{KCY4}$ | | | ns |
| $\overline{SCK0}$↓ from SB0, SB1↓ | $t_{SBK}$ | | | $t_{KCY4}$ | | | ns |
| SB0, SB1 high-level width | $t_{SBH}$ | | | $t_{KCY4}$ | | | ns |
| SB0, SB1 low-level width | $t_{SBL}$ | | | $t_{KCY4}$ | | | ns |
| $\overline{SCK0}$ rise, fall time | $t_{R4}$, $t_{F4}$ | When external device expansion function is used | | | | 160 | ns |
| | | When external device expansion function is not used | When 16-bit timer output function is used | | | 700 | ns |
| | | | When 16-bit timer output function is not used | | | 1000 | ns |

**Note** R and C are the load resistance and load capacitance of the SB0 and SB1 output lines.

### (v) 2-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK0}$ cycle time | $t_{KCY5}$ | R = 1 kΩ, C = 100 pF **Note** | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1600 | | | ns |
| | | | 2.0 V ≤ $V_{DD}$ < 2.7 V | 3200 | | | ns |
| | | | | 4800 | | | ns |
| $\overline{SCK0}$ high-level width | $t_{KH5}$ | | $V_{DD}$ = 2.7 to 5.5 V | $t_{KCY5}$/2 – 160 | | | ns |
| | | | | $t_{KCY5}$/2 – 190 | | | ns |
| $\overline{SCK0}$ low-level width | $t_{KL5}$ | | $V_{DD}$ = 4.5 to 5.5 V | $t_{KCY5}$/2 – 50 | | | ns |
| | | | | $t_{KCY5}$/2 – 100 | | | ns |
| SB0, SB1 setup time (to $\overline{SCK0}$↑) | $t_{SIK5}$ | | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | 300 | | | ns |
| | | | 2.7 V ≤ $V_{DD}$ < 4.5 V | 350 | | | ns |
| | | | 2.0 V ≤ $V_{DD}$ < 2.7 V | 400 | | | ns |
| | | | | 500 | | | ns |
| SB0, SB1 hold time (from $\overline{SCK0}$↑) | $t_{KSI5}$ | | | 600 | | | ns |
| SB0, SB1 output delay time from $\overline{SCK0}$↓ | $t_{KSO5}$ | | | 0 | | 300 | ns |

**Note** R and C are the load resistance and load capacitance of the $\overline{SCK0}$, SB0, and SB1 output lines.

### (vi) 2-wire serial I/O mode ($\overline{SCK0}$... External clock input)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK0}$ cycle time | $t_{KCY6}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 1600 | | | ns |
| | | 2.0 V ≤ $V_{DD}$ < 2.7 V | | 3200 | | | ns |
| | | | | 4800 | | | ns |
| $\overline{SCK0}$ high-level width | $t_{KH6}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 650 | | | ns |
| | | 2.0 V ≤ $V_{DD}$ < 2.7 V | | 1300 | | | ns |
| | | | | 2100 | | | ns |
| $\overline{SCK0}$ low-level width | $t_{KL6}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | 800 | | | ns |
| | | 2.0 V ≤ $V_{DD}$ < 2.7 V | | 1600 | | | ns |
| | | | | 2400 | | | ns |
| SB0, SB1 setup time (to $\overline{SCK0}$↑) | $t_{SIK6}$ | $V_{DD}$ = 2.0 to 5.5 V | | 100 | | | ns |
| | | | | 150 | | | ns |
| SB0, SB1 hold time (from $\overline{SCK0}$↑) | $t_{KSI6}$ | | | $t_{KCY6}$/2 | | | ns |
| SB0, SB1 output delay time from $\overline{SCK0}$↓ | $t_{KSO6}$ | R = 1 kΩ, C = 100 pF **Note** | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | 0 | | 300 | ns |
| | | | 2.0 V ≤ $V_{DD}$ < 4.5 V | 0 | | 500 | ns |
| | | | | 0 | | 800 | ns |
| $\overline{SCK0}$ rise, fall time | $t_{R6}$, $t_{F6}$ | When external device expansion function is used | | | | 160 | ns |
| | | When external device expansion function is not used | When 16-bit timer output function is used | | | 700 | ns |
| | | | When 16-bit timer output function is not used | | | 1000 | ns |

**Note** R and C are the load resistance and load capacitance of the SB0 and SB1 output lines.

**(b) Serial Interface Channel 1**

**(i) 3-wire serial I/O mode ($\overline{SCK1}$... Internal clock output)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $\overline{SCK1}$ cycle time | $t_{KCY7}$ | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | 800 | | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.5 V | 1600 | | | ns |
| | | 2.0 V ≤ $V_{DD}$ < 2.7 V | 3200 | | | ns |
| | | | 4800 | | | ns |
| $\overline{SCK1}$ high-/low-level width | $t_{KH7}$, $t_{KL7}$ | $V_{DD}$ = 4.5 to 5.5 V | $t_{KCY7}/2 - 50$ | | | ns |
| | | | $t_{KCY7}/2 - 100$ | | | ns |
| SI1 setup time (to $\overline{SCK1}$↑) | $t_{SIK7}$ | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | 100 | | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.5 V | 150 | | | ns |
| | | 2.0 V ≤ $V_{DD}$ < 2.7 V | 300 | | | ns |
| | | | 400 | | | ns |
| SI1 hold time (from $\overline{SCK1}$↑) | $t_{KSI7}$ | | 400 | | | ns |
| SO1 output delay time from $\overline{SCK1}$↓ | $t_{KSO7}$ | C = 100 pF **Note** | | | 300 | ns |

**Note** C is the load capacitance of $\overline{SCK1}$ and SO1 output lines.

**(ii) 3-wire serial I/O mode ($\overline{SCK1}$... External clock input)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK1}$ cycle time | $t_{KCY8}$ | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | | 800 | | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.5 V | | 1600 | | | ns |
| | | 2.0 V ≤ $V_{DD}$ < 2.7 V | | 3200 | | | ns |
| | | | | 4800 | | | ns |
| $\overline{SCK1}$ high-/low-level width | $t_{KH8}$, $t_{KL8}$ | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | | 400 | | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.5 V | | 800 | | | ns |
| | | 2.0 V ≤ $V_{DD}$ < 2.7 V | | 1600 | | | ns |
| | | | | 2400 | | | ns |
| SI1 setup time (to $\overline{SCK1}$↑) | $t_{SIK8}$ | $V_{DD}$ = 2.0 to 5.5 V | | 100 | | | ns |
| | | | | 150 | | | ns |
| SI1 hold time (from $\overline{SCK1}$↑) | $t_{KSI8}$ | | | 400 | | | ns |
| SO1 output delay time from $\overline{SCK1}$↓ | $t_{KSO8}$ | C = 100 pF **Note** | $V_{DD}$ = 2.0 to 5.5 V | | | 300 | ns |
| | | | | | | 500 | ns |
| $\overline{SCK1}$ rise, fall time | $t_{R8}$, $t_{F8}$ | When external device expansion function is used | | | | 160 | ns |
| | | When external device expansion function is not used | When 16-bit timer output function is used | | | 700 | ns |
| | | | When 16-bit timer output function is not used | | | 1000 | ns |

**Note** C is the load capacitance of SO1 output line.

**(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$... Internal clock output)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $\overline{SCK1}$ cycle time | $t_{KCY9}$ | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | 800 | | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.5 V | 1600 | | | ns |
| | | 2.0 V ≤ $V_{DD}$ < 2.7 V | 3200 | | | ns |
| | | | 4800 | | | ns |
| $\overline{SCK1}$ high-/low-level width | $t_{KH9}$, $t_{KL9}$ | $V_{DD}$ = 4.5 to 5.5 V | $t_{KCY9}/2 - 50$ | | | ns |
| | | | $t_{KCY9}/2 - 100$ | | | ns |
| SI1 setup time (to $\overline{SCK1}$↑) | $t_{SIK9}$ | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | 100 | | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.5 V | 150 | | | ns |
| | | 2.0 V ≤ $V_{DD}$ < 2.7 V | 300 | | | ns |
| | | | 400 | | | ns |
| SI1 hold time (from $\overline{SCK1}$↑) | $t_{KSI9}$ | | 400 | | | ns |
| SO1 output delay time from $\overline{SCK1}$↓ | $t_{KSO9}$ | C = 100 pF **Note** | | | 300 | ns |
| STB↑ from $\overline{SCK1}$↑ | $t_{SBD}$ | | $t_{KCY9}/2 - 100$ | | $t_{KCY9}/2 + 100$ | ns |
| Strobe signal high-level width | $t_{SBW}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | $t_{KCY9} - 30$ | | $t_{KCY9} + 30$ | ns |
| | | 2.0 V ≤ $V_{DD}$ < 2.7 V | $t_{KCY9} - 60$ | | $t_{KCY9} + 60$ | ns |
| | | | $t_{KCY9} - 90$ | | $t_{KCY9} + 90$ | ns |
| Busy signal setup time (to busy signal detection timing) | $t_{BYS}$ | | 100 | | | ns |
| Busy signal hold time (from busy signal detection timing) | $t_{BYH}$ | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | 100 | | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.5 V | 150 | | | ns |
| | | 2.0 V ≤ $V_{DD}$ < 2.7 V | 200 | | | ns |
| | | | 300 | | | ns |
| $\overline{SCK1}$↓ from busy inactive | $t_{SPS}$ | | | | $2t_{KCY9}$ | ns |

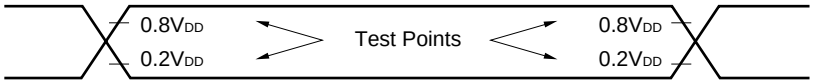
**Note** C is the load capacitance of $\overline{SCK1}$ and SO1 output lines.

**(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$... External clock input)**

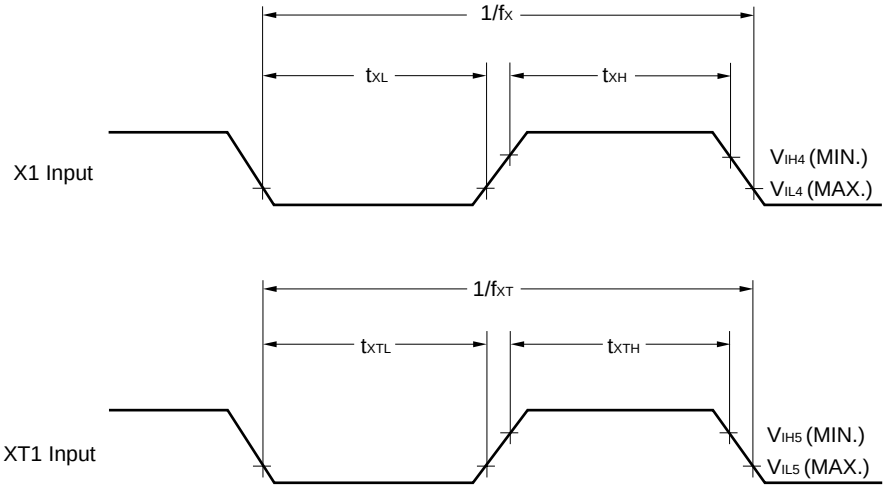
| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK1}$ cycle time | $t_{KCY10}$ | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | | 800 | | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.5 V | | 1600 | | | ns |
| | | 2.0 V ≤ $V_{DD}$ < 2.7 V | | 3200 | | | ns |
| | | | | 4800 | | | ns |
| $\overline{SCK1}$ high-/low-level width | $t_{KH10}$, $t_{KL10}$ | 4.5 V ≤ $V_{DD}$ ≤ 5.5 V | | 400 | | | ns |
| | | 2.7 V ≤ $V_{DD}$ < 4.5 V | | 800 | | | ns |
| | | 2.0 V ≤ $V_{DD}$ < 2.7 V | | 1600 | | | ns |
| | | | | 2400 | | | ns |
| SI1 setup time (to $\overline{SCK1}$↑) | $t_{SIK10}$ | $V_{DD}$ = 2.0 to 5.5 V | | 100 | | | ns |
| | | | | 150 | | | ns |
| SI1 hold time (from $\overline{SCK1}$↑) | $t_{KSI10}$ | | | 400 | | | ns |
| SO1 output delay time from $\overline{SCK1}$↓ | $t_{KSO10}$ | C = 100 pF **Note** | $V_{DD}$ = 2.0 to 5.5 V | | | 300 | ns |
| | | | | | | 500 | ns |
| $\overline{SCK1}$ rise, fall time | $t_{R10}$, $t_{F10}$ | When external device expansion function is used | | | | 160 | ns |
| | | When external device expansion function is not used | | | | 1000 | ns |

**Note** C is the load capacitance of the SO1 output line.

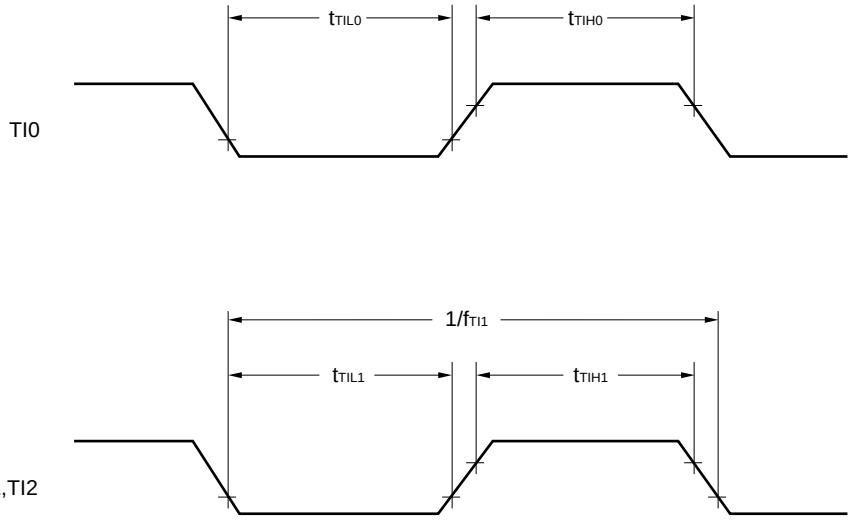
### AC Timing Test Point (Excluding X1, XT1 Input)




### Clock Timing

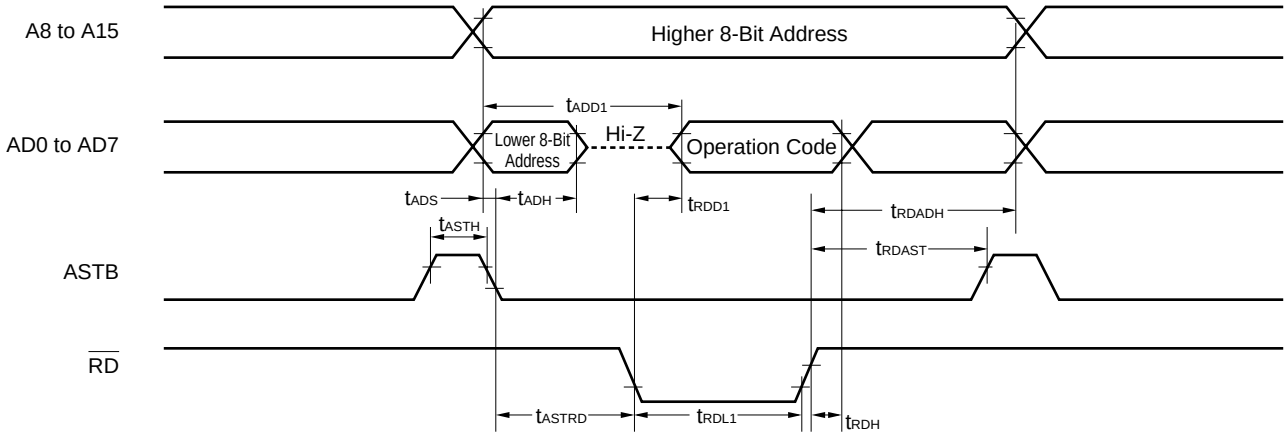



### TI Timing

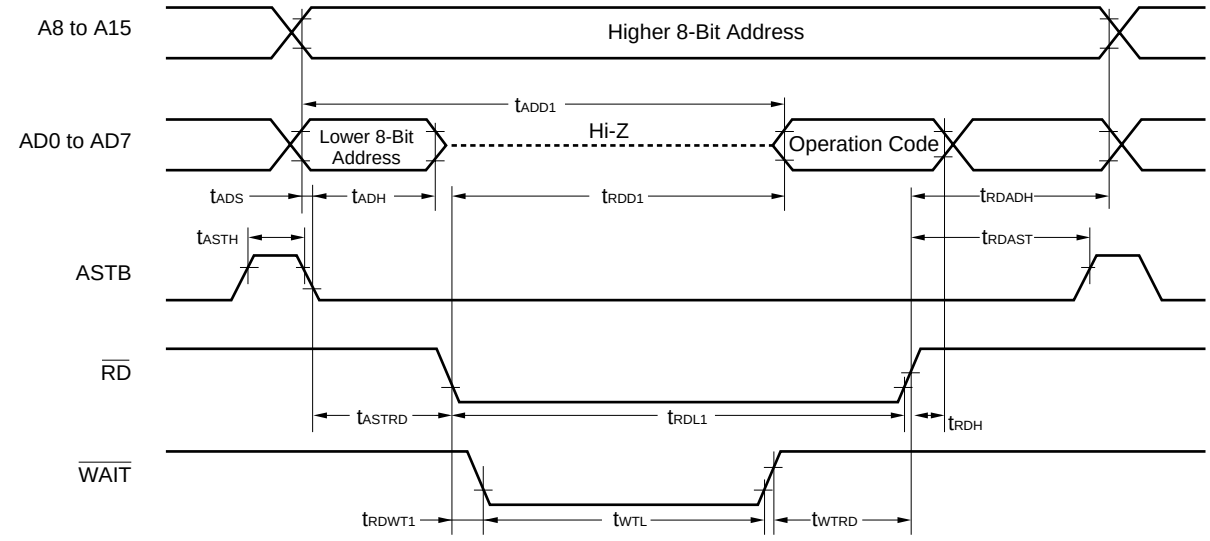


**Read/Write Operation**

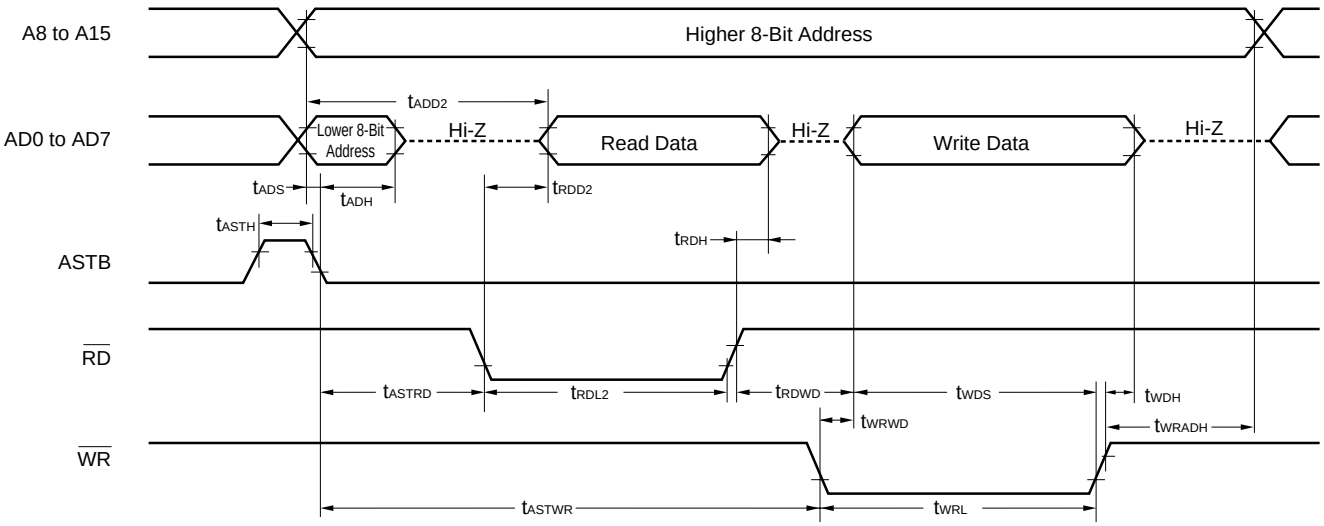
**External fetch (No wait):**



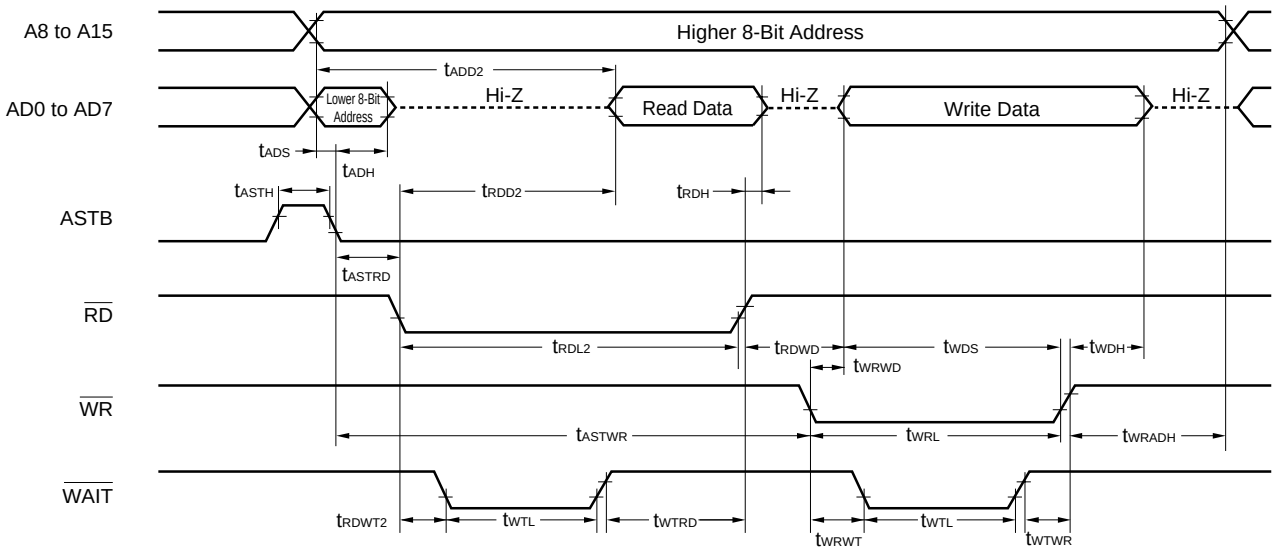

**External fetch (Wait insertion):**



**External data access (No wait):**

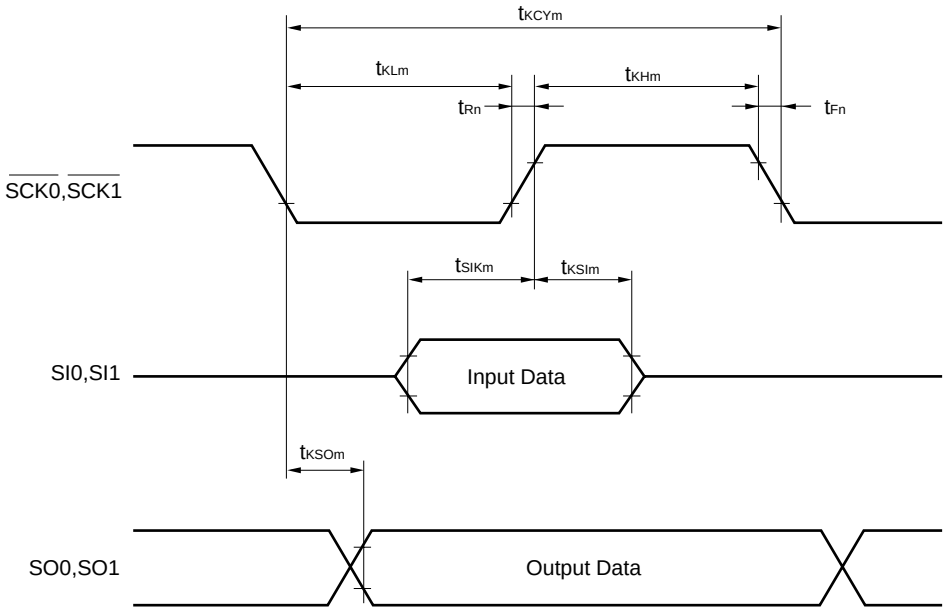



**External data access (Wait insertion):**



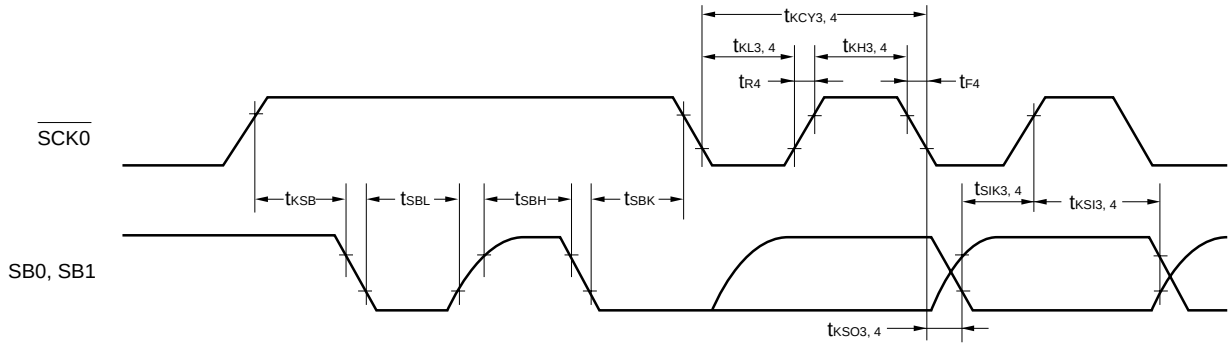
**Serial Transfer Timing**

**3-wire serial I/O mode:**

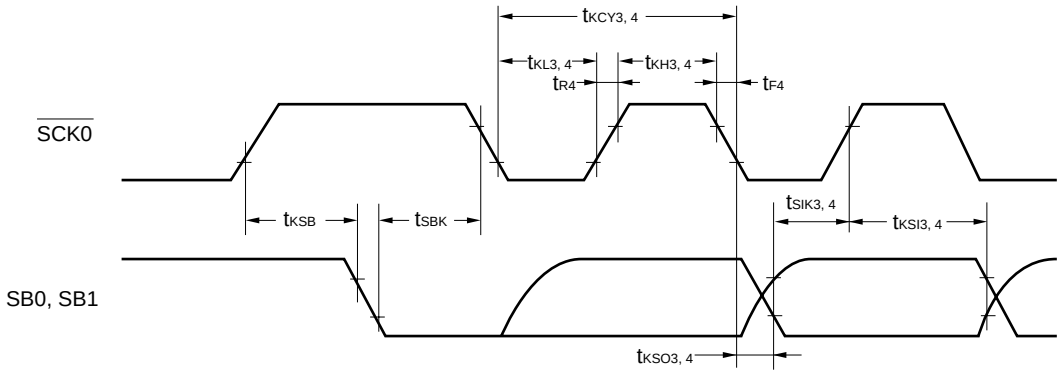



m = 1, 2, 7, 8
n = 2, 8

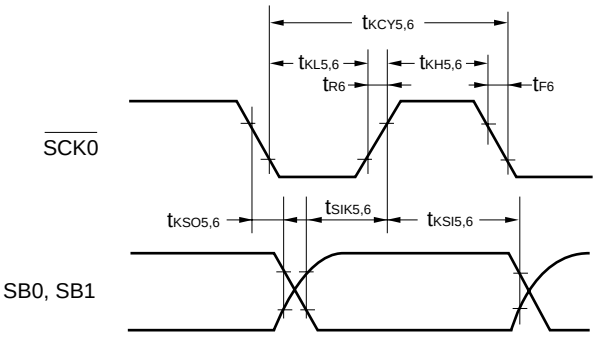
**SBI mode (Bus release signal transfer):**



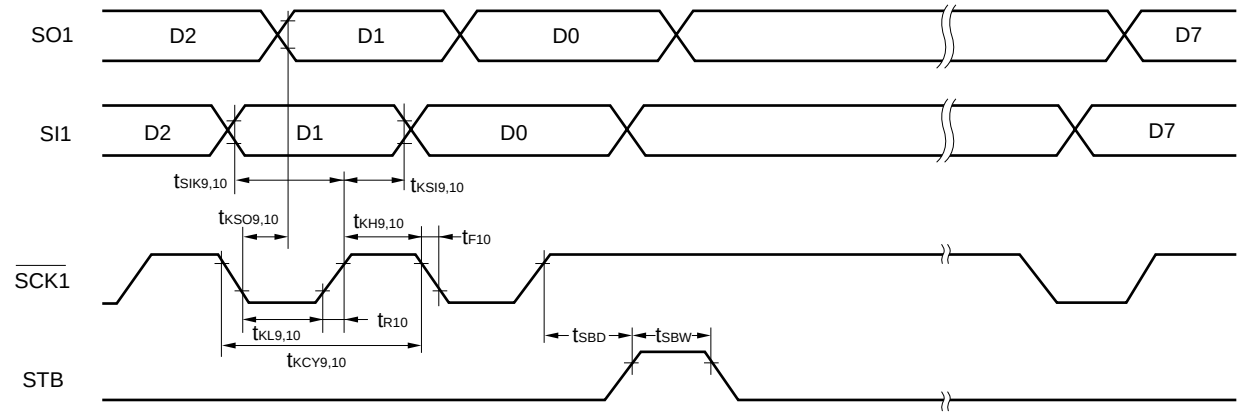

**SBI Mode (command signal transfer):**



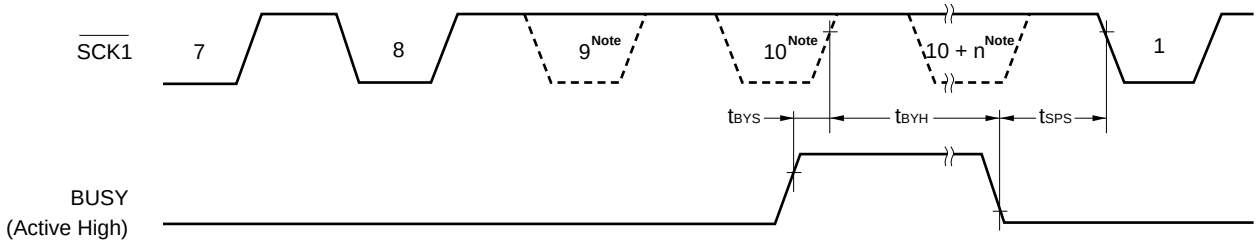
**2-wire serial I/O mode:**




**3-wire serial I/O mode with automatic transmit/receive function:**




**3-wire serial I/O mode with automatic transmit/receive function (busy processing):**




**Note** The signal is not actually driven low here; it is shown as such to indicate the timing.

**A/D Converter Characteristics ($T_A$ = –40 to +85°C, $AV_{DD}$ = $V_{DD}$ = 2.2 to 5.5 V, $AV_{SS}$ = $V_{SS}$ = 0 V)**

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Resolution | | | 8 | 8 | 8 | bit |
| ★ Overall error **Note** | | 2.7 V ≤ $AV_{REF}$ ≤ $AV_{DD}$ | | | 0.6 | % |
| ★ | | 2.2 V ≤ $AV_{REF}$ < 2.7 V | | | 1.4 | % |
| ★ Conversion time | $t_{CONV}$ | 2.7 V ≤ $AV_{REF}$ ≤ $AV_{DD}$ | 19.1 | | 200 | μs |
| ★ | | 2.2 V ≤ $AV_{REF}$ < 2.7 V | 38.2 | | 200 | μs |
| Sampling time | $t_{SAMP}$ | | 24/$f_X$ | | | μs |
| Analog input voltage | $V_{IAN}$ | | $AV_{SS}$ | | $AV_{REF}$ | V |
| ★ Reference voltage | $AV_{REF}$ | | 2.2 | | $AV_{DD}$ | V |
| $AV_{REF}$ resistance | $R_{AIREF}$ | | 4 | 14 | | kΩ |

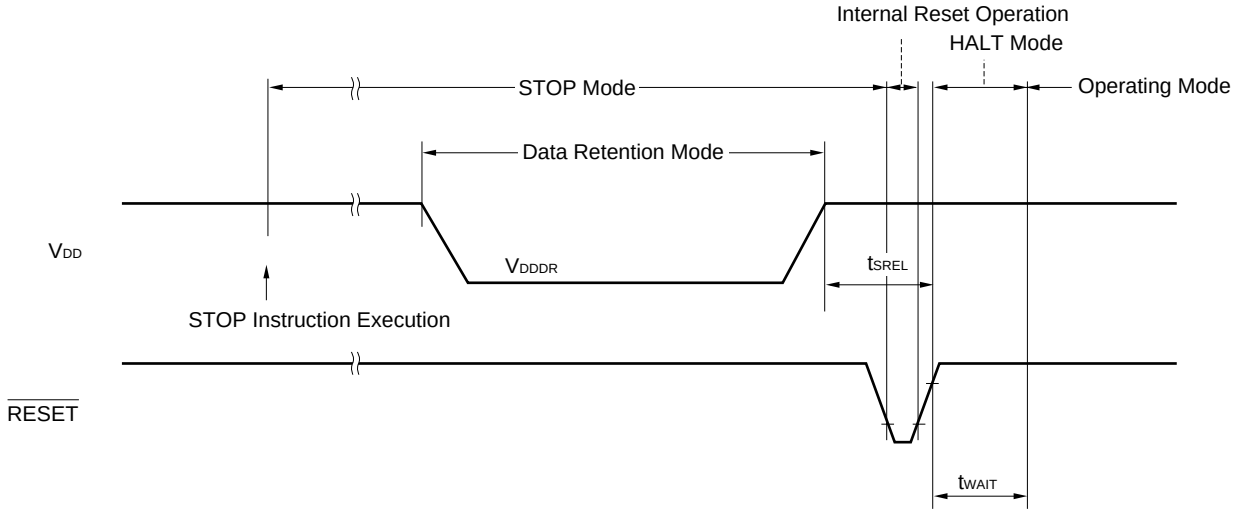
**Note** Overall error excluding quantization error (±1/2 LSB). It is indicated as a ratio to the full-scale value.

**Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics ($T_A$ = –40 to +85°C)**

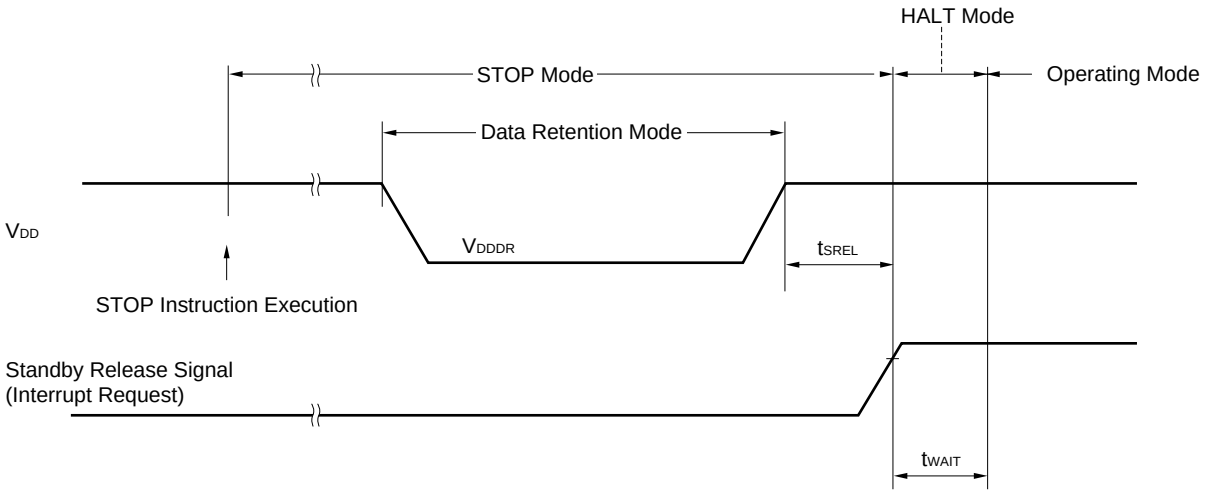
| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.8 | | 5.5 | V |
| Data retention supply current | $I_{DDDR}$ | $V_{DDDR}$ = 1.8 V<br>Subsystem clock stops and feed-back resistor disconnected | | 0.1 | 10 | μA |
| Release signal set time | $t_{SREL}$ | | 0 | | | μs |
| Oscillation stabilization wait time | $t_{WAIT}$ | Release by $\overline{\text{RESET}}$ | | $2^{18}/f_X$ | | ms |
| | | Release by interrupt | | **Note** | | ms |

**Note** In combination with bit 0 to bit 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS), selection of $2^{13}/f_X$ and $2^{15}/f_X$ to $2^{18}/f_X$ is possible.

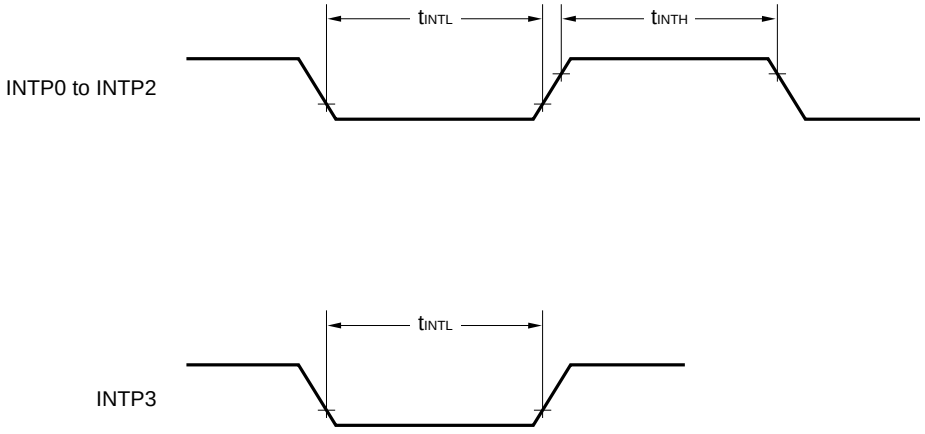
**Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)**



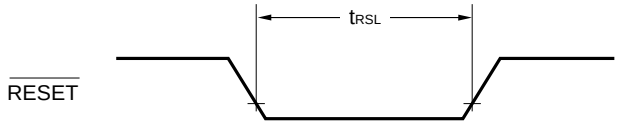
**Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)**




**Interrupt Input Timing**




**$\overline{\text{RESET}}$ Input Timing**



## PROM PROGRAMMING CHARACTERISTICS

### DC Characteristics

**(1) PROM Write Mode ($T_A$ = 25 ±5°C, $V_{DD}$ = 6.5 ±0.25 V, $V_{PP}$ = 12.5 ±0.3 V)**

| Parameter | Symbol | Symbol[Note] | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH}$ | $V_{IH}$ | | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL}$ | $V_{IL}$ | | 0 | | 0.3$V_{DD}$ | V |
| Output voltage, high | $V_{OH}$ | $V_{OH}$ | $I_{OH}$ = –1 mA | $V_{DD}$ – 1.0 | | | V |
| Output voltage, low | $V_{OL}$ | $V_{OL}$ | $I_{OL}$ = 1.6 mA | | | 0.4 | V |
| Input leakage current | $I_{LI}$ | $I_{LI}$ | 0 ≤ $V_{IN}$ ≤ $V_{DD}$ | –10 | | +10 | μA |
| $V_{PP}$ supply voltage | $V_{PP}$ | $V_{PP}$ | | 12.2 | 12.5 | 12.8 | V |
| $V_{DD}$ supply voltage | $V_{DD}$ | $V_{CC}$ | | 6.25 | 6.5 | 6.75 | V |
| $V_{PP}$ supply current | $I_{PP}$ | $I_{PP}$ | $\overline{PGM}$ = $V_{IL}$ | | | 50 | mA |
| $V_{DD}$ supply current | $I_{DD}$ | $I_{CC}$ | | | | 50 | mA |

**Note** Corresponding μPD27C1001A symbol

**(2) PROM Read Mode ($T_A$ = 25 ±5°C, $V_{DD}$ = 5.0 ±0.5 V, $V_{PP}$ = $V_{DD}$ ±0.6 V)**

| Parameter | Symbol | Symbol[Note] | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH}$ | $V_{IH}$ | | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL}$ | $V_{IL}$ | | 0 | | 0.3$V_{DD}$ | V |
| Output voltage, high | $V_{OH1}$ | $V_{OH1}$ | $I_{OH}$ = –1 mA | $V_{DD}$ – 1.0 | | | V |
| | $V_{OH2}$ | $V_{OH2}$ | $I_{OH}$ = –100 μA | $V_{DD}$ – 0.5 | | | V |
| Output voltage, low | $V_{OL}$ | $V_{OL}$ | $I_{OL}$ = 1.6 mA | | | 0.4 | V |
| Input leakage current | $I_{LI}$ | $I_{LI}$ | 0 ≤ $V_{IN}$ ≤ $V_{DD}$ | –10 | | +10 | μA |
| Output leakage current | $I_{LO}$ | $I_{LO}$ | 0 ≤ $V_{OUT}$ ≤ $V_{DD}$, $\overline{OE}$ = $V_{IH}$ | –10 | | +10 | μA |
| $V_{PP}$ supply voltage | $V_{PP}$ | $V_{PP}$ | | $V_{DD}$ – 0.6 | $V_{DD}$ | $V_{DD}$ + 0.6 | V |
| $V_{DD}$ supply voltage | $V_{DD}$ | $V_{CC}$ | | 4.5 | 5.0 | 5.5 | V |
| $V_{PP}$ supply current | $I_{PP}$ | $I_{PP}$ | $V_{PP}$ = $V_{DD}$ | | | 100 | μA |
| $V_{DD}$ supply current | $I_{DD}$ | $I_{CCA1}$ | $\overline{CE}$ = $V_{IL}$, $V_{IN}$ = $V_{IH}$ | | | 50 | mA |

**Note** Corresponding μPD27C1001A symbol

## AC Characteristics

### (1) PROM Write Mode

#### (a) Page program mode ($T_A$ = 25 ±5°C, $V_{DD}$ = 6.5 ±0.25 V, $V_{PP}$ = 12.5 ±0.3 V)

| Parameter | Symbol | Symbol[Note] | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Address setup time (to $\overline{OE}\downarrow$) | $t_{AS}$ | $t_{AS}$ | | 2 | | | μs |
| $\overline{OE}$ setup time | $t_{OES}$ | $t_{OES}$ | | 2 | | | μs |
| $\overline{CE}$ setup time (to $\overline{OE}\downarrow$) | $t_{CES}$ | $t_{CES}$ | | 2 | | | μs |
| Input data setup time (to $\overline{OE}\downarrow$) | $t_{DS}$ | $t_{DS}$ | | 2 | | | μs |
| Address hold time (from $\overline{OE}\uparrow$) | $t_{AH}$ | $t_{AH}$ | | 2 | | | μs |
| | $t_{AHL}$ | $t_{AHL}$ | | 2 | | | μs |
| | $t_{AHV}$ | $t_{AHV}$ | | 0 | | | μs |
| Input data hold time (from $\overline{OE}\uparrow$) | $t_{DH}$ | $t_{DH}$ | | 2 | | | μs |
| Data output float delay time from $\overline{OE}\uparrow$ | $t_{DF}$ | $t_{DF}$ | | 0 | | 250 | ns |
| $V_{PP}$ setup time (to $\overline{OE}\downarrow$) | $t_{VPS}$ | $t_{VPS}$ | | 1.0 | | | ms |
| $V_{DD}$ setup time (to $\overline{OE}\downarrow$) | $t_{VDS}$ | $t_{VCS}$ | | 1.0 | | | ms |
| Program pulse width | $t_{PW}$ | $t_{PW}$ | | 0.095 | 0.1 | 0.105 | ms |
| Valid data delay time from $\overline{OE}\downarrow$ | $t_{OE}$ | $t_{OE}$ | | | | 1 | μs |
| $\overline{OE}$ pulse width during data latching | $t_{LW}$ | $t_{LW}$ | | 1 | | | μs |
| $\overline{PGM}$ setup time | $t_{PGMS}$ | $t_{PGMS}$ | | 2 | | | μs |
| $\overline{CE}$ hold time | $t_{CEH}$ | $t_{CEH}$ | | 2 | | | μs |
| $\overline{OE}$ hold time | $t_{OEH}$ | $t_{OEH}$ | | 2 | | | μs |

**Note** Corresponding μPD27C1001A symbol

#### (b) Byte program mode ($T_A$ = 25 ±5°C, $V_{DD}$ = 6.5 ±0.25 V, $V_{PP}$ = 12.5 ±0.3 V)

| Parameter | Symbol | Symbol[Note] | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Address setup time (to $\overline{PGM}\downarrow$) | $t_{AS}$ | $t_{AS}$ | | 2 | | | μs |
| $\overline{OE}$ setup time | $t_{OES}$ | $t_{OES}$ | | 2 | | | μs |
| $\overline{CE}$ setup time (to $\overline{PGM}\downarrow$) | $t_{CES}$ | $t_{CES}$ | | 2 | | | μs |
| Input data setup time (to $\overline{PGM}\downarrow$) | $t_{DS}$ | $t_{DS}$ | | 2 | | | μs |
| Address hold time (from $\overline{OE}\uparrow$) | $t_{AH}$ | $t_{AH}$ | | 2 | | | μs |
| Input data hold time (from $\overline{PGM}\uparrow$) | $t_{DH}$ | $t_{DH}$ | | 2 | | | μs |
| Data output float delay time from $\overline{OE}\uparrow$ | $t_{DF}$ | $t_{DF}$ | | 0 | | 250 | ns |
| $V_{PP}$ setup time (to $\overline{PGM}\downarrow$) | $t_{VPS}$ | $t_{VPS}$ | | 1.0 | | | ms |
| $V_{DD}$ setup time (to $\overline{PGM}\downarrow$) | $t_{VDS}$ | $t_{VCS}$ | | 1.0 | | | ms |
| Program pulse width | $t_{PW}$ | $t_{PW}$ | | 0.095 | 0.1 | 0.105 | ms |
| Valid data delay time from $\overline{OE}\downarrow$ | $t_{OE}$ | $t_{OE}$ | | | | 1 | μs |
| $\overline{OE}$ hold time | $t_{OEH}$ | — | | 2 | | | μs |

**Note** Corresponding μPD27C1001A symbol

### (2) PROM Read Mode ($T_A$ = 25 ±5°C, $V_{DD}$ = 5.0 ±0.5 V, $V_{PP}$ = $V_{DD}$ ±0.6 V)

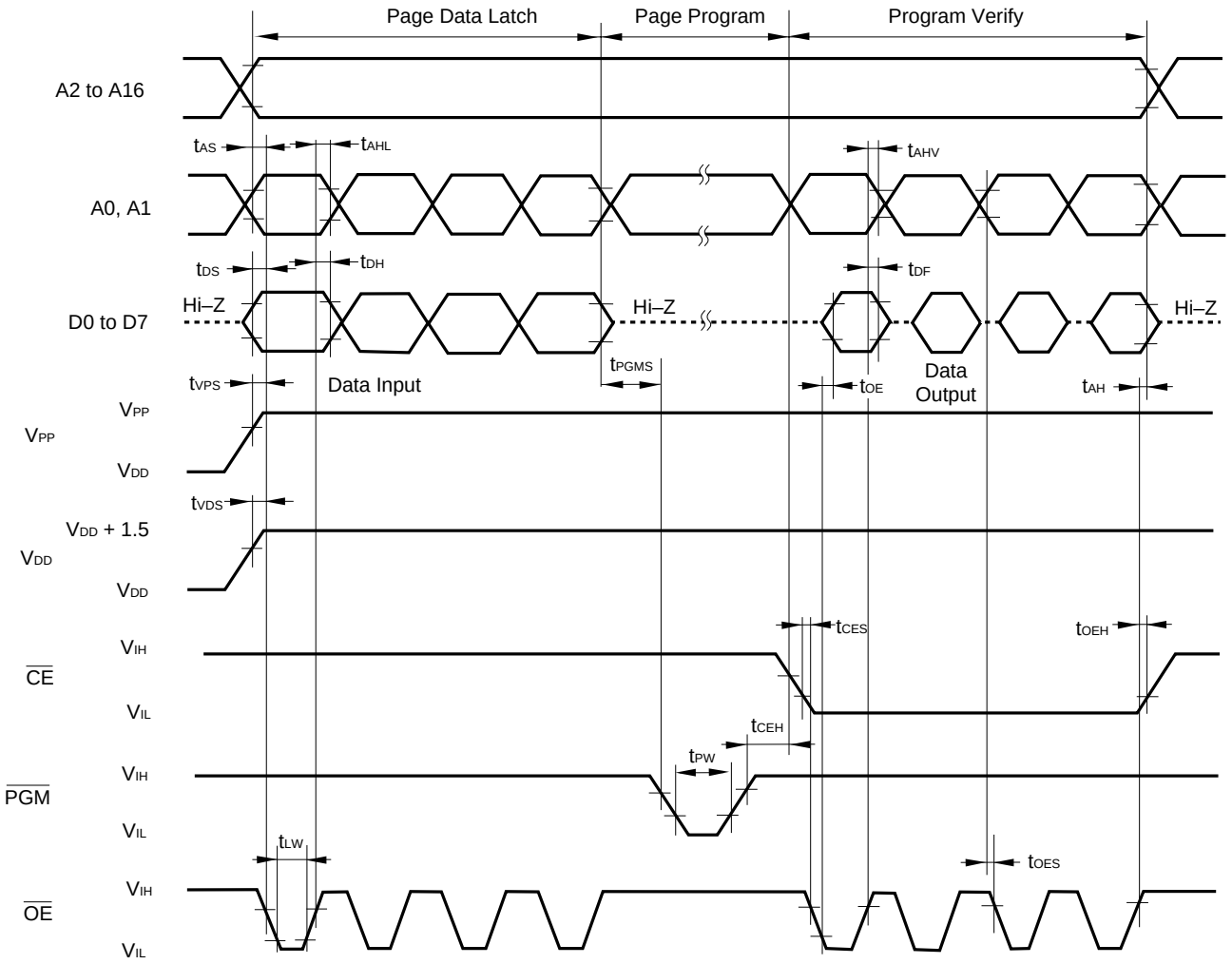
| Parameter | Symbol | Symbol[Note] | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Data output time from address | $t_{ACC}$ | $t_{ACC}$ | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$ | | | 800 | ns |
| Data output delay time from $\overline{CE}$↓ | $t_{CE}$ | $t_{CE}$ | $\overline{OE}$ = $V_{IL}$ | | | 800 | ns |
| Data output delay time from $\overline{OE}$↓ | $t_{OE}$ | $t_{OE}$ | $\overline{CE}$ = $V_{IL}$ | | | 200 | ns |
| Data output float delay time from $\overline{OE}$↑ | $t_{DF}$ | $t_{DF}$ | $\overline{CE}$ = $V_{IL}$ | 0 | | 60 | ns |
| Data hold time from address | $t_{OH}$ | $t_{OH}$ | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$ | 0 | | | ns |

**Note** Corresponding μPD27C1001A symbol

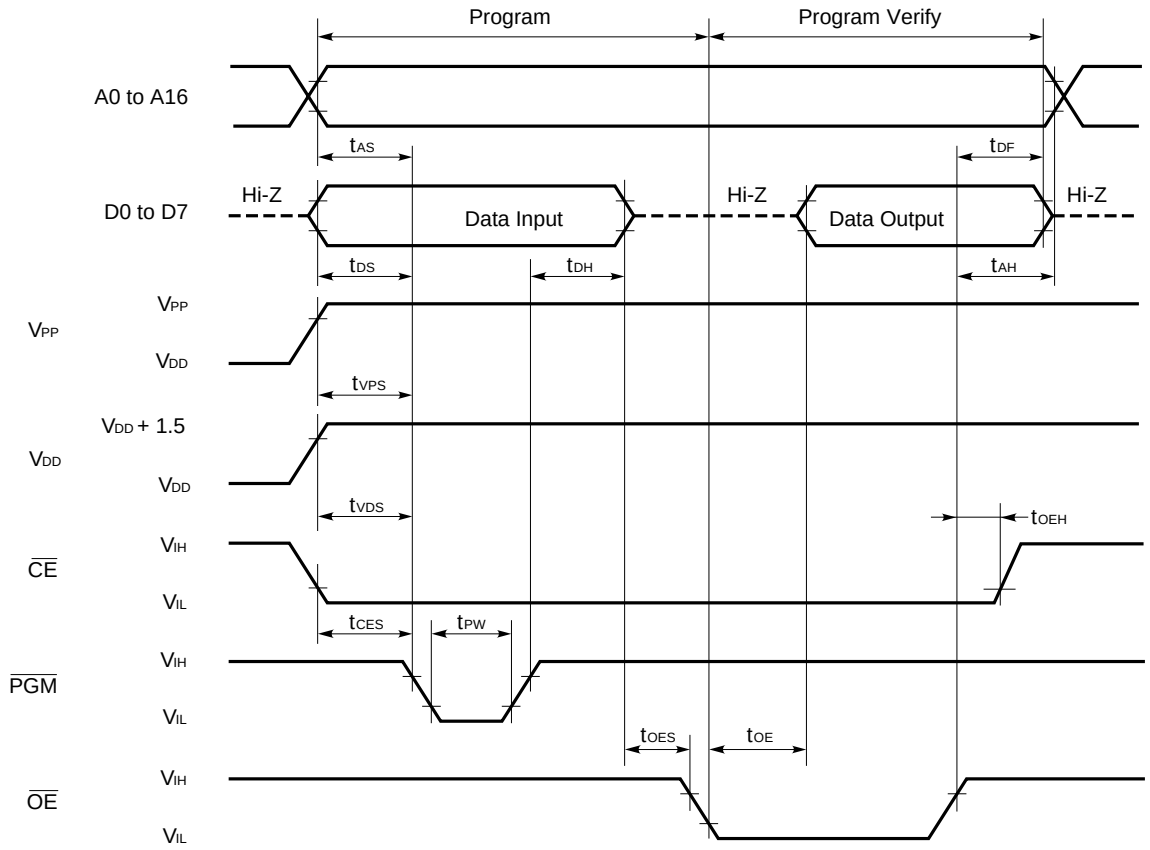
### (3) PROM Programming Mode Setting ($T_A$ = 25°C, $V_{SS}$ = 0 V)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| PROM programming mode setup time | $t_{SMA}$ | | 10 | | | μs |

### PROM Write Mode Timing (Page program mode)



**PROM Write Mode Timing (Byte program mode)**

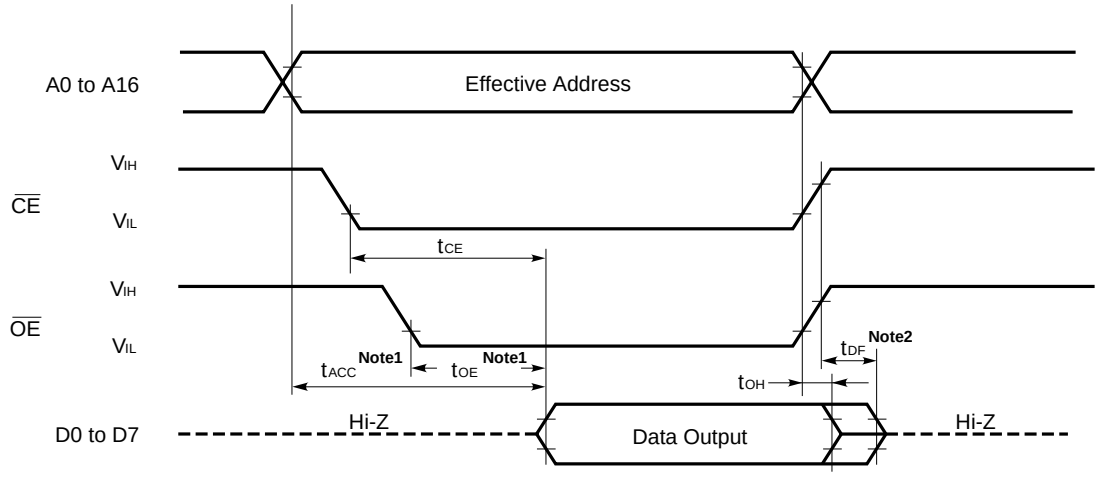



**Cautions 1. $V_{DD}$ must be applied before $V_{PP}$ and cut off after $V_{PP}$.**

**2. $V_{PP}$ must not exceed +13.5 V including overshoot.**

**3. Removing and reinserting while +12.5 V is applied to $V_{PP}$ may adversely affect reliability.**

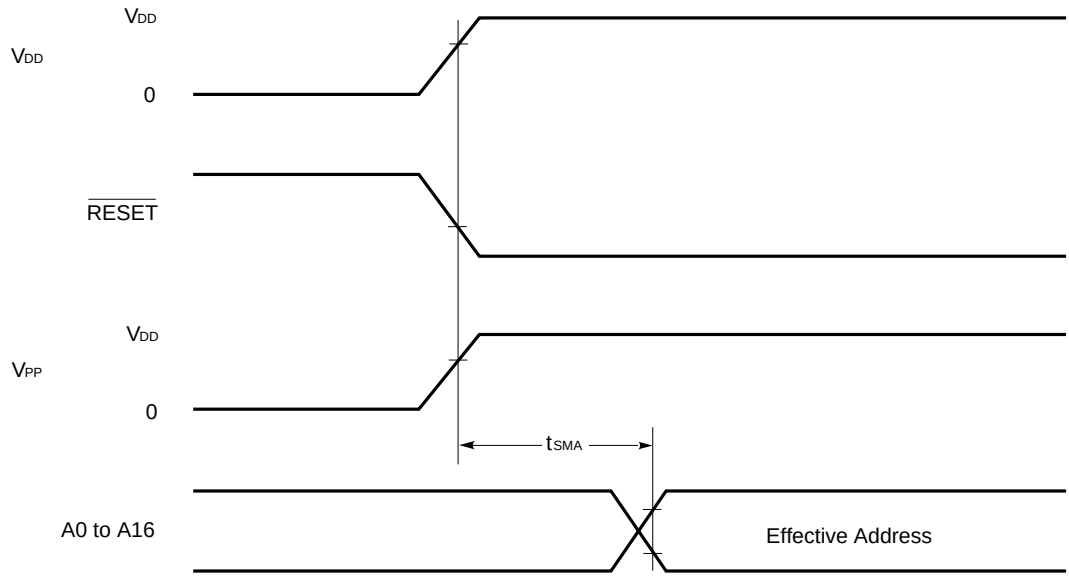
**PROM Read Mode Timing**




**Notes 1.** When reading within the $t_{ACC}$ range, the $\overline{OE}$ input delay time from the $\overline{CE}$ fall time must be maximum of $t_{ACC} - t_{OE}$.

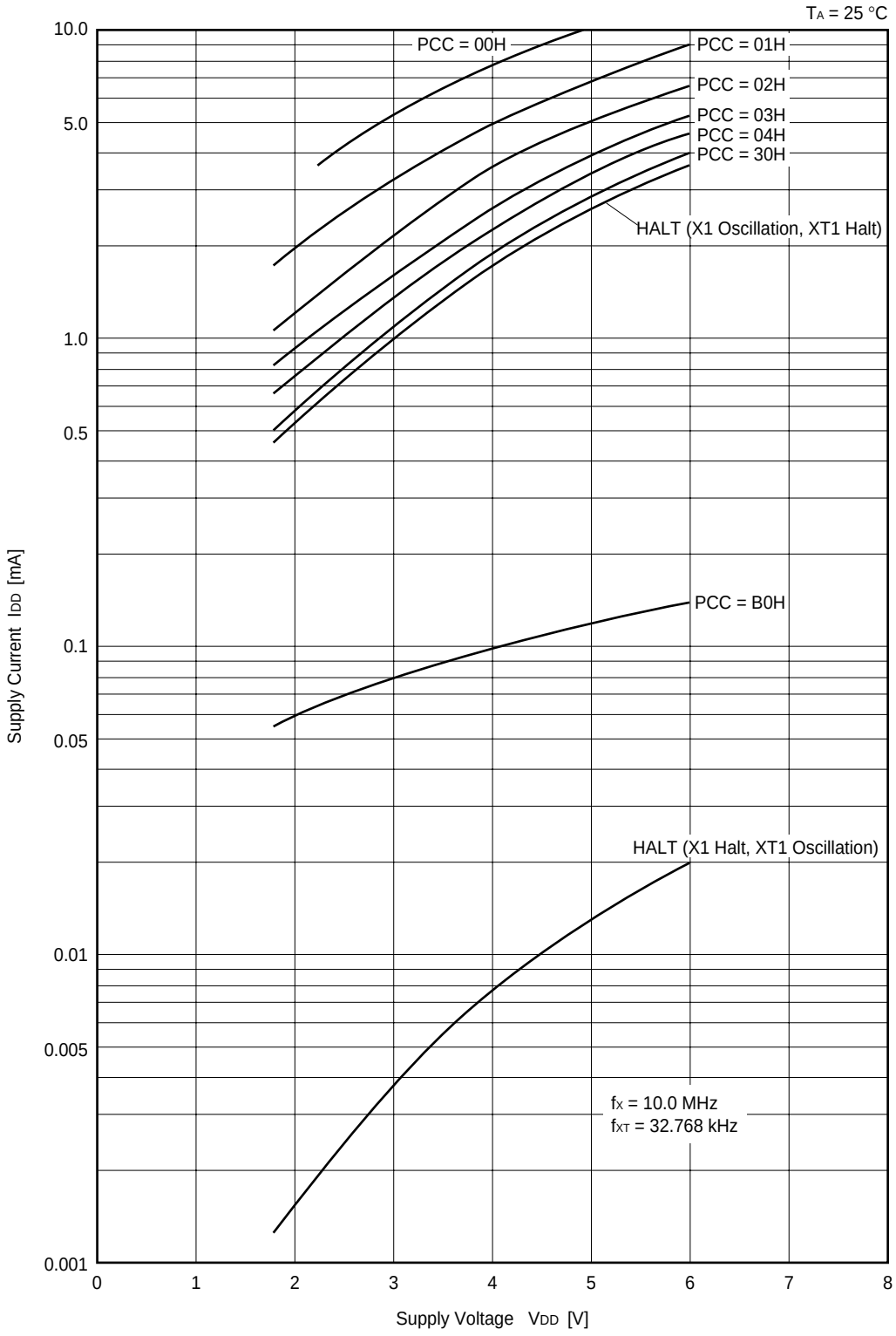
**2.** $t_{DF}$ is the time from the point at which either $\overline{OE}$ or $\overline{CE}$ (whichever is first) reaches VIH.

**PROM Programming Mode Setting Timing**



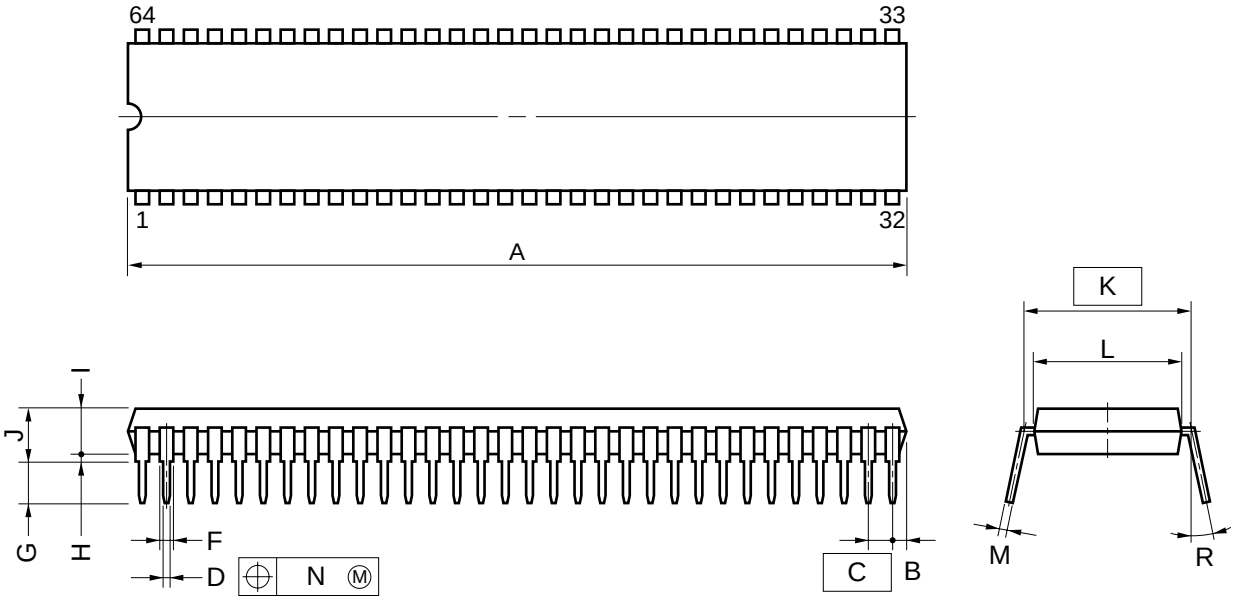
## ★ 8. CHARACTERISTIC CURVE (REFERENCE VALUE)

**$I_{DD}$ vs. $V_{DD}$ (Main System Clock: 10.0 MHz)**



## 9. PACKAGE DRAWINGS

## 64 PIN PLASTIC SHRINK DIP (750 mil)




**NOTE**

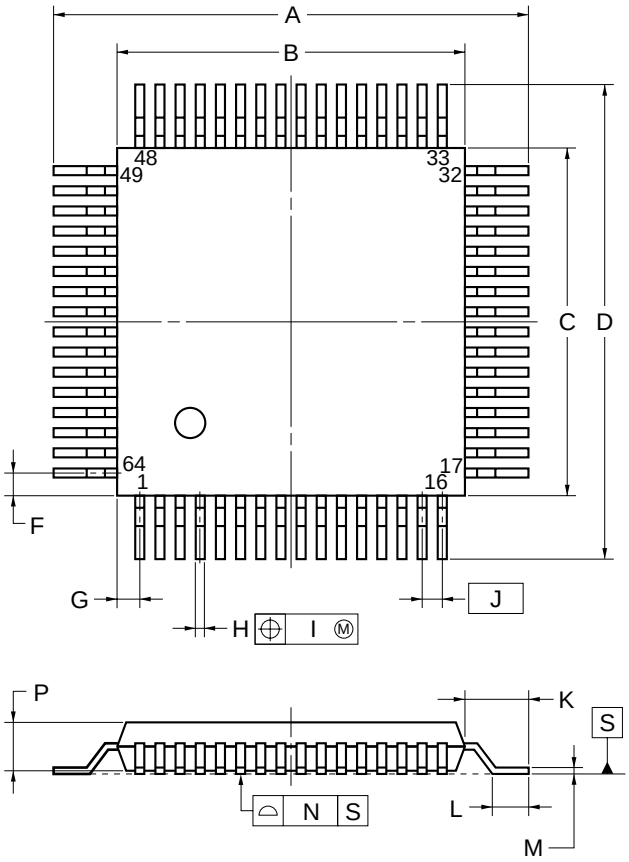
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
2) Item "K" to center of leads when formed parallel.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 58.68 MAX. | 2.311 MAX. |
| B | 1.78 MAX. | 0.070 MAX. |
| C | 1.778 (T.P.) | 0.070 (T.P.) |
| D | $0.50\pm0.10$ | $0.020^{+0.004}_{-0.005}$ |
| F | 0.9 MIN. | 0.035 MIN. |
| G | $3.2\pm0.3$ | $0.126\pm0.012$ |
| H | 0.51 MIN. | 0.020 MIN. |
| I | 4.31 MAX. | 0.170 MAX. |
| J | 5.08 MAX. | 0.200 MAX. |
| K | 19.05 (T.P.) | 0.750 (T.P.) |
| L | 17.0 | 0.669 |
| M | $0.25^{+0.10}_{-0.05}$ | $0.010^{+0.004}_{-0.003}$ |
| N | 0.17 | 0.007 |
| R | 0~15° | 0~15° |

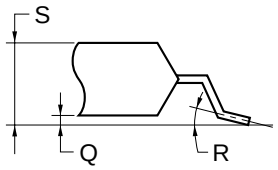
**P64C-70-750A,C-1**

**Remark** The dimensions and materials of ES versions are the same as those of mass-produced versions.

## ★ 64 PIN PLASTIC QFP (14 × 14)




detail of lead end




**NOTE**

1. Controlling dimension — millimeter.

2. Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 17.6±0.4 | 0.693±0.016 |
| B | 14.0±0.2 | $0.551^{+0.009}_{-0.008}$ |
| C | 14.0±0.2 | $0.551^{+0.009}_{-0.008}$ |
| D | 17.6±0.4 | 0.693±0.016 |
| F | 1.0 | 0.039 |
| G | 1.0 | 0.039 |
| H | $0.37^{+0.08}_{-0.07}$ | $0.015^{+0.003}_{-0.004}$ |
| I | 0.15 | 0.006 |
| J | 0.8 (T.P.) | 0.031 (T.P.) |
| K | 1.8±0.2 | 0.071±0.008 |
| L | 0.8±0.2 | $0.031^{+0.009}_{-0.008}$ |
| M | $0.17^{+0.08}_{-0.07}$ | $0.007^{+0.003}_{-0.004}$ |
| N | 0.10 | 0.004 |
| P | 2.55±0.1 | 0.100±0.004 |
| Q | 0.1±0.1 | 0.004±0.004 |
| R | 5°±5° | 5°±5° |
| S | 2.85 MAX. | 0.113 MAX. |

**P64GC-80-AB8-4**

**Remark** The dimensions and materials of ES versions are the same as those of mass-produced versions.

## 10. RECOMMENDED SOLDERING CONDITIONS

The μPD78P018F(A) should be soldered and mounted under the following recommended conditions.

For the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

**Table 10-1. Surface Mounting Type Soldering Conditions**

**μPD78P018FGC(A)-AB8: 64-pin Plastic QFP (14 × 14 mm)**

| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
|---|---|---|
| Infrared rays reflow | Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher), Count: Three times or less | IR35-00-3 |
| VPS | Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher), Count: Three times or less | VP15-00-3 |
| Wave soldering | Solder bath temperature: 260°C, Time: 10 sec. Max., Count: Once, Preheating temperature: 120°C Max. (package surface temperature) | WS60-00-1 |
| Partial heating | Pin temperature: 300°C or below, Time: 3 sec. Max. (per pin row) | — |

**Caution Do not use different soldering methods together (except for partial heating).**

**Table 10-2. Insertion Type Soldering Conditions**

**μPD78P018FCW(A): 64-pin Plastic Shrink DIP (750 mil)**

| Soldering Method | Soldering Conditions |
|---|---|
| Wave soldering (pin only) | Solder bath temperature: 260°C or below, Time: 10 sec. Max. |
| Partial heating | Pin temperature: 300°C or below, Time: 3 sec. Max. (per pin) |

**Caution Apply wave soldering only to the pins and be careful not to bring solder into direct contact with the package.**

## ★ APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78P018F(A).
Also refer to **(5) Cautions on using development tools**.

### (1) Language Processing Software

| | |
|---|---|
| RA78K/0 | 78K/0 Series common assembler package |
| CC78K/0 | 78K/0 Series common C compiler package |
| DF78014 | Device file common to μPD78018F Subseries |
| CC78K/0-L | 78K/0 Series common C compiler library source file |

### (2) PROM Writing Tools

| | |
|---|---|
| PG-1500 | PROM programmer |
| PA-78P018CW<br>PA-78P018GC | Programmer adapter connected to PG-1500 |
| PG-1500 controller | PG-1500 control program |

### (3) Debugging Tool

- **When using in-circuit emulator IE-78K0-NS**

| | |
|---|---|
| IE-78K0-NS | In-circuit emulator common to 78K/0 Series |
| IE-70000-MC-PS-B | Power supply unit for IE-78K0-NS |
| IE-70000-98-IF-C | Interface adapter when using PC-9800 series as host machine (excluding notebook PCs, C bus supported ) |
| IE-70000-CD-IF-A | PC card and interface cable when using notebook PC of PC-9800 series as host machine (PCMCIA socket supported) |
| IE-70000-PC-IF-C | Interface adapter when using IBM PC/AT™ compatible as host machine (ISA bus supported) |
| IE-70000-PCI-IF | Adapter when using PC that incorporates PCI bus as host machine |
| IE-78018-NS-EM1 | Emulation board common to μPD78018F Subseries |
| NP-64CW | Emulation probe for 64-pin plastic shrink DIP (CW type) |
| NP-64GC | Emulation probe for 64-pin plastic QFP (GC-AB8 type) |
| EV-9200GC-64 | Socket to be mounted on target system board manufactured for 64-pin plastic QFP (GC-AB8 type) |
| ID78K0-NS | Integrated debugger for IE-78K0-NS |
| SM78K0 | System simulator common to 78K/0 Series |
| DF78014 | Device file common to μPD78018F Subseries |

• **When using in-circuit emulator IE-78001-R-A**

| | |
|---|---|
| IE-78001-R-A | In-circuit emulator common to 78K/0 Series |
| IE-70000-98-IF-C | Interface adapter when using PC-9800 series as host machine (excluding notebook PCs, C bus supported) |
| IE-70000-PC-IF-C | Interface adapter when using IBM PC/AT compatible as host machine (ISA bus supported) |
| IE-78000-R-SV3 | Interface adapter and cable when using EWS as host machine |
| IE-70000-PCI-IF | Adapter when using PC that incorporates PCI bus as host machine |
| IE-78018-NS-EM1 | Emulation board common to μPD78018F Subseries |
| IE-78K0-R-EX1 | Emulation probe conversion board to use IE-78018-NS-EM1 on IE-78001-R-A |
| EP-78240CW-R | Emulation probe for 64-pin plastic shrink DIP (CW type) |
| EP-78240GC-R | Emulation probe for 64-pin plastic QFP (GC-AB8 type) |
| EV-9200GC-64 | Socket to be mounted on target system board manufactured for 64-pin plastic QFP (GC-AB8 type) |
| ID78K0 | Integrated debugger for IE-78001-R-A |
| SM78K0 | System simulator common to 78K/0 Series |
| DF78014 | Device file common to μPD78018F Subseries |

**(4) Real-time OS**

| | |
|---|---|
| RX78K/0 | Real-time OS for 78K/0 Series |
| MX78K0 | OS for 78K/0 Series |

**(5) Cautions on using development tools**

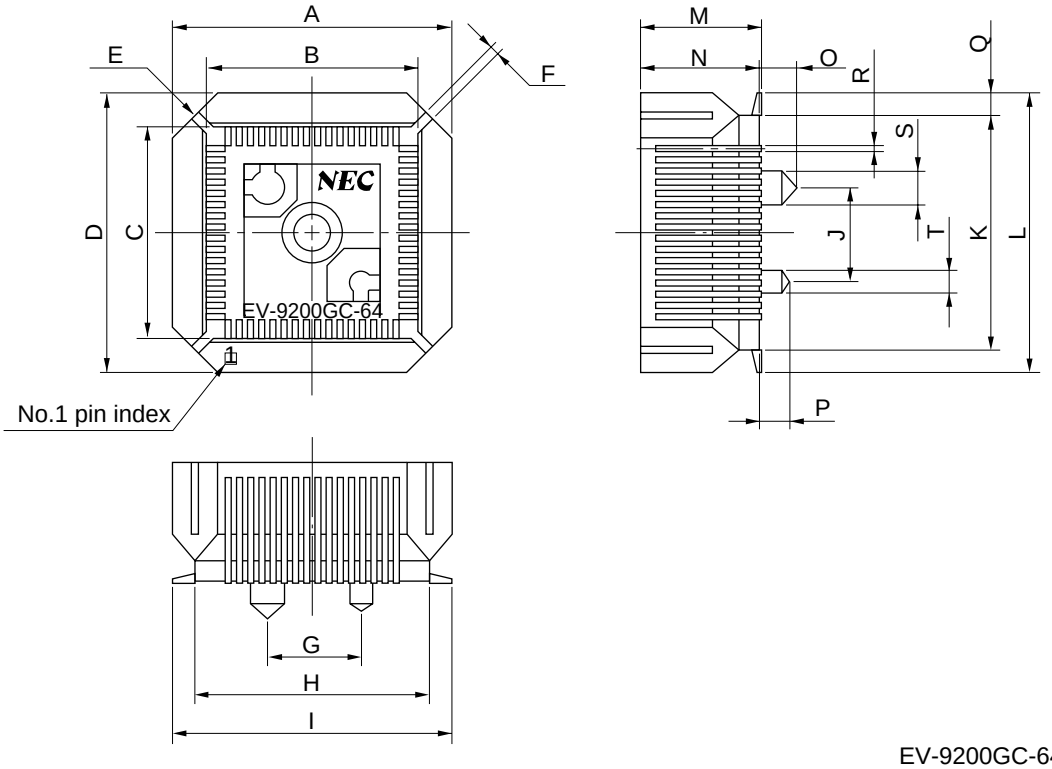
- The ID-78K0-NS, ID78K0, and SM78K0 are used in combination with the DF78014.
- The CC78K/0 and RX78K/0 are used in combination with the RA78K/0 and the DF78014.
- The NP-64CW and NP64GC are products made by Naitou Densei Machidaseisakusho (TEL: +81-44-822-3813). Contact an NEC distributor regarding the purchase of these products.
- For third party development tools, see the **78K/0 Series Selection Guide (U11126E)**.
- The host machines and OSs supporting each software are as follows.

| Host Machine [OS] / Software | PC | EWS |
|---|---|---|
| | PC-9800 series [Windows™]<br>IBM PC/AT compatible<br>[Japanese/English Windows] | HP9000 series 700™ [HP-UX™]<br>SPARCstation™ [SunOS™, Solaris™]<br>NEWS™ (RISC) [NEWS-OS™] |
| RA78K/0 | √Note | √ |
| CC78K/0 | √Note | √ |
| PG-1500 controller | √Note | — |
| ID78K0-NS | √ | — |
| ID78K0 | √ | √ |
| SM78K0 | √ | — |
| RX78K/0 | √Note | √ |
| MX78K0 | √Note | √ |

**Note** DOS-based software

**Conversion Socket Drawing (EV-9200GC-64) and Recommended Footprint**

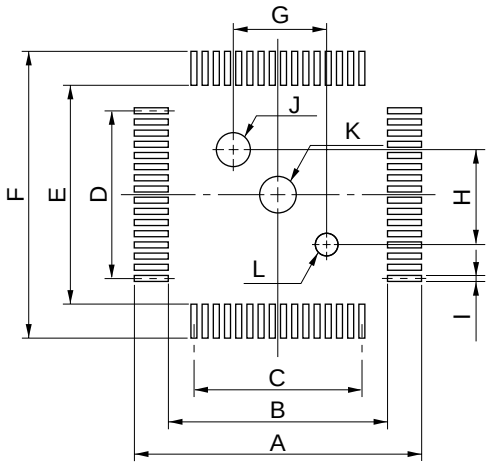
**Figure A-1. Drawing of EV-9200GC-64 (for reference only)**




EV-9200GC-64-G0E

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 18.8 | 0.74 |
| B | 14.1 | 0.555 |
| C | 14.1 | 0.555 |
| D | 18.8 | 0.74 |
| E | 4-C 3.0 | 4-C 0.118 |
| F | 0.8 | 0.031 |
| G | 6.0 | 0.236 |
| H | 15.8 | 0.622 |
| I | 18.5 | 0.728 |
| J | 6.0 | 0.236 |
| K | 15.8 | 0.622 |
| L | 18.5 | 0.728 |
| M | 8.0 | 0.315 |
| N | 7.8 | 0.307 |
| O | 2.5 | 0.098 |
| P | 2.0 | 0.079 |
| Q | 1.35 | 0.053 |
| R | $0.35\pm0.1$ | $0.014^{+0.004}_{-0.005}$ |
| S | $\phi$2.3 | $\phi$0.091 |
| T | $\phi$1.5 | $\phi$0.059 |

★ **Figure A-2. Recommended Footprint of EV-9200GC-64 (for reference only)**




EV-9200GC-64-P1E

| ITEM | MILLIMETERS | INCHES |
|---|---|---|
| A | 19.5 | 0.768 |
| B | 14.8 | 0.583 |
| C | $0.8\pm0.02\times15=12.0\pm0.05$ | $0.031^{+0.002}_{-0.001}\times0.591=0.472^{+0.003}_{-0.002}$ |
| D | $0.8\pm0.02\times15=12.0\pm0.05$ | $0.031^{+0.002}_{-0.001}\times0.591=0.472^{+0.003}_{-0.002}$ |
| E | 14.8 | 0.583 |
| F | 19.5 | 0.768 |
| G | $6.00\pm0.08$ | $0.236^{+0.004}_{-0.003}$ |
| H | $6.00\pm0.08$ | $0.236^{+0.004}_{-0.003}$ |
| I | $0.5\pm0.02$ | $0.197^{+0.001}_{-0.002}$ |
| J | $\phi2.36\pm0.03$ | $\phi0.093^{+0.001}_{-0.002}$ |
| K | $\phi2.2\pm0.1$ | $\phi0.087^{+0.004}_{-0.005}$ |
| L | $\phi1.57\pm0.03$ | $\phi0.062^{+0.001}_{-0.002}$ |

**Caution** Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

## ★ APPENDIX B. RELATED DOCUMENTS

### Device Related Documents

| Document Name | | Document No. | |
|---|---|---|---|
| | | English | Japanese |
| μPD78011F(A), 78012F(A), 78013F(A), 78014F(A), 78015F(A), 78016F(A), 78018F(A) Data Sheet | | U11921E | U11921J |
| μPD78P018F(A) Data Sheet | | This document | U12132J |
| μPD78018F, 78018FY Subseries User's Manual | | U10659E | U10659J |
| 78K/0 Series User's Manual - Instructions | | U12326E | U12326J |
| 78K/0 Series Instruction List | | — | U10903J |
| 78K/0 Series Instruction Set | | — | U10904J |
| μPD78018F Subseries Special Function Register Table | | — | IEM-5594 |
| 78K/0 Series Application Note | Basics (I) | U12704E | U12704J |
| | Floating-Point Arithmetic Programs | IEA-1289 | U13482J |

### Development Tool Documents (User's Manual)

| Document Name | | Document No. | |
|---|---|---|---|
| | | English | Japanese |
| RA78K0 Assembler Package | Operation | U11802E | U11802J |
| | Assembly Language | U11801E | U11801J |
| | Structured Assembly Language | U11789E | U11789J |
| RA78K Series Structured Assembler Preprocessor | | EEU-1402 | U12323J |
| CC78K0 C Compiler | Operation | U11517E | U11517J |
| | Language | U11518E | U11518J |
| CC78K/0 C Compiler Application Note | Programming Know-How | U13034E | U13034J |
| PG-1500 PROM Programmer | | U11940E | U11940J |
| PG-1500 Controller PC-9800 Series (MS-DOS™) Based | | EEU-1291 | EEU-704 |
| PG-1500 Controller IBM PC Series (PC DOS™) Based | | U10540E | EEU-5008 |
| IE-78K0-NS | | To be prepared | To be prepared |
| IE-78001-R-A | | To be prepared | To be prepared |
| IE-78K0-R-EX1 | | To be prepared | To be prepared |
| IE-78018-NS-EM1 | | To be prepared | U13289J |
| EP-78240 | | U10332E | EEU-986 |
| SM78K0 System Simulator Windows Based | Reference | U10181E | U10181J |
| SM78K Series System Simulator | External Part User Open Interface Specification | U10092E | U10092J |
| ID78K0-NS Integrated Debugger Windows Based | Reference | U12900E | U12900J |
| ID78K0 Integrated Debugger EWS Based | Reference | — | U11151J |
| ID78K0 Integrated Debugger PC Based | Reference | U11539E | U11539J |
| ID78K0 Integrated Debugger Windows Based | Guide | U11649E | U11649J |

**Caution The contents of the above related documents are subject to change without notice. The latest documents should be used for design.**

**Embedded Software Documents (User's Manual)**

| Document Name | | Document No. | |
|---|---|---|---|
| | | English | Japanese |
| 78K/0 Series Real-Time OS | Basics | U11537E | U11537J |
| | Installation | U11536E | U11536J |
| 78K/0 Series OS MX78K0 | Basics | U12257E | U12257J |

**Other Documents**

| Document Name | Document No. | |
|---|---|---|
| | English | Japanese |
| NEC IC Package Manual (CD-ROM) | C13388E | — |
| Semiconductor Device Mounting Technology Manual | C10535E | C10535J |
| Quality Grades on NEC Semiconductor Devices | C11531E | C11531J |
| NEC Semiconductor Device Reliability/Quality Control System | C10983E | C10983J |
| Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD) | C11892E | C11892J |
| Guide to Quality Assurance for Semiconductor Devices | MEI-1202 | — |
| Microcomputer Product Series Guide | — | U11416J |

**Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.**

[MEMO]

# NOTES FOR CMOS DEVICES

## ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.**

## ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.**

## ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.**

# Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

**NEC Electronics Inc. (U.S.)**
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

**NEC Electronics (Germany) GmbH**
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

**NEC Electronics (UK) Ltd.**
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

**NEC Electronics Italiana s.r.l.**
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

**NEC Electronics (Germany) GmbH**
Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

**NEC Electronics (France) S.A.**
Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

**NEC Electronics (France) S.A.**
Spain Office
Madrid, Spain
Tel: 01-504-2787
Fax: 01-504-2860

**NEC Electronics (Germany) GmbH**
Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

**NEC Electronics Hong Kong Ltd.**
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

**NEC Electronics Hong Kong Ltd.**
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

**NEC Electronics Singapore Pte. Ltd.**
United Square, Singapore 1130
Tel: 65-253-8311
Fax: 65-250-3583

**NEC Electronics Taiwan Ltd.**
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

**NEC do Brasil S.A.**
Electron Devices Division
Rodovia Presidente Dutra, Km 214
07210-902-Guarulhos-SP Brasil
Tel: 55-11-6465-6810
Fax: 55-11-6465-6829

J98. 11

**FIP, IEBus, and QTOP are trademarks of NEC Corporation.**
**MS-DOS and Windows are trademarks of Microsoft Corporation.**
**PC/AT and PC DOS are trademarks of International Business Machines Corporation.**
**HP9000 series 700 and HP-UX are trademarks of Hewlett-Packard Company.**
**SPARCstation is a trademark of SPARC International, Inc.**
**Solaris and SunOS are trademarks of Sun Microsystems, Inc.**
**NEWS and NEWS-OS are trademarks of Sony Corporation.**

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

The export of this product from Japan is regulated by the Japanese government. To export this product may be prohibited without governmental license, the need for which must be judged by the customer. The export or re-export of this product from a country other than Japan may also be prohibited without a license from that country. Please call an NEC sales representative.