NEC

8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD78F9478, which is a product of the 78K/0S Series, is suitable for remote controllers with an on-chip LCD.

The μPD78F9478 has flash memory in place of the internal ROM of the μPD789478.

Because flash memory allows the program to be written and erased with the device mounted on the target board, this product is ideal for development trials, small-scale production, or for applications that require frequent upgrades.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD789477 Subseries User's Manual:	U15400E
78K/0S Series User's Manual Instructions:	U11047E

FEATURES

- Pin-compatible with mask ROM version (except V_{PP} pin)
- On-chip multiplier: 8 bits × 8 bits = 16 bits
- Flash memory and RAM capacity

Item / Part Number	Program Memory (Flash Memory)	Data Memory	
		Internal High-Speed RAM	LCD Display RAM
μPD78F9478	32 KB	1024 bytes	28 × 4 bits

- Minimum instruction execution time can be selected from high speed (0.4 μs: @5.0 MHz operation with main system clock), low speed (1.6 μs: @5.0 MHz operation with main system clock), and ultra-low speed (122 μs: @32.768 kHz operation with subsystem clock)
- A circuit to multiply the subsystem clock by 4 is selectable by mask option (15.26 μs @131 kHz operation: 32.768 kHz subsystem clock × 4)
- I/O ports: 45 (N-ch open-drain: 4)
- Serial interface: 2 channels
- 8-bit resolution A/D converter: 8 channels
- LCD controller/driver
  Segment signals: 28, common signals: 4
- Timer: 6 channels
- On-chip infrared remote controller receiver
- On-chip key return signal detector
- Supply voltage: V_{DD} = 1.8 to 5.5 V

APPLICATIONS

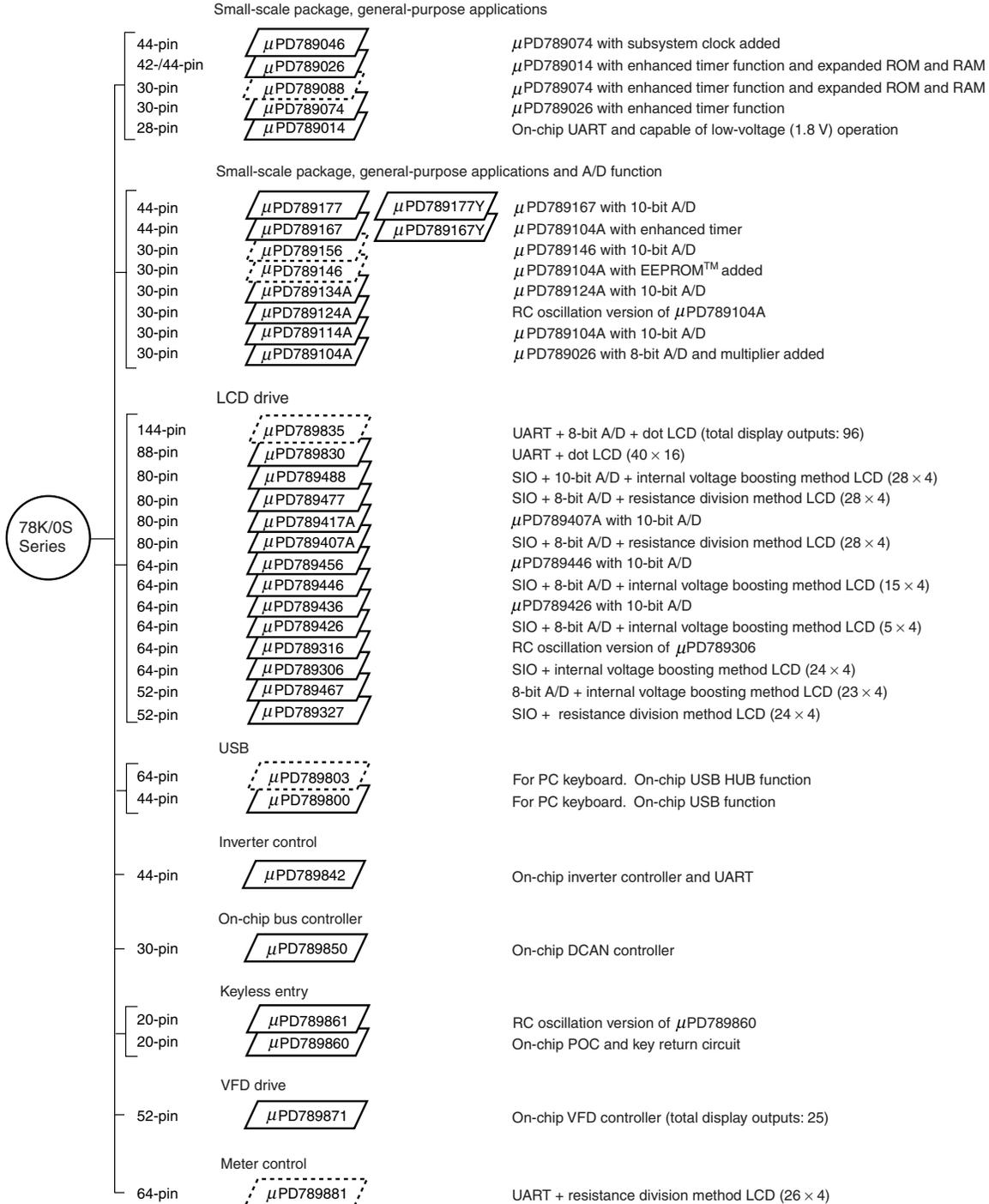CD players, portable audio devices, compact cameras, healthcare equipment, etc.

The mark ★ shows major revised points.

★ **ORDERING INFORMATION**

Part Number	Package
μPD78F9478GC-8BT	80-pin plastic QFP (14 $\times$ 14)

★ **78K/0S SERIES LINEUP**

The products in the 78K/0S Series are listed below. The names enclosed in boxes are subseries names.

Products in mass production

Products under development

Y subseries supports SMB.

Small-scale package, general-purpose applications

44-pin	μPD789046	μPD789074 with subsystem clock added
42-/44-pin	μPD789026	μPD789014 with enhanced timer function and expanded ROM and RAM
30-pin	μPD789088	μPD789074 with enhanced timer function and expanded ROM and RAM
30-pin	μPD789074	μPD789026 with enhanced timer function
28-pin	μPD789014	On-chip UART and capable of low-voltage (1.8 V) operation

Small-scale package, general-purpose applications and A/D function

44-pin	μPD789177	μPD789177Y	μPD789167 with 10-bit A/D
44-pin	μPD789167	μPD789167Y	μPD789104A with enhanced timer
30-pin	μPD789156		μPD789146 with 10-bit A/D
30-pin	μPD789146		μPD789104A with EEPROM™ added
30-pin	μPD789134A		μPD789124A with 10-bit A/D
30-pin	μPD789124A		RC oscillation version of μPD789104A
30-pin	μPD789114A		μPD789104A with 10-bit A/D
30-pin	μPD789104A		μPD789026 with 8-bit A/D and multiplier added

LCD drive

144-pin	μPD789835	UART + 8-bit A/D + dot LCD (total display outputs: 96)
88-pin	μPD789830	UART + dot LCD (40 × 16)
80-pin	μPD789488	SIO + 10-bit A/D + internal voltage boosting method LCD (28 × 4)
80-pin	μPD789477	SIO + 8-bit A/D + resistance division method LCD (28 × 4)
80-pin	μPD789417A	μPD789407A with 10-bit A/D
80-pin	μPD789407A	SIO + 8-bit A/D + resistance division method LCD (28 × 4)
64-pin	μPD789456	μPD789446 with 10-bit A/D
64-pin	μPD789446	SIO + 8-bit A/D + internal voltage boosting method LCD (15 × 4)
64-pin	μPD789436	μPD789426 with 10-bit A/D
64-pin	μPD789426	SIO + 8-bit A/D + internal voltage boosting method LCD (5 × 4)
64-pin	μPD789316	RC oscillation version of μPD789306
64-pin	μPD789306	SIO + internal voltage boosting method LCD (24 × 4)
52-pin	μPD789467	8-bit A/D + internal voltage boosting method LCD (23 × 4)
52-pin	μPD789327	SIO + resistance division method LCD (24 × 4)

USB

64-pin	μPD789803	For PC keyboard. On-chip USB HUB function
44-pin	μPD789800	For PC keyboard. On-chip USB function

Inverter control

44-pin	μPD789842	On-chip inverter controller and UART

On-chip bus controller

30-pin	μPD789850	On-chip DCAN controller

Keyless entry

20-pin	μPD789861	RC oscillation version of μPD789860
20-pin	μPD789860	On-chip POC and key return circuit

VFD drive

52-pin	μPD789871	On-chip VFD controller (total display outputs: 25)

Meter control

64-pin	μPD789881	UART + resistance division method LCD (26 × 4)

78K/0S Series

Remark VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major differences between subseries are shown below.

Series for General-Purpose and LCD Drive

Subseries	Function	ROM Capacity (Bytes)	Timer 8-Bit	16-Bit	Watch	WDT	8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V$_{DD}$ MIN.Value	Remarks
Small-scale package, general-purpose applications	μPD789046	16 K	1 ch	1 ch	1 ch	1 ch	−	−	1 ch (UART: 1ch)	34	1.8 V	−
	μPD789026	4 K to 16 K			−							
	μPD789088	16 K to 32 K	3 ch							24		
	μPD789074	2 K to 8 K	1 ch									
	μPD789014	2 K to 4 K	2 ch	−						22		
Small-scale package, general-purpose applications + A/D converter	μPD789177	16 K to 24 K	3 ch	1 ch	1 ch	1ch	−	8 ch	1 ch (UART: 1ch)	31	1.8 V	−
	μPD789167						8 ch	−				
	μPD789156	8 K to 16 K	1 ch		−		−	4 ch		20		On-chip EEPROM
	μPD789146						4 ch	−				
	μPD789134A	2 K to 8 K					−	4 ch				RC-oscillation version
	μPD789124A						4 ch	−				
	μPD789114A						−	4 ch				−
	μPD789104A						4 ch	−				
LCD drive	μPD789835	24 K to 60 K	6 ch	−	1 ch	1 ch	3 ch	−	1 ch (UART: 1ch)	37	1.8 V[Note]	Dot LCD supported
	μPD789830	24 K	1 ch	1 ch			−			30	2.7 V	
	μPD789488	32 K	3 ch					8 ch	2 ch (UART: 1ch)	45	1.8 V	−
	μPD789478	24 K to 32 K					8 ch	−				
	μPD789417A	12 K to 24 K					−	7 ch	1 ch (UART: 1ch)	43		
	μPD789407A						7 ch	−				
	μPD789456	12 K to 16 K	2 ch				−	6 ch		30		
	μPD789446						6 ch	−				
	μPD789436						−	6 ch		40		
	μPD789426						6 ch	−				
	μPD789316	8 K to 16 K					−		2 ch (UART: 1ch)	23		RC-oscillation version
	μPD789306											−
	μPD789467	4 K to 24 K		−			1 ch		−	18		
	μPD789327						−		1 ch	21		

Note Flash memory version: 3.0 V

Series for ASSP

Function / Subseries		ROM Capacity (Bytes)	Timer				8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_DD MIN.Value	Remarks
			8-Bit	16-Bit	Watch	WDT						
USB	μPD789803	8 K to 16 K	2 ch	−	−	1 ch	−	−	2 ch (USB: 1ch)	41	3.6 V	−
	μPD789800	8 K								31	4.0 V	
Inverter control	μPD789842	8 K to 16 K	3 ch	**Note 1**	1 ch	1 ch	8 ch	−	1 ch (UART: 1ch)	30	4.0 V	−
On-chip bus controller	μPD789850	16 K	1 ch	1 ch	−	1 ch	4 ch	−	2 ch (UART: 1ch)	18	4.0 V	−
Keyless entry	μPD789861	4 K	2 ch	−	−	1 ch	−	−	−	14	1.8 V	RC-oscillation version, on-chip EEPROM
	μPD789860											On-chip EEPROM
VFD drive	μPD789871	4 K to 8 K	3 ch	−	1 ch	1 ch	−	−	1 ch	33	2.7 V	−
Meter control	μPD789881	16 K	2 ch	1 ch	−	1 ch	−	−	1 ch (UART: 1 ch)	28	2.7 V[Note 2]	−

Notes 1. 10-bit timer: 1 channel

2. Flash memory version: 3.0 V

OVERVIEW OF FUNCTIONS

Item		μPD78F9478
Internal memory	Flash memory	32 KB
	High-speed RAM	1024 bytes
	LCD display RAM	28 × 4 bits
Main system clock (oscillation frequency)		Ceramic/crystal oscillation (1.0 to 5.0 MHz)
Subsystem clock (oscillation frequency)		Crystal oscillation (32.768 kHz)
Minimum instruction execution time		0.4 μs/1.6 μs (@5.0 MHz operation with main system clock)
		122 μs (@32.768 kHz operation with subsystem clock)
		15.26 μs (@131 kHz operation with ×4 subsystem clock)
Subsystem clock multiplication function		×4 multiplication circuit (operating supply voltage: V_{DD} = 2.7 to 5.5 V, selected by subclock selection register)
General-purpose registers		8 bits × 8 registers
Instruction set		• 16-bit operations • Bit manipulation (set, reset, test) etc.
Multiplier		8 bits × 8 bits = 16 bits
I/O ports		Total: 45[Note] CMOS I/O: 29 CMOS input: 12 N-ch open-drain I/O: 4
Timers		• 16-bit timer: 1 channel • 8-bit timer: 3 channels • Watch timer: 1 channel • Watchdog timer: 1 channel
Timer outputs		4
Serial interface		UART/3-wire serial I/O mode: 1 channel 3-wire serial I/O mode (with automatic transmit/receive function): 1 channel
A/D converter		8-bit resolution × 8 channels
LCD controller/driver		• Segment signal outputs: 28[Note] • Common signal outputs: 4
Power supply method for LCD drive		External resistance division method
Infrared remote controller reception function		On-chip
Key return detection function		8 pins
Vectored interrupt sources	Maskable	Internal: 16, External: 5
	Non-maskable	Internal: 1
Reset		• Reset by $\overline{\text{RESET}}$ signal input • Internal reset by watchdog timer
Supply voltage		V_{DD} = 1.8 to 5.5 V
Operating ambient temperature		T_A = −40 to +85°C
★ Package		80-pin plastic QFP (14 × 14)

Note 12 pins are used either as a port function or LCD segment output selected by a port function register.

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

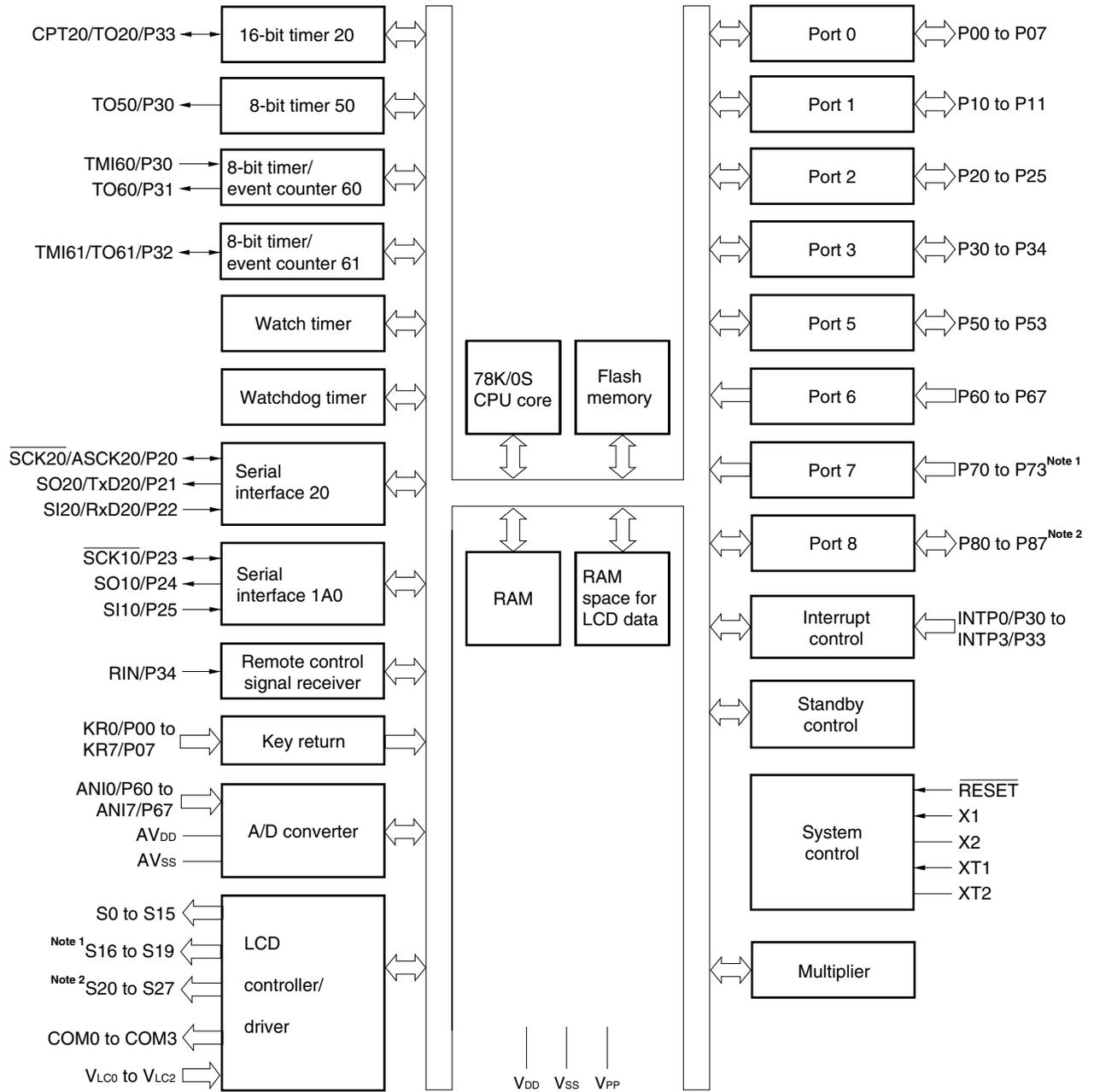**80-pin plastic QFP (14 × 14)**
    µPD78F9478GC-8BT
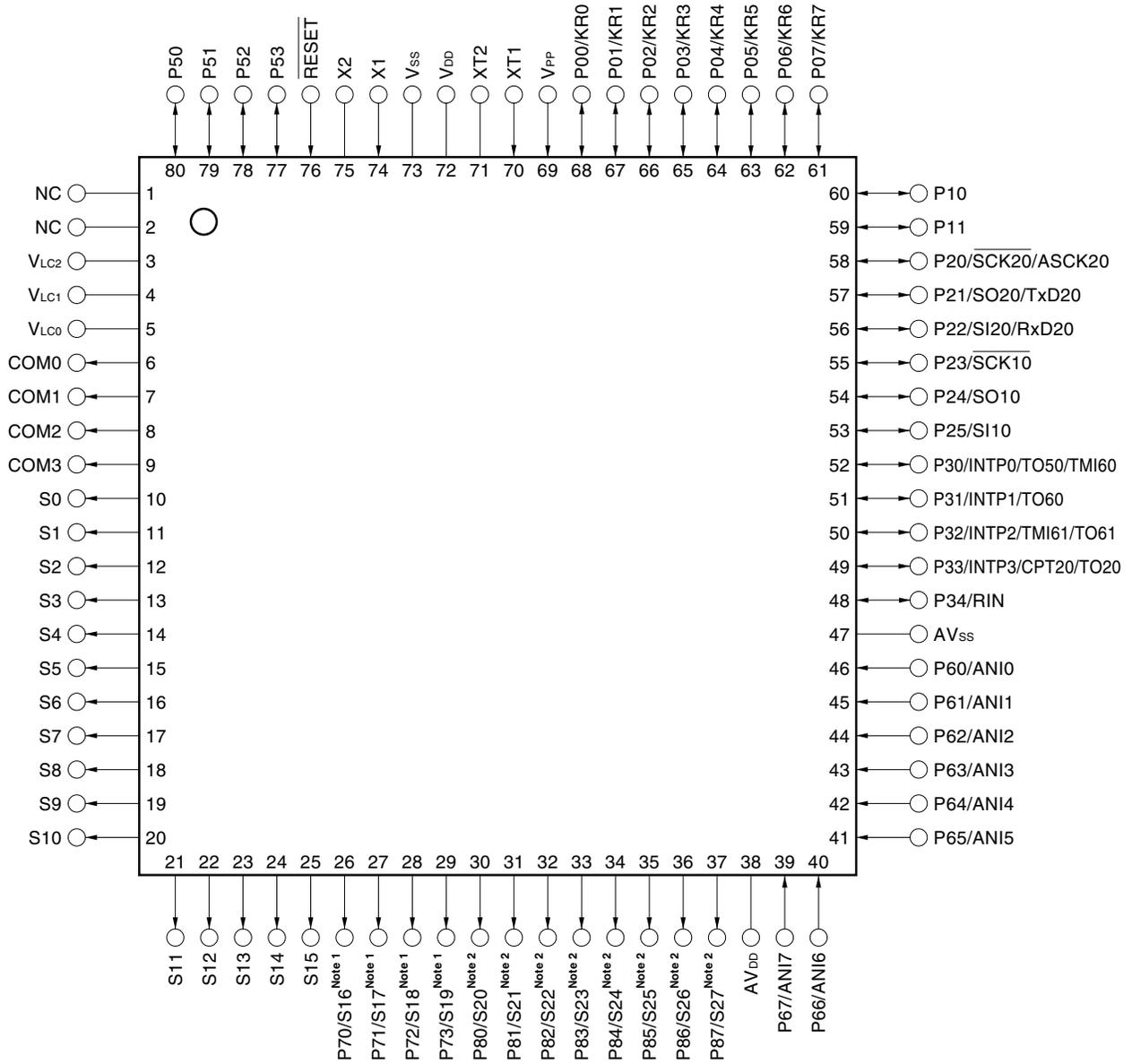
Notes 1. Whether to use these pins as input ports (P70 to P73) or segment outputs (S16 to S19) can be selected in 1-bit units using port function register 7 (PF7).

    2. Whether to use these pins as I/O ports (P80 to P87) or segment outputs (S20 to S27) can be selected in 1-bit units using port function register 8 (PF8).

★ **Caution**   **Connect the V$_{PP}$ pin independently to V$_{SS}$ via a 10 kΩ resistor.**

Pin Name

ANI0 to ANI7:	Analog input	$\overline{\text{RESET}}$:	Reset
ASCK20:	Asynchronous serial input	RIN:	Remote control input
AV$_{DD}$:	Analog power supply	RxD0:	Receive data
AV$_{SS}$:	Analog ground	S0 to S27:	Segment output
CPT20:	Capture trigger input	$\overline{\text{SCK10}}$:	Serial clock input/output
COM0 to COM3:	Common output	SI10:	Serial data input
INTP0 to INTP3:	External interrupt input	SO10:	Serial data output
NC:	No connection	$\overline{\text{SCK20}}$:	Serial clock input/output
KR0 to KR7:	Key return	SI20:	Serial data input
P00 to P07:	Port 0	SO20:	Serial data output
P10, P11:	Port 1	TO20, 50, 60, 61:	Timer output
P20 to P25:	Port 2	TMI60,61:	Timer input
P30 to P34:	Port 3	TxD0:	Transmit data
P50 to P53:	Port 5	V$_{DD}$:	Power supply
P60 to P67:	Port 6	V$_{LC0}$ to V$_{LC2}$:	Power supply for LCD
P70 to P73:	Port 7	V$_{PP}$:	Programming power supply
P80 to P87:	Port 8	V$_{SS}$:	Ground
		X1, X2:	Crystal (main system clock)
		XT1, XT2:	Crystal (subsystem clock)

2. BLOCK DIAGRAM

Notes 1. Whether to use these pins as input ports (P70 to P73) or segment outputs (S16 to S19) can be selected in 1-bit units using port function register 7 (PF7).

2. Whether to use these pins as I/O ports (P80 to P87) or segment outputs (S20 to S27) can be selected in 1-bit units using port function register 8 (PF8).

3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P07	I/O	Port 0. 8-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified in 1-bit units using pull-up resistor option register B0 (PUB0) or key return mode register 00 (KRM00).	Input	KR0 to KR7
P10, P11	I/O	Port 1. 2-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified in 1-bit units using pull-up resistor option register B1 (PUB1).	Input	–
P20	I/O	Port 2. 6-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified in 1-bit units using pull-up resistor option register B2 (PUB2).	Input	$\overline{\text{SCK20}}$/ASCK20
P21				SO20/TxD20
P22				SI20/RxD20
P23				$\overline{\text{SCK10}}$
P24				SO10
P25				SI10
P30	I/O	Port 3. 5-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, on-chip pull-up resistors can be specified in 1-bit units using pull-up resistor option register B3 (PUB3).	Input	INTP0/TO50/TMI60
P31				INTP1/TO60
P32				INTP2/TMI61/TO61
P33				INTP3/CPT20/TO20
P34				RIN
P50 to P53	I/O	Port 5. 4-bit N-ch open-drain I/O port. Input/output can be specified in 1-bit units.	Input	–
P60 to P67	Input	Port 6. 8-bit input port.	Input	ANI0 to ANI7
P70 to P73[Note 1]	Input	Port 7. 4-bit input port. (Only when input port is selected by port function register 7)	Input	–
P80 to P87[Note 2]	I/O	Port 8. 8-bit I/O port. (Only when I/O port is selected by port function register 8)	Input	–

Notes 1. Whether to use these pins as input ports (P70 to P73) or segment outputs (S16 to S19) can be selected in 1-bit units using port function register 7 (PF7).

    2. Whether to use these pins as I/O ports (P80 to P87) or segment outputs (S20 to S27) can be selected in 1-bit units using port function register 8 (PF8).

3.2 Non-Port Pins

| Pin Name	I/O	Function		After Reset	Alternate Function
INTP0 to INTP3	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.		Input	P30 to P33
KR0 to KR7	Input	Key return signal detection		Input	P00 to P07
TO20	Output	16-bit timer 20 output		Input	P33/INTP3/CPT20
CPT20	Output	Capture edge input of 16-bit timer 20		Input	P33/INTP3/TO20
TO50	Output	8-bit timer 50 output		Input	P30/INTP0/TMI60
TO60	Output	8-bit timer 60 output		Input	P31/INTP1
TO61	Output	8-bit timer 61 output		Input	P32/INTP2/TMI61
TMI60	Input	External count clock input to 8-bit timer 60		Input	P30/INTP0/TO50
TMI61	Input	External count clock input to 8-bit timer 61		Input	P32/INTP2/TO61
$\overline{SCK20}$	I/O	Serial clock input/output of serial interface		Input	P20/ASCK20
$\overline{SCK10}$					P23
SO20	Output	Serial data output of serial interface		Input	P21/TxD20
SO10					P24
SI20	Input	Serial data input of serial interface		Input	P22/RxD20
SI10					P25
ASCK20	Input	Serial clock input of asynchronous serial interface		Input	P20/$\overline{SCK20}$
TxD20	Output	Serial data output of asynchronous serial interface		Input	P21/SO20
RxD20	Input	Serial data input of asynchronous serial interface		Input	P22/SI20
RIN	Input	Remote controller receive data input		Input	P34
S0 to S15	Output	LCD controller/driver segment signal outputs		Low-level output	–
S16 to S19[Note 1]			Only when segment output is selected		–
S20 to S27[Note 2]			Only when segment output is selected		–
COM0 to COM3	Output	LCD controller/driver common signal outputs		Low-level output	–
V_{LC0} to V_{LC2}	–	LCD drive voltage		–	–
ANI0 to ANI7	–	A/D converter analog input		–	P60 to P67
AV_{SS}	–	A/D converter ground potential		–	–
AV_{DD}	–	A/D converter analog power supply		–	–
X1	Input	Connecting crystal resonator for main system clock oscillation		–	–
X2	–			–	–
XT1	Input	Connecting crystal resonator for subsystem clock oscillation		–	–
XT2	–			–	–
$\overline{RESET}$	Input	System reset input		Input	–
V_{DD}	–	Positive power supply		–	–
V_{SS}	–	Ground potential		–	–
V_{PP}	–	Flash memory programming mode setting. High-voltage application for program write/verify. Connect independently to V_{SS} via a 10 kΩ resistor.		–	–
NC	–	No connection. Leave open.		–	–

Notes 1. Whether to use these pins as input ports (P70 to P73) or segment outputs (S16 to S19) can be selected in 1-bit units using port function register 7 (PF7)

2. Whether to use these pins as I/O ports (P80 to P87) or segment outputs (S20 to S27) can be selected in 1-bit units using port function register 8 (PF8)

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins is shown in Table 3-1.
For the I/O circuit configuration of each type, refer to Figure 3-1.

Table 3-1. Types of Pin I/O Circuits and Recommended Connection of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/KR0 to P07/KR7	8-A	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P10, P11	5-A		
P20/$\overline{SCK20}$/ASCK20	8-A		
P21/SO20/TxD20	5-A		
P22/SI20/RxD20	8-A		
P23/$\overline{SCK10}$			
P24/SO10	5-A		
P25/SI10	8-A		
P30/INTP0/TO50/TMI60			Input: Independently connect to V_{SS} via a resistor. Output: Leave open.
P31/INTP1/TO60			
P32/INTP2/TO61/TMI61			
P33/INTP3/CPT20/TO20			
P34/RIN			
P50 to P53	13-V		Input: Independently connect to V_{DD} via a resistor. Output: Leave open.
P60/ANI0 to P67/ANI7	9-C	Input	Connect to V_{DD} or V_{SS}.
P70 to P73[Note 1]	2-H		
P80 to P87[Note 1]	5-K	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
COM0 to COM3	18	Output	Leave open.
S0 to S15	17		
S16 to S19[Note 2]			
S20 to S27[Note 2]			
V_{LC0} to V_{LC2}	–	–	
XT1		Input	Connect to V_{SS}.
XT2		–	Leave open.
$\overline{RESET}$	2	Input	–
V_{PP}	–	–	Independently connect to V_{SS} via a 10 kΩ resistor.
NC			Leave open.

Notes 1. Only when selected as a port pin by a port function register.

2. Only when selected as a segment output pin by a port function register.

Figure 3-1. I/O Circuit Types (1/2)

Type 2

IN

Schmitt-triggered input with hysteresis characteristics.

Type 2-H

IN

Input enable

Type 5-A

VDD
Pull-up enable
P-ch
VDD
Data
P-ch
IN/OUT
Output disable
N-ch
VSS
Input enable

Type 5-K

VDD
Data
P-ch
IN/OUT
Output disable
N-ch
Input enable

Type 8-A

VDD
Pull-up enable
P-ch
VDD
Data
P-ch
IN/OUT
Output disable
N-ch
VSS

Type 9-C

IN
P-ch
N-ch
Comparator
AVSS
VREF
(Threshold voltage)
Input enable

Figure 3-1. I/O Circuit Types (2/2)
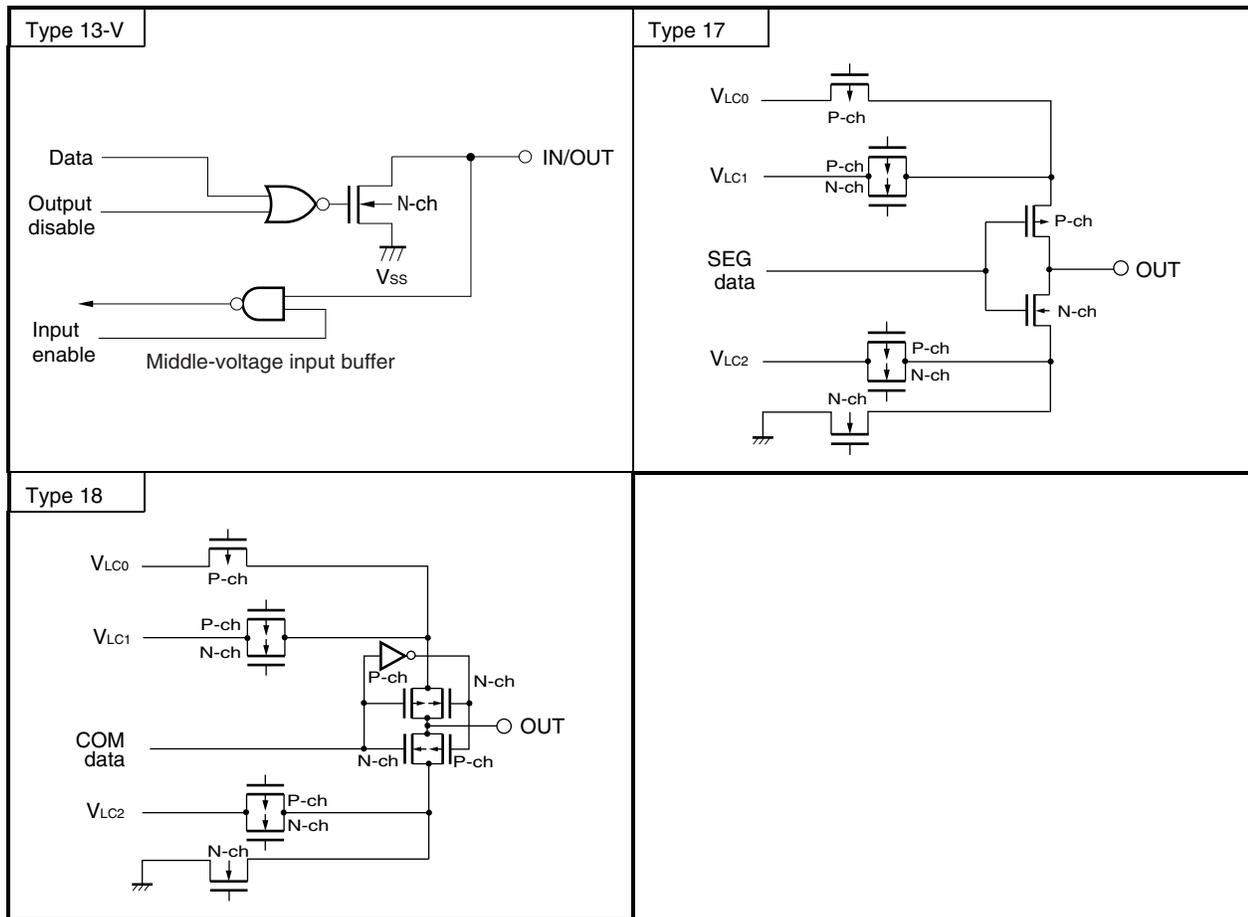
4. MEMORY SPACE

The µPD78F9478 is provided with 64 KB of accessible memory space. Figure 4-1 shows the memory map.

Figure 4-1. Memory Map
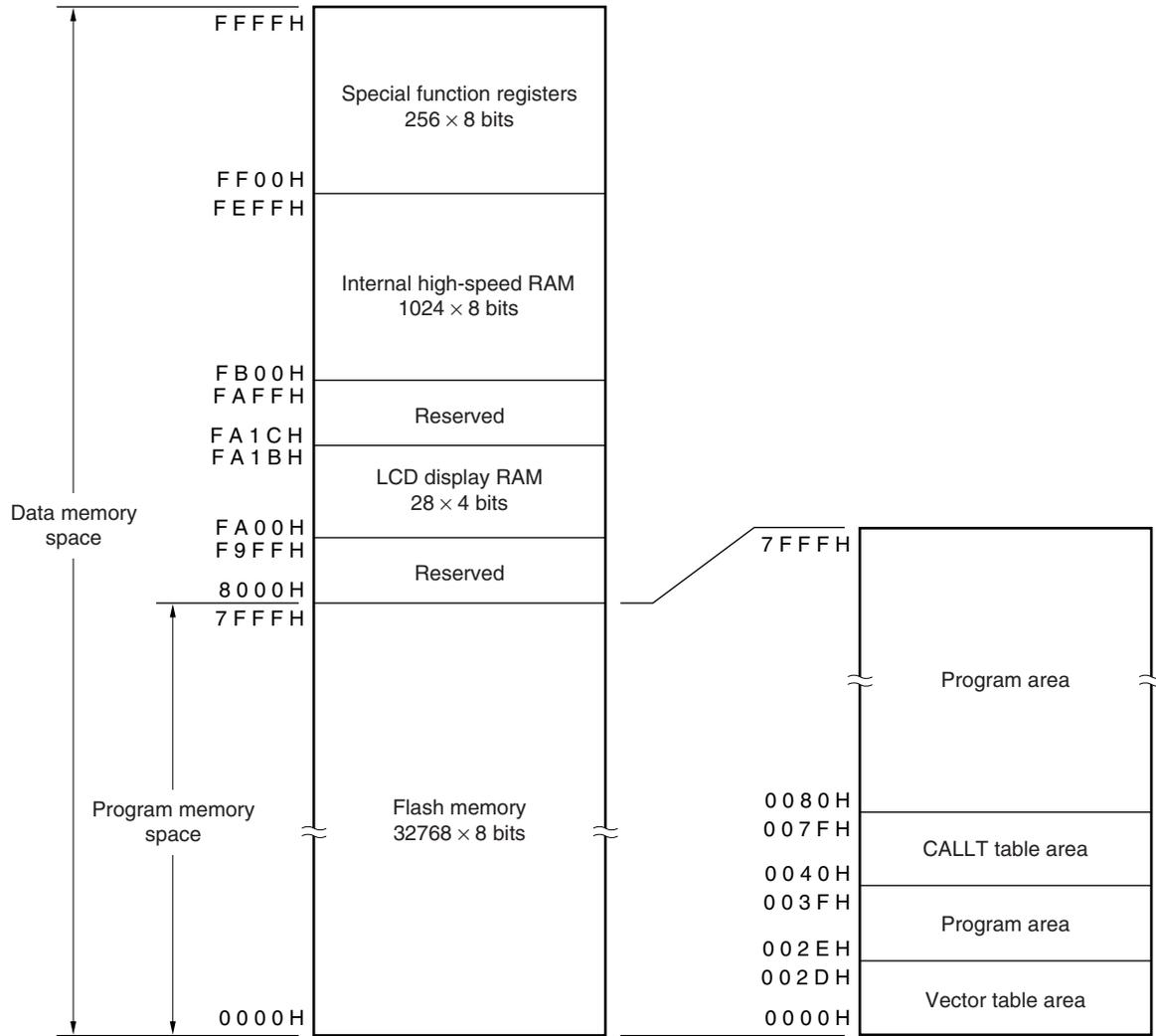
5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

Various kinds of control operations are possible using the ports provided in the μPD78F9478. These ports are illustrated in Figure 5-1 and their functions are listed in Table 5-1.

A number of alternate functions are also provided, except for those ports functioning as digital I/O ports. Refer to **3. PIN FUNCTIONS** for details of the alternate function pins.

Figure 5-1. Ports
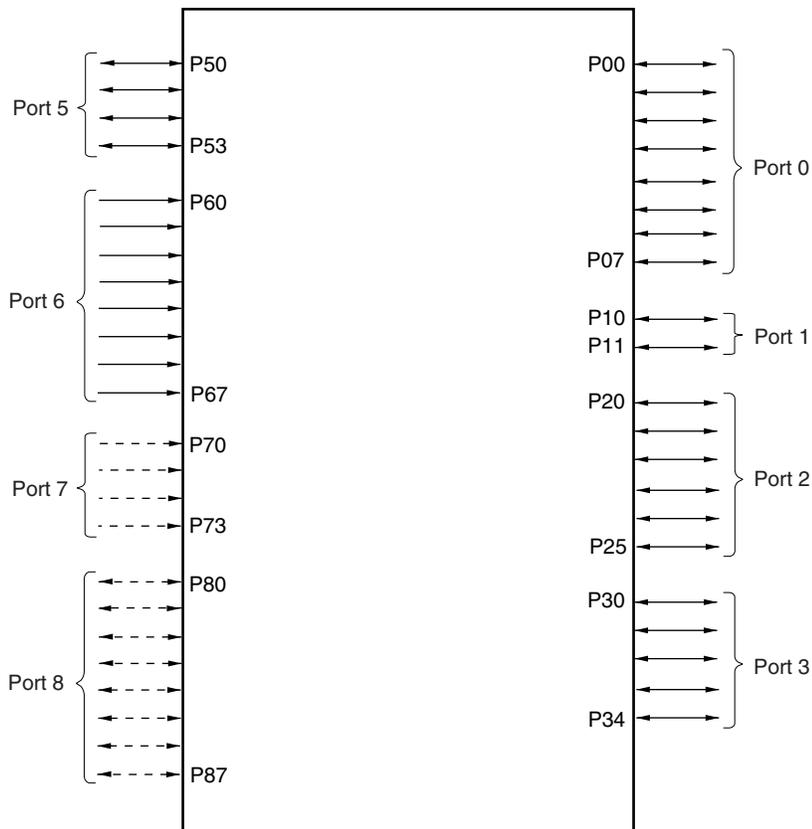
Remark Ports 7 and 8 are used when the port function is selected by a port function register.

Table 5-1. Port Functions

Port Name	Pin Name	Function
Port 0	P00 to P07	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified in 1-bit units using pull-up resistor option register B0 (PUB0) or key return mode register 00 (KRM00).
Port 1	P10, P11	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified in 1-bit units using pull-up resistor option register B1 (PUB1).
Port 2	P20 to P25	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified in 1-bit units using pull-up resistor option register B2 (PUB2).
Port 3	P30 to P34	I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified in 1-bit units using pull-up resistor option register B3 (PUB3).
Port 5	P50 to P53	N-ch open-drain I/O port. Input/output can be specified in 1-bit units.
Port 6	P60 to P67	Input port
Port 7[Note 1]	P70 to P73	Input port (only when input port is selected by a port function register)
Port 8[Note 2]	P80 to P87	I/O port (only when I/O port is selected by a port function register)

Notes 1. Whether to use these pins as input ports (P70 to P73) or segment outputs (S16 to S19) can be selected in 1-bit units using a port function register.

2. Whether to use these pins as I/O ports (P80 to P87) or segment outputs (S20 to S27) can be selected in 1-bit units using a port function register.

5.2 Clock Generator

The clock generator generates the clock pulse to be supplied to the CPU and peripheral hardware.

There are two types of system clock oscillators:

- Main system clock oscillator (ceramic/crystal resonator)

  This circuit oscillates a frequency of 1.0 to 5.0 MHz. Oscillation can be stopped by executing the STOP instruction or by a processor clock control register (PCC) setting.
- Subsystem clock oscillator

  This circuit oscillates a frequency of 32.768 kHz. Oscillation can be stopped using the subclock oscillation mode register (SCKM). A circuit to multiply the subclock by 4 can also be used by a subclock selection register (SSCK).

★

Figure 5-2 Clock Generator Block Diagram
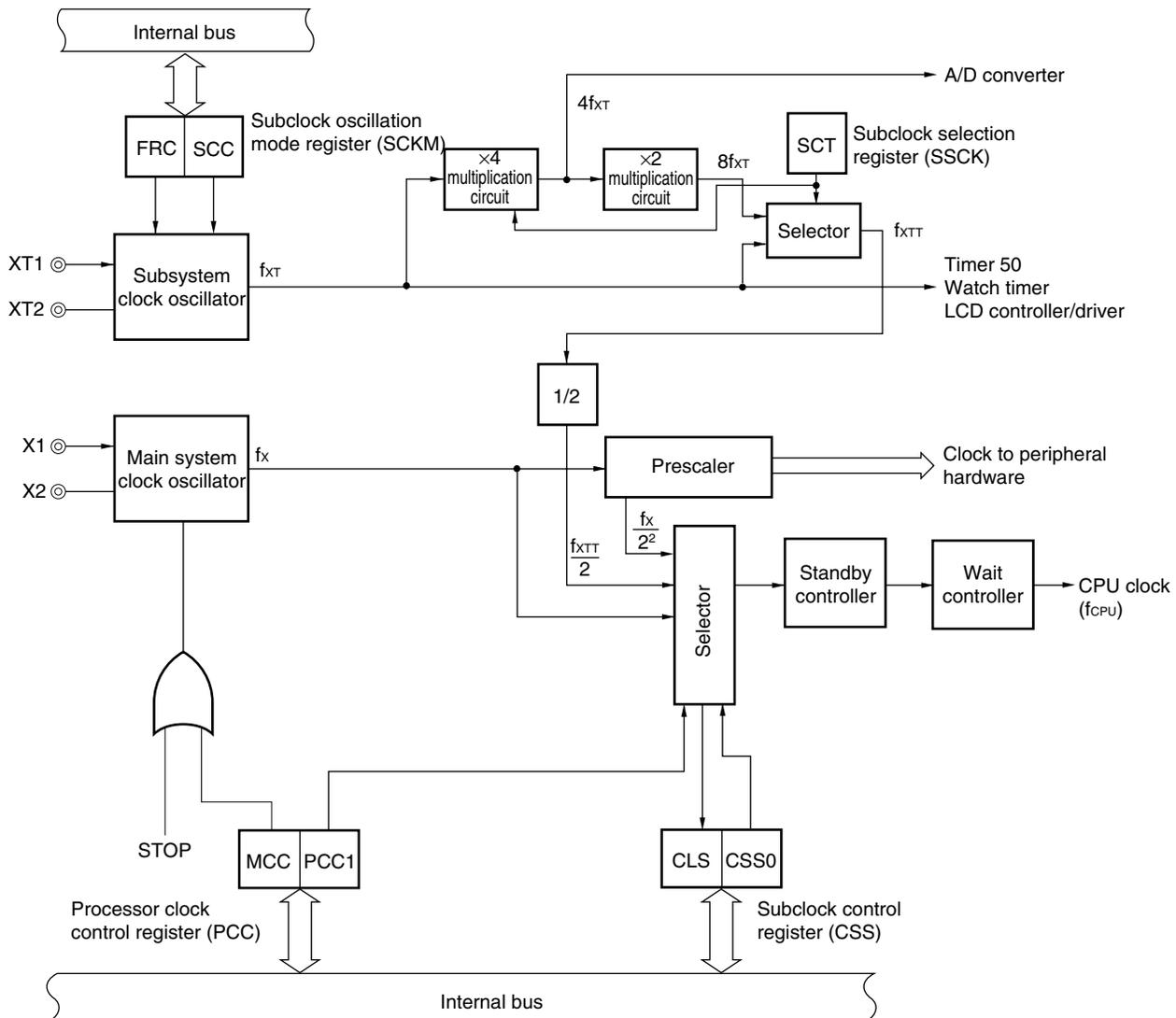
5.3 16-Bit Timer

16-bit timer 20 (TM20) has the following functions.

- Timer interrupt
- Timer output
- Count value capture

(1) Timer interrupt

An interrupt occurs when the count value and compare value match.

(2) Timer output

Timer output control is enabled when the count value and compare value match.

(3) Count value capture

The TM20 count value is captured and held in the capture register in synchronization with the capture trigger.

Figure 5-3. Block Diagram of 16-Bit Timer
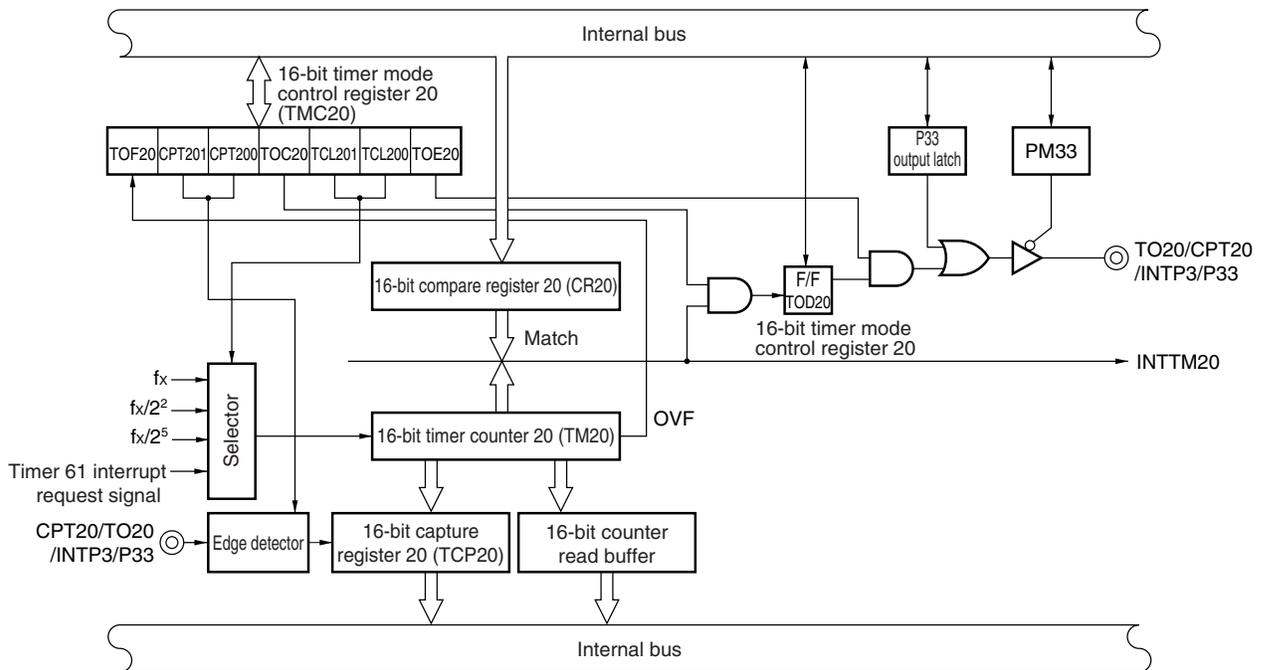
5.4 8-Bit Timer/Event Counter

One 8-bit timer channel (timer 50) and two 8-bit timer/event counter channels (timers 60 and 61) are incorporated in the *μ*PD78F9478. The operation modes listed in the following table can be set via mode register settings.

Table 5-2. Operation Modes

Channel / Mode	Timer 50	Timer 60	Timer 61
8-bit timer counter mode (stand-alone mode)	Available	Available	Available
16-bit timer counter mode (cascade connection mode)	Available		Not available
Carrier generator mode	Available		Not available
PWM output mode	Available	Not available	Not available
PPG output mode	Not available	Available	Available
24-bit event counter mode (connect with 16-bit timer 20)	Not available	Not available	Available

(1) Mode to use 8-bit timer/event counter as discrete unit (stand-alone mode)
    The following functions can be used in this mode.
    <Timer 50>
- Interval timer with 8-bit resolution
- Square-wave output with 8-bit resolution
    <Timer 60 and 61>
- Interval timer with 8-bit resolution
- External event counter with 8-bit resolution
- Square-wave output with 8-bit resolution

(2) Mode to use timer 50 and timer 60 connected in cascade (16-bit resolution: cascade connection)
    Operation as a 16-bit timer/event counter is enabled in cascade connection mode.
    The following functions can be used in this mode.

- Interval timer with 16-bit resolution
- External event counter with 16-bit resolution
- Square-wave output with 16-bit resolution

(3) Carrier generator mode
    The carrier clock generated by timer 60 is output in the cycle set by timer 50.

(4) PWM output mode (PWM: Pulse Width Modulation)
    Pulses are output using any duty ratio (pulse width). The cycle (overflow cycle of the timer) becomes constant (free running).

(5) PPG output mode (PPG: Programmable Pulse Generator)

Pulses are output using any set cycle or duty ratio (pulse width) (both the cycle and pulse width are programmable).

(6) 24-bit event counter mode

Operation as external event counter with 24-bit resolution is enabled using 16-bit timer 20 and timer 61. However, this mode operates only as a counter read function.

There is no compare, match, or clear function.

Figure 5-4. Block Diagram of 24-Bit Event Counter

Figure 5-5. Block Diagram of Timer 50
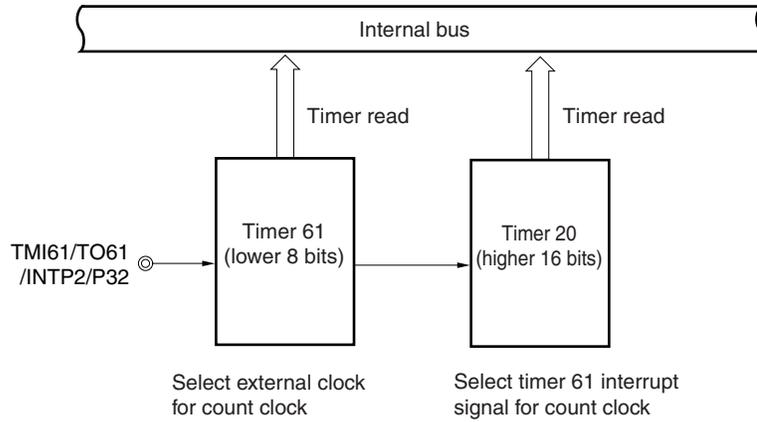
Figure 5-6. Block Diagram of Timer 60
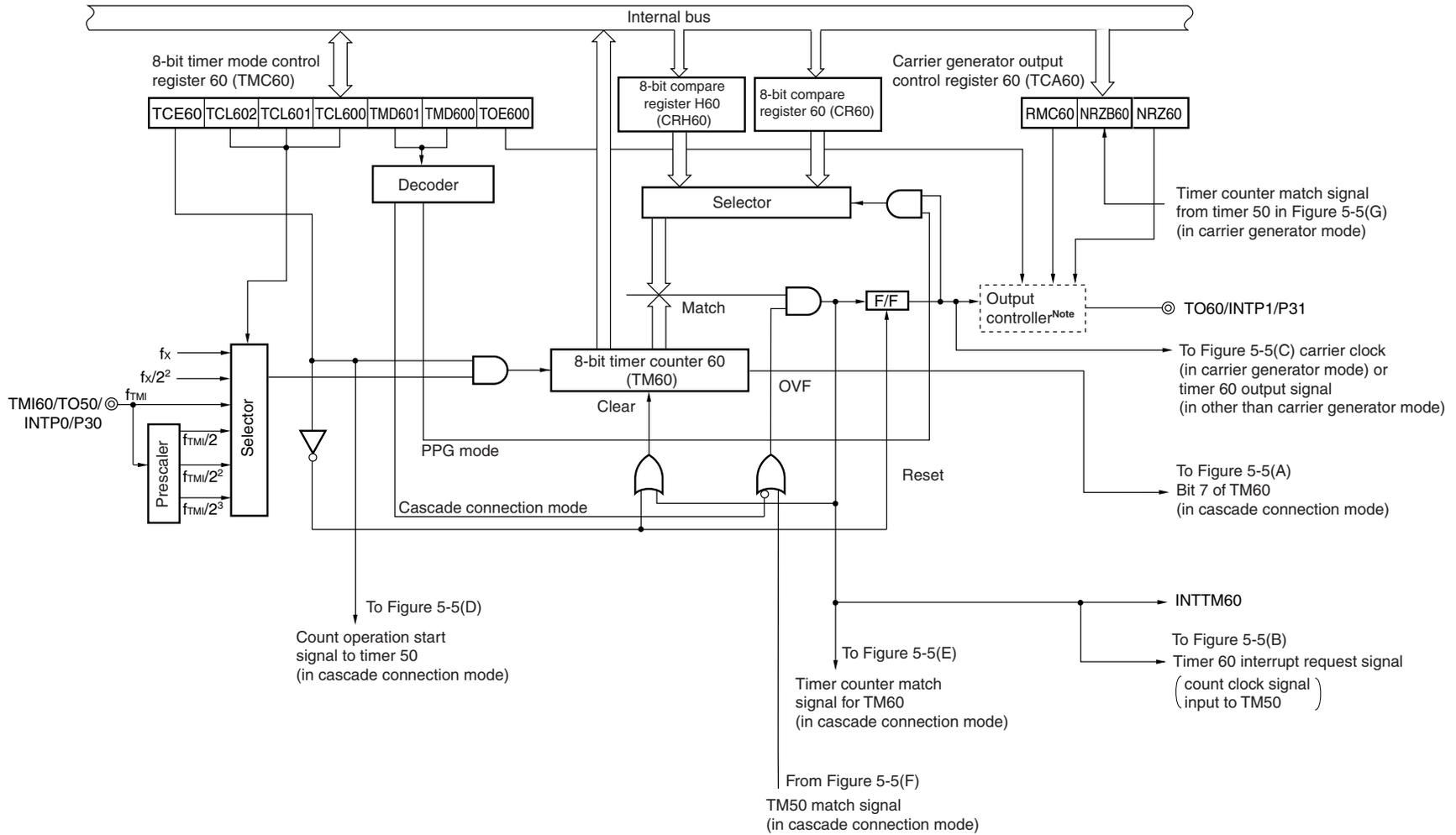
Note For details, see **Figure 5-8**.

Figure 5-7. Block Diagram of Timer 61
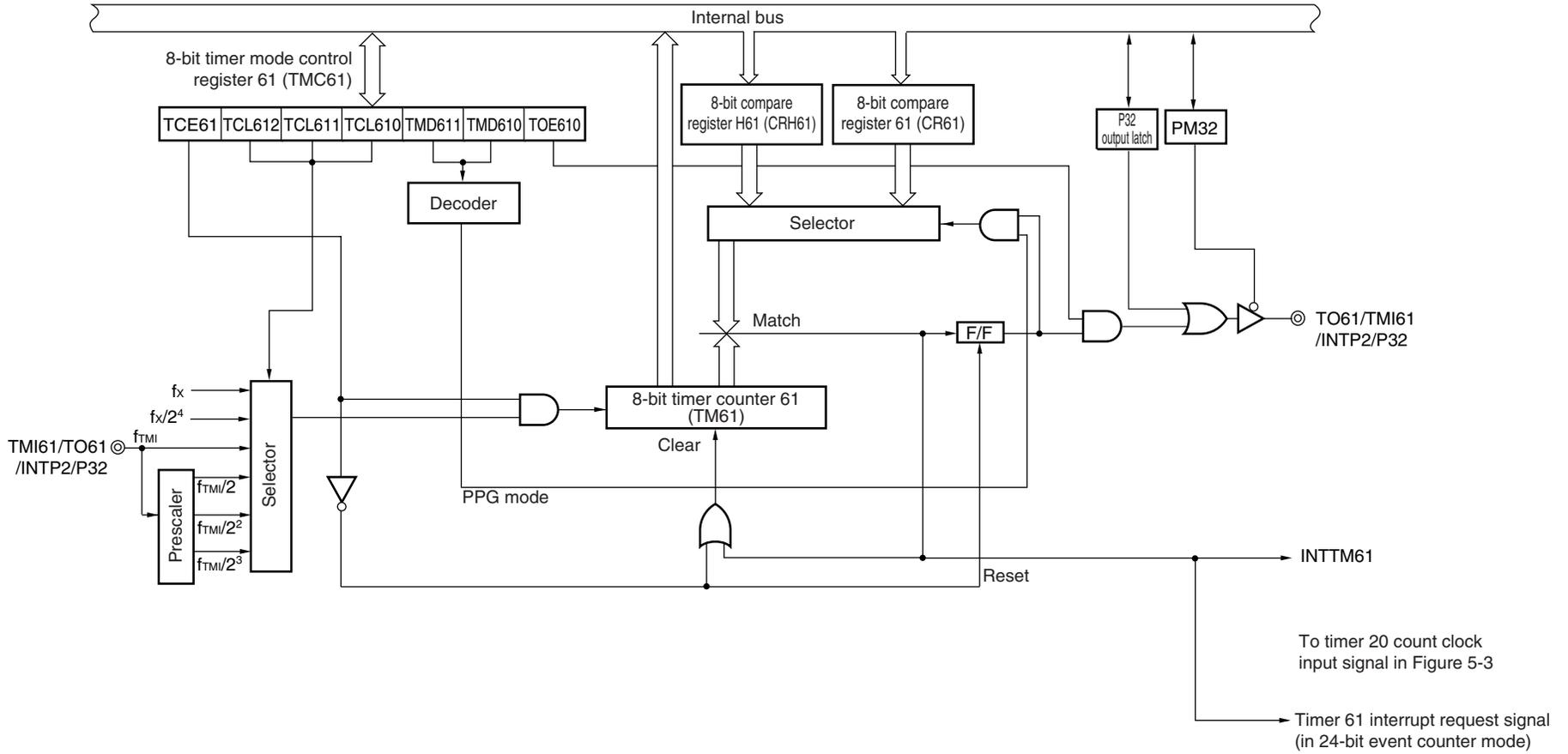
Figure 5-8. Output Controller Block Diagram
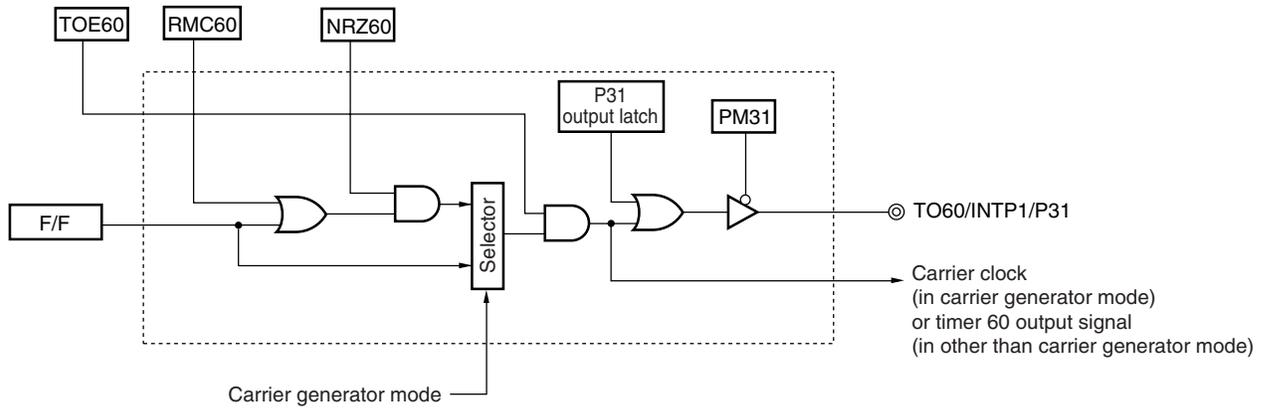
5.5 Watch Timer

The watch timer has the following functions.

- Watch timer
- Interval timer

This timer can be used as a watch timer and interval timer at the same time.

(1) Watch timer

An interrupt request (INTWT) occurs at an interval of 0.5 second when using either the 4.19 MHz main system clock or the 32.768 kHz subsystem clock.

Also, an interrupt request (INTWT) occurs at an interval of 1.0 seconds when using the 32.768 kHz subsystem clock via a setting in the watch timer interrupt time selection register (WTIM).

Caution   An interval of 0.5 second cannot be created when using the 5.0 MHz main system clock. Instead, switch to the 32.768 kHz subsystem clock, and then create the 0.5-second interval.

(2) Interval timer

An interrupt request (INTWTI) occurs at preset intervals.

Figure 5-9. Watch Timer Block Diagram
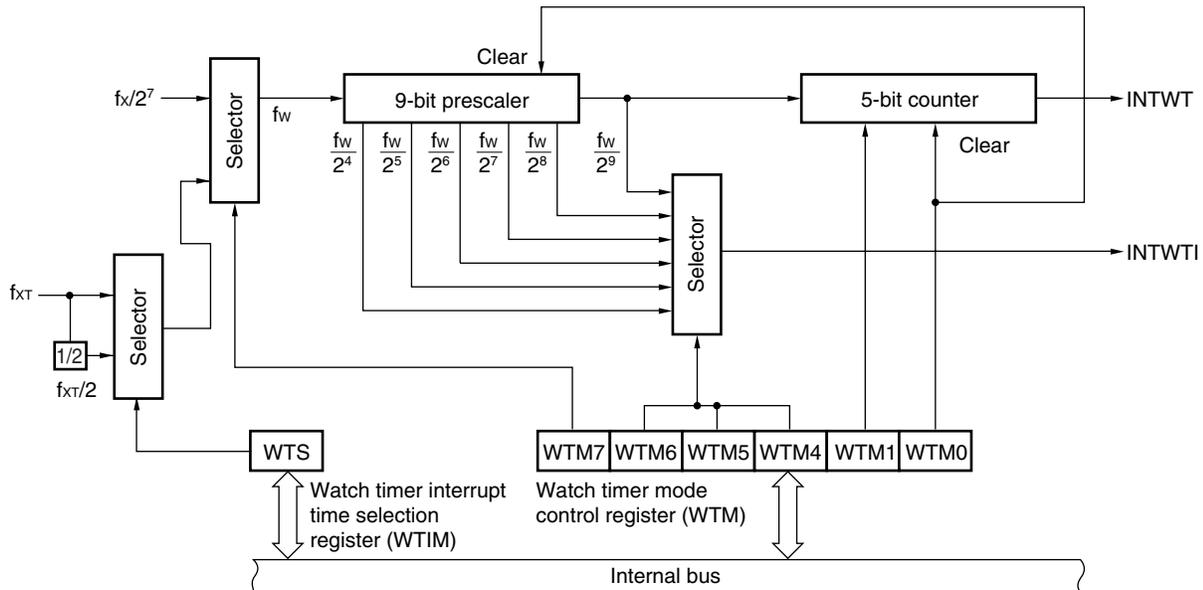
5.6 Watchdog Timer

The watchdog timer has the following functions.

(1) Watchdog timer

The watchdog timer detects an inadvertent program loop. When a loop is detected, a non-maskable interrupt or the $\overline{\text{RESET}}$ signal can be issued.

(2) Interval timer

An interrupt is issued at preset intervals (any interval time can be set).

Figure 5-10. Watchdog Timer Block Diagram
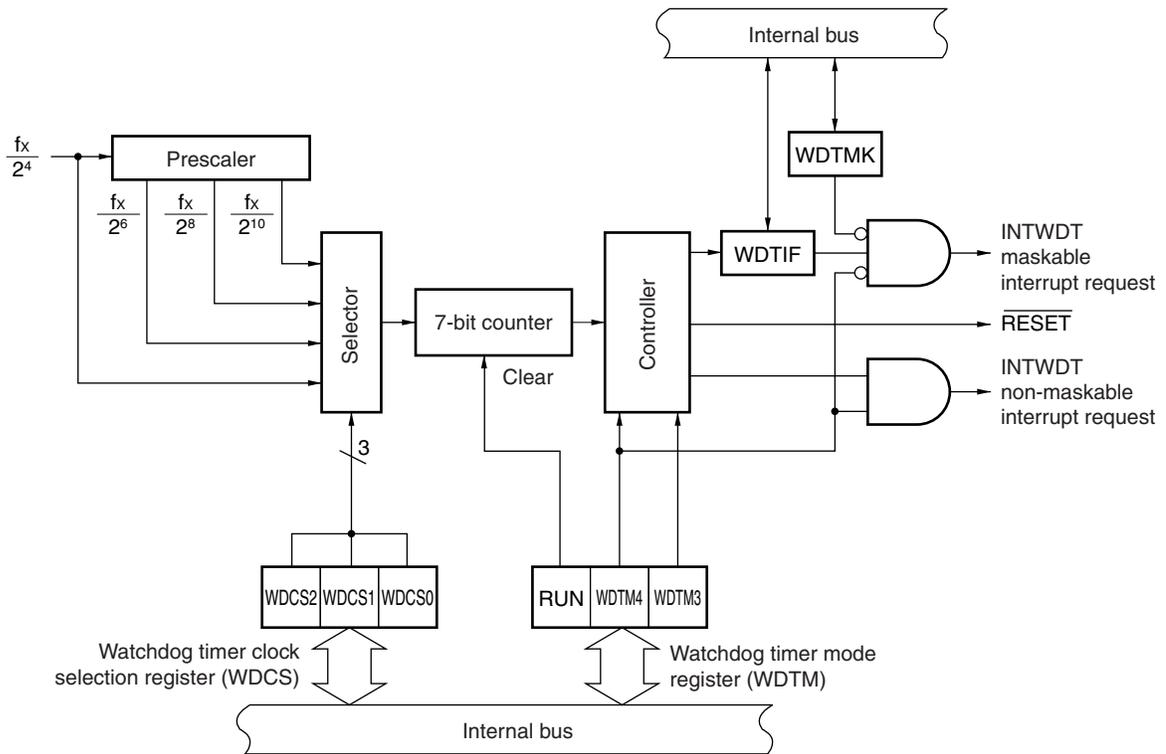
⋆ **5.7 Remote Controller Receiver**

The remote controller receiver uses the following remote controller reception mode.

- A-type reception mode ... with guide pulse (half clock)

It also has a function to supply signals externally input to the RIN pin to the circuit, after eliminating noise.

Figure 5-11. Block Diagram of Remote Controller Receiver
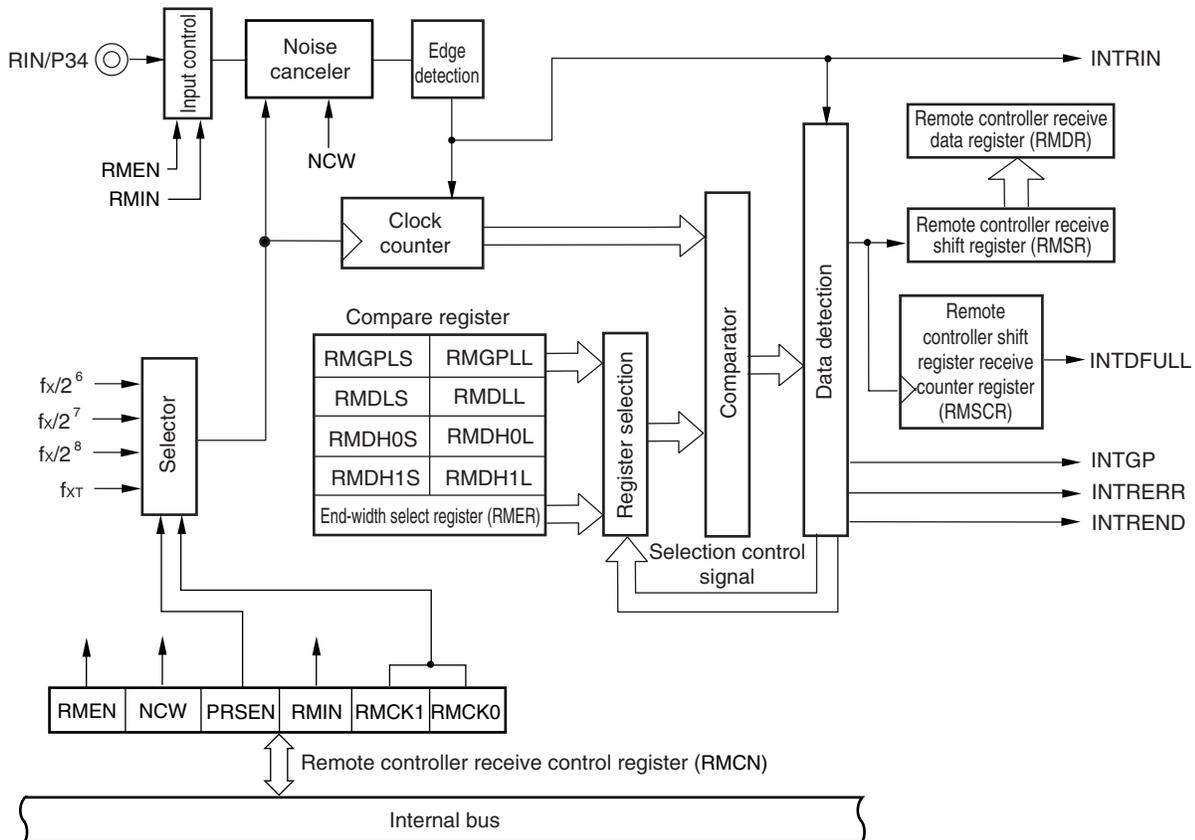
5.8 Serial Interface 20

Serial interface 20 has the following three modes.

- Operation stop mode
- Asynchronous serial interface (UART) mode
- 3-wire serial I/O mode

(1) Operation stop mode

This mode is used when serial transfers will not be performed. It enables a reduction in power consumption.

(2) Asynchronous serial interface (UART) mode

This mode, which is used to transmit and receive the one byte of data that follows a start bit, enables full-duplex communication.

Serial interface 20 contains a dedicated UART baud rate generator, enabling communication over a wide range of baud rates. It is also possible to define baud rates by dividing the frequency of the input clock pulse at the ASCK20 pin.

(3) 3-wire serial I/O mode (MSB/LSB-first switching possible)

This mode is used to transfer 8-bit data using three lines: a serial clock line ($\overline{\text{SCK20}}$) and two serial data lines (SI20 and SO20).

Because this mode supports simultaneous transmission and reception, 3-wire serial I/O mode requires less processing time for data transfer.

Also, when using 3-wire serial I/O mode, it is possible to select whether 8-bit data transfer will start with the MSB or LSB, so any device can be connected regardless of whether that device is designed for MSB-first or LSB-first transfers.

3-wire serial I/O mode is useful for connecting peripheral I/O circuits and display controllers with conventional clocked serial interfaces, such as those found in the 75XL Series, 78K Series, and 17K Series.

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* **Figure 5-12. Block Diagram of Serial Interface**

Internal bus

Serial operating mode register 20 (CSIM20)

Asynchronous serial interface status register 20 (ASIS20)

Asynchronous serial interface mode register 20 (ASIM20)

| CSIE20 | DAP20 | DIR20 | CSCK20 | CKP20 |

Receive buffer register 20 (RXB20)

| PE20 | FE20 | OVE20 |

| TXE20 | RXE20 | PS201 | PS200 | CL20 | SL20 |

Switch of the first bit

Transmit shift register 20 (TXS20)

Transmit shift clock

SI20/P22 /RxD20

Receive shift register 20 (RXS20)

Receive shift clock

Selector — CSIE20

Port mode register (PM21)

Data phase control — DAP20

SO20/P21 /TxD20

Parity operation

Addition of stop bit

Transmit data counter

4

INTST20

Parity detection

Detection of stop bit

Receive data counter

SL20, CL20, PS200, PS201

INTSR20/INTCSI20

Reception enable

Receive clock

Transmit/receive clock control

Baud rate generator**Note**

CSIE20

CSCK20

Detection of start bit

Detection clock

Receive detection

fx/2 to fx/2⁸

4

| TPS203 | TPS202 | TPS201 | TPS200 |

CSIE20

Clock phase control

CSCK20

Internal clock output

Baud rate generator control register 20 (BRGC20)

SCK20/P20 /ASCK20

External clock output

Internal bus

Note   See **Figure 5-13** for the configuration of the baud rate generator.

Figure 5-13. Block Diagram of Baud Rate Generator 20
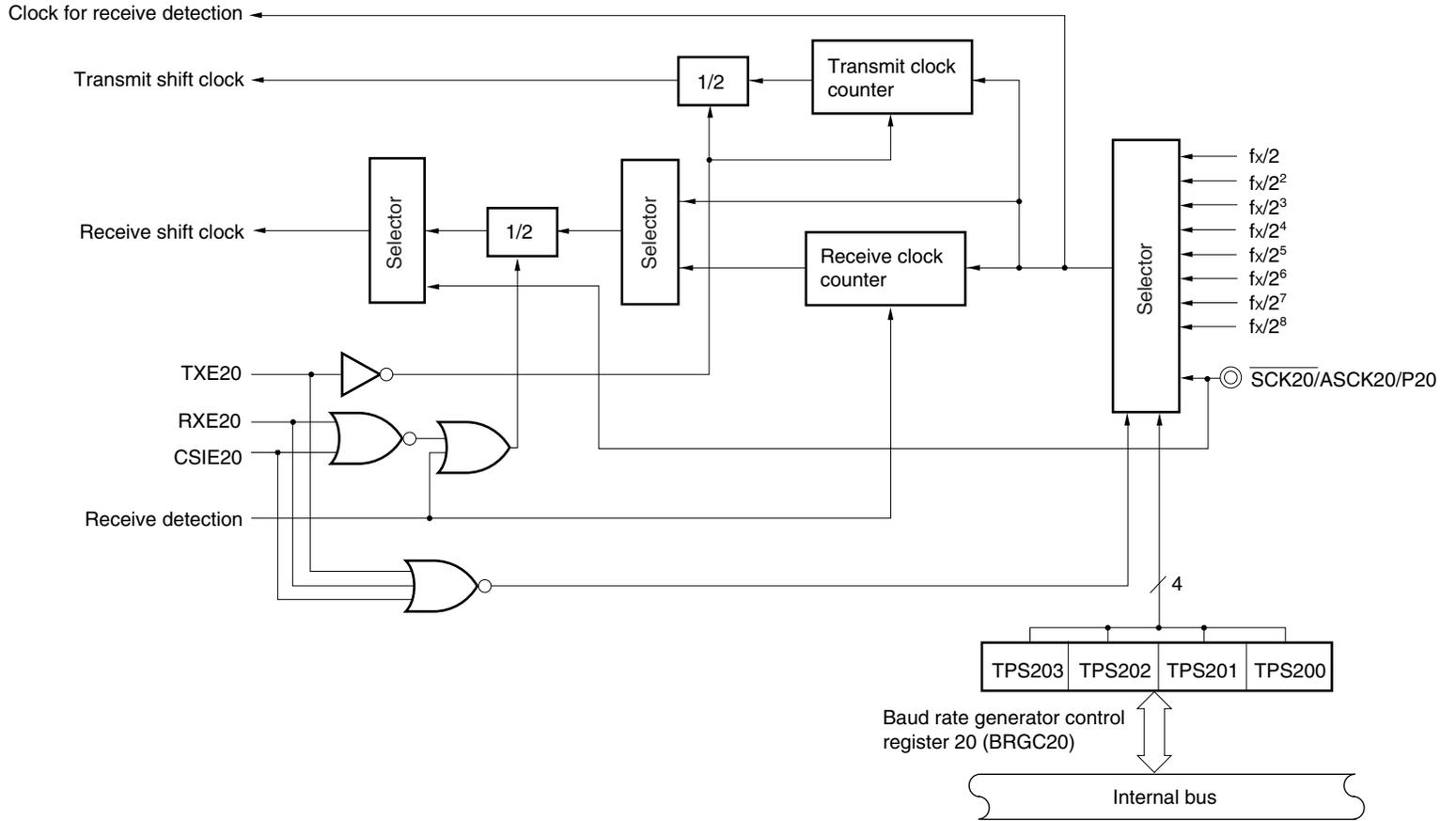
5.9 Serial Interface 1A0

Serial interface 1A0 has the following three modes.

- Operation stop mode
- 3-wire serial I/O mode
- 3-wire serial I/O mode with automatic transmit/receive function

(1) Operation stop mode
This mode is used when serial transfer will not be performed. It enables a reduction in power consumption.

(2) 3-wire serial I/O mode (MSB/LSB-first switchable)
This mode is used to transfer 8-bit data using three lines: a serial clock ($\overline{\text{SCK10}}$) line and two serial data lines (SI10 and SO10).

Because this mode supports simultaneous transmission and reception, 3-wire serial I/O mode requires less processing time for data transfer.

Also, when using 3-wire serial I/O mode, it is possible to select whether 8-bit data transfer will start with the MSB or LSB, so any device can be connected regardless of whether that device is designed for MSB-first or LSB-first transfers.

3-wire serial I/O mode is useful for connecting peripheral I/O circuits and display controllers with conventional clocked serial interfaces, such as those found in the 75XL Series, 78K Series, and 17K Series.

(3) 3-wire serial mode with automatic transmit/receive function
This mode has an automatic transmit/receive function in addition to the functions in **(2)** above.

The automatic transmit/receive function is used to transmit/receive data with a maximum of 16 bytes. This function enables the hardware to transmit/receive data to/from the OSD (On Screen Display) device and a device with an on-chip display controller/driver independently of the CPU, thus alleviating the software load.

Figure 5-14. Block Diagram of Serial Interface 1A0
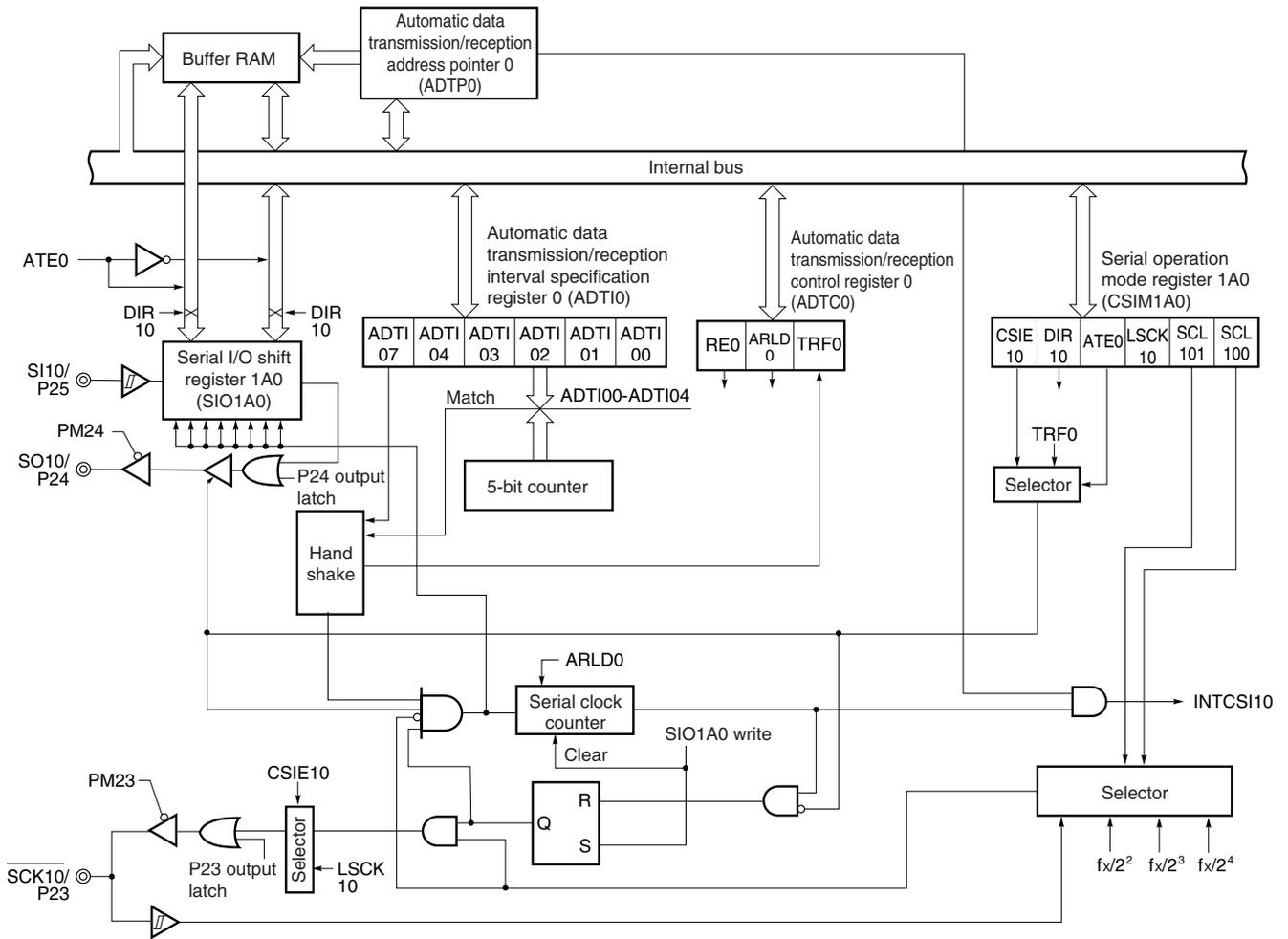
5.10 8-Bit A/D Converter

The A/D converter converts analog inputs into digital values with 8-bit resolution and is configured so as to enable control of 8 channels of analog inputs (ANI0 to ANI7).

An A/D conversion operation can only be started via software.

A/D conversion is repeated, with an interrupt request (INTAD0) generated at the completion of each A/D conversion operation.

A conversion operation is also possible using the subsystem clock multiplied by 4 (131 kHz).

Caution   A/D conversion is stopped in the STOP mode.

Figure 5-15. 8-Bit A/D Converter Block Diagram
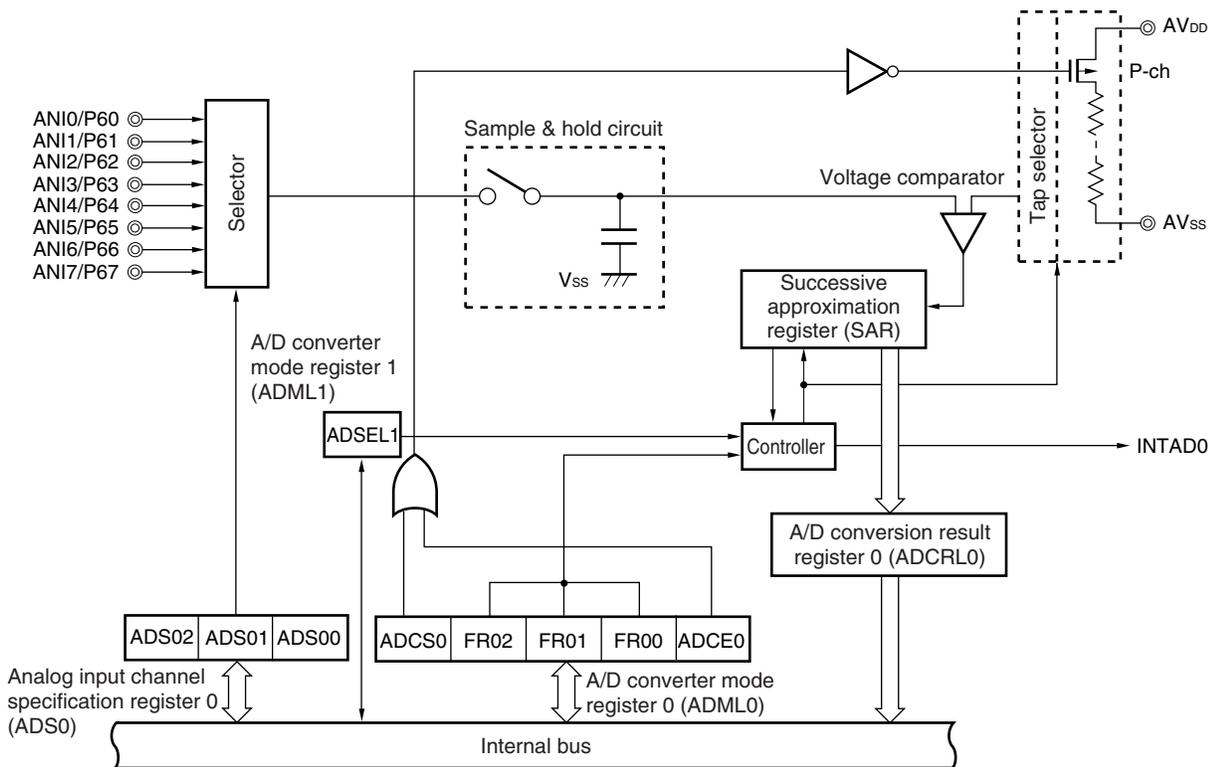
5.11 LCD Controller/Driver

The LCD controller/driver incorporated in the μPD78F9478 has the following features.

(1) Segment and common signals based on the automatic reading of the display data memory can be automatically output
(2) Two types of display modes are selectable
    • 1/3 duty (1/3 bias)
    • 1/4 duty (1/3 bias)
(3) Four types of frame frequencies are selectable in each display mode
(4) 16 to 28 segment signal outputs (S0 to S15, S16 to S27 (usable by a port function register)), 4 common signal outputs (COM0 to COM3)
(5) Operation with a subsystem clock is possible

Figure 5-16. LCD Controller/Driver Block Diagram

Internal bus

LCD clock control register 0 (LCDC0)

| LCDC03 | LCDC02 | LCDC01 | LCDC00 |

LCD display mode register 0 (LCDM0)

| LCDON0 | LIPS0 | LCDM0 |

Display data memory

FA00H 7 6 5 4 3 2 1 0 .... FA0FH 7 6 5 4 3 2 1 0 .... FA10H 7 6 5 4 3 2 1 0 .... FA1BH 7 6 5 4 3 2 1 0

$f_x/2^5$
$f_x/2^6$
$f_x/2^7$
f_{XT}

Selector

f_{LCD}

Prescaler

$\dfrac{f_{LCD}}{2^6}$ $\dfrac{f_{LCD}}{2^7}$ $\dfrac{f_{LCD}}{2^8}$ $\dfrac{f_{LCD}}{2^9}$

LCD clock selector

LCDCL

Timing controller

3 2 1 0 Selector

LCDON0

Segment driver

LCD drive voltage controller

Common driver

V_{LC2} V_{LC1} V_{LC0}

COM0 COM1 COM2 COM3

S0 .... S15

S16 .... S27

Selected by port function register

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5.12 Multiplier

The calculation of 8 bits $\times$ 8 bits = 16 bits can be made by the multiplier.

Figure 5-17. Multiplier Block Diagram
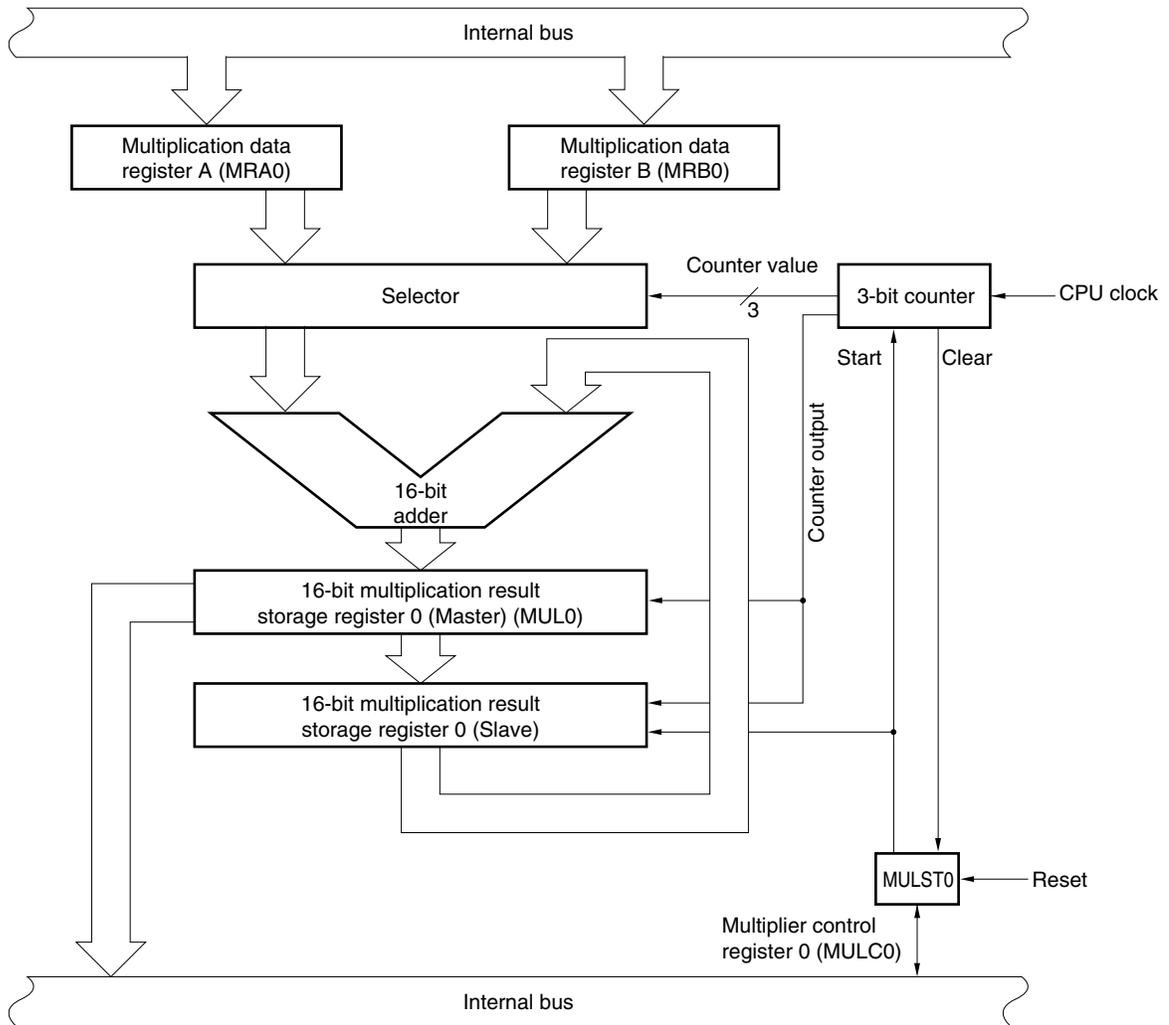
5.13 Key Return Detector

This circuit detects the key return signal (rising edge of port 0).

Figure 5-18. Block Diagram of Falling Edge Detector
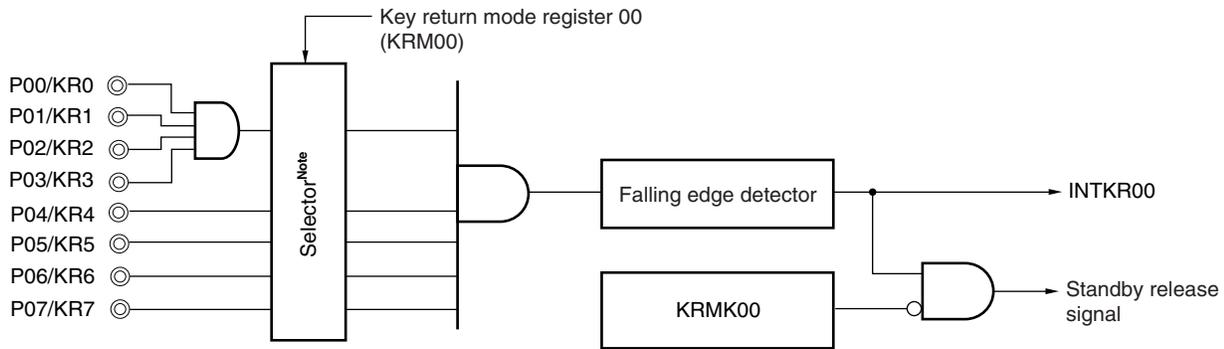
Note   For selecting the pin to be used as the falling edge input.

6. INTERRUPT FUNCTION

6.1 Interrupt Types

Two types of interrupts are supported.

(1) Non-maskable interrupts

Non-maskable interrupt requests are acknowledged unconditionally, i.e. even when interrupts are disabled.
These interrupts take precedence over all other interrupts and are not subject to interrupt priority control.
A non-maskable interrupt causes the generation of the standby release signal.
An interrupt from the watchdog timer is the only non-maskable interrupt source supported in the μPD78F9478.

(2) Maskable interrupts

Maskable interrupts are subject to mask control. If two or more maskable interrupts occur simultaneously, the default priority listed in Table 6-1 applies.
A maskable interrupt causes the generation of the standby release signal.
Maskable interrupts from 5 external and 16 internal sources are supported in the μPD78F9478.

6.2 Interrupt Sources and Configuration

The μPD78F9478 supports a total of 22 maskable and non-maskable interrupt sources (see **Table 6-1**).

Table 6-1. Interrupt Sources

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	–	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			(B)
	1	INTP0	Pin (INTP0) input edge detection	External	0006H	(C)
	2	INTP1	Pin (INTP1) input edge detection		0008H	
	3	INTP2	Pin (INTP2) input edge detection		000AH	
	4	INTP3	Pin (INTP3) input edge detection		000CH	
	5	INTRIN	Remote controller edge detection	Internal	000EH	(B)
	6	INTSR20	UART reception completion		0010H	
		INTCSI20	End of 3-wire SIO transfer for serial interface 20			
	7	INTCSI10	End of 3-wire SIO transfer for serial interface 1A0		0012H	
	8	INTST20	End of UART transmission for serial interface 20		0014H	
	9	INTWTI	Standard time interval signal of watch timer (WT)		0016H	
	10	INTTM20	Match between TM20 and CR20		0018H	
	11	INTTM50	Match between TM50 and CR50		001AH	
	12	INTTM60	Match between TM60 and CR60 (in 8-bit counter mode), and between TM50, TM60 and CR50, CR60 (in 16-bit timer mode)		001CH	
	13	INTTM61	Match between TM61 and CR61		001EH	
	14	INTAD0	End of A/D conversion		0020H	
	15	INTWT	Watch timer (WT) overflow		0022H	
	16	INTKR00	Key return signal detection	External	0024H	(C)
	17	INTRERR	Generation of reception error for remote controller	Internal	0026H	(B)
	18	INTGP	Guide pulse detection for remote controller		0028H	
	19	INTREND	Data reception completion for remote controller		002AH	
	20	INTDFULL	Read request of 8-bit shift data for remote controller		002CH	

Notes 1. The default priority is the priority order when more than one maskable interrupt request is generated at the same time. 0 is the highest priority and 20 is the lowest.

2. Basic configuration types (A), (B), and (C) correspond to (A), (B), and (C) in **Figure 6-1**.

Remark Only one of the two watchdog timer interrupt (INTWDT) sources, non-maskable or maskable (internal), can be selected.
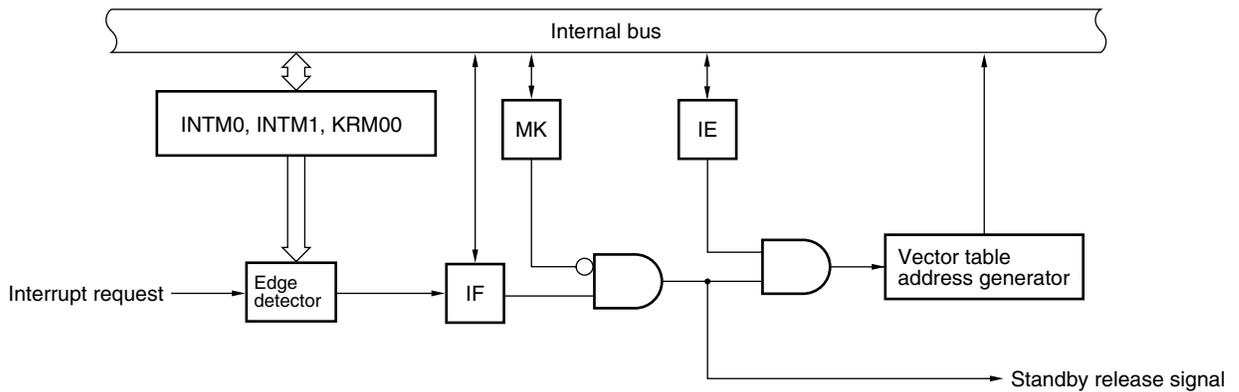
Figure 6-1. Basic Configuration of Interrupt Function

(A) Internal non-maskable interrupt

```
                                    ⎛  Internal bus   ⎞
                                    ⎝                 ⎠
                                         │
                                   ┌─────────────────┐
Interrupt request ─────────●───────│ Vector table    │
                           │       │ address generator│
                           │       └─────────────────┘
                           │
                           └───────────► Standby release signal
```

(B) Internal maskable interrupt

```
   ⎛                        Internal bus                          ⎞
   ⎝                                                              ⎠
          │        ↕             ↕                      ↑
          │      ┌────┐        ┌────┐
          │      │ MK │        │ IE │
          │      └────┘        └────┘
          │         │             │
        ┌────┐      │            ┌───┐     ┌─────────────────┐
Interrupt│ IF │─────┴──○─────────│   ├─────│ Vector table    │
request ─┤    │                  │   │     │ address generator│
        └────┘                ┌──┘   └───┐ └─────────────────┘
                              │          │
                              └──────────┴──► Standby release signal
```

(C) External maskable interrupt

```
   ⎛                            Internal bus                            ⎞
   ⎝                                                                    ⎠
              ↕                  ↑        ↕              ↕          ↑
   ┌──────────────────────┐    │      ┌────┐         ┌────┐
   │ INTM0, INTM1, KRM00   │    │      │ MK │         │ IE │
   └──────────────────────┘    │      └────┘         └────┘
              ║                 │         │              │
         ┌──────────┐        ┌────┐       │           ┌───┐   ┌─────────────────┐
Interrupt│   Edge   │        │ IF │───────┴──○────────│   ├───│ Vector table    │
request ─│ detector │────────│    │                   │   │   │ address generator│
         └──────────┘        └────┘                 ┌─┘   └──┐└─────────────────┘
                                                    │        │
                                                    └────────┴──► Standby release signal
```
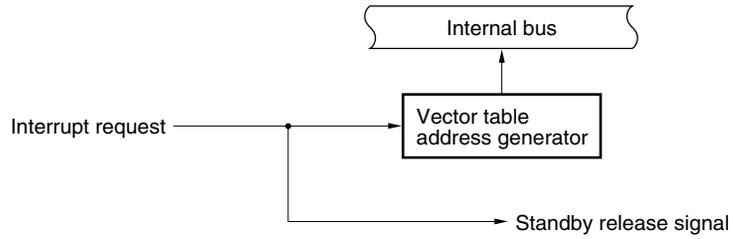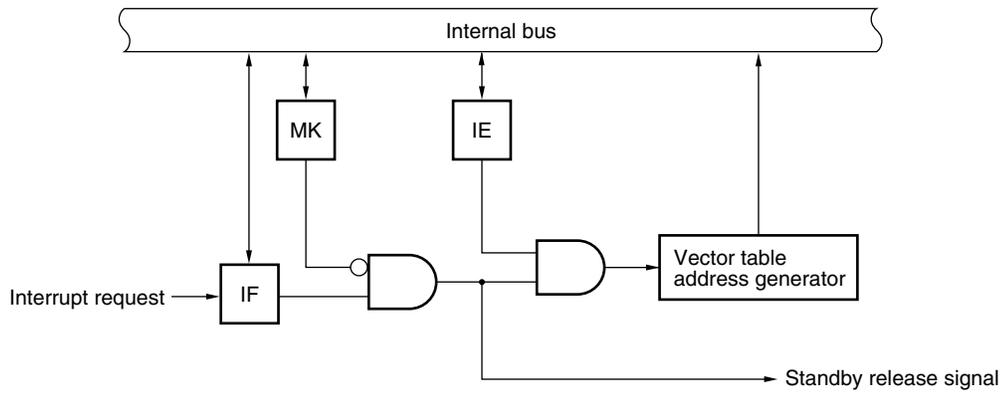
INTM0: External interrupt mode register 0

INTM1: External interrupt mode register 1

KRM00: Key return mode register 00

IF: Interrupt request flag

IE: Interrupt enable flag

MK: Interrupt mask flag

7. STANDBY FUNCTION

A standby function is incorporated to minimize the system's power consumption. There are two standby modes: HALT and STOP.

The HALT and STOP modes are selected using the HALT and STOP instructions.

(1) HALT mode

In this mode, the CPU operating clock is stopped. The average current consumption can be reduced by intermittent operation combining this mode with the normal operation mode.

(2) STOP mode

In this mode, main system clock oscillation is stopped. All operations performed with the main system clock are suspended, thus minimizing power consumption.

Cautions 1. When shifting to STOP mode, execute the STOP instruction after the peripheral hardware the operation has been stopped.

★ **2. Observe the following two constraints when using the μPD78F9478 in the HALT mode with the subclock multiplied by 4 as the CPU clock.**

- **Be sure to insert the following number of NOP instructions immediately after the HALT instruction.**

Operating Temperature	Number of NOP Instructions
$T_A = -40$ to $+45°C$	2
$T_A = -40$ to $+80°C$	3
$T_A = -40$ to $+85°C$	4

- **Save the value of the A register to the internal high-speed RAM area before the HALT instruction is executed (because the value of the A register may be changed when the HALT mode is released).**

Table 7-1. Operation Statuses in HALT Mode

Item	HALT Mode Operation Status During Main System Clock Operation		HALT Mode Operation Status During Subsystem Clock Operation	
	Subsystem Clock Operating	Subsystem Clock Stopped	Main System Clock Operating	Main System Clock Stopped
Clock generator	Oscillation enabled for both main system clock and subsystem clock, however, clock supply to CPU is stopped			
Subsystem clock ×4 multiplication circuit	Operation stopped			
CPU	Operation stopped			
Ports (output latches)	Status before HALT mode setting retained			
16-bit timer 20	Operable			Operable[Note 1]
8-bit timer 50	Operable			Operable[Note 2]
8-bit timer 60	Operable			Operable[Note 3]
8-bit timer 61	Operable			Operable[Note 3]
Watch timer	Operable	Operable[Note 4]	Operable	Operable[Note 5]
Watchdog timer	Operable		Operation stopped	
Key return circuit	Operable			
Serial interface 20	Operable			Operable[Note 6]
Serial interface 1A0	Operable			Operable[Note 6]
Remote controller reception circuit	Operable	Operable[Note 4]	Operable	Operable[Note 5]
LCD controller/driver	Operable[Note 7]	Operable[Notes 4, 7]	Operable[Note 7]	Operable[Notes 5, 7]
A/D converter	Operation stopped			
Multiplier	Operation stopped			
External interrupts	Operable[Note 8]			

★ (marker next to Remote controller reception circuit row)

Notes 1. Operation is enabled when the 24-bit counter mode is selected.
  2. Operation is enabled when either the subsystem clock or input signal from timer 60 (when timer 60 is operable) is selected as the count clock.
  3. Operation is enabled only when the external input clock is selected as the count clock.
  4. Operation is enabled when the main system clock is selected.
  5. Operation is enabled when the subsystem clock is selected.
  6. Operation is enabled only when an external clock is selected.
  7. The HALT instruction can be set after display instruction execution.
  8. Operation is enabled only for a maskable interrupt that is not masked.

Table 7-2. Operation Statuses in STOP Mode

Item	STOP Mode Operation Status During Main System Clock Operation	
	Subsystem Clock Operating	Subsystem Clock Stopped
Main system clock	Oscillation stopped	
Subsystem clock ×4 multiplication circuit	Operation stopped	
CPU	Operation stopped	
Ports (output latches)	Status before STOP mode setting retained	
16-bit timer 20	Operation stopped	
8-bit timer 50	Operable[Note 1]	Operable[Note 2]
8-bit timer 60	Operable[Note 3]	
8-bit timer 61	Operable[Note 3]	
Watch timer	Operable[Note 4]	Operation stopped
Watchdog timer	Operation stopped	
Key return circuit	Operable	
Serial interface 20	Operable[Note 5]	
Serial interface 1A0	Operable[Note 5]	
Remote controller reception circuit	Operable[Note 4]	Operation stopped
LCD controller/driver	Operable[Note 4]	Operation stopped
A/D converter	Operation stopped	
Multiplier	Operation stopped	
External interrupts	Operable[Note 6]	

Notes 1. Operation is enabled when either the subsystem clock or input signal from timer 60 (when timer 60 is operable) is selected as the count clock.

2. Operation is enabled when input signal from timer 60 (when timer 60 is operable) is selected as the count clock.

3. Operation is enabled when the external input clock is selected as the count clock.

4. Operation is enabled when the subsystem clock is selected.

5. Operation is enabled only when an external clock is selected.

6. Operation is enabled only for a maskable interrupt that is not masked

8. RESET FUNCTION

The *μ*PD78F9478 can be reset using the following two methods.

(1) External reset signal input via $\overline{\text{RESET}}$ pin
(2) Internal reset by watchdog timer program loop time detection

Cautions   1. To use an external reset sequence, input a low-level signal to the $\overline{\text{RESET}}$ pin for at least 10 *μ*s.
2. When a reset is used to release STOP mode, the data of when STOP mode was entered is retained during the reset sequence, except for the port pins, which are in the high-impedance state.

Figure 8-1. Reset Function Block Diagram
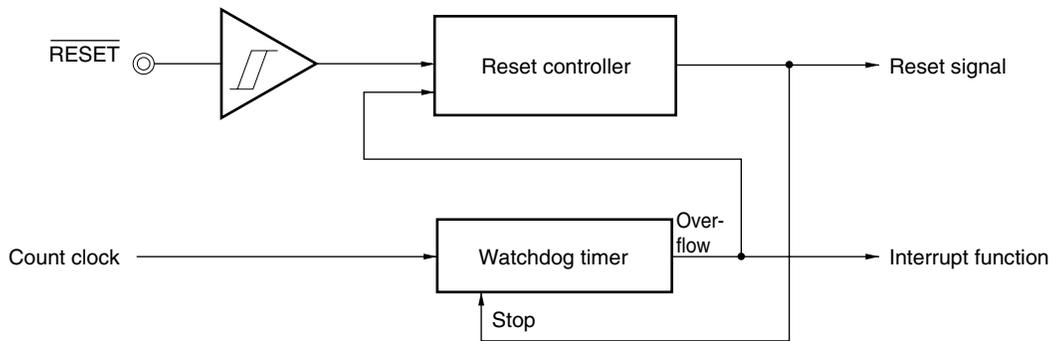
9. FLASH MEMORY PROGRAMMING

The on-chip program memory in the μPD78F9478 is a flash memory.

The flash memory can be written with the μPD78F9478 mounted on the target system (on-board). Connect the dedicated flash programmer (Flashpro III (model number: FL-PR3, PG-FP3)) to the host machine and target system to write the flash memory.

Remark   FL-PR3 is made by Naito Densei Machida Mfg. Co., Ltd.

9.1   Selecting Communication Mode

The flash memory is written by using Flashpro III and by means of serial communication. Select a communication mode from those listed in Table 9-1. To select a communication mode, the format shown in Figure 9-1 is used. Each communication mode is selected by the number of V$_{PP}$ pulses shown in Table 9-1.

Table 9-1. Communication Mode List

Communication Mode	Pins Used[Note]	Number of V$_{PP}$ Pulses
3-wire serial I/O	$\overline{SCK20}$/ASCK20/P20 SO20/TxD20/P21 SI20/RxD20/P22	0
UART	TxD20/SO20/P21 RxD20/SI20/P22	8

★   **Note**   When flash memory programming mode is set, all pins not used for flash memory programming enter the same state as that immediately after a reset. Therefore, when the external device connected to a port cannot recognize that state of the port immediately after a reset, the pins must be connected to the V$_{DD}$ pin, or via a resistor to the V$_{SS}$ pin.

Caution   **Be sure to select a communication mode depending on the V$_{PP}$ pulse number shown in Table 9-1.**

Figure 9-1. Communication Mode Selection Format
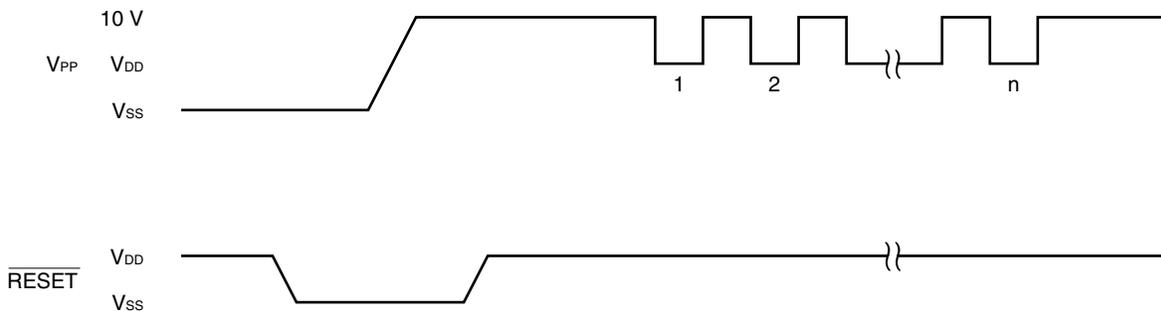
9.2 Function of Flash Memory Programming

By transmitting/receiving commands and data in the selected communication mode, operations such as writing to the flash memory are performed. Table 9-2 shows the major functions of flash memory programming.

Table 9-2. Functions of Flash Memory Programming

Function	Description
Batch erase	Erases all contents of memory
Batch blank check	Checks erased state of entire memory
Data write	Write to flash memory based on write start address and number of data written (number of bytes)
Batch verify	Compares all contents of memory with input data

9.3 Flashpro III Connection

How the Flashpro III is connected to the μPD78F9478 differs depending on the communication mode (3-wire serial I/O or UART). Figures 9-2 and 9-3 show the connection in the respective mode.

★

Figure 9-2. Flashpro III Connection in 3-Wire Serial I/O Mode
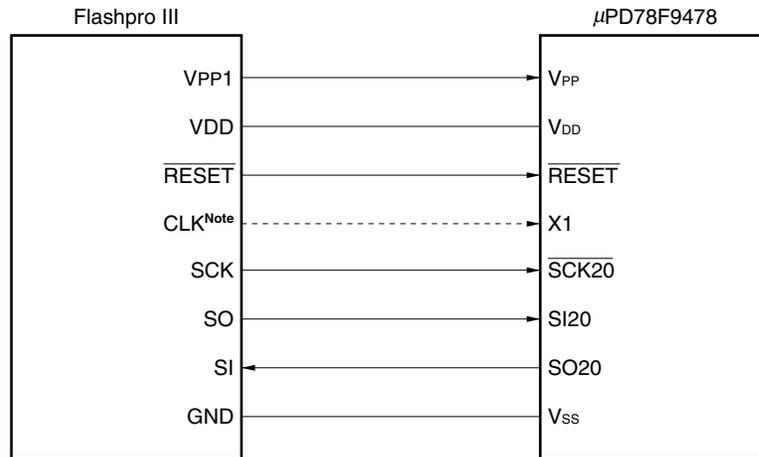
Note Connect the CLK pin when the system clock is input from the Flashpro III. When the resonator has already been connected to the X1 pin, there is no need to connect the CLK pin to the X1 pin.

Caution Be sure to connect the V_{DD} pin to the VDD pin of the Flashpro III even if the power supply has already been connected. When using the power supply, be sure to supply voltage before starting programming.

★   **Figure 9-3. Flashpro III Connection in UART Mode**
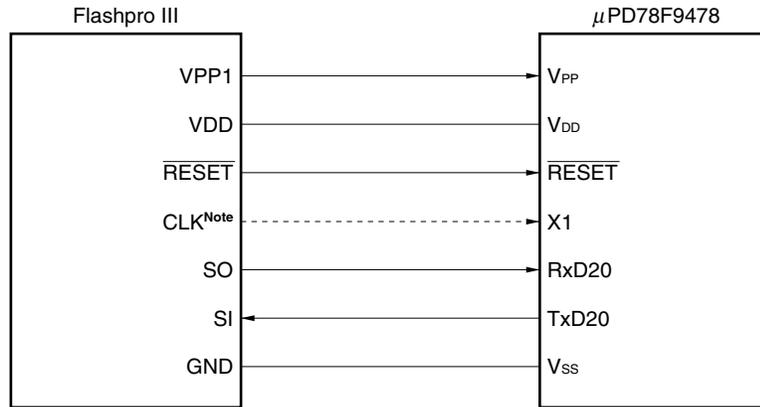
Flashpro III μPD78F9478

VPP1	V$_{PP}$
VDD	V$_{DD}$
$\overline{RESET}$	$\overline{RESET}$
CLK**Note**	X1
SO	RxD20
SI	TxD20
GND	V$_{SS}$

Note   Connect the CLK pin when the system clock is input from the Flashpro III. When the resonator has already been connected to the X1 pin, there is no need to connect the CLK pin to the X1 pin.

Caution Be sure to connect the V$_{DD}$ pin to the VDD pin of the Flashpro III even if the power supply has already been connected. When using the power supply, be sure to supply voltage before starting programming.

9.4   Example of Settings for Flashpro III (PG-FP3)

Set as follows when writing to flash memory using the Flashpro III (PG-FP3).

<1>   Download the parameter file.
<2>   Select the serial mode and the serial clock using the type command.
<3>   The following is a setting example using the PG-FP3.

Table 9-3. Example Using PG-FP3

Communication Mode	Setting Example Using PG-FP3		Number of V$_{PP}$ Pulses[Note1]
3-wire serial I/O mode	COMM PORT	SIO-ch 0	0
	CPU CLK	On target board	
		In Flashpro	
	On target board	4.1943 MHz	
	SIO CLK	1.0 MHz	
	In Flashpro	4.0 MHz	
	SIO CLK	1.0 MHz	
UART	COMM PORT	UART-ch0	8
	CPU CLK	On target board	
		In Flashpro	
	On target board	4.91 MHz	
	UART BPS	9600 bps [Note2]	

Notes 1.   The number of V$_{PP}$ pulses supplied from the Flashpro III during serial communication initialization. The
pins to be used in communication are determined by this number of pulses.
2.   Select one of 9600 bps, 19200 bps, 38400 bps, or 76800 bps.

Remark   COMM PORT: Selection of serial port
SIO CLK: Selection of serial clock frequency
CPU CLK: Selection of CPU clock source to be input

10. INSTRUCTION SET OVERVIEW

The instruction set for the µPD78F9478 is listed in this section.

10.1 Conventions

10.1.1 Operand formats and descriptions

The description made in the operand field of each instruction conforms to the operand format for the instructions listed below (for details, see the assembler specifications). If more than one operand format is listed for an instruction, one is selected. Uppercase letters, #, !, $, and brackets [ ] are used to specify keywords, which must be written exactly as they appear. The meanings of these special characters are as follows.

- #: Immediate data specification
- $: Relative address specification
- !: Absolute address specification
- [ ]: Indirect address specification

Immediate data should be described using appropriate values or labels. The specification of values and labels must be accompanied by #, !, $, or [ ].

Operand registers, expressed as r or rp in the formats, can be described using both functional names (X, A, C, etc.) and absolute names (R0, R1, R2, and other names listed in Table 5-1 below).

Table 10-1. Operand Formats and Descriptions

Format	Description
r rp sfr	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7) AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special function register symbol
saddr saddrp	FE20H to FF1FH Immediate data or label FE20H to FF1FH Immediate data or label (even addresses only)
addr16 addr5	0000H to FFFFH Immediate data or label (only even addresses for 16-bit data transfer instructions) 0040H to 007FH Immediate data or label (even addresses only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label

10.1.2 Operation field definitions

A: A register (8-bit accumulator)

X: X register

B: B register

C: C register

D: D register

E: E register

H: H register

L: L register

AX: AX register pair (16-bit accumulator)

BC: BC register pair

DE: DE register pair

HL: HL register pair

PC: Program counter

SP: Stack pointer

PSW: Program status word

CY: Carry flag

AC: Auxiliary carry flag

Z: Zero flag

IE: Interrupt request enable flag

NMIS: Flag to indicate that a non-maskable interrupt is being processed

():   Contents of a memory location indicated by a parenthesized address or register name

X_H, X_L: Higher and lower 8 bits of a 16-bit register

$\wedge$:   Logical product (AND)

$\vee$:   Logical sum (OR)

$\veebar$:   Exclusive OR

‾:   Inverted data

addr16: 16-bit immediate data or label

jdisp8: Signed 8-bit data (displacement value)

10.1.3 Flag operation field definitions

(Blank): No change

0:      Clear to 0

1:      Set to 1

$\times$:   Set or clear according to the result

R: Restore to the previous value

10.2 Operations

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
MOV	r, #byte	3	6	r ← byte			
	saddr , #byte	3	6	(saddr) ← byte			
	sfr, #byte	3	6	sfr ← byte			
	A, r Note 1	2	4	A ← r			
	r, A Note 1	2	4	r ← A			
	A, saddr	2	4	A ← (saddr)			
	saddr, A	2	4	(saddr) ← A			
	A, sfr	2	4	A ← sfr			
	sfr, A	2	4	sfr ← A			
	A, !addr16	3	8	A ← (addr16)			
	!addr16, A	3	8	(addr16) ← A			
	PSW, #byte	3	6	PSW ← byte	×	×	×
	A, PSW	2	4	A ← PSW			
	PSW, A	2	4	PSW ← A	×	×	×
	A, [DE]	1	6	A ← (DE)			
	[DE], A	1	6	(DE) ← A			
	A, [HL]	1	6	A ← (HL)			
	[HL], A	1	6	(HL) ← A			
	A, [HL + byte]	2	6	A ← (HL + byte)			
	[HL + byte], A	2	6	(HL + byte) ← A			
XCH	A, X	1	4	A ↔ X			
	A, r Note 2	2	6	A ↔ r			
	A, saddr	2	6	A ↔ (saddr)			
	A, sfr	2	6	A ↔ (sfr)			
	A, [DE]	1	8	A ↔ (DE)			
	A, [HL]	1	8	A ↔ (HL)			
	A, [HL + byte]	2	8	A ↔ (HL + byte)			
MOVW	rp, #word	3	6	rp ← word			
	AX, saddrp	2	6	AX ← (saddrp)			
	saddrp, AX	2	8	(saddrp) ← AX			
	AX, rp Note 3	1	4	AX ← rp			
	rp, AX Note 3	1	4	rp ← AX			
XCHW	AX, rp Note 3	1	8	AX ↔ rp			

Notes 1. Except when r = A.

2. Except when r = A or X.

3. Only when rp = BC, DE, or HL.

Remark The instruction clock cycle is based on the CPU clock (f_{CPU}) specified by the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16) + CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A − byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) − byte	×	×	×
	A, r	2	4	A, CY ← A − r	×	×	×
	A, saddr	2	4	A, CY ← A − (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A − (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A − (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A − (HL + byte)	×	×	×
SUBC	A, #byte	2	4	A, CY ← A − byte − CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) − byte − CY	×	×	×
	A, r	2	4	A, CY ← A − r − CY	×	×	×
	A, saddr	2	4	A, CY ← A − (saddr) − CY	×	×	×
	A, !addr16	3	8	A, CY ← A − (addr16) − CY	×	×	×
	A, [HL]	1	6	A, CY ← A − (HL) − CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A − (HL + byte) − CY	×	×	×
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	×		

Remark The instruction clock cycle is based on the CPU clock (f$_{CPU}$) specified by the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
OR	A, #byte	2	4	A ← A ∨ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∨ byte	×		
	A, r	2	4	A ← A ∨ r	×		
	A, saddr	2	4	A ← A ∨ (saddr)	×		
	A, !addr16	3	8	A ← A ∨ (addr16)	×		
	A, [HL]	1	6	A ← A ∨ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∨ (HL + byte)	×		
XOR	A, #byte	2	4	A ← A ∀ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∀ byte	×		
	A, r	2	4	A ← A ∀ r	×		
	A, saddr	2	4	A ← A ∀ (saddr)	×		
	A, !addr16	3	8	A ← A ∀ (addr16)	×		
	A, [HL]	1	6	A ← A ∀ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∀ (HL + byte)	×		
CMP	A, #byte	2	4	A − byte	×	×	×
	saddr, #byte	3	6	(saddr) − byte	×	×	×
	A, r	2	4	A − r	×	×	×
	A, saddr	2	4	A − (saddr)	×	×	×
	A, !addr16	3	8	A − (addr16)	×	×	×
	A, [HL]	1	6	A − (HL)	×	×	×
	A, [HL + byte]	2	6	A − (HL + byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY ← AX + word	×	×	×
SUBW	AX, #word	3	6	AX, CY ← AX − word	×	×	×
CMPW	AX, #word	3	6	AX − word	×	×	×
INC	r	2	4	r ← r + 1	×	×	
	saddr	2	4	(saddr) ← (saddr) + 1	×	×	
DEC	r	2	4	r ← r − 1	×	×	
	saddr	2	4	(saddr) ← (saddr) − 1	×	×	
INCW	rp	1	4	rp ← rp + 1			
DECW	rp	1	4	rp ← rp − 1			
ROR	A, 1	1	2	(CY, $A_7 ← A_0$, $A_{m−1} ← A_m$) × 1			×
ROL	A, 1	1	2	(CY, $A_0 ← A_7$, $A_{m+1} ← A_m$) × 1			×
RORC	A, 1	1	2	(CY ← A_0, A_7 ← CY, $A_{m−1} ← A_m$) × 1			×
ROLC	A, 1	1	2	(CY ← A_7, A_0 ← CY, $A_{m+1} ← A_m$) × 1			×

Remark The instruction clock cycle is based on the CPU clock (fCPU) specified by the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Z	AC	CY
SET1	saddr.bit	3	6	(saddr.bit) ← 1			
	sfr.bit	3	6	sfr.bit ← 1			
	A.bit	2	4	A.bit ← 1			
	PSW.bit	3	6	PSW bit ← 1	×	×	×
	[HL].bit	2	10	(HL).bit ← 1			
CLR1	saddr.bit	3	6	(saddr.bit) ← 0			
	sfr.bit	3	6	sfr.bit ← 0			
	A.bit	2	4	A.bit ← 0			
	PSW.bit	3	6	PSW.bit ← 0	×	×	×
	[HL].bit	2	10	(HL).bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{\text{CY}}$			×
CALL	!addr16	3	6	(SP − 1) ← (PC + 3)$_H$, (SP − 2) ← (PC + 3)$_L$, PC ← addr16, SP ← SP − 2			
CALLT	[addr5]	1	8	(SP − 1) ← (PC + 1)$_H$, (SP − 2) ← (PC + 1)$_L$, PC$_H$ ← (00000000, addr5 + 1), PC$_L$ ← (00000000, addr5), SP ← SP − 2			
RET		1	6	PC$_H$ ← (SP + 1), PC$_L$ ← (SP), SP ← SP + 2			
RETI		1	8	PC$_H$ ← (SP + 1), PC$_L$ ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R	R	R
PUSH	PSW	1	2	(SP − 1) ← PSW, SP ← SP − 1			
	rp	1	4	(SP − 1) ← rp$_H$, (SP − 2) ← rp$_L$, SP ← SP − 2			
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R	R	R
	rp	1	6	rp$_H$ ← (SP + 1), rp$_L$ ← (SP), SP ← SP + 2			
MOVW	SP, AX	2	8	SP ← AX			
	AX, SP	2	6	AX ← SP			
BR	!addr16	3	6	PC ← addr16			
	$addr16	2	6	PC ← PC + 2 + jdisp8			
	AX	1	6	PC$_H$ ← A, PC$_L$ ← X			

Remark The instruction clock cycle is based on the CPU clock (f$_{CPU}$) specified by the processor clock control register (PCC).

| Mnemonic | Operand | Byte | Clock | Operation | Flag |
					Z AC CY
BC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 1	
BNC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 0	
BZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 1	
BNZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 0	
BT	saddr.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr.bit) = 1	
	sfr.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr.bit = 1	
	A.bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A.bit = 1	
	PSW.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW.bit = 1	
BF	saddr.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr.bit) = 0	
	sfr.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr.bit = 0	
	A.bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A.bit = 0	
	PSW.bit, $addr16	4	10	PC ← PC + 4 + disp8 if PSW.bit = 0	
DBNZ	B, $addr16	2	6	B ← B − 1, then PC ← PC + 2 + jdisp8 if B ≠ 0	
	C, $addr16	2	6	C ← C − 1, then PC ← PC + 2 + jdisp8 if C ≠ 0	
	saddr, $addr16	3	8	(saddr) ← (saddr) − 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0	
NOP		1	2	No Operation	
EI		3	6	IE ← 1 (Enable Interrupt)	
DI		3	6	IE ← 0 (Disable Interrupt)	
HALT		1	2	Set HALT Mode	
STOP		1	2	Set STOP Mode	

Remark   The instruction clock cycle is based on the CPU clock (f_{CPU}) specified by the processor clock control register (PCC).

★ **11. ELECTRICAL SPECIFICATIONS**

Absolute Maximum Ratings (T$_A$ = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Power supply voltage	V$_{DD}$	V$_{DD}$ = AV$_{DD}$		−0.3 to +6.5	V
	AV$_{DD}$				
	V$_{PP}$			−0.3 to +10.5	V
Input voltage	V$_{I1}$	P00 to P07, P10, P11, P20 to P25, P30 to P34, P60 to P67, P70 to P73[Note 1], P80 to P87[Note 1], X1, X2, XT1, XT2, $\overline{RESET}$		−0.3 to V$_{DD}$ + 0.3[Note 2]	V
	V$_{I2}$	P50 to P53	N-ch open drain	−0.3 to +13	V
Output voltage	V$_O$	P00 to P07, P10, P11, P20 to P25, P30 to P34, P50 to P53, P80 to P87[Note 1]		−0.3 to V$_{DD}$ + 0.3[Note 2]	V
		S0 to S15, S16 to S27[Note 1], COM0 to COM3		−0.3 to V$_{LC0}$ + 0.3	V
Output current, high	I$_{OH}$	Per pin		−10	mA
		Total for all pins		−30	mA
Output current, low	I$_{OL}$	Per pin		30	mA
		Total for all pins		160	mA
Operating ambient temperature	T$_A$	In normal operation mode		−40 to +85	°C
		In flash memory programming mode		10 to 40	°C
Storage temperature	T$_{stg}$			−40 to +125	°C

Notes 1. Only when selected by a port function register
2. 6.5 V or less

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics (T$_A$ = –40 to +85°C, V$_{DD}$ = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator	V$_{SS}$ X1 X2 / C1 C2	Oscillation frequency (f$_X$)[Note 1]		1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	After V$_{DD}$ reaches oscillation voltage range MIN.			4	ms
Crystal resonator	V$_{SS}$ X1 X2 / C1 C2	Oscillation frequency(f$_X$)[Note 1]		1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	V$_{DD}$ = 4.5 to 5.5 V			10	ms
			V$_{DD}$ = 1.8 to 5.5 V			30	ms
External clock	X1 X2	X1 input frequency (f$_X$)[Note 1]		1.0		5.0	MHz
		X1 input high-/low-level width (t$_{XH}$, t$_{XL}$)		85		500	ns
	X1 X2 OPEN	X1 input frequency (f$_X$)[Note 1]	V$_{DD}$ = 2.7 to 5.5 V	1.0		5.0	MHz
		X1 input high-/low-level width (t$_{XH}$, t$_{XL}$)	V$_{DD}$ = 2.7 to 5.5 V	85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V$_{SS}$.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark For the resonator selection and oscillator constant, customers are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem Clock Oscillator Characteristics (T$_A$ = –40 to +85°C, V$_{DD}$ = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator	V$_{SS}$ XT1 XT2 R C3 C4	Oscillation frequency (f$_{XT}$)[Note 1]		32	32.768	35	kHz
		Oscillation stabilization time[Note 2]	V$_{DD}$ = 4.5 to 5.5 V		1.2	2	s
			V$_{DD}$ = 1.8 to 5.5 V			10	
External clock	XT1 XT2	XT1 input frequency (f$_{XT}$)[Note 1]		32		35	kHz
		XT1 input high-/low-level width (t$_{XTH}$, t$_{XTL}$)		14.3		15.6	μs
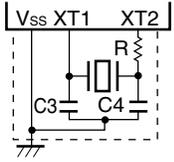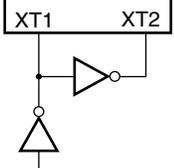
Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V$_{DD}$ reaches oscillation voltage range MIN.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V$_{SS}$.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, customers are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T$_A$ = –40 to +85°C, V$_{DD}$ = 1.8 to 5.5 V)

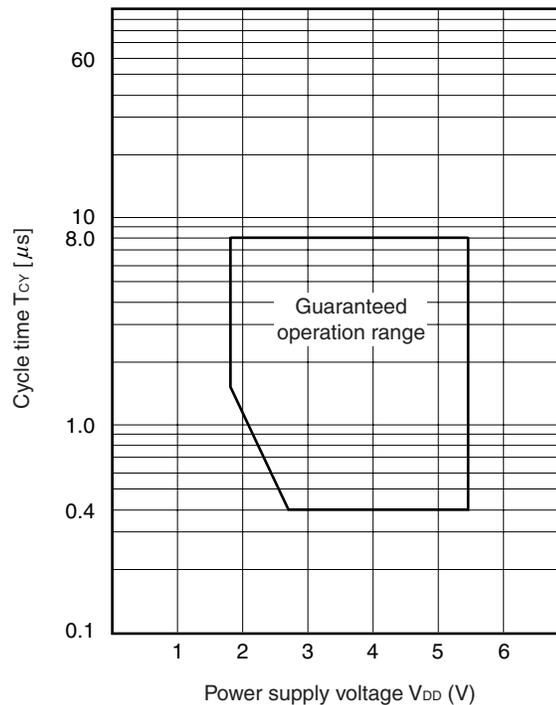| Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, low	I$_{OL}$	Per pin					10	mA
		All pins					80	mA
Output current, high	I$_{OH}$	Per pin					−1	mA
		All pins					−15	mA
Input voltage, high	V$_{IH1}$	P10, P11, P60 to P67		V$_{DD}$ = 2.7 to 5.5 V	0.7V$_{DD}$		V$_{DD}$	V
				V$_{DD}$ = 1.8 to 5.5 V	0.9V$_{DD}$		V$_{DD}$	V
	V$_{IH2}$	P50 to P53	N-ch open drain	V$_{DD}$ = 2.7 to 5.5 V	0.7V$_{DD}$		12	V
				V$_{DD}$ = 1.8 to 5.5 V	0.9V$_{DD}$		12	V
	V$_{IH3}$	$\overline{\text{RESET}}$, P00 to P07, P20 to P25, P30 to P34, P70 to P73[Note], P80 to P87[Note]		V$_{DD}$ = 2.7 to 5.5 V	0.8V$_{DD}$		V$_{DD}$	V
				V$_{DD}$ = 1.8 to 5.5 V	0.9V$_{DD}$		V$_{DD}$	V
	V$_{IH4}$	X1, X2, XT1, XT2		V$_{DD}$ = 4.5 to 5.5 V	V$_{DD}$ − 0.5		V$_{DD}$	V
				V$_{DD}$ = 1.8 to 5.5 V	V$_{DD}$ − 0.1		V$_{DD}$	V
Input voltage, low	V$_{IL1}$	P10, P11, P60 to P67		V$_{DD}$ = 2.7 to 5.5 V	0		0.3V$_{DD}$	V
				V$_{DD}$ = 1.8 to 5.5 V	0		0.1V$_{DD}$	V
	V$_{IL2}$	P50 to P53		V$_{DD}$ = 2.7 to 5.5 V	0		0.3V$_{DD}$	V
				V$_{DD}$ = 1.8 to 5.5 V	0		0.1V$_{DD}$	V
	V$_{IL3}$	$\overline{\text{RESET}}$, P00 to P07, P20 to P25, P30 to P34, P70 to P73[Note], P80 to P87[Note]		V$_{DD}$ = 2.7 to 5.5 V	0		0.2V$_{DD}$	V
				V$_{DD}$ = 1.8 to 5.5 V	0		0.1V$_{DD}$	V
	V$_{IL4}$	X1, X2, XT1, XT2		V$_{DD}$ = 4.5 to 5.5 V	0		0.4	V
				V$_{DD}$ = 1.8 to 5.5 V	0		0.1	V
Output voltage, high	V$_{OH}$			V$_{DD}$ = 4.5 to 5.5 V, I$_{OH}$ = −1 mA	V$_{DD}$ − 1.0			V
				V$_{DD}$ = 1.8 to 5.5 V, I$_{OH}$ = −100 μA	V$_{DD}$ − 0.5			V
Output voltage, low	V$_{OL1}$	P00 to P07, P10, P11, P20 to P25, P30 to P34, P80 to P87[Note]		4.5 ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL}$ = 10 mA			1.0	V
				1.8 ≤ V$_{DD}$ < 4.5 V, I$_{OL}$ = 400 μA			0.5	V
	V$_{OL2}$	P50 to P53		4.5 ≤ V$_{DD}$ < 5.5 V, I$_{OL}$ = 10 mA			1.0	V
				1.8 ≤ V$_{DD}$ < 4.5 V, I$_{OL}$ = 1.6 mA			0.4	V

Note Only when selected by a port function register

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T$_A$ = –40 to +85°C, V$_{DD}$ = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I$_{LIH1}$	V$_I$ = V$_{DD}$	P00 to P07, P10, P11, P20 to P25, P30 to P34, P60 to P67, P70 to P73[Note 1], P80 to P87[Note 1], RESET			3	μA
	I$_{LIH2}$		X1, X2, XT1, XT2			20	μA
	I$_{LIH3}$	V$_I$ = 12 V	P50 to P53 (N-ch open drain)			20	μA
Input leakage current, low	I$_{LIL1}$	V$_I$ = 0 V	P00 to P07, P10, P11, P20 to P25, P30 to P34, P60 to P67, P70 to P73[Note 1], P80 to P87[Note 1], RESET			–3	μA
	I$_{LIL2}$		X1, X2, XT1, XT2			–20	μA
	I$_{LIL3}$		P50 to P53 (N-ch open drain)			–3[Note 2]	μA
Output leakage current, high	I$_{LOH}$	V$_O$ = V$_{DD}$				3	μA
Output leakage current, low	I$_{LOL}$	V$_O$ = 0 V				–3	μA
Software pull-up resistor	R$_1$	V$_I$ = 0 V	P00 to P07, P10, P11, P20 to P25, P30 to P34	50	100	200	kΩ

Notes 1. Only when selected by a port function register

2. If P50 to P53 have been set to input mode when a read instruction is executed to read from P50 to P53, a low-level input leakage current of up to –60 μA flows during only one cycle. At all other times, the maximum leakage current is –3 μA.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}	5.0 MHz crystal oscillation operation mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10%[Note 2]		5.5	9.0	mA
			V_{DD} = 3.0 V ±10%[Note 3]		1.3	2.3	mA
			V_{DD} = 2.0 V ±10%[Note 3]		0.8	1.6	mA
	I_{DD2}	5.0 MHz crystal oscillation HALT mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10%[Note 2]		1.5	2.1	mA
			V_{DD} = 3.0 V ±10%[Note 3]		0.41	0.85	mA
			V_{DD} = 2.0 V ±10%[Note 3]		0.2	0.43	mA
	I_{DD3}	32.768 kHz crystal oscillation operation mode[Note 4] (C3 = C4 = 22 pF, R1 = 220 kΩ)	V_{DD} = 5.0 V ±10%		115	200	μA
			V_{DD} = 3.0 V ±10%		85	140	μA
			V_{DD} = 2.0 V ±10%		70	110	μA
		32.768 kHz crystal oscillation operation × 4 multiplication operation mode[Note 4] (C3 = C4 = 22 pF, R1 = 220 kΩ)	V_{DD} = 5.0 V ±10%		315	480	μA
			V_{DD} = 3.0 V ±10%		200	300	μA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode[Note 4] (C3 = C4 = 22 pF, R1 = 220 kΩ)	LCD not operating[Note 5] V_{DD} = 5.0 V ±10%		25	65	μA
			LCD not operating[Note 5] V_{DD} = 3.0 V ±10%		7	29	μA
			LCD not operating[Note 5] V_{DD} = 2.0 V ±10%		4	20	μA
			LCD operating[Note 6] V_{DD} = 5.0 V ±10%		27	71	μA
			LCD operating[Note 6] V_{DD} = 3.0 V ±10%		8.8	34	μA
			LCD operating[Note 6] V_{DD} = 2.0 V ±10%		5.6	24	μA
		32.768 kHz crystal oscillation × 4 multiplication HALT mode[Note 4] (C3 = C4 = 22 pF, R1 = 220 kΩ)	LCD not operating[Note 5] V_{DD} = 5.0 V ±10%		25	65	μA
			LCD not operating[Note 5] V_{DD} = 3.0 V ±10%		7	29	μA
			LCD operating[Note 6] V_{DD} = 5.0 V ±10%		27	71	μA
			LCD operating[Note 6] V_{DD} = 3.0 V ±10%		8.8	34	μA
	I_{DD5}	STOP mode[Note 5]	V_{DD} = 5.0 V ±10%		0.1	10	μA
			V_{DD} = 3.0 V ±10%		0.05	5	μA
			V_{DD} = 2.0 V ±10%		0.05	3	μA
	I_{DD6}	5.0 MHz crystal oscillation A/D operating mode[Note 7] (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10%[Note 2]		6.5	10.2	mA
			V_{DD} = 3.0 V ±10%[Note 3]		2.0	3.3	mA
			V_{DD} = 2.0 V ±10%[Note 3]		1.3	2.6	mA

Notes 1. The port current (including the current that flows to on-chip pull-up resistors) is not included.

2. High-speed mode operation (when the processor clock control register (PCC) is set to 00H)

3. Low-speed mode operation (when PCC is set to 02H)

4. When the main system clock is stopped

5. When the LCD is not operating (LCDON0 = 0, LIPS0 = 0)

6. Then the LCD is operating (LCDON0 = 1, LIPS0 = 1)

7. This is the total current that flows to V_{DD} and AV_{DD}.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation (T$_A$ = –40 to +85°C, V$_{DD}$ = 1.8 to 5.5 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T$_{CY}$	Operating with main system clock		V$_{DD}$ = 2.7 to 5.5 V	0.4		8.0	μs
				V$_{DD}$ = 1.8 to 5.5 V	1.6		8.0	μs
		Operating with subsystem clock	Original oscillation operation	V$_{DD}$ = 1.8 to 5.5 V	114	122	125	μs
			× 4 multiplication operation	V$_{DD}$ = 2.7 to 5.5 V	14.3	15.3	15.6	μs
Capture input high-/low-level width	t$_{CPTH}$, t$_{CPTL}$	CPT20			10			μs
TMI60, TM61 input frequency	f$_{TI}$	V$_{DD}$ = 2.7 to 5.5 V			0		4	MHz
		V$_{DD}$ = 1.8 to 5.5 V			0		275	kHz
TMI60, TM61 input high-/low-level width	t$_{TIH}$, t$_{TIL}$	V$_{DD}$ = 2.7 to 5.5 V			0.125			μs
		V$_{DD}$ = 1.8 to 5.5 V			1.8			μs
Interrupt input high-/low-level width	t$_{INTH}$, t$_{INTL}$	INTP0 to INTP3			10			μs
Key return input low-level width	t$_{KRL}$	KR0 to KR7			10			μs
$\overline{\text{RESET}}$ low-level width	t$_{RSL}$				10			μs

T$_{CY}$ vs. V$_{DD}$ (main system clock)

(2) Serial interface 20 (SIO20) (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode (internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK20}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V		$t_{KCY1}/2$–50			ns
		V_{DD} = 1.8 to 5.5 V		$t_{KCY1}/2$–150			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
		V_{DD} = 1.8 to 5.5 V		500			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

(b) 3-wire serial I/O mode (external clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK20}$ high-/low-level width	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		1600			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
		V_{DD} = 1.8 to 5.5 V		150			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

(c) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 2.7 to 5.5 V			78125	bps
		V_{DD} = 1.8 to 5.5 V			19531	bps

(d) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	800			ns
		V_{DD} = 1.8 to 5.5 V	3200			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
		V_{DD} = 1.8 to 5.5 V	1600			ns
Transfer rate		V_{DD} = 2.7 to 5.5 V			39063	bps
		V_{DD} = 1.8 to 5.5 V			9766	bps
ASCK20 rise/fall time	t_R, t_F				1	μs

(3) Serial interface 1A0 (SIO1A0) (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode, 3-wire serial I/O mode with automatic transmit/receive function (internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK10}$ cycle time	T_{KCY4}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK10}$ high-/low-level width	T_{KH4}, t_{KL4}	V_{DD} = 2.7 to 5.5 V		$T_{KCY4}/2–50$			ns
		V_{DD} = 1.8 to 5.5 V		$T_{KCY4}/2–150$			ns
SI10 setup time (to $\overline{SCK10}\uparrow$)	T_{SIK4}	V_{DD} = 2.7 to 5.5 V		150			ns
		V_{DD} = 1.8 to 5.5 V		500			ns
SI10 hold time (from $\overline{SCK10}\uparrow$)	T_{KSI4}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO10 output delay time from $\overline{SCK10}\downarrow$	T_{KSO4}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns

Note R and C are the load resistance and load capacitance of the SO10 output line.

(b) 3-wire serial I/O mode, 3-wire serial I/O mode with automatic transmit/receive function (external clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK10}$ cycle time	T_{KCY5}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK10}$ high-/low-level width	T_{KH5}, t_{KL5}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		1600			ns
SI10 setup time (to $\overline{SCK10}\uparrow$)	T_{SIK5}	V_{DD} = 2.7 to 5.5 V		100			ns
		V_{DD} = 1.8 to 5.5 V		150			ns
SI10 hold time (from $\overline{SCK10}\uparrow$)	T_{KSI5}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO10 output delay time from $\overline{SCK10}\downarrow$	T_{KSO5}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns

Note R and C are the load resistance and load capacitance of the SO10 output line.

AC Timing Measurement Points (Excluding X1 and XT1 Inputs)

0.8V$_{DD}$ Point of measurement   0.8V$_{DD}$

0.2V$_{DD}$ 0.2V$_{DD}$

Clock Timing

1/f$_X$

t$_{XL}$ t$_{XH}$

X1 input

V$_{IH4}$ (MIN.)

V$_{IL4}$ (MAX.)

1/f$_{XT}$

t$_{XTL}$ t$_{XTH}$

XT1 input

V$_{IH4}$ (MIN.)

V$_{IL4}$ (MAX.)

Capture Input Timing

t$_{CPTL}$ t$_{CPTH}$

CPT20

TMI Timing

1/f$_{TI}$

t$_{TIL}$ t$_{TIH}$

TMI60, TMI61

Interrupt Input Timing

t$_{INTL}$ t$_{INTH}$

INTP0 to INTP3
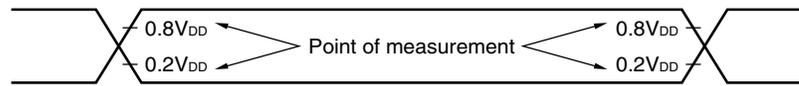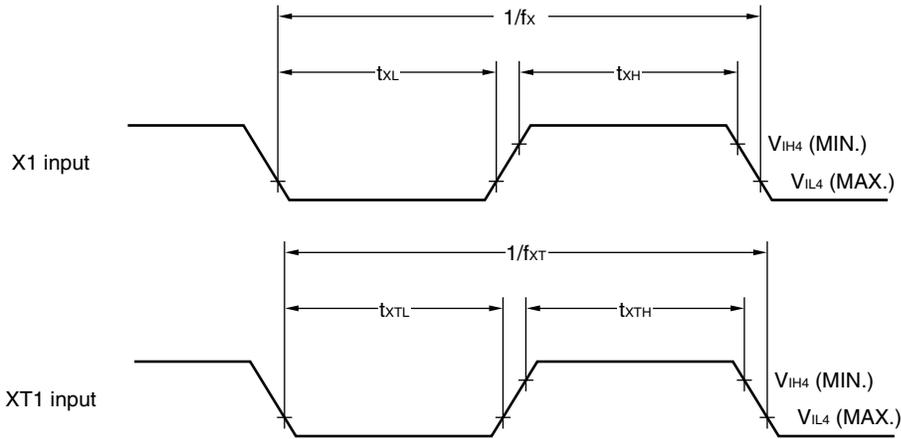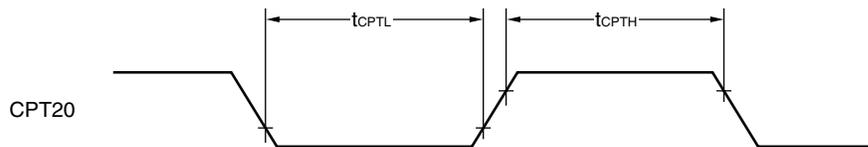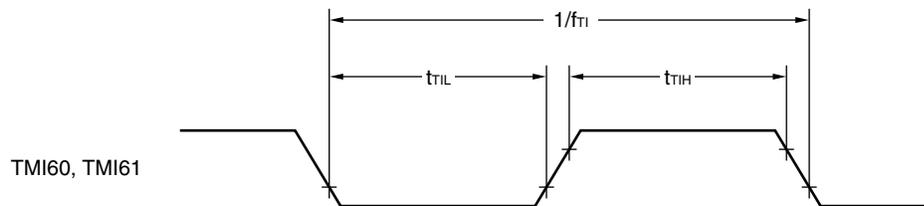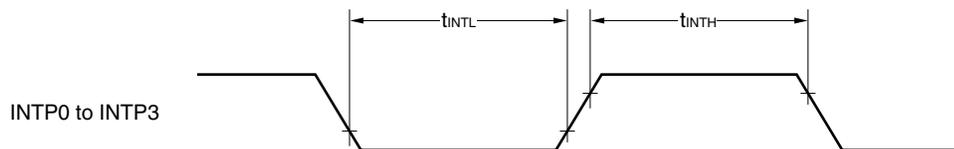
Key Return Input Timing

t$_{KRL}$

KR0 to KR7
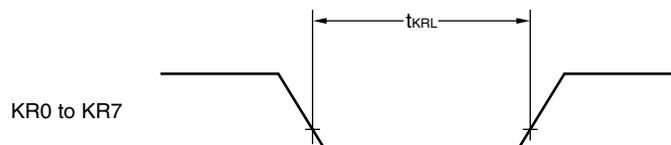
$\overline{\text{RESET}}$ Input Timing
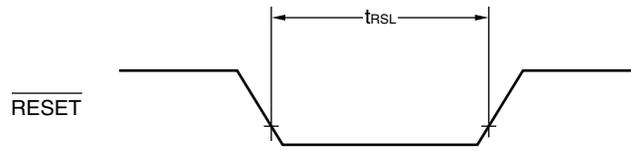
Serial Transfer Timing

3-wire serial I/O mode:
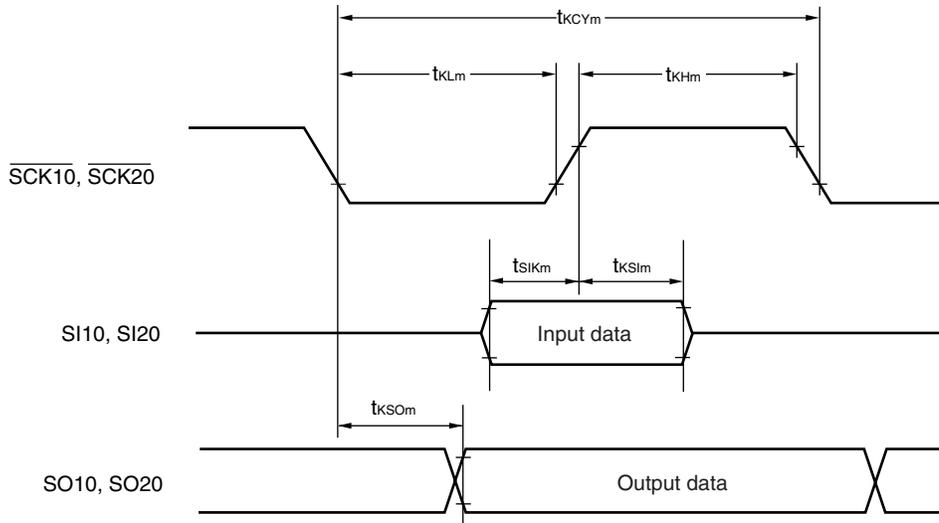
Remark   m = 1, 2, 4, 5

UART mode (external clock input):
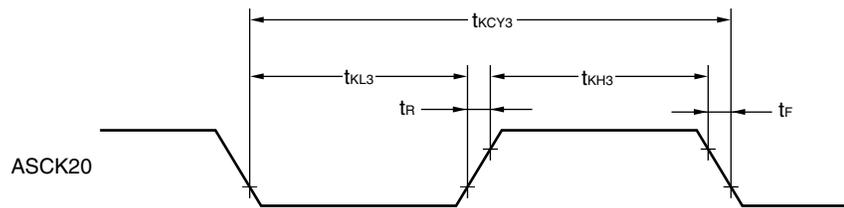
8-Bit A/D Converter Characteristics

(T_A = –40 to +85°C, 1.8 V $\leq$ AV_{DD} = V_{DD} $\leq$ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note 1]		AV_{DD} = 2.7 to 5.5 V			±0.6	%FSR
		AV_{DD} = 1.8 to 5.5 V			±1.2	%FSR
Conversion time	t_{CONV}	AV_{DD} = 2.7 to 5.5 V	14		100	μs
		AV_{DD} = 1.8 to 5.5 V	28		100	μs
		When × 4 subsystem clock is used (ADSEL1 = 1), AV_{DD} = 2.7 to 5.5 V		132[Note 2]		Clock
Analog input voltage	V_{IAN}		0		AV_{DD}	V

Notes **1.** Excludes quantization error (±0.2%)

2. Number of clocks of × 4 subsystem clock

Remark FSR: Full scale range

LCD Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}		2.7		V_{DD}	V
LCD output voltage differential[Note] (common)	V_{ODC}	I_O = ±5 μA	0		±0.2	V
LCD output voltage differential[Note] (segment)	V_{ODS}	I_O = ±1 μA	0		±0.2	V

Note The voltage differential is the difference between the segment and common signal output's actual and ideal output voltages.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T$_A$ = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V$_{DDDR}$		1.8		5.5	V
Release signal set time	t$_{SREL}$		0			*μ*s

Data Retention Timing (STOP Mode Release by $\overline{RESET}$)
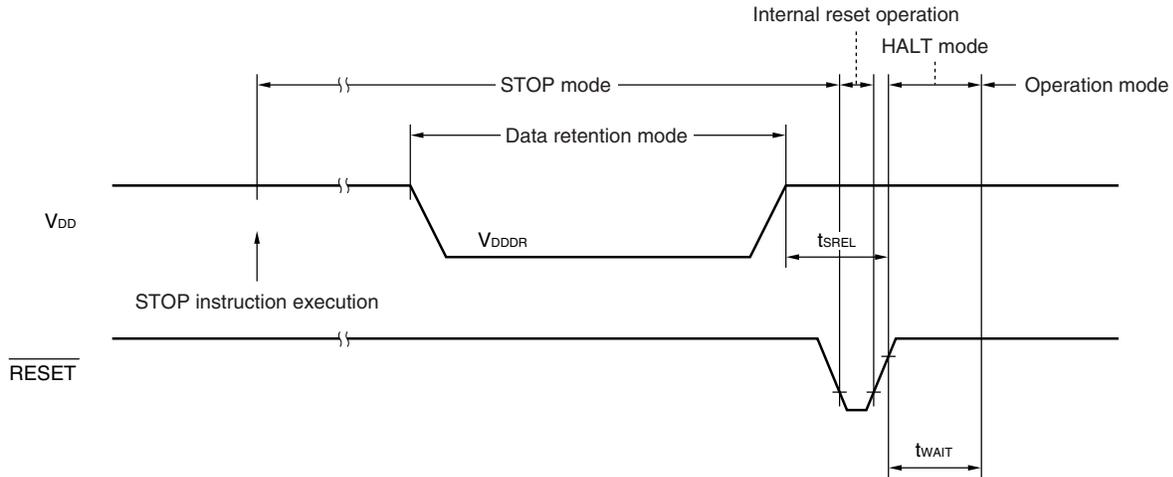
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)
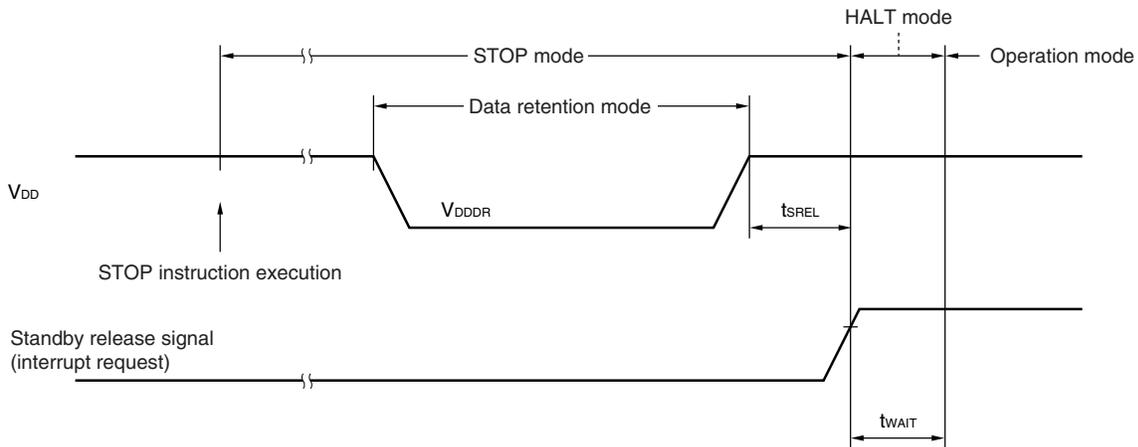
Oscillation Stabilization Wait Time (T$_A$ = –40 to +85°C, V$_{DD}$ = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation stabilization wait time[Note 1]	t$_{WAIT}$	Release by $\overline{RESET}$		2^{15}/fx		s
		Release by interrupt		**Note 2**		s

Notes 1. Use a resonator whose oscillation stabilizes within the oscillation stabilization wait time.

   2. Selection of 2^{12}/fx, 2^{15}/fx, or 2^{17}/fx is possible using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register (OSTS).

Remark fx: Main system clock oscillation frequency

Writing and Erasing Characteristics (T$_A$ = 10 to 40°C, V$_{DD}$ = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Write operation frequency	f$_X$	V$_{DD}$ = 2.7 to 5.5 V	1.0		5	MHz
		V$_{DD}$ = 1.8 to 5.5 V	1.0		1.25	MHz
Write current (V$_{DD}$ pin)[Note]	I$_{DDW}$	When V$_{PP}$ supply voltage = V$_{PP1}$ (at 5.0 MHz operation)			7	mA
Write current (V$_{PP}$ pin)[Note]	I$_{PPW}$	When V$_{PP}$ supply voltage = V$_{PP1}$			13	mA
Erase current (V$_{DD}$ pin)[Note]	I$_{DDE}$	When V$_{PP}$ supply voltage = V$_{PP1}$ (at 5.0 MHz operation)			7	mA
Erase current (V$_{PP}$ pin)[Note]	I$_{PPE}$	When V$_{PP}$ supply voltage = V$_{PP1}$			100	mA
Unit erase time	t$_{er}$		0.5	1	1	s
Total erase time	t$_{era}$				20	s
Number of rewrites		Erase and write is considered as 1 cycle			20	Times
V$_{PP}$ supply voltage	V$_{PP0}$	Normal operation	0		0.2V$_{DD}$	V
	V$_{PP1}$	Flash memory programming	9.7	10.0	10.3	V

Note Excludes current flowing through ports (including on-chip pull-up resistors)

80-PIN PLASTIC QFP (14x14)

detail of lead end
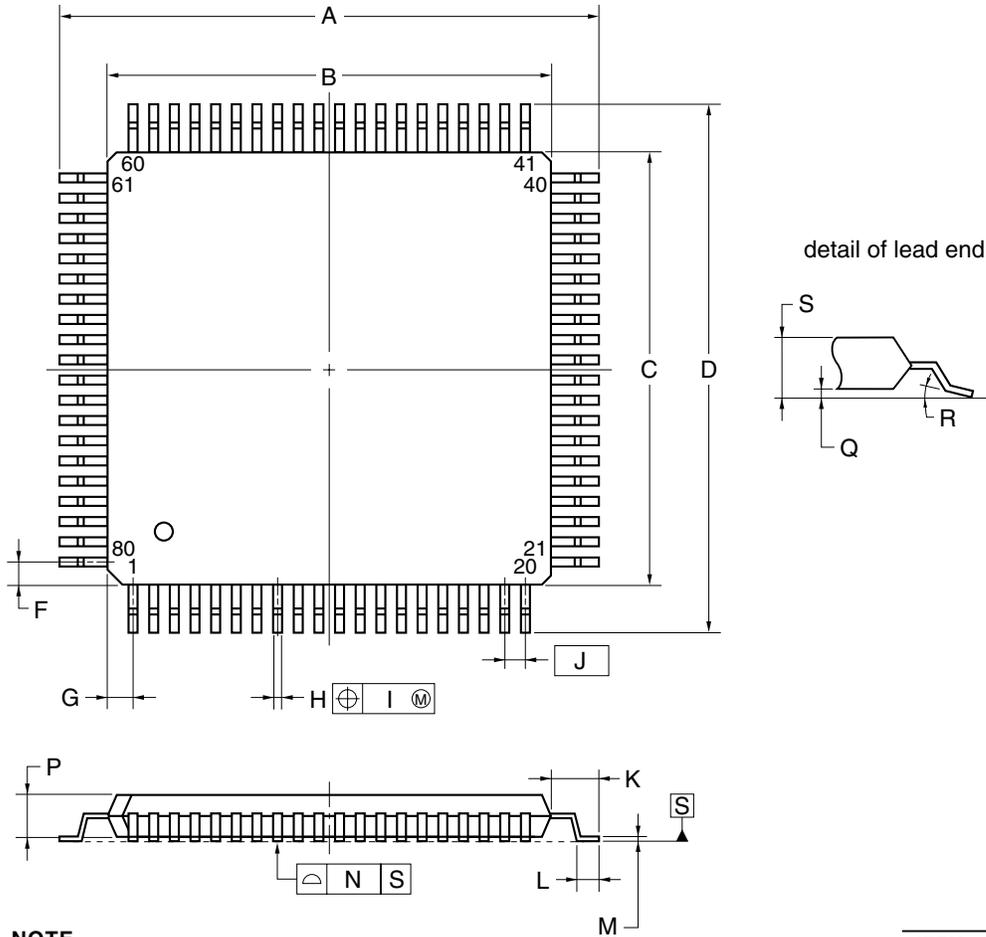
NOTE

Each lead centerline is located within 0.13 mm of
its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.20±0.20
B	14.00±0.20
C	14.00±0.20
D	17.20±0.20
F	0.825
G	0.825
H	0.32±0.06
I	0.13
J	0.65 (T.P.)
K	1.60±0.20
L	0.80±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	1.40±0.10
Q	0.125±0.075
R	$3°^{+7°}_{-3°}$
S	1.70 MAX.

P80GC-65-8BT-1

★   **13. RECOMMENDED SOLDERING CONDITIONS**

     The *μ*PD78F9478 should be soldered and mounted under the following recommended conditions.

     For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**. For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 13-1. Surface Mounting Type Soldering Conditions

*μ*PD78F9478GC-8BT: 80-pin plastic QFP (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

     Caution   Do not use different soldering methods together (except for partial heating).

★ **APPENDIX A. DIFFERENCES BETWEEN μPD78F9478 AND MASK ROM VERSIONS**

The μPD78F9478 is available as the flash memory version of the μPD789478 Subseries.

The differences between the μPD78F9478 and the mask ROM version are shown in Table A-1.

Table A-1. Differences Between μPD78F9478 and Mask ROM Version

Item		Flash Memory Version	Mask ROM Version	
		μPD78F9478	μPD789478	μPD789477
Internal memory	ROM	32 KB (flash memory)	32 KB	24 KB
	High-speed RAM	1,024 bytes		768 bytes
	LCD display RAM	28 × 4 bits		
Pin function selection S16 to S27 (LCD segment output) or P70 to P73 and P80 to P87 (general-purpose port)		Selectable by a port function register (PF7 and PF8) in bit units	Selectable by a mask option in bit units	
On-chip pull-up resistor of port 5		Not provided	Selectable by a mask option in bit units	
Availability of a circuit to multiply the subsystem clock by 4		Selectable by the subclock selection register (SSCK)	Selectable by a mask option	
IC0 pin		Not provided	Provided	
V$_{PP}$ pin		Provided	Not provided	
HALT mode when using subsystem clock multiplied by 4		Restricted. Refer to **7. STANDBY FUNCTION**.	No restriction	
Electrical specification		Refer to the data sheet of each product.		

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the commercial samples (not engineering samples) of the mask ROM version.

APPENDIX B.   DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78F9478.

★ **Software Package**

SP78K0S[Notes 1, 2]	CD-ROM in which the development tools (software) common to the 78K/0S Series are included as a package

Language Processing Software

RA78K0S[Notes 1, 2, 3]	Assembler package common to 78K/0S Series
CC78K0S[Notes 1, 2 ,3]	C compiler package common to 78K/0S Series
DF789488[Notes 1, 2, 3]	Device file for μPD78F9478
CC78K/0S-L[Notes 1, 2, 3]	C compiler library source file common to 78K/0S Series

Flash Memory Writing Tools

Flashpro III (Part number: FL-PR3[Note 4,] PG-FP3)	Dedicated flash memory programmer
★ FA-80GC-8BT[Note 4]	Adapter for writing to flash memory designed for 80-pin plastic QFP (GC-8BT type)

Debugging Tools

★ IE-78K0S-NS-A In-circuit emulator	In-circuit emulator to debug hardware or software when application systems using the 78K/0S Series are developed. The IE-78K0S-NS-A supports an integrated debugger (ID78K0S-NS). The IE-78K0S-NS-A is used in combination with an interface adapter for connection to an AC adapter, emulation probe, or host machine. The IE-78K0S-NS-A provides a coverage function in addition to the IE-78K0S-NS functions, thus enhancing the debug functions, including the tracer and timer functions.
IE-70000-MC-PS-B AC adapter	AC adapter to supply power from a 100 to 240 V AC outlet.
IE-70000-98-IF-C Interface adapter	Interface adapter required when using a PC-9800 Series computer (except notebook type) as the host machine (C bus supported).
IE-70000-CD-IF-A PC card interface	PC card and interface cable required when a notebook PC is used as the host machine (PCMCIA socket supported).
IE-70000-PC-IF-C Interface adapter	Interface adapter required when using an IBM PC/AT™ or compatible as the host machine (ISA bus supported).
★ IE-70000-PCI-IF-A Interface adapter	Interface adapter required when using a PC incorporating a PCI bus as the host machine.
IE-789488-NS-EM1 Emulation board	Emulation board to emulate the peripheral hardware specific to the device. The IE-789488-NS-EM1 is used in combination with the in-circuit emulator.
NP-80GC[Note 4] Emulation prove	Board to connect an in-circuit emulator to the target system. This board is dedicated for a 80-pin plastic QFP (GC-8BT type).
SM78K0S[Notes 1, 2]	System simulator common to 78K/0S Series
ID78K0S-NS[Notes 1, 2]	Integrated debugger common to 78K/0S Series
DF789488[Notes 1, 2]	Device file for μPD78F9478

Notes 1. Based on the PC-9800 series (Japanese Windows™)
    2. Based on IBM PC/AT or compatibles (Japanese/English Windows)
★   **3.** Based on the HP9000 series 700™ (HP-UX™), and SPARCstation™ (SunOS™, Solaris™)
★   **4.** Manufactured by Naito Densei Machida Mfg. Co, Ltd. (+81-45-475-4191).

Remark The RA78K0S, CC78K0S, SM78K0S, and ID78K0S-NS are used in combination with the DF789488 device file.

⋆ **APPENDIX C. RELATED DOCUMENTS**

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
*μ*PD789477, 789478 Data Sheet	U14699E
*μ*PD78F9478 Data Sheet	This document
*μ*PD789477 Subseries User's Manual	U15400E
78K/0S Series Instructions User's Manual	U11047E

Documents Related to Development Tools (Software) (User's Manuals)

Document Name		Document No.
RA78K0S Assembler Package	Operation	U14876E
	Language	U14877E
	Structured Assembly Language	U11623E
CC78K0S C Compiler	Operation	U14871E
	Language	U14872E
SM78K0S, SM78K0 System Simulator Ver. 2.10 or later	Operation (Windows Based)	U14611E
SM78K Series System Simulator Ver. 2.10 or Later	External Part User Open Interface Specifications	U15006E
ID78K0-NS, ID78K0S-NS Integrated Debugger Ver. 2.20 or Later	Operation (Windows Based)	U14910E
Project Manager Ver. 3.12 or Later (Windows Based)		U14610E

Documents Related to Development Tools (Hardware) (User's Manuals)

Document Name	Document No.
IE-78K0S-NS-A In-Circuit Emulator	U15207E
IE-789488-NS-EM1 Emulation Board	To be prepared

Documents Related to Flash Memory Writing

Document Name	Document No.
PG-FP3 Flash Memory Programmer User's Manual	U13502E

Caution   The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Other Documents

Document Name	Document No.
SEMICONDUCTORS SELECTION GUIDE Products and Packages (CD-ROM)	X13769E
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

┌───┐
│   ── **NOTES FOR CMOS DEVICES** ──   │

① **PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② **HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ **STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.
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Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability

- Ordering information

- Product release schedule

- Availability of related technical literature

- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)

- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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