DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD78F9418A

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78F9418A is a product in the μPD789417A Subseries (for driving LCD) of the 78K/0S Series.

The μPD78F9418A has flash memory in place of the internal ROM of the μPD789415A, 789416A, and 789417A.

Because flash memory allows the program to be written and erased electrically with the device mounted on the board, this product is ideal for the evaluation stages of system development, small-scale production, and rapid development of new products.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD789407A, 789417A Subseries User's Manual: U13952E
78K/0S Series User's Manual Instructions: U11047E

FEATURES

- Pin compatible with mask ROM version (except V_{PP} pin)
- Flash memory: 32 KB
- Internal data memory
  - High-speed RAM: 512 bytes
  - LCD display RAM: 28 × 4 bits
- Minimum instruction execution time can be changed from high-speed (0.4 μs:@ 5.0 MHz operation with main system clock) to ultra-low-speed (122 μs:@ 32.768 kHz operation with subsystem clock)
- I/O port: 43 pins
- Serial interface: 1 channel
  3-wire serial I/O mode/UART mode selectable
- 10-bit resolution A/D converter: 7 channels
- Timer: 6 channels
  - 16-bit timer: 1 channel
  - 8-bit timer/event counter: 2 channels
  - 8-bit timer: 1 channel
  - Watch timer: 1 channel
  - Watchdog timer: 1 channel
- LCD controller/driver
  - Segment signal: 28 pins MAX.
  - Common signal: 4 pins MAX.
  - 1/2- or 1/3-bias selectable
- Supply voltage: V_{DD} = 1.8 to 5.5 V

APPLICATIONS

APS compact cameras, blood pressure gauges, rice cookers, etc.

ORDERING INFORMATION

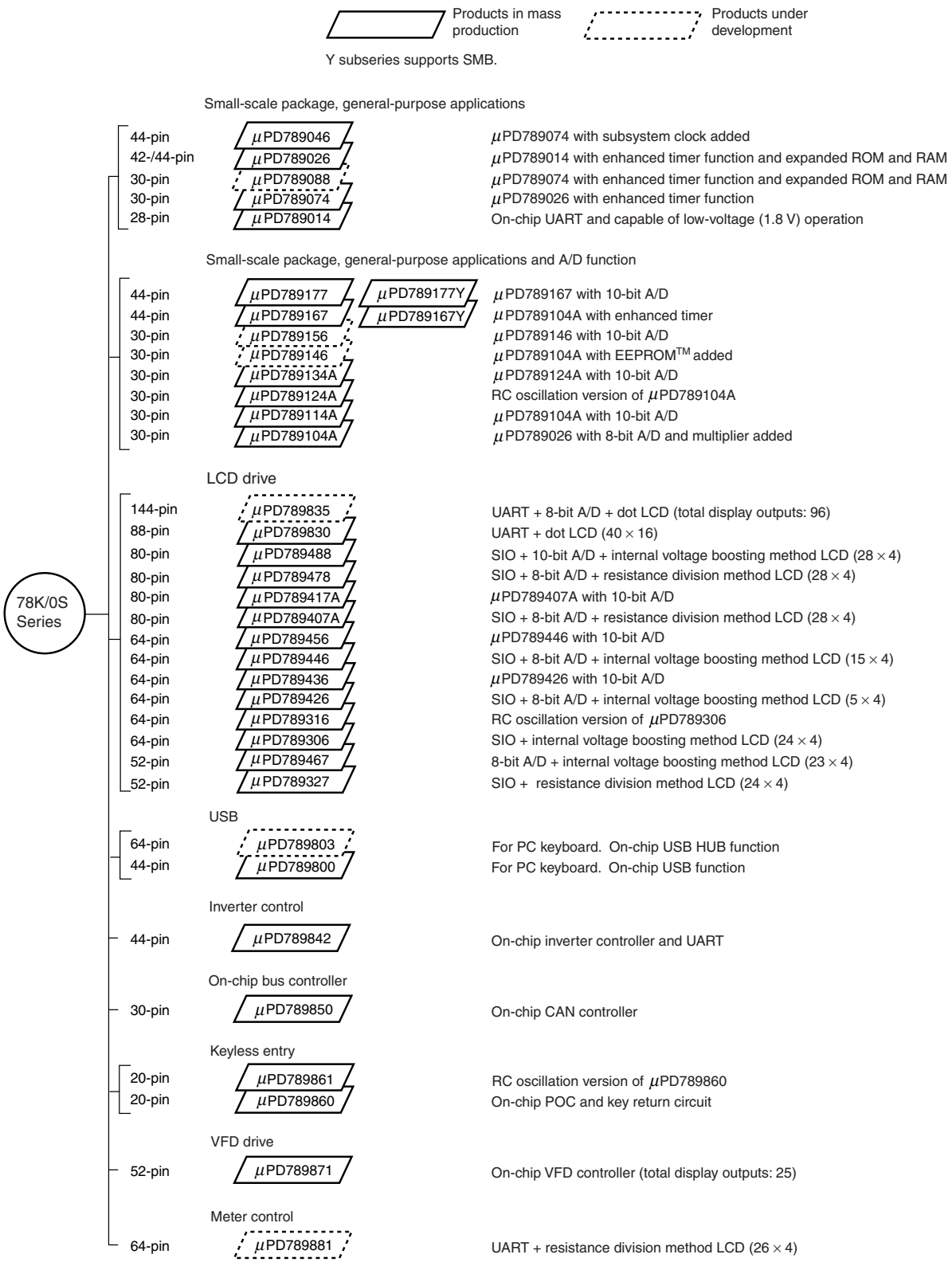
Part Number	Package
μPD78F9418AGC-8BT	80-pin plastic QFP (14 × 14)
μPD78F9418AGK-9EU	80-pin plastic TQFP (fine pitch) (12 ×12)

Document No. U14595EJ2V0DS00 (2nd edition)
Date Published March 2002 N CP(K)
Printed in Japan

The mark ★ shows major revised points.

★ 78K/0S SERIES LINEUP

The products in the 78K/0S Series are listed below. The names enclosed in boxes are subseries names.



Remark VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major functional differences among the subseries are listed below.

Series for General-Purpose and LCD Drive

Subseries Name \ Function		ROM Capacity (Bytes)	Timer				8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_{DD} MIN.Value	Remarks
			8-Bit	16-Bit	Watch	WDT						
Small-scale package, general-purpose applications	μPD789046	16 K	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART: 1ch)	34	1.8 V	–
	μPD789026	4 K to 16 K			–							
	μPD789088	16 K to 32 K	3 ch							24		
	μPD789074	2 K to 8 K	1 ch									
	μPD789014	2 K to 4 K	2 ch	–						22		
Small-scale package, general-purpose applications + A/D converter	μPD789177	16 K to 24 K	3 ch	1 ch	1 ch	1ch	–	8 ch	1 ch (UART: 1ch)	31	1.8 V	–
	μPD789167						8 ch	–				
	μPD789156	8 K to 16 K	1 ch		–		–	4 ch		20		On-chip EEPROM
	μPD789146						4 ch	–				
	μPD789134A	2 K to 8 K					–	4 ch				RC-oscillation version
	μPD789124A						4 ch	–				
	μPD789114A						–	4 ch				–
	μPD789104A						4 ch	–				
LCD drive	μPD789835	24 K to 60 K	6 ch	–	1 ch	1 ch	3 ch	–	1 ch (UART: 1ch)	37	1.8 V[Note]	Dot LCD supported
	μPD789830	24 K	1 ch	1 ch			–			30	2.7 V	
	μPD789488	32 K	3 ch					8 ch	2 ch (UART: 1ch)	45	1.8 V	–
	μPD789478	24 K to 32 K					8 ch	–				
	μPD789417A	12 K to 24 K					–	7 ch	1 ch (UART: 1ch)	43		
	μPD789407A						7 ch	–				
	μPD789456	12 K to 16 K	2 ch				–	6 ch		30		
	μPD789446						6 ch	–				
	μPD789436						–	6 ch		40		
	μPD789426						6 ch	–				
	μPD789316	8 K to 16 K					–		2 ch (UART: 1ch)	23		RC-oscillation version
	μPD789306											–
	μPD789467	4 K to 24 K		–			1 ch		–	18		
	μPD789327						–		1 ch	21		

Note Flash memory version: 3.0 V

Series for ASSP

Subseries Name \ Function		ROM Capacity (Bytes)	Timer				8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_{DD} MIN.Value	Remarks
			8-Bit	16-Bit	Watch	WDT						
USB	μPD789803	8 K to 16 K	2 ch	–	–	1 ch	–	–	2 ch (USB: 1ch)	41	3.6 V	–
	μPD789800	8 K								31	4.0 V	
Inverter control	μPD789842	8 K to 16 K	3 ch	**Note 1**	1 ch	1 ch	8 ch	–	1 ch (UART: 1ch)	30	4.0 V	–
On-chip bus controller	μPD789850	16 K	1 ch	1 ch	–	1 ch	4 ch	–	2 ch (UART: 1ch)	18	4.0 V	–
Keyless entry	μPD789861	4 K	2 ch	–	–	1 ch	–	–	–	14	1.8 V	RC-oscillation version, on-chip EEPROM
	μPD789860											On-chip EEPROM
VFD drive	μPD789871	4 K to 8 K	3 ch	–	1 ch	1 ch	–	–	1 ch	33	2.7 V	–
Meter control	μPD789881	16 K	2 ch	1 ch	–	1 ch	–	–	1 ch (UART: 1 ch)	28	2.7 V[Note 2]	–

Notes 1. 10-bit timer: 1 channel

2. Flash memory version: 3.0 V

OVERVIEW OF FUNCTIONS

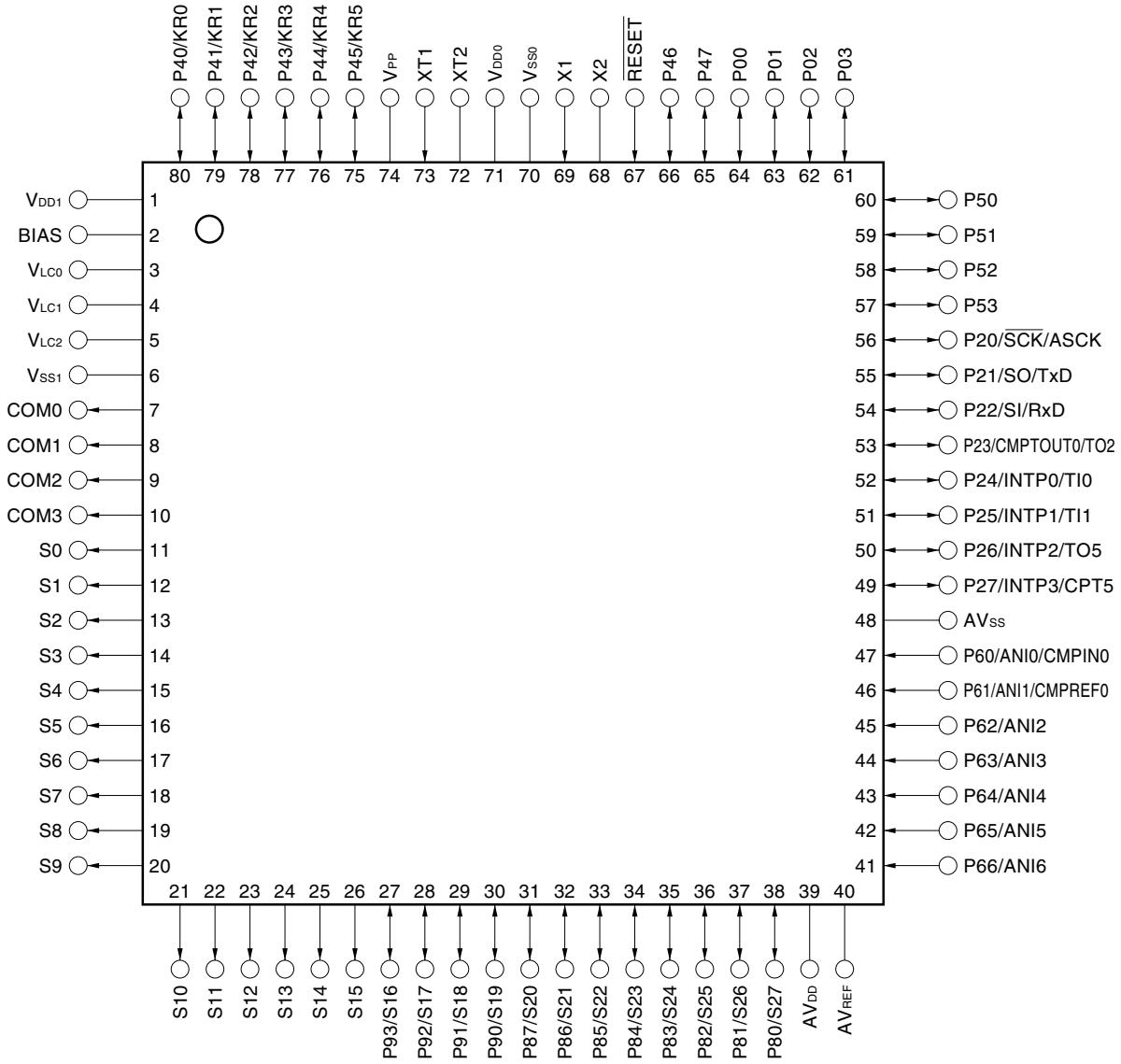
Item		Function
Internal memory	Flash memory	32 KB
	High-speed RAM	512 bytes
	LCD display RAM	28 × 4 bits
Minimum instruction execution time		0.4 μs/1.6 μs (@5.0 MHz operation with main system clock) 122 μs (@32.768 kHz operation with subsystem clock)
General-purpose register		8 bits × 8 registers
Instruction set		• 16-bit operation • Bit manipulation (set, reset, test), etc.
I/O port		Total: 43 pins • CMOS input: 7 pins • CMOS I/O: 32 pins • N-ch open drain (12 V withstand voltage): 4 pins
A/D converter		10-bit resolution × 7 channels
Comparator		Timer output controllable
Serial interface		3-wire serial I/O mode/UART mode selectable: 1 channel
LCD controller/driver		• Segment signal output: 28 pins max. • Common signal output: 4 pins max. • 1/2 or 1/3 bias selectable
Timer		• 16-bit timer: 1 channel • 8-bit timer: 1 channel • 8-bit timer/event counter: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel
Timer output		2 pins
Vectored interrupt source	Maskable	Internal: 12, external: 4
	Non-maskable	Internal: 1
Supply voltage		V_{DD} = 1.8 to 5.5 V
Operating ambient temperature		T_A = –40 to +85°C
Package		• 80-pin plastic QFP (14 × 14) • 80-pin plastic TQFP (fine pitch) (12 × 12)

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

• 80-pin plastic QFP (14 × 14)
μPD78F9418AGC-8BT

• 80-pin plastic TQFP (fine pitch) (12 × 12)
μPD78F9418AGK-9EU

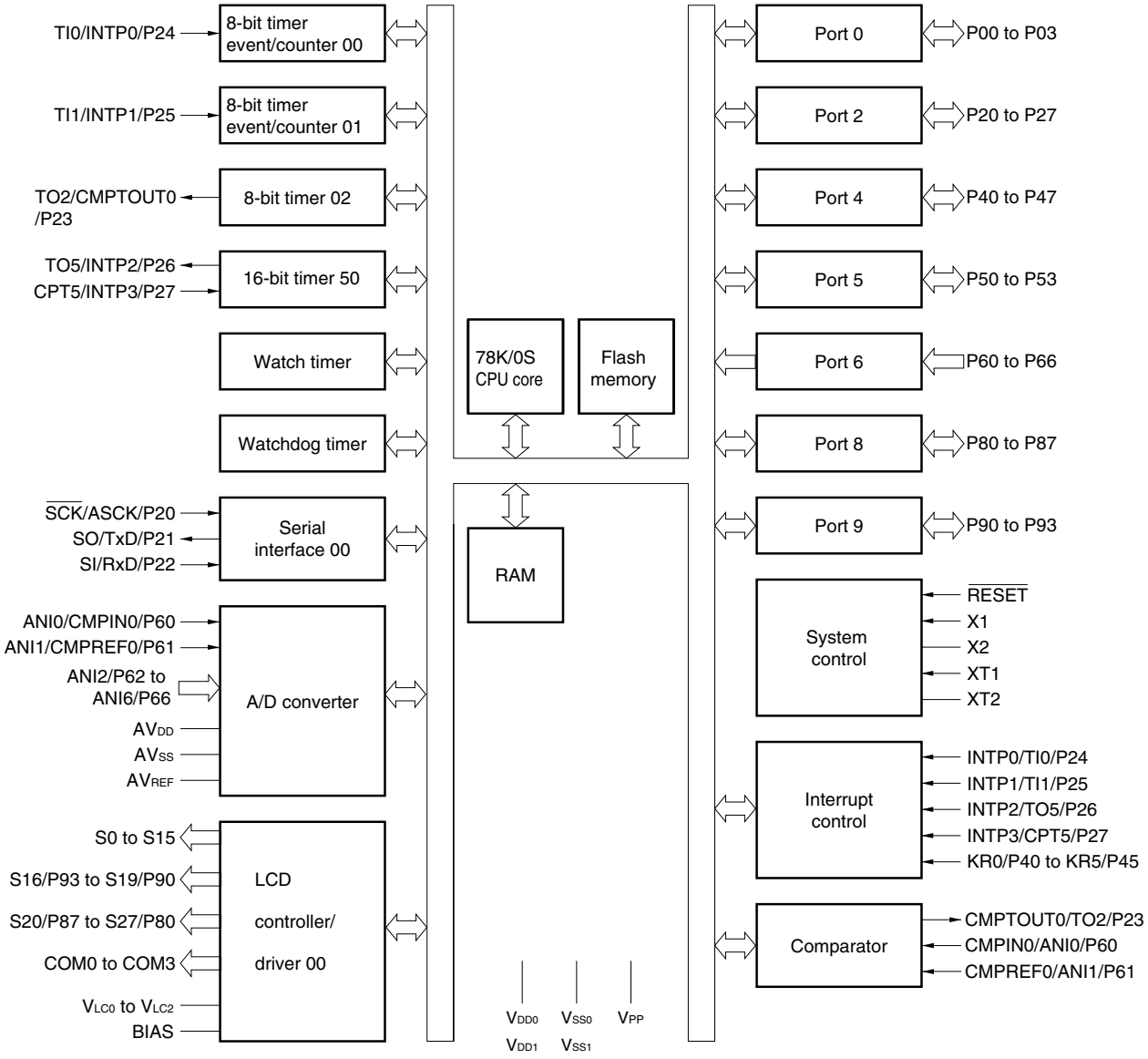


★ **Caution Handle the V_{PP} pin in either of the following ways.**

- **Independently connect a 10 kΩ pull-down resistor.**
- **Set the jumper on the board to switch V_{PP} pin so that it is connected to connect to the dedicated flash programmer in the programming mode, and directly to V_{SS0} in the normal operation mode.**

ANI0 to ANI6:	Analog input
ASCK:	Asynchronous serial input
AV_{DD}:	Analog power supply
AV_{REF}:	Analog reference voltage
AV_{SS}:	Analog ground
BIAS:	LCD power supply bias control
CMPIN0:	Comparator input
CMPREF0:	Comparator reference
CMPTOUT0:	Comparator output
COM0 to COM3:	Common output
CPT5:	Capture trigger input
INTP0 to INTP3:	Interrupt from peripherals
KR0 to KR5:	Key return
P00 to P03:	Port 0
P20 to P27:	Port 2
P40 to P47:	Port 4
P50 to P53:	Port 5
P60 to P66:	Port 6
P80 to P87:	Port 8
P90 to P93:	Port 9
$\overline{\text{RESET}}$:	Reset
RxD:	Receive data
S0 to S27:	Segment output
$\overline{\text{SCK}}$:	Serial clock
SI:	Serial input
SO:	Serial output
TI0, TI1:	Timer input
TO2, TO5:	Timer output
TxD:	Transmit data
V_{DD0}, V_{DD1}:	Power supply
V_{LC0} to V_{LC2}:	LCD power supply
V_{PP}:	Programming power supply
V_{SS0}, V_{SS1}:	Ground
X1, X2:	Crystal (main system clock)
XT1, XT2:	Crystal (subsystem clock)

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P03	I/O	Port 0. 4-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of a software setting.	Input	–
P20	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of a software setting.	Input	$\overline{SCK}$/ASCK
P21				SO/TxD
P22				SI/RxD
P23				CMPTOUT0/TO2
P24				INTP0/TI0
P25				INTP1/TI1
P26				INTP2/TO5
P27				INTP3/CPT5
P40 to P45	I/O	Port 4. 8-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of a software setting.	Input	KR0 to KR5
P46, P47				–
P50 to P53	I/O	Port 5. 4-bit N-ch open-drain I/O port. Input/output can be specified in 1-bit units.	Input	–
P60	Input	Port 6. 7-bit input only port.	Input	ANI0/CMPIN0
P61				ANI1/CMPREF0
P62 to P66				ANI2 to ANI6
P80 to P87	I/O	Port 8. 8-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of a software setting.	Input	S27 to S20
P90 to P93	I/O	Port 9. 4-bit I/O port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of a software setting.	Input	S19 to S16

3.2 Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input for which the valid edge (rising, falling, or both rising and falling edges) can be specified	Input	P24/TI0
INTP1				P25/TI1
INTP2				P26/TO5
INTP3				P27/CPT5
KR0 to KR5	Input	Key return signal detection	Input	P40 to P45
SI	Input	Serial interface serial data input	Input	P22/RxD
SO	Output	Serial interface serial data output	Input	P21/TxD
$\overline{SCK}$	I/O	Serial interface serial clock input/output	Input	P20/ASCK
ASCK	Input	Serial clock input for asynchronous serial interface	Input	P20/$\overline{SCK}$
RxD	Input	Serial data input for asynchronous serial interface	Input	P22/SI
TxD	Output	Serial data output for asynchronous serial interface	Input	P21/SO
TI0	Input	External count clock input to 8-bit timer (TM00)	Input	P24/INTP0
TI1	Input	External count clock input to 8-bit timer (TM01)	Input	P25/INTP1
TO2	Output	8-bit timer (TM02) output	Input	P23/CMPTOUT0
TO5	Output	16-bit timer (TM50) output	Input	P26/INTP2
CPT5	Input	Capture edge input	Input	P27/INTP3
CMPTOUT0	Output	Comparator output	Input	P23/TO2
CMPIN0	Input	Comparator input	Input	P60/ANI0
CMPREF0	Input	Comparator reference voltage input	Input	P61/ANI1
ANI0	Input	Analog input for A/D converter	Input	P60/CMPIN0
ANI1				P61/CMPREF0
ANI2 to ANI6				P62 to P66
AV_{REF}	–	Reference voltage for A/D converter	–	–
AV_{SS}	–	Ground potential for A/D converter	–	–
AV_{DD}	–	Analog power supply for A/D converter	–	–
S0 to S15	Output	Segment signal output of LCD controller/driver	Output	–
S16 to S19			Input	P93 to P90
S20 to S27				P87 to P80
COM0 to COM3	Output	Common signal output of LCD controller/driver	Output	–
V_{LC0} to V_{LC2}	–	LCD driving voltage	–	–
BIAS	–	Supply voltage for LCD driving	–	–
X1	Input	Connecting crystal resonator for main system clock oscillation	–	–
X2	–		–	–
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	–	–
XT2	–		–	–
$\overline{RESET}$	Input	System reset input	Input	–

3.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
V_{DD0}	–	Positive power supply for ports	–	–
V_{DD1}	–	Positive power supply (except ports)	–	–
V_{SS0}	–	Ground potential for ports	–	–
V_{SS1}	–	Ground potential (except ports)	–	–
V_{PP}	–	Flash memory programming mode setting. High-voltage application for program write/verify.	–	–

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.

For the I/O circuit configuration of each type, refer to **Figure 3-1**.

Table 3-1. Types of Pin I/O Circuits and Recommended Connection of Unused Pins

	Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
	P00 to P03	5-H	I/O	Input: Independently connect to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via a resistor.
	P20/$\overline{SCK}$/ASCK	8-C		Output: Leave open.
	P21/SO/TxD			
	P22/SI/RxD			
	P23/CMPTOUT0/TO2	10-B		
★	P24/INTP0/TI0	8-C		Input: Independently connect to V_{DD0} or V_{SS1} via a resistor.
★	P25/INTP1/TI1			Output: Leave open.
★	P26/INTP2/TO5			
★	P27/INTP3/CPT5			
	P40/KR0 to P45/KR5			Input: Independently connect to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via a resistor.
	P46, P47	5-H		Output: Leave open.
	P50 to P53	13-T		Input: Independently connect to V_{DD0} or V_{DD1} via a resistor. Output: Leave open.
	P60/ANI0/CMPIN0	9-D	Input	Connect directly to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1}.
	P61/ANI1/CMPREF0			
	P62/ANI2 to P66/ANI6	9-C		
	P80/S27 to P87/S20	17-F	I/O	Input: Independently connect to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via a resistor.
	P90/S19 to P93/S16			Output: Leave open.
	S0 to S15	17-B	Output	Leave open.
	COM0 to COM3	18-A		
	V_{LC0} to V_{LC2}	–	–	
	BIAS			Leave open (If all V_{LC0} to V_{LC2} are unused, however, independently connect them to V_{SS0} or V_{SS1} via a resistor).
★	AV_{REF}			Connect directly to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1}.
★	AV_{DD}			Connect directly to V_{DD0}, or V_{SS1}.
★	AV_{SS}			Connect directly to V_{DD0}, or V_{SS1}.
	XT1		Input	
	XT2		–	Leave open.
	$\overline{RESET}$	2	Input	–
★	V_{PP}	–	–	Connect a 10 kΩ pull-down resistor or connect directly to V_{SS0} or V_{SS1}.

Figure 3-1. Pin I/O Circuits (1/2)

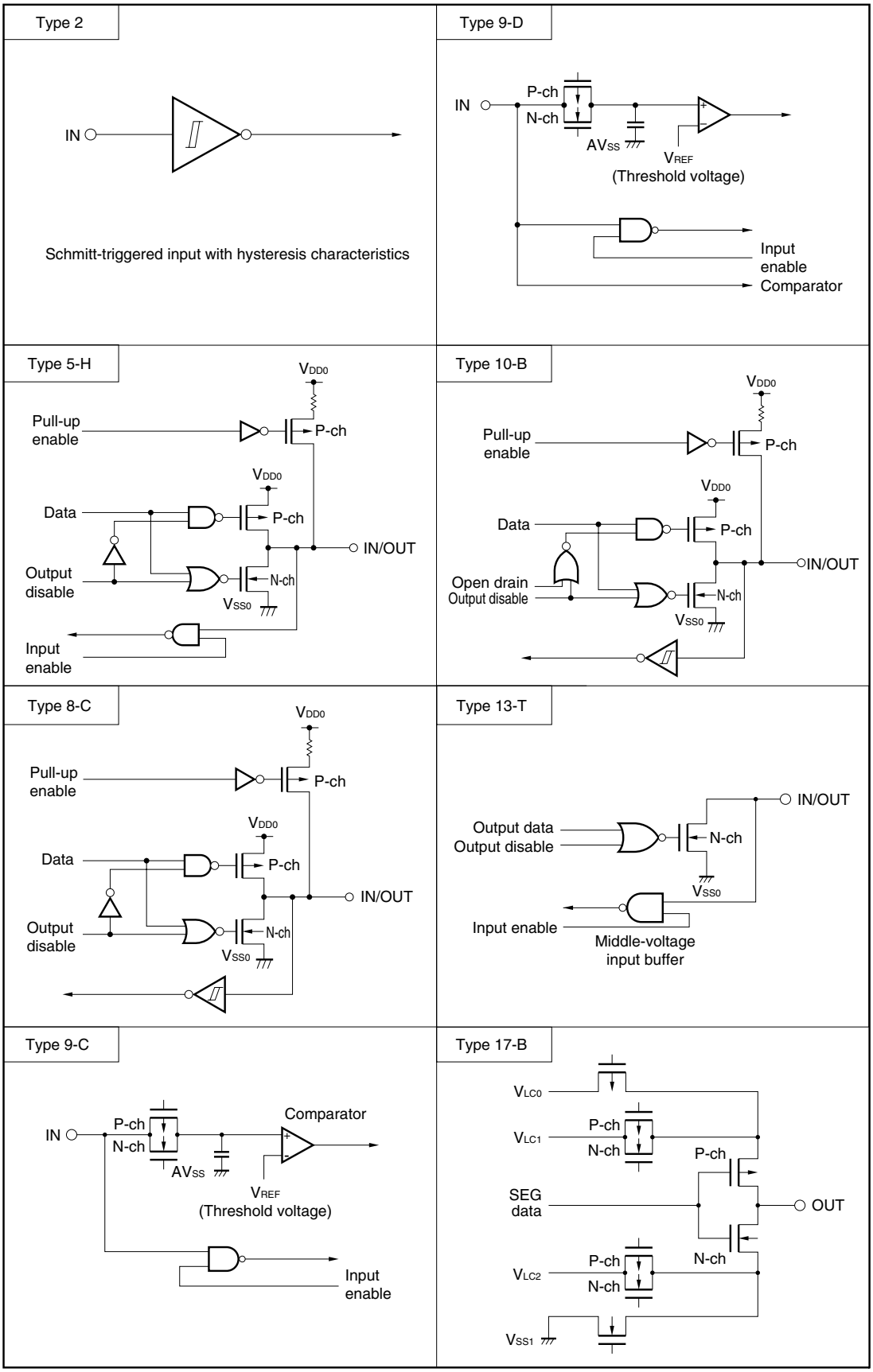
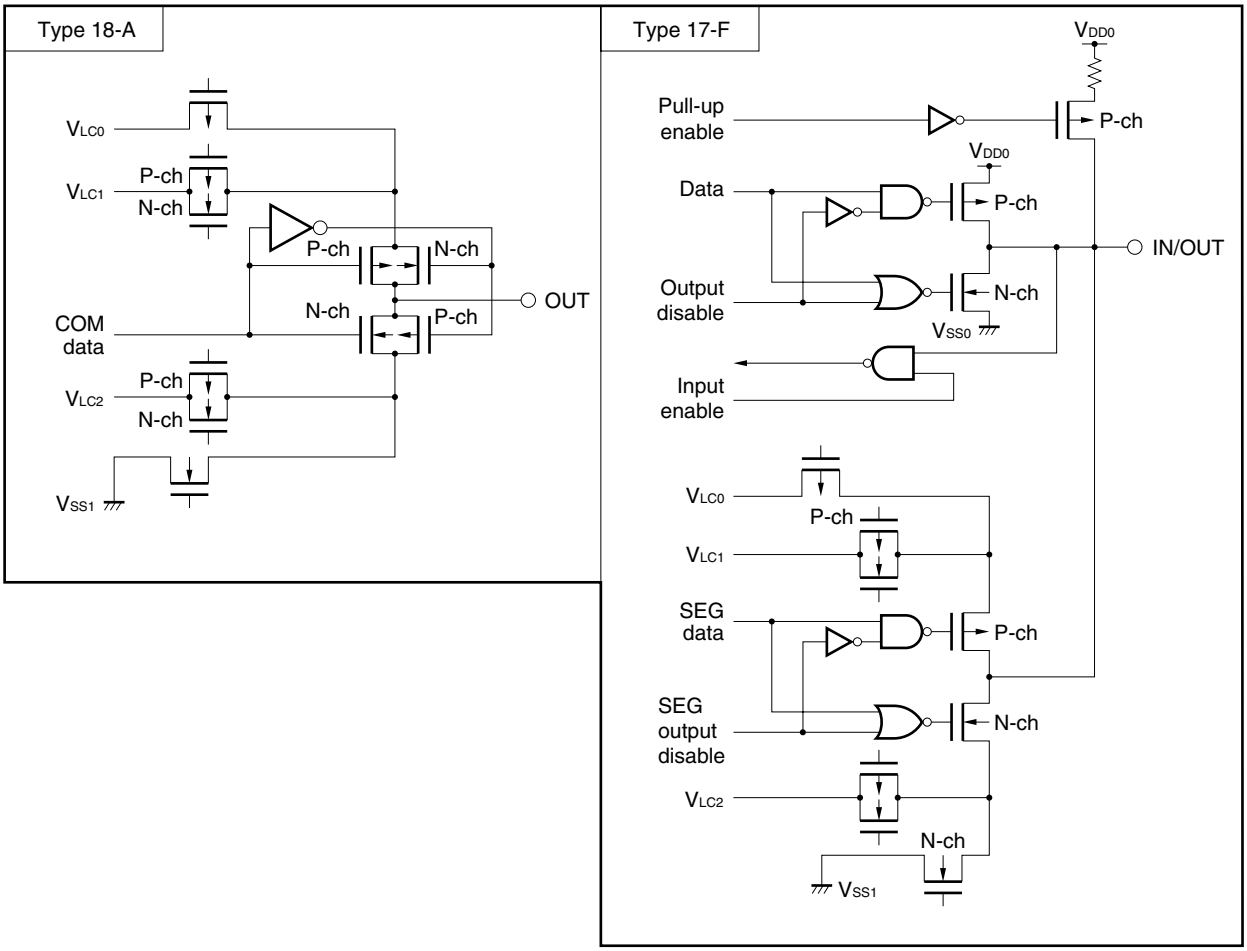


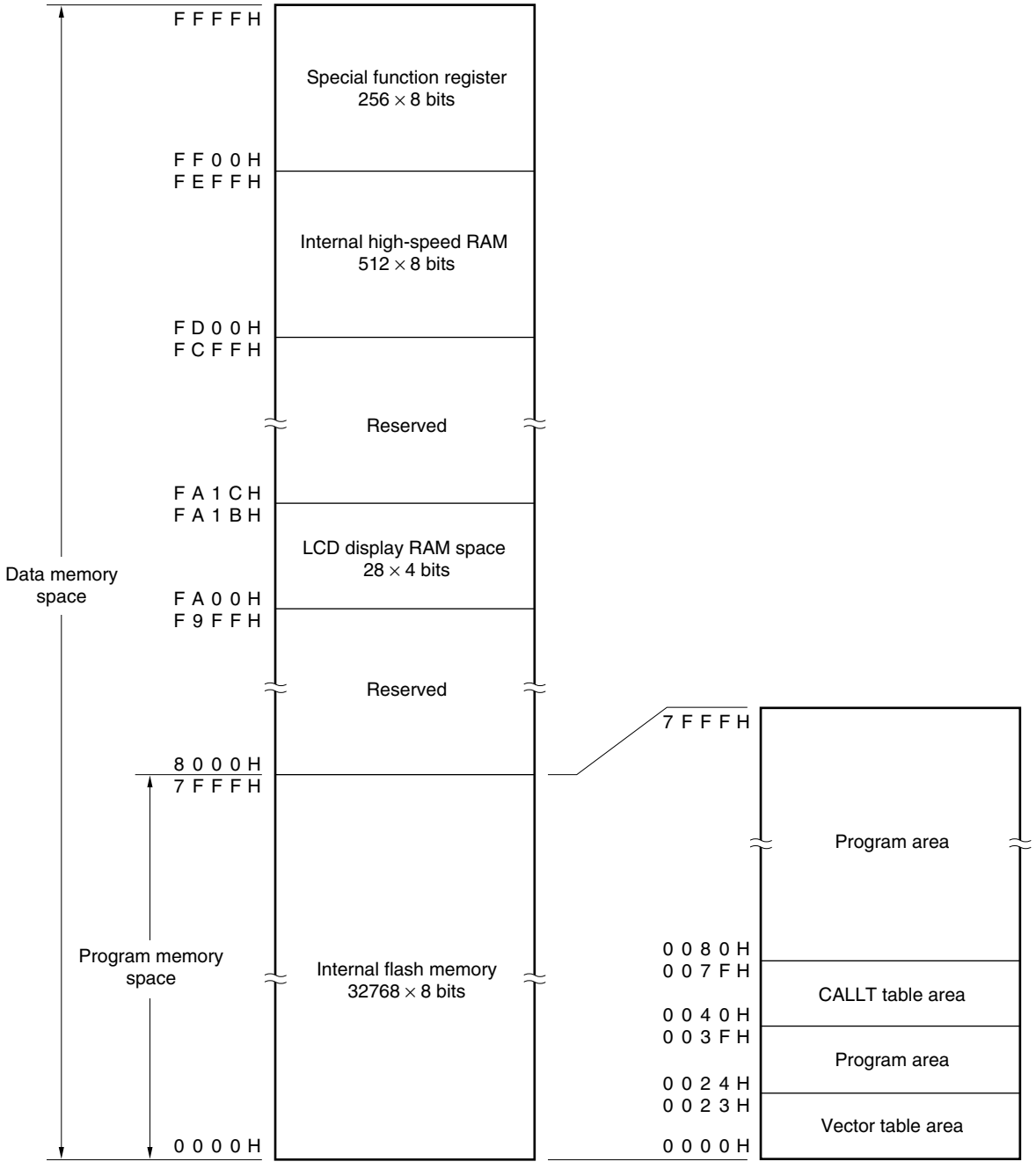
Figure 3-1. Pin I/O Circuits (2/2)



4. MEMORY SPACE

The μPD78F9418A can access 64 KB of memory space. Figure 4-1 shows the memory map.

Figure 4-1. Memory Map



5. FLASH MEMORY PROGRAMMING

The program memory that is incorporated in the μPD78F9418A is flash memory.

With flash memory, it is possible to write programs on-board. Writing is performed by connecting a dedicated flash programmer (Flashpro III (Part No. FL-PR3, PG-FP3)) to the host machine and the target system.

Remark FL-PR3 is a product of Naito Densei Machida Mfg. Co., Ltd.

5.1 Selecting Communication Mode

Writing to flash memory is performed using the Flashpro III in a serial communication mode. Select one of the communication modes in Table 5-1. The selection of the communication mode is made by using the format shown in Figure 5-1. Each communication mode is selected using the number of V_{PP} pulses shown in Table 5-1.

Table 5-1. List of Communication Mode

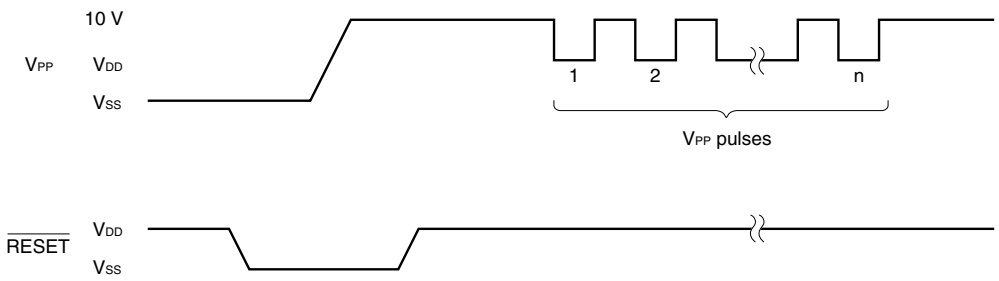
Communication Mode	Pins[Note 1]	V_{PP} Pulses
3-wire serial I/O	$\overline{SCK}$/ASCK/P20 SO/TxD/P21 SI/RxD/P22	0
UART	TxD/SO/P21 RxD/SI/P22	8
Pseudo 3-wire[Note 2]	P00 (Serial clock input) P01 (Serial data output) P02 (Serial data input)	12
	P40/KR0 (Serial clock input) P41/KR1 (Serial data output) P42/KR2 (Serial data input)	13

★ **Notes 1.** Shifting to the flash memory programming mode sets all pins not used for flash memory programming to the same state as that immediately after reset. If the external device connected to each port does not acknowledge the state immediately after reset, pin handling such as connecting to V_{DD} or V_{SS} via a resistor is required.

2. Serial transfer is performed by controlling ports by software.

Caution Be sure to select a communication mode using the number of V_{PP} pulses shown in Table 5-1.

Figure 5-1. Format of Communication Mode Selection



5.2 Function of Flash Memory Programming

Operations such as writing to flash memory are performed by various command/data transmission and reception operations according to the selected communication mode. Table 5-2 shows the major functions of flash memory programming.

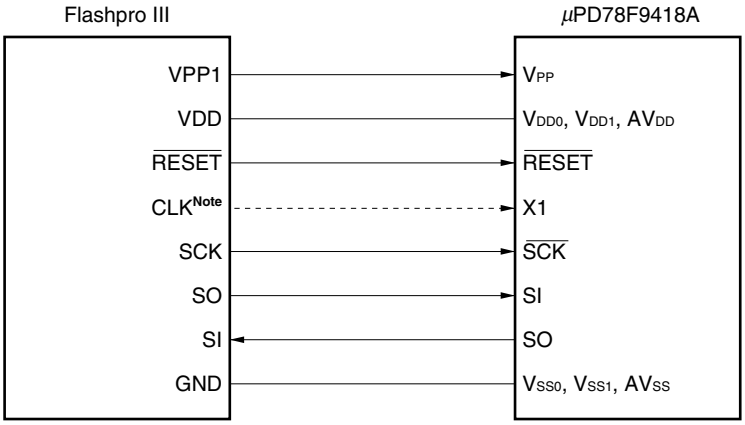
Table 5-2. Major Function of Flash Memory Programming

Function	Description
Batch erase	Deletes the entire memory contents.
Batch blank check	Checks the deletion status of the entire memory.
Data write	Performs a write operation to the flash memory based on the write start address and the number of data to be written (number of bytes).
Batch verify	Compares the entire memory contents with the input data.

5.3 Connecting Flashpro III

The connection of the Flashpro III and the μPD78F9418A differs according to the communication mode (3-wire serial I/O, UART, and pseudo 3-wire). The connections for each communication mode are shown in Figures 5-2, 5-3, and 5-4, respectively.

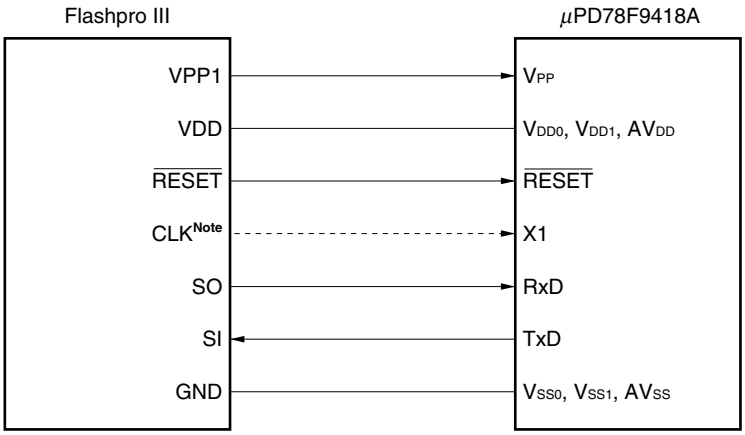
Figure 5-2. Connection Example of Flashpro III When Using 3-Wire Serial I/O Mode



★ **Note** Connect the CLK pin when the system clock is input from the Flashpro III. When a resonator has already been connected to the X1 pin, there is no need to connect the CLK pin to X1 pin.

★ **Caution Be sure to connect the V_{DD} pin to the V_{DD} pin of Flashpro III, even if the power supply is connected to the pin. When using the power supply, apply the voltage before starting programming.**

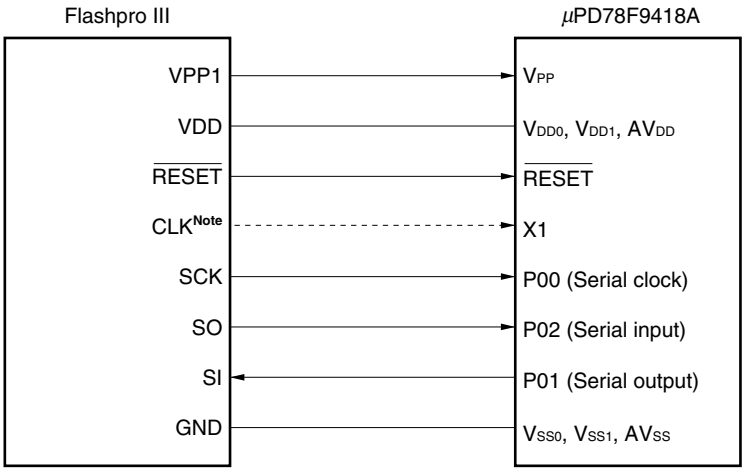
Figure 5-3. Connection Example of Flashpro III When Using UART Mode



★ **Note** Connect the CLK pin when the system clock is input from the Flashpro III. When a resonator has already been connected to the X1 pin, there is no need to connect the CLK pin to X1 pin.

★ **Caution Be sure to connect the V_{DD} pin to the V_{DD} pin of Flashpro III, even if the power supply is connected to the pin. When using the power supply, apply the voltage before starting programming.**

Figure 5-4. Connection Example of Flashpro III When Using Pseudo 3-Wire (When P0 Is Used)



★ **Note** Connect the CLK pin when the system clock is input from the Flashpro III. When a resonator has already been connected to the X1 pin, there is no need to connect the CLK pin to X1 pin.

★ **Caution Be sure to connect the V_{DD} pin to the V_{DD} pin of Flashpro III, even if the power supply is connected to the pin. When using the power supply, apply the voltage before starting programming.**

5.4 Example of Settings for Flashpro III (PG-FP3)

When writing to flash memory using Flashpro III (PG-FP3), make the following settings.

<1> Load a parameter file.

<2> Select the mode of serial communication and serial clock with a type command.

<3> Make the settings according to the example of settings for PG-FP3 shown below.

Table 5-3. Example of Settings for PG-FP3

Communication Mode	Example of Settings for PG-FP3		V_{PP} Pulse Number[Note 1]
3-wire serial I/O	COMM PORT	SIO-ch0	0
	CPU CLK	On Target Board	
		In Flashpro	
	On Target Board	4.1943 MHz	
	SIO CLK	1.0 MHz	
	In Flashpro	4.0 MHz	
	SIO CLK	1.0 MHz	
UART	COMM PORT	UART-ch0	8
	CPU CLK	On Target Board	
★	On Target Board	4.91 MHz	
	UART BPS	9600 bps[Note 2]	
Pseudo 3-wire	COMM PORT	Port A/B	12/13
	CPU CLK	On Target Board	
		In Flashpro	
	On Target Board	4.1943 MHz	
	SIO CLK	1.0 kHz	
	In Flashpro	4.0 MHz	
	SIO CLK	1.0 kHz	

Notes 1. This is the number of V_{PP} pulses that are supplied by the Flashpro III at serial communication initialization. The pins that will be used for communication are determined according to this number.

2. Select one of 9600 bps, 19200 bps, 38400 bps, or 76800 bps.

Remark COMM PORT: Serial port selection
SIO CLK: Serial clock frequency selection
CPU CLK: Input CPU clock source selection

★ 5.5 On-Board Pin Connections

When programming on the target system, provide a connector on the target system to connect to the dedicated flash programmer.

There may be cases in which an on-board function that switches from the normal operation mode to flash memory programming mode is required.

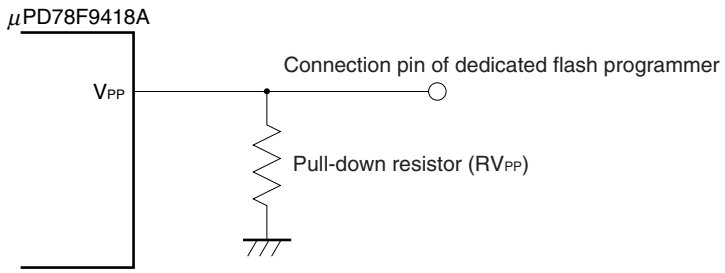
<V_{PP} pin>

Input 0 V to the V_{PP} pin in the normal operation mode. A write voltage of 10.0 V (TYP.) is supplied to the V_{PP} pin in the flash memory programming mode. Therefore, connect the V_{PP} pin using method (1) or (2) below.

(1) Connect a pull-down resistor of RV_{PP} = 10 kΩ to the V_{PP} pin.
(2) Set the jumper on the board to switch the input of V_{PP} pin to the programmer side or directly to GND.

The following shows an example of V_{PP} pin connection.

Figure 5-5. V_{PP} Pin Connection Example



<Serial interface pins>

The following shows the pins used by each serial interface.

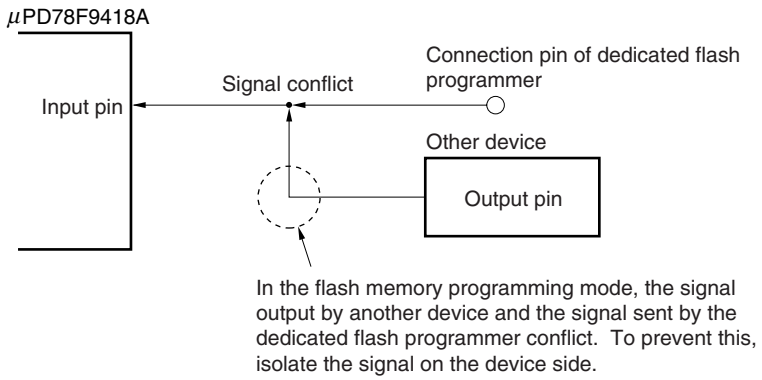
Serial Interface	Pins Used
3-wire serial I/O	SI, SO, $\overline{SCK}$
UART	RxD, TxD
Pseudo 3-wire	P00, P01, P02
	P40, P41, P42

Note that signal conflict or malfunction of other devices may occur when an on-board serial interface pin that is connected to another device is connected to the dedicated flash programmer.

(1) Signal conflict

A signal conflict occurs if the dedicated flash programmer (output) is connected to a serial interface pin (input) connected to another device (output). To prevent this signal conflict, isolate the connection with the other device or put the other device in the output high impedance status.

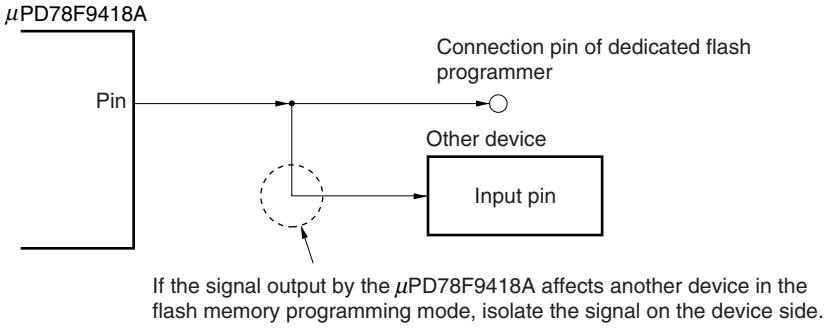
Figure 5-6. Signal Conflict (Serial Interface Input Pin)

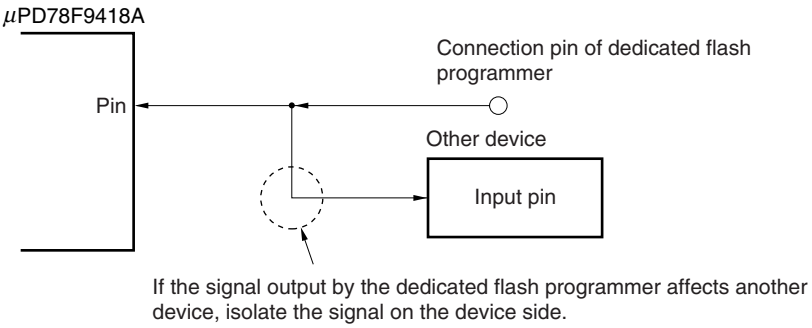


(2) Malfunction of another device

When the dedicated flash programmer (output or input) is connected to a serial interface pin (input or output) connected to another device (input), a signal may be output to the device, causing a malfunction. To prevent such malfunction, isolate the connection with other device or set so that the input signal to the device is ignored.

Figure 5-7. Malfunction of Another Device



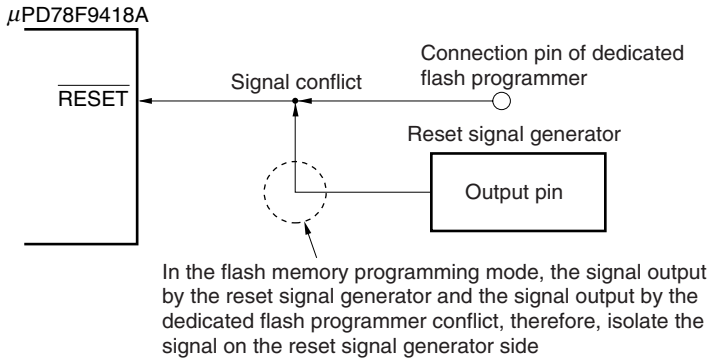


<$\overline{\text{RESET}}$ pin>

When the reset signal of the dedicated flash programmer is connected to the $\overline{\text{RESET}}$ pin connected to the reset signal generator on the board, a signal conflict occurs. To prevent this signal conflict, isolate the connection with the reset signal generator.

If a reset signal is input from the user system in the flash memory programming mode, a normal programming operation will not be performed. Do not input signals other than reset signals from the dedicated flash programmer during this period.

Figure 5-8. Signal Conflict ($\overline{\text{RESET}}$ Pin)



<Port pins>

Shifting to the flash memory programming mode sets all the pins except those used for flash memory programming communication to the status immediately after reset.

Therefore, if the external device does not acknowledge an initial status such as the output high impedance status, connect the external device to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via a resistor.

<Oscillation pins>

When using an on-board clock, connection of X1, X2, XT1, and XT2 must conform to the methods in the normal operation mode.

When using the clock output of the flash programmer, directly connect it to the X1 pin with the on-board main oscillator disconnected, and leave the X2 pin open. For the subclock, connection conforms to that in the normal operation mode.

<Power supply>

To use the power output of the flash programmer, connect the V_{DD0} and V_{DD1} pins to VDD of the flash programmer, and the V_{SS0} and V_{SS1} pins to GND of the flash programmer.

To use the on-board power supply, connection must conform to that in the normal operation mode. However, because the voltage is monitored by the flash programmer, therefore, VDD of the flash programmer must be connected.

For the other power pins (AV_{DD}, AV_{REF}, AV_{SS}), supply the same power supply as in the normal operation mode.

<Other pins>

Handle the other pins (S0 to S15, COM0 to COM3, V_{LC0} to V_{LC2}, BIAS) in the same way as in the normal operation mode.

⋆ 5.6 Connection When Using Flash Memory Writing Adapter

The following shows an example of the recommended connection when using the flash memory writing adapter.

Figure 5-9. Example of Flash Memory Writing Adapter Connection When Using 3-Wire Serial I/O Mode

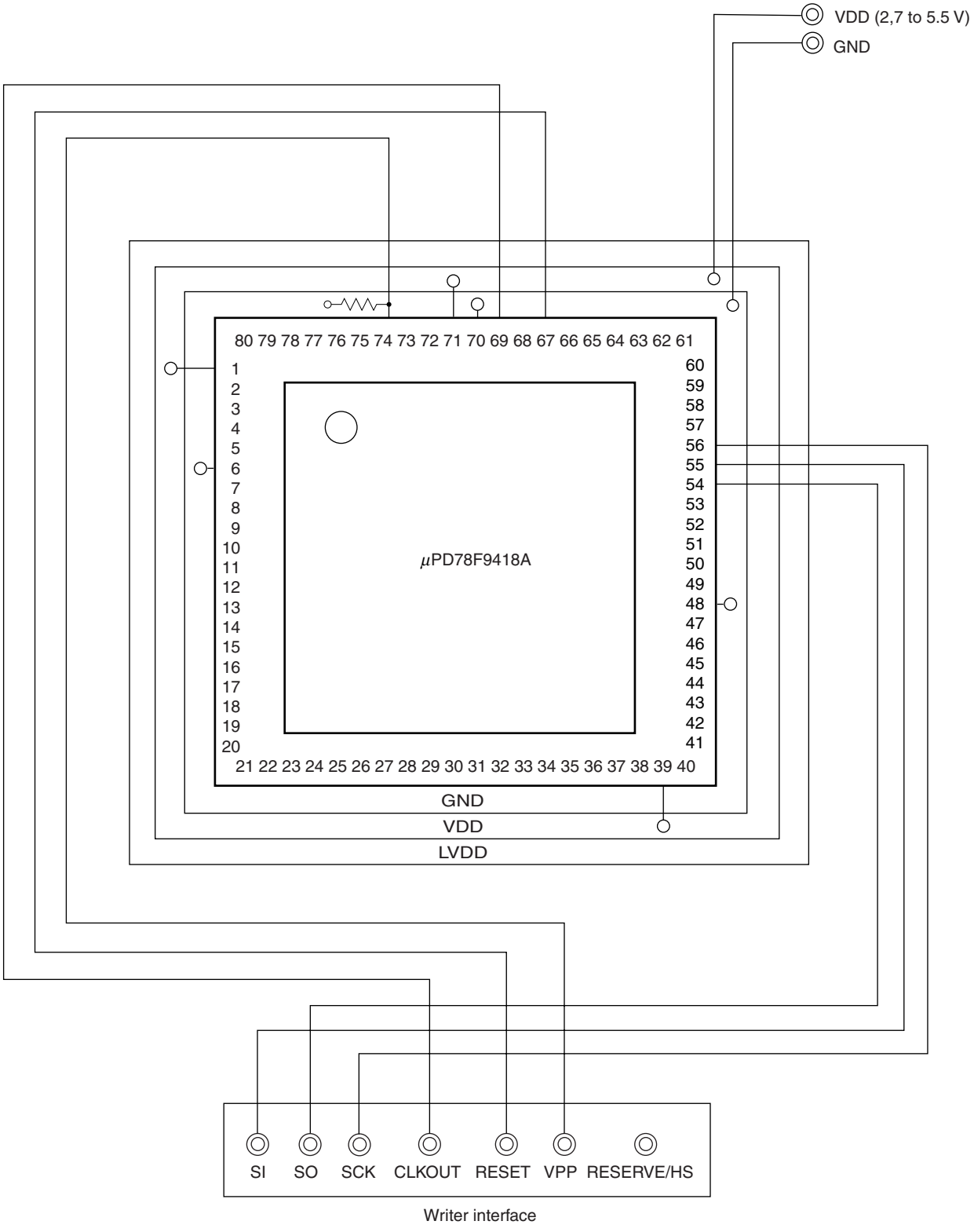


Figure 5-10. Example of Flash Memory Writing Adapter Connection When Using UART Mode

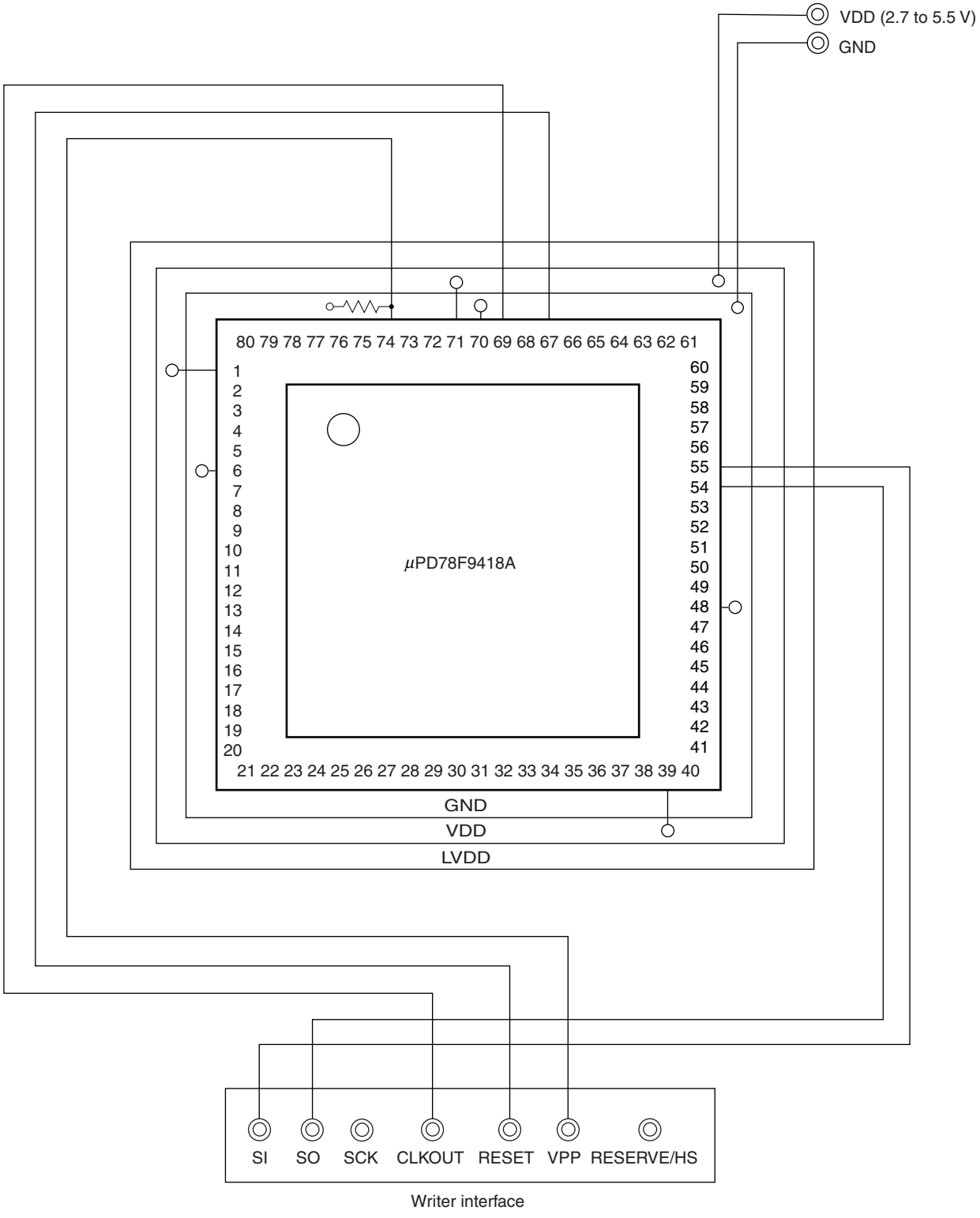
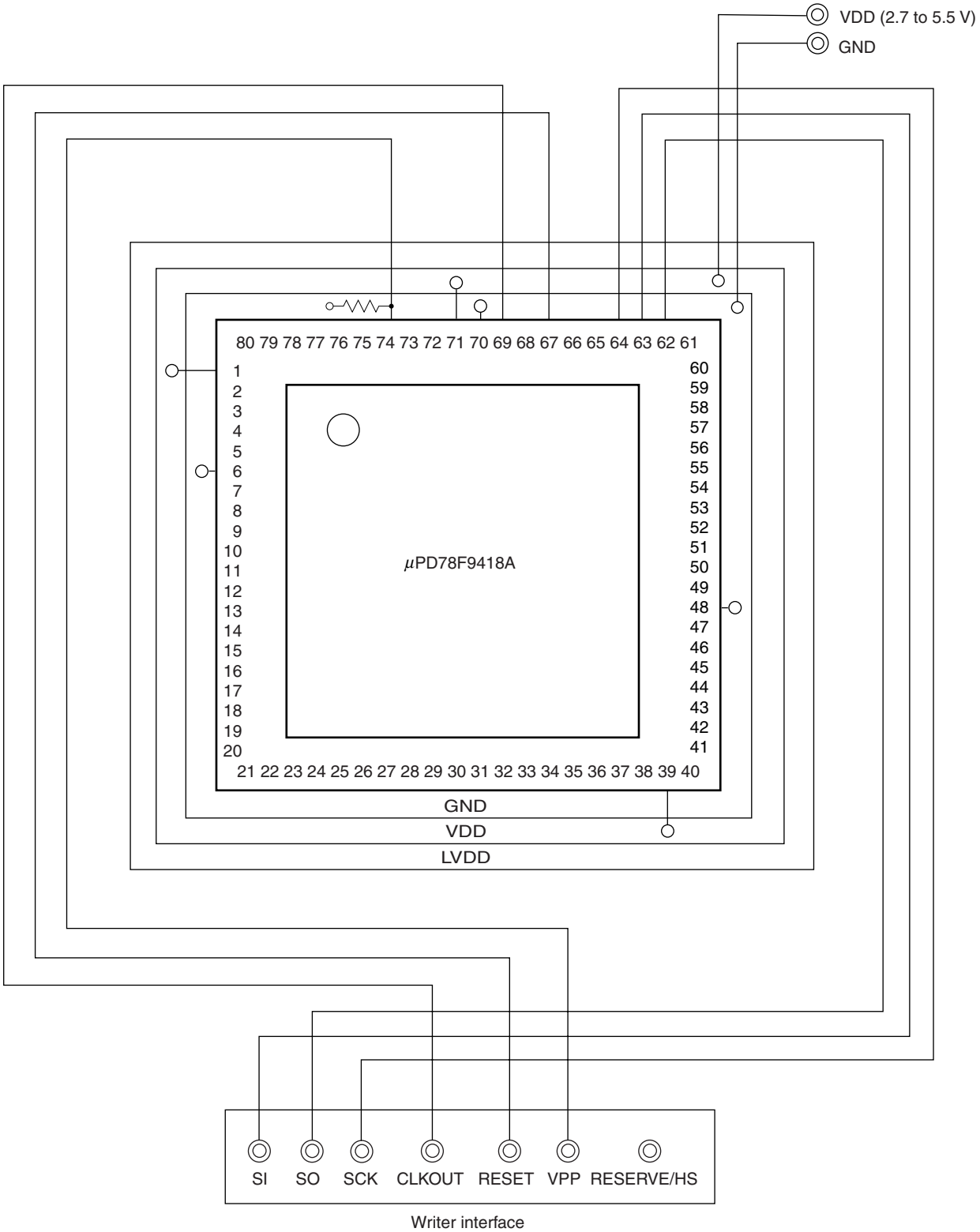


Figure 5-11. Example of Flash Memory Writing Adapter Connection When Using Pseudo 3-Wire Mode (When P0 Is Used)



6. OUTLINE OF INSTRUCTION SET

This section shows a list of the instructions of the μPD78F9418A.

6.1 Conventions

6.1.1 Operand formats and syntax

One or more operands are written in the operand field of each instruction in accordance with the operand format and syntax of that instruction (for details, refer to the assembler specifications). If two or more operands are shown, select one of them. The uppercase characters, and the symbols #, !, $, [, and] are keywords and must be written as shown. The meanings of these symbols are as follows:

- #: Specifies immediate data.
- !: Specifies an absolute address.
- $: Specifies a relative address.
- [ ]: Specifies an indirect address.

To specify immediate data, write an appropriate value or label. When using a label, be sure to use the symbols #, !, $, [, and].

The register syntax operands r and rp can be specified as either a function name (such as X, A, and C) or an absolute name (such as R0, R1, and R2 as shown in the parentheses in the table below).

Table 6-1. Operand Formats and Syntax

Format	Syntax
r	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7)
rp	AX (RP0), BC (RP1), DE (RP2), HL (RP3)
sfr	Special function register symbol
saddr	FE20H to FF1FH Immediate data or label
saddrp	FE20H to FF1FH Immediate data or label (even address only)
addr16	0000H to FFFFH Immediate data or label (even address only when 16-bit data transfer instruction is used)
addr5	0040H to 007FH Immediate data or label (even address only)
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit	3-bit immediate data or label

6.1.2 Explanation of symbols in operation field

A: A register; 8-bit accumulator
X: X register
B: B register
C: C register
D: D register
E: E register
H: H register
L: L register
AX: AX register pair; 16-bit accumulator
BC: BC register pair
DE: DE register pair
HL: HL register pair
PC: Program counter
SP: Stack pointer
PSW: Program status word
CY: Carry flag
AC: Auxiliary carry flag
Z: Zero flag
IE: Interrupt request enable flag
NMIS: Non-maskable interrupt processing flag
( ): Contents of memory addressed by address or register contents in ( )
X_H, X_L: Higher 8 bits and lower 8 bits of 16-bit register
∧: Logical product (AND)
∨: Logical sum (OR)
$\overline{\vee}$: Exclusive logical sum (exclusive OR)
$\overline{\quad}$: Inverted data
addr16: 16-bit immediate data or label
jdisp8: Signed 8-bit data (displacement value)

6.1.3 Explanation of symbols in flag operation field

(Blank): Not affected
0: Cleared to 0
1: Set to 1
×: Set or cleared depending on result
R: Previously saved value is stored

6.2 Operation List

Mnemonic	Operand	Bytes	Clocks	Operation	Flag Z	Flag AC	Flag CY
MOV	r, #byte	3	6	r←byte			
	saddr, #byte	3	6	(saddr)←byte			
	sfr, #byte	3	6	sfr←byte			
	A, r Note 1	2	4	A←r			
	r, A Note 1	2	4	r←A			
	A, saddr	2	4	A←(saddr)			
	saddr, A	2	4	(saddr)←A			
	A, sfr	2	4	A←sfr			
	sfr, A	2	4	sfr←A			
	A, !addr16	3	8	A←(addr16)			
	!addr16, A	3	8	(addr16)←A			
	PSW, #byte	3	6	PSW←byte	×	×	×
	A, PSW	2	4	A←PSW			
	PSW, A	2	4	PSW←A	×	×	×
	A, [DE]	1	6	A←(DE)			
	[DE], A	1	6	(DE)←A			
	A, [HL]	1	6	A←(HL)			
	[HL], A	1	6	(HL)←A			
	A, [HL+byte]	2	6	A←(HL+byte)			
	[HL+byte], A	2	6	(HL+byte)←A			
XCH	A, X	1	4	A↔X			
	A, r Note 2	2	6	A↔r			
	A, saddr	2	6	A↔(saddr)			
	A, sfr	2	6	A↔(sfr)			
	A, [DE]	1	8	A↔(DE)			
	A, [HL]	1	8	A↔(HL)			
	A, [HL+byte]	2	8	A↔(HL+byte)			
MOVW	rp, #word	3	6	rp←word			
	AX, saddrp	2	6	AX←(saddrp)			
	saddrp, AX	2	8	(saddrp)←AX			
	AX, rp Note 3	1	4	AX←rp			
	rp, AX Note 3	1	4	rp←AX			
XCHW	AX, rp Note 3	1	8	AX↔rp			

Notes 1. Except r = A

2. Except r = A, X

3. rp = BC, DE, or HL only

Remark One clock of an instruction is equivalent to one CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
ADD	A, #byte	2	4	A, CY←A+byte	×	×	×
	saddr, #byte	3	6	(saddr), CY←(saddr)+byte	×	×	×
	A, r	2	4	A, CY←A+r	×	×	×
	A, saddr	2	4	A, CY←A+(saddr)	×	×	×
	A, !addr16	3	8	A, CY←A+(addr16)	×	×	×
	A, [HL]	1	6	A, CY←A+(HL)	×	×	×
	A, [HL+byte]	2	6	A, CY←A+(HL+byte)	×	×	×
ADDC	A, #byte	2	4	A, CY←A+byte+CY	×	×	×
	saddr, #byte	3	6	(saddr), CY←(saddr)+byte+CY	×	×	×
	A, r	2	4	A, CY←A+r+CY	×	×	×
	A, saddr	2	4	A, CY←A+(saddr)+CY	×	×	×
	A, !addr16	3	8	A, CY←A+(addr16)+CY	×	×	×
	A, [HL]	1	6	A, CY←A+(HL)+CY	×	×	×
	A, [HL+byte]	2	6	A, CY←A+(HL+byte)+CY	×	×	×
SUB	A, #byte	2	4	A, CY←A–byte	×	×	×
	saddr, #byte	3	6	(saddr), CY←(saddr)–byte	×	×	×
	A, r	2	4	A, C←A–r	×	×	×
	A, saddr	2	4	A, CY←A–(saddr)	×	×	×
	A, !addr16	3	8	A, CY← A–(addr16)	×	×	×
	A, [HL]	1	6	A, CY←A–(HL)	×	×	×
	A, [HL+byte]	2	6	A, CY←A–(HL+byte)	×	×	×
SUBC	A, #byte	2	4	A, CY←A–byte–CY	×	×	×
	saddr, #byte	3	6	(saddr), CY←(saddr)–byte–CY	×	×	×
	A, r	2	4	A, CY←A–r–CY	×	×	×
	A, saddr	2	4	A, CY←A–(saddr)–CY	×	×	×
	A, !addr16	3	8	A, CY←A–(addr16)–CY	×	×	×
	A, [HL]	1	6	A, CY←A–(HL)–CY	×	×	×
	A, [HL+byte]	2	6	A, CY←A–(HL+byte)–CY	×	×	×
AND	A, #byte	2	4	A←A∧byte	×		
	saddr, #byte	3	6	(saddr)←(saddr)∧byte	×		
	A, r	2	4	A←A∧r	×		
	A, saddr	2	4	A←A∧(saddr)	×		
	A, !addr16	3	8	A←A∧(addr16)	×		
	A, [HL]	1	6	A←A∧(HL)	×		
	A, [HL+byte]	2	6	A←A∧(HL+byte)	×		

Remark One clock of an instruction is equivalent to one CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
OR	A, #byte	2	4	A←A∨byte	×		
	saddr, #byte	3	6	(saddr)←(saddr)∨byte	×		
	A, r	2	4	A←A∨r	×		
	A, saddr	2	4	A←A∨ (saddr)	×		
	A, !addr16	3	8	A←A∨(addr16)	×		
	A, [HL]	1	6	A←A∨(HL)	×		
	A, [HL+byte]	2	6	A←A∨(HL+byte)	×		
XOR	A, #byte	2	4	A←A⊻byte	×		
	saddr, #byte	3	6	(saddr)←(saddr)⊻byte	×		
	A, r	2	4	A←A⊻r	×		
	A, saddr	2	4	A←A⊻(saddr)	×		
	A, !addr16	3	8	A←A⊻(addr16)	×		
	A, [HL]	1	6	A←A⊻(HL)	×		
	A, [HL+byte]	2	6	A←A⊻(HL+byte)	×		
CMP	A, #byte	2	4	A–byte	×	×	×
	saddr, #byte	3	6	(saddr)–byte	×	×	×
	A, r	2	4	A–r	×	×	×
	A, saddr	2	4	A–(saddr)	×	×	×
	A, !addr16	3	8	A–(addr16)	×	×	×
	A, [HL]	1	6	A–(HL)	×	×	×
	A, [HL+byte]	2	6	A–(HL+byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY←AX+word	×	×	×
SUBW	AX, #word	3	6	AX, CY←AX–word	×	×	×
CMPW	AX, #word	3	6	AX–word	×	×	×
INC	r	2	4	r←r+1	×	×	
	saddr	2	4	(saddr)←(saddr)+1	×	×	
DEC	r	2	4	r←r–1	×	×	
	saddr	2	4	(saddr)←(saddr)–1	×	×	
INCW	rp	1	4	rp←rp+1			
DECW	rp	1	4	rp←rp–1			
ROR	A, 1	1	2	(CY, A_7←A_0, A_{m-1}←A_m) × 1			×
ROL	A, 1	1	2	(CY, A_0←A_7, A_{m+1}←A_m) × 1			×
RORC	A, 1	1	2	(CY←A_0, A_7←CY, A_{m-1}←A_m) × 1			×
ROLC	A, 1	1	2	(CY←A_7, A_0←CY, A_{m+1}←A_m) × 1			×

Remark One clock of an instruction is equivalent to one CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
SET1	saddr. bit	3	6	(saddr. bit)←1			
	sfr. bit	3	6	sfr. bit←1			
	A. bit	2	4	A. bit←1			
	PSW. bit	3	6	PSW. bit←1	×	×	×
	[HL]. bit	2	10	(HL). bit←1			
CLR1	saddr. bit	3	6	(saddr. bit)←0			
	sfr. bit	3	6	sfr. bit←0			
	A. bit	2	4	A. bit←0			
	PSW. bit	3	6	PSW. bit←0	×	×	×
	[HL]. bit	2	10	(HL). bit←0			
SET1	CY	1	2	CY←1			1
CLR1	CY	1	2	CY←0			0
NOT1	CY	1	2	CY←$\overline{CY}$			×
CALL	!addr16	3	6	(SP−1)←(PC+3)$_H$, (SP−2)←(PC+3)$_L$, PC←addr16, SP←SP−2			
CALLT	[addr5]	1	8	(SP−1)←(PC+1)$_H$, (SP−2)←(PC+1)$_L$, PC$_H$←(00000000, addr5+1), PC$_L$←(00000000, addr5), SP←SP−2			
RET		1	6	PC$_H$← (SP+1), PC$_L$←(SP), SP←SP+2			
RETI		1	8	PC$_H$← (SP+1), PC$_L$←(SP), PSW←(SP+2), SP←SP+3, NMIS←0	R	R	R
PUSH	PSW	1	2	(SP−1)←PSW, SP←SP−1			
	rp	1	4	(SP−1)←rp$_H$, (SP−2)←rp$_L$, SP←SP−2			
POP	PSW	1	4	PSW←(SP), SP←SP+1	R	R	R
	rp	1	6	rp$_H$←(SP+1), rp$_L$← (SP), SP←SP+2			
MOVW	SP, AX	2	8	SP←AX			
	AX, SP	2	6	AX←SP			
BR	!addr16	3	6	PC←addr16			
	$addr16	2	6	PC←PC+2+jdisp8			
	AX	1	6	PC$_H$←A, PC$_L$←X			

Remark One clock of an instruction is equivalent to one CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clocks	Operation	Flag		
					Z	AC	CY
BC	$addr16	2	6	PC←PC+2+jdisp8 if CY = 1			
BNC	$addr16	2	6	PC←PC+2+jdisp8 if CY = 0			
BZ	$addr16	2	6	PC←PC+2+jdisp8 if Z = 1			
BNZ	$addr16	2	6	PC←PC+2+jdisp8 if Z = 0			
BT	saddr. bit, $addr16	4	10	PC←PC+4+jdisp8 if (saddr. bit) = 1			
	sfr. bit, $addr16	4	10	PC←PC+4+jdisp8 if sfr. bit = 1			
	A. bit, $addr16	3	8	PC←PC+3+jdisp8 if A. bit = 1			
	PSW. bit, $addr16	4	10	PC←PC+4+jdisp8 if PSW. bit = 1			
BF	saddr. bit, $addr16	4	10	PC←PC+4+jdisp8 if (saddr. bit) = 0			
	sfr. bit, $addr16	4	10	PC←PC+4+jdisp8 if sfr. bit = 0			
	A. bit, $addr16	3	8	PC←PC+3+jdisp8 if A. bit = 0			
	PSW. bit, $addr16	4	10	PC←PC+4+jdisp8 if PSW. bit = 0			
DBNZ	B, $addr16	2	6	B←B–1, then PC←PC+2+jdisp8 if B ≠ 0			
	C, $addr16	2	6	C←C–1, then PC←PC+2+jdisp8 if C ≠ 0			
	saddr, $addr16	3	8	(saddr)←(saddr)–1, then PC←PC+3+jdisp8 if (saddr) ≠ 0			
NOP		1	2	No Operation			
EI		3	6	IE←1 (Enable Interrupt)			
DI		3	6	IE←0 (Disable Interrupt)			
HALT		1	2	Set HALT Mode			
STOP		1	2	Set STOP Mode			

Remark One clock of an instruction is equivalent to one CPU clock (f_{CPU}) selected by the processor clock control register (PCC).

7. ELECTRICAL SPECIFICATIONS

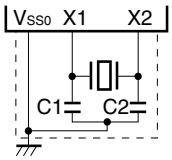
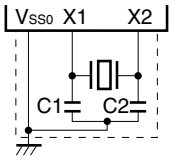
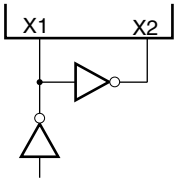
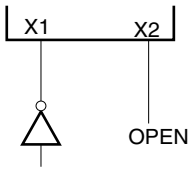
Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}	$AV_{DD} - 0.3\ V \le V_{DD} \le AV_{DD} + 0.3\ V$		−0.3 to +6.5	V
	AV_{DD}	$AV_{REF} \le V_{DD} + 0.3\ V$			
	AV_{REF}	$AV_{REF} \le AV_{DD} + 0.3\ V$			
Input voltage	V_{I1}	Pins other than P50 to P53		−0.3 to V_{DD} + 0.3	V
	V_{I2}	P50 to P53	N-ch open drain	−0.3 to +13	V
Output voltage	V_O			−0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	1 pin		−10	mA
		Total for all pins		−30	mA
Output current, low	I_{OL}	1 pin		30	mA
		Total for all pins		160	mA
Operating ambient temperature	T_A	In normal operation mode		−40 to +85	°C
		During flash memory programming		10 to 40	°C
Storage temperature	T_{stg}			−40 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1	V_{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization timeNote 2	After V_{DD} has reached MIN. of oscillation start voltage			4	ms
Crystal resonator		Oscillation frequency (f_X)Note 1		1.0		5.0	MHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 5.5 V			10	ms
			V_{DD} = 1.8 to 5.5 V			30	ms
External clock		X1 input frequency (f_X)Note 1		1.0		5.0	MHz
		X1 input high-/low-level widths (t_{XH}, t_{XL})		85		500	ns
		X1 input frequency (f_X)Note 1	V_{DD} = 2.7 to 5.5 V	1.0		5.0	MHz
		X1 input high-/low-level widths (t_{XH}, t_{XL})	V_{DD} = 2.7 to 5.5 V	85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator whose oscillation is stabilized within the oscillation wait time.

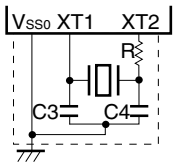
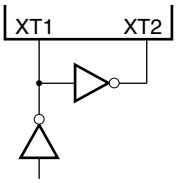
Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})[Note 1]		32	32.768	35	kHz
		Oscillation stabilization time[Note 2]	V_{DD} = 4.5 to 5.5 V		1.2	2	s
			V_{DD} = 1.8 to 5.5 V			10	s
External clock		XT1 input frequency (f_{XT})[Note 1]		32		35	kHz
		XT1 input high-/low-level widths (t_{XTH}, t_{XTL})		14.3		15.6	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator whose oscillation is stabilized within the oscillation wait time.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin				–1	mA
		Total for all pins				–15	mA
Output current, low	I_{OL}	Per pin				10	mA
		Total for all pins				80	mA
Input voltage, high	V_{IH1}	P00 to P03, P46, P47, P60 to P66, P80 to P87, P90 to P93	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P53 N-ch open drain	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		12	V
			V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		12	V
	V_{IH3}	$\overline{RESET}$, P20 to P27, P40 to P45	V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	0.9V_{DD}		V_{DD}	V
	V_{IH4}	X1, X2, XT1, XT2	V_{DD} = 1.8 to 5.5 V	V_{DD}–0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P03, P46, P47, P60 to P66, P80 to P87, P90 to P93	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL2}	P50 to P53	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL3}	$\overline{RESET}$, P20 to P27, P40 to P45	V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
			V_{DD} = 1.8 to 5.5 V	0		0.1V_{DD}	V
	V_{IL4}	X1, X2, XT1, XT2	V_{DD} = 1.8 to 5.5 V	0		0.1	V
Output voltage, high	V_{OH}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD}–1.0			V
		V_{DD} = 1.8 to 5.5 V, I_{OH} = –100 μA		V_{DD}–0.5			V
Output voltage, low	V_{OL1}	Pins other than P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA			1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 400 μA			0.5	V
	V_{OL2}	P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA			1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
Input leakage current, high	I_{LIH1}	V_I = V_{DD}	Pins other than P50 to P53 (N-ch open drain), X1, X2, XT1, and XT2			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_I = 12 V	P50 to P53 (N-ch open drain)			20	μA
Input leakage current, low	I_{LIL1}	V_I = 0 V	Pins other than P50 to P53 (N-ch open drain), X1, X2, XT1, and XT2			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
	I_{LIL3}		P50 to P53 (N-ch open drain)			–3[Note]	μA

Note When P50 to P53 are set in the input mode, a low-level input leakage current of –30 μA (MAX.) flows only for the duration of one cycle time if an instruction to read P50 to P53 is executed. Otherwise, the leakage current of –3 μA (MAX.) flows.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output leakage current, high	I_{LOH}	V_O = V_{DD}				3	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–3	μA
Software pull-up resistor	R_1	V_I = 0 V, pins other than P50 to P53		50	100	200	kΩ
Supply current	I_{DD1} Note 1	5.0 MHz crystal oscillation operating mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		5.0	14.0	mA
			V_{DD} = 3.0 V ±10% Note 5		2.0	5.0	mA
			V_{DD} = 2.0 V ±10% Note 5		1.5	3.0	mA
	I_{DD2} Note 1	5.0 MHz crystal oscillation HALT mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		2.0	6.0	mA
			V_{DD} = 3.0 V ±10% Note 5		1.0	3.0	mA
			V_{DD} = 2.0 V ±10% Note 5		0.7	2.0	mA
	I_{DD3} Note 1	32.768 kHz crystal oscillation operating mode Note 3 (C3 = C4 = 22 pF, R1 = 220 kΩ)	V_{DD} = 5.0 V ±10%		200	600	μA
			V_{DD} = 3.0 V ±10%		150	450	μA
			V_{DD} = 2.0 V ±10%		100	300	μA
	I_{DD4} Note 1	32.768 kHz crystal oscillation HALT mode Note 3 (C3 = C4 = 22 pF, R1 = 220 kΩ)	V_{DD} = 5.0 V ±10%		50	150	μA
			V_{DD} = 3.0 V ±10%		30	90	μA
			V_{DD} = 2.0 V ±10%		20	60	μA
	I_{DD5} Note 1	32.768 kHz crystal oscillation STOP mode	V_{DD} = 5.0 V ±10%		0.1	10	μA
			V_{DD} = 3.0 V ±10%		0.05	5.0	μA
			T_A = 25°C		0.05	3.0	μA
			V_{DD} = 2.0 V ±10%		0.05	3.0	μA
	I_{DD6} Notes 1, 2	5.0 MHz crystal oscillation A/D operation mode (C1 = C2 = 22 pF)	V_{DD} = 5.0 V ±10% Note 4		6.0	16.0	mA
			V_{DD} = 3.0 V ±10% Note 5		3.0	7.0	mA
			V_{DD} = 2.0 V ±10% Note 5		2.5	5.0	mA

Notes 1. The current flowing to the AV_{REF}ON (ADCS0 (bit 7 of A/D converter mode register 0 (ADM0)) = 1) current, AV_{DD} current, and port current (including the current flowing through the on-chip pull-up resistors) is not included.

2. For the current flowing into AV_{REF}, refer to **10-Bit A/D Converter Characteristics**.

3. When main system clock is stopped

4. High-speed mode operation (when processor clock control register (PCC) is set to 00H)

5. Low-speed mode operation (when PCC is set to 02H)

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

LCD Characteristics (T_A = –40 to +85°C, V_{DD} = 2.2 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}	VAON20 = 1		2.2		V_{DD}	V
		VAON20 = 0 Note 1	At 1/3 bias	2.7		V_{DD}	V
			At 1/2 bias	3.0		V_{DD}	V
LCD output voltage deviation Note 2 (common)	V_{ODC}	I_O = ±5 μA	$V_{LCD0} = V_{LCD}$ $V_{LCD1} = V_{LCD} \times 2/3$	0		±0.2	V
LCD output voltage deviation Note 2 (segment)	V_{ODS}	I_O = ±1 μA	2.2 V ≤ V_{LCD} ≤ V_{DD} $V_{LCD2} = V_{LCD} \times 1/3$ Note 1	0		±0.2	V

Notes 1. T_A = –10 to +85°C in the normal mode (VAON20 = 0)

2. Voltage deviation is the voltage difference between the ideal value of a segment or the common output (V_{LCDn}; n = 0 to 2) and output voltage.

Flash Memory Write/Erase Characteristics

(T_A = 10 to 40°C, V_{DD} = 1.8 to 5.5 V, in 5.0 MHz crystal oscillation operating mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Write current Note (V_{DD} pin)	I_{DDW}	When V_{PP} supply voltage = V_{PP1}			18	mA
Write current Note (V_{PP} pin)	I_{PPW}	When V_{PP} supply voltage = V_{PP1}			22.5	mA
Erase current Note (V_{DD} pin)	I_{DDE}	When V_{PP} supply voltage = V_{PP1}			18	mA
Erase current Note (V_{PP} pin)	I_{PPE}	When V_{PP} supply voltage = V_{PP1}			115	mA
Unit erase time	t_{er}		0.5	1	1	s
Total erase time	t_{era}				20	s
Write count		Erase/write are regarded as 1 cycle			20	Times
V_{PP} supply voltage	V_{PP0}	In normal operation	0		0.2V_{DD}	V
	V_{PP1}	During flash memory programming	9.7	10.0	10.3	V

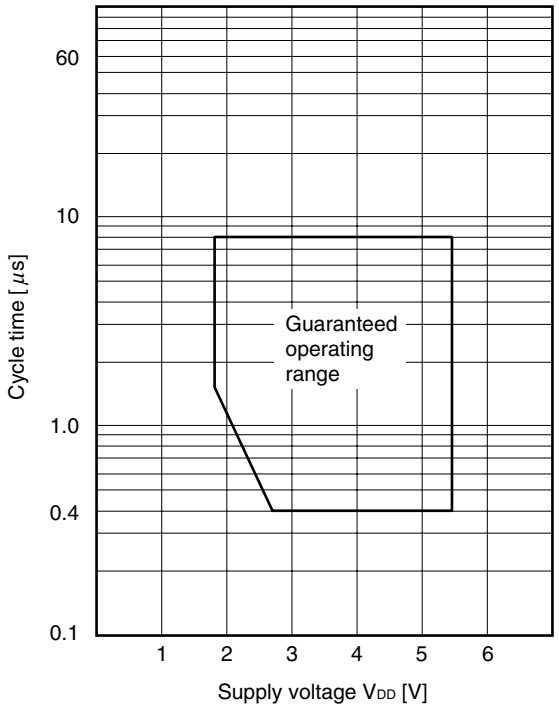
Note The current flowing to the ports (including the current flowing through the on-chip pull-up resistors) is not included.

AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operating with main system clock	V_{DD} = 2.7 to 5.5 V	0.4		8	μs
			V_{DD} = 1.8 to 5.5 V	1.6		8	μs
		Operating with subsystem clock		114	122	125	μs
TI0, TI1 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V		0		4	MHz
		V_{DD} = 1.8 to 5.5 V		0		275	kHz
TI0, TI1 input high-/low-level widths	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V		0.1			μs
		V_{DD} = 1.8 to 5.5 V		1.8			μs
Interrupt input high-/low-level widths	t_{INTH}, t_{INTL}	INTP0 to INTP3		10			μs
$\overline{\text{RESET}}$ input low-level width	t_{RSL}			10			μs

T_{CY} vs V_{DD} (Main system clock)



(2) Serial interface (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode ($\overline{SCK}$ ... Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK}$ high-/low-level widths	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V		t_{KCY1}/2–50			ns
		V_{DD} = 1.8 to 5.5 V		t_{KCY1}/2–150			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
		V_{DD} = 1.8 to 5.5 V		500			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns

Note R and C are the load resistance and load capacitance of the SO output line.

(b) 3-wire serial I/O mode ($\overline{SCK}$ ... External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		900			ns
		V_{DD} = 1.8 to 5.5 V		3500			ns
$\overline{SCK}$ high-/low-level widths	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		1600			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
		V_{DD} = 1.8 to 5.5 V		150			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns

Note R and C are the load resistance and load capacitance of the SO output line.

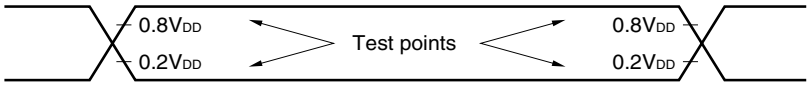
(c) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 2.7 to 5.5 V			78125	bps
		V_{DD} = 1.8 to 5.5 V			19531	bps

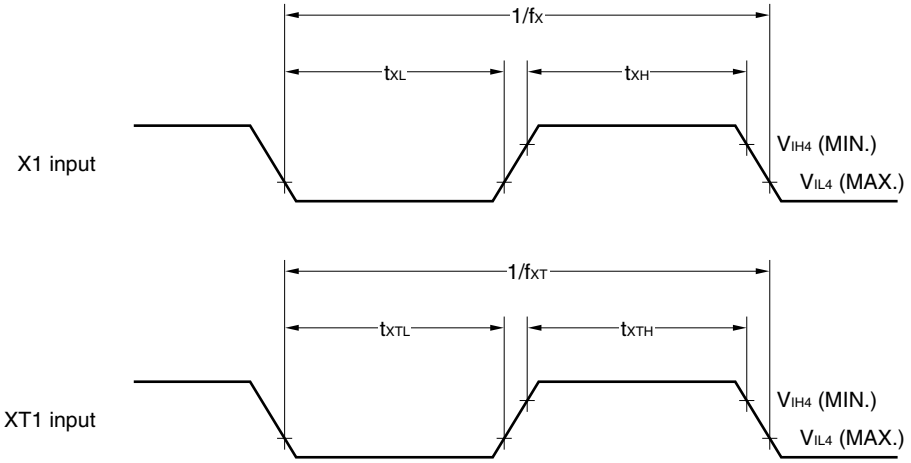
(d) UART mode (External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	900			ns
		V_{DD} = 1.8 to 5.5 V	3500			ns
ASCK high-/low-level widths	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
		V_{DD} = 1.8 to 5.5 V	1600			ns
Transfer rate		V_{DD} = 2.7 to 5.5 V			39063	bps
		V_{DD} = 1.8 to 5.5 V			9766	bps
ASCK rise/fall times	t_R, t_F				1	μs

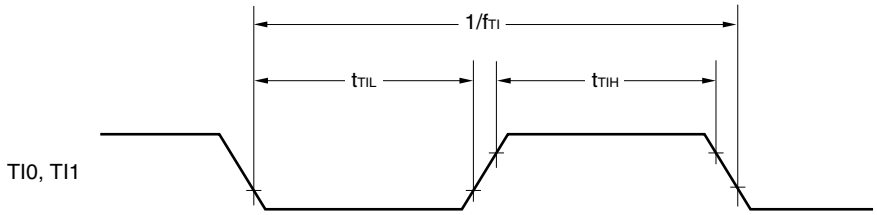
AC Timing Test Points (excluding X1 and XT1 inputs)



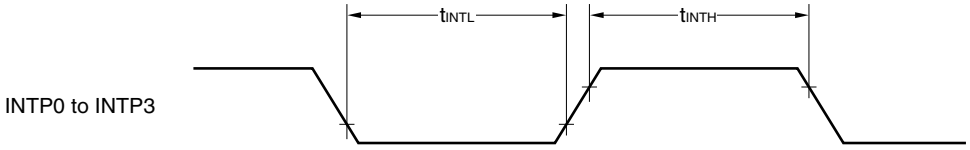
Clock Timing



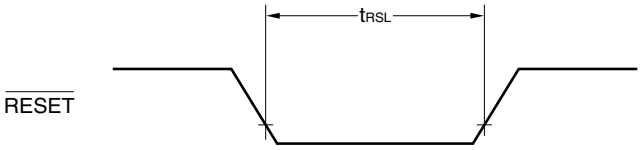
TI Timing



Interrupt Input Timing

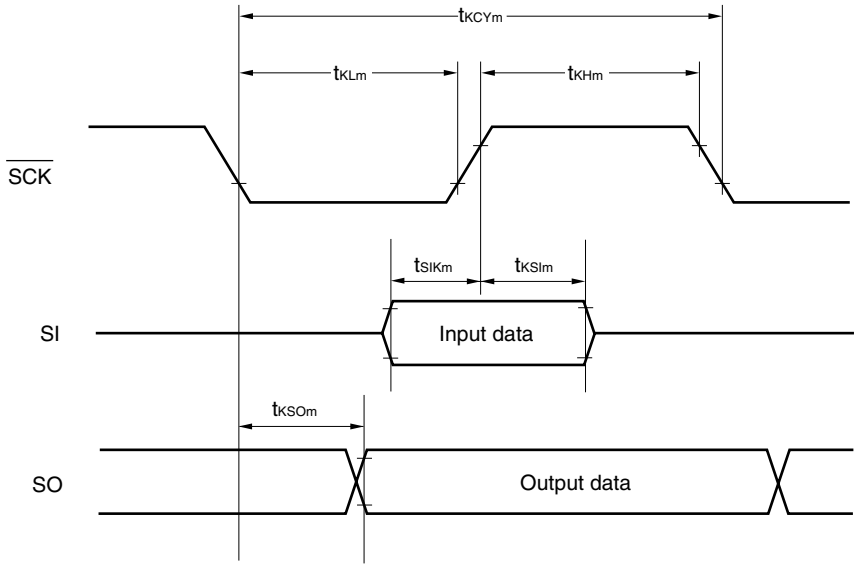


$\overline{\text{RESET}}$ Input Timing



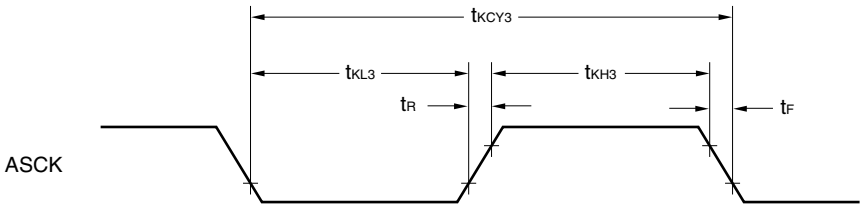
Serial Transfer Timing

3-wire serial I/O mode:



Remark m = 1 or 2

UART mode (external clock input):



10-Bit A/D Converter Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ AV_{REF} ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note]		4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.4	±0.6	%FSR
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.8	±1.2	%FSR
Conversion time	t_{CONV}	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	14		100	μs
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	14		100	μs
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	28		100	μs
Zero-scale error[Note]	AINL	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.2	%FSR
Full-scale error[Note]	AINL	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.6	%FSR
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.2	%FSR
Non-integral linearity[Note]	INL	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±4.5	LSB
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±8.5	LSB
Non-differential linearity[Note]	DNL	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±2.0	LSB
		1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±3.5	LSB
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Reference voltage	AV_{REF}		1.8		AV_{DD}	V
Resistance between AV_{REF} and AV_{SS}	R_{ADREF}		20	40		kΩ

Note Excludes quantization error (±0.05%).

Comparator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Analog input range	V_{CIN}		0		V_{DD}	V
Reference voltage input range	V_{CREF}	V_{DD} = 2.7 to 5.5 V	1.35	1.6	1.85	V
		V_{DD} = 1.8 to 5.5 V	1.35	1.4	1.45	V
Accuracy					±100	mV

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

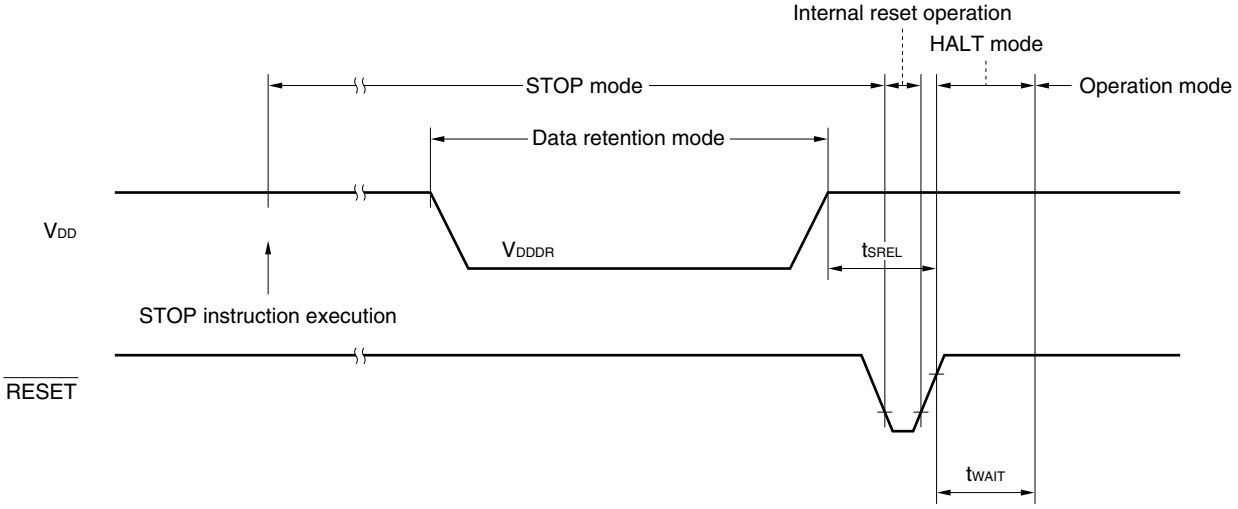
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Release by $\overline{RESET}$		$2^{15}/f_X$		ms
		Release by interrupt request		**Note 2**		ms

Notes 1. The oscillation stabilization wait time is the time after oscillation has started during which the CPU is stopped to prevent unstable operation.

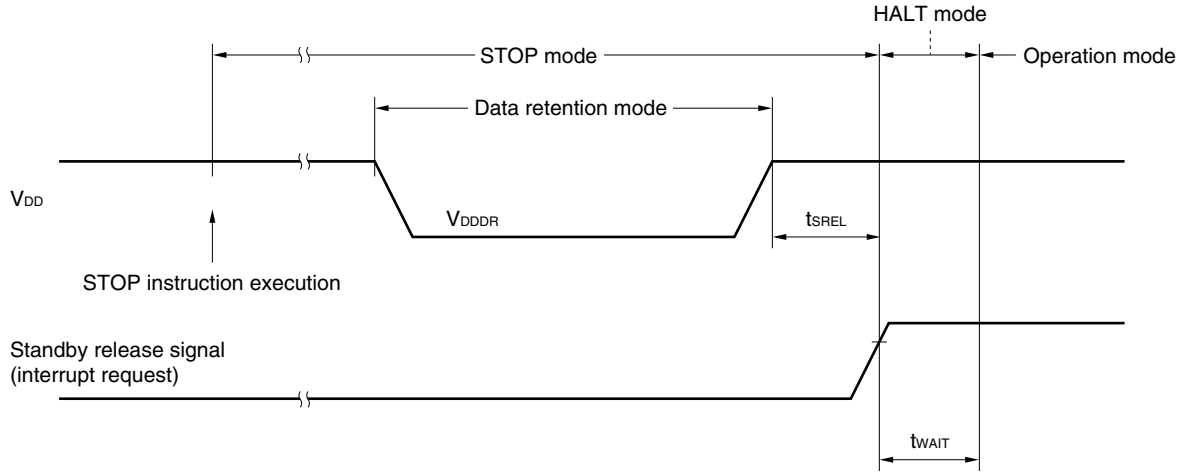
2. Selection of $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

Remark fx: Main system clock oscillation frequency

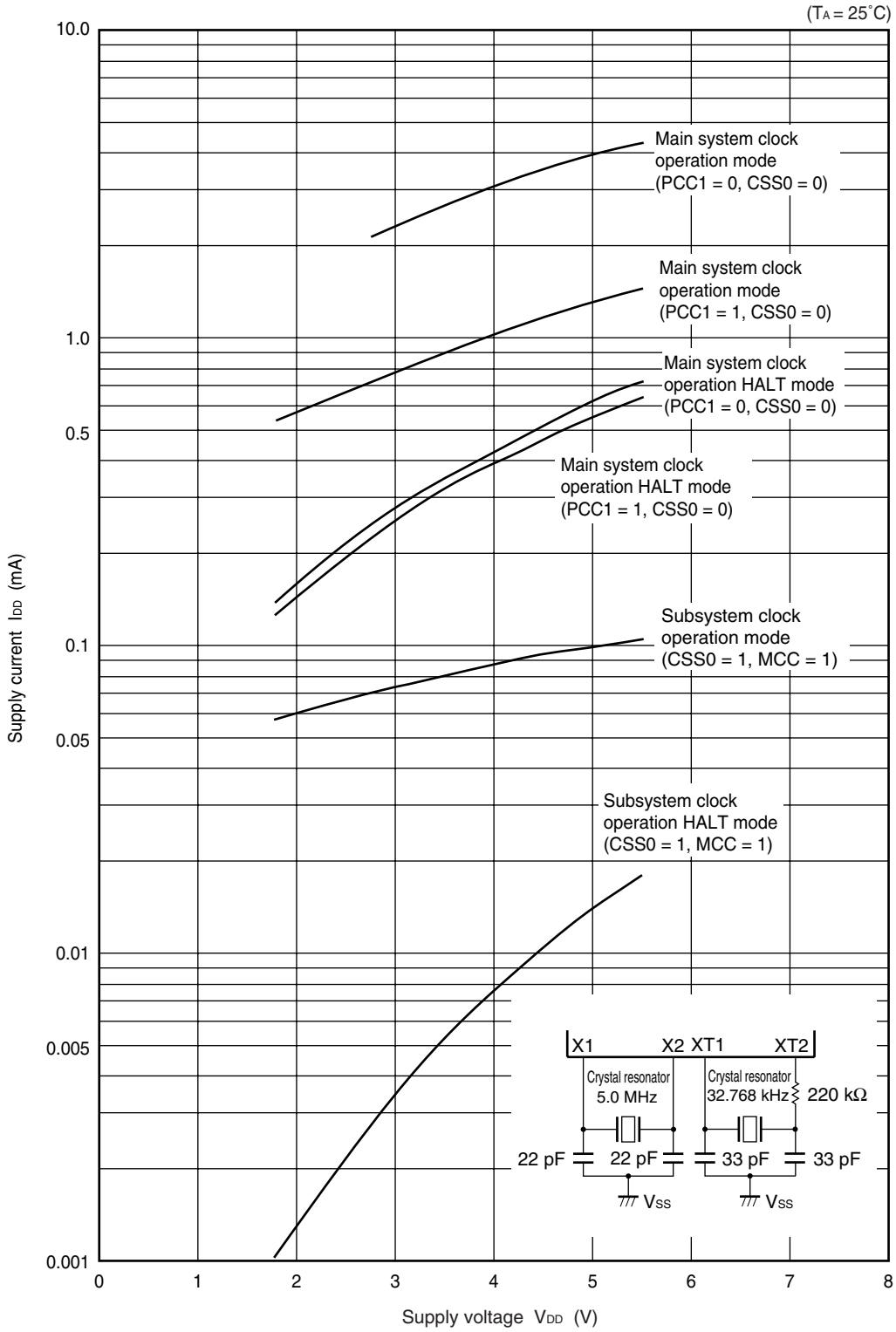
Data Retention Timing (STOP mode release by $\overline{RESET}$)



Data Retention Timing (Standby release signal: STOP mode release by interrupt signal)

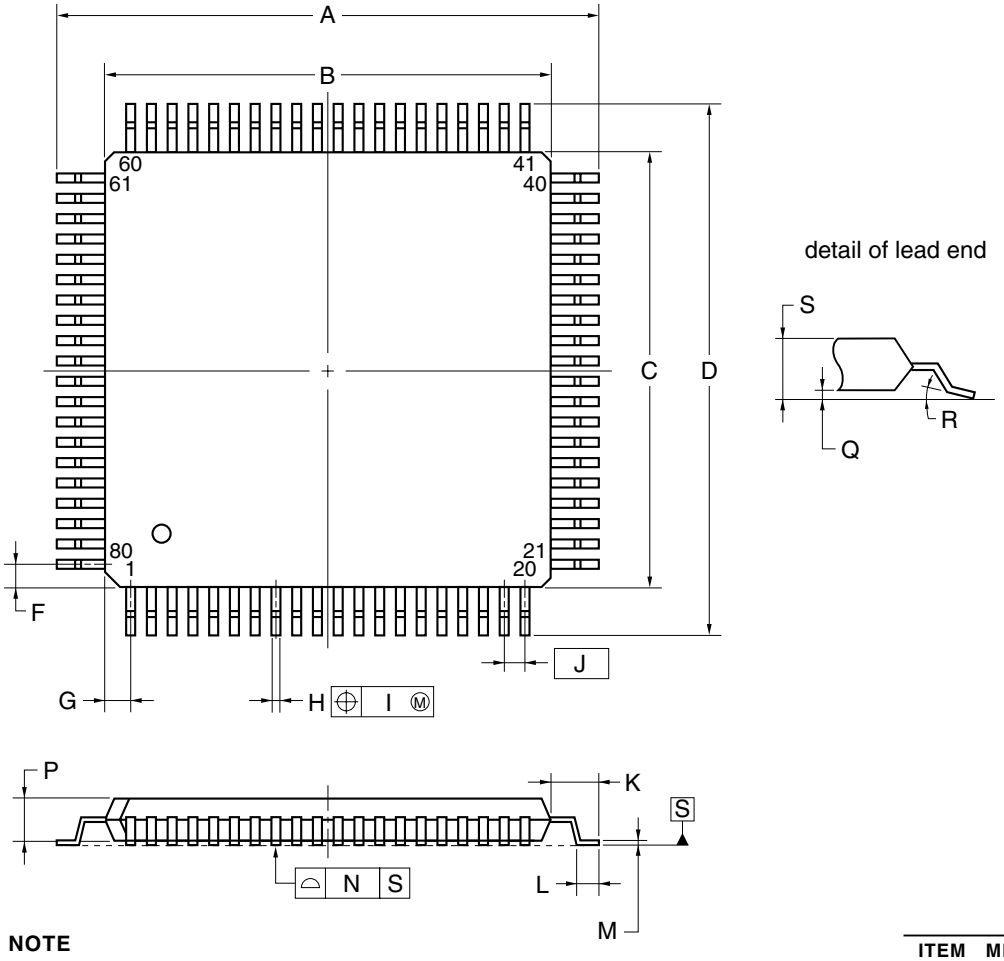


8. CHARACTERISTIC CURVE



9. PACKAGE DRAWINGS

80-PIN PLASTIC QFP (14x14)



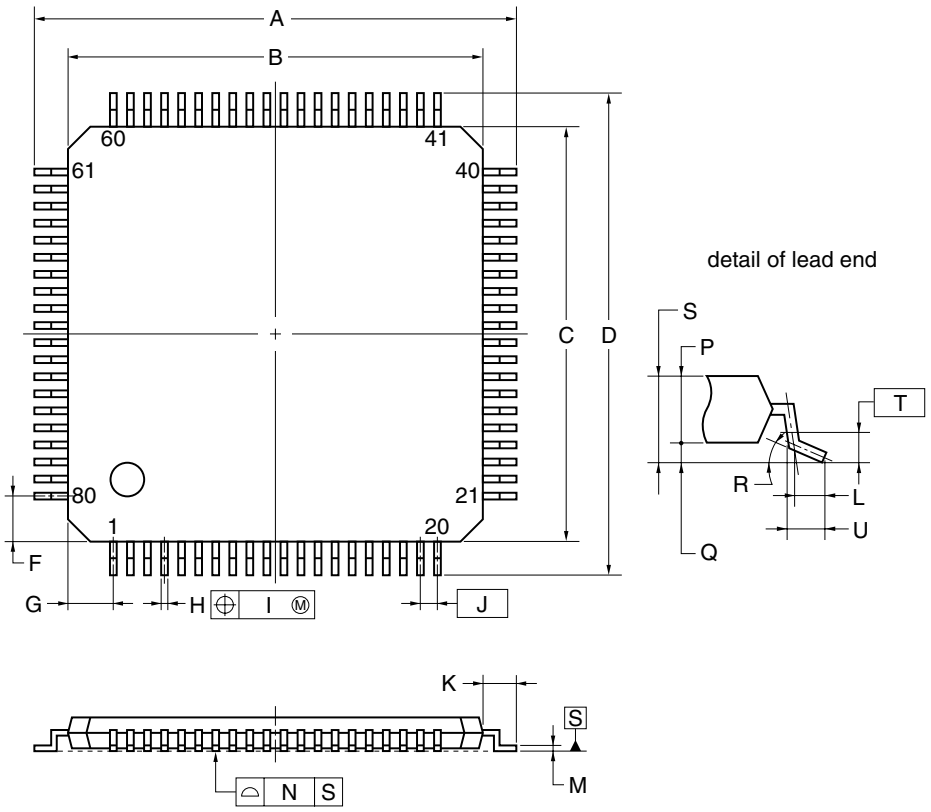
NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.20±0.20
B	14.00±0.20
C	14.00±0.20
D	17.20±0.20
F	0.825
G	0.825
H	0.32±0.06
I	0.13
J	0.65 (T.P.)
K	1.60±0.20
L	0.80±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	1.40±0.10
Q	0.125±0.075
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.70 MAX.

P80GC-65-8BT-1

80-PIN PLASTIC TQFP (FINE PITCH) (12x12)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	14.0±0.2
B	12.0±0.2
C	12.0±0.2
D	14.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5
M	0.145±0.05
N	0.08
P	1.0
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.1±0.1
T	0.25
U	0.6±0.15

P80GK-50-9EU-1

10. RECOMMENDED SOLDERING CONDITIONS

The μPD78F9418A should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 10-1. Surface Mounting Soldering Conditions

(1) μPD78F9418AGC-8BT: 80-pin plastic QFP (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds.max. (at 210°C or higher), Count: Two times or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Caution Do not use different soldering methods together (except for partial heating).

(2) μPD78F9418AGK-9EU: 80-pin plastic TQFP (fine pitch) (12 × 12)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-107-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DIFFERENCES BETWEEN μPD78F9418A AND MASK ROM VERSIONS

The μPD78F9418A has flash memory in place of the internal ROM of the mask ROM versions (μPD789415A, 789416A, and 789417A). Differences between the μPD78F9418A and mask ROM versions are shown in Table A-1.

Table A-1. Differences Between μPD78F9418A and Mask ROM Versions

Parameter		Flash Memory Version	Mask ROM Versions		
		μPD78F9418A	μPD789415A	μPD789416A	μPD789417A
Internal memory	ROM structure	Flash memory	Mask ROM		
	ROM capacity	32 KB	12 KB	16 KB	24 KB
	High-speed RAM capacity	512 bytes			
	LCD display RAM	28 × 4 bits			
Pull-up resistor		32 (software control only)	36 (software control: 32, mask option control: 4)		
Divider resistor for LCD driving		Not available	Can be specified on-chip by mask option		
V_{PP} pin		Available	Not available		
IC pin		Not available	Available		
Electrical specifications		See the relevant data sheet			

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the commercial samples (not engineering samples) of the mask ROM version.

APPENDIX B. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78F9418A.

★ **Software package**

SP78K0S[Notes 1, 2]	CD-ROM in which the development tools (software) common to the 78K/0S Series are included as a package

Language processing software

RA78K0S[Notes 1, 2, 3]	Assembler package common to 78K/0S Series
CC78K0S[Notes 1, 2, 3]	C compiler package common to 78K/0S Series
DF789418[Notes 1, 2, 3]	Device file for μPD789407A and 789417A Subseries

Flash memory writing tools

Flashpro III (Part No. FL-PR3[Note 4], PG-FP3)	Flash programmer for microcontrollers with flash memory
FA-80GC[Note 4]	Flash memory writing adapter for 80-pin plastic QFP (GC-8BT type)
FA-80GK-9EU[Note 4]	Flash memory writing adapter for 80-pin plastic TQFP (fine pitch) (GK-9EU type)

Debugging tools (1/2)

IE-78K0S-NS In-circuit emulator	In-circuit emulator for debugging the hardware and software of the application system using the 78K/0S Series. Supports the integrated debugger (ID78K0S-NS). Used with an AC adapter, emulation probe, and interface adapter that connects the host machine.
★ IE-78K0S-NS-A In-circuit emulator	The IE-78K0S-NS-A provides a coverage function in addition to the IE-78K0S-NS functions, thus enhancing the debug functions, including the tracer and timer functions.
IE-70000-MC-PS-B AC adapter	Adapter that distributes power from an AC 100 to 240 V outlet.
IE-70000-98-IF-C Interface adapter	Adapter necessary when using a PC-9800 series (except notebook type) as the host machine (supports C bus).
IE-70000-CD-IF-A PC card interface	PC card and interface cable necessary when a notebook type personal computer is used as the host machine (supports PCMCIA socket).
IE-70000-PC-IF-C Interface adapter	Adapter necessary when an IBM PC/AT™ or compatible machine is used as the host machine (supports ISA bus).
★ IE-70000-PCI-IF-A Interface adapter	Adapter necessary when using a personal computer with PCI bus is used as the host machine.
IE-789418-NS-EM1 Emulation board	Board for emulating device-specific peripheral hardware. Used with an in-circuit emulator.
NP-80GC[Note 4]	Board for connecting an in-circuit emulator and target system. For 80-pin plastic QFP (GC-8BT type).
NP-80GK[Note 4]	Board for connecting an in-circuit emulator and target system. For 80-pin plastic TQFP (fine pitch) (GK-9EU type).

Notes 1. PC-9800 series (Japanese Windows™) based

2. IBM PC/AT or compatible machine (Japanese/English Windows) based

3. HP9000 series 700™ (HP-UX™) based, SPARCstation™ (SunOS™, Solaris™) based.

4. This is a product of Naito Densei Machida Mfg. Co., Ltd. (Tel: +81-45-475-4191).

Remark The RA78K0S, CC78K0S, SM78K0S, and ID78K0S-NS are used in combination with the DF789418.

Debugging tools (2/2)

SM78K0S[Notes 1, 2]	System simulator common to 78K/0S Series
ID78K0S-NS[Notes 1, 2]	Integrated debugger common to 78K/0S Series
DF789418[Notes 1, 2]	Device file for μPD789407A and 789417A Subseries

Notes 1. PC-9800 series (Japanese Windows) based

2. IBM PC/AT or compatible machine (Japanese/English Windows) based

Remark The RA78K0S, CC78K0S, SM78K0S, and ID78K0S-NS are used in combination with the DF789418.

★ APPENDIX C. RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document No.
μPD789405A, 789406A, 789407A, 789415A, 789416A, 789417A Data Sheet	U14024E
μPD78F9418A Data Sheet	This document
μPD789407A, 789417A Subseries User's Manual	U13952E
78K/0S Series User's Manual Instructions	U11047E

Documents Related to Development Tools (Software) (User's Manuals)

Document Name		Document No.
RA78K0S Assembler Package	Operation	U14876E
	Language	U14877E
	Structured Assembly Language	U11623E
CC78K0S C Compiler	Operation	U14871E
	Language	U14872E
SM78K0S, SM78K0 System Simulator Ver. 2.10 or later	Operation (Windows Based)	U14611E
SM78K Series System Simulator Ver. 2.10 or Later	External Part User Open Interface Specifications	U15006E
ID78K0-NS, ID78K0S-NS Integrated Debugger Ver. 2.20 or Later	Operation (Windows Based)	U14910E
Project Manager Ver. 3.12 or Later (Windows Based)		U14610E

Documents Related to Development Tools (Hardware) (User's Manuals)

Document Name	Document No.
IE-78K0S-NS In-Circuit Emulator	U13549E
IE-78K0S-NS-A In-Circuit Emulator	U15207E
IE-789418-NS-EM1 Emulation Board	U14364E

Documents Related to Flash Memory Writing

Document Name	Document No.
PG-FP3 Flash Memory Programmer User's Manual	U13502E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Other Related Documents

Document Name	Document No.
SEMICONDUCTORS SELECTION GUIDE - Products and Packages -	X13769E
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC do Brasil S.A.
Electron Devices Division
Guarulhos-SP, Brasil
Tel: 11-6462-6810
Fax: 11-6462-6829

NEC Electronics (Europe) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 01
Fax: 0211-65 03 327

• Branch The Netherlands
Eindhoven, The Netherlands
Tel: 040-244 58 45
Fax: 040-244 45 80

• Branch Sweden
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics (France) S.A.
Vélizy-Villacoublay, France
Tel: 01-3067-58-00
Fax: 01-3067-58-99

NEC Electronics (France) S.A.
Representación en España
Madrid, Spain
Tel: 091-504-27-87
Fax: 091-504-28-60

NEC Electronics Italiana S.R.L.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Shanghai, Ltd.
Shanghai, P.R. China
Tel: 021-6841-1138
Fax: 021-6841-1137

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC Electronics Singapore Pte. Ltd.
Novena Square, Singapore
Tel: 253-8311
Fax: 250-3583

J02.3

- **The information in this document is current as of December, 2001. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC semiconductor products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.**
- No part of this document may be copied or reproduced in any form or by any means without prior written consent of NEC. NEC assumes no responsibility for any errors that may appear in this document.
- NEC does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC semiconductor products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of customer's equipment shall be done under the full responsibility of customer. NEC assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC endeavours to enhance the quality, reliability and safety of NEC semiconductor products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC semiconductor products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment, and anti-failure features.
- NEC semiconductor products are classified into the following three quality grades:
  "Standard", "Special" and "Specific". The "Specific" quality grade applies only to semiconductor products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of a semiconductor product depend on its quality grade, as indicated below. Customers must check the quality grade of each semiconductor product before using it in a particular application.

  "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

  The quality grade of NEC semiconductor products is "Standard" unless otherwise expressly specified in NEC's data sheets or data books, etc. If customers wish to use NEC semiconductor products in applications not intended by NEC, they must contact an NEC sales representative in advance to determine NEC's willingness to support a given application.

  (Note)

  (1) "NEC" as used in this statement means NEC Corporation and also includes its majority-owned subsidiaries.

  (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).

M8E 00.4