NEC

MOS INTEGRATED CIRCUIT

μPD78F4225, 78F4225Y

16/8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD78F4225 and 78F4225Y are products in the μPD784225, 784225Y Subseries in the 78K/IV Series.

The μPD78F4225 and 78F4225Y have flash memory in the place of the internal ROM of the μPD784225 and 784225Y. Data can be written to or erased from the flash memory of the μPD78F4225 and 78F4225Y with the microcontroller mounted on a printed wiring board.

The μPD78F4225Y is based on the μPD78F4225 with an I^2C bus interface added supporting multi masters.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD784225, 784225Y Subseries User's Manual Hardware: U12697E
78K/IV Series User's Manual Instruction: U10905E

FEATURES

- Pin-compatible with mask ROM version (except V_{PP} pin)
- Flash memory: 128 KB
- ★ Serial interface: 3 channels
  - UART/IOE (3-wire serial I/O): 2 channels
  - CSI (I^2C bus supporting 3-wire serial I/O multi masters[Note]): 1 channel
- Internal RAM: 4,352 bytes
- ★ Supply voltage: V_{DD} = 1.9 to 5.5 V

Note μPD78F4225Y only

ORDERING INFORMATION

Part Number	Package
μPD78F4225GC-8BT	80-pin plastic QFP (14 × 14)
μPD78F4225GK-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)
μPD78F4225YGC-8BT	80-pin plastic QFP (14 × 14)
μPD78F4225YGK-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)

APPLICATIONS

Car audios, portable audios, telephones, etc.

Unless otherwise specified, descriptions in this document are made using the μPD78F4225Y as the typical product.

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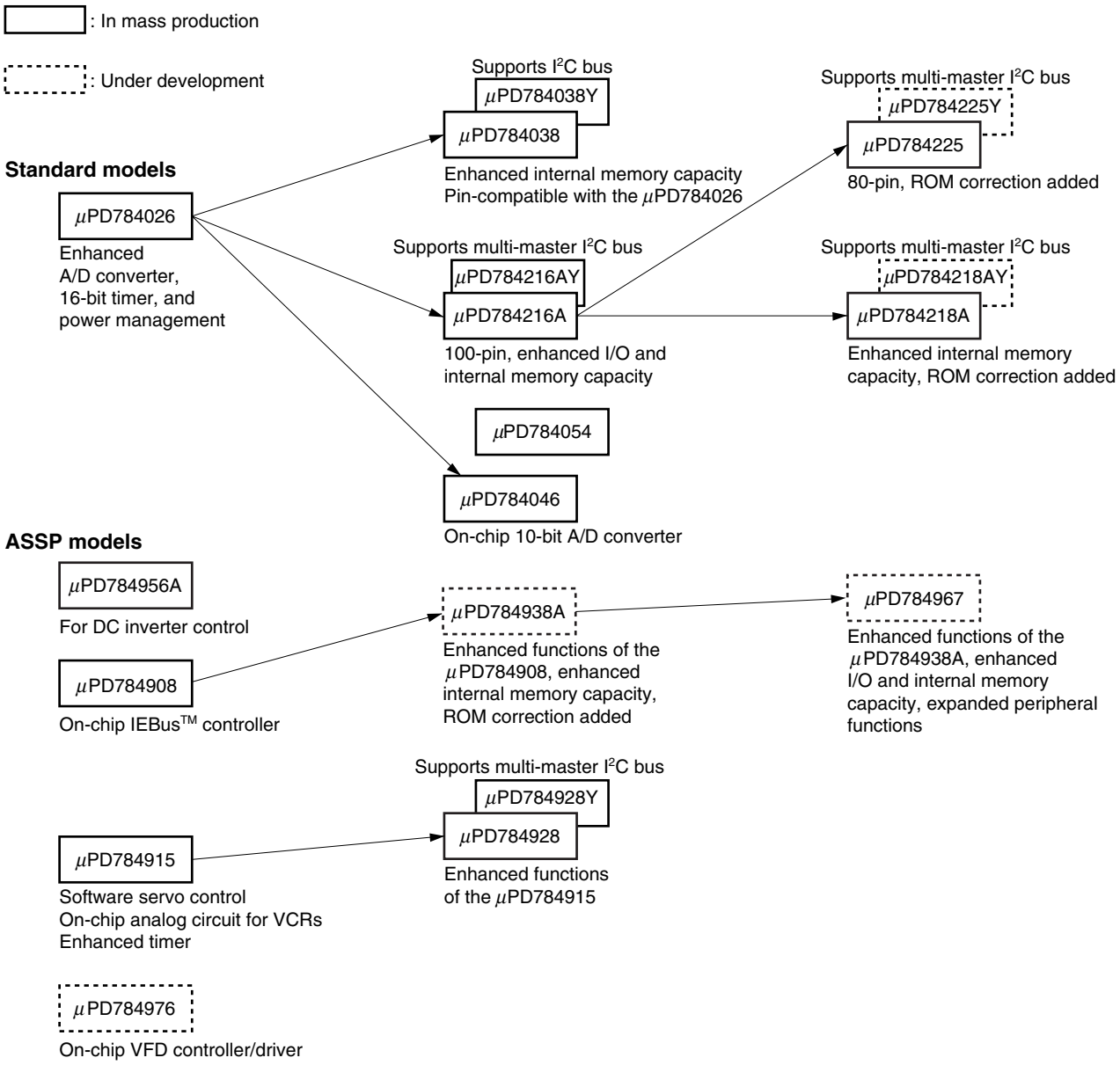
The mark ★ shows major revised points.

★ 78K/IV SERIES LINEUP



OVERVIEW OF FUNCTIONS

Item		Function		
Number of basic instructions (mnemonics)		113		
General-purpose registers		8 bits × 16 registers × 8 banks, or 16 bits × 8 registers × 8 banks (memory mapping)		
Minimum instruction execution time		• 160 ns/320 ns/640 ns/1280 ns/2560 ns (main system clock: f_{XX} = 12.5 MHz) • 61 μs (subsystem clock: f_{XT} = 32.768 kHz)		
Internal memory	Flash memory	128 KB		
	RAM	4,352 bytes		
Memory space		1 MB with program and data spaces combined		
I/O ports	Total	67		
	CMOS input	8		
	CMOS I/O	59		
Pins with ancillary functions[Note 1]	Pins with pull-up resistor	57		
	LEDs direct drive output	16		
Real-time output port		4 bits × 2, or 8 bits × 1		
Timer/counter		Timer/event counter: (16 bits)	timer counter × 1 Capture/compare register × 2	Pulse output • PWM/PPG output • Square wave output • One-shot pulse output
		Timer/event counter 1: (8 bits)	timer counter × 1 Compare register × 1	Pulse output • PWM output • Square wave output
		Timer/event counter 2: (8 bits)	timer counter × 1 Compare register × 1	Pulse output • PWM output • Square wave output
		Timer 5: (8 bits)	timer counter × 1 Compare register × 1	
		Timer 6: (8 bits)	timer counter × 1 Compare register × 1	
Serial interface		• UART/IOE (3-wire serial I/O): 2 channels (on-chip baud rate generator) • CSI (3-wire serial I/O, I^2C bus supporting multi masters[Note 2]): 1 channel		
A/D converter		8-bit resolution × 8 channels		
D/A converter		8-bit resolution × 2 channels		
Clock output		Selectable from f_{XX}, $f_{XX}/2$, $f_{XX}/2^2$, $f_{XX}/2^3$, $f_{XX}/2^4$, $f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$, f_{XT}		
Buzzer output		Selectable from $f_{XX}/2^{10}$, $f_{XX}/2^{11}$, $f_{XX}/2^{12}$, $f_{XX}/2^{13}$		
Watch timer		1 channel		
Watchdog timer		1 channel		
Standby		• HALT/STOP/IDLE mode • In power-saving mode (CPU operation with subsystem clock): HALT/IDLE mode		
Interrupts	Hardware	25 (internal: 18, external: 7)		
	Software	BRK instruction, BRKCS instruction, operand error		
	Non-maskable	Internal: 1, external: 1		
	Maskable	Internal: 17, external: 6		
		• 4 programmable priority levels • 3 servicing modes: vectored interrupt/macro service/context switching		
★ Supply voltage		V_{DD} = 1.9 to 5.5 V		
Package		• 80-pin plastic QFP (14 × 14) • 80-pin plastic TQFP (fine pitch) (12 × 12)		

Notes 1. The pins with ancillary functions are included in the I/O pins.

2. μPD78F4225Y only

CONTENTS

1. DIFFERENCES AMONG PRODUCTS IN μPD784225, 784225Y SUBSERIES

The difference between the μPD784224, 784225, 784224Y, and 784225Y lies in the internal memory capacity. The μPD784224Y and 784225Y are the versions with I^2C bus control added.

The μPD78F4225 and 78F4225Y are provided with a 128 KB flash memory instead of the mask ROM of the above versions. These differences are summarized in Table 1-1.

★ **Table 1-1. Differences Among Products in μPD784225, 784225Y Subseries**

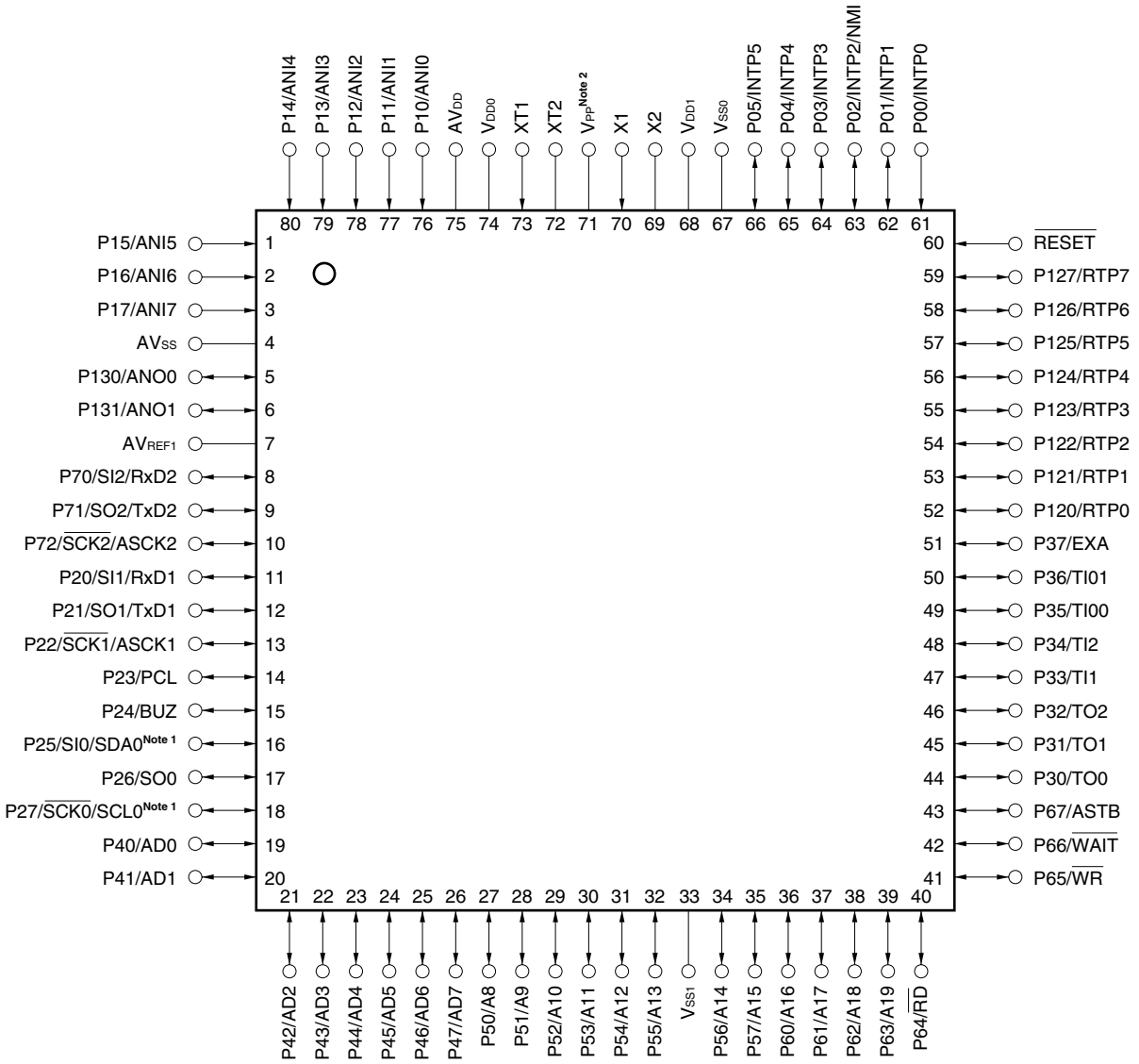
Item \ Part Number	μPD784224, μPD784224Y	μPD784225, μPD784225Y	μPD78F4225, μPD78F4225Y
Internal ROM	96 KB (mask ROM)	128 KB (mask ROM)	128 KB (flash memory)
Internal RAM	3,584 bytes	4,352 bytes	
Internal memory size switching register (IMS)**Note**	None		Provided
Supply voltage	V_{DD} = 1.8 to 4.5 V		V_{DD} = 1.9 to 4.5 V
Electrical specifications	Refer to the relevant data sheet.		
Recommended soldering conditions			
TEST pins	Provided		None
V_{PP} pin	None		Provided

Note Internal flash memory capacity and internal RAM capacity can be changed with the internal memory size switching register (IMS).

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the commercial samples (not engineering samples) of the mask ROM version.

2. PIN CONFIGURATION (TOP VIEW)

- **80-pin plastic QFP (14 × 14)**
  μPD78F4225GC-8BT, 78F4225YGC-8BT
- **80-pin plastic TQFP (fine pitch) (12 × 12)**
  μPD78F4225GK-9EU, 78F4225YGK-9EU



Notes 1. μPD78F4225Y only

2. In normal operation mode, connect V_{PP} pin directly to the V_{SS} pin, or pull it down.
In a system where the internal flash memory is rewritten while mounted on board, pull the V_{PP} pin down.
When pulling down, connection via a 470 kΩ or higher and 10 kΩ or lower resistor is recommended.

Cautions 1. Connect the AV_{DD} pin to V_{DD} pin.

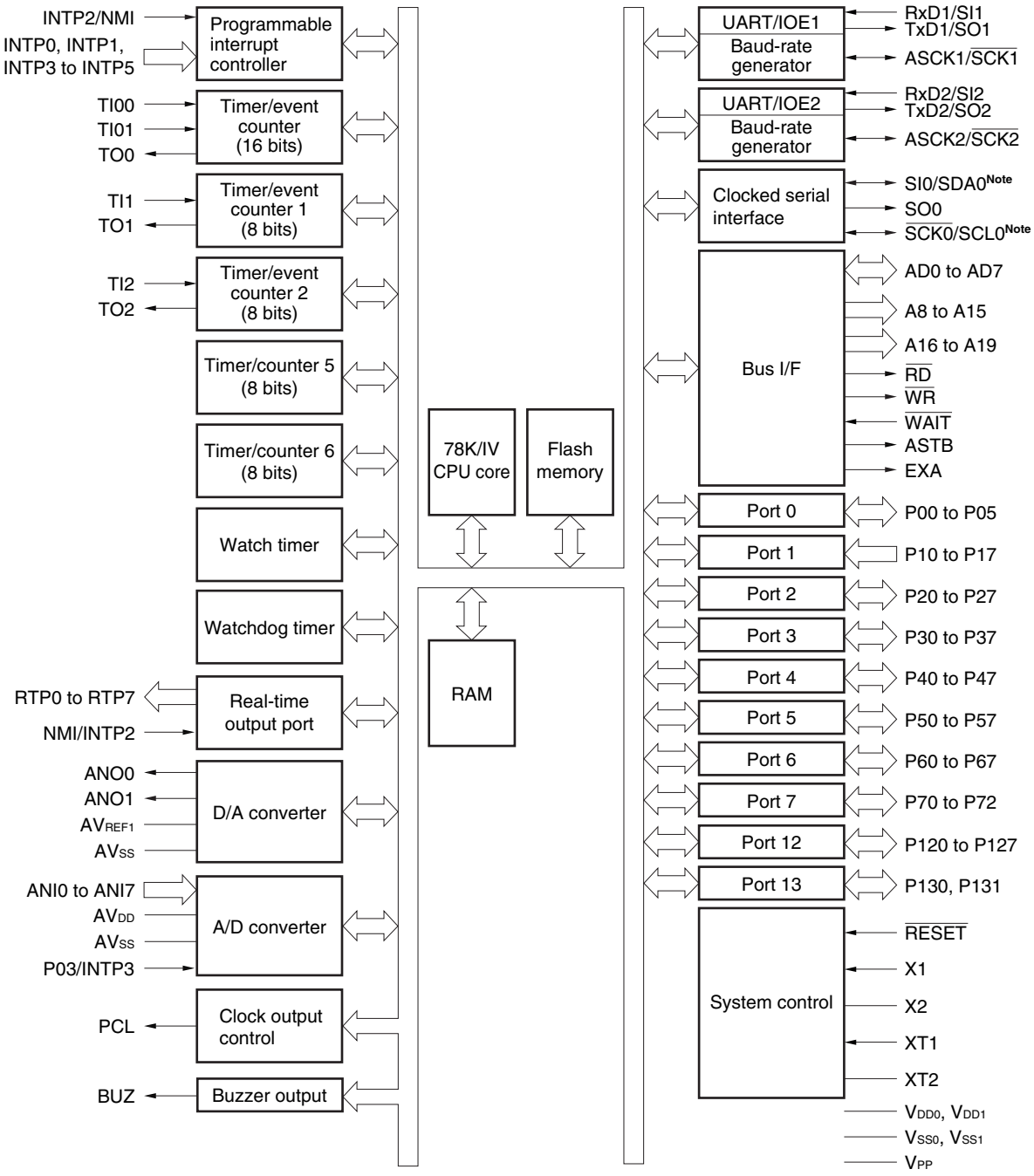
2. Connect the AV_{SS} pin to V_{SS} pin.

Remark When using in applications where noise from inside the microcontroller has to be reduced, it is recommended to take countermeasures against noise such as supplying power to V_{DD0} and V_{DD1} independently, and connecting V_{SS0} and V_{SS1} to different ground lines.

A8 to A19:	Address bus	P130, P131:	Port 13
AD0 to AD7:	Address/data bus	PCL:	Programmable clock
ANI0 to ANI7:	Analog input	$\overline{RD}$:	Read strobe
ANO0, ANO1:	Analog output	$\overline{RESET}$:	Reset
ASCK1, ASCK2:	Asynchronous serial clock	RTP0 to RTP7:	Real-time output port
ASTB:	Address strobe	RxD1, RxD2:	Receive data
AV_{DD}:	Analog power supply	$\overline{SCK0}$ to $\overline{SCK2}$:	Serial clock
AV_{REF1}:	Analog reference voltage	SCL0[Note]:	Serial clock
AV_{SS}:	Analog ground	SDA0[Note]:	Serial data
BUZ:	Buzzer clock	SI0 to SI2:	Serial input
EXA:	External access status output	SO0 to SO2:	Serial output
INTP0 to INTP5:	Interrupt from peripherals	TI00, TI01, TI1, TI2:	Timer input
NMI:	Non-maskable interrupt	TO0 to TO2:	Timer output
P00 to P05:	Port 0	TxD1, TxD2:	Transmit data
P10 to P17:	Port 1	V_{DD0}, V_{DD1}:	Power supply
P20 to P27:	Port 2	V_{PP}:	Programming power supply
P30 to P37:	Port 3	V_{SS0}, V_{SS1}:	Ground
P40 to P47:	Port 4	$\overline{WAIT}$:	Wait
P50 to P57:	Port 5	$\overline{WR}$:	Write strobe
P60 to P67:	Port 6	X1, X2:	Crystal (main system clock)
P70 to P72:	Port 7	XT1, XT2:	Crystal (subsystem clock)
P120 to P127:	Port 12		

Note μPD78F4225Y only

3. BLOCK DIAGRAM



Note μPD78F4225Y only. Supports I^2C bus interface.

4. PIN FUNCTION

4.1 Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function
P00	I/O	INTP0	Port 0 (P0): • 6-bit I/O port • Input/output can be specified in 1-bit units. • Pins set in input mode can be connected to internal pull-up resistors by software in 1-bit units.
P01		INTP1	
P02		INTP2/NMI	
P03		INTP3	
P04		INTP4	
P05		INTP5	
P10 to P17	Input	ANI0 to ANI7	Port 1 (P1): • 8-bit input port
P20	I/O	RxD1/SI1	Port 2 (P2): • 8-bit I/O port • Input/output can be specified in 1-bit units. • Pins set in input mode can be connected to internal pull-up resistors by software in 1-bit units.
P21		TxD1/SO1	
P22		ASCK1/$\overline{\text{SCK1}}$	
P23		PCL	
P24		BUZ	
P25		SI0/SDA0**Note**	
P26		SO0	
P27		$\overline{\text{SCK0}}$/SCL0**Note**	
P30	I/O	TO0	Port 3 (P3): • 8-bit I/O port • Input/output can be specified in 1-bit units. • Pins set in input mode can be connected to internal pull-up resistors by software in 1-bit units.
P31		TO1	
P32		TO2	
P33		TI1	
P34		TI2	
P35		TI00	
P36		TI01	
P37		EXA	
P40 to P47	I/O	AD0 to AD7	Port 4 (P4): • 8-bit I/O port • Input/output can be specified in 1-bit units. • All pins set in input mode can be connected to internal pull-up resistors by software. • Can drive LEDs.
P50 to P57	I/O	A8 to A15	Port 5 (P5): • 8-bit I/O port • Input/output can be specified in 1-bit units. • All pins set in input mode can be connected to internal pull-up resistors by software. • Can drive LEDs.

Note μPD78F4225Y only

4.1 Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
P60	I/O	A16	Port 6 (P6): • 8-bit I/O port • Input/output can be specified in 1-bit units. • All pins set in input mode can be connected to internal pull-up resistors by software.
P61		A17	
P62		A18	
P63		A19	
P64		$\overline{RD}$	
P65		$\overline{WR}$	
P66		$\overline{WAIT}$	
P67		ASTB	
P70	I/O	RxD2/SI2	Port 7 (P7): • 3-bit I/O port • Input/output can be specified in 1-bit units. • Pins set in input mode can be connected to internal pull-up resistor by software in 1-bit units.
P71		TxD2/SO2	
P72		ASCK2/$\overline{SCK2}$	
P120 to P127	I/O	RTP0 to RTP7	Port 12 (P12): • 8-bit I/O port • Input/output can be specified in 1-bit units. • Pins set in input mode can be connected to internal pull-up resistor by software in 1-bit units.
P130, P131	I/O	ANO0, ANO1	Port 13 (P13): • 2-bit I/O port • Input/output can be specified in 1-bit units.

4.2 Non-Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function
TI00	Input	P35	External count clock input to 16-bit timer register
TI01		P36	Capture trigger signal input to capture/compare register 00
TI1		P33	External count clock input to 8-bit timer register 1
TI2		P34	External count clock input to 8-bit timer register 2
TO0	Output	P30	16-bit timer output (shared by 14-bit PWM output)
TO1		P31	8-bit timer output (shared by 8-bit PWM output)
TO2		P32	
RxD1	Input	P20/SI1	Serial data input (UART1)
RxD2		P70/SI2	Serial data input (UART2)
TxD1	Output	P21/SO1	Serial data output (UART1)
TxD2		P71/SO2	Serial data output (UART2)
ASCK1	Input	P22/$\overline{SCK1}$	Baud rate clock input (UART1)
ASCK2		P72/$\overline{SCK2}$	Baud rate clock input (UART2)
SI0	Input	P25/SDA0[Note]	Serial data input (3-wire serial clock I/O0)
SI1		P20/RxD1	Serial data input (3-wire serial clock I/O1)
SI2		P70/RxD2	Serial data input (3-wire serial clock I/O2)
SO0	Output	P26	Serial data output (3-wire serial I/O0)
SO1		P21/TxD1	Serial data output (3-wire serial I/O1)
SO2		P71/TxD2	Serial data output (3-wire serial I/O2)
SDA0	I/O	P25/SI0	Serial data input/output (I^2C bus)
$\overline{SCK0}$	I/O	P27/SCL0[Note]	Serial clock input/output (3-wire serial I/O0)
$\overline{SCK1}$		P22/ASCK1	Serial clock input/output (3-wire serial I/O1)
$\overline{SCK2}$		P72/ASCK2	Serial clock input/output (3-wire serial I/O2)
SCL0		P27/$\overline{SCK0}$	Serial clock input/output (I^2C bus)
NMI	Input	P02/INTP2	Non-maskable interrupt request input
INTP0		P00	External interrupt request input
INTP1		P01	
INTP2		P02/NMI	
INTP3		P03	
INTP4		P04	
INTP5		P05	
PCL	Output	P23	Clock output (for trimming main system clock and subsystem clock)
BUZ	Output	P24	Buzzer output
RTP0 to RTP7	Output	P120 to P127	Real-time output port that outputs data in synchronization with trigger
AD0 to AD7	I/O	P40 to P47	Low-order address/data bus when external memory is connected
A8 to A15	Output	P50 to P57	Middle-order address bus when external memory is connected
A16 to A19		P60 to P63	High-order address bus when external memory is connected
$\overline{RD}$	Output	P64	Strobe signal output for read operation of external memory
$\overline{WR}$		P65	Strobe signal output for write operation of external memory

Note μPD78F4225Y only

4.2 Non-Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
$\overline{WAIT}$	Input	P66	To insert wait state(s) when external memory is accessed
ASTB	Output	P67	Strobe output to externally latch address information output to ports 4 through 6 to access external memory
EXA	Output	P37	External access status output
$\overline{RESET}$	Input	—	System reset input
X1	Input	—	Connecting crystal resonator for main system clock oscillation
X2	—		
XT1	Input	—	Connecting crystal resonator for subsystem clock oscillation
XT2	—		
ANI0 to ANI7	Input	P10 to P17	Analog voltage input for A/D converter
ANO0, ANO1	Output	P130, P131	Analog voltage output for D/A converter
AV_{REF1}	—	—	To apply reference voltage for D/A converter
AV_{DD}			Positive power supply for A/D converter. Connected to V_{DD0}.
AV_{SS}			GND for A/D converter and D/A converter. Connected to V_{SS0}.
V_{DD0}			Positive power supply for port block
V_{SS0}			GND potential for port block
V_{DD1}			Positive power supply (except port block)
V_{SS1}			GND potential (except port block)
★ V_{PP}		—	Sets flash memory programming mode. For high voltage application when program is written or verified. In normal operation mode, connect V_{PP} pin directly to the V_{SS} pin, or pull it down. In a system where the internal flash memory is rewritten while mounted on board, pull the V_{PP} pin down. When pulling down, connection via a 470 kΩ or higher and 10 kΩ or lower resistor is recommended.

4.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit types of each pin and the recommended connection of unused pins are shown in Table 4-1. For the I/O circuit configuration of each type, refer to **Figure 4-1**.

★ **Table 4-1. Pin I/O Circuits and Recommended Connection of Unused Pins (1/2)**

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0	8-K	I/O	Input : Independently connect to V_{SS0} via a resistor Output: Leave open
P01/INTP1			
P02/INTP2/NMI			
P03/INTP3 to P05/INTP5			
P10/ANI0 to P17/ANI7	9	Input	Connect to V_{SS0} or V_{DD0}
P20/RxD1/SI1	10-I	I/O	Input : Independently connect to V_{SS0} via a resistor Output: Leave open
P21/TxD1/SO1	10-J		
P22/ASCK1/$\overline{SCK1}$	10-I		
P23/PCL	10-J		
P24/BUZ			
P25/SDA0[Note]/SI0	10-I		
P26/SO0	10-J		
P27/SCL0[Note]/$\overline{SCK0}$	10-I		
P30/TO0 to P32/TO2	8-M		
P33/TI1, P34/TI2	8-K		
P35/TI00, P36/TI01	8-L		
P37/EXA	8-M		
P40/AD0 to P47/AD7	5-H		
P50/A8 to P57/A15			
P60/A16 to P63/A19			
P64/$\overline{RD}$			
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
P70/RxD2/SI2	8-K		
P71/TxD2/SO2	8-L		
P72/ASCK2/$\overline{SCK2}$	8-K		
P120/RTP0 to P127/RTP7			
P130/ANO0, P131/ANO1	12-D		

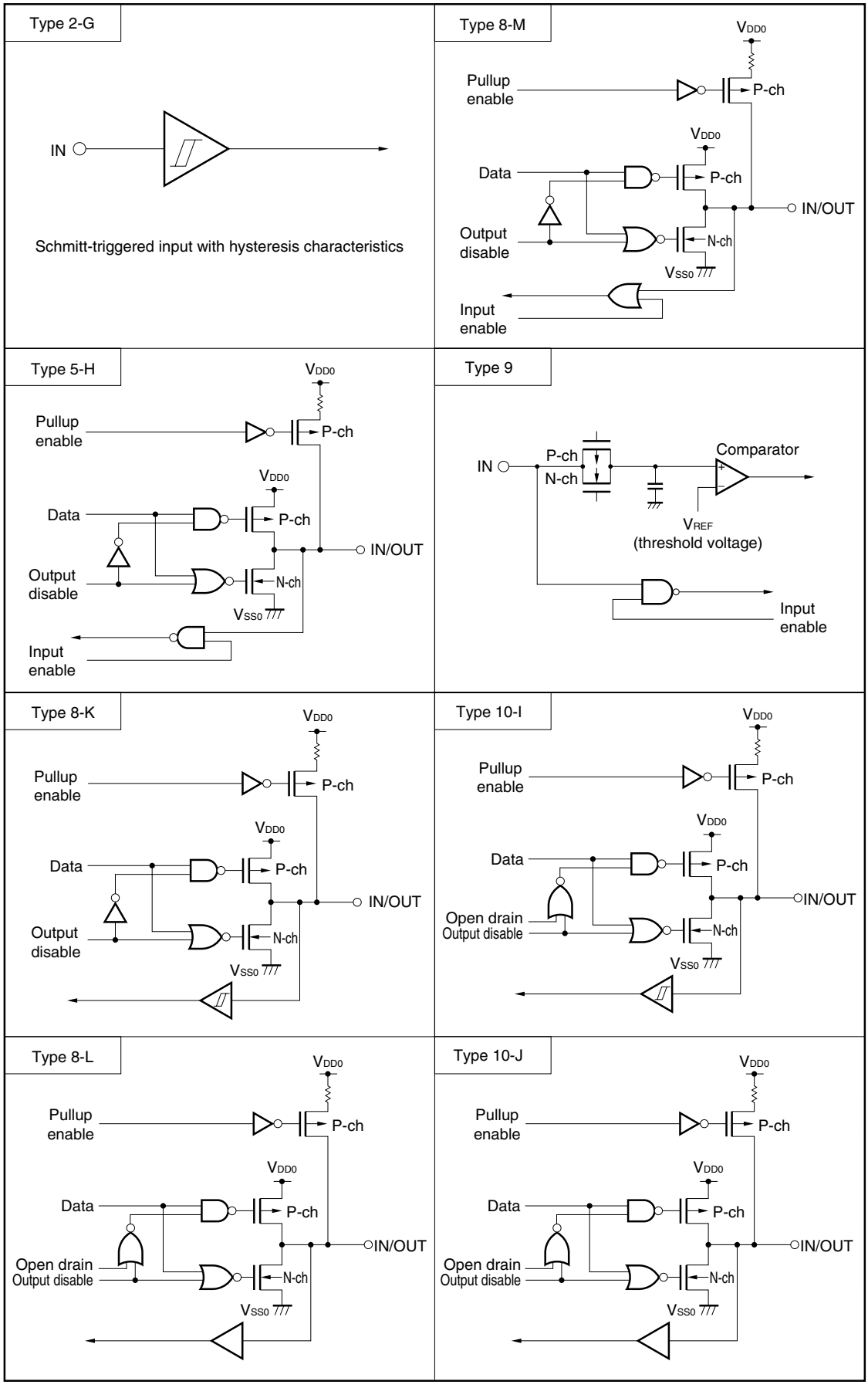
Note μPD78F4225Y only

Table 4-1. Pin I/O Circuits and Recommended Connection of Unused Pins (2/2)

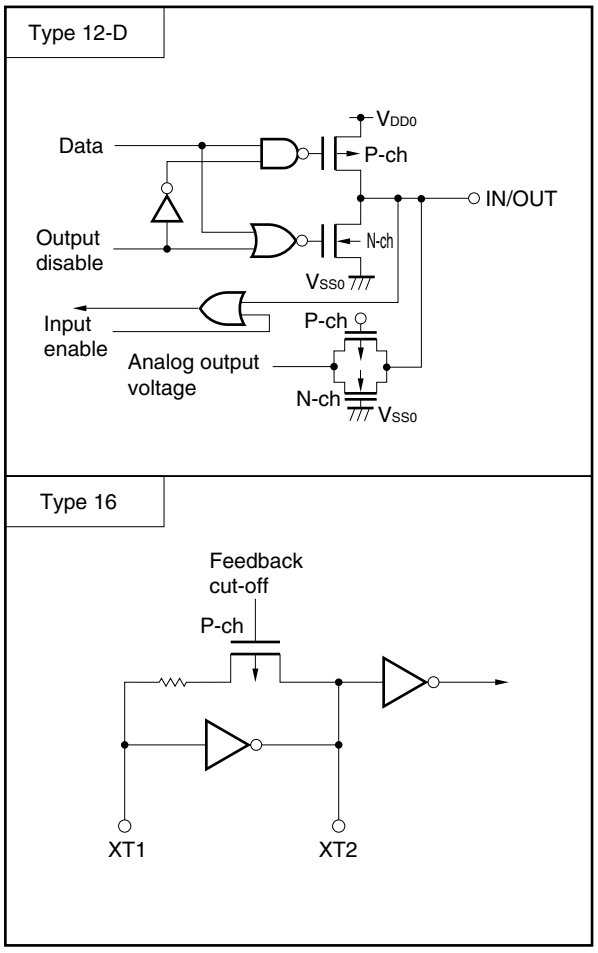
Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
$\overline{\text{RESET}}$	2-G	Input	—
XT1	16		Connect to V_{SS0}
XT2		—	Leave open
AV_{REF1}	—		Connect to V_{DD0}
AV_{DD}			
AV_{SS}			Connect to V_{SS0}
V_{PP}			Directly connect to V_{SS0}

Remark Because the circuit type numbers are standardized among the 78K Series products, they are not sequential in some models (i.e., some circuits are not provided).

★ **Figure 4-1. Types of Pin I/O Circuits (1/2)**



★ **Figure 4-1. Types of Pin I/O Circuits (2/2)**



5. INTERNAL MEMORY SIZE SWITCHING REGISTER (IMS)

IMS is a register that prevents by software a part of the internal memory from being used. By using this register, the memory of the μPD78F4225Y can be mapped in the same manner as a mask ROM version with a different internal memory (ROM and RAM) capacity.

This register is set by using an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets IMS to FFH.

Figure 5-1. Format of Internal Memory Size Switching Register (IMS)

Address: 0FFFCH After reset: FFH W

	7	6	5	4	3	2	1	0
IMS	1	1	ROM1	ROM0	1	1	RAM1	RAM0

ROM1	ROM0	Internal ROM capacity selection
0	0	48 KB
0	1	64 KB
1	0	96 KB
1	1	128 KB

RAM1	RAM0	Peripheral RAM capacity selection
0	0	1,536 bytes
0	1	2,304 bytes
1	0	3,072 bytes
1	1	3,840 bytes

Caution IMS is not provided in the mask ROM versions (μPD784224, 784225, 784224Y, and 784225Y).

The value to be set to IMS to map the memory of the μPD78F4225Y in the same manner as the mask ROM version is shown in Table 5-1.

Table 5-1. Setting Value of Internal Memory Size Switching Register (IMS)

Mask ROM Version	Setting Value of IMS
μPD784224, 784224Y	EEH
μPD784225, 784225Y	FFH

★ 6. PROGRAMMING FLASH MEMORY

The flash memory can be written with the μPD78F4225Y mounted on the target board (on-board). To do so, connect a dedicated flash programmer (Flashpro III (Part No.: FL-PR3, PG-FR3)) to the host machine and target system.

Writing to the flash memory can be performed on the flash memory writing adapter connected to Flashpro III.

Remark FL-PR3 is a product of Naito Densei Machida Mfg. Co., Ltd.

6.1 Selecting Communication Mode

To write the flash memory, use Flashpro III and serial communication. Select a serial communication mode from those listed in Table 6-1 in the format shown in Figure 6-1. Each communication mode is selected by the number of V_{PP} pulses shown in Table 6-1.

★ **Table 6-1. Communication Modes**

Communication Mode	Number of Channels	Pins Used[Note 1]	Number of V_{PP} Pulses
3-wire serial I/O	3	$\overline{SCK0}$/P27/SCL0[Note 2] SO0/P26 SI0/P25/SDA0[Note 2]	0
		$\overline{SCK1}$/ASCK1/P22 SO1/TxD1/P21 SI1/RxD1/P20	1
		$\overline{SCK2}$/ASCK2/P72 SO2/TxD2/P71 SI2/RxD2/P70	2
3-wire serial I/O (handshake[Note 3])	1	$\overline{SCK0}$/P27/SCL0[Note 2] SO0/P26 SI0/P25/SDA0[Note 2] P24/BUZ	3
UART	2	TxD1/SO1/P21 RxD1/SI1/P20	8
		TxD2/SO2/P71 RxD2/SI2/P70	9

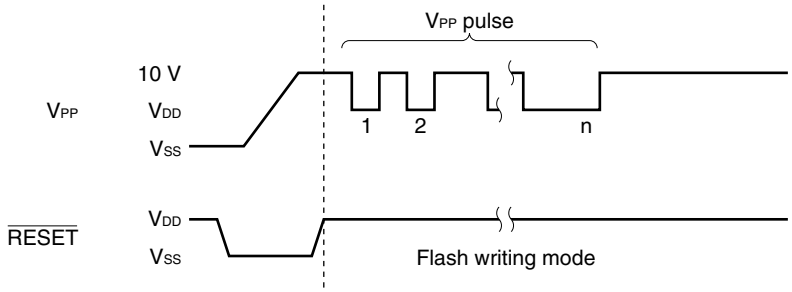
Notes 1. Shifting to the flash memory programming mode sets all pins not used for flash memory programming to the same state as immediately after reset. Therefore, if the external devices do not acknowledge the port state immediately after reset, handling such as connecting to V_{DD} via a resistor or connecting to V_{SS} via a resistor is required.

2. μPD78F4225Y only

3. Other than I, K standards

Caution Be sure to select a communication mode with the number of V_{PP} pulses shown in Table 6-1.

★ **Figure 6-1. Communication Mode Selection Format**



6.2 Flash Memory Programming Function

The flash memory is written by transferring or receiving commands and data in the selected communication mode. The major functions of flash memory programming are listed in Table 6-2.

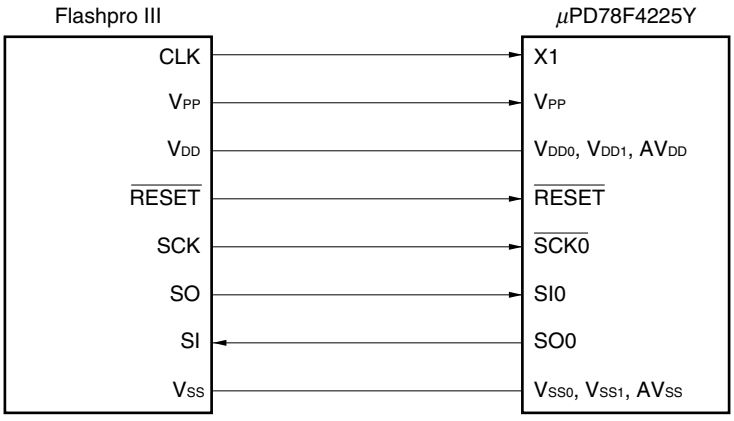
★ **Table 6-2. Major Functions of Flash Memory Programming**

Function	Description
Area erasure	Erases contents of specified memory area.
Area blank check	Checks erased status of specified area.
Data write	Writes flash memory based on write start address and number of data to be written (in bytes).
Area verify	Compares contents of specified memory area with input data.

6.3 Connecting Flashpro III

The Flashpro III and μPD78F4225Y are connected differently depending on the selected communication mode. Figures 6-2 to 6-5 show the connections in the respective communication modes.

Figure 6-2. Connection of Flashpro III in 3-Wire Serial I/O Mode (When Using 3-Wire Serial I/O 0)



★ **Figure 6-3. Connection of Flashpro III in 3-Wire Serial I/O Mode (When Using Handshake)**

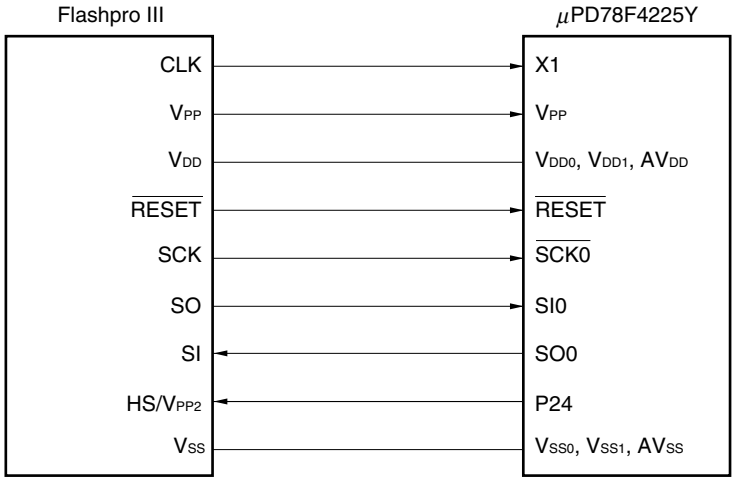
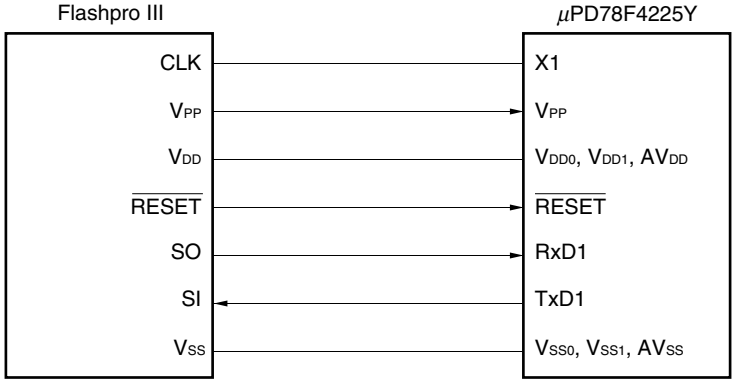


Figure 6-4. Connection of Flashpro III in UART Mode (When Using UART1)



★ 7. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

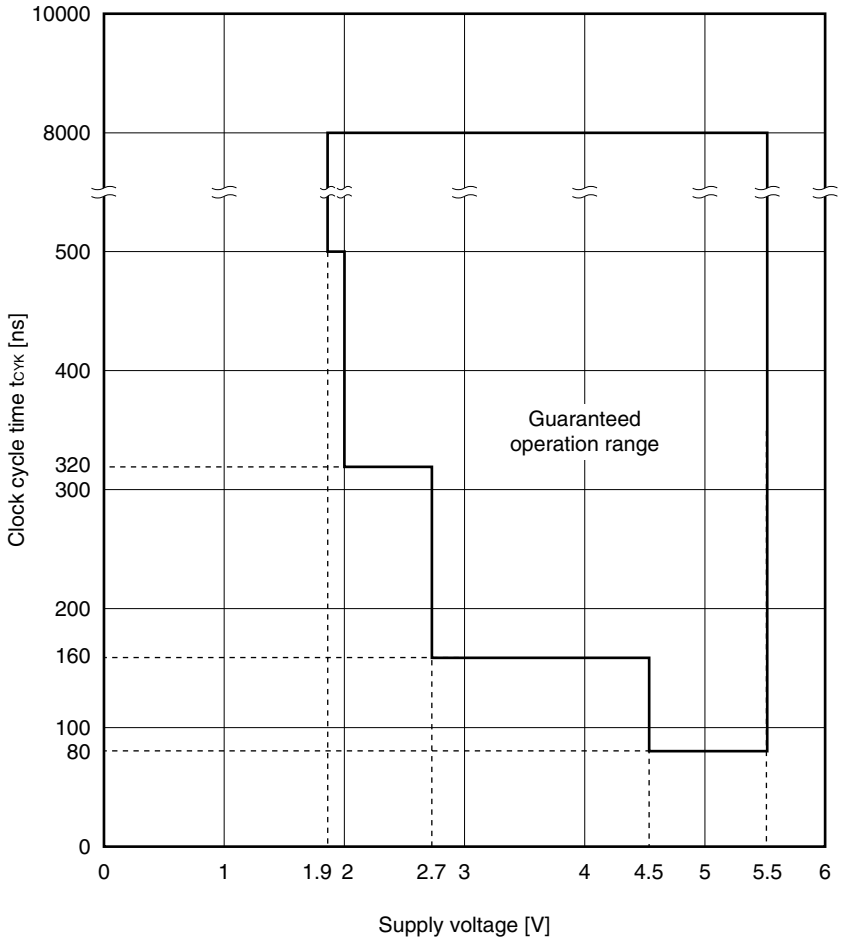
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD0}		–0.3 to +6.5	V
	V_{DD1}		–0.3 to +6.5	V
	V_{PP}		–0.3 to +10.5	V
	AV_{DD}		–0.3 to V_{DD0} + 0.3	V
	AV_{SS}		–0.3 to V_{SS0} + 0.3	V
	AV_{REF1}	D/A converter reference voltage input	–0.3 to V_{DD0} + 0.3	V
Input voltage	V_{I1}		–0.3 to V_{DD0} + 0.3	V
	V_{I2}	V_{PP} pin during programming	–0.3 to +10.5	V
Analog input voltage	V_{AN}	Analog input pin	AV_{SS} – 0.3 to AV_{REF1} + 0.3	V
Output voltage	V_O		–0.3 to V_{DD} + 0.3	V
Output current, low	I_{OL}	Per pin	15	mA
		Total for all pins	100	mA
Output current, high	I_{OH}	Per pin	–10	mA
		Total for all pins	–40	mA
Operating ambient temperature	T_A	During normal operation	–40 to +85	°C
		During flash memory programming	+10 to +40	°C
Storage temperature	T_{stg}		–65 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Operating Conditions

- Operating ambient temperature (T_A): –40 to +85°C
- Power supply voltage and clock cycle time: See **Figure 7-1**
- Operating voltage during the subsystem clock operation: V_{DD} = 1.9 to 5.5 V

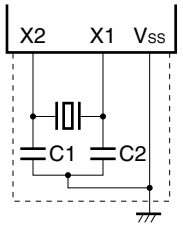
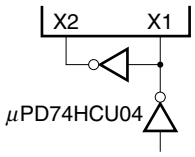
Figure 7-1. Power Supply Voltage and Clock Cycle Time (CPU Clock Frequency: f_{CPU})



Capacitance (T_A = 25°C, V_{DD} = V_{DD0} = V_{DD1} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz			15	pF
Output capacitance	C_O	Unmeasured pins returned to 0 V.			15	pF
I/O capacitance	C_{IO}				15	pF

Main System Clock Oscillator Characteristics (T_A = −40 to +85°C, V_{DD} = V_{DD0} = V_{DD1})

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator or crystal resonator		Oscillation frequency (f_X)	4.5 V ≤ V_{DD} ≤ 5.5 V	2		12.5	MHz
			2.7 V ≤ V_{DD} < 4.5 V	2		6.25	
			2.0 V ≤ V_{DD} < 2.7 V	2		3.125	
			1.9 V ≤ V_{DD} < 2.0 V	2		2	
External clock		X1 input frequency (f_X)	4.5 V ≤ V_{DD} ≤ 5.5 V	2		12.5	MHz
			2.7 V ≤ V_{DD} < 4.5 V	2		6.25	
			2.0 V ≤ V_{DD} < 2.7 V	2		3.125	
			1.9 V ≤ V_{DD} < 2.0 V	2		2	
		X1 input high-/low-level width (t_{WXH}, t_{WXL})		15		250	ns
		X1 input rise/fall time (t_{XR}, t_{XF})	4.5 V ≤ V_{DD} ≤ 5.5 V	0		5	ns
			2.7 V ≤ V_{DD} < 4.5 V	0		10	
			2.0 V ≤ V_{DD} < 2.7 V	0		20	
			1.9 V ≤ V_{DD} < 2.0 V	0		30	

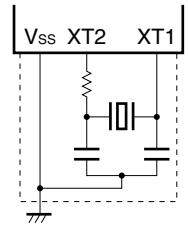
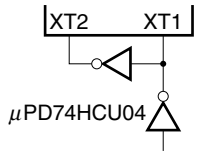
Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark For the resonator selection and oscillator constant, customers are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem Clock Oscillator Characteristics (T_A = −40 to +85°C, V_{DD} = V_{DD0} = V_{DD1})

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})		32	32.768	35	kHz
		Oscillation stabilization time[Note]	4.5 V ≤ V_{DD} ≤ 5.5 V		1.2	2	s
			1.9 V ≤ V_{DD} < 4.5 V			10	
External clock		XT1 input frequency (f_{XT})		32		35	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		14.3		15.6	μs

Note Time required to stabilize oscillation after applying supply voltage (V_{DD}).

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark For the resonator selection and oscillator constant, customers are required to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Recommended Oscillator Constant

Main system clock resonator (T_A = –40 to +85°C)

Manufacturer	Part Number	Oscillation Frequency f_{XX} (MHz)	Recommended Circuit Constant		Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) Tost (ms)
			C1 (pf)	C2 (pf)	MIN. (V)	MAX. (V)	
Murata Mfg. Co., Ltd.	CSTLS2M00G56-B0	2.0	On-chip	On-chip	1.9	5.5	0.44
	CSTCC2.00MG0H6	2.0	On-chip	On-chip	1.9	5.5	0.40
	CSTCR4M00G55-R0	4.0	On-chip	On-chip	2.7	5.5	0.38
	CSTS0400MG06	4.0	On-chip	On-chip	2.7	5.5	0.40
	CSTCC4.00MG0H6	4.0	On-chip	On-chip	2.7	5.5	0.38
	CSTCR6M00G53-R0	6.0	On-chip	On-chip	2.7	5.5	0.28
	CSTS0600MG03	6.0	On-chip	On-chip	2.7	5.5	0.24
	CSTCC6.00MG	6.0	On-chip	On-chip	2.7	5.5	0.23
	CSTS0800MG03	8.0	On-chip	On-chip	4.5	5.5	0.22
	CSTCC8.00MG	8.0	On-chip	On-chip	4.5	5.5	0.22
	CSTS1000MG03	10.0	On-chip	On-chip	4.5	5.5	0.23
	CSTCC10.0MG	10.0	On-chip	On-chip	4.5	5.5	0.22
	CSA12.5MTZ	12.5	30	30	4.5	5.5	0.24
	CST12.5MTW	12.5	On-chip	On-chip	4.5	5.5	0.24
	CSTCV12.5MTJ0C4	12.5	On-chip	On-chip	4.5	5.5	0.22
Kyocera Corporation	PBRC4.00HR	4.0	On-chip	On-chip	2.7	5.5	0.3
	PBRC4.00GR	4.0	33	33	2.7	5.5	0.3
	KBR-4.0MKC	4.0	On-chip	On-chip	2.7	5.5	0.3
	KBR-4.0MSB	4.0	33	33	2.7	5.5	0.3
	PBRC8.00HR	8.0	On-chip	On-chip	4.5	5.5	0.3
	PBRC8.00GR	8.0	33	33	4.5	5.5	0.3
	KBR-8.0MKC	8.0	On-chip	On-chip	4.5	5.5	0.3
	KBR-8.0MSB	8.0	33	33	4.5	5.5	0.3
	PBRC10.00BR-A	10.0	On-chip	On-chip	4.5	5.5	0.2
	PBRC12.50BR-A	12.5	On-chip	On-chip	4.5	5.5	0.1
TDK	FCR4.0MC5	4.0	On-chip	On-chip	2.7	5.5	0.15
	FCR6.0MC5	6.0	On-chip	On-chip	2.7	5.5	0.15
	FCR8.0MC5	8.0	On-chip	On-chip	4.5	5.5	0.12
	FCR10.0MC5	10.0	On-chip	On-chip	4.5	5.5	0.12

Caution The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. Oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation frequency must be adjusted on the implementation circuit. For details, please contact directly the manufacturer of the resonator you will use.

DC Characteristics

(T_A = −40 to +85°C, V_{DD} = V_{DD0} = V_{DD1} = AV_{DD} = 1.9 to 5.5 V, V_{SS} = V_{SS0} = V_{SS1} = AV_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
V_{PP} supply voltage	V_{PP1}	In normal operation		0		0.2V_{DD}	V
Input voltage, low	V_{IL1}	**Note 1**	2.2 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			1.9 V ≤ V_{DD} < 2.2 V	0		0.2V_{DD}	
	V_{IL2}	P00 to P05, P20, P22, P33, P34, P70, P72, $\overline{\text{RESET}}$	2.2 V ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
			1.9 V ≤ V_{DD} < 2.2 V	0		0.15V_{DD}	
	V_{IL4}	P10 to P17, P130, P131	2.2 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			1.9 V ≤ V_{DD} < 2.2 V	0		0.2V_{DD}	
	V_{IL5}	X1, X2, XT1, XT2	2.2 V ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
			1.9 V ≤ V_{DD} < 2.2 V	0		0.1V_{DD}	
	V_{IL6}	P25, P27	2.2 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			1.9 V ≤ V_{DD} < 2.2 V	0		0.2V_{DD}	
Input voltage, high	V_{IH1}	**Note 1**	2.2 V ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		V_{DD}	V
			1.9 V ≤ V_{DD} < 2.2 V	0.8V_{DD}		V_{DD}	
	V_{IH2}	P00 to P05, P20, P22, P33, P34, P70, P72, $\overline{\text{RESET}}$	2.2 V ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			1.9 V ≤ V_{DD} < 2.2 V	0.85V_{DD}		V_{DD}	
	V_{IH4}	P10 to P17, P130, P131	2.2 V ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		V_{DD}	V
			1.9 V ≤ V_{DD} < 2.2 V	0.8V_{DD}		V_{DD}	
	V_{IH5}	X1, X2, XT1, XT2	2.2 V ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
			1.9 V ≤ V_{DD} < 2.2 V	0.85V_{DD}		V_{DD}	
	V_{IH6}	P25, P27	2.2 V ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		V_{DD}	V
			1.9 V ≤ V_{DD} < 2.2 V	0.8V_{DD}		V_{DD}	
Output voltage, low	V_{OL1}	For pins other than P40 to P47, P50 to P57, I_{OL} = 1.6 mA**Note 2**	4.5 V ≤ V_{DD} ≤ 5.5 V			0.4	V
		P40 to P47, P50 to P57 I_{OL} = 8 mA**Note 2**	4.5 V ≤ V_{DD} ≤ 5.5 V			1.0	V
	V_{OL2}	I_{OL} = 400 μA**Note 2**				0.5	V
Output voltage, high	V_{OH1}	I_{OH} = −1 mA**Note 2**	4.5 V ≤ V_{DD} ≤ 5.5 V	V_{DD} − 1.0			V
		I_{OH} = −100 μA**Note 2**		V_{DD} − 0.5			V
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	Except X1, X2, XT1, XT2			−3	μA
	I_{LIL2}		X1, X2, XT1, XT2			−20	μA
Input leakage current, high	I_{LIH1}	V_{IN} = V_{DD0}	Except X1, X2, XT1, XT2			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA

Notes 1. P21, P23, P24, P26, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P71, P80 to P87, P120 to P127

2. Per pin

DC Characteristics

(T_A = −40 to +85°C, V_{DD} = V_{DD0} = V_{DD1} = AV_{DD} = 1.9 to 5.5 V, V_{SS} = V_{SS0} = V_{SS1} = AV_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output leakage current, low	I_{LOL1}	V_{OUT} = 0 V				−3	μA
Output leakage current, high	I_{LOH1}	V_{OUT} = V_{DD}				3	μA
Supply voltage	I_{DD1}	Operating mode	f_{XX} = 12.5 MHz, V_{DD} = 5.0 V ±10%		24	40	mA
			f_{XX} = 6 MHz, V_{DD} = 3.0 V ±10%		8	17	mA
			f_{XX} = 2 MHz, V_{DD} = 2.0 V ±5%		2	10	mA
	I_{DD2}	HALT mode	f_{XX} = 12.5 MHz, V_{DD} = 5.0 V ±10%		8	20	mA
			f_{XX} = 6 MHz, V_{DD} = 3.0 V ±10%		2	10	mA
			f_{XX} = 2 MHz, V_{DD} = 2.0 V ±5%		0.7	7	mA
	I_{DD3}	IDLE mode	f_{XX} = 12.5 MHz, V_{DD} = 5.0 V ±10%		1	3	mA
			f_{XX} = 6 MHz, V_{DD} = 3.0 V ±10%		0.5	1.3	mA
			f_{XX} = 2 MHz, V_{DD} = 2.0 V ±5%		0.3	0.9	mA
	I_{DD4}	Operating mode**Note**	f_{XX} = 32 kHz, V_{DD} = 5.0 V ±10%		130	500	μA
			f_{XX} = 32 kHz, V_{DD} = 3.0 V ±10%		90	350	μA
			f_{XX} = 32 kHz, 2.0 V ≤ V_{DD} < 2.7 V		80	300	μA
			f_{XX} = 32 kHz, 1.9 V ≤ V_{DD} < 2.0 V		70	250	μA
	I_{DD5}	HALT mode**Note**	f_{XX} = 32 kHz, V_{DD} = 5.0 V ±10%		60	200	μA
			f_{XX} = 32 kHz, V_{DD} = 3.0 V ±10%		20	160	μA
			f_{XX} = 32 kHz, 2.0 V ≤ V_{DD} < 2.7 V		15	120	μA
			f_{XX} = 32 kHz, 1.9 V ≤ V_{DD} < 2.0 V		10	100	μA
	I_{DD6}	IDLE mode**Note**	f_{XX} = 32 kHz, V_{DD} = 5.0 V ±10%		50	190	μA
			f_{XX} = 32 kHz, V_{DD} = 3.0 V ±10%		15	150	μA
			f_{XX} = 32 kHz, 2.0 V ≤ V_{DD} < 2.7 V		12	110	μA
			f_{XX} = 32 kHz, 1.9 V ≤ V_{DD} < 2.0 V		7	90	μA
Data retention voltage	V_{DDDR}	HALT, IDLE modes		1.9		5.5	V
Data retention current	I_{DDDR}	STOP mode	V_{DD} = 2.0 V ±10%		2	10	μA
			V_{DD} = 5.0 V ±10%		10	50	μA
Pull-up resistor	R_L	V_{IN} = 0 V		10	30	100	kΩ

Note When main system clock is stopped.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(T_A = −40 to +85°C, V_{DD} = V_{DD0} = V_{DD1} = AV_{DD} = 1.9 to 5.5 V, V_{SS} = V_{SS0} = V_{SS1} = AV_{SS} = 0 V)

(1) Read/write operation (1/3)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time	t_{CYK}	4.5 V ≤ V_{DD} ≤ 5.5 V	80			ns
		2.7 V ≤ V_{DD} < 4.5 V	160			ns
		2.0 V ≤ V_{DD} < 2.7 V	320			ns
		1.9 V ≤ V_{DD} < 2.0 V	500			ns
Address setup time (to ASTB↓)	t_{SAST}	V_{DD} = 5.0 V ±10%	(0.5 + a) T − 20			ns
		V_{DD} = 3.0 V ±10%	(0.5 + a) T − 40			ns
		V_{DD} = 2.0 V ±5%	(0.5 + a) T − 80			ns
Address hold time (from ASTB↓)	t_{HSTLA}	V_{DD} = 5.0 V ±10%	0.5T − 19			ns
		V_{DD} = 3.0 V ±10%	0.5T − 24			ns
		V_{DD} = 2.0 V ±5%	0.5T − 34			ns
ASTB high-level width	t_{WSTH}	V_{DD} = 5.0 V ±10%	(0.5 + a) T − 17			ns
		V_{DD} = 3.0 V ±10%	(0.5 + a) T − 40			ns
		V_{DD} = 2.0 V ±5%	(0.5 + a) T − 110			ns
Address hold time (from $\overline{RD}$↑)	t_{HRA}	V_{DD} = 5.0 V ±10%	0.5T − 14			ns
		V_{DD} = 3.0 V ±10%	0.5T − 14			ns
		V_{DD} = 2.0 V ±5%	0.5T − 14			ns
Delay time from address to $\overline{RD}$↓	t_{DAR}	V_{DD} = 5.0 V ±10%	(1 + a) T − 24			ns
		V_{DD} = 3.0 V ±10%	(1 + a) T − 35			ns
		V_{DD} = 2.0 V ±5%	(1 + a) T − 80			ns
Address float time (from $\overline{RD}$↓)	t_{FAR}	V_{DD} = 5.0 V ±10%			0	ns
		V_{DD} = 3.0 V ±10%			0	ns
		V_{DD} = 2.0 V ±5%			0	ns
Data input time from address	t_{DAID}	V_{DD} = 5.0 V ±10%			(2.5 + a + n) T − 37	ns
		V_{DD} = 3.0 V ±10%			(2.5 + a + n) T − 52	ns
		V_{DD} = 2.0 V ±5%			(2.5 + a + n) T − 120	ns
Data input time from ASTB↓	t_{DSTID}	V_{DD} = 5.0 V ±10%			(2 + n) T − 35	ns
		V_{DD} = 3.0 V ±10%			(2 + n) T − 50	ns
		V_{DD} = 2.0 V ±5%			(2 + n) T − 80	ns
Data input time from $\overline{RD}$↓	t_{DRID}	V_{DD} = 5.0 V ±10%			(1.5 + n) T − 40	ns
		V_{DD} = 3.0 V ±10%			(1.5 + n) T − 50	ns
		V_{DD} = 2.0 V ±5%			(1.5 + n) T − 90	ns

Remark T: t_{CYK} = 1/fxx (fxx: Main system clock frequency)
a: 1 (during address wait), otherwise, 0
n: Number of wait states (n ≥ 0)

AC Characteristics

(T_A = −40 to +85°C, V_{DD} = V_{DD0} = V_{DD1} = AV_{DD} = 1.9 to 5.5 V, V_{SS} = V_{SS0} = V_{SS1} = AV_{SS} = 0 V)

(1) Read/write operation (2/3)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Delay time from ASTB↓ to $\overline{RD}$↓	t_{DSTR}	V_{DD} = 5.0 V ±10%	0.5T – 9			ns
		V_{DD} = 3.0 V ±10%	0.5T – 9			ns
		V_{DD} = 2.0 V ±5%	0.5T – 20			ns
Data hold time (from $\overline{RD}$↑)	t_{HRID}	V_{DD} = 5.0 V ±10%	0			ns
		V_{DD} = 3.0 V ±10%	0			ns
		V_{DD} = 2.0 V ±5%	0			ns
Address active time from $\overline{RD}$↑	t_{DRA}	V_{DD} = 5.0 V ±10%	0.5T – 2			ns
		V_{DD} = 3.0 V ±10%	0.5T – 12			ns
		V_{DD} = 2.0 V ±5%	0.5T – 35			ns
Delay time from $\overline{RD}$↑ to ASTB↑	t_{DRST}	V_{DD} = 5.0 V ±10%	0.5T – 9			ns
		V_{DD} = 3.0 V ±10%	0.5T – 9			ns
		V_{DD} = 2.0 V ±5%	0.5T – 40			ns
$\overline{RD}$ low-level width	t_{WRL}	V_{DD} = 5.0 V ±10%	(1.5 + n) T – 25			ns
		V_{DD} = 3.0 V ±10%	(1.5 + n) T – 30			ns
		V_{DD} = 2.0 V ±5%	(1.5 + n) T – 25			ns
Delay time from address to $\overline{WR}$↓	t_{DAW}	V_{DD} = 5.0 V ±10%	(1 + a) T – 24			ns
		V_{DD} = 3.0 V ±10%	(1 + a) T – 34			ns
		V_{DD} = 2.0 V ±5%	(1 + a) T – 70			ns
Address hold time (from $\overline{WR}$↑)	t_{HRD}	V_{DD} = 5.0 V ±10%	0.5T – 14			ns
		V_{DD} = 3.0 V ±10%	0.5T – 14			ns
		V_{DD} = 2.0 V ±5%	0.5T – 14			ns
Delay time from ASTB↓ to data output	t_{DSTOD}	V_{DD} = 5.0 V ±10%			0.5T + 15	ns
		V_{DD} = 3.0 V ±10%			0.5T + 30	ns
		V_{DD} = 2.0 V ±5%			0.5T + 240	ns
Delay time from $\overline{WR}$↓ to data output	t_{DWOD}	V_{DD} = 5.0 V ±10%			0.5T – 30	ns
		V_{DD} = 3.0 V ±10%			0.5T – 30	ns
		V_{DD} = 2.0 V ±5%			0.5T – 30	ns
Delay time from ASTB↓ to $\overline{WR}$↓	t_{DSTW}	V_{DD} = 5.0 V ±10%	0.5T – 9			ns
		V_{DD} = 3.0 V ±10%	0.5T – 9			ns
		V_{DD} = 2.0 V ±5%	0.5T – 20			ns
Data setup time (to $\overline{WR}$↑)	t_{SODWR}	V_{DD} = 5.0 V ±10%	(1.5 + n) T – 20			ns
		V_{DD} = 3.0 V ±10%	(1.5 + n) T – 25			ns
		V_{DD} = 2.0 V ±5%	(1.5 + n) T – 70			ns

Remark T: t_{CYK} = 1/fxx (fxx: Main system clock frequency)

a: 1 (during address wait), otherwise, 0

n: Number of wait states (n ≥ 0)

AC Characteristics

(T_A = −40 to +85°C, V_{DD} = V_{DD0} = V_{DD1} = AV_{DD} = 1.9 to 5.5 V, V_{SS} = V_{SS0} = V_{SS1} = AV_{SS} = 0 V)

(1) Read/write operation (3/3)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	Data hold time (from $\overline{WR}$↑)	t_{HWOD}	V_{DD} = 5.0 V ±10%	0.5T – 14			ns
			V_{DD} = 3.0 V ±10%	0.5T – 14			ns
			V_{DD} = 2.0 V ±5%	0.5T – 50			ns
	Delay time from $\overline{WR}$↑ to ASTB↑	t_{DWST}	V_{DD} = 5.0 V ±10%	0.5T – 9			ns
			V_{DD} = 3.0 V ±10%	0.5T – 9			ns
			V_{DD} = 2.0 V ±5%	0.5T – 30			ns
	$\overline{WR}$ low-level width	t_{WWL}	V_{DD} = 5.0 V ±10%	(1.5 + n) T – 25			ns
			V_{DD} = 3.0 V ±10%	(1.5 + n) T – 30			ns
			V_{DD} = 2.0 V ±5%	(1.5 + n) T – 30			ns
★	Delay time from address to EXA↓	t_{ADEXD}	V_{DD} = 5.0 V ±10%	0			ns
			V_{DD} = 3.0 V ±10%	0			ns
			V_{DD} = 2.0 V ±5%	0			ns
★	Delay time from EXA↓ to ASTB↓	t_{EXTAH}	V_{DD} = 5.0 V ±10%	0.5T – 20			ns
			V_{DD} = 3.0 V ±10%	0.5T – 30			ns
			V_{DD} = 2.0 V ±5%	0.5T – 40			ns
★	Delay time from $\overline{RD}$↑ to EXA↑	t_{EXRDS}	V_{DD} = 5.0 V ±10%	0			ns
			V_{DD} = 3.0 V ±10%	0			ns
			V_{DD} = 2.0 V ±5%	0			ns
★	Delay time from $\overline{WR}$↑ to EXA↑	t_{EXWDS}	V_{DD} = 5.0 V ±10%	T			ns
			V_{DD} = 3.0 V ±10%	T			ns
			V_{DD} = 2.0 V ±5%	T			ns
★	Delay time from EXA↑ to ASTB↑	t_{EXADR}	V_{DD} = 5.0 V ±10%	0.5T			ns
			V_{DD} = 3.0 V ±10%	0.5T			ns
			V_{DD} = 2.0 V ±5%	0.5T			ns

Remark T: t_{CYK} = 1/f_{XX} (f_{XX}: Main system clock frequency)
n: Number of wait states (n ≥ 0)

AC Characteristics (T_A = −40 to +85°C, V_{DD} = V_{DD0} = V_{DD1} = AV_{DD} = 1.9 to 5.5 V, V_{SS} = V_{SS0} = V_{SS1} = AV_{SS} = 0 V)

(2) External wait timing (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input time from address to $\overline{WAIT}$↓	t_{DAWT}	V_{DD} = 5.0 V ±10%			(2 + a) T − 40	ns
		V_{DD} = 3.0 V ±10%			(2 + a) T − 60	ns
		V_{DD} = 2.0 V ±5%			(2 + a) T − 300	ns
Input time from ASTB↓ to $\overline{WAIT}$↓	t_{DSTWT}	V_{DD} = 5.0 V ±10%			1.5T − 40	ns
		V_{DD} = 3.0 V ±10%			1.5T − 60	ns
		V_{DD} = 2.0 V ±5%			1.5T − 260	ns
Hold time from ASTB↓ to $\overline{WAIT}$	t_{HSTWT}	V_{DD} = 5.0 V ±10%	(0.5 + n) T + 5			ns
		V_{DD} = 3.0 V ±10%	(0.5 + n) T + 10			ns
		V_{DD} = 2.0 V ±5%	(0.5 + n) T + 30			ns
Delay time from ASTB↓ to $\overline{WAIT}$↑	t_{DSTWTH}	V_{DD} = 5.0 V ±10%			(1.5 + n) T − 40	ns
		V_{DD} = 3.0 V ±10%			(1.5 + n) T − 60	ns
		V_{DD} = 2.0 V ±5%			(1.5 + n) T − 90	ns
Input time from $\overline{RD}$↓ to $\overline{WAIT}$↓	t_{DRWTL}	V_{DD} = 5.0 V ±10%			T − 40	ns
		V_{DD} = 3.0 V ±10%			T − 60	ns
		V_{DD} = 2.0 V ±5%			T − 70	ns
Hold time from $\overline{RD}$↓ to $\overline{WAIT}$↓	t_{HRWT}	V_{DD} = 5.0 V ±10%	nT + 5			ns
		V_{DD} = 3.0 V ±10%	nT + 10			ns
		V_{DD} = 2.0 V ±5%	nT + 30			ns
Delay time from $\overline{RD}$↓ to $\overline{WAIT}$↑	t_{DRWTH}	V_{DD} = 5.0 V ±10%			(1 + n) T − 40	ns
		V_{DD} = 3.0 V ±10%			(1 + n) T − 60	ns
		V_{DD} = 2.0 V ±5%			(1 + n) T − 90	ns
Data input time from $\overline{WAIT}$↑	t_{DWTID}	V_{DD} = 5.0 V ±10%			0.5T − 5	ns
		V_{DD} = 3.0 V ±10%			0.5T − 10	ns
		V_{DD} = 2.0 V ±5%			0.5T − 30	ns
Delay time from $\overline{WAIT}$↑ to $\overline{RD}$↑	t_{DWTR}	V_{DD} = 5.0 V ±10%	0.5T			ns
		V_{DD} = 3.0 V ±10%	0.5T			ns
		V_{DD} = 2.0 V ±5%	0.5T + 5			ns
Delay time from $\overline{WAIT}$↑ to $\overline{WR}$↑	t_{DWTW}	V_{DD} = 5.0 V ±10%	0.5T			ns
		V_{DD} = 3.0 V ±10%	0.5T			ns
		V_{DD} = 2.0 V ±5%	0.5T + 5			ns
Input time from $\overline{WR}$↓ to $\overline{WAIT}$↓	t_{DWWTL}	V_{DD} = 5.0 V ±10%			T − 40	ns
		V_{DD} = 3.0 V ±10%			T − 60	ns
		V_{DD} = 2.0 V ±5%			T − 90	ns

Remark T: t_{CYK} = 1/f_{XX} (f_{XX}: Main system clock frequency)
a: 1 (during address wait), otherwise, 0
n: Number of wait states (n ≥ 0)

(2) External wait timing (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Hold time from $\overline{WR}\downarrow$ to $\overline{WAIT}$	t_{HWWT}	V_{DD} = 5.0 V ±10%	nT + 5			ns
		V_{DD} = 3.0 V ±10%	nT + 10			ns
		V_{DD} = 2.0 V ±5%	nT + 30			ns
Delay time from $\overline{WR}\downarrow$ to $\overline{WAIT}\uparrow$	t_{DWWTH}	V_{DD} = 5.0 V ±10%			(1 + n) T – 40	ns
		V_{DD} = 3.0 V ±10%			(1 + n) T – 60	ns
		V_{DD} = 2.0 V ±5%			(1 + n) T – 90	ns

Remark T: t_{CYK} = 1/f_{XX} (f_{XX}: Main system clock frequency)
n: Number of wait states (n ≥ 0)

Serial Operation (T_A = −40 to +85°C, V_{DD} = V_{DD0} = V_{DD1} = AV_{DD} = 1.9 to 5.5 V, V_{SS} = V_{SS0} = V_{SS1} = AV_{SS} = 0 V)

★ **(a) 3-wire serial I/O mode ($\overline{SCK}$: Internal clock output)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 5.5 V	640			ns
		2.7 V ≤ V_{DD} < 4.5 V	1,280			ns
		2.0 V ≤ V_{DD} < 2.7 V	2,560			ns
		1.9 V ≤ V_{DD} < 2.0 V	4,000			ns
$\overline{SCK}$ high-/low-level width	t_{KH1}, t_{KL1}	4.5 V ≤ V_{DD} ≤ 5.5 V	270			ns
		2.7 V ≤ V_{DD} < 4.5 V	590			ns
		2.0 V ≤ V_{DD} < 2.7 V	1,180			ns
		1.9 V ≤ V_{DD} < 2.0 V	1,900			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 5.5 V	10			ns
			30			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI1}		40			ns
SO output delay time (from $\overline{SCK}$↓)	t_{KSO1}				30	ns

★ **(b) 3-wire serial I/O mode ($\overline{SCK}$: External clock input)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 5.5 V	640			ns
		2.7 V ≤ V_{DD} < 4.5 V	1,280			ns
		2.0 V ≤ V_{DD} < 2.7 V	2,560			ns
		1.9 V ≤ V_{DD} < 2.0 V	4,000			ns
$\overline{SCK}$ high-/low-level width	t_{KH2} t_{KL2}	4.5 V ≤ V_{DD} ≤ 5.5 V	320			ns
		2.7 V ≤ V_{DD} < 4.5 V	640			ns
		2.0 V ≤ V_{DD} < 2.7 V	1,280			ns
		1.9 V ≤ V_{DD} < 2.0 V	2,000			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V	10			ns
			30			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI2}		40			ns
SO output delay time (from $\overline{SCK}$↓)	t_{KSO2}				30	ns

(c) UART mode

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY3}	4.5 V ≤ V_{DD} ≤ 5.5 V	417			ns
		2.7 V ≤ V_{DD} < 4.5 V	833			ns
			1,667			ns
ASCK high-/low-level width	t_{KH3} t_{KL3}	4.5 V ≤ V_{DD} ≤ 5.5 V	208			ns
		2.7 V ≤ V_{DD} < 4.5 V	416			ns
			833			ns

(d) I²C bus mode (μPD78F4225Y only)

Parameter		Symbol	Standard Mode		High-Speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f_{CLK}	0	100	0	400	kHz
Bus free time (between stop and start conditions)		t_{BUF}	4.7	–	1.3	–	μs
Hold time[Note1]		$t_{HD:STA}$	4.0	–	0.6	–	μs
Low-level width of SCL0 clock		t_{LOW}	4.7	–	1.3	–	μs
High-level width of SCL0 clock		t_{HIGH}	4.0	–	0.6	–	μs
Setup time of start/restart conditions		$t_{SU:STA}$	4.7	–	0.6	–	μs
Data hold time	When using CBUS-compatible master	$t_{HD:DAT}$	5.0	–	–	–	μs
	When using I²C bus		0[Note 2]	–	0[Note 2]	0.9[Note 3]	μs
Data setup time		$t_{SU:DAT}$	250	–	100[Note 4]	–	ns
Rise time of SDA0 and SCL0 signals		t_R	–	1,000	20 + 0.1Cb[Note 5]	300	ns
Fall time of SDA0 and SCL0 signals		t_F	–	300	20 + 0.1Cb[Note 5]	300	ns
Setup time of stop condition		$t_{SU:STO}$	4.0	–	0.6	–	μs
Pulse width of spike restricted by input filter		t_{SP}	–	–	0	50	ns
Load capacitance of each bus line		Cb	–	400	–	400	pF

Notes 1. For the start condition, the first clock pulse is generated after the hold time.

2. To fill the undefined area of the SCL0 falling edge, it is necessary for the device to provide an internal SDA0 signal (on $V_{IHmin.}$) with at least 300 ns of hold time.

3. If the device does not extend the SCL0 signal low-level hold time (t_{LOW}), only the maximum data hold time $t_{HD:DAT}$ needs to be satisfied.

4. The high-speed mode I²C bus can be used in a standard mode I²C bus system. In this case, the conditions described below must be satisfied.

- If the device does not extend the SCL0 signal low-level hold time
  $t_{SU:DAT} \geq 250$ ns
- If the device extends the SCL0 signal low-level hold time
  Be sure to transmit the data bit to the SDA0 line before the SCL0 line is released ($t_{Rmax.} + t_{SU:DAT}$ = 1,000 + 250 = 1,250 ns by standard mode I²C bus specification)

5. Cb: Total capacitance per bus line (unit: pF)

Other Operations (T_A = −40 to +85°C, V_{DD} = V_{DD0} = V_{DD1} = AV_{DD} = 1.9 to 5.5 V, V_{SS} = V_{SS0} = V_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
NMI high-/low-level width	t_{WNIL} t_{WNIH}		10			μs
Interrupt input high-/low-level width	t_{WITL} t_{WITH}	INTP0 to INTP5	100			ns
$\overline{\text{RESET}}$ high-/low-level width	t_{WRSL} t_{WRSH}		10			μs

Clock Output Operation

(T_A = −40 to +85°C, V_{DD} = V_{DD0} = V_{DD1} = AV_{DD} = 1.9 to 5.5 V, V_{SS} = V_{SS0} = V_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
PCL cycle time	t_{CYCL}	4.5 V ≤ V_{DD} ≤ 5.5 V, nT	80		31,250	ns
PCL high-/low-level width	t_{CLL} t_{CLH}	4.5 V ≤ V_{DD} ≤ 5.5 V, 0.5T − 10	30		15,615	ns
PCL rise/fall time	t_{CLR} t_{CLF}	4.5 V ≤ V_{DD} ≤ 5.5 V			5	ns
		2.7 V ≤ V_{DD} < 4.5 V			10	ns
		1.9 V ≤ V_{DD} < 2.7 V			20	ns

Remark T: t_{CYK} = 1/fxx (fxx: Main system clock frequency)

n: Division ratio set by software in the CPU

- When using the main system clock: n = 1, 2, 4, 8, 16, 32, 64, 128
- When using the subsystem clock: n = 1

A/D Converter Characteristics

(T_A = −40 to +85°C, V_{DD} = V_{DD0} = V_{DD1} = AV_{DD} = 1.9 to 5.5 V, V_{SS} = V_{SS0} = V_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note]		6.25 MHz < f_{XX} ≤ 12.5 MHz, 4.5 V ≤ V_{DD} ≤ 5.5 V, AV_{DD} = V_{DD0}			±1.2	%FSR
		3.125 MHz < f_{XX} ≤ 6.25 MHz, 2.7 V ≤ V_{DD} ≤ 5.5 V, AV_{DD} = V_{DD0}			±1.2	%FSR
		2 MHz < f_{XX} ≤ 3.125 MHz, 2.0 V ≤ V_{DD} ≤ 5.5 V, AV_{DD} = V_{DD0}			±1.6	%FSR
		f_{XX} = 2 MHz, 1.9 V ≤ V_{DD} ≤ 5.5 V AV_{DD} = V_{DD0}			±1.6	%FSR
Conversion time	t_{CONV}		14		144	μs
Sampling time	t_{SAMP}		24/f_{XX}			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{DD}	V
Reference voltage	AV_{DD}		V_{DD}	V_{DD}	V_{DD}	V
Resistance between AV_{DD} and AV_{SS}	R_{AVREF0}	A/D conversion is not performed		40		kΩ

Note Excludes quantization error (±0.2%FSR).

Remark FSR: Full-scale range

D/A Converter Characteristics

(T_A = −40 to +85°C, V_{DD} = V_{DD0} = V_{DD1} = AV_{DD} = 1.9 to 5.5 V, V_{SS} = V_{SS0} = V_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution				8	8	8	bit
Overall error[Note]		2.0 V ≤ V_{DD} ≤ 5.5 V, AV_{DD} = V_{DD0} R = 10 MΩ, 2.0 V ≤ AV_{REF1} ≤ AV_{DD}				±0.6	%FSR
		1.9 V ≤ V_{DD} ≤ 2.0 V, AV_{DD} = V_{DD0} R = 10 MΩ, 1.9 V ≤ AV_{REF1} ≤ AV_{DD}				±1.2	%FSR
Settling time		Load conditions: C = 30 pF	4.5 V ≤ AV_{REF1} ≤ 5.5 V			10	μs
			2.7 V ≤ AV_{REF1} < 4.5 V			15	μs
			1.9 V ≤ AV_{REF1} < 2.7 V			20	μs
Output resistance	R_O	DACS0, 1 = 55H			8		kΩ
Reference voltage	AV_{REF1}			1.9		V_{DD0}	V
AV_{REF1} current	AI_{REF1}	For only 1 channel				2.5	mA

Note Excludes quantization error (±0.2%FSR).

Remark FSR: Full-scale range

Flash Memory Programming Characteristics

(T_A = 10 to 40°C, V_{DD} = AV_{DD} = 1.9 to 5.5 V, V_{SS} = AV_{SS} = 0 V, V_{PP} = 9.7 to 10.3 V)

★ **(1) Basic characteristics**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_{XX}	4.5 V ≤ V_{DD} ≤ 5.5 V	2		12.5	MHz
		2.7 V ≤ V_{DD} < 4.5 V	2		6.25	MHz
		2.0 V ≤ V_{DD} < 2.7 V	2		3.125	MHz
		1.9 V ≤ V_{DD} < 2.0 V	2	2	2	MHz
Oscillation frequency[Note 1]	f_X	4.5 V ≤ V_{DD} ≤ 5.5 V	4		25	MHz
		2.7 V ≤ V_{DD} < 4.5 V	4		12.5	MHz
		2.0 V ≤ V_{DD} < 2.7 V	4		6.25	MHz
		1.9 V ≤ V_{DD} < 2.0 V	4	4	4	MHz
Supply voltage	V_{DD}		1.9		5.5	V
	V_{PPL}	When detecting V_{PP} low level	0		$0.2V_{DD}$	V
	V_{PP}	When detecting V_{PP} high level	$0.9V_{DD}$		$1.1V_{DD}$	V
	V_{PPH}	When detecting V_{PP} high voltage	9.7	10	10.3	V
Write time	C_{WRT}		20[Note 2]			times
Operating temperature	T_A		–40		85	°C
Storage temperature	T_{stg}		–65		125	°C
Programming temperature	T_{PRG}		10		40	°C

Notes 1. When rewriting without using handshake mode

2. Operation cannot be guaranteed when the number of rewrites exceeds 20.
In the case of K standard products, operation cannot be guaranteed when the number of rewrites exceeds 5.

Cautions 1. If writing is not successful in the initial write operation, execute the program command again, and then execute the verify command to confirm that the write operation has been completed normally (I, K standard).

2. Handshake mode is supported by products other than those with the I or K standard.

Remarks 1. The fifth letter from the left in the lot number indicates the standard of the product.

2. After executing the program command, execute the verify command to confirm that the write operation has been completed normally.

3. Handshake mode is the CSI write mode that uses P24. Handshake mode can be used with the PG-FR3 and FL-PR3.

4. The I standard only applies to ES (engineering sample) products. Because these products are engineering samples, their operation cannot be guaranteed.

Flash Memory Programming Characteristics

(T_A = 10 to 40°C, V_{DD} = AV_{DD} = 1.9 to 5.5 V, V_{SS} = AV_{SS} = 0 V, V_{PP} = 9.7 to 10.3 V)

(2) Write erase characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{PP} supply voltage	V_{PP2}	During flash memory programming	9.7	10.0	10.3	V
V_{DD} supply current	I_{DD}	When V_{PP} = V_{PP2}, f_{XX} = 12.5 kHz			40	mA
V_{PP} supply current	I_{PP}	When V_{PP} = V_{PP2}			100	mA
Step erase time	T_{er}	**Note 1**		0.2		s
Overall erase time per area	T_{era}	When step erase time = 0.2 s**Note 2**			20	s/area
Write-back time	T_{wb}	**Note 3**		50		ms
Number of write-backs per write-back command	C_{wb}	When write-back time = 50 ms**Note 4**			60	times/ write-back command
Number of erase/ write-backs	C_{erwb}				16	times
Step write time	T_{wr}	**Note 5**		50		μs
Overall write time per word	T_{wrw}	When step write time = 50 μs (1 word = 1 byte)**Note 6**	50		500	μs/ word
Number of rewrites per area	C_{erwr}	1 erase + 1 write after erase = 1 rewrite**Note 7**		20		times/ area

Notes 1. The recommended setting value for the step erase time is 0.2 s.

2. The prewrite time before erasure and the erase verify time (write-back time) is not included.

3. The recommended setting value for the write-back time is 50 ms.

4. Write-back is executed once by the issuance of the write-back command. Therefore, the retry times must be the maximum value minus the number of commands issued.

6. The actual write time per word is 100 μs longer. The internal verify time during or after a write is not included.

7. When a product is first written after shipment, "erase → write" and "write only" are both taken as one rewrite.

Example: P: Write, E: Erase

Shipped product → P → E → P→ E → P: 3 rewrites

Shipped product → E → P → E → P → E → P: 3 rewrites

Remarks 1. The range of the operating clock during flash memory programming is the same as the range during normal operation.

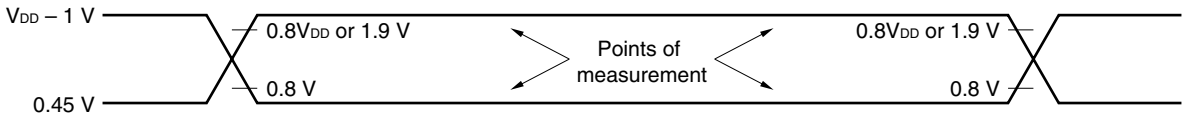
2. When using the PG-FP3, the time parameters that need to be downloaded from the parameter files for write/erase are automatically set. Unless otherwise directed, do not change the set values.

Data Retention Characteristics

(T_A = −40 to +85°C, V_{DD} = V_{DD0} = V_{DD1} = AV_{DD} = 1.9 to 5.5 V, V_{SS} = V_{SS0} = V_{SS1} = AV_{SS} = 0 V)

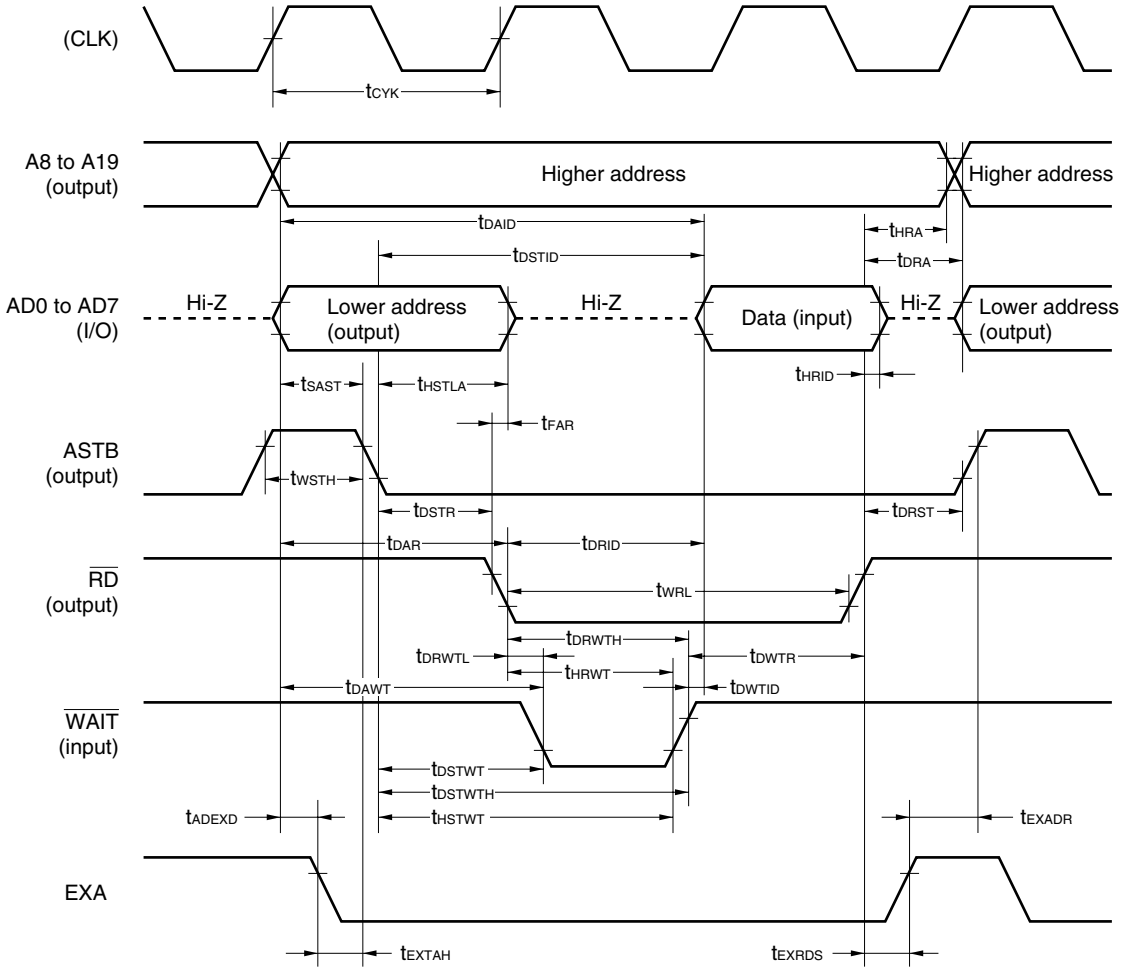
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode	1.9		5.5	V
Data retention current	I_{DDDR}	V_{DDDR} = 5.0 V ±10%		10	50	μA
		V_{DDDR} = 2.0 V ±5%		2	10	μA
V_{DD} rise time	t_{RVD}		200			μs
V_{DD} fall time	t_{FVD}		200			μs
V_{DD} hold time (from STOP mode setting)	t_{HVD}		0			ms
STOP release signal input time	t_{DREL}		0			ms
Oscillation stabilization wait time	t_{WAIT}	Crystal resonator	30			ms
		Ceramic resonator	5			ms
Input voltage, low	V_{IL}	$\overline{\text{RESET}}$, P00/INTP0 to P05/INTP5	0		$0.1V_{DDDR}$	V
Input voltage, high	V_{IH}		$0.9V_{DDDR}$		V_{DDDR}	V

AC Timing Measurement Points

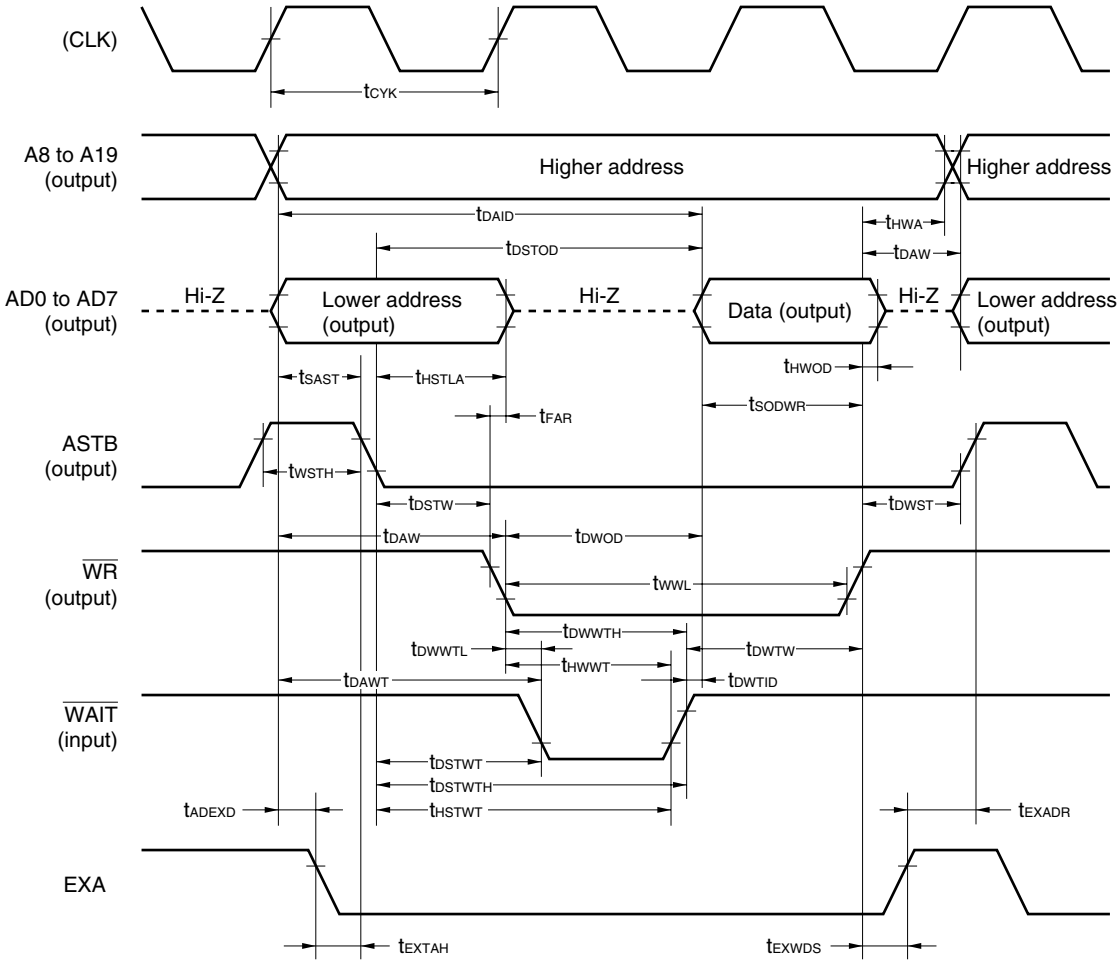


Timing Waveform

★ **(1) Read operation**

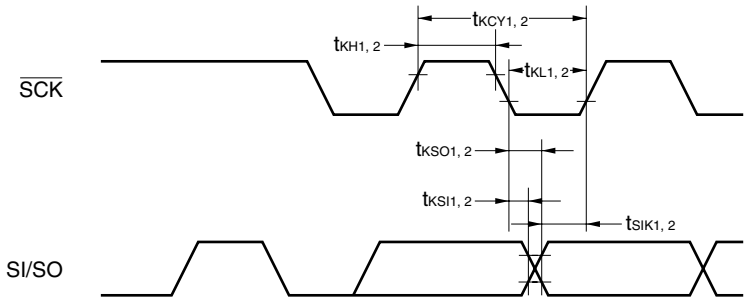


★ **(2) Write operation**

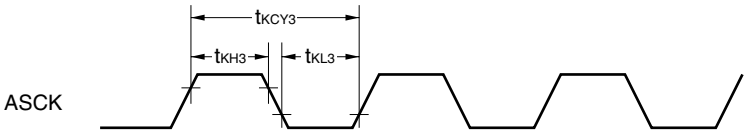


Serial Operation

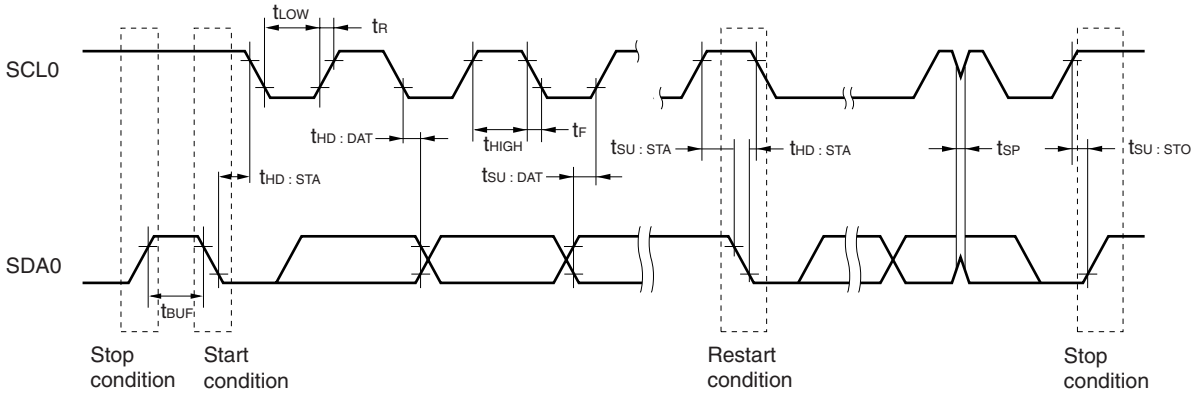
(1) 3-wire serial I/O mode



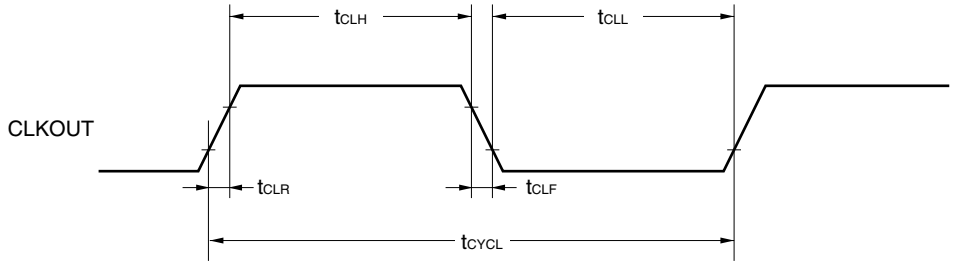
(2) UART mode



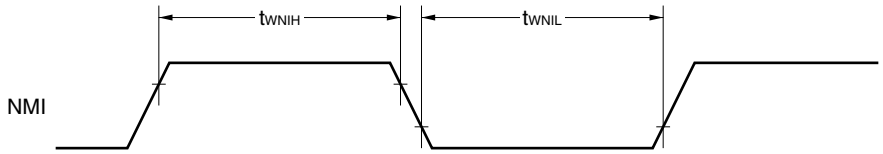
(3) I²C bus mode (μPD78F4255Y only)

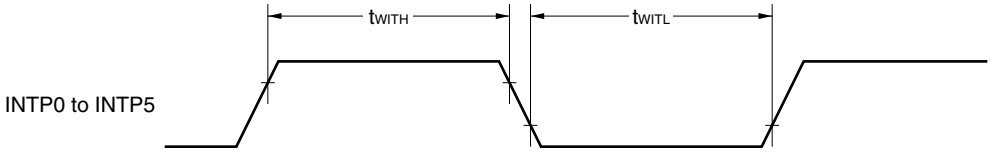


Clock Output Timing

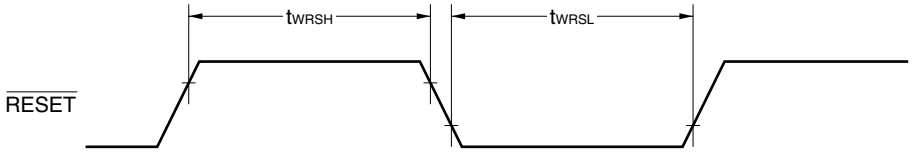


Interrupt Input Timing

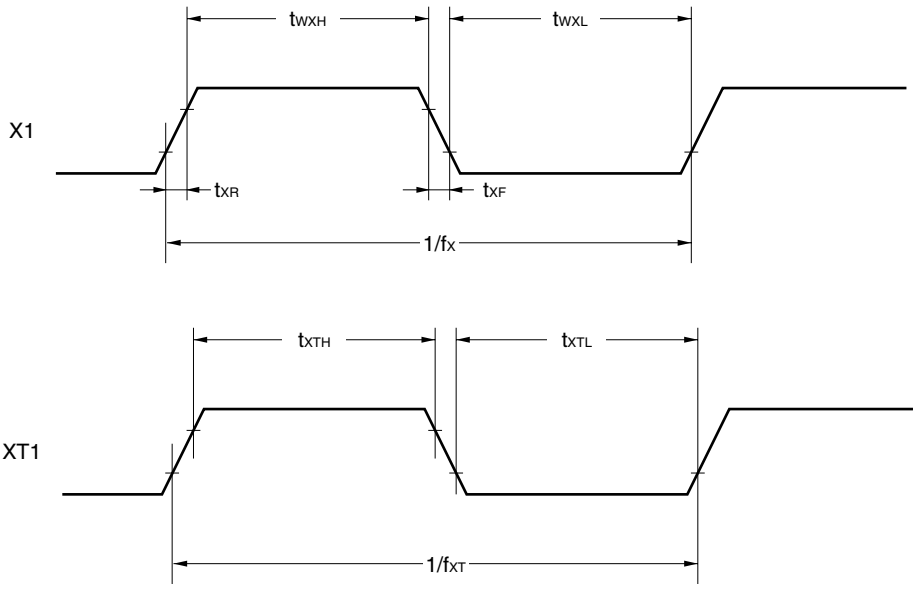




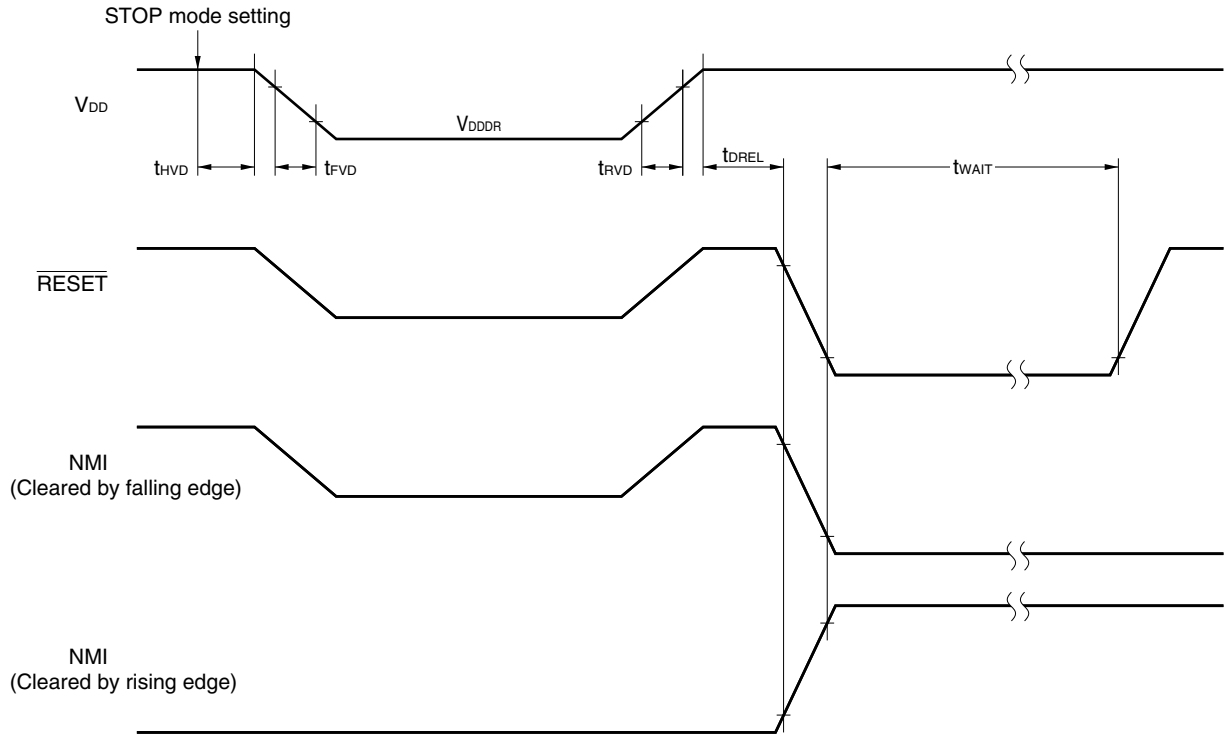
Reset Input Timing



Clock Timing

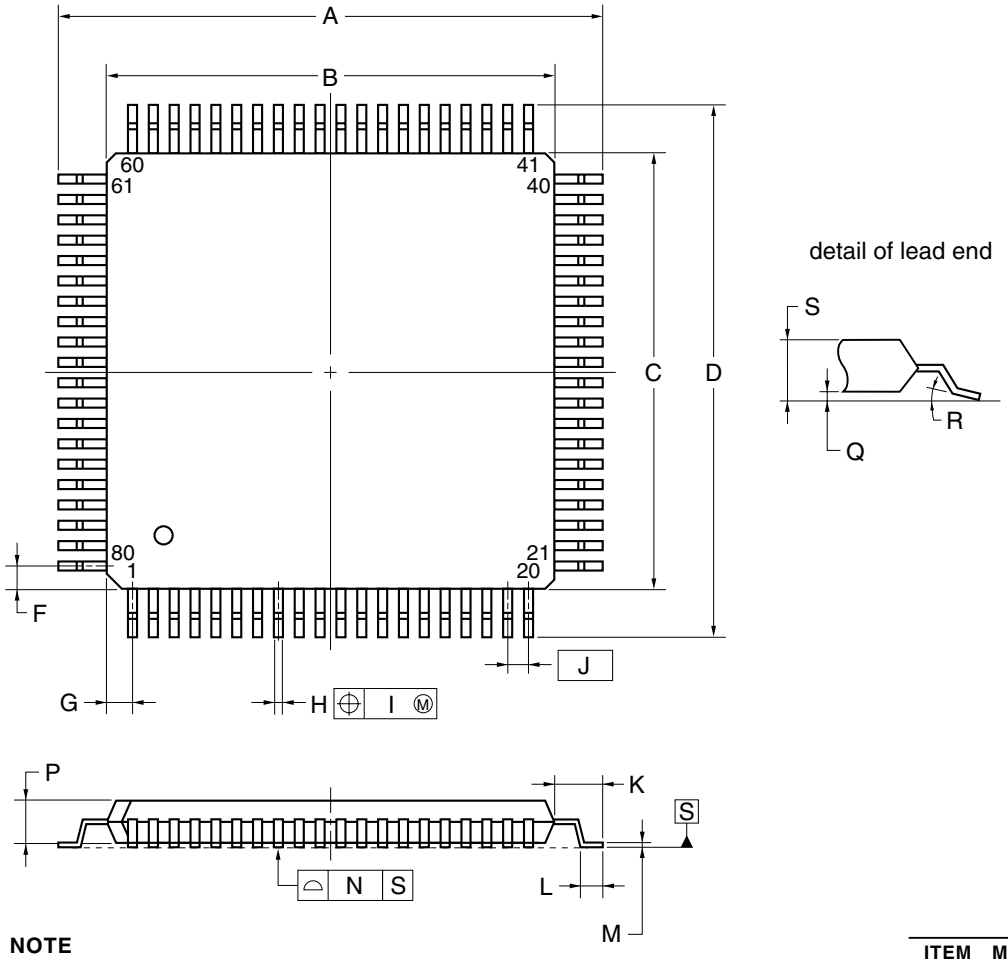


Data Retention Characteristics



★ **8. PACKAGE DRAWINGS**

80-PIN PLASTIC QFP (14x14)



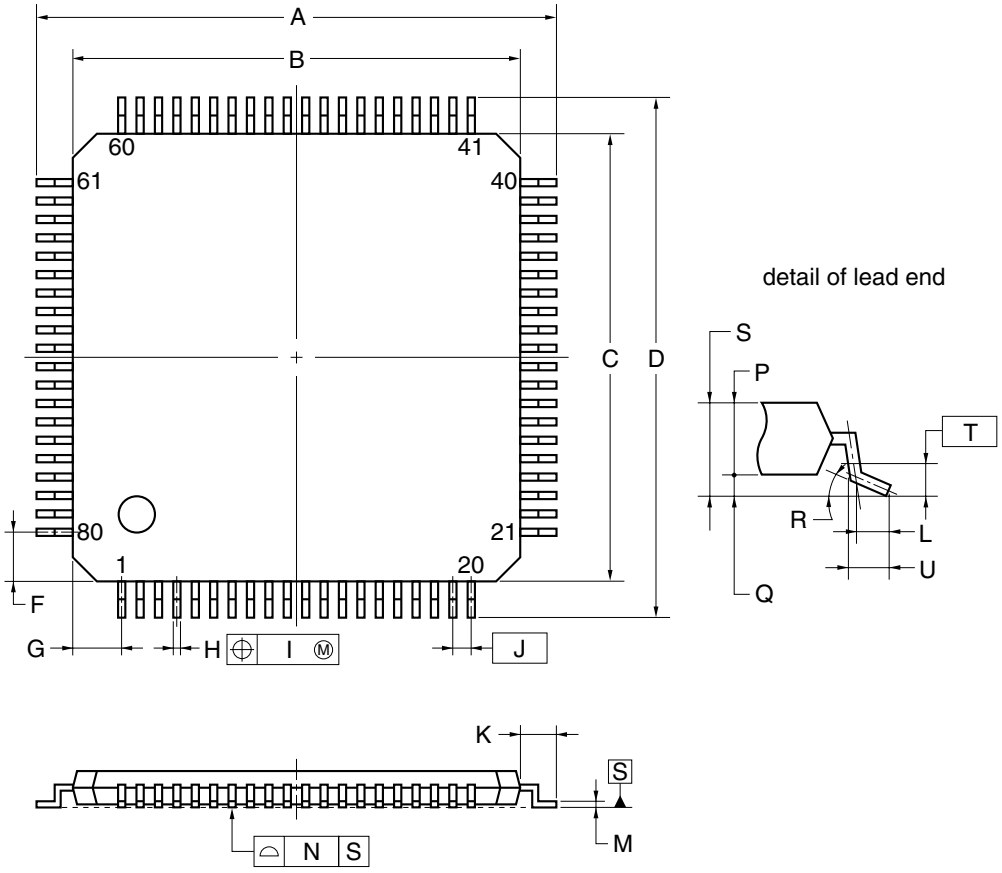
NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.20±0.20
B	14.00±0.20
C	14.00±0.20
D	17.20±0.20
F	0.825
G	0.825
H	0.32±0.06
I	0.13
J	0.65 (T.P.)
K	1.60±0.20
L	0.80±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	1.40±0.10
Q	0.125±0.075
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.70 MAX.

P80GC-65-8BT-1

80-PIN PLASTIC TQFP (FINE PITCH) (12x12)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	14.0±0.2
B	12.0±0.2
C	12.0±0.2
D	14.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5
M	0.145±0.05
N	0.08
P	1.0
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.1±0.1
T	0.25
U	0.6±0.15

P80GK-50-9EU-1

★ 9. RECOMMENDED SOLDERING CONDITIONS

The μPD78F4225Y should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 9-1. Soldering Conditions for Surface Mount Type

(1) μPD78F4225GC-8BT: 80-pin plastic QFP (14 × 14)
μPD78F4225YGC-8BT: 80-pin plastic QFP (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-107-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature) Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	WS60-107-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

(2) μPD78F4225GK-9EU: 80-pin plastic TQFP (fine pitch) (12 × 12)
μPD78F4225YGK-9EU: 80-pin plastic TQFP (fine pitch) (12 × 12)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-103-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-103-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78F4225Y. Also see **(5) Cautions on Using Development Tools**.

(1) Language Processing Software

RA78K4	Assembler package common to 78K/IV Series
CC78K4	C compiler package common to 78K/IV Series
DF784225	Device file common to μPD784225, 784225Y Subseries
CC78K4-L	C compiler library source file common to 78K/IV Series

(2) Flash Memory Writing Tools

Flashpro III (Part No.: FL-PR3, PG-FP3)	Dedicated flash programmer for microcontroller incorporating flash memory
FA-80GC	Adapter for writing 80-pin plastic QFP (GC-8BT type) flash memory
FA-80GK	Adapter for writing 80-pin plastic TQFP (GK-9EU type) flash memory

(3) Debugging Tools

- **When IE-78K4-NS in-circuit emulator is used**

IE-78K4-NS	In-circuit emulator common to 78K/IV Series
IE-70000-MC-PS-B	Power supply unit for IE-78K4-NS
IE-70000-98-IF-C	Interface adapter used when PC-9800 series PC (except notebook type) is used as host machine (C bus supported)
IE-70000-CD-IF-A	PC card and cable when notebook PC is used as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT™ or compatible as host machine (ISA bus supported)
IE-70000-PCI-IF-A	Interface adapter when using PC that incorporates PCI bus as host machine
IE-784225-NS-EM1	Emulation board to emulate μPD784225, 784225Y Subseries
NP-80GC	Emulation probe for 80-pin plastic QFP (GC-8BT type)
NP-80GK	Emulation probe for 80-pin plastic TQFP (GK-9EU type)
EV-9200GC-80	Socket to be mounted on a target system board made for 80-pin plastic QFP (GC-8BT type)
TGK-080-SDW	Conversion adapter to connect the NP-80GK and a target system board on which an 80-pin plastic TQFP (GK-9EU type) can be mounted
ID78K4-NS	Integrated debugger for IE-78K4-NS
SM78K4	System simulator common to 78K/IV Series
DF784225	Device file common to μPD784225, 784225Y Subseries

- **When IE-784000-R in-circuit emulator is used**

IE-784000-R	In-circuit emulator common to 78K/IV Series
IE-70000-98-IF-C	Interface adapter used when PC-9800 series PC (except notebook type) is used as host machine (C bus supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT or compatible as host machine (ISA bus supported)
IE-70000-PCI-IF-A	Interface adapter when using PC that incorporates PCI bus as host machine
IE-78000-R-SV3	Interface adapter and cable used when EWS is used as host machine
IE-784225-NS-EM1	Emulation board to emulate μPD784225, 784225Y Subseries
IE-784000-R-EM	Emulation board common to 78K/IV Series
IE-78K4-R-EX2	Emulation probe conversion board necessary when using IE-784225-NS-EM1 on IE-784000-R
EP-78230GC-R	Emulation probe for 80-pin plastic QFP (GC-8BT type)
EP-78054GK-R	Emulation probe for 80-pin plastic LQFP (GK-9EU type)
EV-9200GC-80	Socket to be mounted on a target system board made for 80-pin plastic QFP (GC-8BT type)
TGK-080SDW	Conversion adapter to connect the EP-78054GK-R and a target system board on which an 80-pin plastic TQFP (GK-9EU type) can be mounted
ID78K4	Integrated debugger for IE-784000-R
SM78K4	System simulator common to 78K/IV Series
DF784225	Device file common to μPD784225, 784225Y Subseries

(4) Real-time OS

RX78K/IV	Real-time OS for 78K/IV Series
MX78K4	OS for 78K/IV Series

(5) Cautions on Using Development Tools

- The ID78K4-NS, ID78K4, and SM78K4 are used in combination with the DF784225.
- The CC78K4 and RX78K/IV are used in combination with the RA78K4 and DF784225.
- The FL-PR3, FA-80GC, FA-80GK, NP-80GC, and NP-80GK are products made by Naito Densei Machida Mfg. Co., Ltd. (TEL: +81-44-822-3813).
- The TGK-080-SDW is a product made by TOKYO ELETECH CORPORATION.
  For further information, contact Daimaru Kogyo, Ltd.
  Tokyo Electronics Department (TEL: +81-3-3820-7112)
  Osaka Electronics Department (TEL: +81-6-6244-6672)
- For third-party development tools, see the **Single-Chip Microcontroller Development Tools Selection Guide (U11069E)**.
- The host machine and OS suitable for each software are as follows:

Host Machine [OS] / Software	PC	EWS
	PC-9800 series [Windows] IBM PC/AT and compatibles [Japanese/English Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K4	○Note	○
CC78K4	○Note	○
ID78K4-NS	○	–
ID78K4	○	○
SM78K4	○	–
RX78K/IV	○Note	○
MX78K4	○Note	○

Note DOS-based software

★ APPENDIX B. RELATED DOCUMENTS

Documents Related to Device

Document Name	Document No.
μPD784224, 784225, 784224Y, 784225Y Data Sheet	U12376E
μPD78F4225, 78F4225Y Data Sheet	This document
μPD784225, 784225Y Subseries User's Manual Hardware	To be prepared
78K/IV Series User's Manual Instruction	U10905E

Documents Related to Development Tools (User's Manuals)

Document Name		Document No.
RA78K4 Assembler Package	Operation	U11334E
	Language	U11162E
	Structured Assembler Preprocessor	U11743E
CC78K4 Series	Operation	U11572E
	Language	U11571E
IE-78K4-NS		U13356E
IE-784000-R		U12903E
IE-784225-NS-EM1		U13742E
EP-78230		EEU-1515
EP-78054		U13630E
SM78K4 System Simulator Windows Base	Reference	U10093E
SM78K Series System Simulator	External component user open interface specification	U10092E
ID78K4-NS Integrated Debugger PC based	Reference	U12796E
ID78K4 Integrated Debugger Windows based	Reference	U10440E
ID78K4 Integrated Debugger HP-UX, SunOS, NEWS-OS based	Reference	U11960E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Documents Related to Embedded Software (User's Manual)

Document Name		Document No.
78K/IV Series Real-Time OS	Fundamentals	U10603E
	Installation	U10604E

Other Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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800-366-9782
Fax: 408-588-6130
800-729-9288

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Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

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Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

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Fax: 08-63 80 388

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Fax: 65-250-3583

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Taipei, Taiwan
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Fax: 02-2719-5951

NEC do Brasil S.A.
Electron Devices Division
Guarulhos-SP Brasil
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Fax: 55-11-6462-6829

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