NEC

MOS INTEGRATED CIRCUIT

μPD78F4216Y

16/8-BIT SINGLE-CHIP MICROCONTROLLERS

The μPD78F4216Y is a member of the μPD784216Y Subseries in the 78K/IV Series.

The μPD78F4216Y has a flash memory in place of the internal ROM of the μPD784216Y. The flash memory can be written or erased while mounted on the target board.

The μPD78F4216Y is based on the μPD78F4216 but with an I^2C bus control function added, and is suited to AV equipment applications.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD784216, 784216Y Subseries User's Manual - Hardware: U12015E
78K/IV Series User's Manual - Instruction: U10905E

FEATURES

- I^2C bus serial interface supporting multi master
- Pin-compatible with mask ROM model (except V_{PP} pin)
- Flash memory: 128 Kbytes
- Internal RAM: 8192 bytes
★ - Supply voltage: V_{DD} = 2.7 to 5.5 V

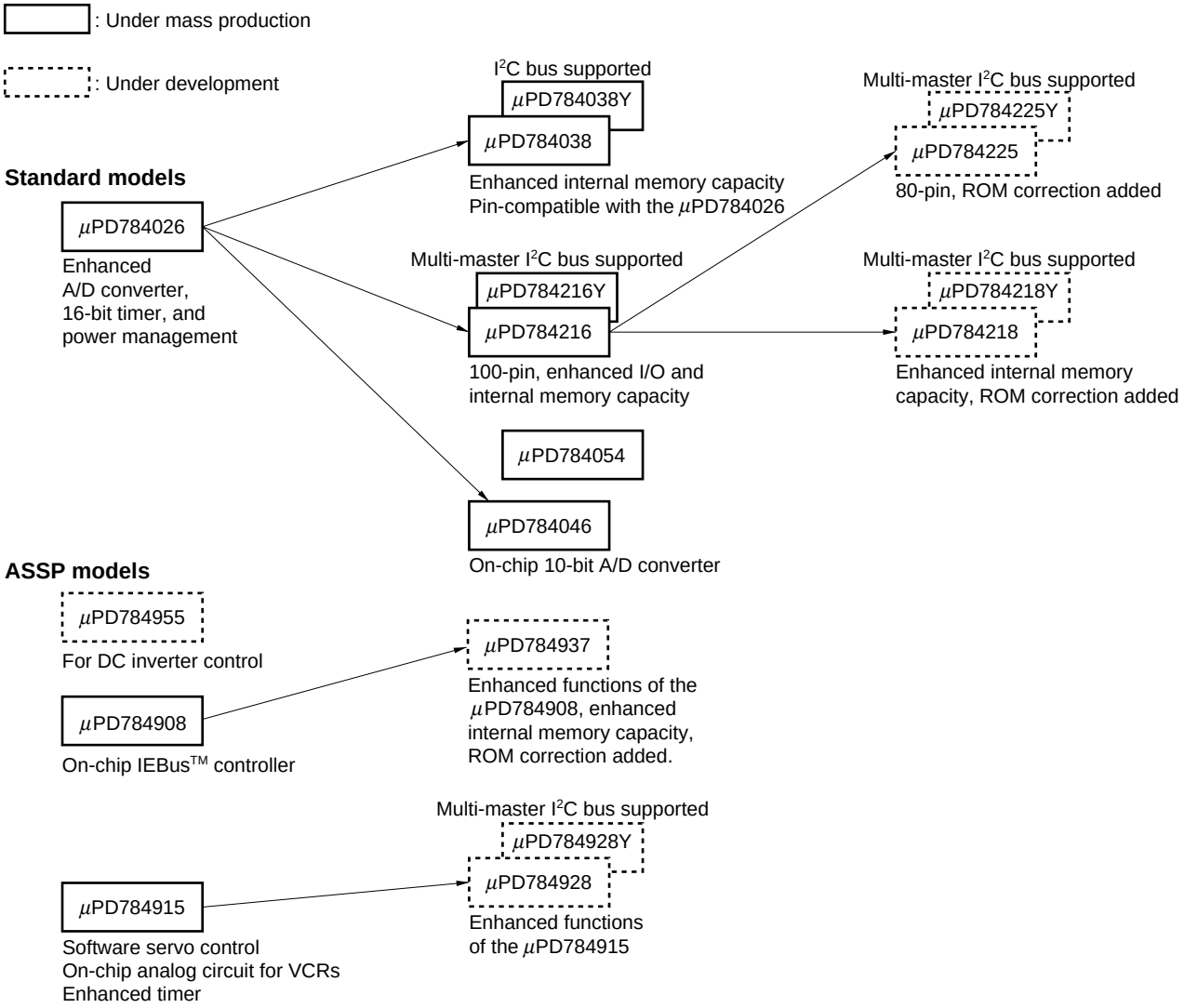
ORDERING INFORMATION

Part Number	Package
★ μPD78F4216YGC-8EU	100-pin plastic LQFP (fine pitch) (14 × 14 mm)
μPD78F4216YGF-3BA	100-pin plastic QFP (14 × 20 mm)

Document No. U11824EJ1V0DS00 (1st edition)
Date Published February 1999 N CP(K)
Printed in Japan

The mark ★ shows major revised points.

★ 78K/IV SERIES LINEUP



FUNCTIONS (1/2)

Item			Function		
Number of basic instructions (mnemonics)			113		
General-purpose register			8 bits × 16 registers × 8 banks, or 16 bits × 8 registers × 8 banks (memory mapping)		
★ Minimum instruction execution time			160 ns/320 ns/640 ns/1280 ns/2560 ns (@ f_{XX} = 12.5-MHz operation with main system clock)		
Internal memory		Flash memory	128 Kbytes		
		RAM	8192 bytes		
Memory space			1 Mbyte with program and data spaces combined		
I/O port		Total	86		
		CMOS Input	8		
		CMOS I/O	72		
		N-ch open-drain I/O	6		
	Pins with ancillary functions[Note]	Pins with pull-up resistor	70		
		LEDs direct drive output	22		
		Middle voltage pin	6		
Real-time output port			4 bits × 2, or 8 bits × 1		
Timer/counter			Timer/counter: (16-bit)	Timer register × 1 Capture/compare register × 2	Pulse output • PPG output • Square wave output • One-shot pulse output
			Timer/counter 1: (8-bit)	Timer register × 1 Compare register × 1	Pulse output • PWM output • Square wave output
			Timer/counter 2: (8-bit)	Timer register × 1 Compare register × 1	Pulse output • PWM output • Square wave output
			Timer/counter 5: (8-bit)	Timer register × 1 Compare register × 1	Pulse output • PWM output • Square wave output
			Timer/counter 6: (8-bit)	Timer register × 1 Compare register × 1	Pulse output • PWM output • Square wave output
			Timer/counter 7: (8-bit)	Timer register × 1 Compare register × 1	Pulse output • PWM output • Square wave output
			Timer/counter 8: (8-bit)	Timer register × 1 Compare register × 1	Pulse output • PWM output • Square wave output

Note The pins with ancillary functions are included in the I/O pins.

FUNCTIONS (2/2)

	Item		Function
	Serial interface		UART/IOE (3-wire serial I/O): 2 channels (on-chip baud rate generator) CSI (3-wire serial I/O, I^2C bus supporting multi master): 1 channel
	A/D converter		8-bit resolution × 8 channels
	D/A converter		8-bit resolution × 2 channels
	Clock output		Selectable from f_{XX}, $f_{XX}/2$, $f_{XX}/2^2$, $f_{XX}/2^3$, $f_{XX}/2^4$, $f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$, f_{XT}
	Buzzer output		Selectable from $f_{XX}/2^{10}$, $f_{XX}/2^{11}$, $f_{XX}/2^{12}$, $f_{XX}/2^{13}$
	Watch timer		1 channel
	Watchdog timer		1 channel
★	Standby		HALT/STOP/IDLE mode
	Interrupt	Hardware source	29 (internal: 20, external: 9)
		Software source	BRK instruction, BRKCS instruction, operand error
		Non-maskable	Internal: 1, external: 1
		Maskable	Internal: 19, external: 8
			• 4 programmable priority levels • 3 service modes: vectored interrupt/macro service/context switching
★	Supply voltage		V_{DD} = 2.7 to 5.5 V
★	Package		100-pin plastic LQFP (fine pitch) (14 × 14 mm) 100-pin plastic QFP (14 × 20 mm)

CONTENTS

1. DIFFERENCES AMONG MODELS IN μPD784216Y SUBSERIES

The only difference among the μPD784214Y, 784215Y, and 784216Y lies in the internal memory capacity.

The μPD78F4216Y is provided with a 128-Kbytes flash memory instead of the mask ROM of the above models. These differences are summarized in Table 1-1.

★ **Table 1-1. Differences among Models in μPD784216Y Subseries**

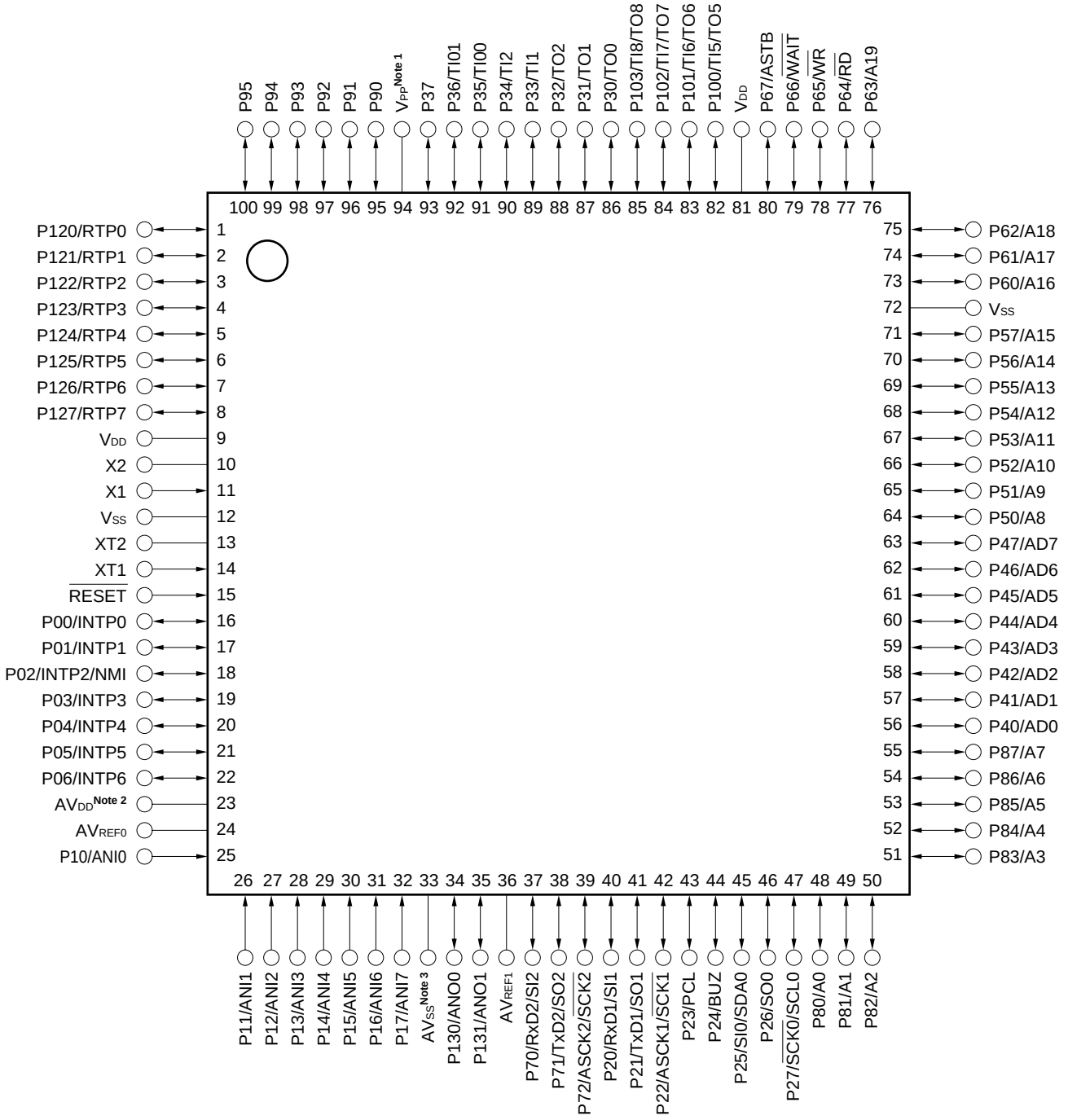
Item \ Part Number	μPD784214Y	μPD784215Y	μPD784216Y	μPD78F4216Y
Internal ROM	96 Kbytes (mask ROM)	128 Kbytes (mask ROM)		128 Kbytes (Flash memory)
Internal RAM	3584 bytes	5120 bytes	8192 bytes	
Internal memory size switching register (IMS)	None			Provided[Note]
Supply voltage	V_{DD} = 2.2 to 5.5 V			V_{DD} = 2.7 to 5.5 V
CPU clock	Main system clock, subsystem clock			Main system clock
Electrical specifications	Refer to the Data Sheet for each devices			
Recommended soldering conditions				
TEST pins	Provided			None
V_{PP} pin	None			Provided

Note The internal flash memory capacity and the internal RAM capacity can be changed with the internal memory size switching register (IMS).

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the commercial samples (not engineering samples) of the mask ROM version.

2. PIN CONFIGURATION (Top View)

★ • **100-pin plastic LQFP (fine pitch) (14 × 14 mm)**
μPD78F4216YGC-8EU

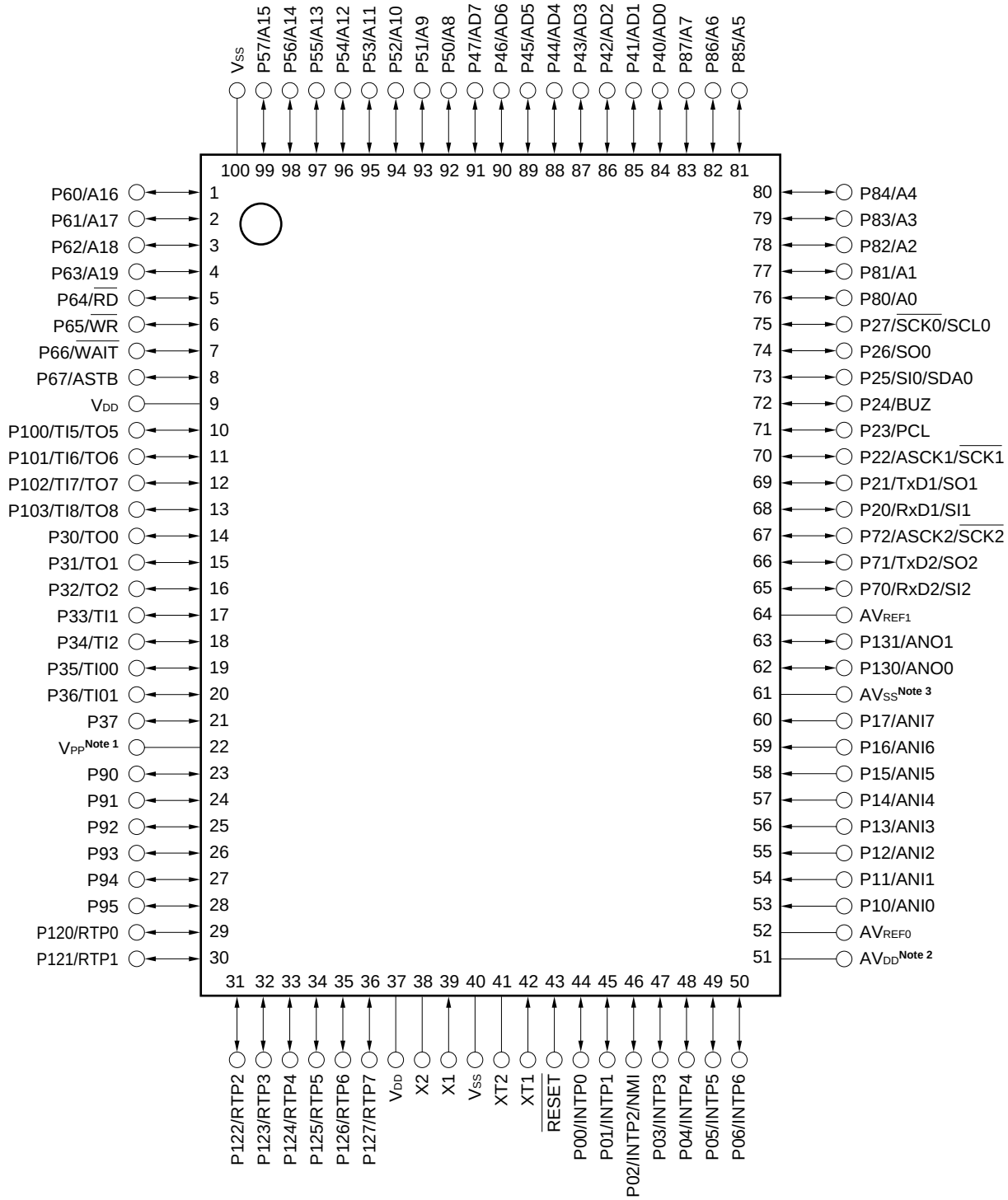


Notes 1. Connect the V_{PP} pin directly to V_{SS} in normal operation mode.

2. Connect the AV_{DD} pin to V_{DD}.

3. Connect the AV_{SS} pin to V_{SS}.

- **100-pin plastic QFP (14 × 20 mm)**
  μPD78F4216YGF-3BA



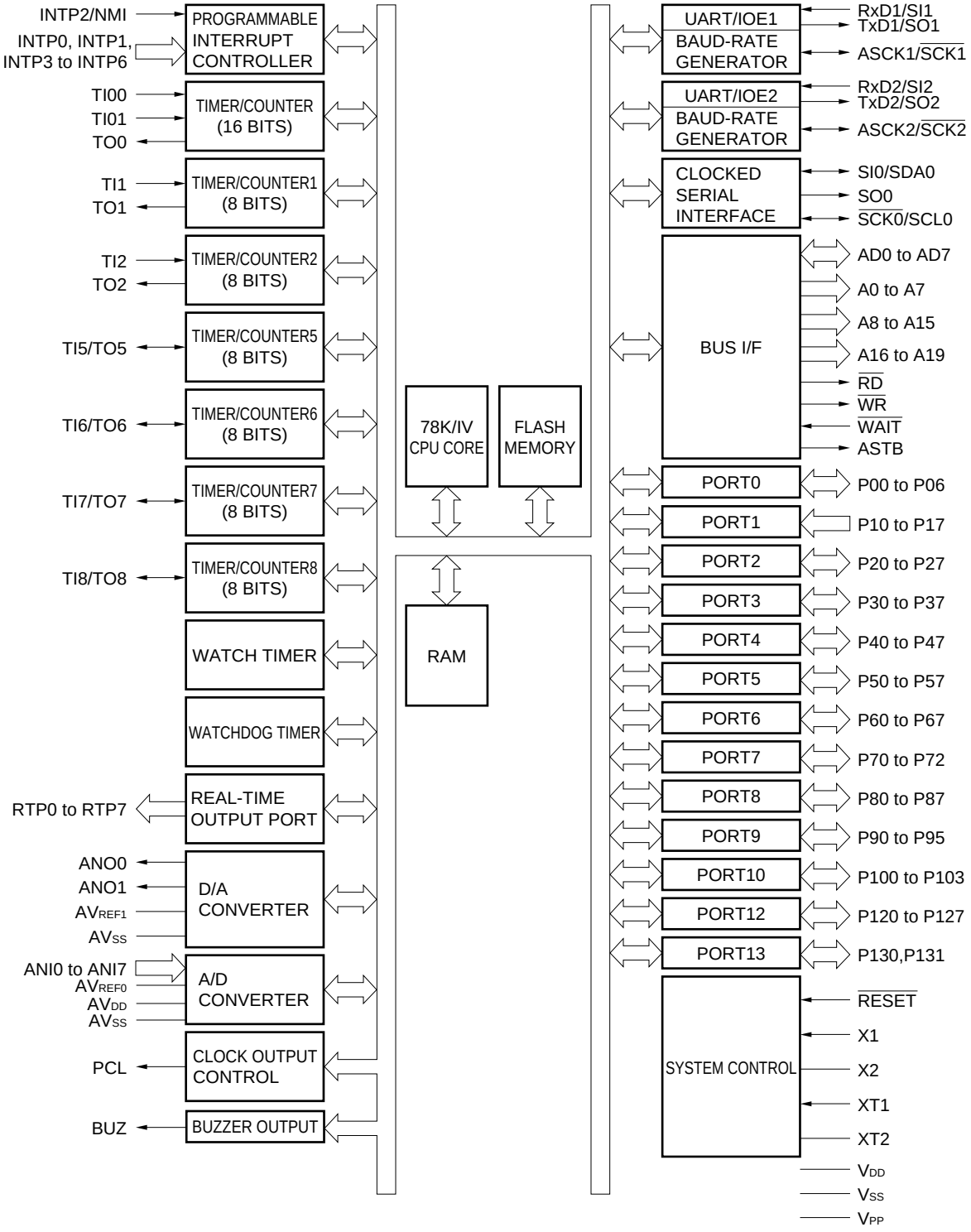
Notes 1. Connect the V_{PP} pin directly to V_{SS} in normal operation mode.

2. Connect the AV_{DD} pin to V_{DD}.

3. Connect the AV_{SS} pin to V_{SS}.

A0 to A19:	Address Bus	P130, P131:	Port13
AD0 to AD7:	Address/Data Bus	PCL:	Programmable Clock
ANI0 to ANI7:	Analog Input	$\overline{RD}$:	Read Strobe
ANO0, ANO1:	Analog Output	$\overline{RESET}$:	Reset
ASCK1, ASCK2:	Asynchronous Serial Clock	RTP0 to RTP7:	Real-time Output Port
ASTB:	Address Strobe	RxD1, RxD2:	Receive Data
AV_{DD}:	Analog Power Supply	$\overline{SCK0}$ to $\overline{SCK2}$:	Serial Clock
AV_{REF0}, AV_{REF1}:	Analog Reference Voltage	SCL0:	Serial Clock
AV_{SS}:	Analog Ground	SDA0:	Serial Data
BUZ:	Buzzer Clock	SI0 to SI2:	Serial Input
INTP0 to INTP6:	Interrupt from Peripherals	SO0 to SO2:	Serial Output
NMI:	Non-maskable Interrupt	TI00, TI01,	
P00 to P06:	Port0	TI1, TI2, TI5 to TI8:	Timer Input
P10 to P17:	Port1	TO0 to TO2,	
P20 to P27:	Port2	TO5 to TO8:	Timer Output
P30 to P37:	Port3	TxD1, TxD2:	Transmit Data
P40 to P47:	Port4	V_{DD}:	Power Supply
P50 to P57:	Port5	V_{PP}:	Programming Power Supply
P60 to P67:	Port6	V_{SS}:	Ground
P70 to P72:	Port7	$\overline{WAIT}$:	Wait
P80 to P87:	Port8	$\overline{WR}$:	Write Strobe
P90 to P95:	Port9	X1, X2:	Crystal (Main System Clock)
P100 to P103:	Port10	XT1, XT2:	Crystal (Subsystem Clock)
P120 to P127:	Port12		

3. BLOCK DIAGRAM



4. PIN FUNCTION

4.1 Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function
P00	I/O	INTP0	Port 0 (P0): • 7-bit I/O port • Input/output can be specified in 1-bit units. • Whether specifying input mode or output mode, an on-chip pull-up resistor can be specified in 1-bit units by means of software.
P01		INTP1	
P02		INTP2/NM1	
★ P03		INTP3	
P04		INTP4	
P05		INTP5	
P06		INTP6	
P10 to P17	Input	ANI0 to ANI7	Port 1 (P1): • 8-bit dedicated input port
P20	I/O	RxD1/SI1	Port 2 (P2): • 8-bit I/O port • Input/output can be specified in 1-bit units. • Whether specifying input mode or output mode, an on-chip pull-up resistor can be specified in 1-bit units by means of software.
P21		TxD1/SO1	
P22		ASCK1/$\overline{\text{SCK1}}$	
★ P23		PCL	
P24		BUZ	
P25		SI0/SDA0	
P26		SO0	
P27		$\overline{\text{SCK0}}$/SCL0	
P30	I/O	TO0	Port 3 (P3): • 8-bit I/O port • Input/output can be specified in 1-bit units. • Whether specifying input mode or output mode, an on-chip pull-up resistor can be specified in 1-bit units by means of software.
P31		TO1	
P32		TO2	
★ P33		TI1	
P34		TI2	
P35		TI00	
P36		TI01	
P37		—	
P40 to P47	I/O	AD0 to AD7	Port 4 (P4): • 8-bit I/O port • Input/output can be specified in 1-bit units. • For all pins set in input mode, an on-chip pull-up resistor can be specified in one operation by means of software. • LEDs can be driven directly.
P50 to P57	I/O	A8 to A15	Port 5 (P5): • 8-bit I/O port • Input/output can be specified in 1-bit units. • For all pins set in input mode, an on-chip pull-up resistor can be specified in one operation by means of software. • LEDs can be driven directly.

4.1 Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
P60	I/O	A16	Port 6 (P6): • 8-bit I/O port • Input/output can be specified in 1-bit units. • For all pins set in input mode, an on-chip pull-up resistor can be specified in one operation by means of software.
P61		A17	
P62		A18	
P63		A19	
P64		$\overline{RD}$	
P65		$\overline{WR}$	
P66		$\overline{WAIT}$	
P67		ASTB	
P70	I/O	RxD2/SI2	Port 7 (P7): • 3-bit I/O port • Input/output can be specified in 1-bit units. • Whether specifying input mode or output mode, an on-chip pull-up resistor can be specified in 1-bit units by means of software.
★ P71		TxD2/SO2	
P72		ASCK2/$\overline{SCK2}$	
P80 to P87	I/O	A0 to A7	Port 8 (P8): • 8-bit I/O port • Input/output can be specified in 1-bit units. • Whether specifying input mode or output mode, an on-chip pull-up resistor can be specified in 1-bit units by means of software. • Interrupt control flag (KRIF) is set to 1 when falling edge is detected at a pin of this port.
P90 to P95	I/O	—	Port 9 (P9): • N-ch open-drain middle-voltage I/O port • 6-bit I/O port • Input/output can be specified in 1-bit units. • LEDs can be driven directly.
P100	I/O	TI5/TO5	Port 10 (P10): • 4-bit I/O port • Input/output can be specified in 1-bit units. • Whether specifying input mode or output mode, an on-chip pull-up resistor can be specified in 1-bit units by means of software.
P101		TI6/TO6	
★ P102		TI7/TO7	
P103		TI8/TO8	
P120 to P127	I/O	RTP0 to RTP7	Port 12 (P12): • 8-bit I/O port • Input/output can be specified in 1-bit units. • Whether specifying input mode or output mode, an on-chip pull-up resistor can be specified in 1-bit units by means of software.
★			
P130, P131	I/O	ANO0, ANO1	Port 13 (P13): • 2-bit I/O port • Input/output can be specified in 1-bit units.

4.2 Non-Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function
TI00	Input	P35	External count clock input to 16-bit timer register
TI01		P36	Capture trigger signal input to capture/compare register 00
TI1		P33	External count clock input to 8-bit timer register 1
TI2		P34	External count clock input to 8-bit timer register 2
TI5		P100/TO5	External count clock input to 8-bit timer register 5
TI6		P101/TO6	External count clock input to 8-bit timer register 6
TI7		P102/TO7	External count clock input to 8-bit timer register 7
TI8		P103/TO8	External count clock input to 8-bit timer register 8
TO0	Output	P30	16-bit timer output (shared by 14-bit PWM output)
TO1		P31	8-bit timer output (shared by 8-bit PWM output)
TO2		P32	
TO5		P100/TI5	
TO6		P101/TI6	
TO7		P102/TI7	
TO8		P103/TI8	
RxD1	Input	P20/SI1	Serial data input (UART1)
RxD2		P70/SI2	Serial data input (UART2)
TxD1	Output	P21/SO1	Serial data output (UART1)
TxD2		P71/SO2	Serial data output (UART2)
ASCK1	Input	P22/$\overline{\text{SCK1}}$	Baud rate clock input (UART1)
ASCK2		P72/$\overline{\text{SCK2}}$	Baud rate clock input (UART2)
SI0	Input	P25/SDA0	Serial data input (3-wire serial I/O0)
SI1		P20/RxD1	Serial data input (3-wire serial I/O1)
SI2		P70/RxD2	Serial data input (3-wire serial I/O2)
SO0	Output	P26	Serial data output (3-wire serial I/O0)
SO1		P21/TxD1	Serial data output (3-wire serial I/O1)
SO2		P71/TxD2	Serial data output (3-wire serial I/O2)
SDA0	I/O	P25/SI0	Serial data input/output (I^2C bus)
$\overline{\text{SCK0}}$	I/O	P27/SCL0	Serial clock input/output (3-wire serial I/O0)
$\overline{\text{SCK1}}$		P22/ASCK1	Serial clock input/output (3-wire serial I/O1)
$\overline{\text{SCK2}}$		P72/ASCK2	Serial clock input/output (3-wire serial I/O2)
SCL0		P27/$\overline{\text{SCK0}}$	Serial clock input/output (I^2C bus)
NMI	Input	P02/INTP2	Non-maskable interrupt request input
INTP0		P00	External interrupt request input
INTP1		P01	
INTP2		P02/NMI	
INTP3		P03	
INTP4		P04	
INTP5		P05	
INTP6		P06	

4.2 Pins Other Than Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
PCL	Output	P23	Clock output (for trimming of main system clock and subsystem clock)
BUZ	Output	P24	Buzzer output
RTP0 to RTP7	Output	P120 to P127	Real-time output port from which data is output in synchronization with trigger
AD0 to AD7	I/O	P40 to P47	Lower address/data bus for expanding memory externally
A0 to A7	Output	P80 to P87	Lower address bus for expanding memory externally
A8 to A15		P50 to P57	Middle address bus for expanding memory externally
A16 to A19		P60 to P63	Higher address bus for expanding memory externally
$\overline{RD}$	Output	P64	Strobe signal output for reading from external memory
$\overline{WR}$		P65	Strobe signal output for writing external memory
$\overline{WAIT}$	Input	P66	Wait insertion at external memory access
ASTB	Output	P67	Strobe output that externally latches address information output to ports 4 through 6 and port 8 to access external memory
$\overline{RESET}$	Input	—	System reset input
X1	Input	—	Connecting crystal resonator for main system clock oscillation
X2	—		
XT1	Input	—	Connecting crystal resonator for subsystem clock oscillation
XT2	—		
ANI0 to ANI7	Input	P10 to P17	A/D converter analog voltage input
ANO0, ANO1	Output	P130, P131	D/A converter analog voltage output
AV_{REF0}	—	—	To apply A/D converter reference voltage
AV_{REF1}			To apply D/A converter reference voltage
AV_{DD}			A/D converter positive power supply. Connect to V_{DD}.
AV_{SS}			GND for A/D converter and D/A converter. Connect to V_{SS}.
V_{DD}			Positive power supply
V_{SS}			GND
★ V_{PP}			Sets flash memory programming mode. To apply a high voltage when program is written or verified. In normal operation mode, connect directly to V_{SS}.

4.3 Pin Input/Output Circuit and Recommended Connections of Unused Pins

Table 4-1 shows symbols indicating the input/output circuit types of the respective pins and the recommended connection of unused pins.

For the circuit diagram of each type of input/output circuit, refer to Figure 4-1.

Table 4-1. Types of Pin Input/Output Circuits and Recommended Connections of Unused Pins (1/2)

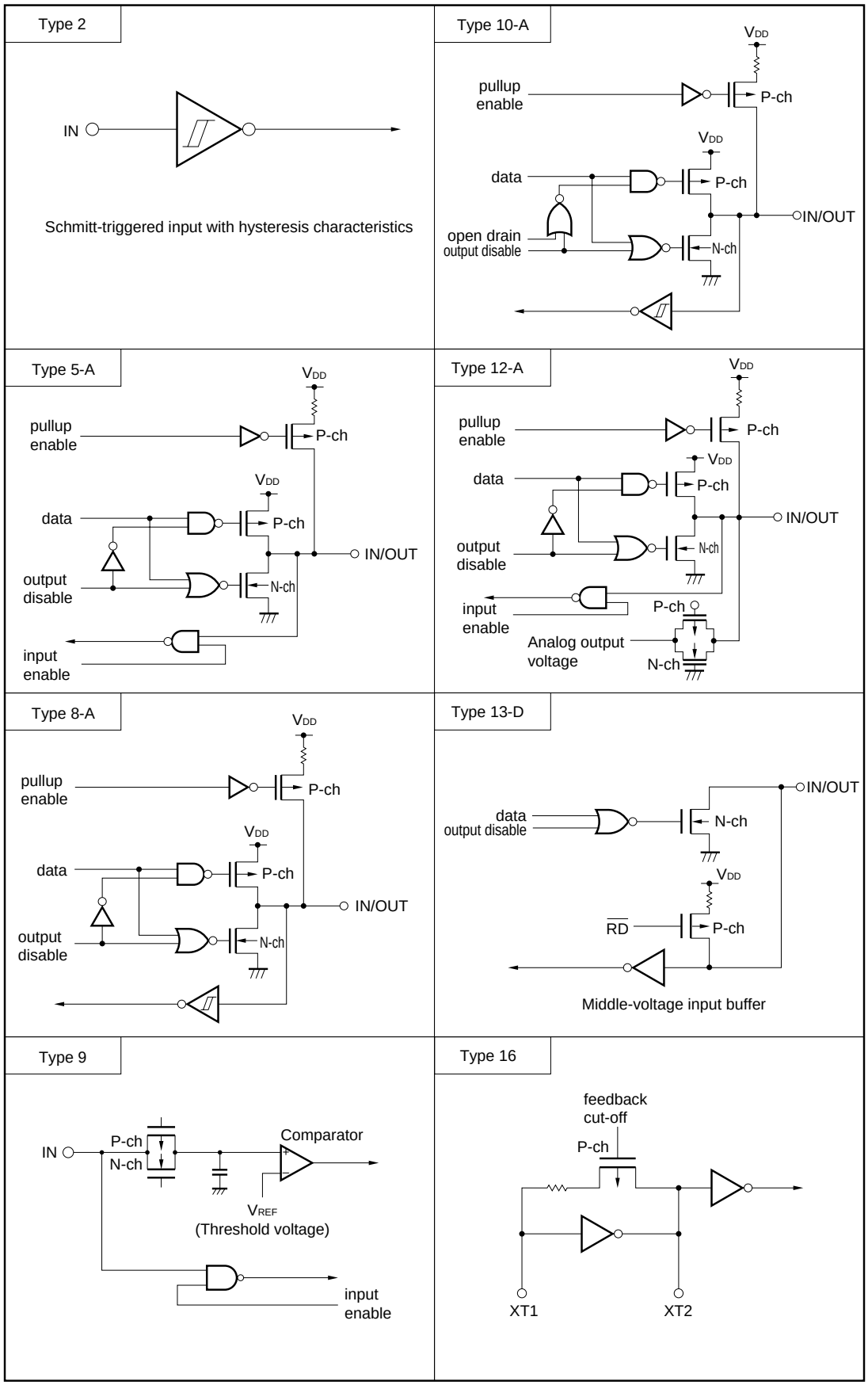
Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
P00/INTP0	8-A	I/O	Input: Independently connect to V_{SS} via a resistor Output: Leave open
P01/INTP1			
P02/INTP2/NMI			
P03/INTP3 to P06/INTP6			
P10/ANI0 to P17/ANI7	9	Input	Connect to V_{SS} or V_{DD}
P20/RxD1/SI1	10-A	I/O	Input: Independently connect to V_{SS} via a resistor Output: Leave open
P21/TxD1/SO1			
P22/ASCK1/$\overline{SCK1}$			
P23/PCL			
P24/BUZ			
P25/SDA0/SI0			
P26/SO0			
P27/SCL0/$\overline{SCK0}$			
P30/TO0 to P32/TO2	8-A		
P33/TI1, P34/TI2			
P35/TI00, P36/TI01			
P37			
P40/AD0 to P47/AD7	5-A		
P50/A8 to P57/A15			
P60/A16 to P63/A19			
P64/$\overline{RD}$			
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
P70/RxD2/SI2	8-A		
P71/TxD2/SO2			
P72/ASCK2/$\overline{SCK2}$			
P80/A0 to P87/A7			
P90 to P95	13-D		
P100/TI5/TO5	8-A		
P101/TI6/TO6			
P102/TI7/TO7			
P103/TI8/TO8			
P120/RTP0 to P127/RTP7			
P130/ANO0, P131/ANO1	12-A		

Table 4-1. Types of Pin Input/Output Circuits and Recommended Connections of Unused Pins (2/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
$\overline{\text{RESET}}$	2	Input	—
XT1	16		Connect to V_{SS}
XT2		—	Leave open
AV_{REF0}	—		Connect to V_{SS}
AV_{REF1}			Connect to V_{DD}
AV_{DD}			
AV_{SS}			Connect to V_{SS}
V_{PP}			Connect directly to V_{SS}

Remark Because the circuit type numbers are standardized among the 78K Series products, they are not sequential in some models (i.e., some circuits are not provided).

Figure 4-1. Types of Pin Input/Output Circuits



5. INTERNAL MEMORY SIZE SWITCHING REGISTER (IMS)

The IMS is a register that prevents a part of the internal memory from being used by means of software. By setting this register, the memory of the μPD78F4216Y can be mapped in the same manner as a mask ROM model with different internal memory (ROM and RAM) capacity.

This register is set by using an 8-bit memory manipulation instruction.

Its value is set to FFH by $\overline{\text{RESET}}$ input.

Figure 5-1. Format of Internal Memory Size Switching Register (IMS)

Address: 0FFFCH At reset: FFH W

	7	6	5	4	3	2	1	0
IMS	1	1	ROM1	ROM0	1	1	RAM1	RAM0

ROM1	ROM0	Selects internal ROM capacity
0	0	48 Kbytes
0	1	64 Kbytes
1	0	96 Kbytes
1	1	128 Kbytes

RAM1	RAM0	Selects peripheral RAM capacity
0	0	3072 bytes
0	1	4608 bytes
1	0	6114 bytes
1	1	7680 bytes

Caution IMS is not provided on the mask ROM models (μPD784214Y, 784215Y, and 784216Y).

The value to be set to the IMS to map the memory of the μPD78F4216Y in the same manner as the mask ROM model is shown in Table 5-1.

Table 5-1. Set Value of Internal Memory Size Switching Register (IMS)

Mask ROM Model	Set Value of IMS
μPD784214Y	ECH
μPD784215Y	FDH
μPD784216Y	FFH

6. PROGRAMMING FLASH MEMORY

The flash memory can be written with the μPD78F4216Y mounted on the target board (on-board). To do so, ★ connect a dedicated flash programmer (Flashpro II (Model number: FL-PR2), Flashpro III (Model number: FL-PR3, PG-FP3)) to the host machine and target system.

★ **Remark** FL-PR2 and FL-PR3 are products of Naitou Densei Machidaseisakusho Co., Ltd.

6.1 Selecting Communication Mode

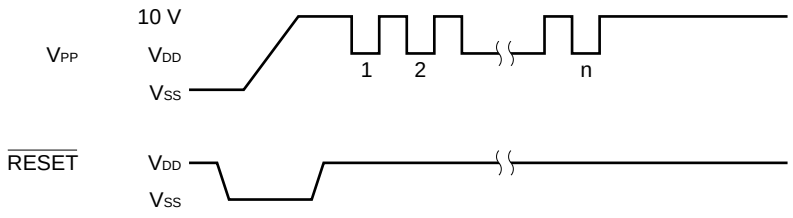
To write the flash memory, use Flashpro II and Flashpro III with serial communication. Select a serial communication mode from those listed in Table 6-1 in the format shown in Figure 6-1. Each communication mode is selected by the number of V_{PP} pulses shown in Table 6-1.

Table 6-1. Communication Modes

Communication Mode	Number of Channels	Pins Used	Number of V_{PP} Pulses
3-wire serial I/O	3	$\overline{SCK0}$/SCL0/P27 SO0/P26 SI0/SDA0/P25	0
		$\overline{SCK1}$/ASCK1/P22 SO1/TxD1/P21 SI1/RxD1/P20	1
		$\overline{SCK2}$/ASCK2/P72 SO2/TxD2/P71 SI2/RxD2/P70	2
UART	2	TxD1/SO1/P21 RxD1/SI1/P20	8
		TxD2/SO2/P71 RxD2/SI2/P70	9

Caution Be sure to select a communication mode with the number of V_{PP} pulses shown in Table 6-1.

Figure 6-1. Communication Mode Selecting Format



6.2 Flash Memory Programming Function

The flash memory is written by transmitting or receiving commands and data in a selected communication mode. The major functions of flash memory programming are listed in Table 6-2.

Table 6-2. Major Functions of Flash Memory Programming

Function	Description
Batch erasure	Erases all contents of memory.
Block erasure	Erases contents of specified memory block with one memory block consisting of 16 Kbytes.
Batch blank check	Checks erased status of entire memory.
Block blank check	Checks erased status of specified block
Data write	Writes flash memory based on write start address and number of data to be written (in bytes).
Batch verify	Compares all contents of memory with input data.
Block verify	Compares contents of specified memory block with input data.

6.3 Connecting Flashpro II, Flashpro III

The Flashpro II, Flashpro III and μPD78F4216Y are connected differently depending on the selected communication mode (3-wire serial I/O or UART). Figures 6-2 and 6-3 show the connections in the respective communication modes.

Figure 6-2. Connection of Flashpro II, Flashpro III in 3-Wire Serial I/O Mode

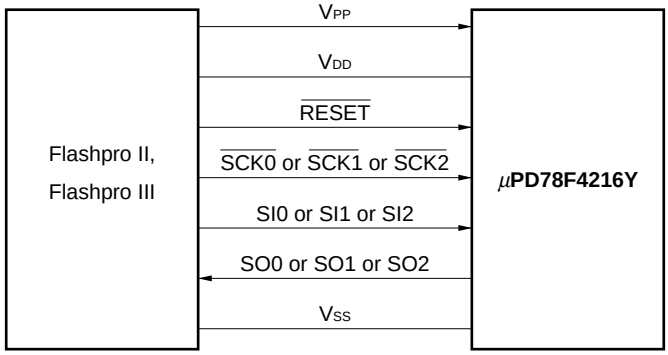
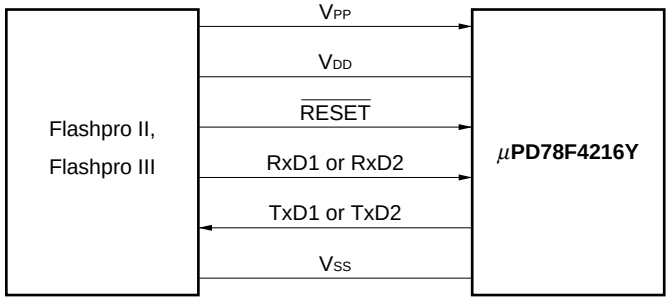


Figure 6-3. Connection of Flashpro II, Flashpro III in UART Mode



★ 7. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to V_{SS} + 0.3	V
	AV_{REF0}	A/D converter reference voltage input		–0.3 to V_{DD} + 0.3	V
	AV_{REF1}	D/A converter reference voltage input		–0.3 to V_{DD} + 0.3	V
Input voltage	V_{I1}	Other than P90 to P95		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P90 to P95	N-ch open drain	–0.3 to +12	V
Analog input voltage	V_{AN}	Analog input pin		AV_{SS} – 0.3 to AV_{REF0} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current, low	I_{OL}	Per pin		15	mA
		Total for all pins of Ports 2, 4 to 8		75	mA
		Total for all pins of Ports 0, 3, 9, 10, 12, and 13		75	mA
Output current, high	I_{OH}	Per pin		–10	mA
		Total for all pins of Ports 2, 4 to 8		–50	mA
		Total for all pins of Ports 0, 3, 9, 10, 12, and 13		–50	mA
Operating ambient temperature	T_A			–10 to +60	°C
Storage temperature	T_{stg}			–10 to +80	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

<< Restriction >>

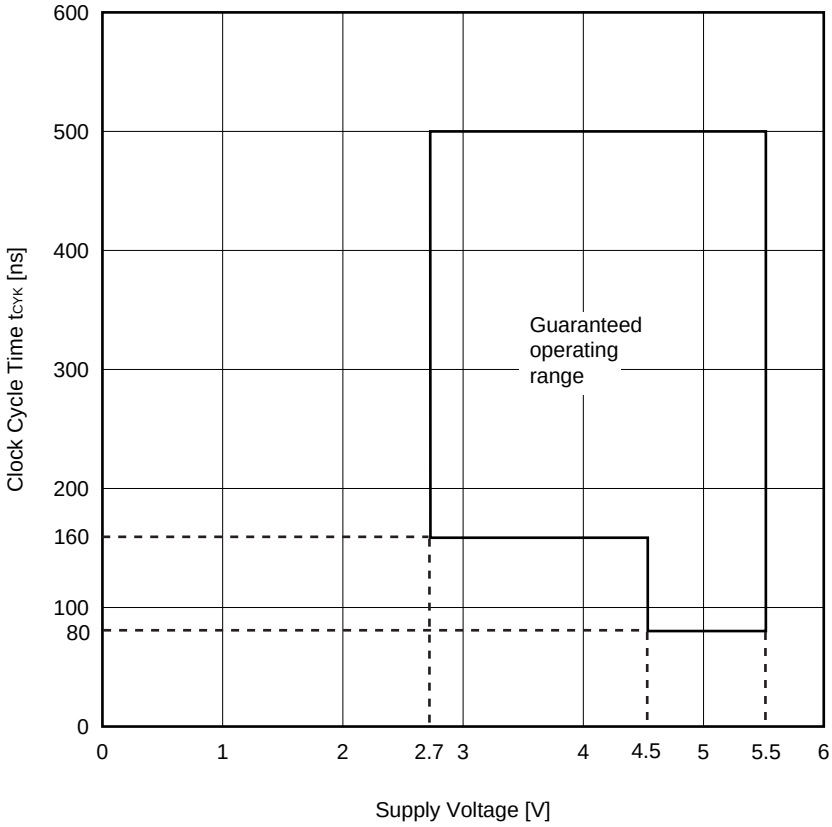
Do not select the subsystem clock as the operation clock of CPU.

When the operation clock of CPU is supplied from the subsystem clock, a malfunction may occur in the μPD78F4216Y.

Operating Conditions

- Operating ambient temperature (T_A): –10 to +60°C
- Supply voltage and clock cycle time: See Figure 7-1

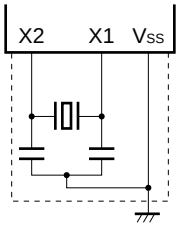
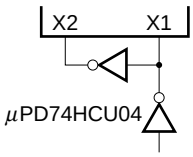
Figure 7-1. Supply Voltage and Clock Cycle Time



CAPACITANCE (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz Unmeasured pins returned to 0 V.	Other than Port 9			15	pF
			Port 9			20	pF
Output capacitance	C_O		Other than Port 9			15	pF
			Port 9			20	pF
I/O capacitance	C_{IO}		Other than Port 9			15	pF
			Port 9			20	pF

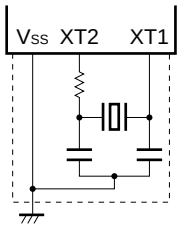
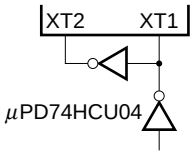
Main System Clock Oscillator Characteristics (T_A = –10 to +60°C)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator or crystal resonator		Oscillation frequency (f_X)	4.5 V ≤ V_{DD} ≤ 5.5 V	2		12.5	MHz
			2.7 V ≤ V_{DD} < 4.5 V	2		6.25	
External clock		X1 input frequency (f_X)	4.5 V ≤ V_{DD} ≤ 5.5 V	2		25	MHz
			2.7 V ≤ V_{DD} < 4.5 V	2		12.5	
		X1 input high/low-level width (t_{WXH}, t_{WXL})		35		250	ns
		X1 input rise/ fall time (t_{XR}, t_{XF})	4.5 V ≤ V_{DD} ≤ 5.5 V	0		5	ns
			2.7 V ≤ V_{DD} < 4.5 V	0		10	

Caution When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor in a ground pattern in which a high current flows.**
- **Do not fetch signals from the oscillator.**

Subsystem Clock Oscillator Characteristics (T_A = –10 to +60°C)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})		32	32.768	35	kHz
		Oscillation stabilization time[Note]	4.5 V ≤ V_{DD} ≤ 5.5 V		1.2	2	s
			2.7 V ≤ V_{DD} < 4.5 V			10	
External clock		XT1 input frequency (f_{XT})		32		35	kHz
		XT1 input high/low-level width (t_{XTH}, t_{XTL})		5		15	μs

Note Time required to stabilize oscillation after V_{DD} reaches oscillator voltage MIN.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern in which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Do not select the subsystem clock as the operation clock of CPU.
When the operation clock of CPU is supplied from subsystem clock, a malfunction may occur in the μPD78F4216Y.

DC Characteristics (T_A = –10 to +60°C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V) (1/2)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input voltage, low	V_{IL1}	**Note**		0		0.3 V_{DD}	V
	V_{IL2}	Total for P00 to P06, P20, P22, P33, P34, P70, P72, P100 to P103, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V
	V_{IL3}	P90 to P95 (N-ch open drain)		0		0.3 V_{DD}	V
	V_{IL4}	Total for P10 to P17, P130, P131		0		0.3 V_{DD}	V
	V_{IL5}	Total for X1, X2, XT1, XT2		0		0.2 V_{DD}	V
	V_{IL6}	P25, P27		0		0.3 V_{DD}	V
Input voltage, high	V_{IH1}	**Note**		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	Total for P00 to P06, P20, P22, P33, P34, P70, P72, P100 to P103, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	P90 to P95 (N-ch open drain)		0.7 V_{DD}		12	V
	V_{IH4}	Total for P10 to P17, P130, P131		0.7 V_{DD}		V_{DD}	V
	V_{IH5}	Total for X1, X2, XT1, XT2		0.8 V_{DD}		V_{DD}	V
	V_{IH6}	P25, P27		0.7 V_{DD}		V_{DD}	V
Output voltage, low	V_{OL1}	For pins other than P40 to P47, P50 to P57, P90 to P95 I_{OL} = 1.6 mA	V_{DD} = 4.5 to 5.5 V			0.4	V
		Total for P40 to P47, P50 to P57 I_{OL} = 8 mA	V_{DD} = 4.5 to 5.5 V			1.0	V
		P90 to P95 I_{OL} = 15 mA	V_{DD} = 4.5 to 5.5 V		0.4	2.0	V
	V_{OL2}	I_{OL} = 400 μA				0.5	V
Output voltage, high	V_{OH1}	I_{OH} = –1 mA	V_{DD} = 4.5 to 5.5 V	V_{DD}–1.0			V
		I_{OL} = –100 μA		V_{DD}–0.5			V
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	Except X1, X2, XT1, XT2			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
Input leakage current, high	I_{LIH1}	V_{IN} = V_{DD}	Except X1, X2, XT1, XT2			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
Output leakage current, low	I_{LOL1}	V_{OUT} = 0 V				–3	μA
Output leakage current, high	I_{LOH1}	V_{OUT} = V_{DD}				3	μA

Note P21, P23, P24, P26, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P71, P80 to P87, P120 to P127

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –10 to +60°C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V) (2/2)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1}	Operation mode	f_{XX} = 12.5 MHz			40	mA
			f_{XX} = 6 MHz, V_{DD} = 2.7 to 3.3 V			20	mA
	I_{DD2}	HALT mode	f_{XX} = 12.5 MHz			20	mA
			f_{XX} = 6 MHz, V_{DD} = 2.7 to 3.3 V			10	mA
	I_{DD3}	IDLE mode	f_{XX} = 12.5 MHz			20	mA
			f_{XX} = 6 MHz, V_{DD} = 2.7 to 3.3 V			10	mA
Data retention voltage	V_{DDDR}	HALT, IDLE modes		2.7		5.5	V
Data retention current	I_{DDDR}	STOP mode	V_{DD} = 2.7 V		2	10	μA
			V_{DD} = 4.5 to 5.5 V		10	50	μA
Pull-up resistor	R_L	V_{IN} = 0 V		10	30	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics (T_A = –10 to +60°C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(1) Read/write operation (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Minimum Instruciton execution time)	t_{CYK}	4.5 V ≤ V_{DD} ≤ 5.5 V		80			ns
		2.7 V ≤ V_{DD} < 4.5 V		160			ns
Address setup time (to ASTB↓)	t_{SAST}	V_{DD} = 5.0 V	(0.5 + a) T – 11	29			ns
		V_{DD} = 3.0 V	(0.5 + a) T – 15	65			ns
Address hold time (from ASTB↓)	t_{HSTLA}	V_{DD} = 5.0 V	0.5T – 19	21			ns
		V_{DD} = 3.0 V	0.5T – 24	56			ns
ASTB high-level width	t_{WSTH}	V_{DD} = 5.0 V	(0.5 + a) T – 17	23			ns
		V_{DD} = 3.0 V	(0.5 + a) T – 40	40			ns
Address hold time (from $\overline{RD}$↑)	t_{HRA}	V_{DD} = 5.0 V	0.5T – 14	26			ns
		V_{DD} = 3.0 V	0.5T – 14	66			ns
$\overline{RD}$↓ delay time from address	t_{DAR}	V_{DD} = 5.0 V	(1 + a) T – 24	56			ns
		V_{DD} = 3.0 V	(1 + a) T – 24	136			ns
Address float time (from $\overline{RD}$↓)	t_{FRA}			0			ns
Data input time from address	t_{DAID}	V_{DD} = 5.0 V	(2.5 + a + n) T – 37			403	ns
		V_{DD} = 3.0 V	(2.5 + a + n) T – 52			828	ns
Data input time from ASTB↓	t_{DSTID}	V_{DD} = 5.0 V	(2 + n) T – 35			285	ns
		V_{DD} = 3.0 V	(2 + n) T – 50			590	ns
Data input time from $\overline{RD}$↓	t_{DRID}	V_{DD} = 5.0 V	(1.5 + n) T – 40			240	ns
		V_{DD} = 3.0 V	(1.5 + n) T – 50			510	ns
$\overline{RD}$↓ delay time from ASTB↓	t_{DSTR}	V_{DD} = 5.0 V	0.5T – 9	31			ns
		V_{DD} = 3.0 V	0.5T – 9	71			ns
Data hold time (from $\overline{RD}$↑)	t_{HRID}			0			ns
Address active time from $\overline{RD}$↑	t_{DRA}	V_{DD} = 5.0 V	0.5T – 2	38			ns
		V_{DD} = 3.0 V	0.5T – 12	68			ns
ASTB↑ delay time from $\overline{RD}$↑	t_{DRST}	V_{DD} = 5.0 V	0.5T – 9	31			ns
		V_{DD} = 3.0 V	0.5T – 9	71			ns
$\overline{RD}$ low-level width	t_{WRL}	V_{DD} = 5.0 V	(1.5 + n) T – 25	95			ns
		V_{DD} = 3.0 V	(1.5 + n) T – 30	210			ns
$\overline{WR}$↓ delay time from address	t_{DAW}	V_{DD} = 5.0 V	(1 + a) T – 24	56			ns
		V_{DD} = 3.0 V	(1 + a) T – 24	136			ns
Address hold time (from $\overline{WR}$↑)	t_{HWA}	V_{DD} = 5.0 V	0.5T – 14	26			ns
		V_{DD} = 3.0 V	0.5T – 14	66			ns
Data output delay time from ASTB↓	t_{DSTOD}	V_{DD} = 5.0 V	0.5T + 15			55	ns
		V_{DD} = 3.0 V	0.5T + 20			100	ns

Remark T: t_{CYK} = 1/f_{XX} (f_{XX}: main system clock frequency)
a: 1 (during address wait), otherwise, 0
n: Number of wait states (n ≥ 0)

AC Characteristics

(1) Read/write operation (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Data output delay time from $\overline{WR}\downarrow$	t_{DWOD}				10	62	ns
$\overline{WR}\downarrow$ delay time from ASTB↓	t_{DSTW}	V_{DD} = 5.0 V	0.5T – 9	31			ns
		V_{DD} = 3.0 V	0.5T – 9	71			ns
Data setup time (to $\overline{WR}\uparrow$)	t_{SODWR}	V_{DD} = 5.0 V	(1.5 + n) T – 20	100			ns
		V_{DD} = 3.0 V	(1.5 + n) T – 25	215			ns
Data hold time (from $\overline{WR}\uparrow$)	t_{HWOD}	V_{DD} = 5.0 V	0.5T – 14	26			ns
		V_{DD} = 3.0 V	0.5T – 14	66			ns
ASTB↑ delay time from $\overline{WR}\uparrow$	t_{DWST}	V_{DD} = 5.0 V	0.5T – 9	31			ns
		V_{DD} = 3.0 V	0.5T – 9	71			ns
$\overline{WR}$ low-level width	t_{WWL}	V_{DD} = 5.0 V	(1.5 + n) T – 25	95			ns
		V_{DD} = 3.0 V	(1.5 + n) T – 30	210			ns

Remark T: $t_{CYK} = 1/f_{XX}$ (f_{XX}: main system clock frequency)
a: 1 (during address wait), otherwise, 0
n: Number of wait states ($n \geq 0$)

AC Characteristics

(2) External wait timing

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{WAIT}$↓ input time from address	t_{DAWT}	V_{DD} = 5.0 V	(2 + a) T – 40			200	ns
		V_{DD} = 3.0 V	(2 + a) T – 60			420	ns
$\overline{WAIT}$↓ input time from ASTB↓	t_{DSTWT}	V_{DD} = 5.0 V	1.5T – 40			80	ns
		V_{DD} = 3.0 V	1.5T – 60			180	ns
$\overline{WAIT}$ hold time from ASTB↓	t_{HSTWT}	V_{DD} = 5.0 V	(0.5 + n) T + 5	125			ns
		V_{DD} = 3.0 V	(0.5 + n) T + 10	250			ns
$\overline{WAIT}$↑ delay time from ASTB↓	t_{DSTWTH}	V_{DD} = 5.0 V	(1.5 + n) T – 40			240	ns
		V_{DD} = 3.0 V	(1.5 + n) T – 60			500	ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{DRWTL}	V_{DD} = 5.0 V	T – 40			40	ns
		V_{DD} = 3.0 V	T – 60			100	ns
$\overline{WAIT}$↓ hold time from $\overline{RD}$↓	t_{HRWT}	V_{DD} = 5.0 V	nT + 5	85			ns
		V_{DD} = 3.0 V	nT + 10	170			ns
$\overline{WAIT}$↑ delay time from $\overline{RD}$↓	t_{DRWTH}	V_{DD} = 5.0 V	(1 + n) T – 40			200	ns
		V_{DD} = 3.0 V	(1 + n) T – 60			420	ns
Data input time from $\overline{WAIT}$↑	t_{DWTID}	V_{DD} = 5.0 V	0.5T – 5			35	ns
		V_{DD} = 3.0 V	0.5T – 10			70	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t_{DWTR}	V_{DD} = 5.0 V	0.5T	40			ns
		V_{DD} = 3.0 V	0.5T	80			ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t_{DWTW}	V_{DD} = 5.0 V	0.5T	40			ns
		V_{DD} = 3.0 V	0.5T	80			ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{DWWTL}	V_{DD} = 5.0 V	T – 40			40	ns
		V_{DD} = 3.0 V	T – 60			100	ns
$\overline{WAIT}$ hold time from $\overline{WR}$↓	t_{HWWT}	V_{DD} = 5.0 V	nT + 5	85			ns
		V_{DD} = 3.0 V	nT + 10	170			ns
$\overline{WAIT}$↑ delay time from $\overline{WR}$↓	t_{DWWTH}	V_{DD} = 5.0 V	(1 + n) T – 40			200	ns
		V_{DD} = 3.0 V	(1 + n) T – 60			420	ns

Remark T: t_{CYK} = 1/f_{XX} (f_{XX}: main system clock frequency)

a: 1 (during address wait), otherwise, 0

n: Number of wait states (n ≥ 0)

Serial Operation (T_A = –10 to +60°C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(a) 3-wire serial I/O mode ($\overline{SCK}$: internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Serial clock ($\overline{SCK}$) cycle time	t_{KCY1}		800			ns
Serial clock ($\overline{SCK}$) high/low-level width	t_{KH1}, t_{KL1}		350			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK1}		10			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI1}		40			ns
SO output delay time (from $\overline{SCK}$↓)	t_{KSO1}				30	ns

(b) 3-wire serial I/O mode ($\overline{SCK}$: external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Serial clock ($\overline{SCK}$) cycle time	t_{KCY2}		800			ns
Serial clock ($\overline{SCK}$) high/low-level width	t_{KH2}, t_{KL2}		400			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK2}		10			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI2}		40			ns
SO output delay time (from $\overline{SCK}$↓)	t_{KSO2}				30	ns

(c) UART mode

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY3}	4.5 V ≤ V_{DD} ≤ 5.5 V	417			ns
		2.7 V ≤ V_{DD} < 4.5 V	833			ns
ASCK high/low-level width	t_{KH3},	4.5 V ≤ V_{DD} ≤ 5.5 V	208			ns
	t_{KL3}	2.7 V ≤ V_{DD} < 4.5 V	416			ns

(d) I²C bus mode

Parameter		Symbol	Normal Operation Mode		High-Speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f_{CLK}	0	100	0	400	kHz
Bus free time (between stop and start conditions)		t_{BUF}	4.7	—	1.3	—	μs
Hold time[Note 1]		$t_{HD:STA}$	4.0	—	0.6	—	μs
SCL0 clock low-level width		t_{LOW}	4.7	—	1.3	—	μs
SCL0 clock high-level width		t_{HIGH}	4.0	—	0.6	—	μs
Start/restart condition setup time		$t_{SU:STA}$	4.7	—	0.6	—	μs
Data hold time	CBUS compatible master	$t_{HD:DAT}$	5.0	—	—	—	μs
	I²C bus		0[Note 2]	—	0[Note 2]	0.9[Note 3]	μs
Data setup time		$t_{SU:DAT}$	250	—	100[Note 4]	—	ns
Rise time of SDA0 and SCL0 signal		t_R	—	1000	20+0.1Cb[Note 5]	300	ns
Fall time of SDA0 and SCL0 signal		t_F	—	300	20+0.1Cb[Note 5]	300	ns
Stop condition setup time		$t_{SU:STO}$	4.0	—	0.6	—	μs
Spike pulse width suppressed by input filter		t_{SP}	—	—	0	50	ns
Load capacitance of each bus line		Cb	—	400	—	400	pF

Notes 1. At the start condition, the first clock pulse is generated after this hold time.

2. In order to fill out the undefined area of the falling edge of SCL0, supply a hold time internally at least 300-ns for the SDA0 signal (at $V_{IHmin.}$ of SCL0 signal).

3. When the low hold time (t_{LOW}) of the SCL0 signal is not extended, only the maximum data hold time ($t_{HD:DAT}$) should be filled.

4. High-speed mode I²C bus can be used in the normal operation mode I²C bus system. In this case, the following conditions should be met.

- When the low-state hold time (t_{LOW}) of the SCL0 signal is not extended
  $t_{SU:DAT} \geq 250$ ns
- When the low-state hold time (t_{LOW}) of the SCL0 signal is extended
  Send out the next data bits to the SDA0 line before the SCL0 line is released ($t_{Rmax.} + t_{SU:DAT} = 1000 + 250 = 1250$ ns: by normal operation mode I²C bus specification).

5. Cb: Total capacitance of a bus line (Unit: pF)

Other Operations (T_A = –10 to +60°C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
NMI high/low-level width	t_{WNIL} t_{WNIH}		10			μs
INTP input high/low-level width	t_{WITL} t_{WITH}	INTP0 to INTP6	10			μs
$\overline{RESET}$ high/low-level width	t_{WRSL} t_{WRSH}		10			μs

Clock Output Operation (T_A = –10 to +60°C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
PCL cycle time	t_{CYCL}	V_{DD} = 4.5 to 5.5 V, nT	80		31250	ns
PCL high/low-level width	t_{CLL} t_{CLH}	V_{DD} = 4.5 to 5.5 V, 0.5T – 10	30		15615	ns
PCL rise/fall time	t_{CLR} t_{CLF}	4.5 V ≤ V_{DD} ≤ 5.5 V			5	ns
		2.7 V ≤ V_{DD} < 4.5 V			10	ns

Remark T: t_{CYK} = 1/f_{XX} (f_{XX}: main system clock frequency)

n: Divided frequency ratio set by software in the CPU

- When using the main system clock: n = 1, 2, 4, 8, 16, 32, 64, 128
- When using the subsystem clock: n = 1

A/D Converter Characteristics (T_A = –10 to +60°C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Total error[Note]		2.7 V ≤ AV_{REF0} ≤ AV_{DD}			1.2	%
Conversion time	t_{CONV}		14		144	μs
Sampling time	t_{SAMP}		24/f_{XX}			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}		2.7		AV_{DD}	V
Resistance between AV_{REF0} and AV_{SS}	R_{AVREF0}			29.4		kΩ

Note Quantization error (±1/2 LSB) is not included.

Remark f_{XX}: Main system clock frequency

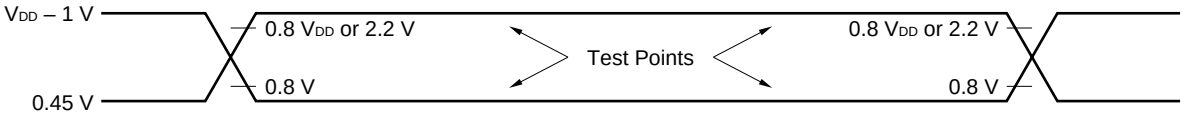
D/A Converter Characteristics (T_A = –10 to +60°C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution				8	8	8	bit
Total error		R = 2 MΩ, 2.7 V < AV_{REF1} ≤ 5.5 V				1.2	%
		R = 4 MΩ, 2.7 V < AV_{REF1} ≤ 5.5 V				0.8	%
		R = 10 MΩ, 2.7 V < AV_{REF1} ≤ 5.5 V				0.6	%
Settling time		Load conditions: C = 30 pF	4.5 V ≤ AV_{REF1} ≤ 5.5 V			10	μs
			2.7 V ≤ AV_{REF1} < 4.5 V			15	μs
Output resistance	R_O	DACS0, 1 = 7 FH			5.3		kΩ
Reference voltage	AV_{REF1}			2.7		V_{DD}	V
AV_{REF1} current	AI_{REF1}	For only 1 channel				2.5	mA

Data Retention Characteristics (T_A = –10 to +60°C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

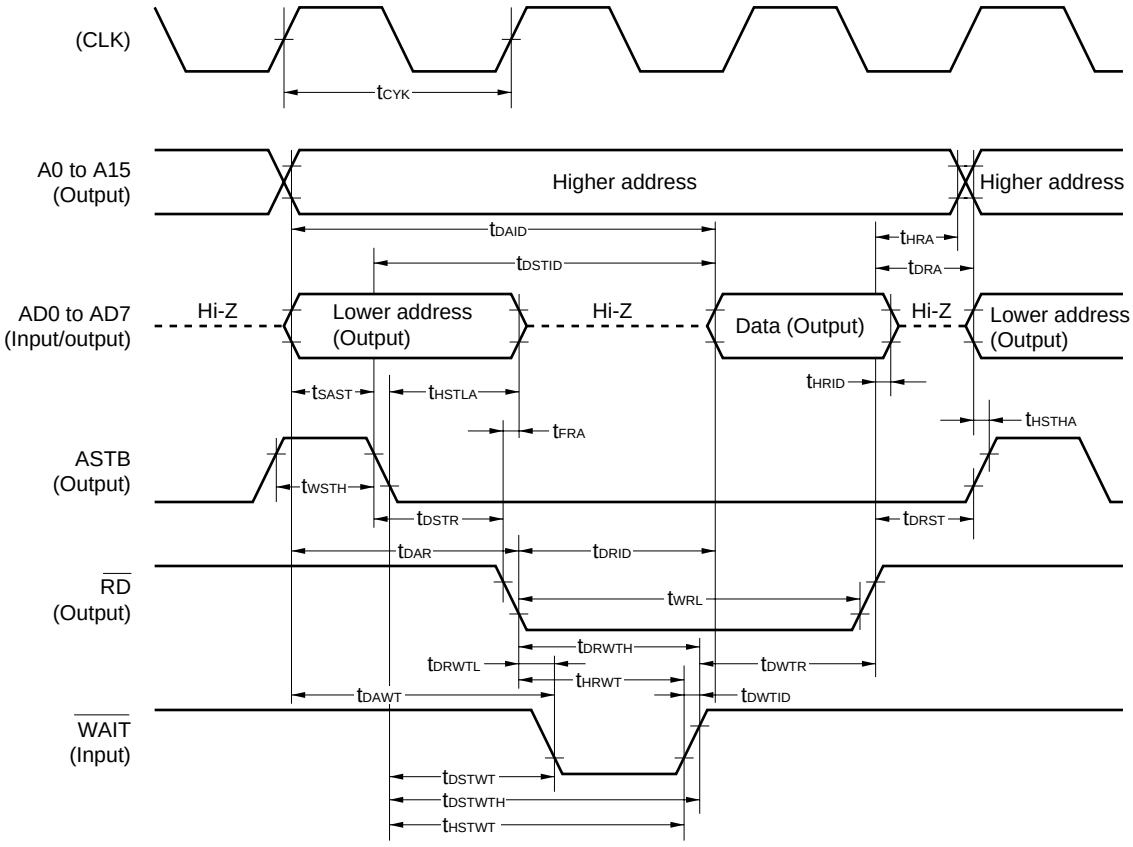
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode	2.7		5.5	V
Data retention current	I_{DDDR}	V_{DDDR} = +4.5 to 5.5 V		5	20	μA
		V_{DDDR} = +2.7 V		2	10	μA
V_{DD} rise time	t_{RVD}		200			μs
V_{DD} fall time	t_{FVD}		200			μs
V_{DD} hold time (from STOP mode setting)	t_{HVD}		0			ms
STOP release signal input time	t_{DREL}		0			ms
Oscillation stabilization wait time	t_{WAIT}	Crystal resonator	30			ms
		Ceramic resonator	5			ms
Input voltage, low	V_{IL}	$\overline{\text{RESET}}$, P00/INTP0 to P06/INTP6	0		0.1 V_{DDDR}	V
Input voltage, high	V_{IH}		0.9 V_{DDDR}		V_{DDDR}	V

AC Timing Test Points

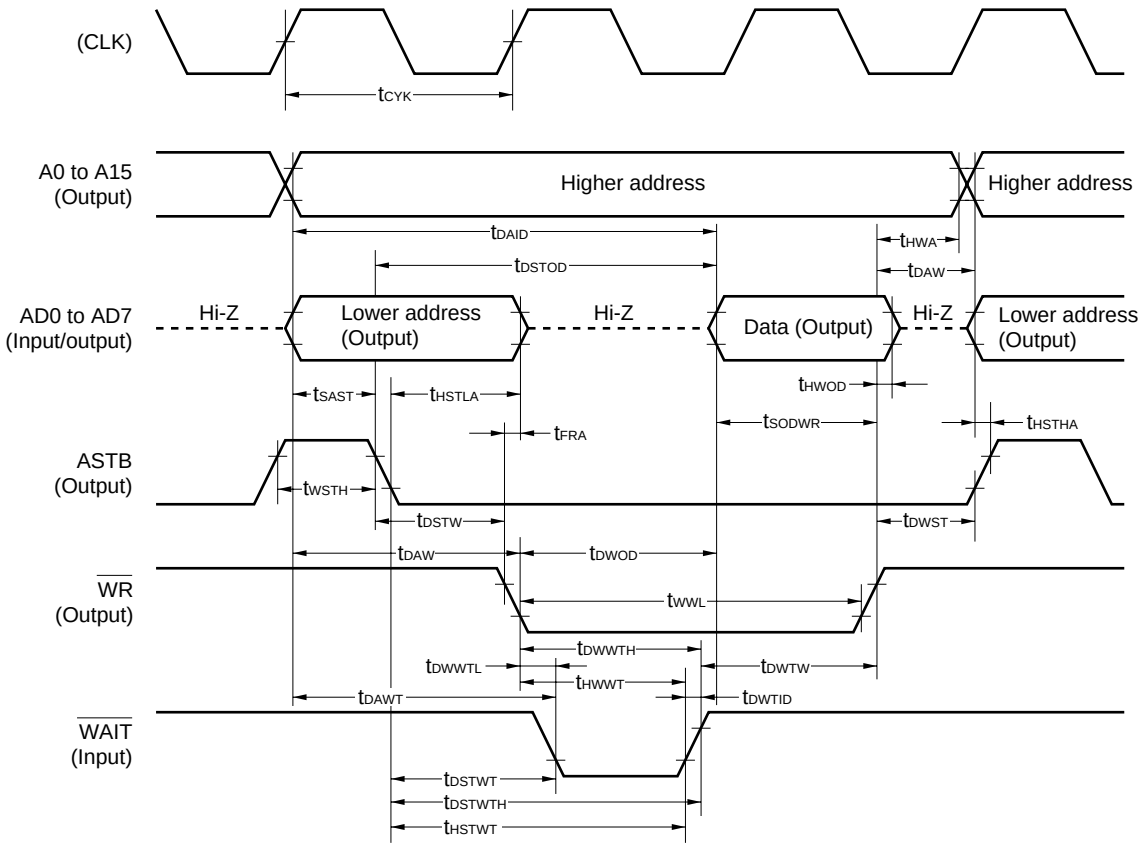


Timing Wave Form

(1) Read operation

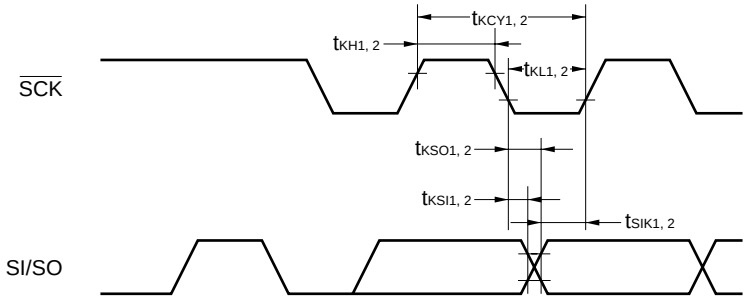


(2) Write operation

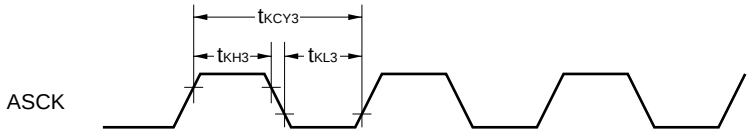


Serial Operation

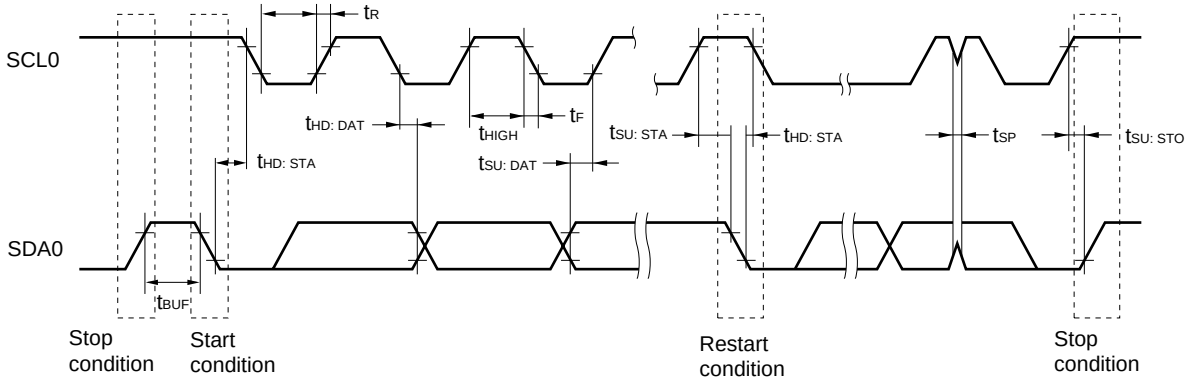
(1) 3-wire serial I/O mode



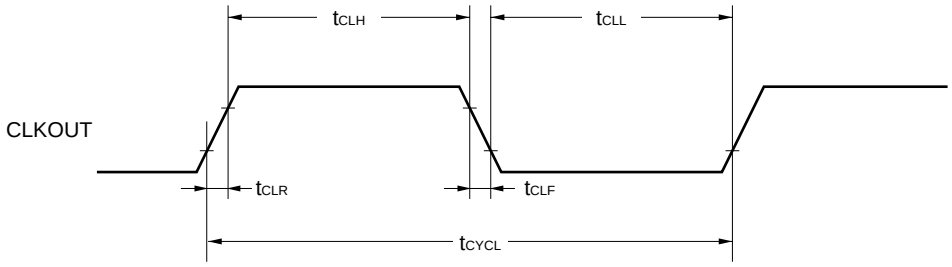
(2) UART mode



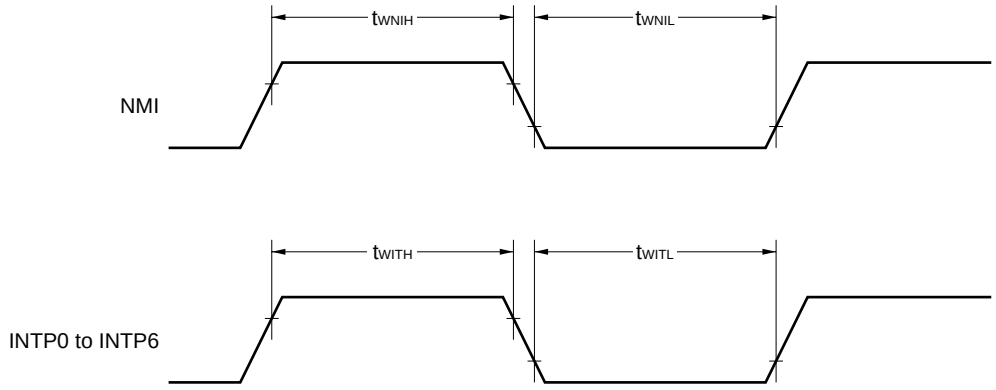
(3) I²C bus mode



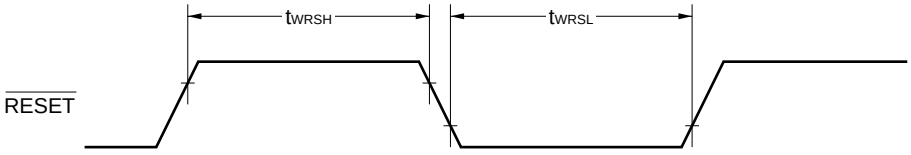
Clock Output Timing



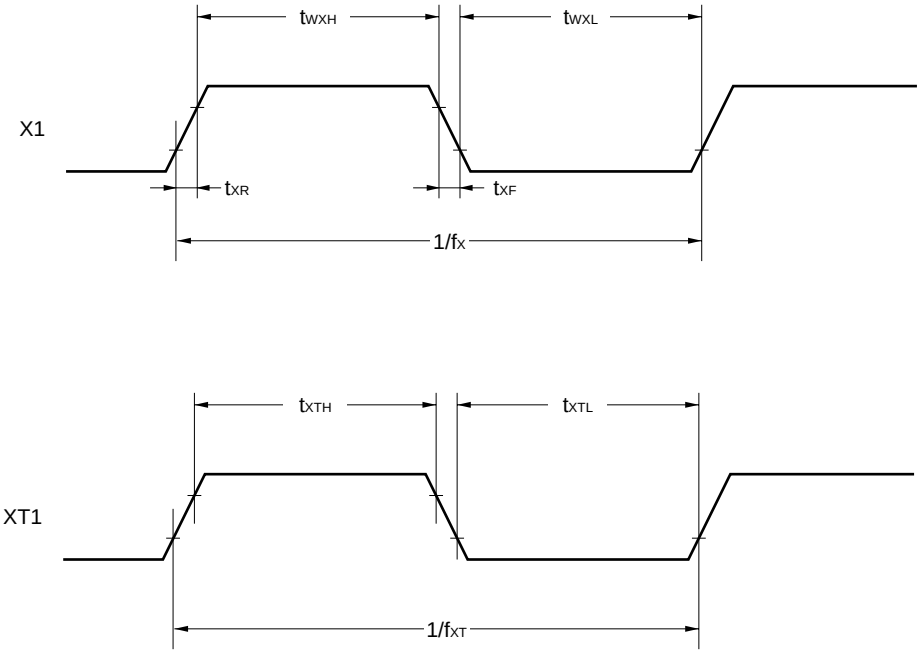
Interrupt Input Timing



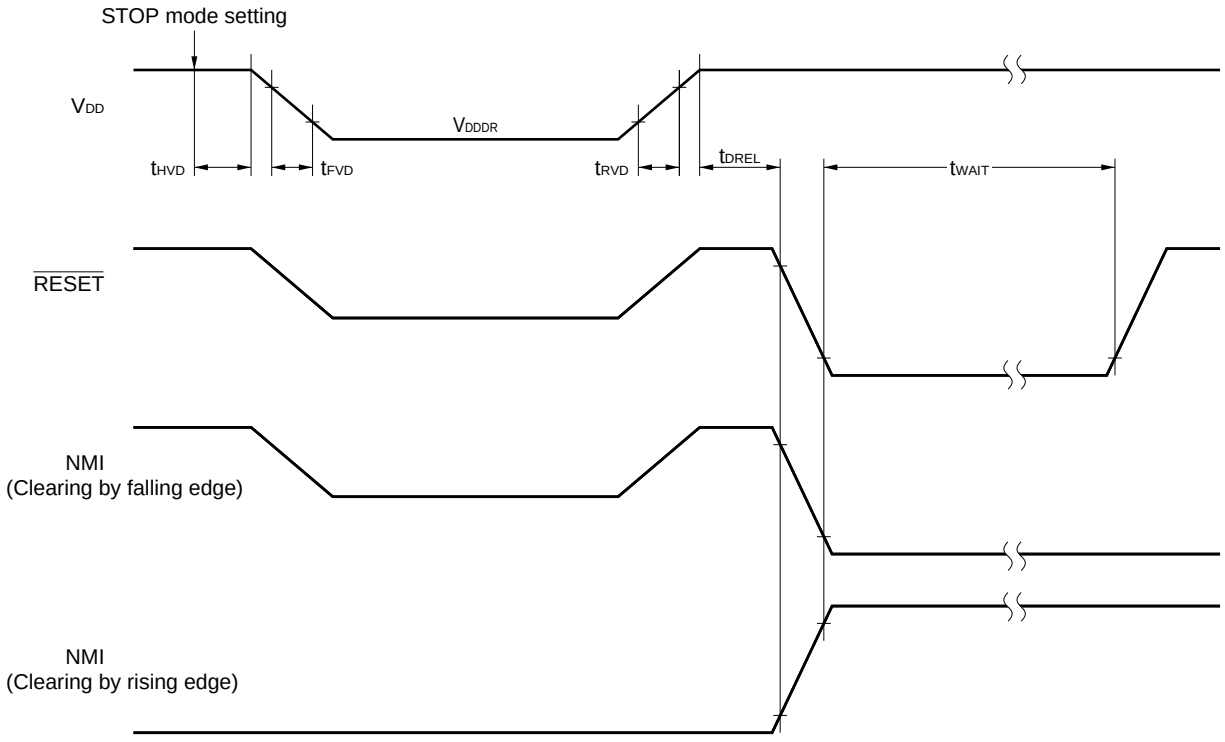
Reset Input Timing



Clock Timing

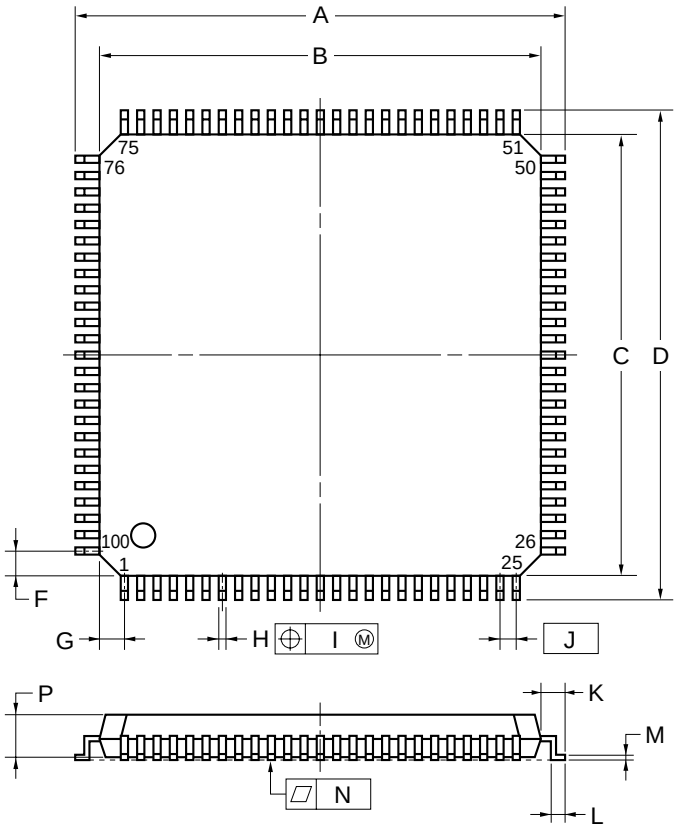


Data Retention Characteristics

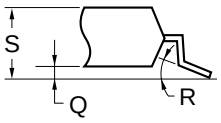


★ 8. PACKAGE DRAWINGS

100 PIN PLASTIC LQFP (FINE PITCH) (14×14)



detail of lead end



NOTE

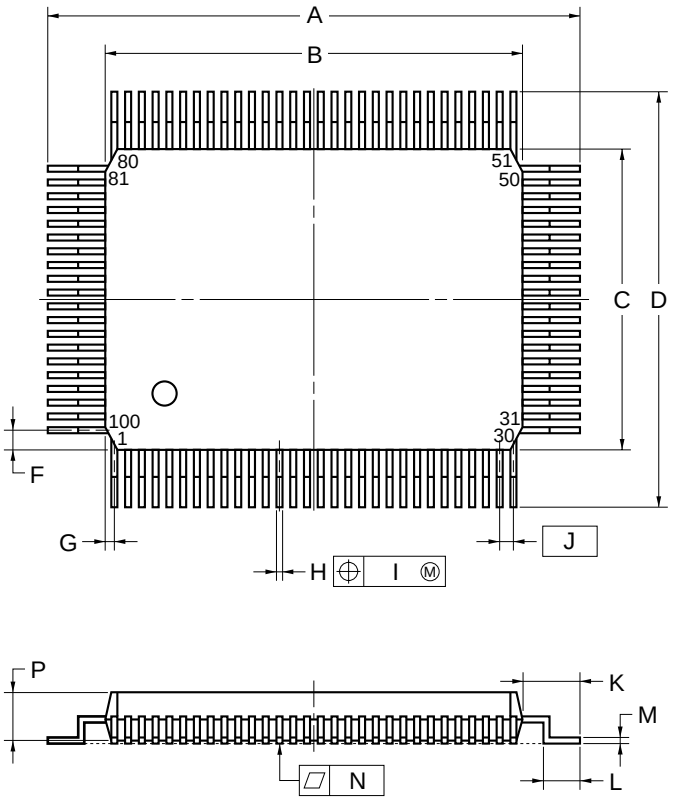
Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

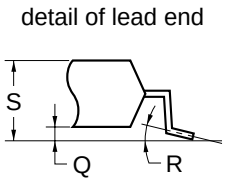
ITEM	MILLIMETERS	INCHES
A	16.00±0.20	0.630±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	16.00±0.20	0.630±0.008
F	1.00	0.039
G	1.00	0.039
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.08	0.003
J	0.50 (T.P.)	0.020 (T.P.)
K	1.00±0.20	$0.039^{+0.009}_{-0.008}$
L	0.50±0.20	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.08	0.003
P	1.40±0.05	0.055±0.002
Q	0.10±0.05	0.004±0.002
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.60 MAX.	0.063 MAX.

S100GC-50-8EU

Remark The external dimensions and material of the ES version are the same as those of the mass-produced version.

100PIN PLASTIC QFP (14x20)





NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7±0.1	$0.106^{+0.005}_{-0.004}$
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P100GF-65-3BA1-3

Remark The external dimensions and material of the ES version are the same as those of the mass-produced version.

★ 9. RECOMMENDED SOLDERING CONDITIONS

The μPD78F4216Y should be soldered and mounted under the following recommended conditions. For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Caution Because μPD78F4216YGC-8EU is under development, the recommended soldering conditions are undefined.

Table 9-1. Soldering Conditions for Surface Mounting Type

μPD78F4216YGF-3BA: 100-pin plastic QFP (14 × 20 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher), Count: two times or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher), Count: two times or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C Max., Time: 10 sec. Max., Count: once, Preheating temperature: 120°C Max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C Max., Time: 3 sec. Max. (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating).

★ APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78F4216Y. Also refer to **(5) Cautions on Using Development Tools**.

(1) Language Processing Software

RA78K4	Assembler package common to 78K/IV Series
CC78K4	C compiler package common to 78K/IV Series
DF784218	Device file common to μPD784216Y Subseries
CC78K4-L	C compiler library source file common to 78K/IV Series

(2) Flash Memory Writing Tools

Flashpro II (Model number: FL-PR2), Flashpro III (Model number: FL-PR3, PG-FP3)	Dedicated flash programmer for microcontrollers incorporating flash memory
FA-100GF	Adapter for writing 100-pin plastic QFP (GF-3BA type) flash memory. Connection must be performed depending on the target product.
FA-100GC	Adapter for writing 100-pin plastic LQFP (GC-8EU type) flash memory. Connection must be performed depending on the target product.
Flashpro II controller, Flashpro III controller	Control program that runs on a personal computer and is attached to Flashpro II and Flashpro III. Operates on Windows™95, etc.

(3) Debugging Tools

- **When in-circuit emulator IE-78K4-NS is used**

IE-78K4-NS	In-circuit emulator common to 78K/IV Series
IE-70000-MC-PS-B	Power supply unit for IE-78K4-NS
IE-70000-98-IF-C	Interface adapter used when PC-9800 series PC (except notebook type) is used as host machine (C bus supported)
IE-70000-CD-IF-A**Note**	PC card and cable when PC-9800 series notebook PC is used as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT™ compatible as host machine (ISA bus supported)
IE-70000-PCI-IF**Note**	Interface adapter when using PC that incorporates PCI bus as host machine
IE-784225-NS-EM1	Emulation board to emulate μPD784216Y Subseries
NP-100GF	Emulation probe for 100-pin plastic QFP (GF-3BA type)
NP-100GC	Emulation probe for 100-pin plastic LQFP (GC-8EU type)
EV-9200GF-100	Socket to be mounted on a target system board made for 100-pin plastic QFP (GF-3BA type)
TGC-100SDW	Conversion adapter to connect the NP-100GC and a target system board on which a 100-pin plastic LQFP (GC-8EU type) can be mounted
ID78K4-NS	Integrated debugger for IE-78K4-NS
SM78K4	System simulator common to 78K/IV Series
DF784218	Device file common to μPD784216Y Subseries

Note Under development

- **When in-circuit emulator IE-784000-R is used**

IE-784000-R	In-circuit emulator common to 78K/IV Series
IE-70000-98-IF-C	Interface adapter used when PC-9800 series PC (except notebook type) is used as host machine (C bus supported)
IE-70000-98N-IF	Interface adapter and cable used when PC-9800 series notebook PC is used as host machine
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT compatible as host machine (ISA bus supported)
IE-70000-PCI-IF[Note]	Interface adapter when using PC that incorporates PCI bus as host machine
IE-78000-R-SV3	Interface adapter and cable used when EWS is used as host machine
IE-784225-NS-EM1 IE-784216-R-EM1	Emulation board to emulate μPD784216Y Subseries
IE-784000-R-EM	Emulation board common to 78K/IV Series
IE-78K4-R-EX3	Emulation probe conversion board necessary when using IE-784225-NS-EM1 on IE-784000-R. Not necessary when IE-784216-R-EM1 is used.
EP-78064GF-R	Emulation probe for 100-pin plastic QFP (GF-3BA type)
EP-78064GC-R	Emulation probe for 100-pin plastic LQFP (GC-8EU type)
EV-9200GF-100	Socket to be mounted on a target system board made for 100-pin plastic QFP (GF-3BA type)
TGC-100SDW	Conversion adapter to connect the NP-100GC and a target system board on which a 100-pin plastic LQFP (GC-8EU type) can be mounted
ID78K4	Integrated debugger for IE-784000-R
SM78K4	System simulator common to 78K/IV Series
DF784218	Device file common to μPD784216Y Subseries

Note Under development

(4) Real-time OS

RX78K/IV	Real-time OS for 78K/IV Series
MX78K4	OS for 78K/IV Series

(5) Cautions on Using Development Tools

- The ID78K4-NS, ID78K4, and SM78K4 are used in combination with the DF784218.
- The CC78K4 and RX78K/IV are used in combination with the RA78K4 and DF784218.
- The FL-PR2, FL-PR3, FA-100GF, FA-100GC, NP-100GF, and NP-100GC are products made by Naitou Densei Machidaseisakusho Co., Ltd. (TEL: +81-44-822-3813). Contact an NEC distributor regarding the purchase of these products.
- The TGC-100SDW is a product made by TOKYO ELETECH CORPORATION.
- For further information, contact to: Daimaru Kogyo, Ltd.
  Electronics Dept. (Tokyo) (TEL: +81-3-3820-7112)
  Electronics Dept. (Osaka) (TEL: +81-6-6244-6672)
- For third party development tools, see the **78K/IV Series Selection Guide (U13355E)**.
- The host machine and OS suitable for each software are as follows:

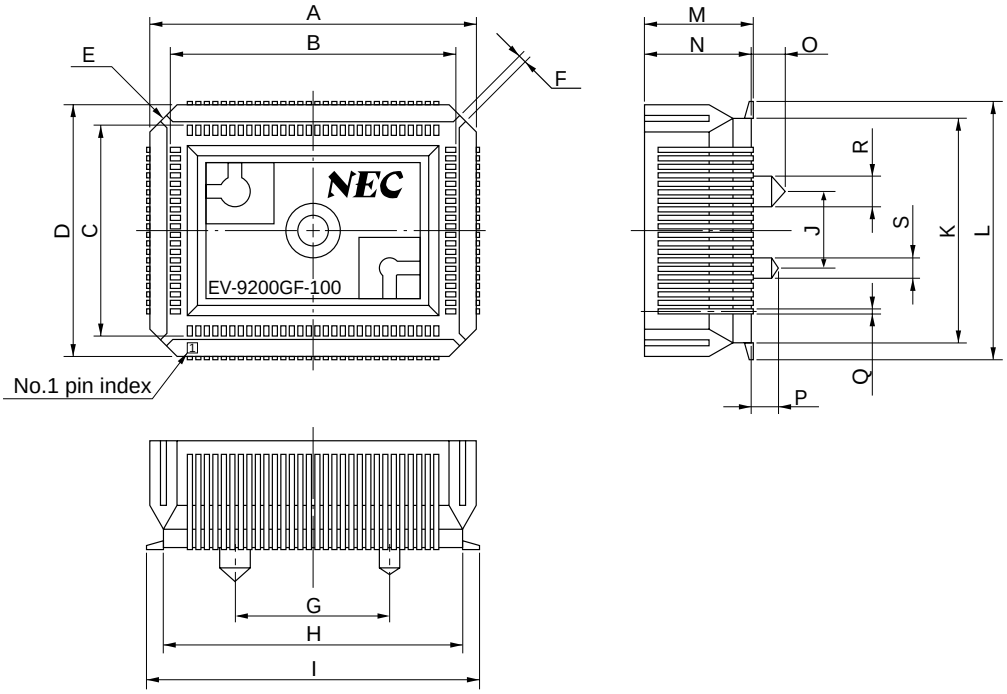
Host Machine [OS] / Software	PC PC-9800 series [Windows] IBM PC/AT and compatibles [Japanese/English Windows]	EWS HP9000 Series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K4	√ **Note**	√
CC78K4	√ **Note**	√
ID78K4-NS	√	–
ID78K4	√	√
SM78K4	√	–
RX78K/IV	√ **Note**	√
MX78K4	√ **Note**	√

Note DOS-based software

★ **Drawing of Conversion Socket (EV-9200GF-100) and Recommended Footprint**

Mount the conversion socket together with the EP-78064GF-R.

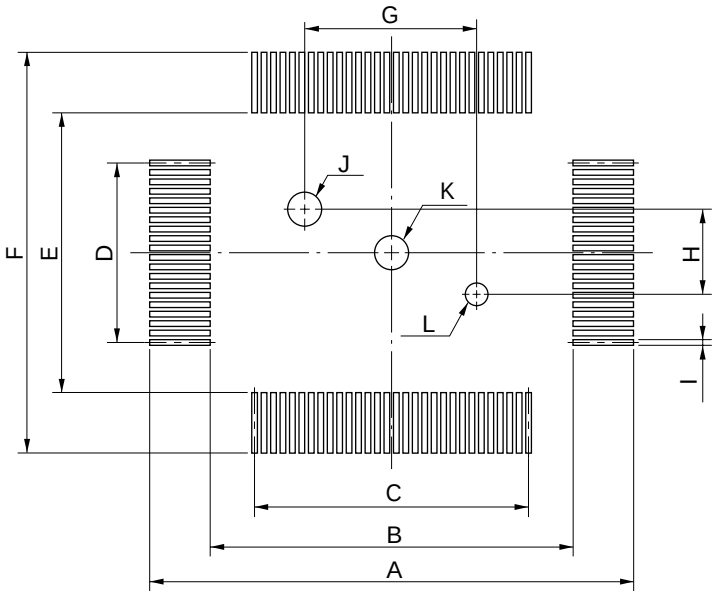
Figure A-1. Drawing of EV-9200GF-100 (for reference only)



EV-9200GF-100-G0E

ITEM	MILLIMETERS	INCHES
A	24.6	0.969
B	21	0.827
C	15	0.591
D	18.6	0.732
E	4-C 2	4-C 0.079
F	0.8	0.031
G	12.0	0.472
H	22.6	0.89
I	25.3	0.996
J	6.0	0.236
K	16.6	0.654
L	19.3	0.76
M	8.2	0.323
N	8.0	0.315
O	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	φ2.3	φ0.091
S	φ1.5	φ0.059

Figure A-2. Recommended Footprint of EV-9200GF-100 (for reference only)



EV-9200GF-100-P1E

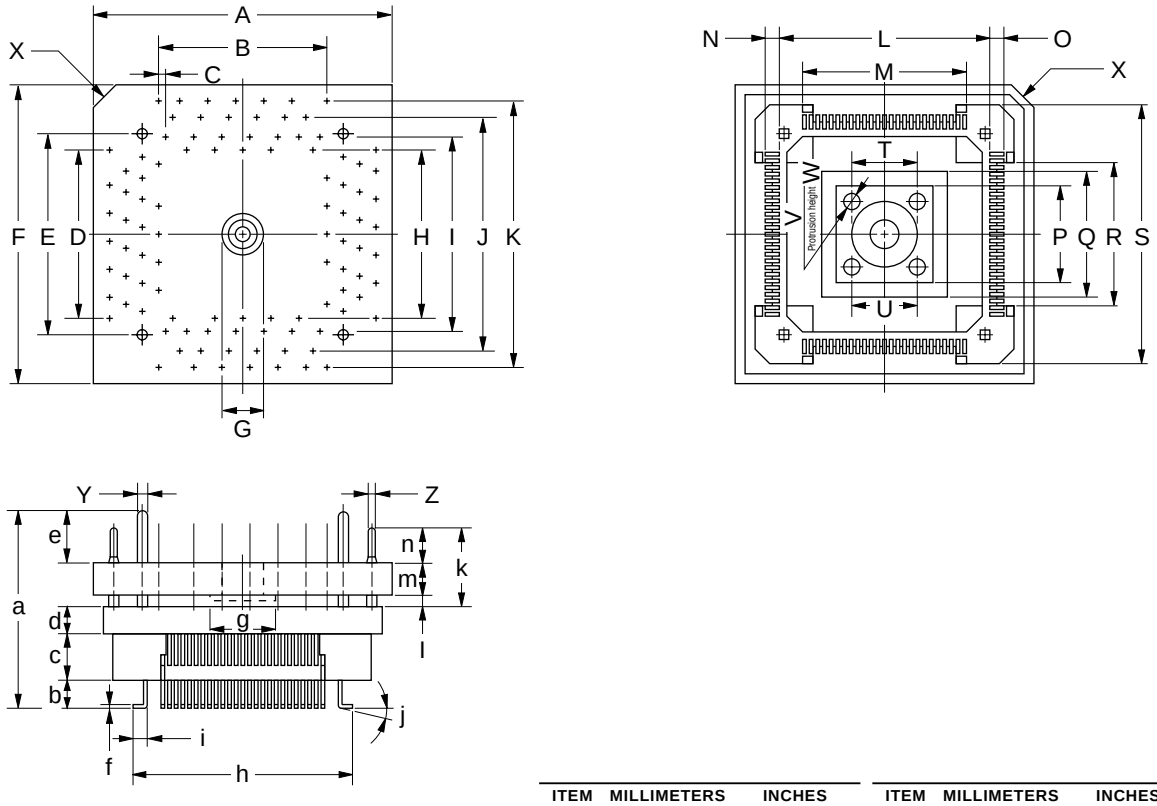
ITEM	MILLIMETERS	INCHES
A	26.3	1.035
B	21.6	0.85
C	$0.65\pm0.02\times29=18.85\pm0.05$	$0.026^{+0.001}_{-0.002}\times1.142=0.742^{+0.002}_{-0.002}$
D	$0.65\pm0.02\times19=12.35\pm0.05$	$0.026^{+0.001}_{-0.002}\times0.748=0.486^{+0.003}_{-0.002}$
E	15.6	0.614
F	20.3	0.799
G	12 ± 0.05	$0.472^{+0.003}_{-0.002}$
H	6 ± 0.05	$0.236^{+0.003}_{-0.002}$
I	0.35 ± 0.02	$0.014^{+0.001}_{-0.001}$
J	$\phi2.36\pm0.03$	$\phi0.093^{+0.001}_{-0.002}$
K	$\phi2.3$	$\phi0.091$
L	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

★ **Drawing of Conversion Adapter (TGC-100SDW)**

Mount the conversion adapter together with the EP-78064GC-R.

Figure A-3. Drawing of TGC-100SDW (for reference only)



ITEM	MILLIMETERS	INCHES
A	21.55	0.848
B	0.5x24=12	0.020x0.945=0.472
C	0.5	0.020
D	0.5x24=12	0.020x0.945=0.472
E	15.0	0.591
F	21.55	0.848
G	ϕ3.55	ϕ0.140
H	10.9	0.429
I	13.3	0.524
J	15.7	0.618
K	18.1	0.713
L	13.75	0.541
M	0.5x24=12.0	0.020x0.945=0.472
N	1.125±0.3	0.044±0.012
O	1.125±0.2	0.044±0.008
P	7.5	0.295
Q	10.0	0.394
R	11.3	0.445
S	18.1	0.713
T	ϕ5.0	ϕ0.197
U	5.0	0.197
V	4-ϕ1.3	4-ϕ0.051
W	1.8	0.071
X	C 2.0	C 0.079
Y	ϕ0.9	ϕ0.035
Z	ϕ0.3	ϕ0.012

ITEM	MILLIMETERS	INCHES
a	14.45	0.569
b	1.85±0.25	0.073±0.010
c	3.5	0.138
d	2.0	0.079
e	3.9	0.154
f	0.25	0.010
g	ϕ4.5	ϕ0.177
h	16.0	0.630
i	1.125±0.3	0.044±0.012
j	0~5°	0.000~0.197°
k	5.9	0.232
l	0.8	0.031
m	2.4	0.094
n	2.7	0.106

TGC-100SDW-G1E

note: Product by TOKYO ELETECH CORPORATION.

★ APPENDIX B. RELATED DOCUMENTS

Documents Related to Device

Document Name	Document No.	
	Japanese	English
μPD784214Y, 784215Y, 784216Y Data Sheet	U11725J	U11725E
μPD78F4216Y Data Sheet	U11824J	This document
μPD784216, 784216Y Subseries User's Manual Hardware	U12015J	U12015E
μPD784216Y Subseries Special Function Register Table	U12046J	–
78K/IV Series User's Manual Instructions	U10905J	U10905E
78K/IV Series Instruction Table	U10594J	–
78K/IV Series Instruction Set	U10595J	–
78K/IV Series Application Note Software Basics	U10095J	U10095E

Documents Related to Development Tool (User's Manual)

Document Name		Document No.	
		Japanese	English
RA78K4 Assembler Package	Language	U11162J	U11162E
	Operation	U11334J	U11334E
RA78K Structured Assembler Preprocessor		U11743J	U11743E
CC78K4 C Compiler	Language	U11571J	U11571E
	Operation	U11572J	U11572E
IE-78K4-NS		U13356J	U13356E
IE-784000-R		U12903J	U12903E
IE-784218-R-EM1		U12155J	U12155E
IE-784225-NS-EM1		To be prepared	—
EP-78064		EEU-934	EEU-1469
SM78K4 System Simulator Windows Based	Reference	U10093J	U10093E
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092J	U10092E
ID78K4-NS Integrated Debugger PC Based	Reference	U12796J	U12796E
ID78K4 Integrated Debugger Windows Based	Reference	U10440J	U10440E
ID78K4 Integrated Debugger HP-UX, SunOS, NEWS-OS based	Reference	U11960J	U11960E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Documents Related to Embedded Software (User's Manual)

Document Name		Document No.	
		Japanese	English
78K/IV Series Real-Time OS	Fundamental	U10603J	U10603E
	Installation	U10604J	U10604E
	Debugger	U10364J	–

Other Documents

Document Name	Document No.	
	Japanese	English
NEC IC Package Manual (CD-ROM)	–	C13388E
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Guide to Quality Assurance for Semiconductor Devices	–	MEI-1202
Guide to Microcontroller-Related Products by Third Parties	C11416J	–

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, pIease contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.l.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH
Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

NEC Electronics (France) S.A.
Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

NEC Electronics (France) S.A.
Spain Office
Madrid, Spain
Tel: 01-504-2787
Fax: 01-504-2860

NEC Electronics (Germany) GmbH
Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
United Square, Singapore 1130
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.
Electron Devices Division
Rodovia Presidente Dutra, Km 214
07210-902-Guarulhos-SP Brasil
Tel: 55-11-6465-6810
Fax: 55-11-6465-6829

J98. 11

Caution Purchase of NEC I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

M4 96.5