NEC

MOS INTEGRATED CIRCUIT

μPD78F4216

16/8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD78F4216 is a product in the μPD784216 subseries in the 78K/IV series.

The μPD78F4216 has a flash memory in the place of the internal ROM of the μPD784216. Data can be written to or erased from the flash memory of the μPD78F4216 with the microcontroller mounted on a printed wiring board.

The functions are explained in detail in the following user's manuals. Be sure to read this manual when designing your system.

μPD784216, 784216Y Subseries User's Manual - Hardware : U12015E
78K/IV Series User's Manual - Instruction : U10905E

FEATURES

- Pin-compatible with mask ROM model (except V_{PP} pin)
- Flash memory: 128K bytes
- Internal RAM: 8192 bytes
★ • Supply voltage: V_{DD} = 2.7 to 5.5 V

ORDERING INFORMATION

Part Number	Package
★ μPD78F4216GC-8EU	100-pin plastic LQFP (fine pitch) (14 × 14 mm)
μPD78F4216GF-3BA	100-pin plastic QFP (14 × 20 mm)

The information in this document is subject to change without notice.

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The mark ★ shows major revised points.

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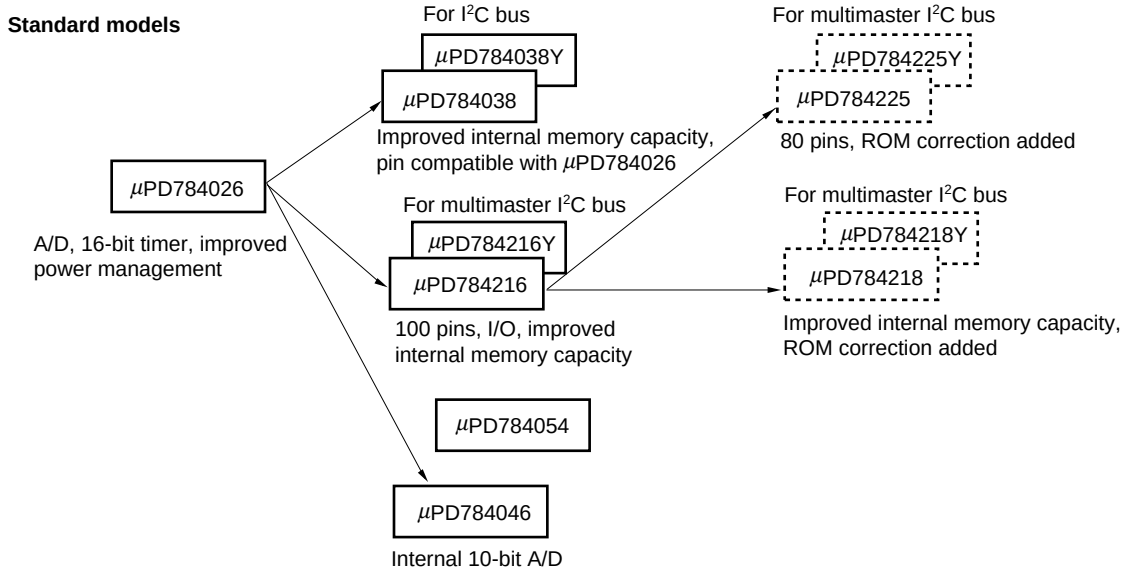
★ Product Development of 78K/IV Series

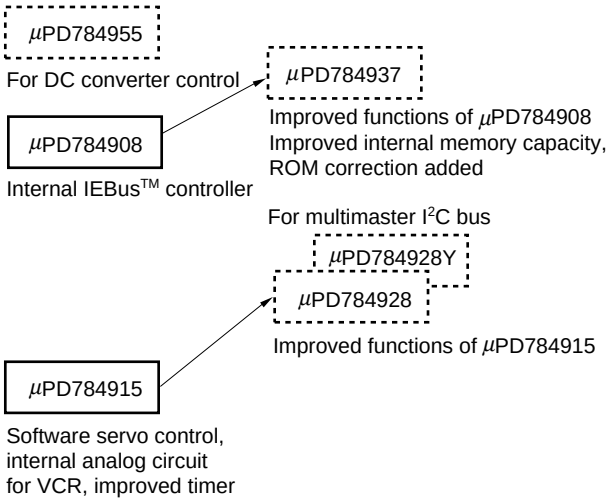
: Under mass production

: Under development

Standard models



ASSP models



FUNCTIONS (1/2)

Item		Function		
Number of basic instructions (mnemonics)		113		
General-purpose register		8 bits × 16 registers × 8 banks, or 16 bits × 8 registers × 8 banks (memory mapping)		
★ Minimum instruction execution time		160 ns/320 ns/640 ns/1280 ns/2560 ns (main system clock: f_{XX} = 12.5 MHz)		
Internal memory	Flash memory	128 KBytes		
	RAM	8192 Bytes		
Memory space		1 MB with program and data spaces combined		
I/O port	Total	86		
	CMOS Input	8		
	CMOS I/O	72		
	N-ch open-drain I/O	6		
Pins with ancillary functions[Note]	Pins with pull-up resistor	70		
	LEDs direct drive output	22		
	Medium voltage pin	6		
Real-time output port		4 bits × 2, or 8 bits × 1		
Timer/counter		Timer/counter (16-bit) :	timer register × 1 Capture/compare register × 2	Pulse output • PPG output • Square wave output • One-shot pulse output
		Timer/counter 1 (8-bit) :	timer register × 1 Compare register × 1	Pulse output • PWM output • Square wave output
		Timer/counter 2 (8-bit) :	timer register × 1 Compare register × 1	Pulse output • PWM output • Square wave output
		Timer/counter 5 (8-bit) :	timer register × 1 Compare register × 1	Pulse output • PWM output • Square wave output
		Timer/counter 6 (8-bit) :	timer register × 1 Compare register × 1	Pulse output • PWM output • Square wave output
		Timer/counter 7 (8-bit) :	timer register × 1 Compare register × 1	Pulse output • PWM output • Square wave output
		Timer/counter 8 (8-bit) :	timer register × 1 Compare register × 1	Pulse output • PWM output • Square wave output

Note The pins with ancillary functions are included in the I/O pins.

FUNCTIONS (2/2)

	Item		Function
	Serial interface		• UART/IOE (3-wire serial I/O): 2 channels (on-chip baud rate generator) • CSI (3-wire serial I/O): 1 channel
	A/D converter		8-bit resolution × 8 channels
	D/A converter		8-bit resolution × 2 channels
	Clock output		Selectable from f_{XX}, $f_{XX}/2$, $f_{XX}/2^2$, $f_{XX}/2^3$, $f_{XX}/2^4$, $f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$, f_{XT}
	Buzzer output		Selectable from $f_{XX}/2^{10}$, $f_{XX}/2^{11}$, $f_{XX}/2^{12}$, $f_{XX}/2^{13}$
	Watch timer		1 channel
	Watchdog timer		1 channel
★	Standby		HALT/STOP/IDLE mode
	Interrupt	Hardware source	29 (internal: 20, external: 9)
		Software source	BRK instruction, BRKCS instruction, operand error
		Non-maskable	Internal: 1, external: 1
		Maskable	Internal: 19, external: 8
			• 4 programmable priority levels • 3 service modes: vectored interrupt/macro service/context switching
★	Supply voltage		V_{DD} = 2.7 to 5.5 V
★	Package		• 100-pin plastic LQFP (fine pitch) (14 × 14 mm) • 100-pin plastic QFP (14 × 20 mm)

CONTENTS

1. DIFFERENCES AMONG MODELS IN μPD784216 SUBSERIES

The only difference among the μPD784214, 784215, and 784216 lies in the internal memory capacity.

The μPD78P4216 is provided with a 128-KB flash memory instead of the mask ROM of the above models. These differences are summarized in Table 1-1.

★ **Table 1-1. Differences among Models in μPD784216 Subseries**

Part Number / Item	μPD784214	μPD784215	μPD784216	μPD78F4216
Internal ROM	96 KBytes (mask ROM)	128 KBytes (mask ROM)		128 KBytes (Flash memory)
Internal RAM	3584 Bytes	5120 Bytes	8192 Bytes	
Internal memory size switching register (IMS)	None			Provided[Note]
Supply voltage	V_{DD} = 2.2 to 5.5 V			V_{DD} = 2.7 to 5.5 V
CPU clock	Main system clock, subsystem clock			Main system clock
Electrical specifications	Refer to the Data Sheet of each product.			
Recommended soldering conditions				
TEST pin	Provided			None
V_{PP} pin	None			Provided

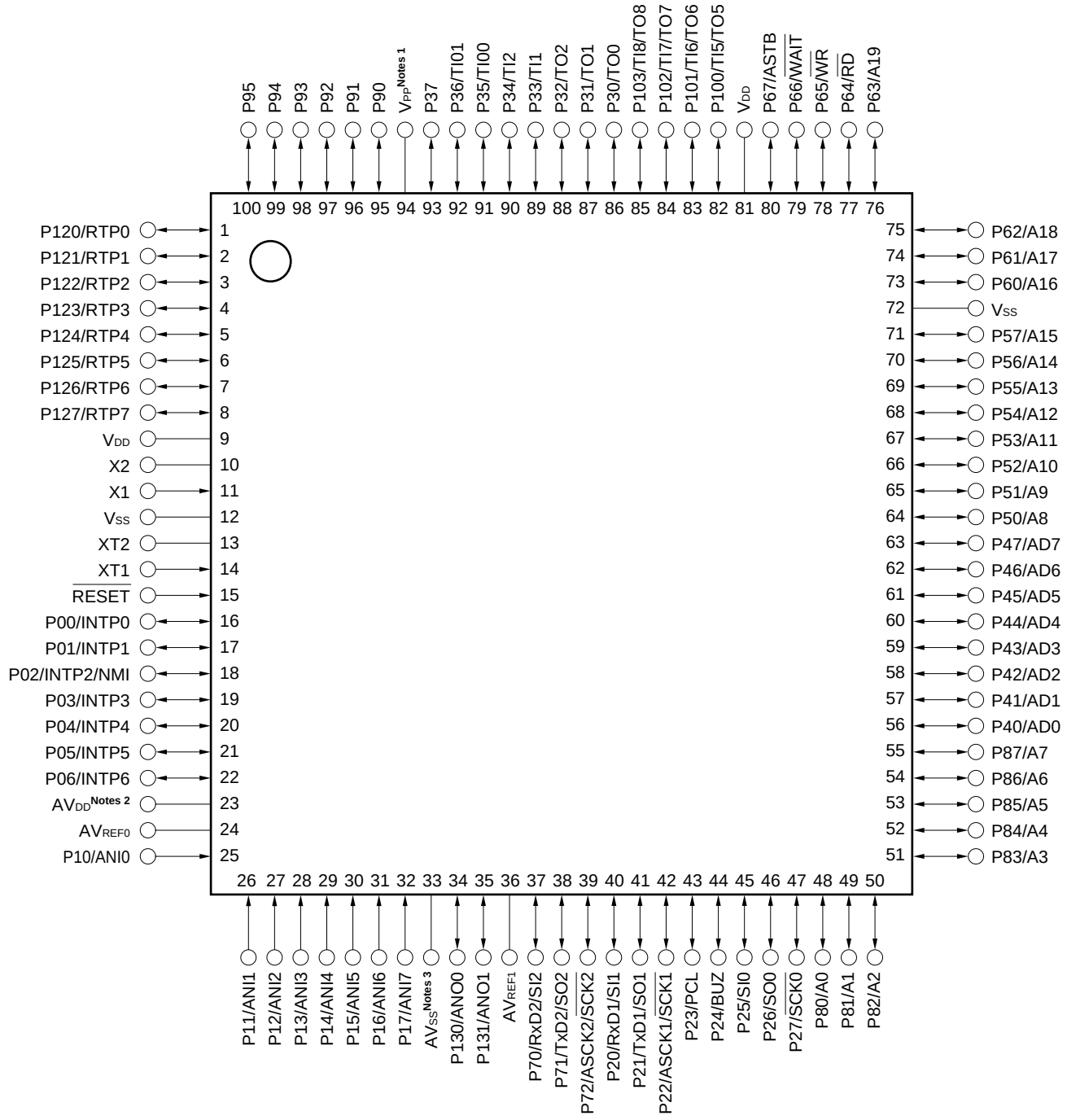
Note The internal flash memory capacity and the internal RAM capacity can be changed by the internal memory size select register (IMS).

Caution The noise immunity and radiation differ between the flash memory model and mask ROM model. To replace a flash memory model with a mask ROM model in the course from experimental production to mass production, evaluate your system with the CS model (not ES model) of the mask ROM model.

2. PIN CONFIGURATION (Top View)

- **100-pin plastic LQFP (fine pitch) (14 × 14 mm)**

★ μPD78F4216GC-8EU

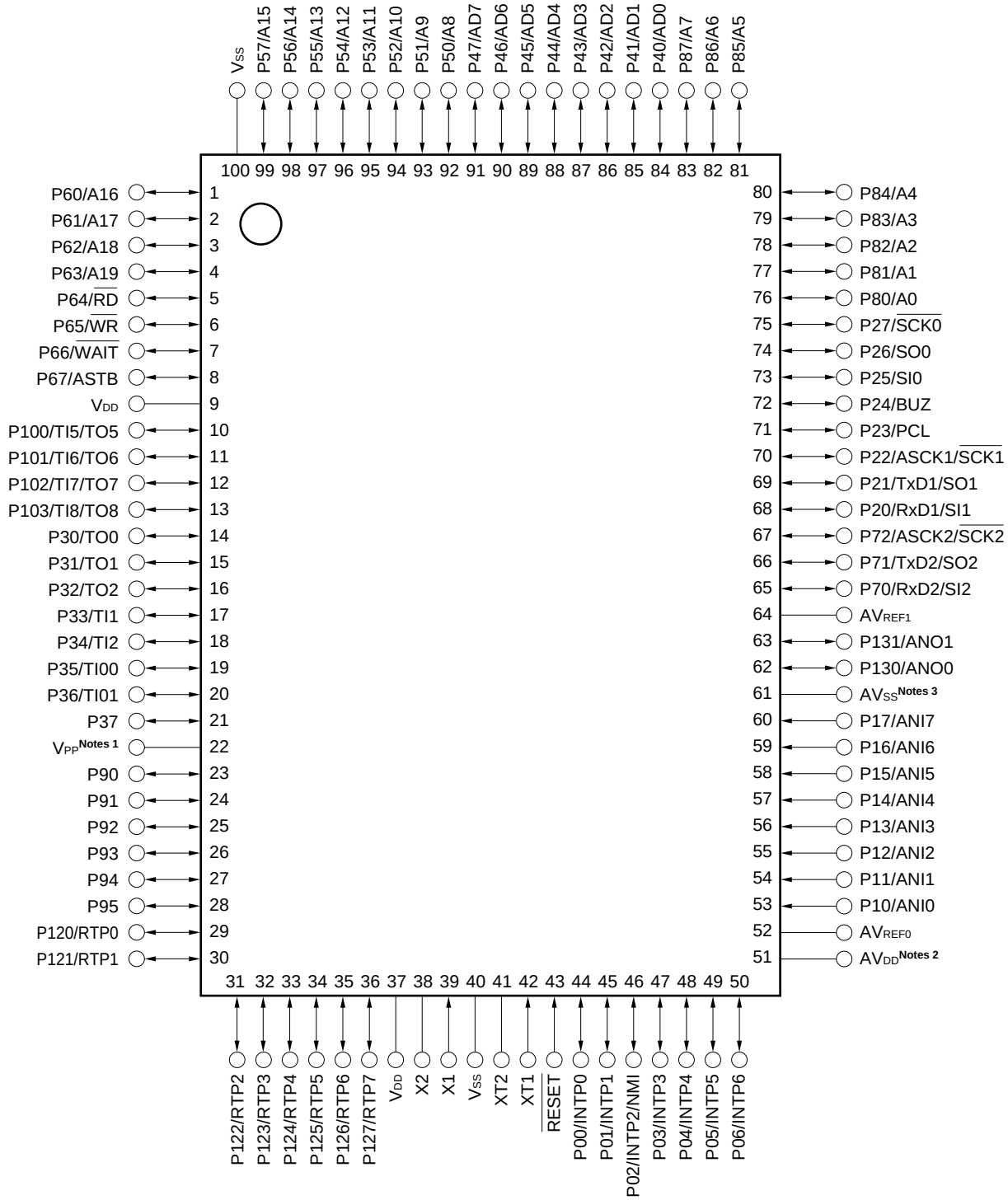


Notes 1. Directly connect the V_{PP} pin to V_{SS} in normal operation mode.

2. Connect the AV_{DD} pin to V_{DD}.

3. Connect the AV_{SS} pin to V_{SS}.

- **100-pin plastic QFP (14 × 20 mm)**
  μPD78F4216GF-3BA



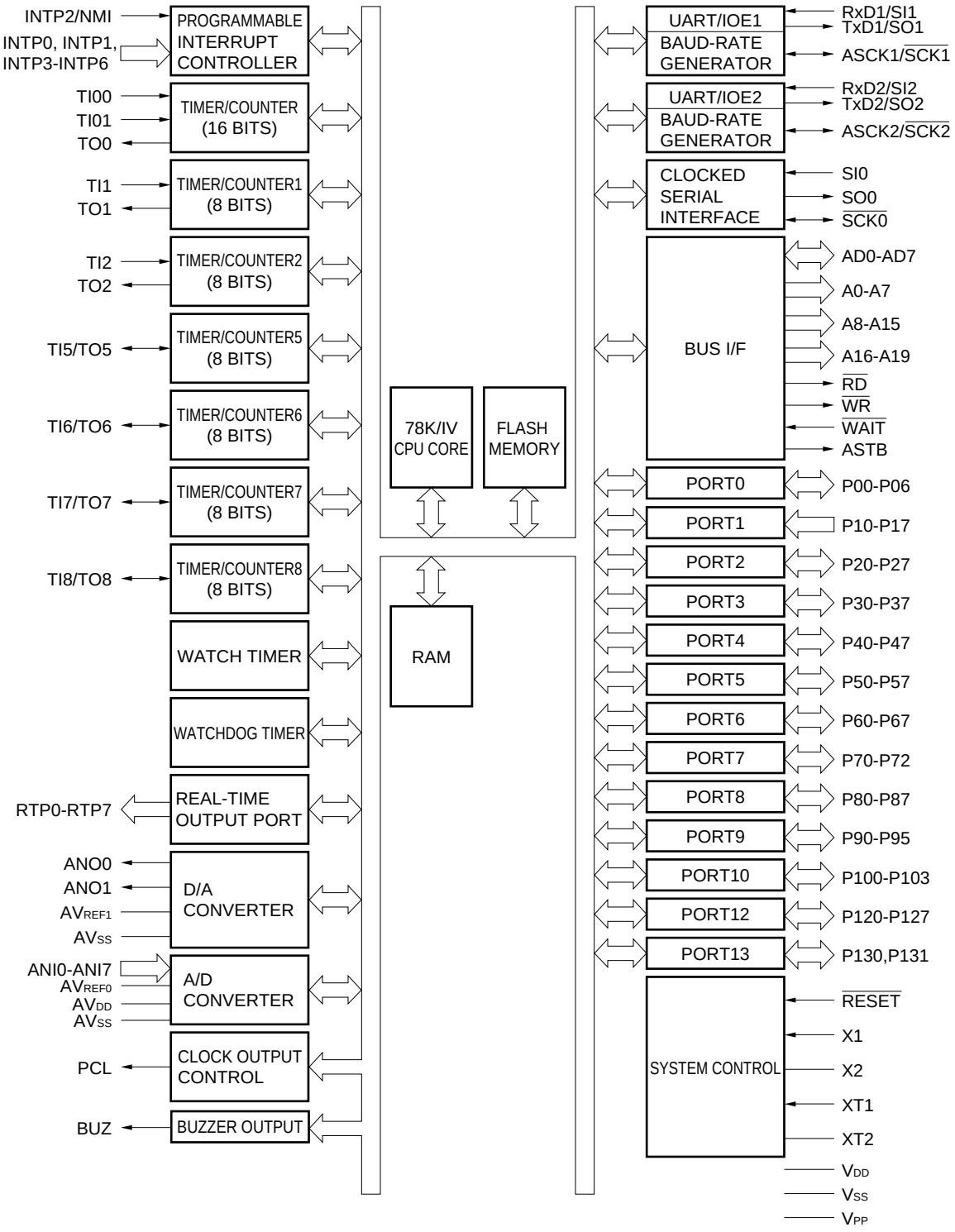
Notes 1. Directly connect the V_{PP} pin to V_{SS} in normal operation mode.

2. Connect the AV_{DD} pin to V_{DD}.

3. Connect the AV_{SS} pin to V_{SS}.

A0-A19	: Address Bus	P100-P103	: Port10
AD0-AD7	: Address/Data Bus	P120-P127	: Port12
ANI0-ANI7	: Analog Input	P130, P131	: Port13
ANO0, ANO1	: Analog Output	PCL	: Programmable Clock
ASCK1, ASCK2	: Asynchronous Serial Clock	$\overline{RD}$	: Read Strobe
ASTB	: Address Strobe	$\overline{RESET}$	: Reset
AV_{DD}	: Analog Power Supply	RTP0-RTP7	: Real-time Output Port
AV_{REF0}, AV_{REF1}	: Analog Reference Voltage	RxD1, RxD2	: Receive Data
AV_{SS}	: Analog Ground	$\overline{SCK0}$-$\overline{SCK2}$	: Serial Clock
BUZ	: Buzzer Clock	SI0-SI2	: Serial Input
INTP0-INTP6	: Interrupt from Peripherals	SO0-SO2	: Serial Output
NMI	: Non-maskable Interrupt	TI00, TI01,	
P00-P06	: Port0	TI1, TI2, TI5-TI8	: Timer Input
P10-P17	: Port1	TO0-TO2, TO5-TO8	: Timer Output
P20-P27	: Port2	TxD1, TxD2	: Transmit Data
P30-P37	: Port3	V_{DD}	: Power Supply
P40-P47	: Port4	V_{PP}	: Programming Power Supply
P50-P57	: Port5	V_{SS}	: Ground
P60-P67	: Port6	$\overline{WAIT}$	: Wait
P70-P72	: Port7	$\overline{WR}$	: Write Strobe
P80-P87	: Port8	X1, X2	: Crystal (Main System Clock)
P90-P95	: Port9	XT1, XT2	: Crystal (Subsystem Clock)

3. BLOCK DIAGRAM



4. PIN FUNCTION

4.1 Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function
P00	I/O	INTP0	Port 0 (P0): • 7-bit I/O port • Can be set in input or output mode bit-wise. • Can be connected to internal pull-up resistors by software bit-wise regardless of input mode or output mode.
P01		INTP1	
P02		INTP2/NM1	
★ P03		INTP3	
P04		INTP4	
P05		INTP5	
P06		INTP6	
P10-P17	Input	ANI0-ANI7	Port 1 (P1): • 8-bit input port
P20	I/O	RxD1/SI1	Port 2 (P2): • 8-bit I/O port • Can be set in input or output mode bit-wise. • Can be connected to internal pull-up resistors by software bit-wise regardless of input mode or output mode.
P21		TxD1/SO1	
P22		ASCK1/$\overline{\text{SCK1}}$	
★ P23		PCL	
P24		BUZ	
P25		SI0	
P26		SO0	
P27		$\overline{\text{SCK0}}$	
P30	I/O	TO0	Port 3 (P3): • 8-bit I/O port • Can be set in input or output mode bit-wise. • Can be connected to internal pull-up resistors by software bit-wise regardless of input mode or output mode.
P31		TO1	
P32		TO2	
★ P33		TI1	
P34		TI2	
P35		TI00	
P36		TI01	
P37		—	
P40-P47	I/O	AD0-AD7	Port 4 (P4): • 8-bit I/O port • Can be set in input or output mode bit-wise. • All pins set in input mode can be connected to internal pull-up resistors by software. • Can drive LEDs.
P50-P57	I/O	A8-A15	Port 5 (P5): • 8-bit I/O port • Can be set in input or output mode bit-wise. • All pins set in input mode can be connected to internal pull-up resistors by software. • Can drive LEDs.

4.1 Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
P60	I/O	A16	Port 6 (P6): • 8-bit I/O port • Can be set in input or output mode bit-wise. • All pins set in input mode can be connected to internal pull-up resistors by software.
P61		A17	
P62		A18	
P64		$\overline{RD}$	
P65		$\overline{WR}$	
P66		$\overline{WAIT}$	
P67		ASTB	
P70	I/O	RxD2/SI2	Port 7 (P7): • 3-bit I/O port • Can be set in input or output mode bit-wise. • Can be connected to internal pull-up resistor by software bit-wise regardless of input mode or output mode.
P71		TxD2/SO2	
★ P72		ASCK2/$\overline{SCK2}$	
P80-P87	I/O	A0-A7	Port 8 (P8): • 8-bit I/O port • Can be set in input or output mode bit-wise. • Can be connected to internal pull-up resistor by software bit-wise regardless of input or output mode. • Interrupt control flag (KRIF) is set to 1 when falling edge is detected at a pin of this port.
★ P90-P95	I/O	—	Port 9 (P9): • N-ch open-drain medium-voltage I/O port • 6-bit I/O port • Can be set in input or output mode bit-wise. • Can directly drive LEDs.
P100	I/O	TI5/TO5	Port 10 (P10): • 4-bit I/O port • Can be set in input or output mode bit-wise. • Can be connected to internal pull-up resistor by software bit-wise regardless of input mode or output mode.
P101		TI6/TO6	
P102		TI7/TO7	
★ P103		TI8/TO8	
P120-P127	I/O	RTP0-RTP7	Port 12 (P12): • 8-bit I/O port • Can be set in input or output mode bit-wise. • Can be connected to internal pull-up resistor by software bit-wise regardless of input mode or output mode.
★ P130, P131	I/O	ANO0, ANO1	Port 13 (P13): • 2-bit I/O port • Can be set in input or output mode bit-wise.

4.2 Pins Other Than Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function
TI00	Input	P35	External count clock input to 16-bit timer register
TI01		P36	Capture trigger signal input to capture/compare register 00
TI1		P33	External count clock input to 8-bit timer register 1
TI2		P34	External count clock input to 8-bit timer register 2
TI5		P100/TO5	External count clock input to 8-bit timer register 5
TI6		P101/TO6	External count clock input to 8-bit timer register 6
TI7		P102/TO7	External count clock input to 8-bit timer register 7
TI8		P103/TO8	External count clock input to 8-bit timer register 8
TO0	Output	P30	16-bit timer output (shared by 14-bit PWM output)
TO1		P31	8-bit timer output (shared by 8-bit PWM output)
TO2		P32	
TO5		P100/TI5	
TO6		P101/TI6	
TO7		P102/TI7	
TO8		P103/TI8	
RxD1	Input	P20/SI1	Serial data input (UART1)
RxD2		P70/SI2	Serial data input (UART2)
TxD1	Output	P21/SO1	Serial data output (UART1)
TxD2		P71/SO2	Serial data output (UART2)
ASCK1	Intput	P22/$\overline{\text{SCK1}}$	Baud rate clock input (UART1)
ASCK2		P72/$\overline{\text{SCK2}}$	Baud rate clock input (UART2)
SI0	Input	P25	Serial data input (3-wire serial clock I/O0)
SI1		P20/RxD1	Serial data input (3-wire serial clock I/O1)
SI2		P70/RxD2	Serial data input (3-wire serial clock I/O2)
SO0	Output	P26	Serial data output (3-wire serial I/O0)
SO1		P21/TxD1	Serial data output (3-wire serial I/O1)
SO2		P71/TxD2	Serial data output (3-wire serial I/O2)
$\overline{\text{SCK0}}$	I/O	P27/SCL0	Serial clock input/output (3-wire serial I/O0)
$\overline{\text{SCK1}}$		P22/ASCK1	Serial clock input/output (3-wire serial I/O1)
$\overline{\text{SCK2}}$		P72/ASCK2	Serial clock input/output (3-wire serial I/O2)
NMI	Input	P02/INTP2	Non-maskable interrupt request input
INTP0		P00	External interrupt request input
INTP1		P01	
INTP2		P02/NMI	
INTP3		P03	
INTP4		P04	
INTP5		P05	
INTP6		P06	

4.2 Pins Other Than Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
PCL	Output	P23	Clock output (for trimming main system clock and subsystem clock)
BUZ	Output	P24	Buzzer output
RTP0-RTP7	Output	P120-P127	Real-time output port that outputs data in synchronization with trigger
AD0-AD7	I/O	P40-P47	Low-order address/data bus when external memory is connected
A0-A7	Output	P80-P87	Low-order address bus when external memory is connected
A8-A15		P50-P57	Middle-order address bus when external memory is connected
A16-A19		P60-P63	High-order address bus when external memory is connected
$\overline{RD}$	Output	P64	Strobe signal output for read operation of external memory
$\overline{WR}$		P65	Strobe signal output for write operation of external memory
$\overline{WAIT}$	Input	P66	To insert wait state(s) when external memory is accessed
ASTB	Output	P67	Strobe output to externally latch address information output to ports 4 through 6 and port 8 to access external memory
$\overline{RESET}$	Input	—	System reset input
X1	Input	—	To connect main system clock oscillation crystal
X2	—		
XT1	Input	—	To connect subsystem clock oscillation crystal
XT2	—		
ANI0-ANI7	Input	P10-P17	Analog voltage input for A/D converter
ANO0, ANO1	Output	P130, P131	Analog voltage output for D/A converter
AV_{REF0}	—	—	To apply reference voltage for A/D converter
AV_{REF1}			To apply reference voltage for D/A converter
AV_{DD}			Positive power supply for A/D converter. Connect to V_{DD}.
AV_{SS}			GND for A/D converter and D/A converter. Connect to V_{SS}.
V_{DD}			Positive power supply
V_{SS}			GND
★ V_{PP}			Sets flash memory programming mode. To apply a high voltage when program is written or verified. Directly connect to V_{SS} in normal operation mode.

4.3 I/O Circuit Type of Respective Pins and Recommended Connections of Unused Pins

Table 4-1 shows symbols indicating the I/O circuit types of the respective pins and the recommended connection of unused pins.

For the circuit diagram of each type of I/O circuit, refer to **Figure 4-1**.

Table 4-1. I/O Circuit Type of Respective Pins and Recommended Connections of Unused Pins (1/2)

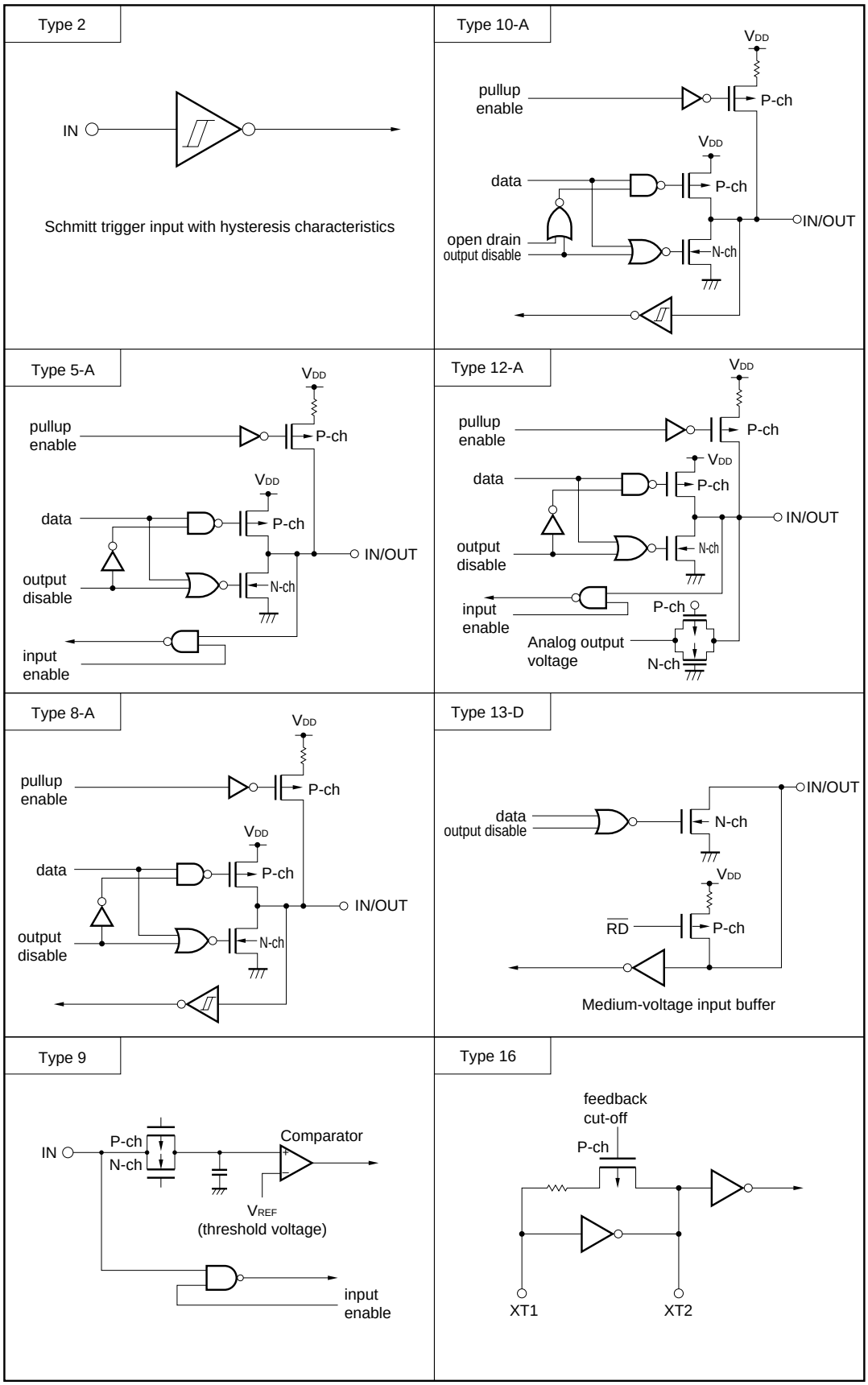
Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
P00/INTP0	8-A	I/O	Input : Individually connect to V_{SS} via resistor. Output: Leave open.
P01/INTP1			
P02/INTP2/NMI			
P03/INTP3-P06/INTP6			
P10/ANI0-P17/ANI7	9	Input	Connect to V_{SS} or V_{DD}
P20/RxD1/SI1	10-A	I/O	Input : Individually connect to V_{SS} via resistor. Output: Leave open.
P21/TxD1/SO1			
P22/ASCK1/$\overline{SCK1}$			
P23/PCL			
P24/BUZ			
P25/SI0			
P26/SO0			
P27/$\overline{SCK0}$			
P30/TO0-P32/TO2	8-A		
P33/TI1, P34/TI2			
P35/TI00, P36/TI01			
P37			
P40/AD0-P47/AD7	5-A		
P50/A8-P57/A15			
P60/A16-P63/A19			
P64/$\overline{RD}$			
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
P70/RxD2/SI2	8-A		
P71/TxD2/SO2			
P72/ASCK2/$\overline{SCK2}$			
P80/A0-P87/A7			
P90-P95	13-D		
P100/TI5/TO5	8-A		
P101/TI6/TO6			
P102/TI7/TO7			
P103/TI8/TO8			
P120/RTP0-P127/RTP7			
P130/ANO0, P131/ANO1	12-A		

Table 4-1. I/O Circuit Type of Respective Pins and Recommended Connections of Unused Pins (2/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
$\overline{\text{RESET}}$	2	Input	—
XT1	16		Connect to V_{SS}.
XT2		—	Leave open.
AV_{REF0}	—		Connect to V_{SS}.
AV_{REF1}			Connect to V_{DD}.
AV_{DD}			
AV_{SS}			Connect to V_{SS}.
V_{PP}			Directly connect to V_{SS}.

Remark Because the circuit type numbers are standardized among the 78K series products, they are not sequential in some models (i.e., some circuits are not provided).

Figure 4-1. Types of Pin I/O Circuits



5. INTERNAL MEMORY SIZE SELECT REGISTER (IMS)

The IMS is a register that prevents by software a part of the internal memory from being used. By using this register, the memory of the μPD78F4216 can be mapped in the same manner as a mask ROM model with different internal memory (ROM and RAM) capacity.

This register is set by using an 8-bit memory manipulation instruction.

Its value is set to FFH by $\overline{\text{RESET}}$ input.

Figure 5-1. Format of Internal Memory Size Select Register (IMS)

Address: 0FFFCH At reset: FFH W

	7	6	5	4	3	2	1	0
IMS	1	1	ROM1	ROM0	1	1	RAM1	RAM0

ROM1	ROM0	Selects internal ROM capacity
0	0	48K bytes
0	1	64K bytes
1	0	96K bytes
1	1	128K bytes

RAM1	RAM0	Selects peripheral RAM capacity
0	0	3072 bytes
0	1	4608 bytes
1	0	6114 bytes
1	1	7680 bytes

Caution IMS is not provided on the mask ROM models (μPD784214, 784215, and 784216).

The value to be set to the IMS to map the memory of the μPD78F4216 in the same manner as the mask ROM model is shown in Table 5-1.

Table 5-1. Set Value of Internal Memory Size Select Register (IMS)

Mask ROM Model	Set Value of IMS
μPD784214	ECH
μPD784215	FDH
μPD784216	FFH

6. PROGRAMMING FLASH MEMORY

The flash memory can be written with the μPD78F4216 mounted on the target board (on-board). To do so, ★ connect a dedicated flash programmer (Flashpro II (part number: FL-PR2), Flashpro III (part number: FL-PR3, PG-FP3) to the host machine and target system.

★ **Remark** FL-PR2 and FL-PR3 are products of Naito Densei Machida Mfg. Co. Ltd.

6.1 Selecting Communication Mode

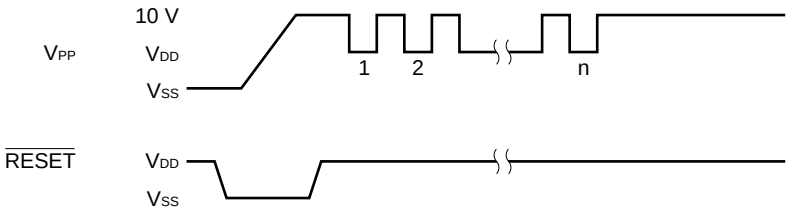
To write the flash memory, use Flashpro II and Flashpro III by serial communication. Select a serial communication mode from those listed in Table 6-1 in the format shown in Figure 6-1. Each communication mode is selected by the number of V_{PP} pulses shown in Table 6-1.

Table 6-1. Communication Modes

Communication Mode	Number of Channels	Pins Used	Number of V_{PP} Pulses
3-wire serial I/O	3	$\overline{SCK0}$/P27 SO0/P26 SI0/P25	0
		$\overline{SCK1}$/ASCK1/P22 SO1/TxD1/P21 SI1/RxD1/P20	1
		$\overline{SCK2}$/ASCK2/P72 SO2/TxD2/P71 SI2/RxD2/P70	2
UART	2	TxD1/SO1/P21 RxD1/SI1/P20	8
		TxD2/SO2/P71 RxD2/SI2/P70	9

Caution Be sure to select a communication mode with the number of V_{PP} pulses shown in Table 6-1.

Figure 6-1. Communication Mode Selecting Format



6.2 Flash Memory Programming Function

The flash memory is written by transferring or receiving commands and data in a selected communication mode. The major functions of flush memory programming are listed in Table 6-2.

Table 6-2. Major Functions of Flash Memory Programming

Function	Description
Batch erasure	Erases all contents of memory.
Block erasure	Erases contents of specified memory block with one memory block consisting of 16K bytes.
Batch blank check	Checks erased status of entire memory.
Block blank check	Checks erased status of specified block
Data write	Writes flash memory based on write start address and number of data to be written (in bytes).
Batch verify	Compares all contents of memory with input data.
Block verify	Compares contents of specified memory block with input data.

6.3 Connecting Flashpro II and Flashpro III

The Flashpro II, Flashpro III and μPD78F4216 are connected differently depending on the selected communication mode (3-wire serial I/O or UART). Figures 6-2 and 6-3 show the connections in the respective communication modes.

Figure 6-2. Connection of Flashpro II and Flashpro III in 3-Wire Serial I/O Mode

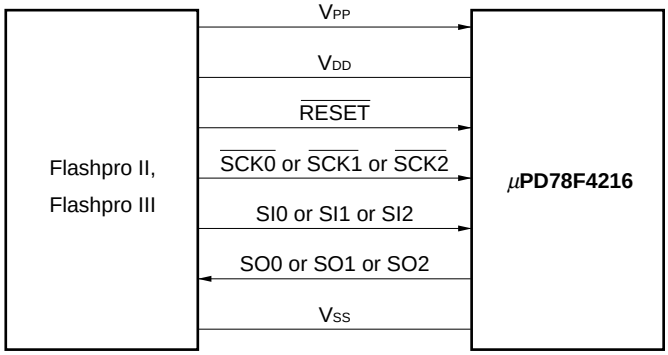
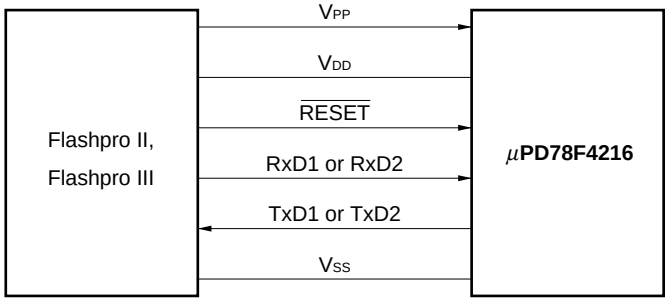


Figure 6-3. Connection of Flashpro II and Flashpro III in UART Mode



★ 7. ELECTRICAL SPECIFICATIONS

Maximum Absolute Rating (T_A = 25 °C)

Parameter	Symbol	Test Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to V_{SS} + 0.3	V
	AV_{REF0}	A/D converter reference voltage input		–0.3 to V_{DD} + 0.3	V
	AV_{REF1}	D/A converter reference voltage input		–0.3 to V_{DD} + 0.3	V
Input voltage	V_{I1}	Pins other than P90-P95		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P90-P95	N-ch open drain	–0.3 to +12	V
Analog input voltage	V_{AN}	Analog input pin		AV_{SS} – 0.3 to AV_{REF0} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Low-level output current	I_{OL}	1 pin		15	mA
		Total of all pins of ports 2, 4-8		75	mA
		Total of all pins of ports 0, 3, 9, 10, 12, 13		75	mA
High-level output current	I_{OH}	1 pin		–10	mA
		Total of all pins of ports 2, 4-8		–50	mA
		Total of all pins of ports 0, 3, 9, 10, 12, 13		–50	mA
Operating temperature	T_A			–10 to +60	°C
Storage temperature	T_{stg}			–10 to +80	°C

Caution If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the product(s). Be sure to use the product(s) within the ratings.

<Limitation>

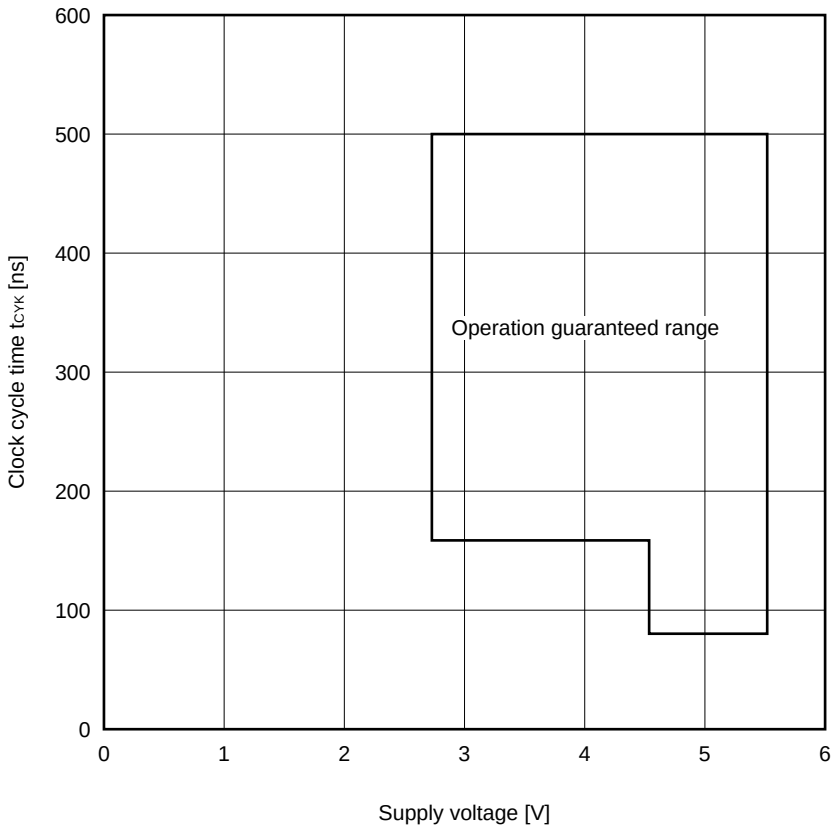
Don't select subsystem clock as the operating clock of CPU.

If the operating clock of CPU is supplied from the subsystem clock, the μPD78F4216 may malfunction.

Operating Condition

- Operating ambient temperature (T_A): –10 to +60 °C
- Supply voltage and clock cycle time: Refer to **Figure 7-1**

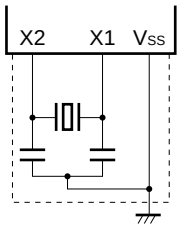
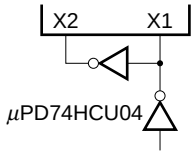
Figure 7-1. Supply Voltage and Clock Cycle Time



Capacitance (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz, 0 V except measured pins	Other than port 9			15	pF
			Port 9			20	pF
Output capacitance	C_O		Other than port 9			15	pF
			Port 9			20	pF
I/O capacitance	C_{IO}		Other than port 9			15	pF
			Port 9			20	pF

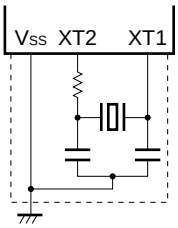
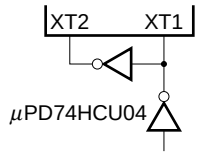
Main System Clock Oscillation Circuit Characteristics (T_A = –10 to +60 °C)

Resonator	Recommended Circuit	Item	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic or crystal resonator		Oscillation frequency (f_X)	4.5 V ≤ V_{DD} ≤ 5.5 V	2		12.5	MHz
			2.7 V ≤ V_{DD} < 4.5 V	2		6.25	
External clock		X1 input frequency (f_X)	4.5 V ≤ V_{DD} ≤ 5.5 V	2		25	MHz
			2.7 V ≤ V_{DD} < 4.5 V	2		12.5	
		X1 high-/low-level width (t_{WXH}, t_{WXL})		35		250	ns
		X1 input rise, fall time (t_{XR}, t_{XF})	4.5 V ≤ V_{DD} ≤ 5.5 V	0		5	ns
			2.7 V ≤ V_{DD} < 4.5 V	0		10	

Caution When using a main system clock oscillation circuit, wire the portion enclosed by the dotted line in the diagram above as follows to prevent adverse influence from wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with any other signal lines.**
- **Do not route the wiring in the vicinity of a line through which a high alternating current flows.**
- **Always keep the ground potential for the capacitor in the oscillation circuit at the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not extract any signal from the oscillation circuit.**

Subsystem Clock Oscillation Circuit Characteristics (T_A = –10 to +60 °C)

Resonator	Recommended Circuit	Item	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_{XT})		32	32.768	35	kHz
		Oscillation stabilization time[Note]	4.5 V ≤ V_{DD} ≤ 5.5 V		1.2	2	s
			2.2 V ≤ V_{DD} < 4.5 V			10	
External clock		XT1 input frequency (f_{XT})		32		35	kHz
		XT1 high-/low-level width (t_{XTH}, t_{XTL})		5		15	μs

Note Oscillation stabilization time is the time required for the oscillation to stabilize after power application (V_{DD}).

Cautions 1. When using a subsystem clock oscillation circuit, wire the portion enclosed by the dotted line in the diagram above as follows to prevent adverse influence from wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with any other signal lines.**
- **Do not route the wiring in the vicinity of a line through which a high alternating current flows.**
- **Always keep the ground potential for the capacitor in the oscillation circuit at the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not extract any signal from the oscillation circuit.**

2. Don't select subsystem clock as the operating clock of CPU.
If the operating clock of CPU is supplied from the subsystem clock, the μPD78F4216 may malfunction.

DC Characteristics (T_A = –10 to +60 °C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Low-level input voltage	V_{IL1}	**Note**		0		0.3 V_{DD}	V
	V_{IL2}	Total of P00-P06, P20, P22, P33, P34, P70, P72, P100-P103, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V
	V_{IL3}	P90-P95 (N-ch open drain)		0		0.3 V_{DD}	V
	V_{IL4}	Total of P10-17, P130, P131		0		0.3 V_{DD}	V
	V_{IL5}	Total of X1, X2, XT1, XT2		0		0.2 V_{DD}	V
	V_{IL6}	P25, P27		0		0.3 V_{DD}	V
High-level input voltage	V_{IH1}	**Note**		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	Total of P00-P06, P20, P22, P33, P34, P70, P72, P100-P103, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	P90-P95 (N-ch open drain)		0.7 V_{DD}		12	V
	V_{IH4}	Total of P10-17, P130, P131		0.7 V_{DD}		V_{DD}	V
	V_{IH5}	Total of X1, X2, XT1, XT2		0.8 V_{DD}		V_{DD}	V
	V_{IH6}	P25, P27		0.7 V_{DD}		V_{DD}	V
Low-level output voltage	V_{OL1}	Pins other than P40-47, P50-57, P90-P95, I_{OL} = 1.6 mA	V_{DD} = 4.5 to 5.5 V			0.4	V
		Total of P40-47, P50-57, I_{OL} = 8 mA	V_{DD} = 4.5 to 5.5 V			1.0	V
		P90-P95 I_{OL} = 15 mA	V_{DD} = 4.5 to 5.5 V		0.4	2.0	V
	V_{OL2}	I_{OL} = 400 μA				0.5	V
High-level output voltage	V_{OH1}	I_{OH} = –1 mA	V_{DD} = 4.5 to 5.5 V	V_{DD}–1.0			V
		I_{OL} = –100 μA		V_{DD}–0.5			V
Low-level input leakage current	I_{LIL1}	V_{IN} = 0 V	Except X1, X2, XT1, XT2			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
High-level input leakage current	I_{LIH1}	V_{IN} = V_{DD}	Except X1, X2, XT1, XT2			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
Low-level output leakage current	I_{LOL1}	V_{OUT} = 0 V				–3	μA
High-level output leakage current	I_{LOH1}	V_{OUT} = V_{DD}				3	μA
Supply voltage	I_{DD1}	Operation mode	f_{XX} = 12.5 MHz			40	mA
			f_{XX} = 6 MHz, V_{DD} = 2.7 to 3.3 V			20	mA
	I_{DD2}	HALT mode	f_{XX} = 12.5 MHz			20	mA
			f_{XX} = 6 MHz, V_{DD} = 2.7 to 3.3 V			10	mA
	I_{DD3}	IDLE mode	f_{XX} = 12.5 MHz			20	mA
			f_{XX} = 6 MHz, V_{DD} = 2.7 to 3.3 V			10	mA
Data retention voltage	V_{DDDR}	HALT, IDLE mode		2.7		5.5	V
Data retention current	I_{DDDR}	STOP mode	V_{DD} = 2.7 V		2	10	μA
			V_{DD} = 4.5 to 5.5 V		10	50	μA
Pull-up resistor	R_L	V_{IN} = 0 V		10	30	100	kΩ

Note P21, P23, P24, P26, P30-P32, P35-P37, P40-P47, P50-P57, P60-P67, P71, P80-P87, P120-P127

Remark Unless otherwise specified, the characteristics of the shared pins are the same as that of the port pins.

AC Characteristics (T_A = –10 to +60 °C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(1) Read/write operation (1/2)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	t_{CYK}	V_{DD} = 4.5 V to 5.5 V		80			ns
				160			ns
Address setup time (vs. ASTB↓)	t_{SAST}	V_{DD} = 5.0 V	(0.5 + a)T – 11	29			ns
		V_{DD} = 3.0 V	(0.5 + a)T – 15	65			ns
Address hold time (vs. ASTB↓)	t_{HSTLA}	V_{DD} = 5.0 V	0.5T – 19	21			ns
		V_{DD} = 3.0 V	0.5T – 24	56			ns
Address high-level width	t_{WSTH}	V_{DD} = 5.0 V	(0.5 + a)T – 17	23			ns
		V_{DD} = 3.0 V	(0.5 + a)T – 40	40			ns
Address hold time (vs. $\overline{RD}$↑)	t_{HRA}	V_{DD} = 5.0 V	0.5T – 14	26			ns
		V_{DD} = 3.0 V	0.5T – 14	66			ns
Address → $\overline{RD}$↓ delay time	t_{DAR}	V_{DD} = 5.0 V	(1 + a)T – 24	56			ns
		V_{DD} = 3.0 V	(1 + a)T – 24	136			ns
Address float time (vs. $\overline{RD}$↓)	t_{FRA}			0			ns
Address → data input time	t_{DAID}	V_{DD} = 5.0 V	(2.5 + a + n)T – 37			403	ns
		V_{DD} = 3.0 V	(2.5 + a + n)T – 52			828	ns
ASTB↓ → data input time	t_{DSTID}	V_{DD} = 5.0 V	(2 + n)T – 35			285	ns
		V_{DD} = 3.0 V	(2 + n)T – 50			590	ns
$\overline{RD}$↓ → data input time	t_{DRID}	V_{DD} = 5.0 V	(1.5 + n)T – 40			240	ns
		V_{DD} = 3.0 V	(1.5 + n)T – 50			510	ns
ASTB↓ → $\overline{RD}$↓ delay time	t_{DSTR}	V_{DD} = 5.0 V	0.5T – 9	31			ns
		V_{DD} = 3.0 V	0.5T – 9	71			ns
Data hold time (vs. $\overline{RD}$↑)	t_{HRID}			0			ns
$\overline{RD}$↑ → Address active time	t_{DRA}	V_{DD} = 5.0 V	0.5T – 2	38			ns
		V_{DD} = 3.0 V	0.5T – 12	68			ns
$\overline{RD}$↑ → ASTB↑ delay time	t_{DRST}	V_{DD} = 5.0 V	0.5T – 9	31			ns
		V_{DD} = 3.0 V	0.5T – 9	71			ns
$\overline{RD}$ low-level width	t_{WRL}	V_{DD} = 5.0 V	(1.5 + n)T – 25	95			ns
		V_{DD} = 3.0 V	(1.5 + n)T – 30	210			ns
Address → $\overline{WR}$↓ delay time	t_{DAW}	V_{DD} = 5.0 V	(1 + a)T – 24	56			ns
		V_{DD} = 3.0 V	(1 + a)T – 24	136			ns
Address hold time (vs. $\overline{WR}$↑)	t_{HWA}	V_{DD} = 5.0 V	0.5T – 14	26			ns
		V_{DD} = 3.0 V	0.5T – 14	66			ns
ASTB↓ → data output delay time	t_{DSTOD}	V_{DD} = 5.0 V	0.5T + 15			55	ns
		V_{DD} = 3.0 V	0.5T + 20			100	ns
$\overline{WR}$↓ → data output delay time	t_{DWOD}				10	62	ns

Remark T: t_{CYK} = 1/f_{XX} (f_{XX}: main system clock frequency)
a = 1 when an address wait is inserted. Otherwise, 0
n: number of wait cycle (n ≥ 0)

(1) Read/write operation (2/2)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
ASTB↓ → $\overline{WR}$↓ delay time	t_{DSTW}	V_{DD} = 5.0 V	0.5T – 9	31			ns
		V_{DD} = 3.0 V	0.5T – 9	71			ns
Data setup time (vs. $\overline{WR}$↑)	t_{SODWR}	V_{DD} = 5.0 V	(1.5 + n)T – 20	100			ns
		V_{DD} = 3.0 V	(1.5 + n)T – 25	215			ns
Data hold time (vs. $\overline{WR}$↑)	t_{HWOD}	V_{DD} = 5.0 V	0.5T – 14	26			ns
		V_{DD} = 3.0 V	0.5T – 14	66			ns
$\overline{WR}$↑ → ASTB↑ delay time	t_{DWST}	V_{DD} = 5.0 V	0.5T – 9	31			ns
		V_{DD} = 3.0 V	0.5T – 9	71			ns
$\overline{WR}$ low-level width	t_{WWL}	V_{DD} = 5.0 V	(1.5 + n)T – 25	95			ns
		V_{DD} = 3.0 V	(1.5 + n)T – 30	210			ns

Remark T: t_{CYK} = 1/f_{XX} (f_{XX}: main system clock frequency)

a = 1 when an address wait is inserted. Otherwise, 0

n: number of wait cycle (n ≥ 0)

AC Characteristics

(2) External wait timing

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Address → $\overline{WAIT}$↓ input time	t_{DAWT}	V_{DD} = 5.0 V	(2 + a)T – 40			200	ns
		V_{DD} = 3.0 V	(2 + a)T – 60			420	ns
ASTB↓ → $\overline{WAIT}$↓ input time	t_{DSTWT}	V_{DD} = 5.0 V	1.5T – 40			80	ns
		V_{DD} = 3.0 V	1.5T – 60			180	ns
ASTB↓ → $\overline{WAIT}$ hold time	t_{HSTWT}	V_{DD} = 5.0 V	(0.5 + n)T + 5	125			ns
		V_{DD} = 3.0 V	(0.5 + n)T + 10	250			ns
ASTB↓ → $\overline{WAIT}$↑ delay time	t_{DSTWTH}	V_{DD} = 5.0 V	(1.5 + n)T – 40			240	ns
		V_{DD} = 3.0 V	(1.5 + n)T – 60			500	ns
$\overline{RD}$↓ → $\overline{WAIT}$↓ input time	t_{DRWTL}	V_{DD} = 5.0 V	T – 40			40	ns
		V_{DD} = 3.0 V	T – 60			100	ns
$\overline{RD}$↓ → $\overline{WAIT}$↓ hold time	t_{HRWT}	V_{DD} = 5.0 V	nT + 5	85			ns
		V_{DD} = 3.0 V	nT + 10	170			ns
$\overline{RD}$↓ → $\overline{WAIT}$↑ delay time	t_{DRWTH}	V_{DD} = 5.0 V	(1 + n)T – 40			200	ns
		V_{DD} = 3.0 V	(1 + n)T – 60			420	ns
$\overline{WAIT}$↑ → data input time	t_{DWTID}	V_{DD} = 5.0 V	0.5T – 5			35	ns
		V_{DD} = 3.0 V	0.5T – 10			70	ns
$\overline{WAIT}$↑ → $\overline{RD}$↑ delay time	t_{DWTR}	V_{DD} = 5.0 V	0.5T	40			ns
		V_{DD} = 3.0 V	0.5T	80			ns
$\overline{WAIT}$↑ → $\overline{WR}$↑ delay time	t_{DWTW}	V_{DD} = 5.0 V	0.5T	40			ns
		V_{DD} = 3.0 V	0.5T	80			ns
$\overline{WR}$↓ → $\overline{WAIT}$↓ input time	t_{DWWTL}	V_{DD} = 5.0 V	T – 40			40	ns
		V_{DD} = 3.0 V	T – 60			100	ns
$\overline{WR}$↓ → $\overline{WAIT}$ hold time	t_{HWWT}	V_{DD} = 5.0 V	nT + 5	85			ns
		V_{DD} = 3.0 V	nT + 10	170			ns
$\overline{WR}$↓ → $\overline{WAIT}$↑ delay time	t_{DWWTH}	V_{DD} = 5.0 V	(1 + n)T – 40			200	ns
		V_{DD} = 3.0 V	(1 + n)T – 60			420	ns

Remark T: $t_{CYK} = 1/f_{XX}$ (f_{XX}: main system clock frequency)
a = 1 when an address wait is inserted. Otherwise, 0
n: number of wait cycle ($n \geq 0$)

Serial Operation (T_A = –10 to +60 °C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(a) 3-wire serial I/O mode ($\overline{SCK}$: internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}		800			ns
$\overline{SCK}$ high-/low-level width	t_{KH1}, t_{KL1}		350			ns
SI setup time (vs. $\overline{SCK}$↑)	t_{SIK1}		10			ns
SI hold time (vs. $\overline{SCK}$↑)	t_{KSI1}		40			ns
SO output delay time (vs. $\overline{SCK}$↓)	t_{KSO1}				30	ns

(b) 3-wire serial I/O mode ($\overline{SCK}$: external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK}$ high-/low-level width	t_{KH2} t_{KL2}		400			ns
SI setup time (vs. $\overline{SCK}$↑)	t_{SIK2}		10			ns
SI hold time (vs. $\overline{SCK}$↑)	t_{KSI2}		40			ns
SO output delay time (vs. $\overline{SCK}$↓)	t_{KSO2}				30	ns

(c) UART mode

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY3}	V_{DD} = 4.5 to 5.5 V	417			ns
			833			ns
ASCK high-/low-level width	t_{KH3}	V_{DD} = 4.5 to 5.5 V	208			ns
	t_{KL3}		416			ns

Other Operations (T_A = –10 to +60 °C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
NMI high-/low-level width	t_{WNIL} t_{WNIH}		10			μs
Interrupt input high-/low-level width	t_{WITL} t_{WITH}	INTP0-INTP6	10			μs
$\overline{RESET}$ high-/low-level width	t_{WRSL} t_{WRSH}		10			μs

Clock Output Operations (T_A = –10 to +60 °C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
PCL cycle time	t_{CYCL}	V_{DD} = 4.5 to 5.5 V, nT	80		31250	ns
PCL high-/low-level width	t_{CLL} t_{CLH}	V_{DD} = 4.5 to 5.5 V, 0.5T – 10	30		15615	ns
PCL rise, fall time	t_{CLR}	4.5 V ≤ V_{DD} ≤ 5.5 V			5	ns
	t_{CLF}	2.7 V ≤ V_{DD} < 4.5 V			10	ns

Remark T: t_{CYK} = 1/f_{XX} (f_{XX}: main system clock frequency)

n: division ratio set by software in the CPU

- At main system clock: n = 1, 2, 4, 8, 16, 32, 64, 128
- At subsystem clock: n = 1

A/D Converter Characteristics (T_A = –10 to +60 °C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Total error[Note]					1.2	%
Conversion time	t_{CONV}		14		144	μs
Sampling time	t_{SAMP}		24/f_{XX}			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}		2.7		AV_{DD}	V
Resistor between AV_{REF0} and AV_{SS}	R_{AVREF0}			29.4		kΩ

Note The quantization error (±1/2 LSB) is excluded.

Remark f_{XX}: main system clock frequency

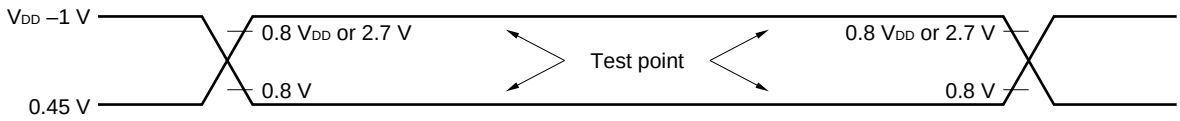
D/A Converter Characteristics (T_A = –10 to +60 °C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Resolution				8	8	8	bit
Total error		R = 2 MΩ, 2.7 V < AV_{REF1} ≤ 5.5 V				1.2	%
		R = 4 MΩ, 2.7 V < AV_{REF1} ≤ 5.5 V				0.8	%
		R = 10 MΩ, 2.7 V < AV_{REF1} ≤ 5.5 V				0.6	%
Settling time		Load condition:	4.5 V ≤ AV_{REF1} ≤ 5.5 V			10	μs
		C = 30 pF	2.7 V ≤ AV_{REF1} < 4.5 V			15	μs
Output resistor	R_0	DACS0, 1 = 7FH			5.3		kΩ
Reference voltage	AV_{REF1}			2.7		V_{DD}	V
AV_{REF1} current	AI_{REF1}	For 1 channel				2.5	mA

Data Retention Characteristics (T_A = –10 to +60 °C, V_{DD} = AV_{DD} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

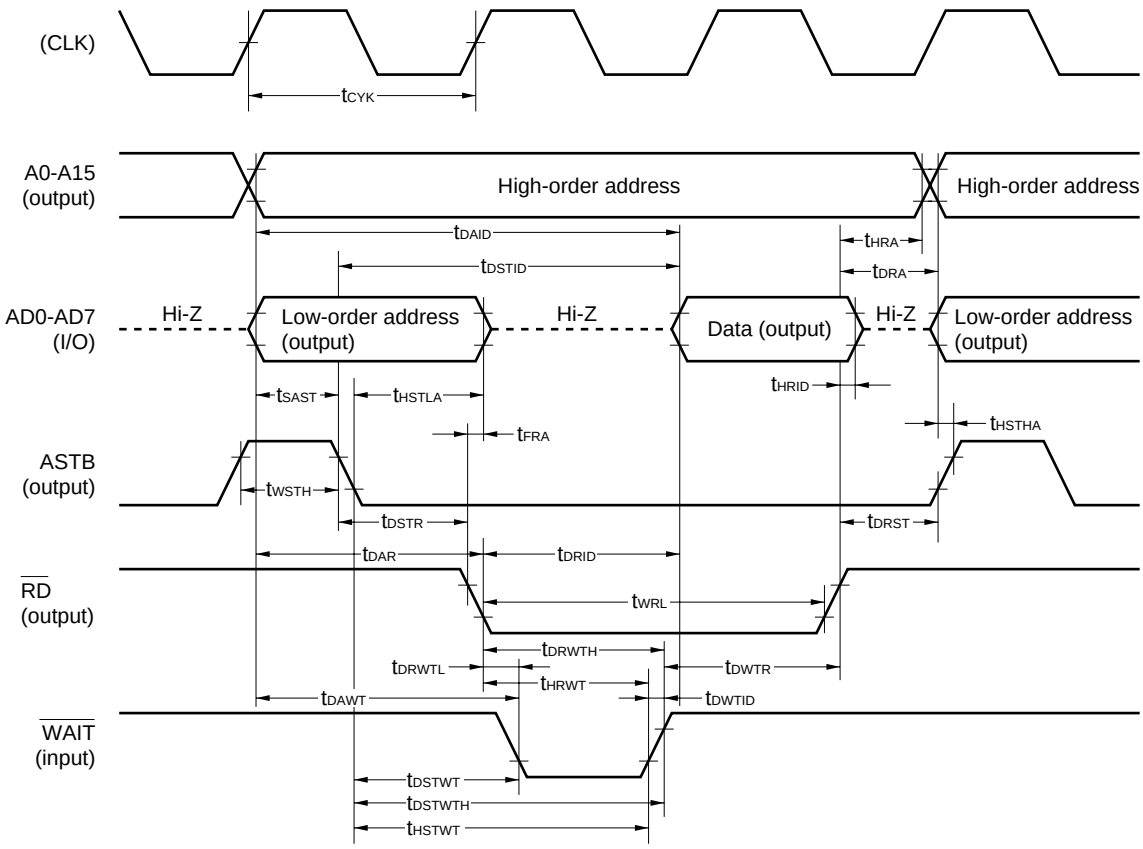
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode	2.7		5.5	V
Data retention current	I_{DDDR}	V_{DDDR} = +4.5 to 5.5 V		5	20	μA
		V_{DDDR} = +2.7 V		2	10	μA
V_{DD} rise time	t_{RVD}		200			μs
V_{DD} fall time	t_{FVD}		200			μs
V_{DD} retention time (vs. STOP mode setting)	t_{HVD}		0			ms
STOP release signal input time	t_{DREL}		0			ms
Oscillation stabilization wait time	t_{WAIT}	Crystal resonator	30			ms
		Ceramic resonator	5			ms
Low-level input voltage	V_{IL}	$\overline{\text{RESET}}$, P00/INTP0-P06/INTP6	0		0.1 V_{DDDR}	V
High-level input voltage	V_{IH}		0.9 V_{DDDR}		V_{DDDR}	V

AC Timing Test Point

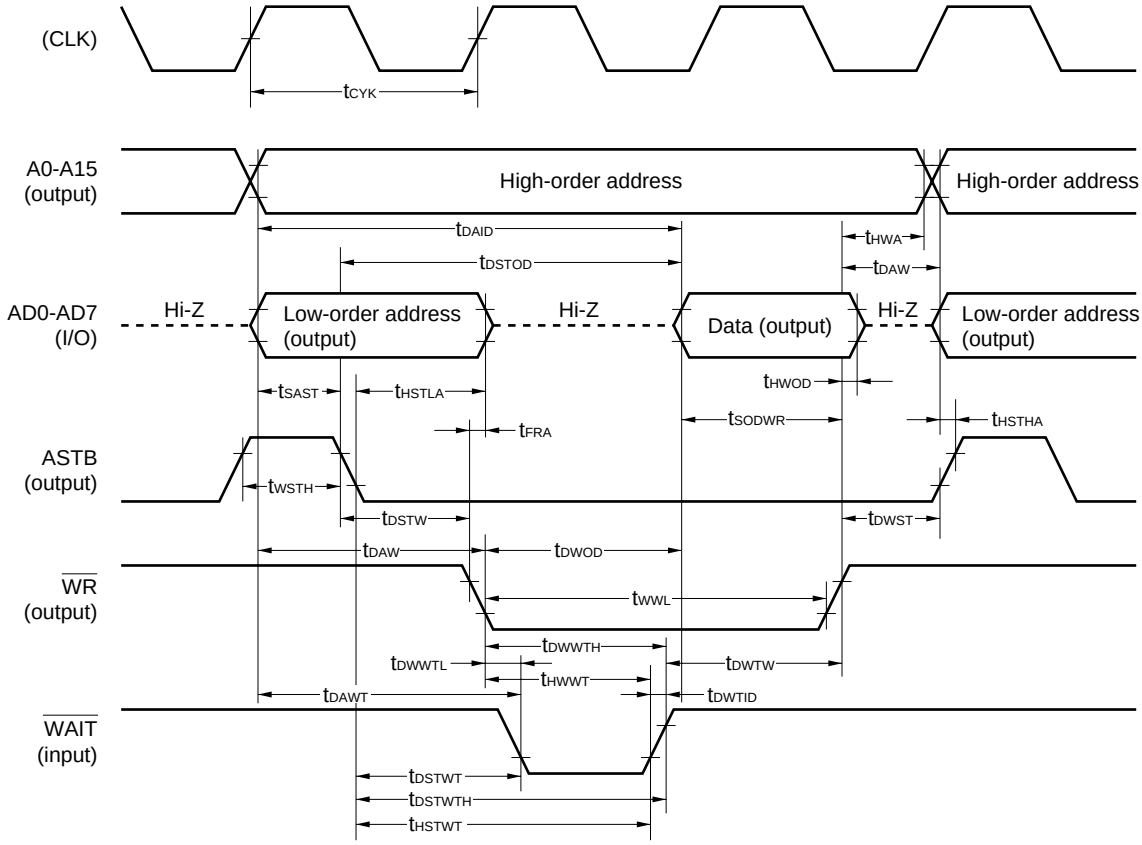


Timing Waveform

(1) Read operation

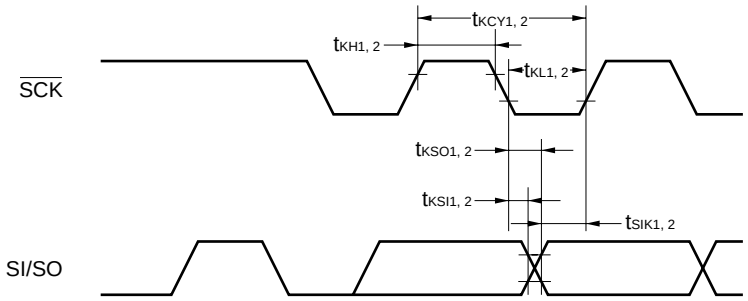


(2) Write operation

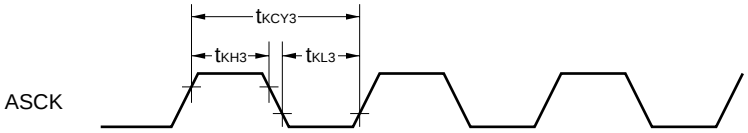


Serial Operation

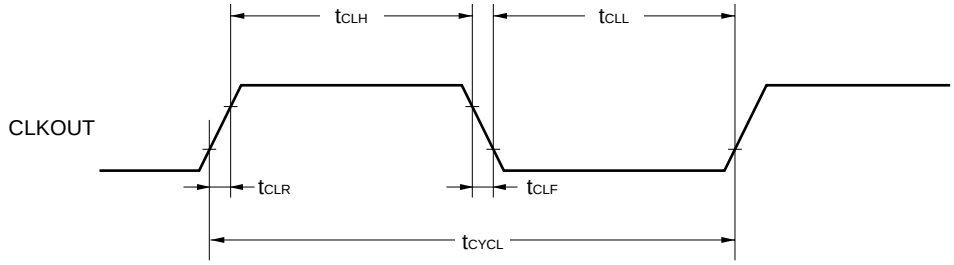
(1) 3-wire serial I/O mode



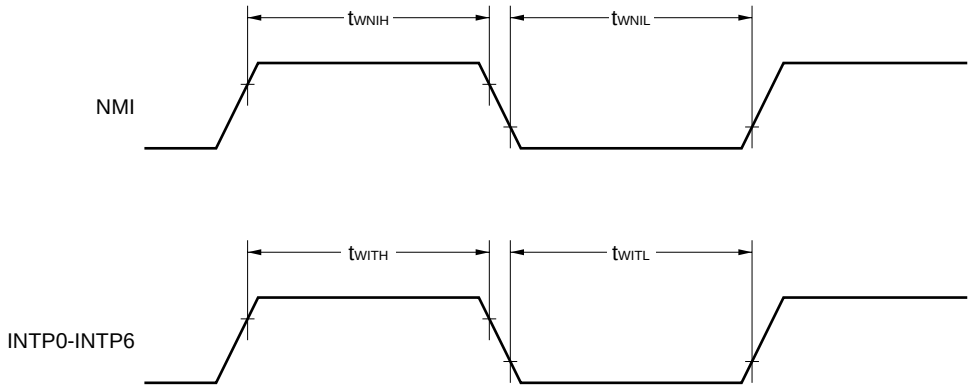
(2) UART mode



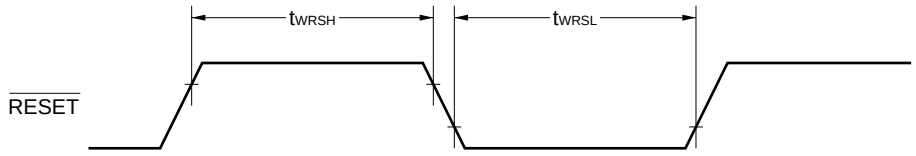
Clock Output Timing



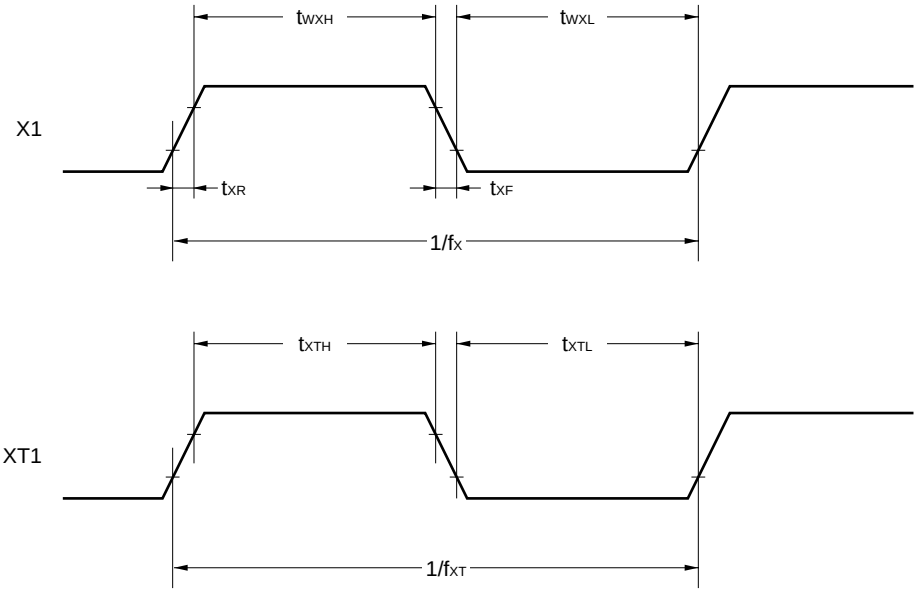
Interrupt Input Timing



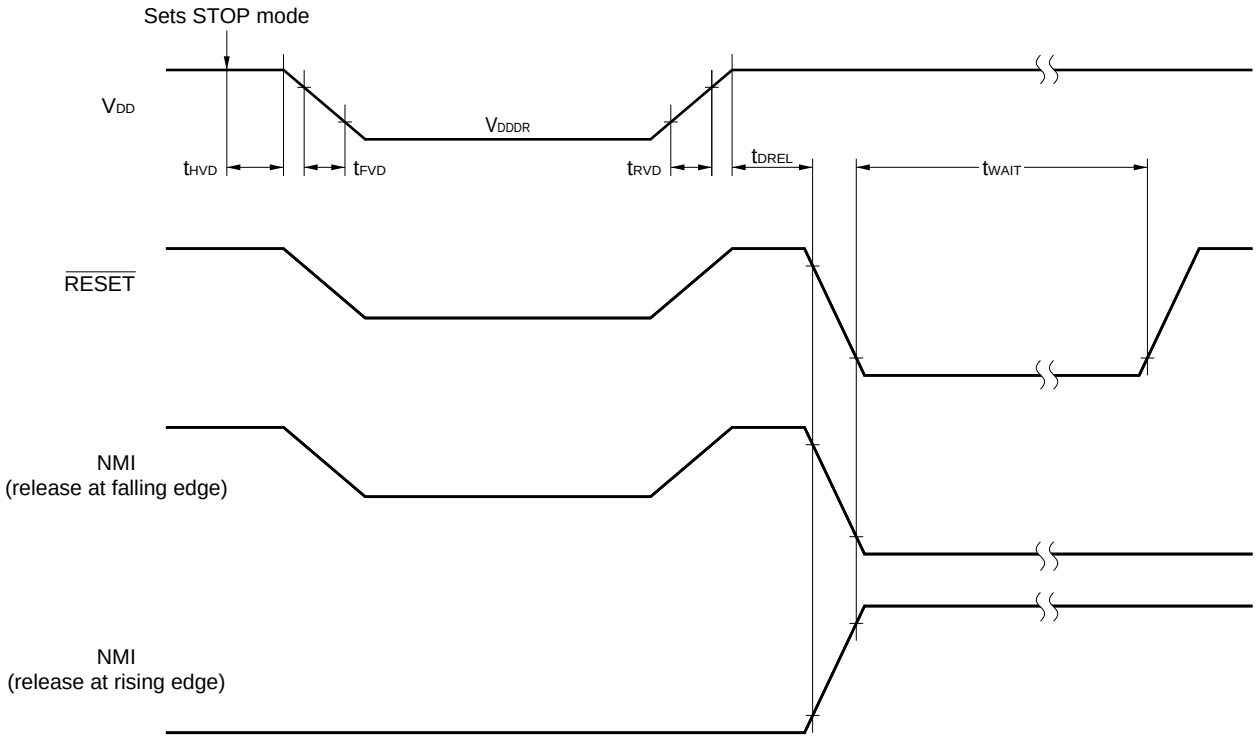
Reset Input Timing



Clock Timing

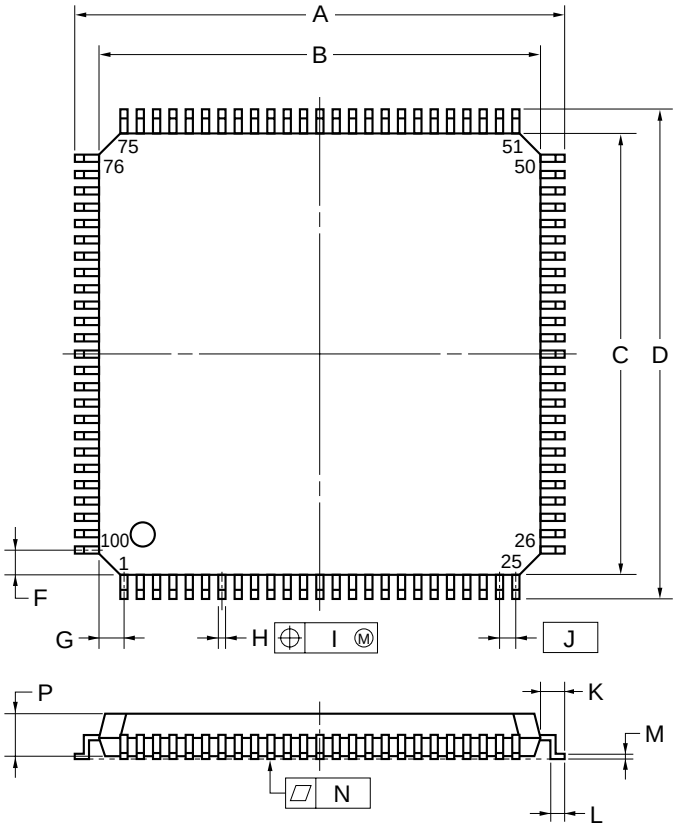


Data Retention Timing

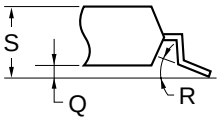


★ 8. PACKAGE DRAWINGS

100 PIN PLASTIC LQFP (FINE PITCH) (14×14)



detail of lead end



NOTE

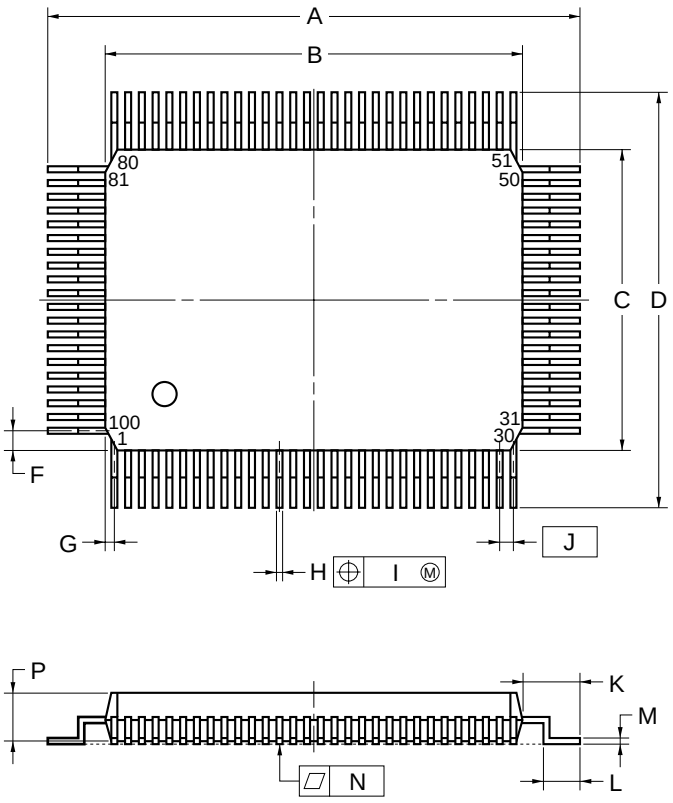
Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

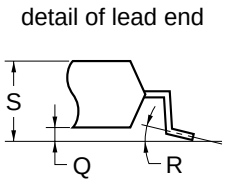
ITEM	MILLIMETERS	INCHES
A	16.00±0.20	0.630±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	16.00±0.20	0.630±0.008
F	1.00	0.039
G	1.00	0.039
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.08	0.003
J	0.50 (T.P.)	0.020 (T.P.)
K	1.00±0.20	$0.039^{+0.009}_{-0.008}$
L	0.50±0.20	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.08	0.003
P	1.40±0.05	0.055±0.002
Q	0.10±0.05	0.004±0.002
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.60 MAX.	0.063 MAX.

S100GC-50-8EU

Remark The package dimensions and materials of ES versions are the same as those of mass-production versions.

100PIN PLASTIC QFP (14x20)





NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7±0.1	$0.106^{+0.005}_{-0.004}$
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P100GF-65-3BA1-3

Remark The package dimensions and materials of ES versions are the same as those of mass-production versions.

★ 9. RECOMMENDED SOLDERING CONDITIONS

Solder this product under the following recommended conditions.

For details of the recommended soldering conditions, refer to information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended, consult NEC.

Table 9-1. Soldering Conditions for Surface-mount Type

(1) μPD78F4216GC-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14 mm)

Soldering Method(s)	Soldering Conditions	Recommended Conditions Symbol
Infrared reflow	Package peak temperature: 235 °C, Time: 30 secs. max. (210 °C min.), Number of times: twice max., Number of days: 7[Note] (after that, prebaking is necessary at 125 °C for 10 hours) <Precaution> Products other than in heat-resistance trays (such as those packaged in a magazine, taping, or non-heat-resistance tray) cannot be baked while they are in their package.	IR35-107-2
VPS	Package peak temperature: 215 °C, Time: 40 secs. max. (200 °C min.), Number of times: twice max., Number of days: 7[Note] (after that, prebaking is necessary at 125 °C for 10 hours) <Precaution> Products other than in heat-resistance trays (such as those packaged in a magazine, taping, or non-heat-resistance tray) cannot be baked while they are in their package.	VP15-107-2
Partial heating	Pin temperature: 300 °C max., Time: 3 secs. max. (per device side)	—

Note Number of days in storage after the dry pack has been opened. The storage conditions are at 25 °C, 65% RH MAX.

Caution Do not use two or more soldering methods in combination (except partial heating).

(2) μPD78F4216GF-3BA: 100-pin plastic QFP (14 × 20 mm)

Soldering Method(s)	Soldering Conditions	Recommended Conditions Symbol
Infrared reflow	Package peak temperature: 235 °C, Time: 30 secs. max. (210 °C min.), Number of times: twice max.	IR35-00-2
VPS	Package peak temperature: 215 °C, Time: 40 secs. max. (200 °C min.), Number of times: twice max.	VP15-00-2
Wave soldering	Solder bath temperature: 260 °C max., Time: 10 secs. max., Number of times: once, Preheating temperature: 120 °C max. (Package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300 °C max., Time: 3 secs. max. (per device side)	—

Caution Do not use two or more soldering methods in combination (except partial heating).

★ APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for developing systems using the μPD78F4216.
Refer to **(5) Cautions when the development tools are used.**

(1) Language processing software

RA78K4	78K/IV series common assembler package
CC78K4	78K/IV series common C compiler package
DF784216	μPD784216 subseries common device file
CC78K4-L	78K/IV series common C compiler library source file

(2) Flash memory writing tools

Flashpro II (Part number: FL-PR2), Flashpro III (Part number: FL-PR3, PG-FP3)	Dedicated flash programmer for microcomputers incorporating flash memory
FA-100GF	Adapter for flash memory writing for 100-pin plastic QFP (GF-3BA type) Wiring is needed according to the target product.
FA-100GC	Adapter for flash memory writing for 100-pin plastic LQFP (GC-8EU type) Wiring is needed according to depending on the target product.
Flashpro II controller, Flashpro III controller	This is the controlling program on PC, and is supplied with the Flashpro II and Flashpro III. Operated on Windows™ 95.

(3) Debugging tools

- **When using the IE-78K4-NS in-circuit emulator**

IE-78K4-NS	78K/IV series common in-circuit emulator
IE-70000-MC-PS-B	Power supply unit for IE-78K4-NS
IE-70000-98-IF-C	Interface adapter necessary when a PC-9800 series computer (except notebook-type personal computer) is used as host machine (C bus compatible)
IE-70000-CD-IF-A**Note**	PC card and interface cable necessary when a PC-9800 series notebook-type personal computer is used as host machine (PCMCIA compatible)
IE-70000-PC-IF-C	Interface adapter necessary when an IBM PC/AT™ compatible machine is used as host machine (ISA bus compatible)
IE-70000-PCI-IF**Note**	Interface adapter necessary when a PC with a PCI bus is used as host machine
IE-784225-NS-EM1	Emulation board for emulating the μPD784216 subseries
NP-100GF	Emulation probe for 100-pin plastic QFP (GF-3BA type)
NP-100GC	Emulation probe for 100-pin plastic LQFP (GC-8EU type)
EV-9200GC-100	Socket to be mounted on the board of the target system for 100-pin plastic QFP (GF-3BA type)
TGC-100SDW	Socket to be mounted on the board of the target system for 100-pin plastic LQFP (GC-8EU type)
ID78K4-NS	Integrated debugger for IE-78K4-NS
SM78K4	78K/IV series common system simulator
DF784218	μPD784216 subseries common device file

Note Under development

- **When using the IE-784000-R in-circuit emulator**

IE-784000-R	78K/IV series common in-circuit emulator
IE-70000-98-IF-C	Interface adapter necessary when a PC-9800 series computer (except notebook-type personal computer) is used as host machine (C bus compatible)
IE-70000-98N-IF	Interface adapter and cable necessary when a PC-9800 series notebook-type personal computer is used as host machine
IE-70000-PC-IF-C	Interface adapter necessary when an IBM PC/AT compatible machine is used as host machine (ISA compatible)
IE-70000-PCI-IF**Note**	Interface adapter necessary when a PC with a PCI bus is used as host machine
IE-78000-R-SV3	Interface adapter and cable necessary when an EWS is used as host machine
IE-784225-NS-EM1 IE-784216-R-EM1	Emulation board for emulating the μPD784216 subseries
IE-784000-R-EM	78K/IV series common emulation board
IE78K4-R-EX3	Emulation probe conversion board necessary when the IE-784225-NS-EM1 is used in the IE-784000-R. Not necessary when the IE-784216-R-EM1 is used.
EP-78064GF-R	Emulation probe for 100-pin plastic QFP (GF-3BA type)
EP-78064GC-R	Emulation probe for 100-pin plastic QFP (GC-8EU type)
EV-9200GF-100	Socket to be mounted on the board of the target system made for the 100-pin plastic QFP (GF-3BA type)
TGC-100SDW	Socket to be mounted on the board of the target system for 100-pin plastic LQFP (GC-8EU type)
ID78K4	Integrated debugger for IE-784000-R
SM78K4	78K/IV series common system simulator
DF784218	μPD784216 subseries common device file

Note Under development

(4) Real-time OS

RX78K/IV	Real-time OS for 78K/IV series
MX78K4	OS for 78K/IV series

(5) Cautions when the development tools are used

- The ID78K4-NS, ID78K4, and SM78K4 are used in combination with the DF784218.
- The CC78K4 and RX78K/IV are used in combination with the RA78K4 and DF784218.
- FL-PR2, FL-PR3, FA-100GF, FA-100GC, NP-100GF, and NP-100GC are product of Naito Densei Machida Mfg. Co., Ltd. (TEL: (044)822-3813). Contact an NEC distributor when purchasing these products.
- TGC-100SDW is a product of Tokyo Eletech Corp.
  Reference: Daimaru Kogyo Ltd. Electronics Dept. (TEL: Tokyo 03-3820-7112)
  Electronics 2nd Dept. (TEL: Osaka 06-244-6672)
- For development tools made by third parties, refer to **78K/IV series Selection Guide (U13355E)**.
- Host machines and OSs compatible with the software are as follows:

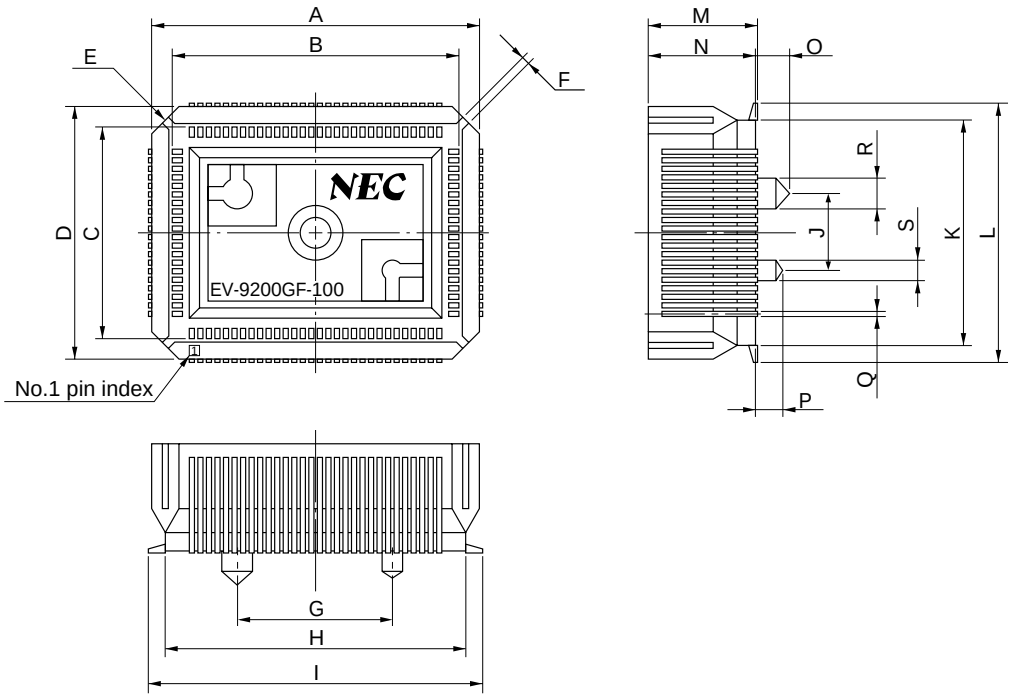
Host Machine [OS] / Software	PC	EWS
	PC-9800 Series [Windows] IBM PC/AT compatible machines [Japanese/English Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K4	○Note	○
CC78K4	○Note	○
ID78K4-NS	○	—
ID78K4	○	○
SM78K4	○	—
RX78K/IV	○Note	○
MX78K4	○Note	○

Note DOS based software

★ **Package Dimensions of Conversion Socket (EV-9200GF-100) and Recommended Pattern for Board Mounting**

EV-9200GF-100 is mounted on the board combining with the EP-78064GF-R.

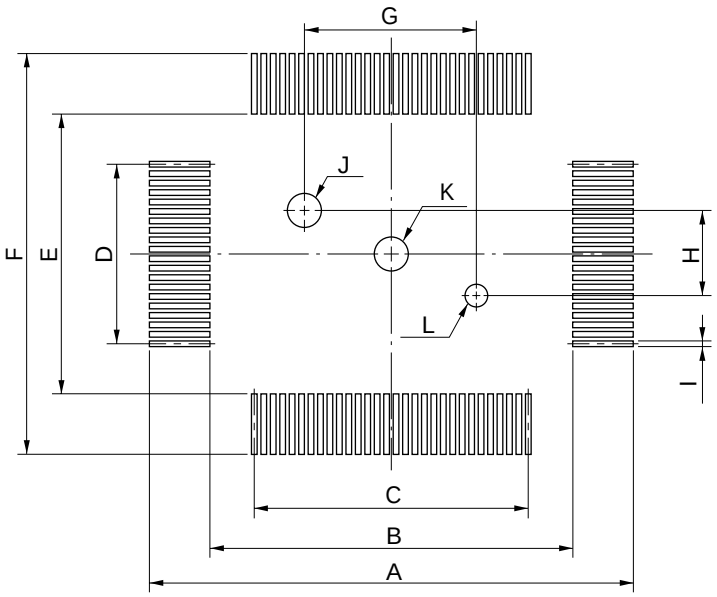
Figure A-1. Package Dimensions of EV-9200GF-100 (for reference)



EV-9200GF-100-G0E

ITEM	MILLIMETERS	INCHES
A	24.6	0.969
B	21	0.827
C	15	0.591
D	18.6	0.732
E	4-C 2	4-C 0.079
F	0.8	0.031
G	12.0	0.472
H	22.6	0.89
I	25.3	0.996
J	6.0	0.236
K	16.6	0.654
L	19.3	0.76
M	8.2	0.323
N	8.0	0.315
O	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	φ2.3	φ0.091
S	φ1.5	φ0.059

Figure A-2. Recommended Pattern for Board Mounting (for reference)



EV-9200GF-100-P1E

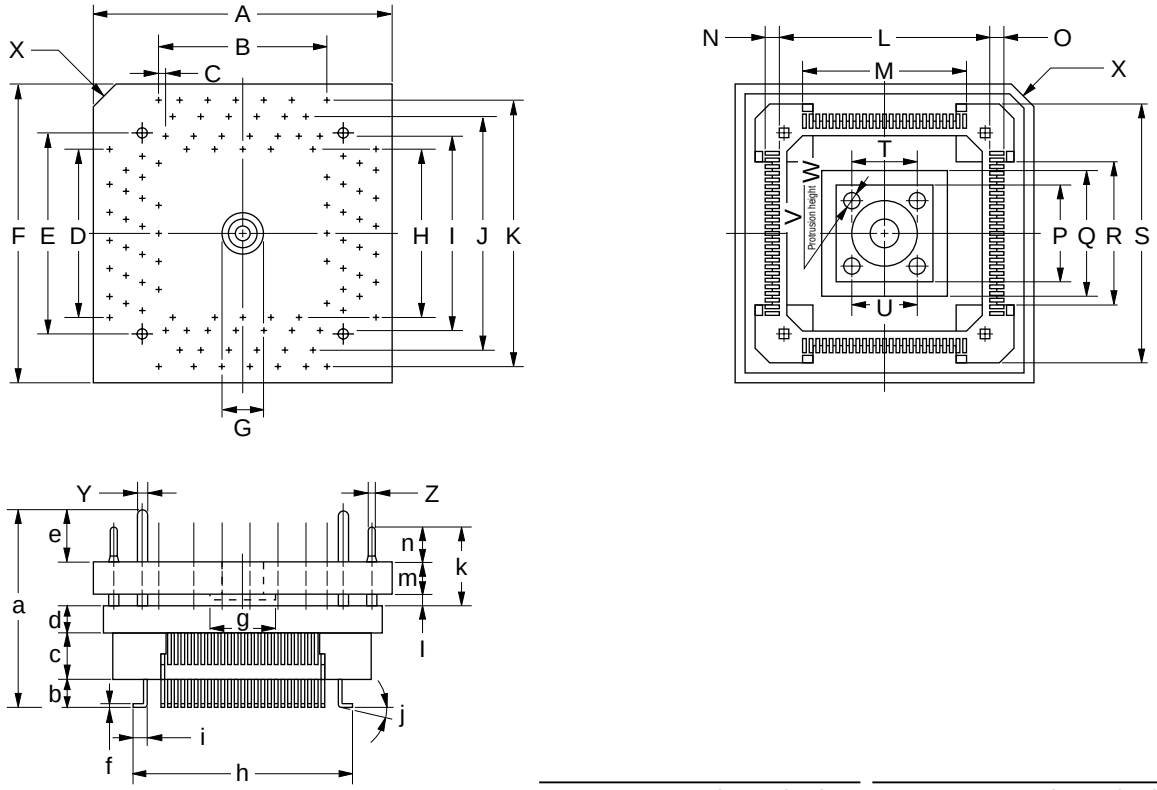
ITEM	MILLIMETERS	INCHES
A	26.3	1.035
B	21.6	0.85
C	$0.65\pm0.02\times29=18.85\pm0.05$	$0.026^{+0.001}_{-0.002}\times1.142=0.742^{+0.002}_{-0.002}$
D	$0.65\pm0.02\times19=12.35\pm0.05$	$0.026^{+0.001}_{-0.002}\times0.748=0.486^{+0.003}_{-0.002}$
E	15.6	0.614
F	20.3	0.799
G	12 ± 0.05	$0.472^{+0.003}_{-0.002}$
H	6 ± 0.05	$0.236^{+0.003}_{-0.002}$
I	0.35 ± 0.02	$0.014^{+0.001}_{-0.001}$
J	$\phi2.36\pm0.03$	$\phi0.093^{+0.001}_{-0.002}$
K	$\phi2.3$	$\phi0.091$
L	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

Package Dimensions of Conversion Adapter (TGC-100SDW)

TGC-100SDW is mounted on the board combining with the EP-78064GC-R.

Figure A-3. Package Dimensions of TGC-100SDW (for reference)



ITEM	MILLIMETERS	INCHES
A	21.55	0.848
B	0.5x24=12	0.020x0.945=0.472
C	0.5	0.020
D	0.5x24=12	0.020x0.945=0.472
E	15.0	0.591
F	21.55	0.848
G	ϕ3.55	ϕ0.140
H	10.9	0.429
I	13.3	0.524
J	15.7	0.618
K	18.1	0.713
L	13.75	0.541
M	0.5x24=12.0	0.020x0.945=0.472
N	1.125±0.3	0.044±0.012
O	1.125±0.2	0.044±0.008
P	7.5	0.295
Q	10.0	0.394
R	11.3	0.445
S	18.1	0.713
T	ϕ5.0	ϕ0.197
U	5.0	0.197
V	4-ϕ1.3	4-ϕ0.051
W	1.8	0.071
X	C 2.0	C 0.079
Y	ϕ0.9	ϕ0.035
Z	ϕ0.3	ϕ0.012

ITEM	MILLIMETERS	INCHES
a	14.45	0.569
b	1.85±0.25	0.073±0.010
c	3.5	0.138
d	2.0	0.079
e	3.9	0.154
f	0.25	0.010
g	ϕ4.5	ϕ0.177
h	16.0	0.630
i	1.125±0.3	0.044±0.012
j	0~5°	0.000~0.197°
k	5.9	0.232
l	0.8	0.031
m	2.4	0.094
n	2.7	0.106

TGC-100SDW-G1E

note: Product by TOKYO ELETECH CORPORATION.

★ APPENDIX B. RELATED DOCUMENTS

Device-related documents

Document	Document No.	
	Japanese	English
μPD784214, 784215, 784216 Data Sheet	U11813J	U11813E
μPD78F4216 Data Sheet	U11825J	This document
μPD784216, 784216Y Subseries User's Manual - Hardware	U12015J	U12015E
μPD784216 Subseries Special Function Register Table	U12054J	–
78K/IV Series User's Manual - Instruction	U10905J	U10905E
78K/IV Series Instruction Table	U10594J	–
78K/IV Series Instruction Set	U10595J	–
78K/IV Series Application Note - Software Basics	U10095J	U10095E

Development tool-related documents (User's Manuals)

Document		Document No.	
		Japanese	English
RA78K4 Assembler Package	Operation	U11334J	U11334E
	Language	U11162J	U11162E
RA78K4 Structured Assembler Preprocessor		U11743J	U11743E
CC78K4 C Compiler	Operation	U11572J	U11572E
	Language	U11571J	U11571E
IE-78K4-NS		U13356J	U13356E
IE-784000-R		U12903J	U12903E
IE-784218-R-EM1		U12155J	U12155E
IE-784225-NS-EM1		Planned	Planned
EP-78064		EEU-934	EEU-1469
SM78K4 System Simulator Windows Based	Reference	U10093J	U10093E
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092J	U10092E
ID78K4-NS Integrated Debugger	Reference	U12796J	U12796E
ID78K4 Integrated Debugger Windows Based	Reference	U10440J	U10440E
ID78K4 Integrated Debugger HP-UX, SunOS, NEWS-OS based	Reference	U11960J	U11960E

Caution The contents of the above related documents are subject to change without notice. Be sure to use the latest edition of the document when designing your system.

Embedded software-related documents (User's Manual)

Document		Document No.	
		Japanese	English
78K/IV Series Real-Time OS	Fundamental	U10603J	U10603E
	Installation	U10604J	U10604E
	Debugger	U10364J	—
78K/IV Series OS, MX78K4	Fundamental	U11779J	—

Other documents

Document	Document No.	
	Japanese	English
NEC IC Package Manual (CD-ROM)	—	C13388E
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability and Quality Control	C10983J	C10983E
Guide to Prevent Damages for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Semiconductor Quality/Reliability Handbook	C12769J	—
Microcontroller-Related Product Guide - Third Parties	U11416J	—

Caution The contents of the above related documents are subject to change without notice. Be sure to use the latest edition of the document when designing your system.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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