DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD789860, 789861

8-BIT SINGLE-CHIP MICROCONTROLLERS

The μPD789860 and μPD789861 are products of the μPD789860, 789861 Subseries in the 78K/0S Series.

In addition to an 8-bit CPU, they have on-chip hardware for keyless entry, including EEPROM™, a key return function, and a timer with a carrier generator that can easily output waveforms for infrared remote control. The μPD78E9860 and μPD78E9861, EEPROM products that can operate using the same power supply voltage as mask ROM products, and various development tools also are under development.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD789860, 789861 Subseries User's Manual: U14826E
78K/0S Series User's Manual Instructions: U11047E

FEATURES

- Internal ROM: 4 KB
- On-chip EEPROM needed for reading/writing by program in RAM area: 32 bytes
- System clock oscillator
  - μPD789860: Crystal/ceramic oscillator
  - μPD789861: RC oscillator (externally attached resistor and capacitor)
- Minimum instruction execution time
  - μPD789860: 0.4 μs/1.6 μs (@ f_X = 5.0 MHz operation)
  - μPD789861: 2.0 μs/8.0 μs (@ f_{CC} = 1.0 MHz operation)
- I/O ports: 14
- Timer: 3 channels
  - 8-bit timer: 2 channels
  - Watchdog timer: 1 channel
- On-chip power-on-clear circuit
- On-chip bit sequential buffer
- Power supply voltage: V_{DD} = 1.8 to 3.6 V

APPLICATIONS

Keyless entry and other automotive electrical equipment

In this Data Sheet, the oscillation frequency of a crystal/ceramic oscillator (μPD789860) is described as f_X and the oscillation frequency of an RC oscillator (μPD789861) is described as f_{CC}.

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Date Published August 2001 N CP(K)

The mark ★ shows major revised points.

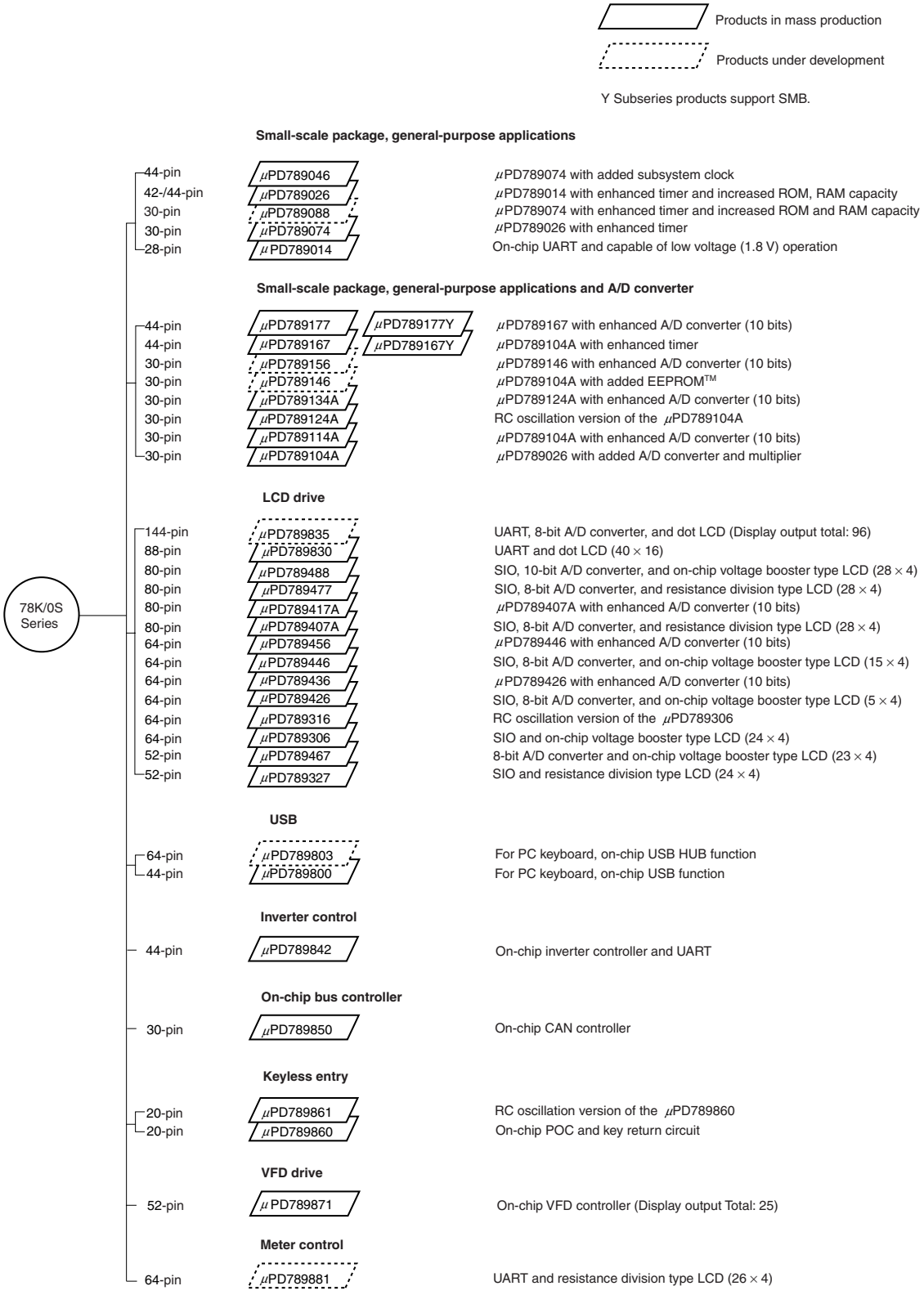
ORDERING INFORMATION

Part Number	Package
μPD789860MC-×××-5A4	20-pin plastic SSOP (7.62 mm (300))
μPD789861MC-×××-5A4	20-pin plastic SSOP (7.62 mm (300))

Remark ××× indicates ROM code suffix.

★ 78K/0S SERIES LINEUP

The products in the 78K/0S Series are listed below. The names enclosed in boxes are subseries names.



Remark VFD (Vacuum Fluorescent Display) is referred to as "FIP™" (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major functional differences among the subseries are listed below.

Series for LCD drive, general-purpose applications

Subseries Name \ Function		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_{DD} MIN. Value	Remarks
			8-Bit	16-Bit	Watch	WDT						
Small-scale package, general-purpose applications	μPD789046	16 KB	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART: 1 ch)	34	1.8 V	–
	μPD789026	4 KB to 16 KB			–							
	μPD789088	16 KB to 32 KB	3 ch							24		
	μPD789074	2 KB to 8 KB	1 ch									
	μPD789014	2 KB to 4 KB	2 ch	–						22		
Small-scale package, general-purpose applications and A/D converter	μPD789177	16 KB to 24 KB	3 ch	1 ch	1 ch	1 ch	–	8 ch	1 ch (UART: 1 ch)	31	1.8 V	–
	μPD789167						8 ch	–				
	μPD789156	8 KB to 16 KB	1 ch		–		–	4 ch		20		On-chip EEPROM
	μPD789146						4 ch	–				
	μPD789134A	2 KB to 8 KB					–	4 ch				RC oscillation version
	μPD789124A						4 ch	–				
	μPD789114A						–	4 ch				–
	μPD789104A						4 ch	–				
LCD drive	μPD789835	24 KB to 60 KB	6 ch	–	1 ch	1 ch	3 ch	–	1 ch (UART: 1 ch)	37	1.8 V Note	Dot LCD supported
	μPD789830	24 KB	1 ch	1 ch			–			30	2.7 V	
	μPD789488	32 KB	3 ch					8 ch	2 ch (UART: 1 ch)	45	1.8 V	–
	μPD789477	24 KB					8 ch	–				
	μPD789417A	12 KB to 24 KB					–	7 ch	1 ch (UART: 1 ch)	43		
	μPD789407A						7 ch	–				
	μPD789456	12 KB to 16 KB	2 ch				–	6 ch		30		
	μPD789446						6 ch	–				
	μPD789436						–	6 ch		40		
	μPD789426						6 ch	–				
	μPD789316	8 KB to 16 KB					–		2 ch (UART: 1 ch)	23		RC oscillation version
	μPD789306											–
	μPD789467	4 KB to 24 KB		–			1 ch		–	18		
	μPD789327						–		1 ch	21		

Note 10-bit timer: 1 channel

Series for ASSP

Subseries Name \ Function		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_{DD} MIN. Value	Remarks
			8-Bit	16-Bit	Watch	WDT						
USB	μPD789803	8 KB to 16 KB	2 ch	–	–	1 ch	–	–	2 ch (USB: 1 ch)	41	3.6 V	–
	μPD789800	8 KB								31	4.0 V	
Inverter control	μPD789842	8 KB to 16 KB	3 ch	**Note 1**	1 ch	1 ch	8 ch	–	1 ch (UART: 1 ch)	30	4.0 V	–
On-chip bus controller	μPD789850	16 KB	1 ch	1 ch	–	1 ch	4 ch	–	2 ch (UART: 1 ch)	18	4.0 V	–
Keyless entry	μPD789861	4 KB	2 ch	–	–	1 ch	–	–	–	14	1.8 V	RC oscillation version, on-chip EEPROM
	μPD789860											On-chip EEPROM
VFD drive	μPD789871	4 KB to 8 KB	3 ch	–	1 ch	1 ch	–	–	1 ch	33	2.7 V	–
Meter control	μPD789881	16 KB	2 ch	1 ch	–	1 ch	–	–	1 ch (UART: 1 ch)	28	2.7 V Note 2	–

Notes 1. 10-bit timer: 1 channel

2. Flash memory version: 3.0 V

OVERVIEW OF FUNCTIONS

Item \ Part Number		μPD789860	μPD789861
Internal memory	ROM	4 KB	
	High-speed RAM	128 bytes	
	EEPROM	32 bytes	
Oscillator		Ceramic/crystal oscillator	RC oscillator
Minimum instruction execution time		0.4 μs/1.6 μs (@ f_X = 5.0 MHz operation)	2.0 μs/8.0 μs (@ f_{CC} = 1.0 MHz operation)
General-purpose registers		8 bits × 8 registers	
Instruction set		• 16-bit operation • Bit manipulation (set, reset, test), etc.	
I/O ports		Total: 14 CMOS I/O: 10 CMOS input: 4	
Timer		• 8-bit timer: 2 channels • Watchdog timer: 1 channel	
Power-on-clear circuit	POC circuit	Generates internal reset signal according to comparison of detection voltage to power supply voltage	
	LVI circuit	Generates interrupt request signal according to comparison of detection voltage to power supply voltage	
Bit sequence buffer		8 bits × 8 bits = 16 bits	
Key return function		Generates key return signal according to falling edge detection	
Vectored interrupt sources	Maskable	Internal: 5	
	Non-maskable	Internal: 1, External: 1	
Power supply voltage		V_{DD} = 1.8 to 3.6 V	
Operating ambient temperature		T_A = –40 to +85°C	
Package		20-pin plastic SSOP (7.62 mm (300))	

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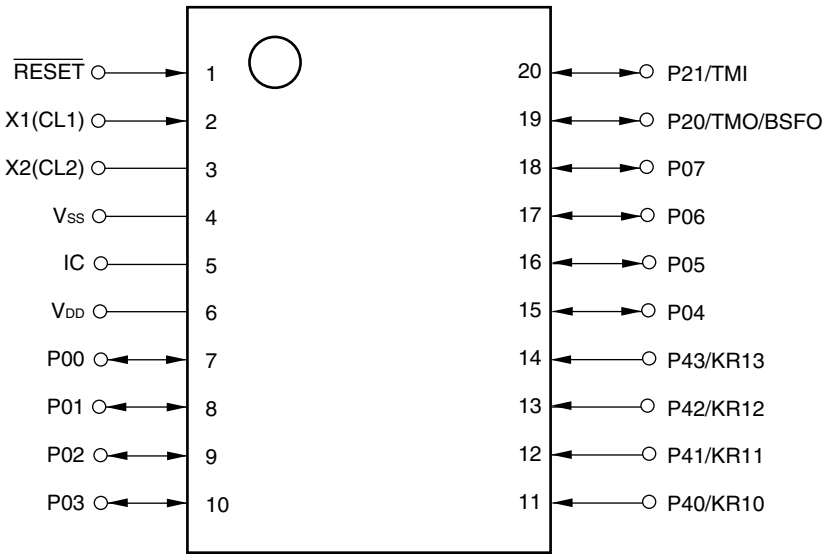
1. PIN CONFIGURATION (TOP VIEW)

- 20-pin plastic SSOP (7.62 mm (300))
  μPD789860MC-×××-5A4
  μPD789861MC-×××-5A4

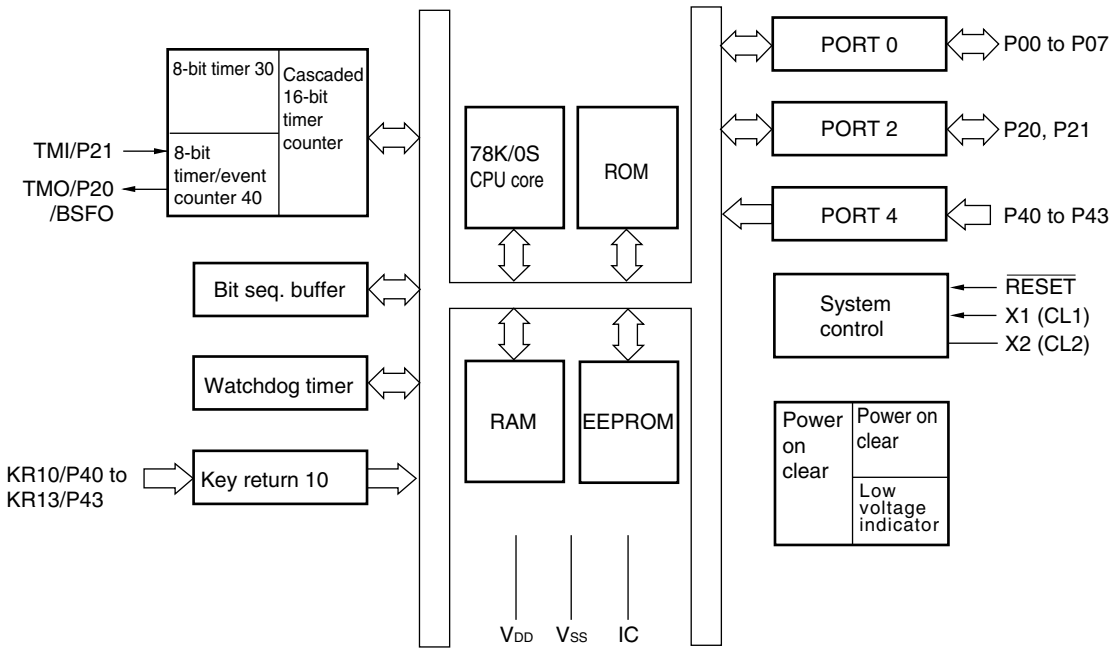


Caution Connect the IC (Internally Connected) pin directly to V_{SS}.

Remark Pin connections in parentheses apply to the μPD789861.

BSFO:	Bit sequential buffer output	$\overline{\text{RESET}}$:	Reset
CL1, CL2:	RC oscillator	TMI:	Timer input
IC:	Internally connected	TMO:	Timer output
KR10 to KR13:	Key return	V_{DD}:	Power supply
P00 to P07:	Port 0	V_{SS}:	Ground
P20, P21:	Port 2	X1, X2:	Crystal/ceramic oscillator
P40 to P43:	Port 4		

2. BLOCK DIAGRAM



Remark Items in parentheses apply to the μPD789861.

3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P07	I/O	Port 0 8-bit I/O port Input/output can be specified in 1-bit units.	Input	–
P20	I/O	Port 2 2-bit I/O port Input/output can be specified in 1-bit units.	Input	TMO/BSFO
P21				TMI
P40 to P43	Input	Port 4 4-bit input-only port. An on-chip pull-up resistor can be specified by the mask option.	Input	KR10 to KR13

3.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
TMI	Input	8-bit timer (TM40) input	Input	P21
TMO	Output	8-bit timer (TM40) output	Input	P20/BSFO
BSFO	Output	Bit sequential buffer (BSF10) output	Input	P20/TMO
KR10 to KR13	Input	Key return input	Input	P40 to P43
X1 Note 1	Input	Connecting crystal resonator for system clock oscillation	–	–
X2 Note 1	–		–	–
CL1 Note 2	Input	Connecting resistor (R) and capacitor (C) for system clock oscillation	–	–
CL2 Note 2	–		–	–
$\overline{\text{RESET}}$	Input	System reset input	Input	–
V_{DD}	–	Positive power supply	–	–
V_{SS}	–	Ground potential	–	–
IC	–	Internally connected. Connect directly to V_{SS}.	–	–

Notes 1. μPD789860 only.

2. μPD789861 only.

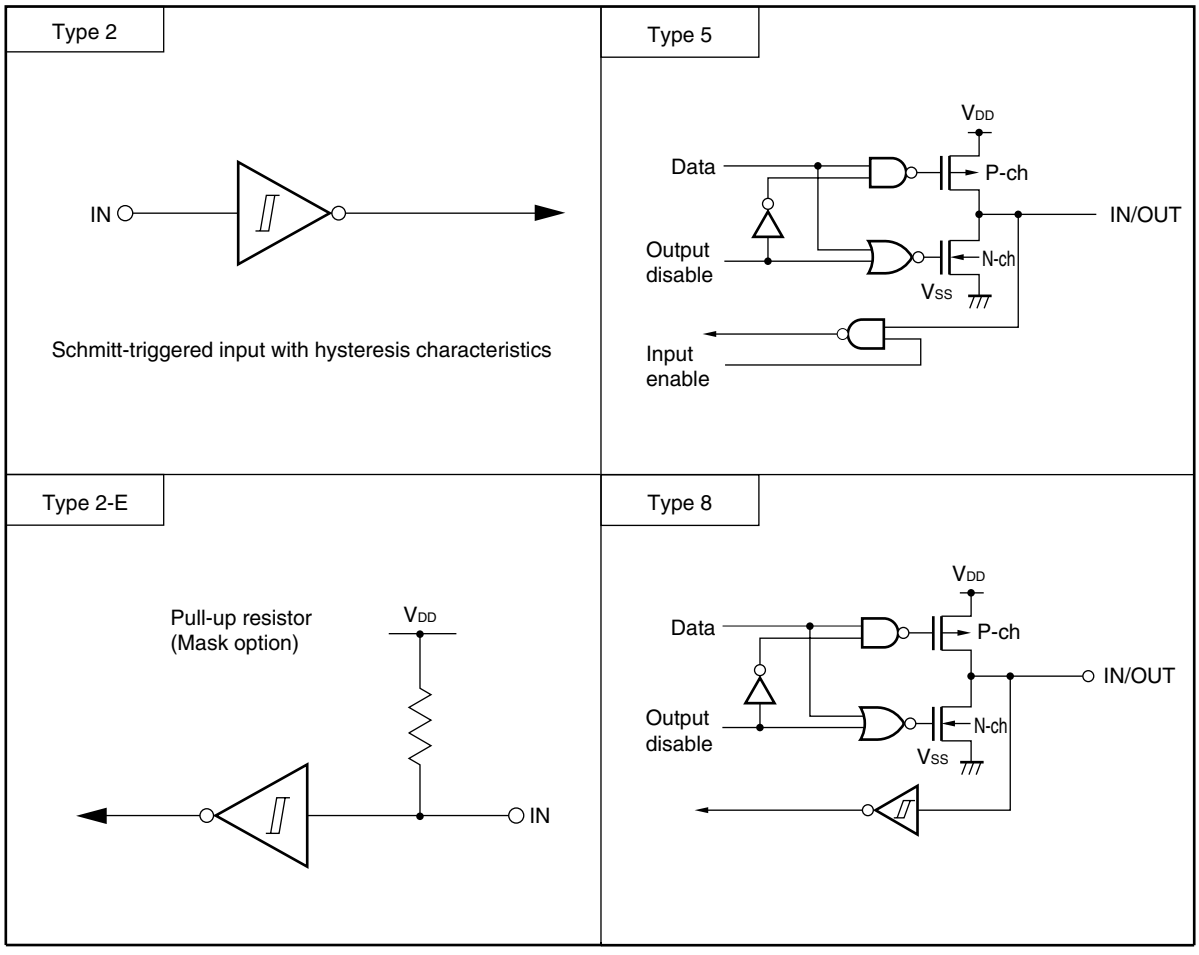
3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type for each pin and recommended connections of unused pins are shown in Table 3-1.
For the I/O circuit configuration of each type, refer to Figure 3-1.

Table 3-1. Types of Pin I/O Circuits and Recommended Connection of Unused Pins

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection of Unused Pins
P00 to P07	5	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor.
P20/TMO/BSFO	8		Output: Leave open.
P21/TMI			
P40/KR10 to P43/KR13	2-E	Input	Connect directly to V_{DD} or V_{SS}.
$\overline{\text{RESET}}$	2		–
IC	–	–	Connect directly to V_{SS}.

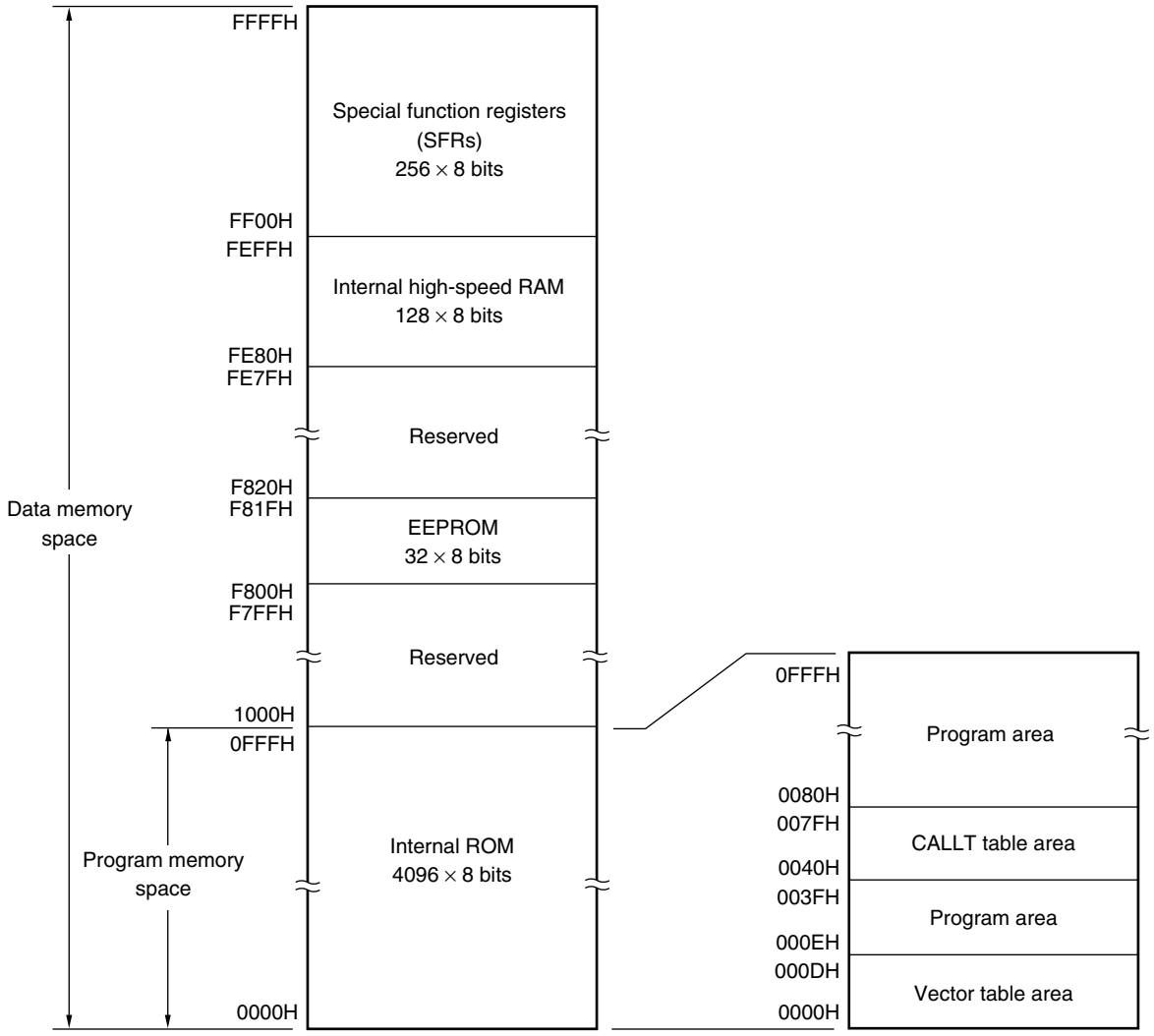
Figure 3-1. Pin I/O Circuits



4. MEMORY SPACE

The μPD789860 and μPD789861 can each access a 64 KB memory space. Figure 4-1 shows the memory map.

Figure 4-1. Memory Map

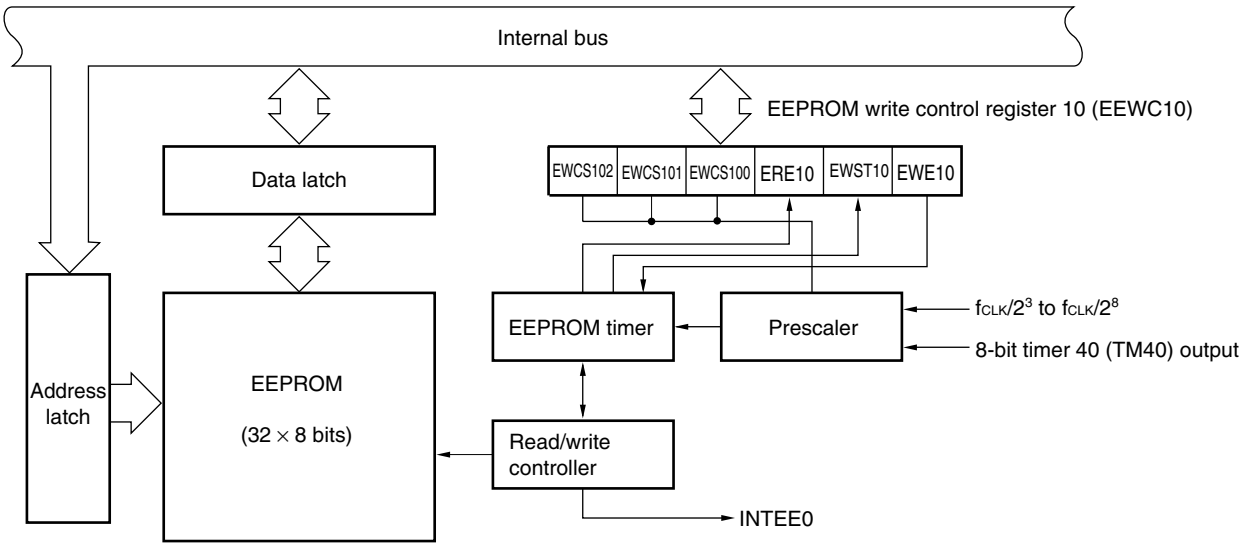


5. EEPROM

Besides internal high-speed RAM, the μPD789860 and μPD789861 have 32 × 8 bits of electrically erasable PROM (EEPROM) on-chip as data memory.

Unlike normal RAM, EEPROM can maintain its contents even if its power supply is cut. In addition, unlike EPROM, its electrical contents can be erased without using ultraviolet rays.

Figure 5-1. EEPROM Block Diagram



Remark f_{CLK}: fx or fCC

6. PERIPHERAL HARDWARE FUNCTIONS

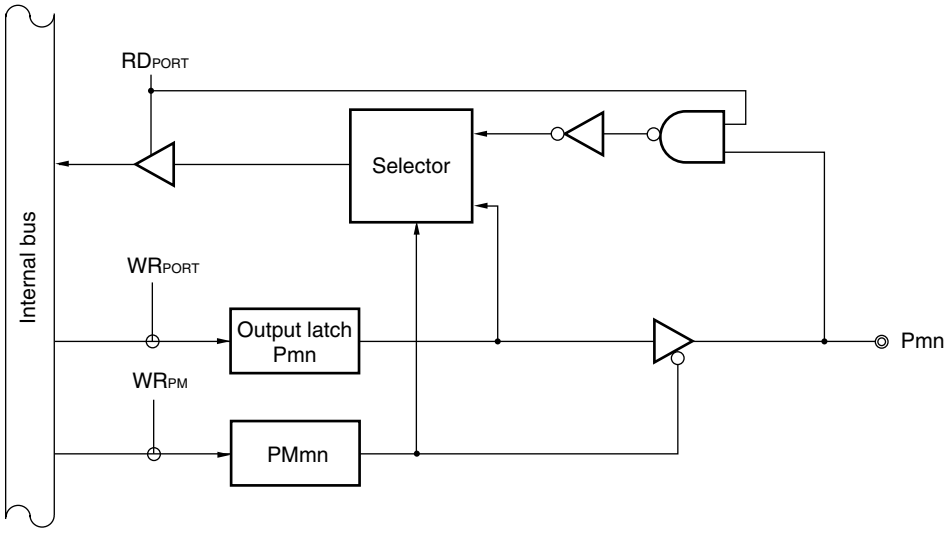
6.1 Ports

The μPD789860 and μPD789861 are provided with the ports shown in Table 6-1, by which many kinds of control are possible. Moreover, these have a variety of alternate functions besides their functions as digital I/O ports. Refer to **3 PIN FUNCTIONS** for details of the alternate functions.

Table 6-1. Port Functions

Name	Pin Name	Function
Port 0	P00 to P07	I/O port. Input/output can be specified in 1-bit units.
Port 2	P20, P21	I/O port. Input/output can be specified in 1-bit units.
Port 4	P40 to P43	Input-only port. Use of an on-chip pull-up resistor can be specified by the mask option.

Figure 6-1. Basic Configuration of CMOS Port



Caution Figure 6-1 is the basic configuration of a CMOS I/O port. The configuration varies according to the functions of alternate-function pins.

Remarks PMmn: Bit n of port mode register m (m = 0, 2 n = 0 to 7)
Pmn: Bit n of port m (m = 0, 2 n = 0 to 7)
RD: Port read signal
WR: Port write signal

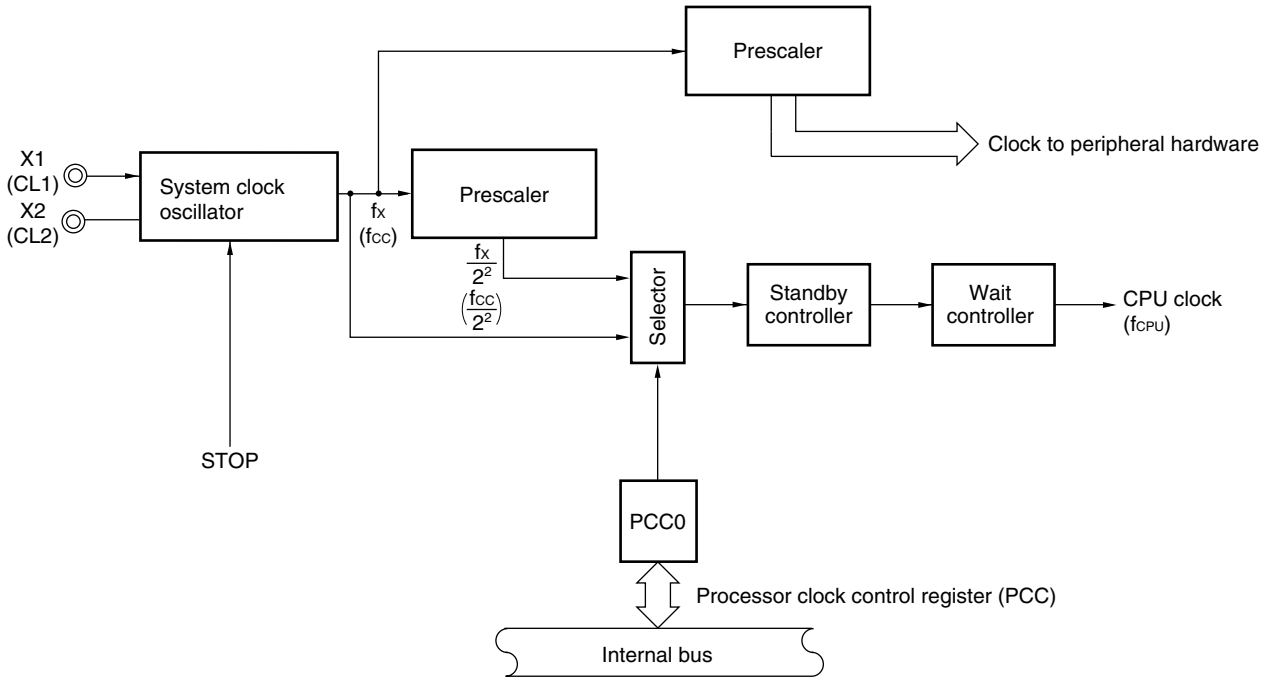
6.2 Clock Generator

The clock generator specifications differ as follows for the μPD789860 and μPD789861.

- Ceramic/crystal oscillation: μPD789860
  Oscillates at frequency from 1.0 to 5.0 MHz. Minimum instruction execution time can be switched between 0.4 μs and 1.6 μs (@ 5.0 MHz operation).

- RC oscillation: μPD789861
  Oscillates at frequency of 1.0 MHz ±15%. Minimum instruction execution time can be switched between 2.0 μs and 8.0 μs (@ 1.0 MHz operation).

Figure 6-2. Clock Generator Block Diagram



Remark Items in the parentheses apply to the RC oscillation version (μPD789861).

6.3 Timer

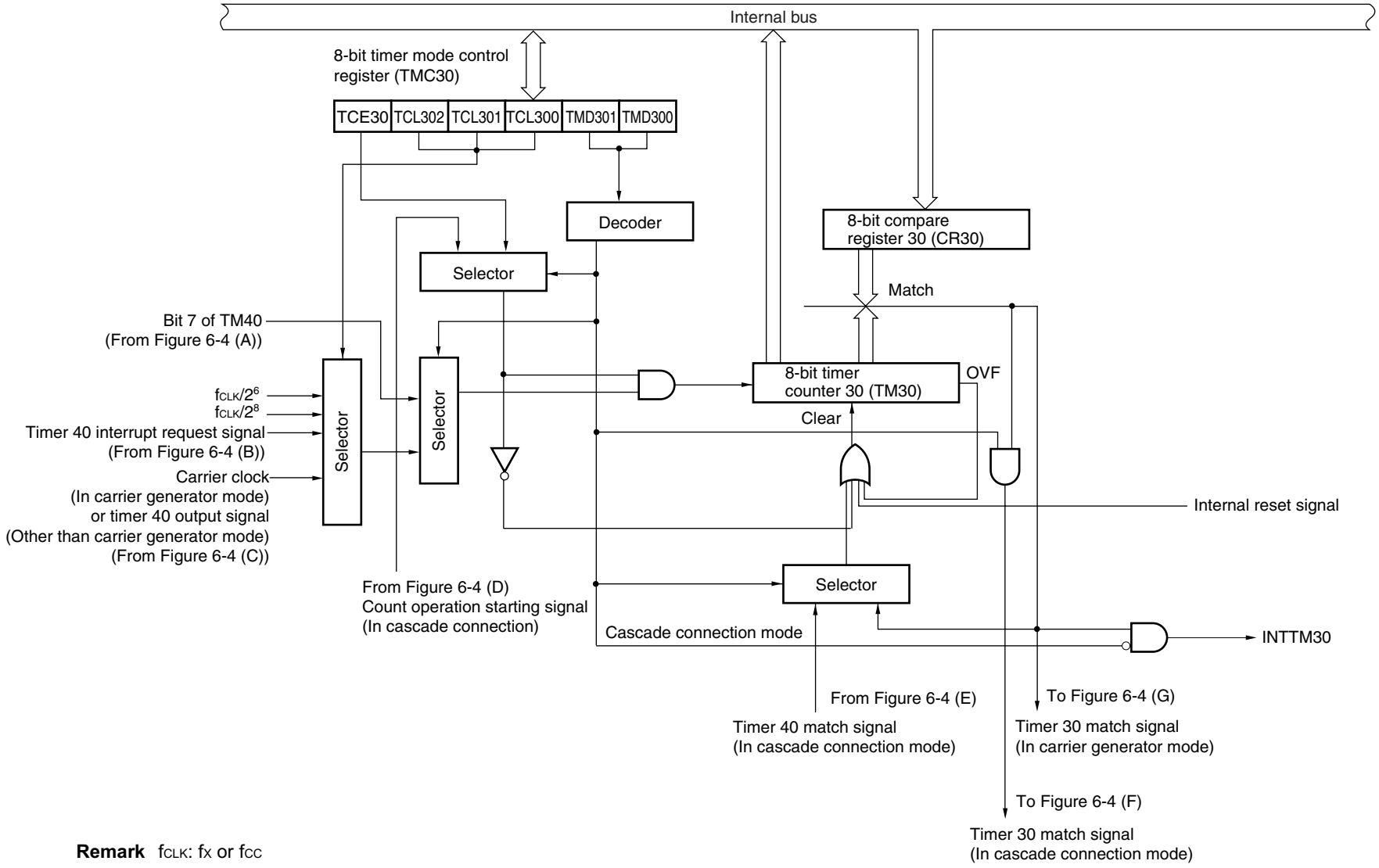
Three channels of timers are incorporated.

- 8-bit timer: 2 channels
- Watchdog timer: 1 channel

Table 6-2. Timer Operation

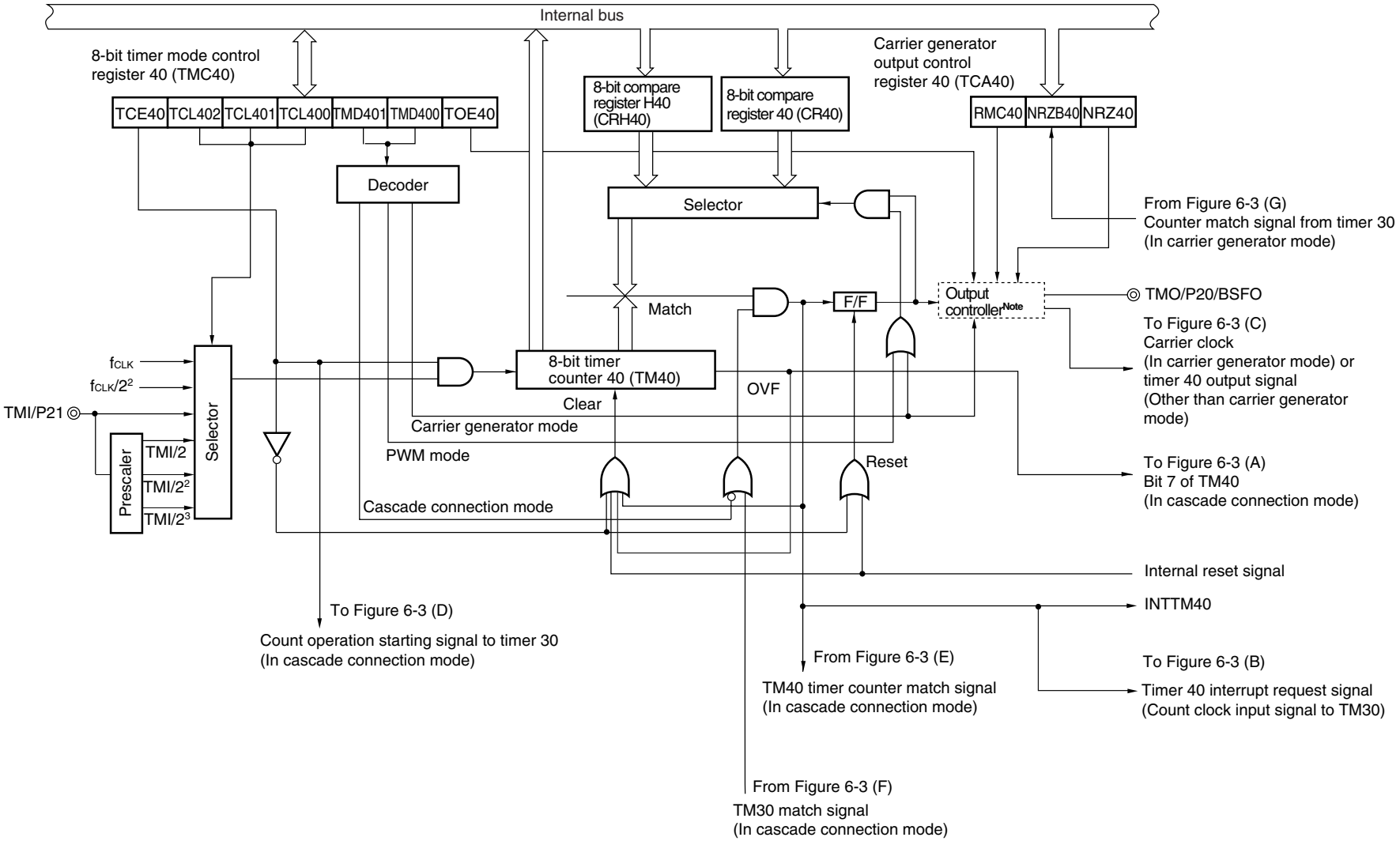
		8-Bit Timer 30	8-Bit Timer 40	Watchdog Timer
Operating mode	Interval timer	1 channel	1 channel	1 channel
	External event counter	–	1 channel	–
Function	Timer output	–	1 output	–
	Square wave output	–	1 output	–
	PWM output	–	1 output	–
	Interrupt request	1	1	1

Figure 6-3. 8-Bit Timer 30 Block Diagram



Remark f_{CLK}: fx or f_{CC}

Figure 6-4. 8-Bit Timer 40 Block Diagram



Note For details, refer to Figure 6-5.

Remark f_{CLK}: fx or f_{CC}

Figure 6-5. Block Diagram of Output Controller (Timer 40)

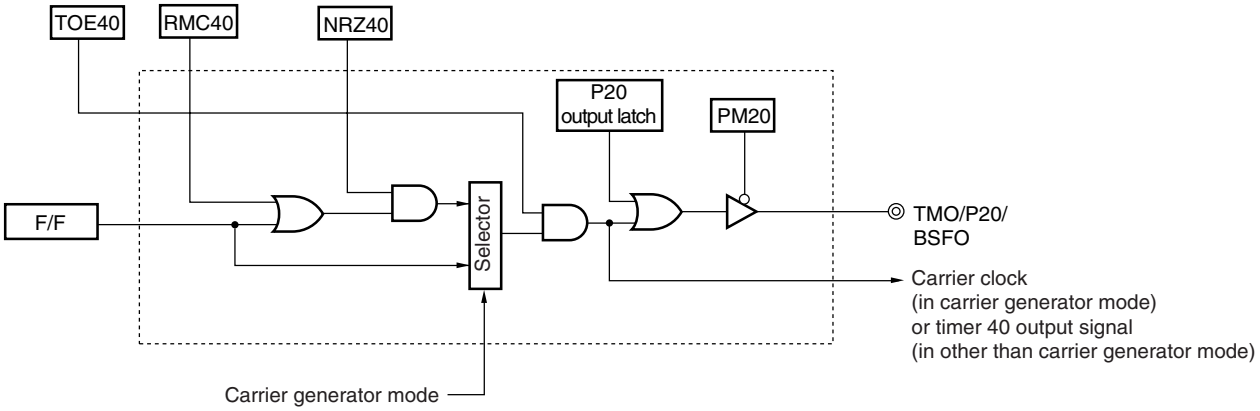
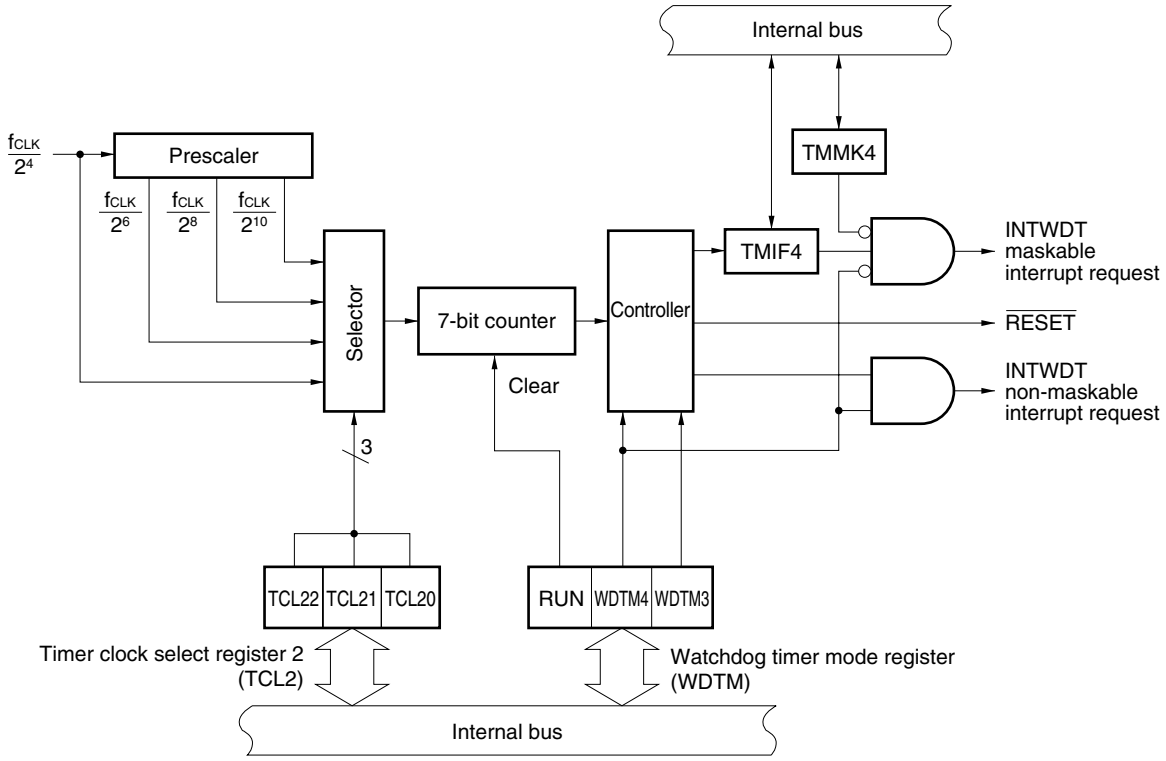


Figure 6-6. Watchdog Timer Block Diagram



Remark f_{CLK}: f_X or f_{CC}

6.4 Power-On-Clear Circuits

The power-on-clear circuits include the following two circuits, which have the following functions.

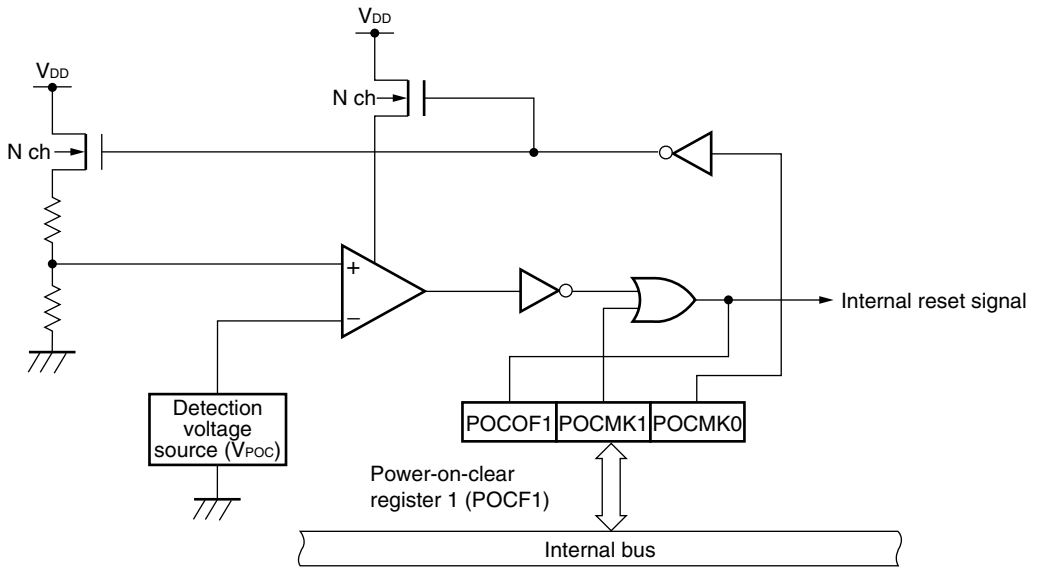
(1) Power-on-clear (POC) circuit

- Compares the detection voltage (V_{POC}) with the power supply voltage (V_{DD}) and generates an internal reset signal if $V_{DD} < V_{POC}$.
- By using a mask option, it is possible to select a POC switching circuit, normally operating circuit, or normally halted circuit. When a POC switching circuit is selected, POC operation can be controlled by software (refer to **10 MASK OPTIONS**).
- This circuit can operate even in STOP mode.

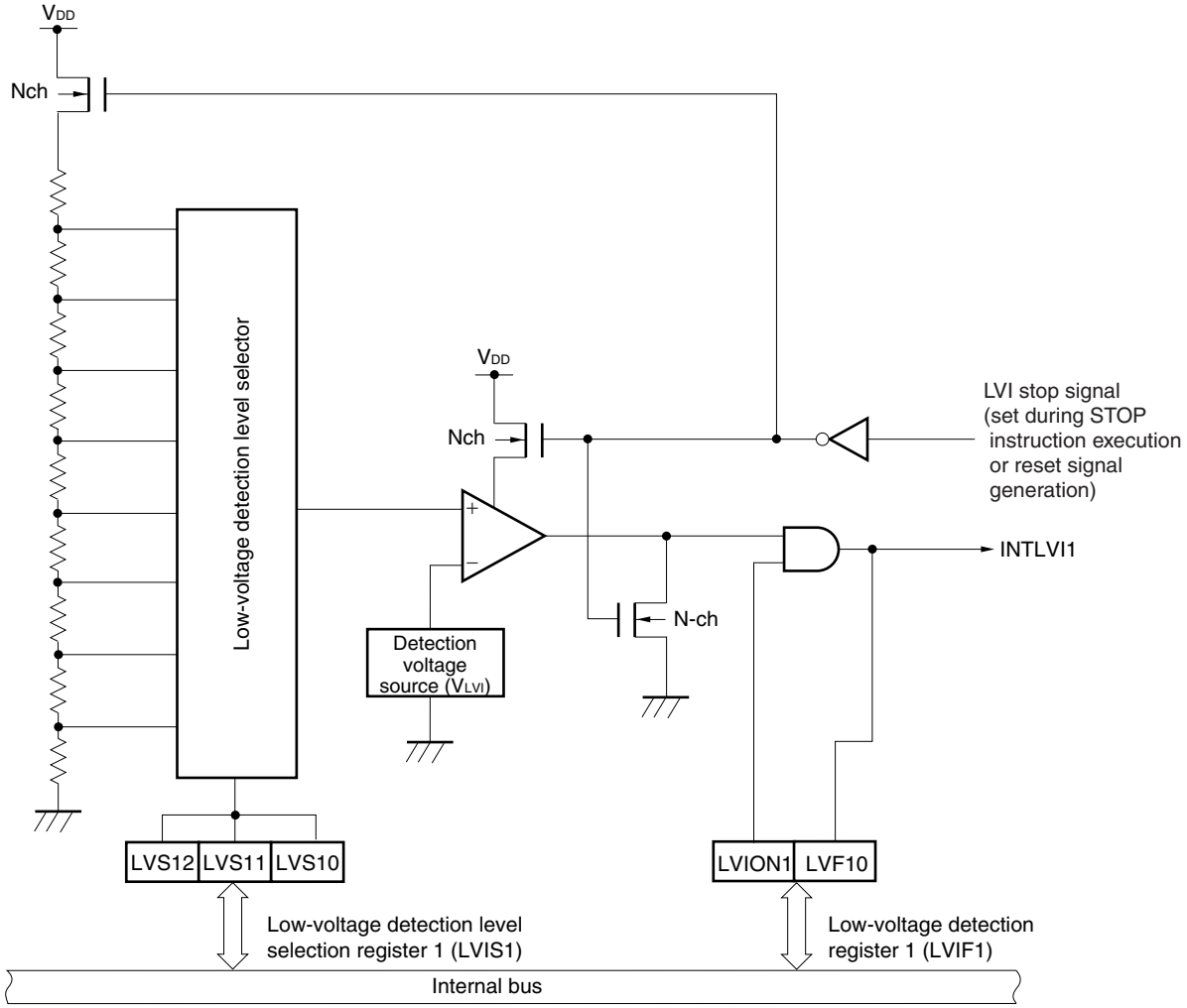
(2) Low-voltage detection (LVI) circuit

- Compares the detection voltage (V_{LVI}) to the power supply voltage (V_{DD}) and generates an interrupt request signal (INTLVI) if $V_{DD} < V_{LVI}$.
- Eight levels of detection voltage can be selected using software.
- This circuit stops operation in STOP mode.

Figure 6-7. Power-On-Clear Circuit Block Diagram



★ **Figure 6-8. Low-Voltage Detection Circuit Block Diagram**

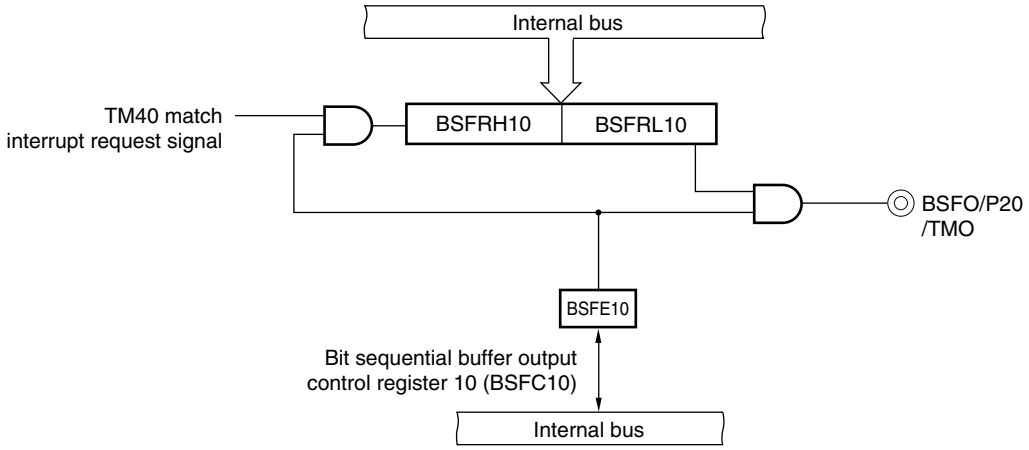


6.5 Bit Sequential Buffer

The μPD789860 and μPD789861 have an on-chip bit sequential buffer of 8 bits × 8 bits = 16 bits.
The functions of the bit sequential buffer are shown below.

- If the value of the bit sequential buffer 10 data register (BSFRL10, BSFRH10) is shifted 1 bit to the lower side, the LSB can be output to the port at the same time.
- It is possible to write to BSFRL10 and BSFRH10 using an 8-bit or 16-bit manipulation instruction.
- Overwriting is enabled during a shift operation on the higher 8 bits only (the period in which shift clock is low level).

Figure 6-9. Bit Sequential Buffer Block Diagram

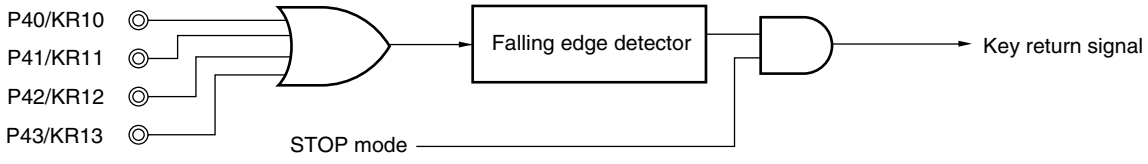


6.6 Key Return Circuit

In STOP mode, this circuit generates a key return interrupt by inputting a P40/KR10 to P43/KR13 falling edge.
It can be used in judging the cause of a STOP mode release in software.

Caution The key return interrupt is a non-maskable interrupt that is in effect only in STOP mode. In addition, P40/KR10 to P43/KR13 key input cannot be controlled by the mask options.

Figure 6-10. Key Return Circuit Block Diagram



7. INTERRUPT FUNCTIONS

7.1 Types of Interrupt Functions

The following two kinds of interrupt functions are available.

(1) Non-maskable interrupts

A non-maskable interrupt is an interrupt that is accepted unconditionally even in a state in which interrupts are disabled. In addition, it is not subject to interrupt priority control and has a greater priority than all other interrupt requests.

A non-maskable interrupt generates a standby release signal.

Non-maskable interrupts have one internal interrupt source and one external interrupt source.

(2) Maskable interrupts

A maskable interrupt is an interrupt that is mask controlled. The order of priority when multiple interrupt requests are generated at the same time is determined as shown in Table 7-1.

A maskable interrupt generates a standby release signal.

Maskable interrupts have 5 internal interrupt sources.

7.2 Sources and Configuration of Interrupts

There are a total of seven sources of interrupts for non-maskable interrupts and maskable interrupts combined (see Table 7-1).

Table 7-1. List of Interrupt Sources

Interrupt Type	Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	–	INTKR1	Key return input falling edge detected	External	0002H	(A)
		INTWDT	Watchdog timer overflow (watchdog timer mode 1 selected)	Internal	0004H	
Maskable	0	INTWDT	Watchdog timer overflow (interval timer mode selected)			(B)
	1	INTTM30	8-bit timer 30 match signal generation		0006H	
	2	INTTM40	8-bit timer 40 match signal generation		0008H	
	3	INTLVI1	LVI interrupt request signal		000AH	
	4	INTEE0	EEPROM write termination signal		000CH	

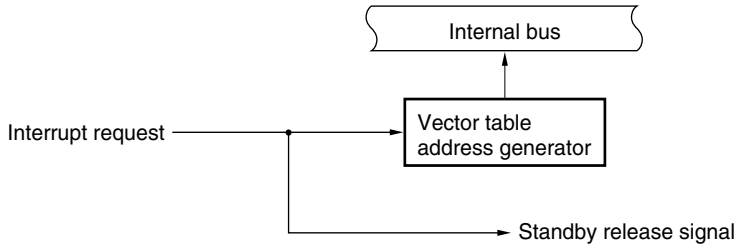
Notes 1. Priority is the priority order when several maskable interrupts are generated at the same time. 0 is the highest order and 4 is the lowest.

2. (A) and (B) in Basic Configuration Type above correspond to (A) and (B) in Figure 7-1.

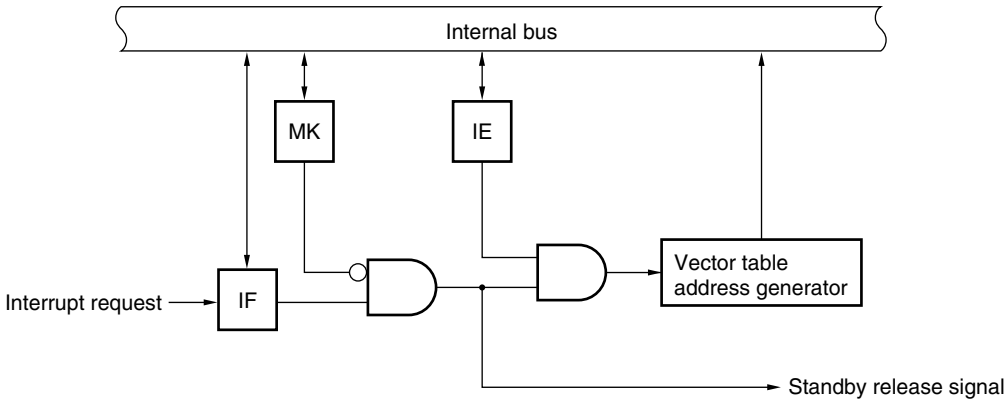
Remark Non-maskable and maskable interrupts (internal) are available as the watchdog timer interrupt sources (INTWDT), and either one can be selected.

Figure 7-1. Basic Configuration of Interrupt Functions

(A) External/internal non-maskable interrupt



(B) Internal maskable interrupt



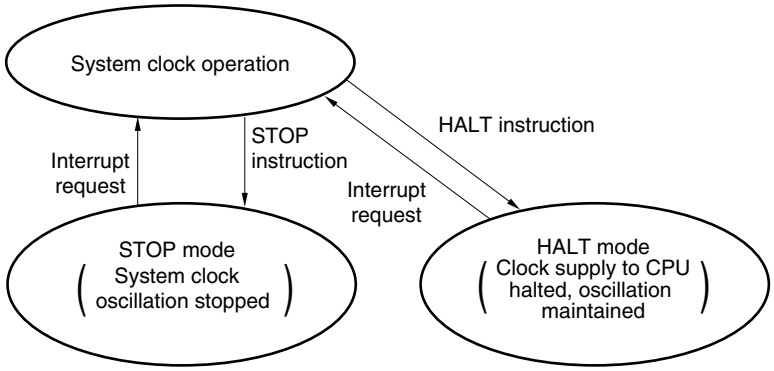
IF: Interrupt request flag
IE: Interrupt enable flag
MK: Interrupt mask flag

8. STANDBY FUNCTION

The following two standby modes are available for further reduction of system current consumption.

- HALT mode: In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation.
- STOP mode: In this mode, oscillation of the system clock is stopped. All operations performed on the system clock are suspended resulting in extremely small power consumption.

Figure 8-1. Standby Function



9. RESET FUNCTION

The following three reset methods are available.

- External reset by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer program loop time detection
- Internal reset by the POC circuit according to comparison of the detection voltage to the power supply voltage

10. MASK OPTIONS

The μPD789860 and μPD789861 have the following mask options.

- P40 to P43 mask options
  On-chip pull-up resistors can be selected.
  <1> Specify on-chip pull-up resistors in bit units
  <2> Do not specify on-chip pull-up resistors

- POC circuit mask options
  The POC circuit can be selected.
  <1> Select POC switching circuit (POC circuit operation control by software is possible)
  <2> Select POC circuit normally operating
  <3> Select POC circuit normally halted

- Oscillation stabilization wait time (μPD789860 only)
  The oscillation stabilization wait time after the release of STOP mode by $\overline{\text{RESET}}$ or the release of reset by POC can be selected.
  <1> 2^{15}/fx
  <2> 2^{17}/fx

★ **Caution The oscillation stabilization wait time of the μPD789861 is fixed to 2^7/fCC.**

11. INSTRUCTION SET SUMMARY

This section lists the μPD789860 and μPD789861 instruction set.

11.1 Conventions

11.1.1 Operand identifiers and description methods

Operands are described in “Operand” column of each instruction in accordance with the description method of the instruction operand identifier (refer to the assembler specifications for details). When there are two or more description methods, select one of them. Alphabetic letters in capitals and the symbols #, !, $, and [ ] are key words and must be described as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: Absolute address specification
- $: Relative address specification
- [ ]: Indirect address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to describe the #, !, $, and [ ] symbols.

For operand register identifiers, r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for description.

Table 11-1. Operand Identifiers Forms and Description Methods

Identifier	Description Method
r	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7)
rp	AX (RP0), BC (RP1), DE (RP2), HL (RP3)
sfr	Special function register symbol
saddr	FE20H to FF1FH immediate data or label
saddrp	FE20H to FF1FH immediate data or label (Even numbered addresses only)
addr16	0000H to FFFFH immediate data or label
	(Even numbered addresses only if a 16-bit data transfer instruction)
addr5	0040H to 007FH immediate data or label (Even numbered addresses only)
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit	3-bit immediate data or label

11.1.2 Explanation of operation column

A: A register; 8-bit accumulator
X: X register
B: B register
C: C register
D: D register
E: E register
H: H register
L: L register
AX: AX register pair; 16-bit accumulator
BC: BC register pair
DE: DE register pair
HL: HL register pair
PC: Program counter
SP: Stack pointer
PSW: Program status word
CY: Carry flag
AC: Auxiliary carry flag
Z: Zero flag
IE: Interrupt request enable flag
NMIS: Non-maskable interrupt processing flag
( ): Contents of memory represented by contents of register or address in parentheses
X_H, X_L: Higher 8 bits and lower 8 bits of 16-bit register
∧: Logical product (AND)
∨: Logical sum (OR)
∨̸: Exclusive logical sum (exclusive OR)
$\overline{\quad}$: Inverted data
addr16: 16-bit immediate data or label
jdisp8: Signed 8-bit data (displacement value)

11.1.3 Explanation of flags column

(blank): No change
0: Cleared to 0
1: Set to 1
×: Set or cleared according to result
R: Previously stored value is stored

11.2 List of Operations

Mnemonic	Operand	Bytes	Clock	Operation	Flags
					Z AC CY
MOV	r. #byte	3	6	r ← byte	
	saddr, #byte	3	6	(saddr) ← byte	
	sfr, #byte	3	6	sfr ← byte	
	A, r[Note 1]	2	4	A ← r	
	r, A[Note 1]	2	4	r ← A	
	A, saddr	2	4	A ← (saddr)	
	saddr, A	2	4	(saddr) ← A	
	A, sfr	2	4	A ← sfr	
	sfr, A	2	4	sfr ← A	
	A, !addr16	3	8	A ← (addr16)	
	!addr16, A	3	8	(addr16) ← A	
	PSW, #byte	3	6	PSW ← byte	× × ×
	A, PSW	2	4	A ← PSW	
	PSW, A	2	4	PSW ← A	× × ×
	A, [DE]	1	6	A ← (DE)	
	[DE], A	1	6	(DE) ← A	
	A, [HL]	1	6	A ← (HL)	
	[HL], A	1	6	(HL) ← A	
	A, [HL + byte]	2	6	A ← (HL + byte)	
	[HL + byte], A	2	6	(HL + byte) ← A	
XCH	A, X	1	4	A ←→ X	
	A, r[Note 2]	2	6	A ←→ r	
	A, saddr	2	6	A ←→ (saddr)	
	A, sfr	2	6	A ←→ (sfr)	
	A, [DE]	1	8	A ←→ (DE)	
	A, [HL]	1	8	A ←→ (HL)	
	A, [HL + byte]	2	8	A ←→ (HL+byte)	
MOVW	rp, #word	3	6	rp ← word	
	AX, saddrp	2	6	AX ← (saddrp)	
	saddrp, AX	2	8	(saddrp) ← AX	
	AX, rp[Note 3]	1	4	AX ← rp	
	rp, AX[Note 3]	1	4	rp ← AX	

Notes 1. Excludes r = A

2. Excludes r = A, X

3. rp = BC, DE, HL only

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
XCHW	AX, rp[Note]	1	8	AX ←→ rp			
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A+ (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A+ (addr16) +CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A+ (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A – byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r	2	4	A, CY ← A – r	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte)	×	×	×
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r	2	4	A, CY ← A – r – CY	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte) – CY	×	×	×

Note rp = BC, DE, HL only

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	×		
OR	A, #byte	2	4	A ← A ∨ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∨ byte	×		
	A, r	2	4	A ← A ∨ r	×		
	A, saddr	2	4	A ← A ∨ (saddr)	×		
	A, !addr16	3	8	A ← A ∨ (addr16)	×		
	A, [HL]	1	6	A ← A ∨ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∨ (HL + byte)	×		
XOR	A, #byte	2	4	A ← A ⊻ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ⊻ byte	×		
	A, r	2	4	A ← A ⊻ r	×		
	A, saddr	2	4	A ← A ⊻ (saddr)	×		
	A, !addr16	3	8	A ← A ⊻ (addr16)	×		
	A, [HL]	1	6	A ← A ⊻ (HL)	×		
	A, [HL + byte]	2	6	A ← A ⊻ (HL + byte)	×		
CMP	A, #byte	2	4	A – byte	×	×	×
	saddr, #byte	3	6	(saddr) – byte	×	×	×
	A, r	2	4	A – r	×	×	×
	A, saddr	2	4	A – (saddr)	×	×	×
	A, !addr16	3	8	A – (addr16)	×	×	×
	A, [HL]	1	6	A – (HL)	×	×	×
	A, [HL + byte]	2	6	A – (HL + byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY ← AX + word	×	×	×
SUBW	AX, #word	3	6	AX, CY ← AX – word	×	×	×
CMPW	AX, #word	3	6	AX – word	×	×	×
INC	r	2	4	r ← r + 1	×	×	
	saddr	2	4	(saddr) ← (saddr) + 1	×	×	
DEC	r	2	4	r ← r– 1	×	×	
	saddr	2	4	(saddr) ← (saddr) – 1	×	×	

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
INCW	rp	1	4	rp ← rp + 1			
DECW	rp	1	4	rp ← rp – 1			
ROR	A, 1	1	2	(CY, A_7 ← A_0, A_{m-1} ← A_m) × 1			×
ROL	A, 1	1	2	(CY, A_0 ← A_7, A_{m+1} ← A_m) × 1			×
RORC	A, 1	1	2	(CY ← A_0, A_7 ← CY, A_{m-1} ← A_m) × 1			×
ROLC	A, 1	1	2	(CY ← A_7, A_0 ← CY, A_{m+1} ← A_m) × 1			×
SET1	saddr. bit	3	6	(saddr. bit) ← 1			
	sfr. bit	3	6	sfr. bit ← 1			
	A. bit	2	4	A. bit ← 1			
	PSW. bit	3	6	PSW. bit ← 1	×	×	×
	[HL]. bit	2	10	(HL). bit ← 1			
CLR1	saddr. bit	3	6	(saddr. bit) ← 0			
	sfr. bit	3	6	sfr. bit ← 0			
	A. bit	2	4	A. bit ← 0			
	PSW. bit	3	6	PSW. bit ← 0	×	×	×
	[HL]. bit	2	10	(HL). bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{CY}$			×
CALL	!addr16	3	6	(SP – 1) ← (PC + 3)$_H$, (SP – 2) ← (PC + 3)$_L$, PC ← addr16, SP ←SP – 2			
CALLT	[addr5]	1	8	(SP – 1) ← (PC + 1)$_H$, (SP – 2) ← (PC + 1)$_L$, PC_H ← (00000000, addr5 + 1) PC_L ← (00000000, addr5) SP ← SP – 2			
RET		1	6	PC_H ← (SP + 1), PC_L ← (SP), SP ← SP + 2			
RETI		1	8	PC_H ← (SP + 1), PC_L ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R	R	R
PUSH	PSW	1	2	(SP – 1) ← PSW, SP ← SP – 1			
	rp	1	4	(SP – 1) ← rp_H, (SP – 2) ← rp_L, SP ← SP – 2			
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R	R	R
	rp	1	6	rp_H ← (SP + 1), rp_L ← (SP), SP ← SP + 2			
MOVW	SP, AX	2	8	SP ← AX			
	AX, SP	2	6	AX ← SP			

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags
					Z AC CY
BR	!addr16	3	6	PC ← addr16	
	$addr16	2	6	PC ← PC + 2 + jdisp8	
	AX	1	6	PC_H ← A, PC_L ← X	
BC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 1	
BNC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 0	
BZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 1	
BNZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 0	
BT	saddr, bit, $saddr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 1	
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 1	
	A. bit, $saddr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 1	
	PSW. bit $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 1	
BF	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 0	
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 0	
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 0	
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 0	
DBNZ	B, $addr16	2	6	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0	
	C, $addr16	2	6	C ← C – 1, then PC ← PC + 2 + jdisp8 if C ≠ 0	
	saddr, $addr16	3	8	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0	
NOP		1	2	No Operation	
EI		3	6	IE ← 1 (Enable Interrupt)	
DI		3	6	IE ← 0 (Disable Interrupt)	
HALT		1	2	Set HALT Mode	
STOP		1	2	Set Stop Mode	

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

12. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +6.5	V
Input voltage	V_I		–0.3 to V_{DD} + 0.3	V
Output voltage	V_O		–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	–10	mA
		Total of all pins	–30	mA
Output current, low	I_{OL}	Per pin	30	mA
		Total of all pins	80	mA
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–40 to +125	°C

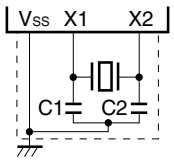
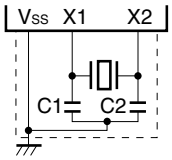
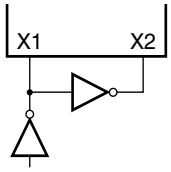
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

System Clock Oscillator Characteristics

Ceramic or crystal oscillation (μPD789860)

(T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note 1]	V_{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)[Note 1]		1.0		5.0	MHz
		Oscillation stabilization time[Note 2]				30	ms
External clock		X1 input frequency (f_X)[Note 1]		1.0		5.0	MHz
		X1 input high-/low-level width(t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

Caution When using a ceramic or crystal oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

★ **Recommended Oscillator Constant**

Ceramic Resonator (T_A = –40 to +85°C)

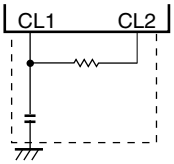
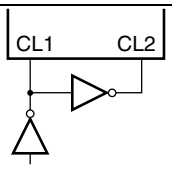
Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant (pF)		Oscillation Voltage Range (V_{DD})		Remark
			C1	C2	MIN.	MAX.	
Murata Mfg. Co., Ltd.	CSBLA1M00J58-B0 (CSB1000J)	1.0	100	100	2.1	3.6	
	CSBFB1M00J58-B0 (CSBF1000J)		100	100	2.1	3.6	
	CSTLS2M00G56-B0	2.0	–	–	1.8	3.6	On-chip capacitor
	CSTCC2M00G56-B0 (CSTCC2.00MG0H6)		–	–	1.8	3.6	On-chip capacitor
	CSTLS4M00G53-B0 (CSTS0400MG03)	4.0	–	–	1.8	3.6	On-chip capacitor
	CSTCR4M00G53-R0		–	–	1.8	3.6	On-chip capacitor
	CSTLS4M19G53-B0 (CSTS0419MG03)	4.19	–	–	1.8	3.6	On-chip capacitor
	CSTCR4M19G53-R0		–	–	1.8	3.6	On-chip capacitor
	CSTLS4M91G53-B0 (CSTS0491MG03)	4.91	–	–	1.9	3.6	On-chip capacitor
	CSTCR4M91G53-R0		–	–	1.8	3.6	On-chip capacitor
	CSTLS5M00G53-B0 (CSTS0500MG03)	5.0	–	–	1.9	3.6	On-chip capacitor
	CSTCR5M00G53-R0		–	–	1.8	3.6	On-chip capacitor

Caution The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. Oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation must be adjusted on the implementation circuit. For details, please contact directly the manufacturer of the resonator you will use.

Remark Part numbers in the parentheses indicate old part numbers.

RC oscillation (μPD789861)

(T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
★ RC resonator		Oscillation frequency (f_{CC})Notes 1,2,3	V_{DD} = Oscillation voltage range	0.85	1.0	1.15	MHz
External clock		CL1 input frequency (f_{CC})Note 1		1.0		5.0	MHz
		CL1 input high-/low-level width (t_{XH},t_{XL})		85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

3. Variations in external resistance and external capacitance are not included.

Caution When using an RC oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)

	Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
	Output current, low	I_{OL}	Per pin				2.0	mA
			All pins				5.0	mA
	Output current, high	I_{OH}	Per pin				–0.5	mA
			All pins				–5.0	mA
	Input voltage, high	V_{IH1}	P00 to P07	$2.7 \le V_{DD} < 3.6$	$0.7V_{DD}$		V_{DD}	V
				$1.8 \le V_{DD} < 2.7$	$0.9V_{DD}$		V_{DD}	V
		V_{IH2}	$\overline{\text{RESET}}$, P20, P21, P40 to P43	$2.7 \le V_{DD} < 3.6$	$0.8V_{DD}$		V_{DD}	V
				$1.8 \le V_{DD} < 2.7$	$0.9V_{DD}$		V_{DD}	V
		V_{IH3}	X1 (CL1), X2 (CL2)		V_{DD} – 0.1		V_{DD}	V
	Input voltage, low	V_{IL1}	P00 to P07	$2.7 \le V_{DD} < 3.6$	0		$0.3V_{DD}$	V
				$1.8 \le V_{DD} < 2.7$	0		$0.1V_{DD}$	V
		V_{IL2}	$\overline{\text{RESET}}$, P20, P21, P40 to P43	$2.7 \le V_{DD} < 3.6$	0		$0.2V_{DD}$	V
				$1.8 \le V_{DD} < 2.7$	0		$0.1V_{DD}$	V
★		V_{IL3}	X1 (CL1), X2 (CL2)		0		0.1	V
	Output voltage, high	V_{OH1}	P00 to P07, P20, P21	I_{OH} = –100 μA	V_{DD} – 0.5			V
		V_{OH2}		I_{OH} = –500 μA	V_{DD} – 0.7			V
	Output voltage, low	V_{OL1}	P00 to P07, P20, P21	I_{OL} = 400 μA			0.5	V
		V_{OL2}		I_{OL} = 2.5 mA			0.7	V
★	Input leakage current, high	I_{LIH1}	P00 to P07, P20, P21, P40 to P43, $\overline{\text{RESET}}$	$V_{IN} = V_{DD}$			3	μA
		I_{LIH2}	X1 (CL1), X2 (CL2)				20	μA
★	Input leakage current, low	I_{LIL1}	P00 to P07, P20, P21, P40 to P43, $\overline{\text{RESET}}$	V_{IN} = 0 V			–3	μA
		I_{LIL2}	X1 (CL1), X2 (CL2)				–20	μA
	Output leakage current, high	I_{LOH}	P00 to P07, P20, P21	$V_{OUT} = V_{DD}$			3	μA
	Output leakage current, low	I_{LOL}	P00 to P07, P20, P21	V_{OUT} = 0 V			–3	μA
★	Mask-option pull-up resistor	R	V_{IN} = 0 V, P40 to P43		50	100	200	kΩ

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

2. Items in parentheses apply to the μPD789861.

★ **DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current[Note] Ceramic/crystal oscillation: μPD789860	I_{DD1}	5.0 MHz Crystal oscillation operating mode (EEPROM halted) $C_1 = C_2$ = 22 pF	V_{DD} = 3.0 V ±10%		0.5	1.0	mA
	I_{DD2}	5.0 MHz Crystal oscillation operating mode (EEPROM operating) $C_1 = C_2$ = 22 pF	V_{DD} = 3.0 V ±10%		0.8	1.6	mA
	I_{DD3}	5.0 MHz Crystal oscillation HALT mode (EEPROM halted) $C_1 = C_2$ = 22 pF	V_{DD} = 3.0 V ±10%		0.25	0.6	mA
	I_{DD4}	STOP mode (POC operating)	V_{DD} = 3.0 V ±10%		1.0	2.5	μA
			V_{DD} = 3.0 V ±10% T_A = –20 to +75°C		1.0	1.5	μA
	I_{DD5}	STOP mode (POC operation halted)	V_{DD} = 3.0 V ±10%			0.7	μA
RC oscillation: μPD789861	I_{DD1}	1.0 MHz RC oscillation operating mode (EEPROM halted) R = 24 kΩ, C = 30 pF	V_{DD} = 3.0 V ±10%		0.3	0.8	mA
	I_{DD2}	1.0 MHz RC oscillation operating mode (EEPROM operating) R = 24 kΩ, C = 30 pF	V_{DD} = 3.0 V ±10%		0.5	1.0	mA
	I_{DD3}	1.0 MHz RC oscillation HALT mode (EEPROM halted) R = 24 kΩ, C = 30 pF	V_{DD} = 3.0 V ±10%		0.25	0.6	mA
	I_{DD4}	STOP mode (POC operating)	V_{DD} = 3.0 V ±10%		1.0	2.5	μA
			V_{DD} = 3.0 V ±10% T_A = –20 to +75°C		1.0	1.5	μA
	I_{DD5}	STOP mode (POC operation halted)	V_{DD} = 3.0 V ±10%			0.7	μA

Note Port current (including current flowing in on-chip pull-up resistors) is not included.

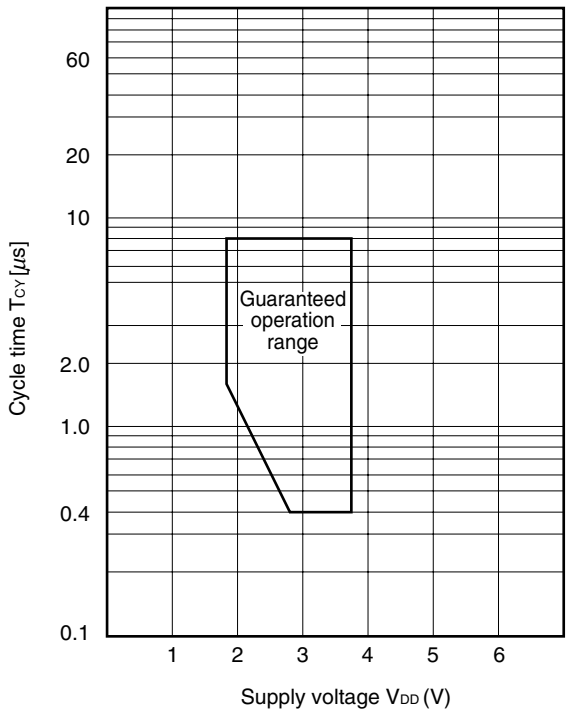
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

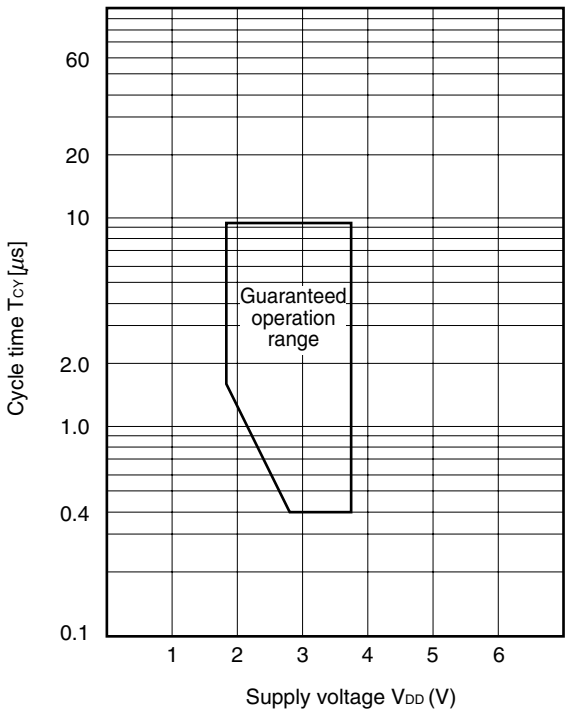
(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (Minimum instruction execution time) Ceramic/crystal oscillation	T_{CY1}	$2.7 \le V_{DD} \le 3.6$	0.4		8	μs
		$1.8 \le V_{DD} < 2.7$	1.6		8	μs
★ Cycle time (Minimum instruction execution time) RC oscillation	T_{CY2}	$2.7 \le V_{DD} \le 3.6$	0.4		9.42	μs
		$1.8 \le V_{DD} < 2.7$	1.6		9.42	μs
TMI input Input frequency	f_{TI}	$2.7 \le V_{DD} \le 3.6$	0		4.0	MHz
		$1.8 \le V_{DD} < 2.7$	0		500	kHz
TMI High-/low-level width	f_{TIH}, f_{TIL}	$2.7 \le V_{DD} \le 3.6$	0.1			μs
		$1.8 \le V_{DD} < 2.7$	1.0			μs
Key return input pin Low-level width	t_{KRIL}	KR10 to KR13	10			μs
$\overline{\text{RESET}}$ Low-level width	t_{RST}		10			μs

★ **T_{CY1} vs. V_{DD} (System Clock: Ceramic/Crystal Oscillation)**



T_{CY2} vs. V_{DD} (System Clock: RC Oscillation)

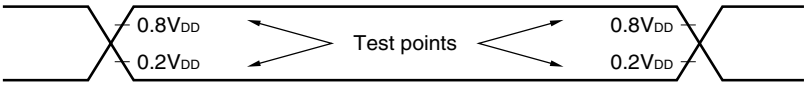


(2) RC frequency oscillation characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)

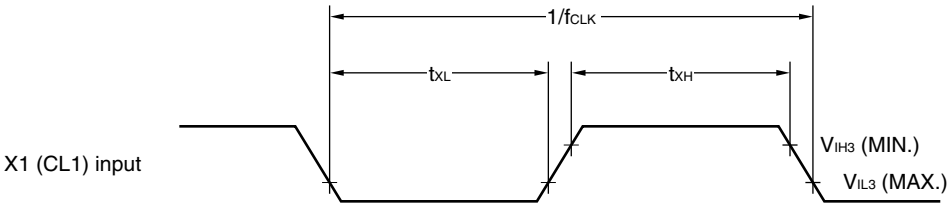
	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★	Oscillation frequency[Note]	f_{CC}	R = 24 kΩ, C = 30 pF	0.85		1.15	MHz

Note Does not include variations due to external resistance and external capacitance

AC Timing Test Points (excluding X1 and CL1 inputs)

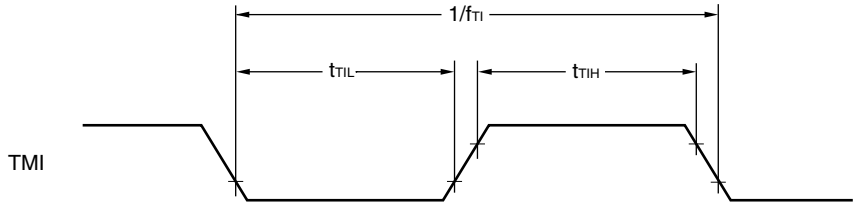


Clock Timing

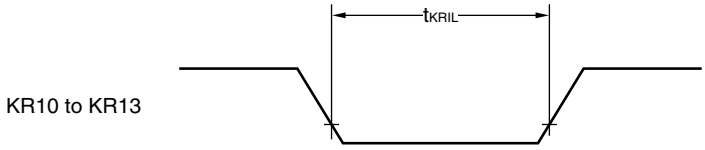


Remark f_{CLK}: fx or f_{CC}

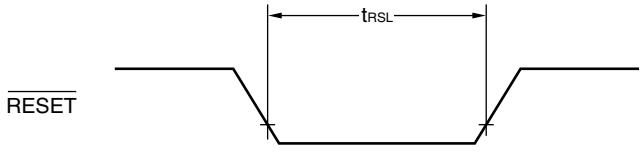
TMI Timing



Key Return Input Timing



$\overline{\text{RESET}}$ Input Timing



Power-On-Clear Circuit Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)

(1) POC

(a) DC characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POC}	Response time[Note]: 2 ms	1.8	1.9	2.0	V

Note Time from detecting voltage until output reverses and time until stable operation after transition from halted state to operating state

(b) AC characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power rise time	V_{Pth1}	POC switching circuit used	V_{DD}: 0 → 1.8 V	0.01		100	ms
	V_{Pth2}	POC normally operating	V_{DD}: 0 → 1.8 V	0.01		100	ms
★	V_{Pth3}	POC normally operating	V_{DD}: 0 → 1.8 V T_A = +25°C	10			μs

(2) LVI

(a) DC characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LVI7 detection voltage	V_{LVI7}	Response time[Note 1]: 2 ms	2.4	2.6	2.8	V
LVI6 detection voltage	V_{LVI6}	Response time[Note 1]: 2 ms		**Note 2**		V
LVI5 detection voltage	V_{LVI5}	Response time[Note 1]: 2 ms		**Note 2**		V
LVI4 detection voltage	V_{LVI4}	Response time[Note 1]: 2 ms		**Note 2**		V
LVI3 detection voltage	V_{LVI3}	Response time[Note 1]: 2 ms		**Note 2**		V
LVI2 detection voltage	V_{LVI2}	Response time[Note 1]: 2 ms		**Note 2**		V
LVI1 detection voltage	V_{LVI1}	Response time[Note 1]: 2 ms		**Note 2**		V
LVI0 detection voltage	V_{LVI0}	Response time[Note 1]: 2 ms	**Note 3**	2.0	2.2	V

Notes 1. Time from detecting voltage until output reverses and time until stable operation after transition from halted state to operating state

2. Relativity: $V_{LVI1} < V_{LVI2} < V_{LVI3} < V_{LVI4} < V_{LVI5} < V_{LVI6}$

3. $V_{POC} < V_{LVI0}$

★ **EEPROM Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)**

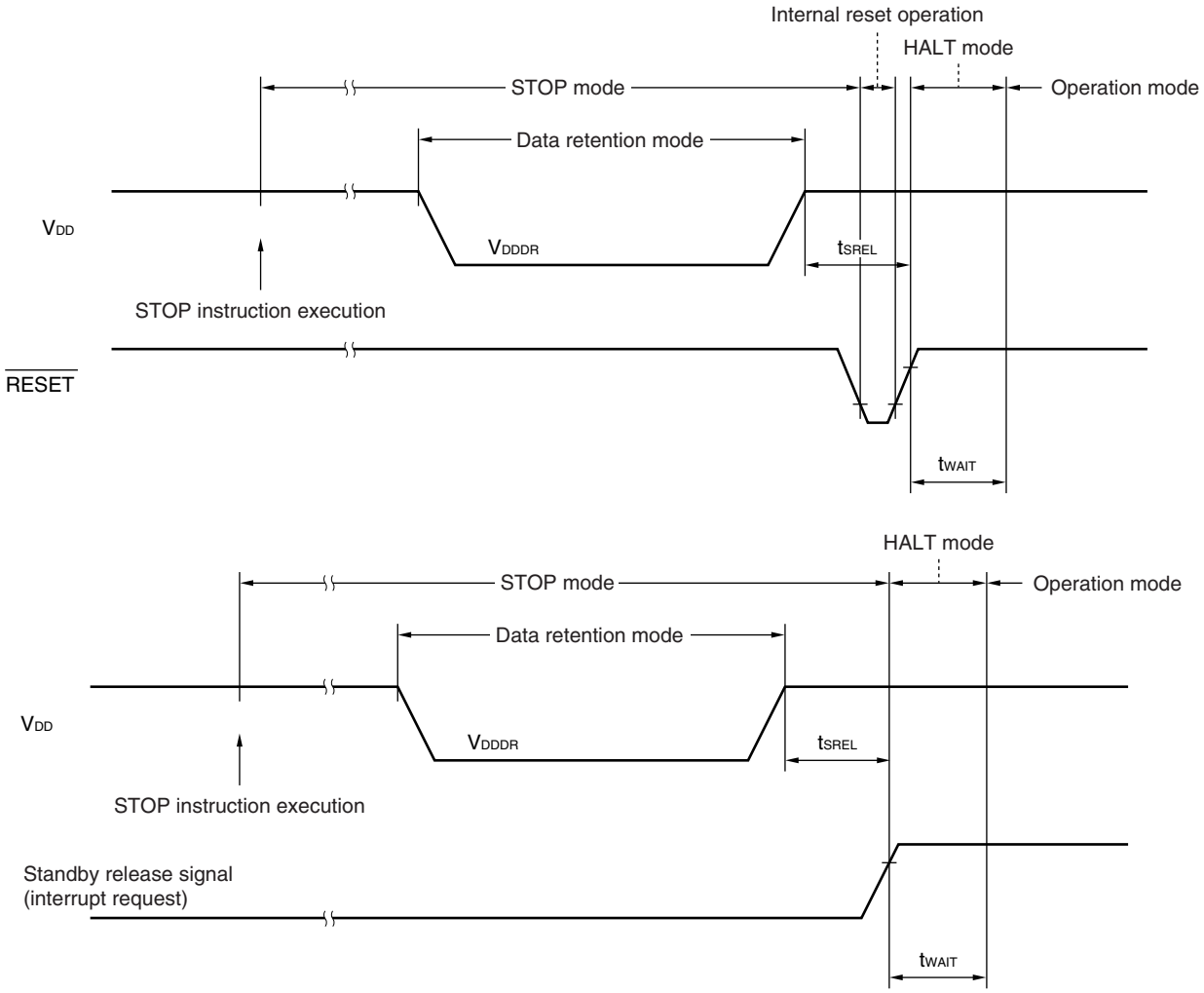
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Write time[Note 1]			3.3		6.6	ms
Number of overwrites		Per byte			10	10,000 times

Note Write time = T × 145 (T = time of 1 clock cycle selected by EWCS100 to EWCS102)

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.8		3.6	V
Release signal set time	t_{SREL}	STOP release by $\overline{\text{RESET}}$ pin	10			μs

★ **Data Retention Timing**



Oscillation Stabilization Wait Time (T_A = –40 to +85°C, V_{DD} = 1.8 to 3.6 V)

(a) Ceramic/crystal oscillation (μPD789860)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation wait time[Note 1]		Stop release by $\overline{\text{RESET}}$ or reset release by POC		**Note 2**		s
		Release by interrupt		**Note 3**		s

Notes 1. Time required to stabilize oscillation after reset or STOP mode release.

2. 2^{15}/fx or 2^{17}/fx can be selected using the mask option.

3. 2^{12}/fx, 2^{15}/fx, or 2^{17}/fx can be selected using bits 0 to 2 of the oscillation stabilization time selection register (OSTS0 to OSTS2).

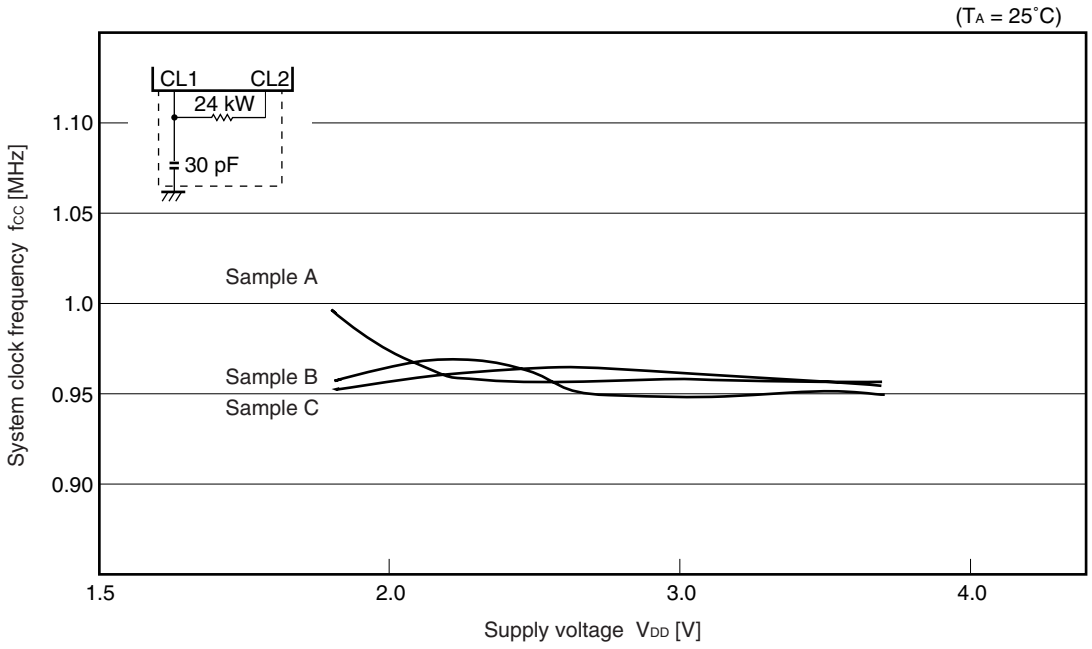
(b) RC oscillation (μPD789861)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation wait time[Note]		STOP release by $\overline{\text{RESET}}$ or reset release by POC		$2^7/f_{CC}$		s
		Release by interrupt		$2^7/f_{CC}$		s

Note Time required to stabilize oscillation after reset or STOP mode release.

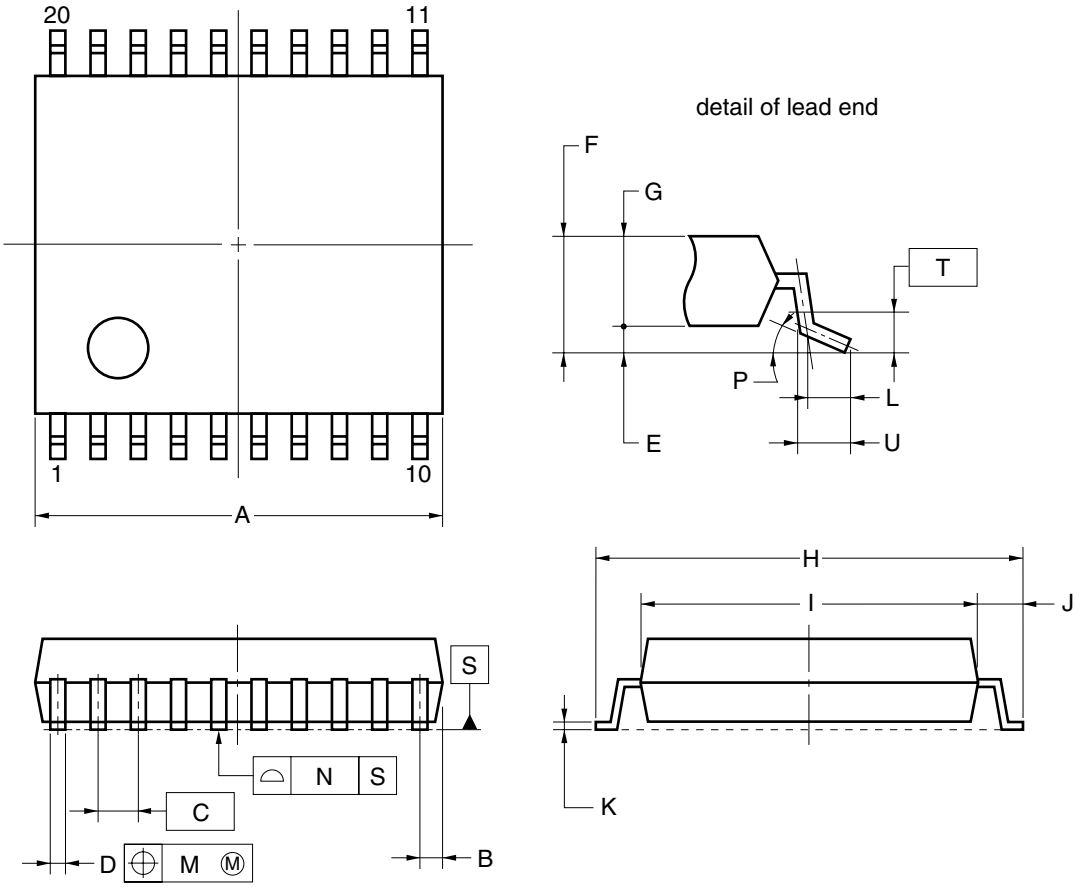
★ 13. EXAMPLE OF RC OSCILLATION FREQUENCY CHARACTERISTICS (REFERENCE VALUES)

F_{CC} vs. V_{DD} (RC Oscillation: μPD789861, R = 24 kΩ, C = 30 pF)



14. PACKAGE DRAWING

20-PIN PLASTIC SSOP (7.62 mm (300))



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	6.65±0.15
B	0.475 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.08}_{-0.07}$
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25
U	0.6±0.15

S20MC-65-5A4-2

★ 15. RECOMMENDED SOLDERING CONDITIONS

The μPD789860 and 789861 should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 15-1. Surface Mounting Type Soldering Conditions

μPD789860MC-×××-5A4: 20-pin plastic SSOP (7.62 mm (300))
μPD789861MC-×××-5A4: 20-pin plastic SSOP (7.62 mm (300))

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: three times or less	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: three times or less	VP15-00-3
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max. Time: 3 seconds max. (per pin row)	—

Caution Do not use different soldering method together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD789860 and μPD789861.

Language Processing Software

RA78K0S[Notes 1,2,3]	Assembler package common to 78K/0S Series
CC78K0S[Notes 1,2,3]	C compiler package common to 78K/0S Series
CC78K0S-L[Notes 1,2,3]	C compiler source file common to 78K/0S Series
DF789861[Notes 1,2,3]	Device file for μPD789860, 789861 Subseries

Flash Memory Writing Tools

Flashpro III (FL-PR3[Note 4], PG-FP3)	Flash programmer dedicated to microcontrollers with on-chip flash memory (EEPROM)
FA-20MC[Note 4]	Flash memory (EEPROM) writing adapter for 20-pin plastic shrink SOP (MC-5A4 type)

Debugging Tools

IE-78K0S-NS In-circuit emulator	This is the in-circuit emulator for debugging hardware and software when developing an application system using the 78K/0S Series. It corresponds to the integrated debugger (ID78K0S-NS). It is used in combination with an AC adapter, emulation probe, and interface adapter for connecting to a host machine.
★ IE-78K0S-NS-A In-circuit emulator	In-circuit emulator with expanded functions of IE-78K0S-NS. The debugging function is enhanced by the addition of a coverage function and the tracer function and timer function are also enhanced.
IE-70000-MC-PS-B AC adapter	This is an adapter for providing power from a 100 to 240 V AC.
IE-70000-98-IF-C Interface adapter	This is an adapter (C bus supported) that is needed when using a PC-9800 series (except a notebook type) as a host machine.
IE-70000-CD-IF-A PC card interface	This is a PC card and interface cable (PCMCIA socket supported) that is needed when using a notebook type as a host machine.
IE-70000-PC-IF-C Interface adapter	This is an adapter (ISA bus supported) that is needed when using an IBM PC/AT™ or compatible as a host machine.
★ IE-70000-PCI-IF-A Interface adapter	This is an adapter that is needed when using a personal computer in which a PCI bus is incorporated as a host machine.
IE-789860-NS-EM1 Emulation board	This is a board for emulating the peripheral hardware of a device. It is used in combination with the in-circuit emulator.
★ NP-20GS[Note 4] Emulation probe	Board for connecting in-circuit emulator and target system. Used in combination with EV-9500GS-20.
EV-9500GS-20 Conversion adapter	Conversion adapter for connecting target system board for mounting 20-pin plastic SSOP and NP-20GS.
SM78K0S[Notes 1,2]	System emulator common to 78K/0S Series
DF789861[Notes 1,2]	Device file for μPD789860, 789861 Subseries

Real-Time OS

MX78K0S[Notes 1,2]	OS for 78K/0S Series

Notes 1. PC-9800 series (Japanese Windows) based

2. IBM PC/AT or compatibles (Japanese/English Windows) based

3. HP9000 series 700™ (HP-UX™) based, SPARCstation™ (SunOS™, Solaris™) based

4. This is a product of Naito Densei Machida Mfg. Co., Ltd. (+81-45-475-4191).

Remark Use this in combination with RA78K0S, CC78K0S, SM78K0S, and DF789861.

APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD789860, 789861 Data Sheet	This manual
μPD78E9860, 78E9861 Preliminary Product Information	U14385E
μPD789860, 789861 Subseries User's Manual	U14826E
78K/0S Series Instructions User's Manual	U11047E

Documents Related to Development Tools (Software) (User's Manuals)

Document Name		Document No.
RA78K0S Assembler Package	Operation	U11622E
	Language	U11599E
	Structured Assembly Language	U11623E
CC78K0S C Compiler	Operation	U11816E
	Language	U11817E
SM78K0S, SM78K0 System Simulator Ver. 2.10 or Later Windows Based	Operation	U14611E
SM78K Series System Simulator Ver. 2.10 or Later	External Part User Open Interface Specification	U15006E
ID78K0S-NS Integrated Debugger Ver. 2.20 or Later Windows Based	Operation	U14910E

Document Related to Development Tools (Hardware) (User's Manuals)

Document Name	Document No.
IE-78K0S-NS In-Circuit Emulator	U13549E
IE-78K0S-NS-A In-Circuit Emulator	U15207E
IE-789860-NS-EM1 Emulation Board	To be prepared

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Other Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE - Products & Packages -	X13769E
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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800-729-9288

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