μPD789121A(A1),122A(A1),124A(A1),131A(A1),132A(A1),134A(A1), 121A(A2),122A(A2),124A(A2),131A(A2),132A(A2),134A(A2)

8-BIT SINGLE-CHIP MICROCONTROLLERS

The μPD789121A(A1), 789122A(A1), 789124A(A1), PD789121A(A2), 789122A(A2), and 789124A(A2) (μPD78912xA(A1), 78912xA(A2) hereafter) are μPD789124A Subseries products of the 78K/0S Series.

The μPD789131A(A1), 789132A(A1), 789134A(A1), PD789131A(A2), 789132A(A2), and 789134A(A2) (μPD78913xA(A1), 78913xA(A2) hereafter) are μPD789134A Subseries products of the 78K/0S Series.

Besides an 8-bit CPU, these microcontrollers incorporate a variety of hardware such as I/O ports, timers, a serial interface, A/D converters, and interrupt control.

A stricter quality assurance program (called special grade in NEC's grade classification) is applied to the (A1) and (A2) products compared to the μPD78912xA and 78913xA, which are classified as standard grade.

In addition, a flash memory version (μPD78F9136A) that can operate within the same power supply voltage range as the mask ROM version, and a range of development tools are also being prepared.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD789104A, 789114A, 789124A, 789134A Subseries User's Manual: U14643E
78K/0S Series User's Manual Instruction: U11047E

FEATURES

- On-chip multiplier: 8 bits × 8 bits = 16 bits
- ROM and RAM sizes

Item / Part Number	Program Memory (ROM)	Data Memory (Internal High-Speed RAM)	Package
μPD789121A(A1), 789131A(A1), 789121A(A2), 789131A(A2)	2 Kbytes	256 bytes	30-pin plastic SSOP (7.62 mm (300))
μPD789122A(A1), 789132A(A1), 789122A(A2), 789132A(A2)	4 Kbytes		
μPD789124A(A1), 789134A(A1), 789124A(A2), 789134A(A2)	8 Kbytes		

- Built-in RC oscillator
- Minimum instruction execution time can be changed from high-speed (0.5 μs) to low-speed (2.0 μs) (@ 4.0-MHz operation with system clock)
- I/O ports: 20
- Serial interface: 1 channel: Switchable between 3-wire serial I/O and UART modes
- 8-bit resolution A/D converter: 4 channels (μPD78912xA(A1), 78912xA(A2))
- 10-bit resolution A/D converter: 4 channels (μPD78913xA(A1), 78913xA(A2))
- Timers: 3 channels
  - 16-bit timer: 1 channel
  - 8-bit timer/event counter: 1 channel
  - Watchdog timer: 1 channel
- Power supply voltage: V_{DD} = 4.5 to 5.5 V

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APPLICATIONS

Cleaners, washing machines, and refrigerators

ORDERING INFORMATION

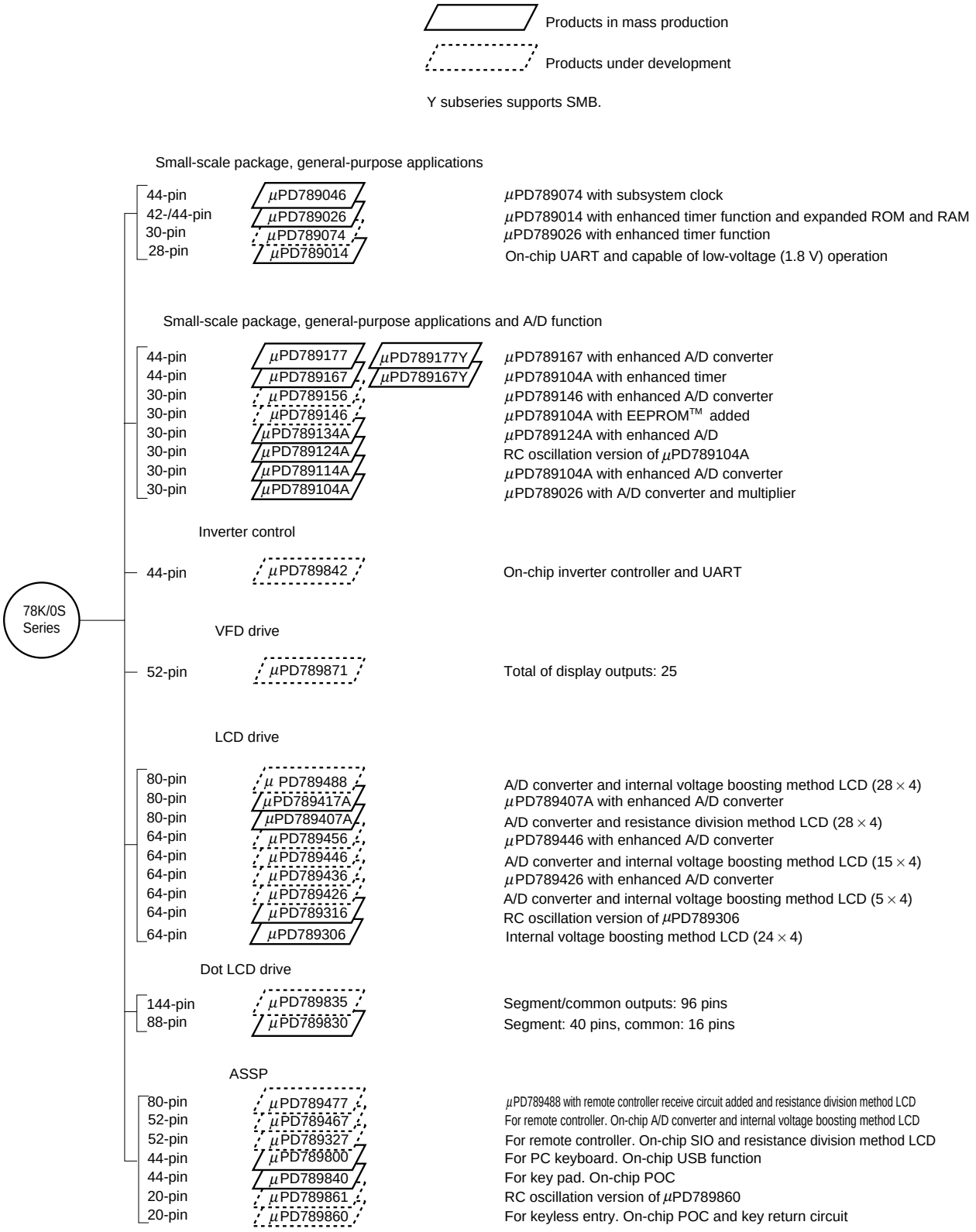
Part Number	Package	Quality grade
μPD789121AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789122AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789124AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789131AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789132AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789134AMC(A1)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789121AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789122AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789124AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789131AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789132AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special
μPD789134AMC(A2)-×××-5A4	30-pin plastic SSOP (7.62 mm (300))	Special

Remark ××× indicates ROM code suffix.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

78K/0S SERIES LINEUP

The products in the 78K/0S Series are listed below. The names enclosed in boxes are subseries names.



The major functional differences among the subseries are listed below.

Subseries Name \ Function		ROM Capacity	8-Bit	16-Bit	Watch	WDT	8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_{DD} MIN Value	Remark
Small scale, general-purpose applications	μPD789046	16 K	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART: 1 ch)	34	1.8 V	–
	μPD789026	4 K to 16 K			–							
	μPD789074	2 K to 8 K								24		
	μPD789014	2 K to 4 K	2 ch	–						22		
Small-scale, general-purpose applications + A/D function	μPD789177	16 K to 24 K	3 ch	1 ch	1 ch		–	8 ch	1 ch (UART: 1 ch)	31		–
	μPD789167						8 ch	–				
	μPD789156	8 K to 16 K	1 ch		–		–	4 ch		20		On-chip EEPROM
	μPD789146						4 ch	–				
	μPD789134A	2 K to 8 K						4 ch				RC oscillation version
	μPD789124A						4 ch	–				
	μPD789114A						–	4 ch				–
	μPD789104A						4 ch	–				
Inverter control	μPD789842	8 K to 16 K	3 ch	**Note**	1 ch	1 ch	8 ch	–	1 ch (UART: 1 ch)	30	4.0 V	–
VFD drive	μPD789871	4 K to 8 K	3 ch	–	1 ch	1 ch	–	–	1 ch	33	2.7 V	–
LCD drive	μPD789488	32 K	3 ch	1 ch	1 ch	1 ch	–	8 ch	2 ch (UART: 1 ch)	45	1.8 V	–
	μPD789417A	12 K to 24 K						7 ch	1 ch (UART: 1 ch)	43		
	μPD789407A						7 ch	–				
	μPD789456	12 K to 16 K	2 ch				–	6 ch		30		
	μPD789446						6 ch	–				
	μPD789436						–	6 ch		40		
	μPD789426						6 ch	–				
	μPD789316	8 K to 16 K					–		2 ch (UART: 1 ch)	23		RC oscillation version
	μPD789306											–
Dot LCD drive	μPD789835	24 K to 60 K	6 ch	–	1 ch	1 ch	3 ch	–	1 ch (UART: 1 ch)	28	1.8 V	–
	μPD789830	24 K	1 ch	1 ch			–			30	2.7 V	
ASSP	μPD789477	24 K	3 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch (UART: 1 ch)	45	1.8 V	On-chip LCD
	μPD789467	4 K to 24 K	2 ch	–			1 ch		–	18		
	μPD789327						–		1 ch	21		
	μPD789800	8 K			–				2 ch (USB: 1 ch)	31	4.0 V	–
	μPD789840						4 ch		1 ch	29	2.8 V	
	μPD789861	4 K					–		–	14	1.8 V	RC oscillation version, on-chip EEPROM
	μPD789860											On-chip EEPROM

Note 10-bit timer: 1 channel

OVERVIEW OF FUNCTIONS

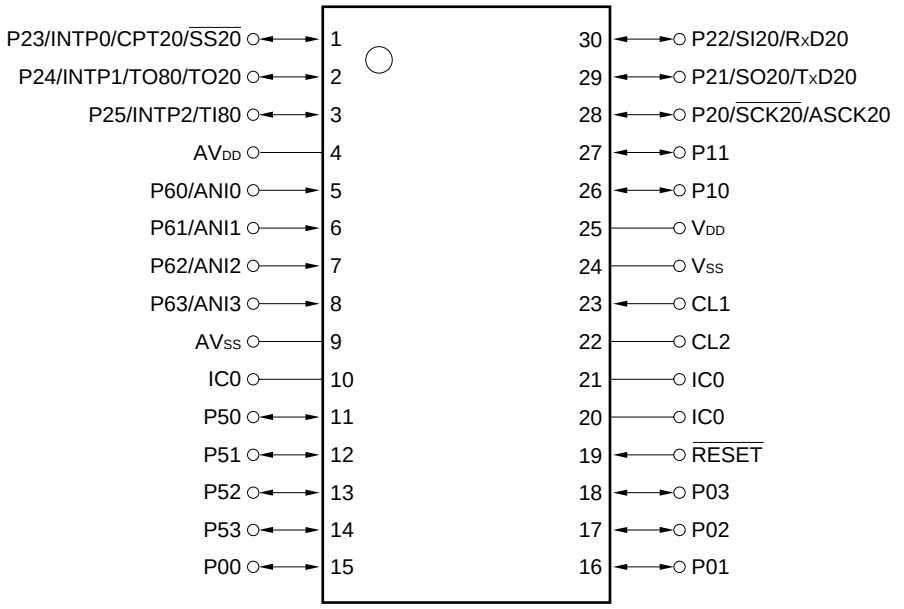
Item		μPD789121A(A1) μPD789131A(A1) μPD789121A(A2) μPD789131A(A2)	μPD789122A(A1) μPD789132A(A1) μPD789122A(A2) μPD789132A(A2)	μPD789124A(A1) μPD789134A(A1) μPD789124A(A2) μPD789134A(A2)
Internal memory	ROM	2 Kbytes	4 Kbytes	8 Kbytes
	High-speed RAM	256 bytes		
Oscillator		RC Oscillator		
Minimum instruction execution time		0.5/2.0 μs (@ 4.0-MHz operation with system clock)		
General-purpose registers		8 bits × 8 registers		
Instruction set		• 16-bit operations • Bit manipulations (set, reset, and test)		
Multiplier		8 bits × 8 bits = 16 bits		
I/O ports		Total: 20 • CMOS input: 4 • CMOS I/O: 12 • N-ch open-drain (12-V withstand voltage): 4		
A/D converters		• 8-bit resolution × 4 channels (μPD78912xA(A1), 78912xA(A2)) • 10-bit resolution × 4 channels (μPD78913xA(A1), 78913xA(A2))		
Serial interface		• Switchable between 3-wire serial I/O and UART modes		
Timer		• 16-bit timer: 1 channel • 8-bit timer/event counter: 1 channel • Watchdog timer: 1 channel		
Timer output		1 output (16-bit/8-bit timer alternate function)		
Vectored interrupt sources	Maskable	Internal: 6, External: 3		
	Non-maskable	Internal: 1		
Power supply voltage		V_{DD} = 4.5 to 5.5 V		
Operating ambient temperature		• T_A = –40 to +110°C (μPD78912xA(A1), 78913xA(A1)) • T_A = –40 to +125°C (μPD78912xA(A2), 78913xA(A2))		
Package		• 30-pin plastic SSOP (7.62 mm (300))		

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- 30-pin plastic SSOP (7.62 mm (300))

  μPD789121AMC(A1)-×××-5A4 μPD789122AMC(A1)-×××-5A4 μPD789124AMC(A1)-×××-5A4
  μPD789131AMC(A1)-×××-5A4 μPD789132AMC(A1)-×××-5A4 μPD789134AMC(A1)-×××-5A4
  μPD789121AMC(A2)-×××-5A4 μPD789122AMC(A2)-×××-5A4 μPD789124AMC(A2)-×××-5A4
  μPD789131AMC(A2)-×××-5A4 μPD789132AMC(A2)-×××-5A4 μPD789134AMC(A2)-×××-5A4



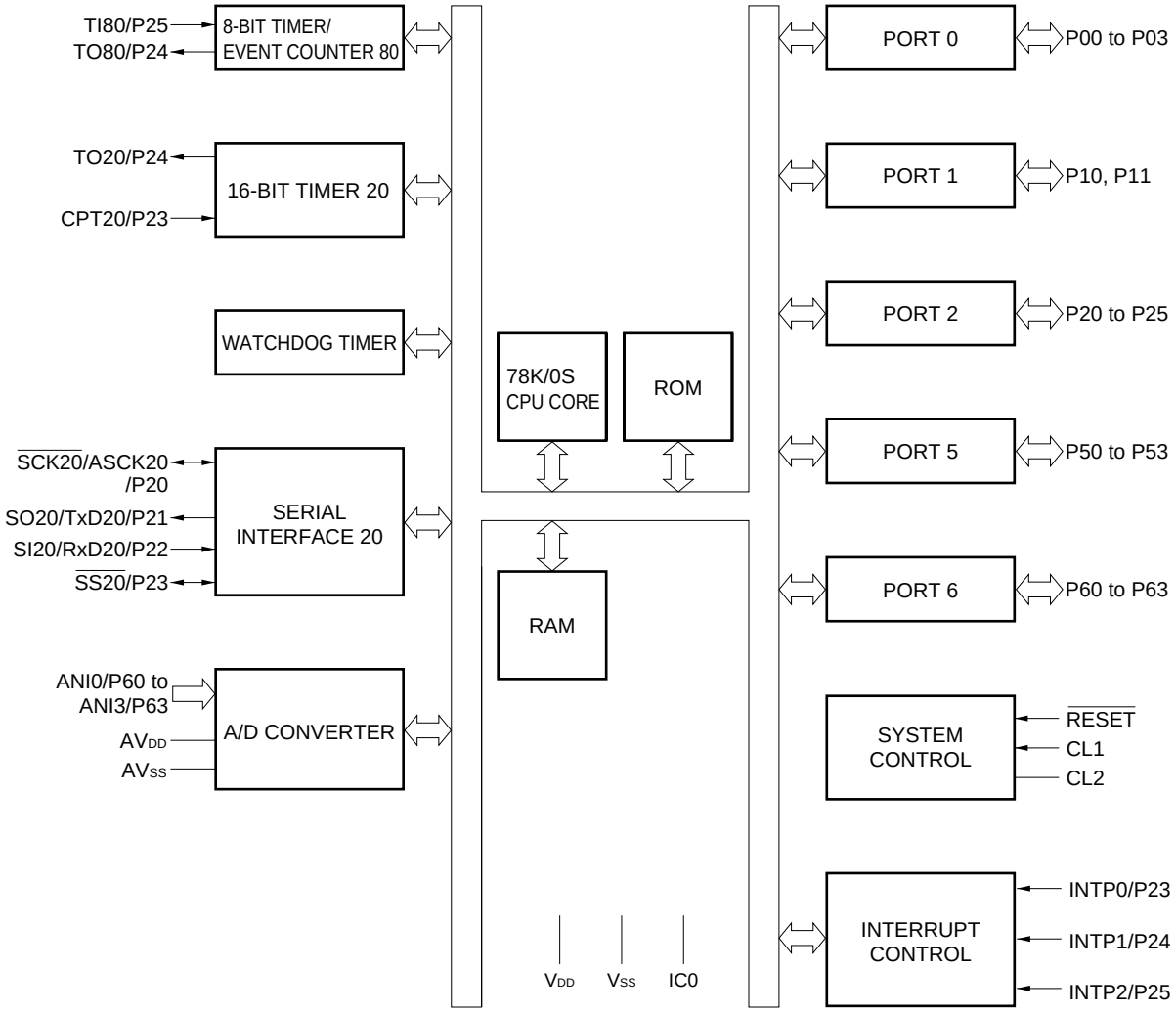
Cautions 1. Connect the IC0 (Internally Connected) pin directly to V_{SS}.

2. Connect the AV_{DD} pin to V_{DD}.

3. Connect the AV_{SS} pin to V_{SS}.

ANI0 to ANI3:	Analog Input	$\overline{\text{RESET}}$:	Reset
ASCK20:	Asynchronous Serial Input	RxD20:	Receive Data
AV_{DD}:	Analog Power Supply	$\overline{\text{SCK20}}$:	Serial Clock Input/Output
AV_{SS}:	Analog Ground	SI20:	Serial Data Input
CL1, CL2:	RC Oscillator	SO20:	Serial Data Output
CPT20:	Capture Trigger Input	$\overline{\text{SO20}}$:	Serial Data Output
IC0:	Internally Connected	SS20:	Chip Select Input
INTP0 to INTP2:	Interrupt from Peripherals	TI80:	Timer Input
P00 to P03:	Port0	TO20, TO80:	Timer Output
P10, P11:	Port1	TxD20:	Transmit Data
P20 to P25:	Port2	V_{DD}:	Power Supply
P50 to P53:	Port5	V_{SS}:	Ground
P60 to P63:	Port6		

2. BLOCK DIAGRAM



Remark The internal ROM capacity varies depending on the product.

3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P03	I/O	Port 0 4-bit input/output port Input/output can be specified in 1-bit units When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	–
P10, P11	I/O	Port 1 2-bit input/output port Input/output can be specified in 1-bit units When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	–
P20	I/O	Port 2 6-bit input/output port Input/output can be specified in 1-bit units When used as an input port, an on-chip pull-up resistor can be specified by means of software.	Input	$\overline{\text{SCK20}}$/ASCK20
P21				SO20/TxD20
P22				SI20/RxD20
P23				INTP0/CPT20 /$\overline{\text{SS20}}$
P24				INTP1/TO80/TO20
P25				INTP2/TI80
P50 to P53	I/O	Port 5 4-bit N-ch open-drain input/output port Input/output can be specified in 1-bit units An on-chip pull-up resistor can be specified by the mask option.	Input	–
P60 to P63	Input	Port 6 4-bit input-only port	Input	ANI0 to ANI3

3.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P23/CPT20/$\overline{SS20}$
INTP1				P24/TO80/TO20
INTP2				P25/TI80
SI20	Input	Serial interface serial data input	Input	P22/RxD20
SO20	Output	Serial interface serial data output	Input	P21/TxD20
$\overline{SCK20}$	I/O	Serial interface serial clock input/output	Input	P20/ASCK20
ASCK20	Input	Serial clock input for asynchronous serial interface	Input	P20/$\overline{SCK20}$
$\overline{SS20}$	Input	Chip select input for serial interface	Input	P23/CPT20/INTP0
RxD20	Input	Serial data input for asynchronous serial interface	Input	P22/SI20
TxD20	Output	Serial data output for asynchronous serial interface	Input	P21/SO20
TI80	Input	External count clock input to 8-bit timer/event counter 80	Input	P25/INTP2
TO80	Output	8-bit timer/event counter 80 output	Input	P24/INTP1/TO20
TO20	Output	16-bit timer 20 output	Input	P24/INTP1/TO80
CPT20	Input	Capture edge input	Input	P23/INTP0/$\overline{SS20}$
ANI0 to ANI3	Input	A/D converter analog input	Input	P60 to P63
AV_{DD}	-	A/D converter analog power supply	–	–
AV_{SS}	-	A/D converter ground potential	–	–
CL1	Input	Connected to resistor (R) or capacitor (C)	–	–
CL2	-		–	–
$\overline{RESET}$	Input	System reset input	Input	–
V_{DD}	-	Positive power supply	–	–
V_{SS}	-	Ground potential	–	–
IC0	-	Internally connected. Connect directly to V_{SS}.	–	–

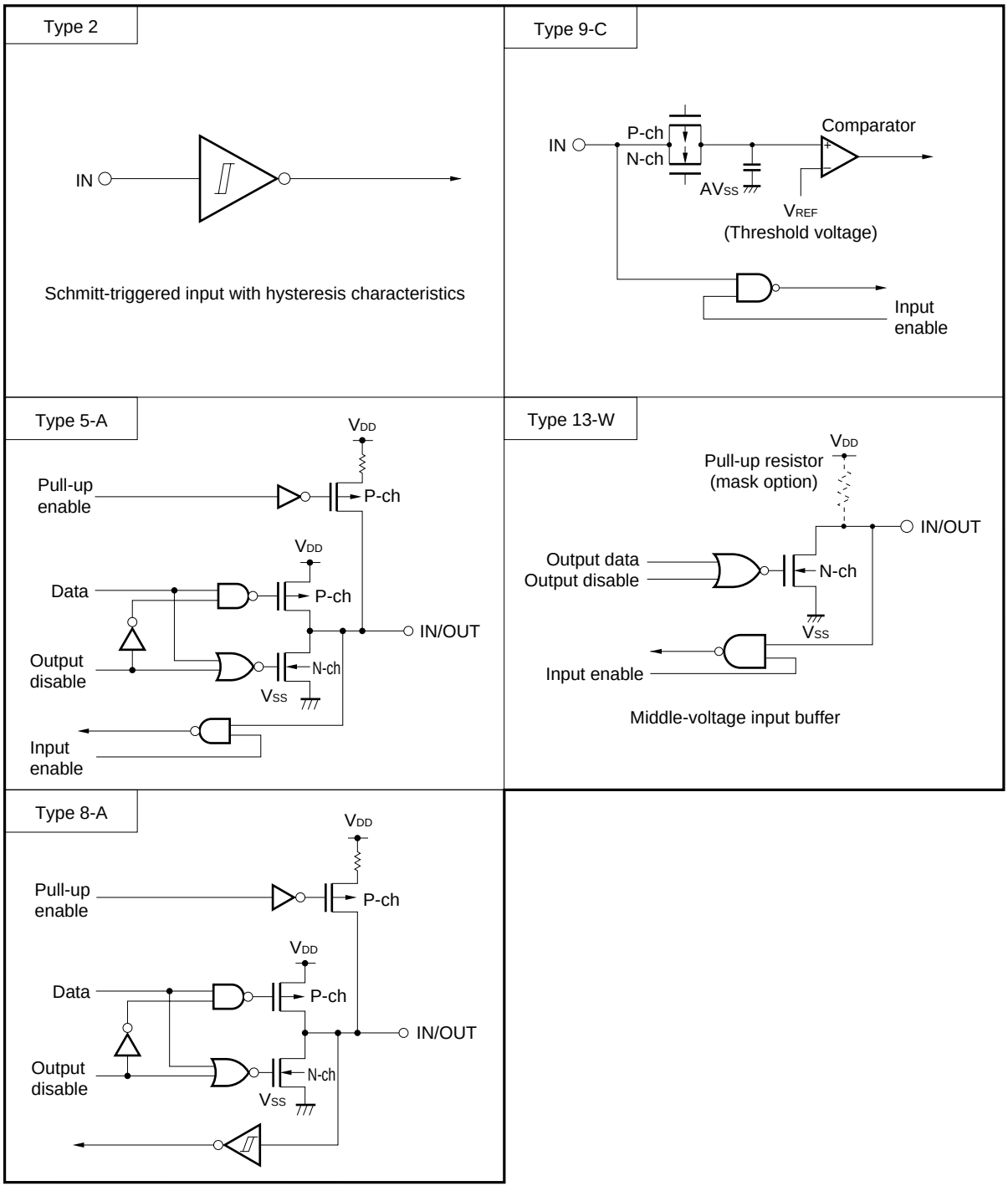
3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, refer to Figure 3-1.

Table 3-1. Types of Pin Input/Output Circuits

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection of Unused Pins
P00 to P03	5-A	I/O	Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open
P10, P11			
P20/$\overline{SCK20}$/ASCK20	8-A		
P21/SO20/T_XD20			
P22/SI20/R_XD20			
P23/INTP0/CPT20/$\overline{SS20}$			Input: Independently connect to V_{SS} via a resistor. Output: Leave open
P24/INTP1/TO80/TO20			
P25/INTP2/TI80			
P50 to P53	13-W		Input: Independently connect to V_{DD} via a resistor. Output: Leave open
P60/ANI0 to P63/ANI3	9-C	Input	Connect directly to V_{DD} or V_{SS}.
AV_{DD}	–	–	Connect to V_{DD}.
AV_{SS}			Connect to V_{SS}.
$\overline{RESET}$	2	Input	–
IC0	–	–	Connect directly to V_{SS}.

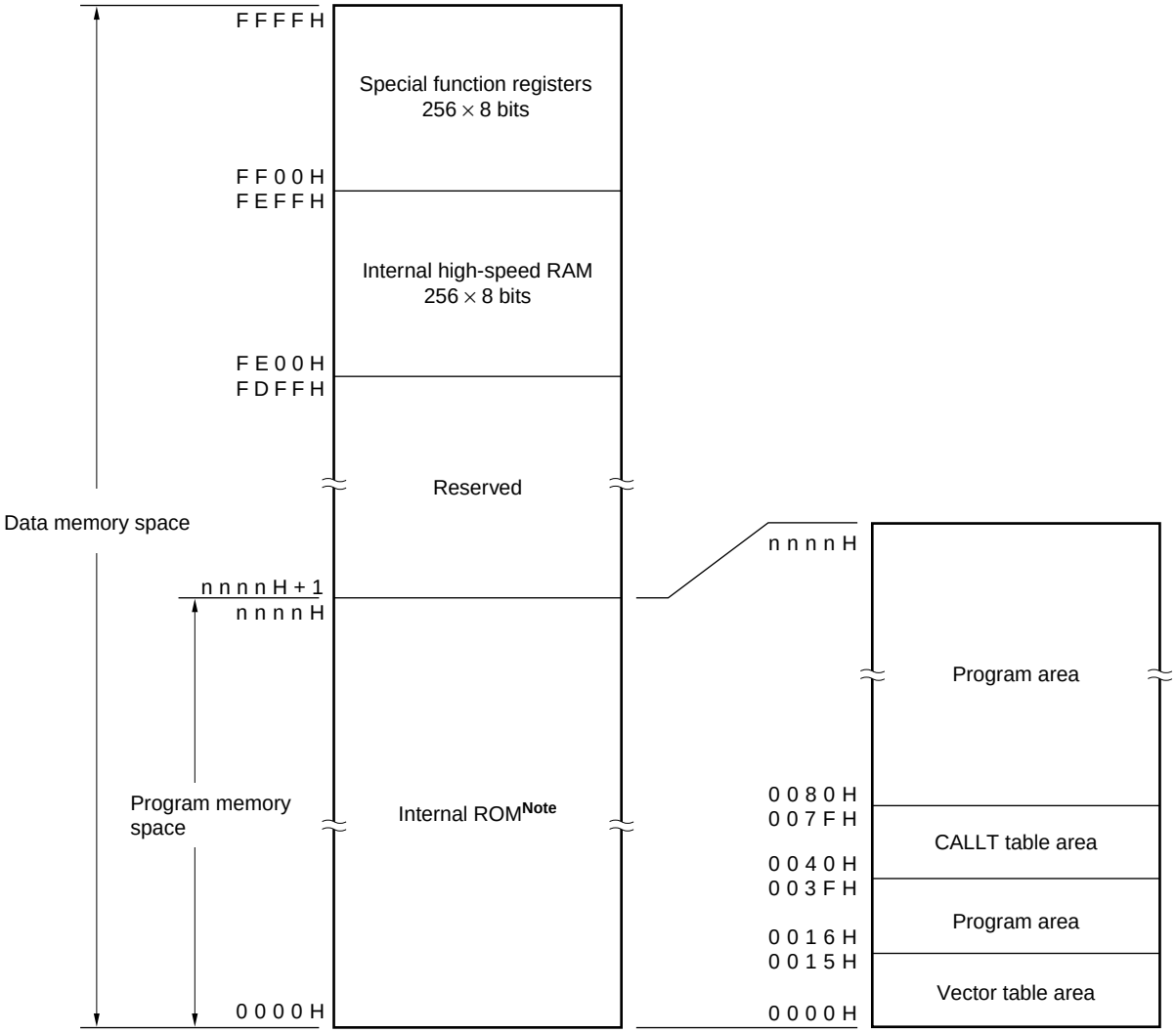
Figure 3-1. Pin Input/Output Circuits



4. MEMORY SPACE

Figure 4-1 shows the memory map of the μPD78912xA(A1), 78913xA(A1), 78912xA(A2), and 78913xA(A2).

Figure 4-1. Memory Map



Note The internal ROM capacity depends on the product. (See the following table).

Part Number	Last Address of Internal ROM nnnnH
μPD789121A(A1), 789131A(A1), 789121A(A2), 789131A(A2)	07FFH
μPD789122A(A1), 789132A(A1), 789122A(A2), 789132A(A2)	0FFFH
μPD789124A(A1), 789134A(A1), 789124A(A2), 789134A(A2)	1FFFH

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

The following three types of I/O ports are available:

- CMOS Input (port 6): 4
- CMOS input/output (ports 0 to 2): 12
- N-ch open-drain input/output (port 5): 4

Total: 20

Table 5-1. Port Functions

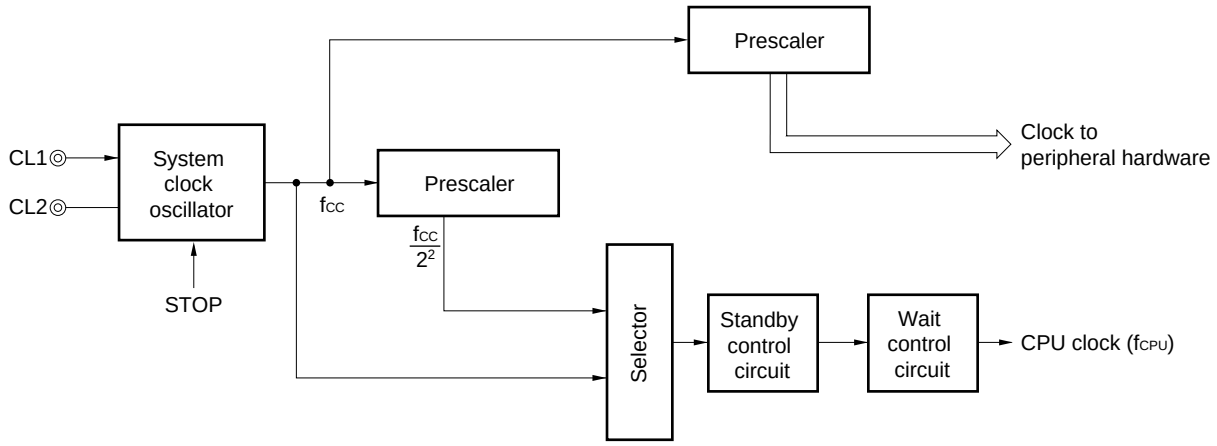
Port Name	Pin Name	Function
Port 0	P00 to P03	Input/output port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.
Port 1	P10, P11	Input/output port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.
Port 2	P20 to P25	Input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.
Port 5	P50 to P53	N-channel open-drain input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by the mask option.
Port 6	P60 to P63	Input-only port

5.2 Clock Generator

An on-chip system clock generator is provided.
The minimum instruction execution time can be changed.

- 0.5 μs/2.0 μs (@ 4.0-MHz operation with system clock)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer

Three on-chip timers are provided.

- 16-bit timer 20: 1 channel
- 8-bit timer/event counter 80: 1 channel
- Watchdog timer: 1 channel

Table 5-2. Timer Operation

		16-Bit Timer 20	8-Bit Timer/Event Counter 80	Watchdog Timer
Operation mode	Interval timer	–	1 channel	1 channel
	External event counter	–	1 channel	–
Function	Timer output	1 output	1 output	–
	PWM output	–	1 output	–
	Square wave output	–	1 output	–
	Capture	1 input	–	–
	Interrupt request	1	1	1

Figure 5-2. Block Diagram of 16-Bit Timer 20 (TM20)

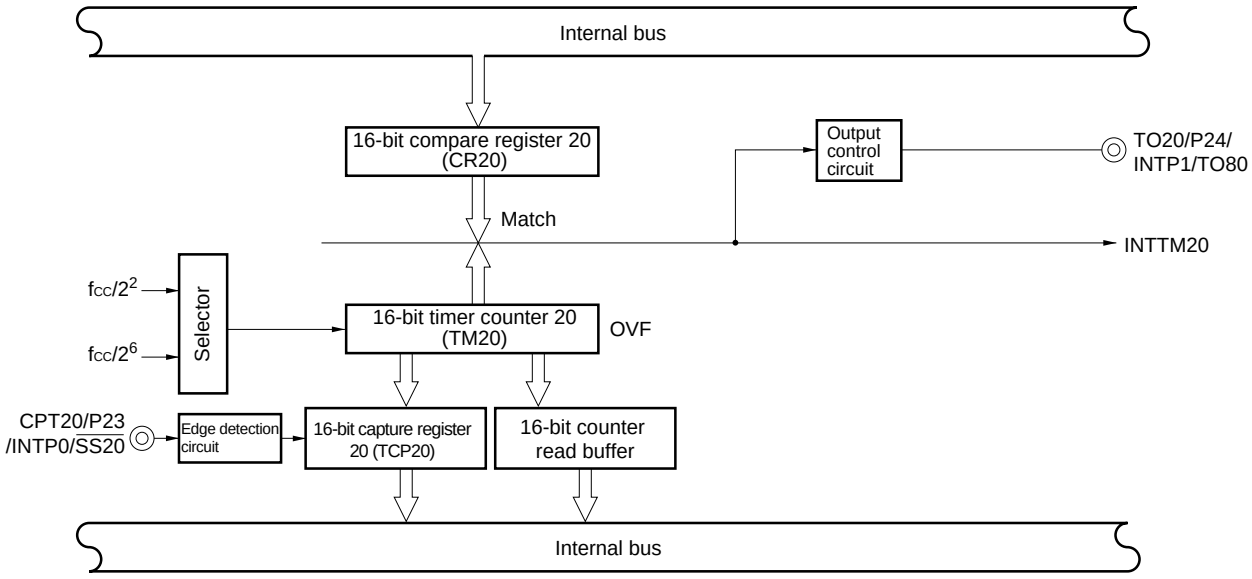


Figure 5-3. Block Diagram of 8-Bit Timer/Event Counter 80 (TM80)

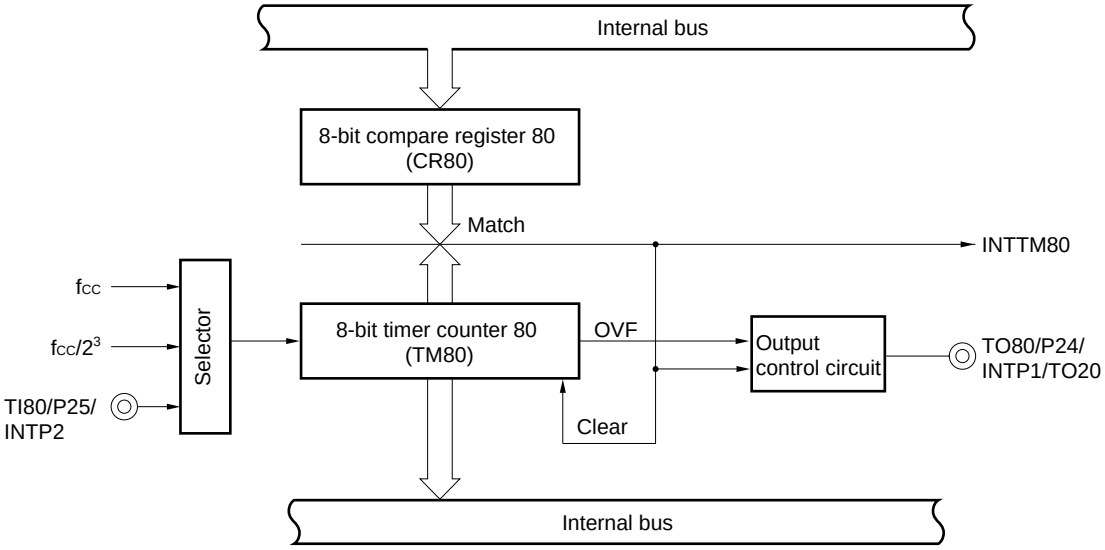
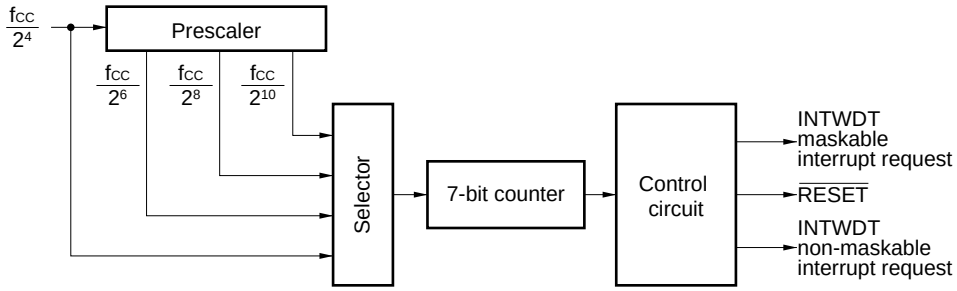


Figure 5-4. Watchdog Timer Block Diagram



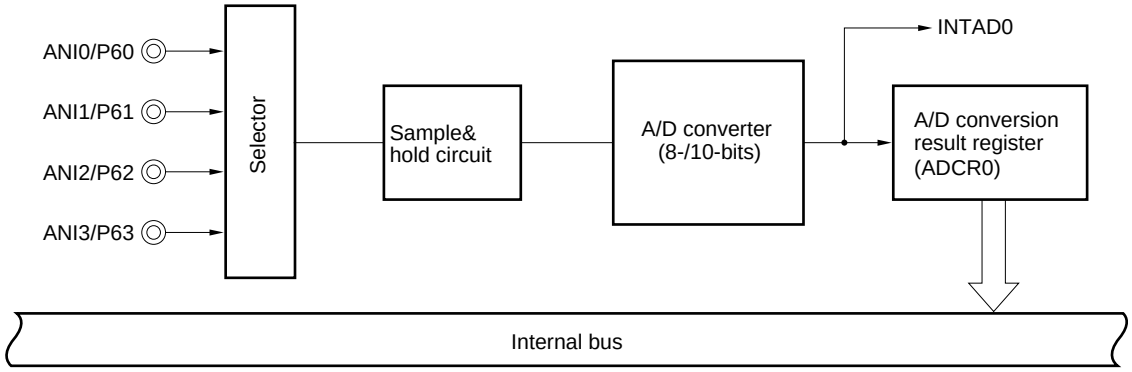
5.4 A/D Converter

The conversion resolution of the A/D converter differs depending on the product as shown below.

- 8-bit A/D converter × 4 channels
  ..... μPD789121A(A1), 789122A(A1), 789124A(A1), 789121A(A2), 789122A(A2), 789124A(A2)
- 10-bit A/D converter × 4 channels
  ..... μPD789131A(A1), 789132A(A1), 789134A(A1), 789131A(A2), 789132A(A2), 789134A(A2)

A/D conversion can be only started by software.

Figure 5-5. A/D Converter Block Diagram



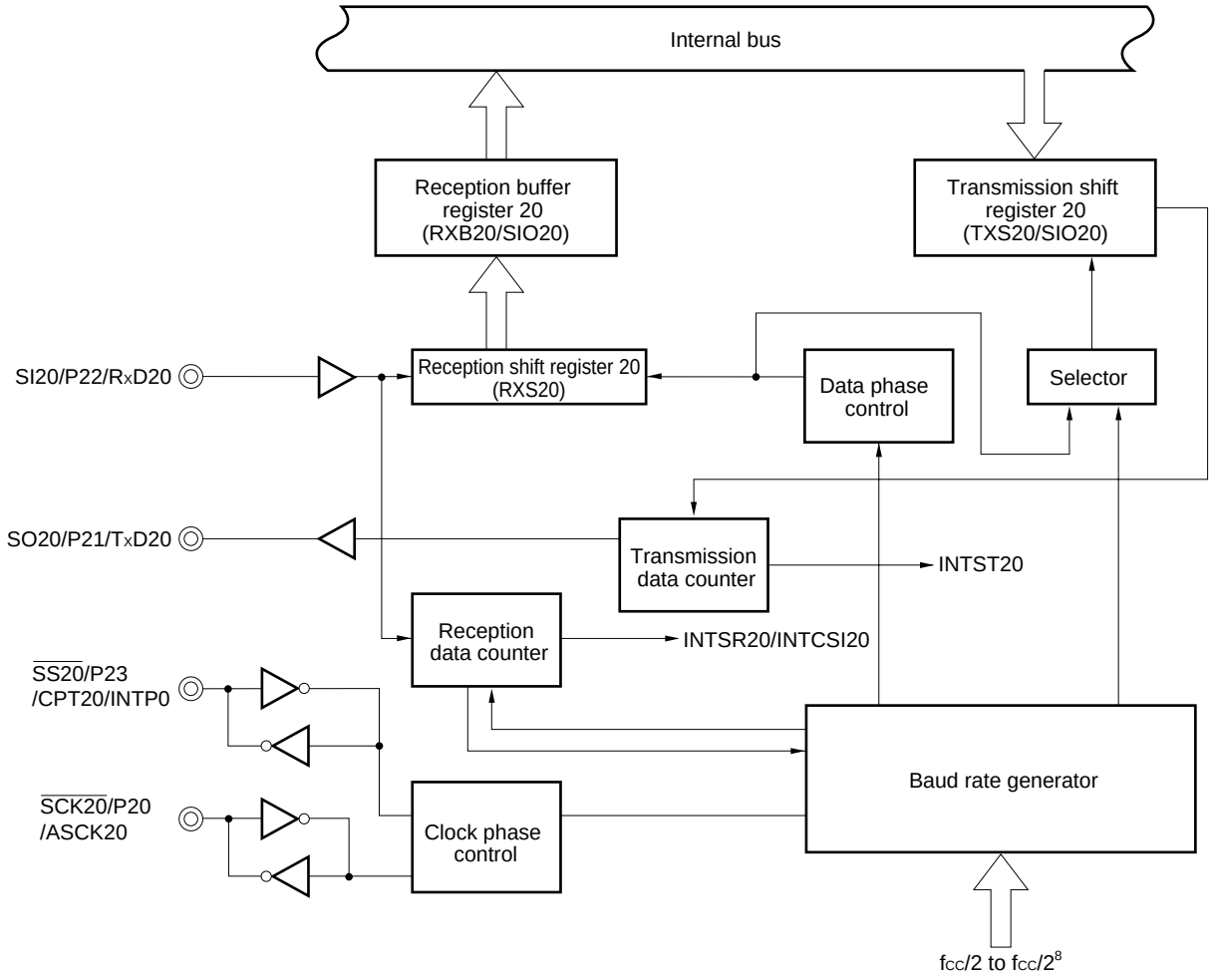
5.5 Serial Interface 20

A one-channel serial interface is incorporated.

Serial interface 20 has following three modes:

- Operation stop mode: Power consumption can be reduced.
- Asynchronous serial interface (UART) mode: A dedicated baud rate generator is incorporated.
- 3-wire serial I/O mode: A function to select the clock phase or data phase is incorporated.

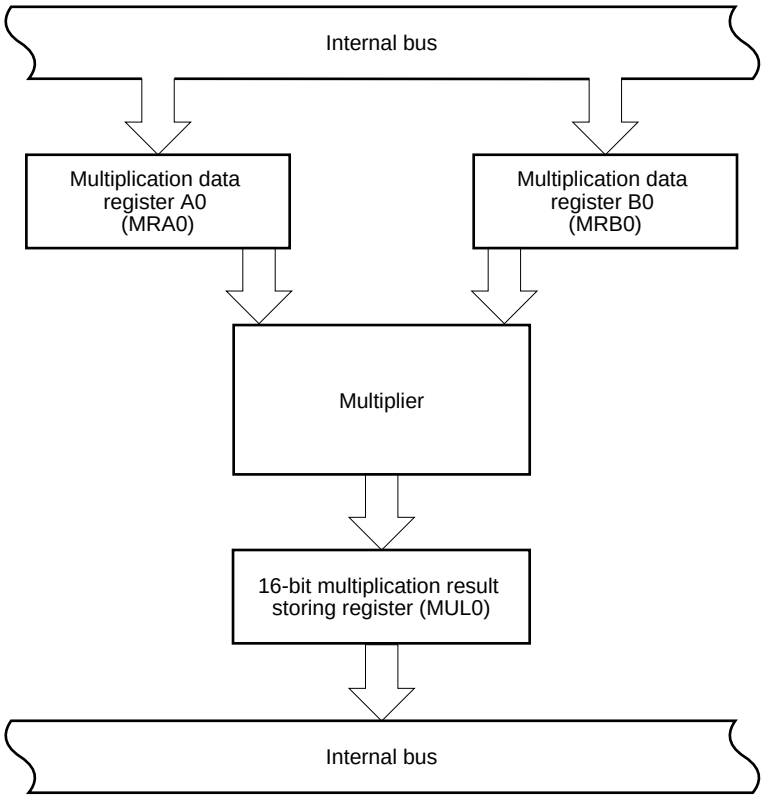
Figure 5-6. Block Diagram of Serial Interface 20



5.6 Multiplier

The calculation of 8 bits × 8 bits = 16 bits can be performed.

Figure 5-7. Multiplier Block Diagram



6. INTERRUPT FUNCTION

A total of 10 interrupt sources are provided, divided into the following two types.

- Non-maskable interrupts: 1 source
- Maskable interrupts: 9 sources

Table 6-1. Interrupt Source List

Interrupt Type	Priority[Note 1]	Interrupt Source		Internal/External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	–	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with the interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTSR20	End of serial interface 20 UART reception	Internal	000CH	(B)
		INTCSI20	End of serial interface 20 3-wire SIO transfer reception			
	5	INTST20	End of serial interface 20 UART transmission		000EH	
	6	INTTM80	Generation of matching signal of 8-bit timer/event counter 80		0010H	
	7	INTTM20	Generation of matching signal of 16-bit timer 20		0012H	
	8	INTAD0	A/D conversion completion signal		0014H	

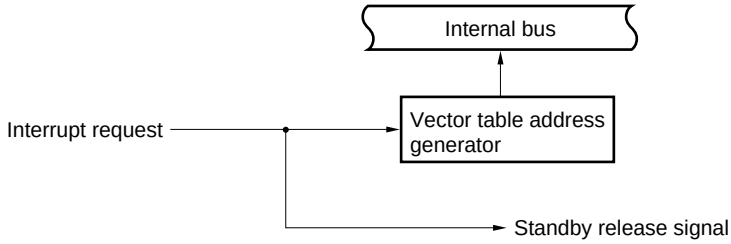
Notes 1. Priority is the priority order when several maskable interrupt requests are generated at the same time. 0 is the highest order and 8 is the lowest order.

2. Basic configuration types (A), (B), and (C) correspond to (A), (B), and (C) in Figure 6-1.

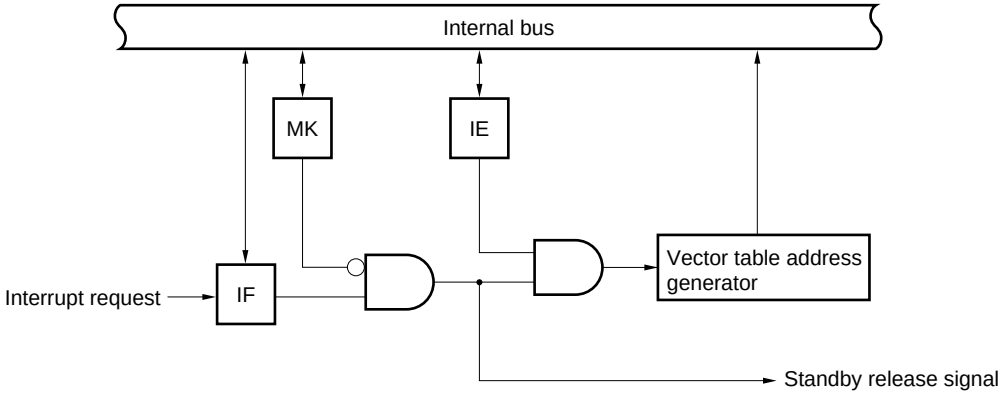
Remark As the interrupt source of the watchdog timer (INTWDT), either a non-maskable interrupt or a maskable interrupt (internal) can be selected.

Figure 6-1. Basic Configuration of Interrupt Function

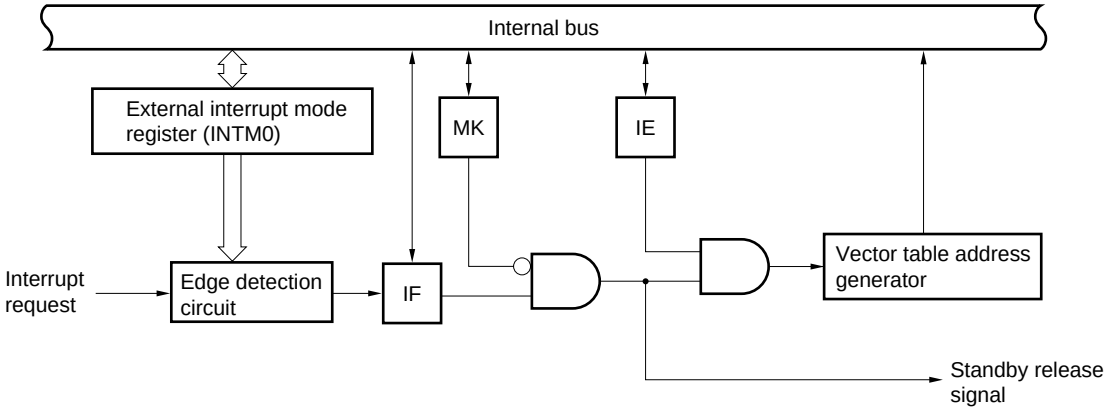
(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt



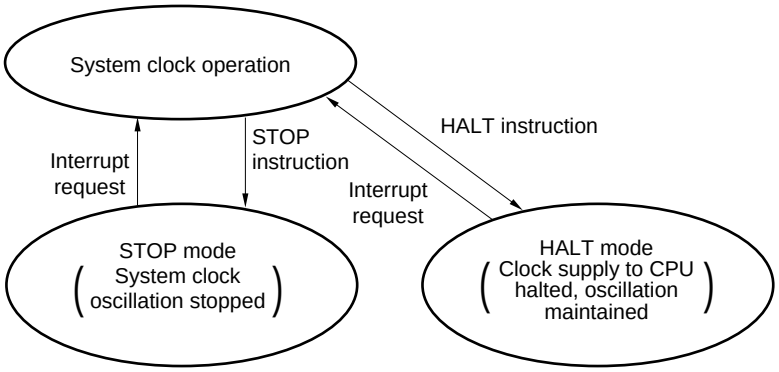
IF: Interrupt request flag
IE: Interrupt enable flag
MK: Interrupt mask flag

7. STANDBY FUNCTION

The following two standby functions are available for further reduction of system current consumption.

- HALT mode: In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.
- STOP mode: In this mode, oscillation of the system clock is stopped. All the operations performed on the system clock are suspended, resulting in extremely small power consumption.

Figure 7-1. Standby Function



8. RESET FUNCTION

The following two reset methods are available.

- External reset by $\overline{\text{RESET}}$ signal input
- Internal reset by watchdog timer runaway time detection

9. MASK OPTION

The μPD78912×A(A1), 78913×A(A1), 78912×A(A2), and 78913×A(A2) have the following mask options.

- Mask options for P50 to P53
  An on-chip pull-up resistor can be selected in bit units.
  <1> Specifies on-chip pull-up resistor.
  <2> Does not specify on-chip pull-up resistor.

10. INSTRUCTION SET OVERVIEW

The instruction set for the μPD78912×A(A1), 78913×A(A1), 78912×A(A2), and 78913×A(A2) is listed later.

10.1 Conventions

10.1.1 Operand identifiers and description methods

Operands are described in the “Operand” column of each instruction in accordance with the description method of the instruction operand identifier (refer to the assembler specifications for detail). When there are two or more description methods, select one of them. Alphabetic letters in capitals and the symbols, #, !, $, and [ ], are keywords and must be described as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: Absolute address specification
- $: Relative address specification
- [ ]: Indirect address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to describe the #,!, $, or [ ] symbols.

For operand register identifiers, r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for description.

Table 10-1. Operand Identifiers and Description Methods

Identifier	Description Method
r rp sfr	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7), AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special function register symbol
saddr saddrp	FE20H to FF1FH immediate data or label FE20H to FF1FH immediate data or label (even address only)
addr16 addr5	0000H to FFFFH immediate data or label (Only even addresses for 16-bit data transfer instructions) 0040H to 007FH immediate data or label (even address only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label

10.1.2 Descriptions of the operation field

A:	A register; 8-bit accumulator
X:	X register
B:	B register
C:	C register
D:	D register
E:	E register
H:	H register
L:	L register
AX:	AX register pair; 16-bit accumulator
BC:	BC register pair
DE:	DE register pair
HL:	HL register pair
PC:	Program counter
SP:	Stack pointer
PSW:	Program status word
CY:	Carry flag
AC:	Auxiliary carry flag
Z:	Zero flag
IE:	Interrupt request enable flag
NMIS:	Non-maskable interrupt servicing flag
( ):	Memory contents indicated by address or register contents in parentheses
X_H, X_L:	Higher 8 bits and lower 8 bits of 16-bit register
∧:	Logical product (AND)
∨:	Logical sum (OR)
$\overline{\vee}$:	Exclusive OR
$\overline{\quad}$:	Inverted data
addr16:	16-bit immediate data or label
jdisp8:	Signed 8-bit data (displacement value)

10.1.3 Description of the flag operation field

(Blank):	Not affected
0:	Cleared to 0
1:	Set to 1
×:	Set/cleared according to the result
R:	Previously saved value is restored

10.2 Operations

Mnemonic	Operand	Byte	Clock	Operation	Flag
					Z AC CY
MOV	r, #byte	3	6	r ← byte	
	saddr , #byte	3	6	(addr) ← byte	
	sfr, #byte	3	6	sfr ← byte	
	A, r Note 1	2	4	A ← r	
	r, A Note 1	2	4	r ← A	
	A, saddr	2	4	A ← (saddr)	
	saddr, A	2	4	(saddr) ← A	
	A, sfr	2	4	A ← sfr	
	sfr, A	2	4	sfr ← A	
	A, !addr16	3	8	A ← (addr16)	
	!addr16, A	3	8	(addr16) ← A	
	PSW, #byte	3	6	PSW ← byte	× × ×
	A, PSW	2	4	A ← PSW	
	PSW, A	2	4	PSW ← A	× × ×
	A, [DE]	1	6	A ← (DE)	
	[DE], A	1	6	(DE) ← A	
	A, [HL]	1	6	A ← (HL)	
	[HL], A	1	6	(HL) ← A	
	A, [HL + byte]	2	6	A ← (HL + byte)	
	[HL + byte], A	2	6	(HL + byte) ← A	
XCH	A, X	1	4	A ↔ X	
	A, r Note 2	2	6	A ↔ r	
	A, saddr	2	6	A ↔ (saddr)	
	A, sfr	2	6	A ↔ (sfr)	
	A, [DE]	1	8	A ↔ (DE)	
	A, [HL]	1	8	A ↔ (HL)	
	A, [HL + byte]	2	8	A ↔ (HL + byte)	
MOVW	rp, #word	3	6	rp ← word	
	AX, saddrp	2	6	AX ← (saddrp)	
	saddrp, AX	2	8	(saddrp) ← AX	
	AX, rp Note 3	1	4	AX ← rp	
	rp, AX Note 3	1	4	rp ← AX	
XCHW	AX, rp Note 3	1	8	AX ↔ rp	

Notes 1. Except r = A

2. Except r = A or X

3. Only when rp = BC, DE, HL

Remark One instruction clock cycle is one cycle of the CPU clock (f_{CPU}), selected by the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag		
					Z	AC	CY
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A ,CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16) + CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A – byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r	2	4	A, CY ← A – r	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte)	×	×	×
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r	2	4	A, CY ← A – r – CY	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte) – CY	×	×	×
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	×		

Remark One instruction clock cycle is one cycle of the CPU clock (f_{CPU}), selected by the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag
					Z AC CY
OR	A, #byte	2	4	A ← A ∨ byte	×
	saddr, #byte	3	6	(saddr) ← (saddr) ∨ byte	×
	A, r	2	4	A ← A ∨ r	×
	A, saddr	2	4	A ← A ∨ (saddr)	×
	A, !addr16	3	8	A ← A ∨ (addr16)	×
	A, [HL]	1	6	A ← A ∨ (HL)	×
	A, [HL + byte]	2	6	A ← A ∨ (HL + byte)	×
XOR	A, #byte	2	4	A ← A ▽ byte	×
	saddr, #byte	3	6	(saddr) ← (saddr) ▽ byte	×
	A, r	2	4	A ← A ▽ r	×
	A, saddr	2	4	A ← A ▽ (saddr)	×
	A, !addr16	3	8	A ← A ▽ (addr16)	×
	A, [HL]	1	6	A ← A ▽ (HL)	×
	A, [HL + byte]	2	6	A ← A ▽ (HL + byte)	×
CMP	A, #byte	2	4	A – byte	× × ×
	saddr, #byte	3	6	(saddr) – byte	× × ×
	A, r	2	4	A – r	× × ×
	A, saddr	2	4	A – (saddr)	× × ×
	A, !addr16	3	8	A – (addr16)	× × ×
	A, [HL]	1	6	A – (HL)	× × ×
	A, [HL + byte]	2	6	A – (HL + byte)	× × ×
ADDW	AX, #word	3	6	AX, CY ← AX + word	× × ×
SUBW	AX, #word	3	6	AX, CY ← AX – word	× × ×
CMPW	AX, #word	3	6	AX – word	× × ×
INC	r	2	4	r ← r + 1	× ×
	saddr	2	4	(saddr) ← (saddr) + 1	× ×
DEC	r	2	4	r ← r – 1	× ×
	saddr	2	4	(saddr) ← (saddr) – 1	× ×
INCW	rp	1	4	rp ← rp + 1	
DECW	rp	1	4	rp ← rp – 1	
ROR	A, 1	1	2	(CY, $A_7 \leftarrow A_0$, $A_{m-1} \leftarrow A_m$) × 1	×
ROL	A, 1	1	2	(CY, $A_0 \leftarrow A_7$, $A_{m+1} \leftarrow A_m$) × 1	×
RORC	A, 1	1	2	(CY ← A_0, $A_7 \leftarrow$ CY, $A_{m-1} \leftarrow A_m$) × 1	×
ROLC	A, 1	1	2	(CY ← A_7, $A_0 \leftarrow$ CY, $A_{m+1} \leftarrow A_m$) × 1	×

Remark One instruction clock cycle is one cycle of the CPU clock (f_{CPU}), selected by the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag
					Z AC CY
SET1	saddr. bit	3	6	(saddr. bit) ← 1	
	sfr. bit	3	6	sfr. bit ← 1	
	A. bit	2	4	A. bit ← 1	
	PSW. bit	3	6	PSW. bit ← 1	× × ×
	[HL]. bit	2	10	(HL) . bit ← 1	
CLR1	saddr. bit	3	6	(saddr. bit) ← 0	
	sfr. bit	3	6	sfr. bit ← 0	
	A. bit	2	4	A. bit ← 0	
	PSW. bit	3	6	PSW. bit ← 0	× × ×
	[HL]. bit	2	10	(HL) . bit ← 0	
SET1	CY	1	2	CY ← 1	1
CLR1	CY	1	2	CY ← 0	0
NOT1	CY	1	2	CY ← $\overline{CY}$	×
CALL	!addr16	3	6	(SP – 1) ← (PC + 3)$_H$,(SP – 2) ← (PC + 3)$_L$, PC ← addr16, SP ← SP – 2	
CALLT	[addr5]	1	8	(SP – 1) ← (PC + 1)$_H$,(SP – 2) ← (PC + 1)$_L$, PC$_H$ ← (00000000, addr5 + 1), PC$_L$ ← (00000000, addr5), SP ← SP – 2	
RET		1	6	PC$_H$ ← (SP + 1), PC$_L$ ← (SP), SP ← SP + 2	
RETI		1	8	PC$_H$ ← (SP + 1), PC$_L$ ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R R R
PUSH	PSW	1	2	(SP – 1) ← PSW, SP ← SP – 1	
	rp	1	4	(SP – 1) ← rp$_H$, (SP – 2) ← rp$_L$, SP ← SP – 2	
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R R R
	rp	1	6	rp$_H$ ← (SP + 1), rp$_L$ ← (SP), SP ← SP + 2	
MOVW	SP, AX	2	8	SP ← AX	
	AX, SP	2	6	AX ← SP	
BR	!addr16	3	6	PC ← addr16	
	$addr16	2	6	PC ← PC + 2 + jdisp8	
	AX	1	6	PC$_H$ ← A, PC$_L$ ← X	

Remark One instruction clock cycle is one cycle of the CPU clock (f_{CPU}), selected by the processor clock control register (PCC).

Mnemonic	Operand	Byte	Clock	Operation	Flag
					Z AC CY
BC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 1	
BNC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 0	
BZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 1	
BNZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 0	
BT	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 1	
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 1	
	A. bit , $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 1	
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 1	
BF	saddr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 0	
	sfr. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 0	
	A. bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 0	
	PSW. bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 0	
DBNZ	B, $addr16	2	6	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0	
	C, $addr16	2	6	C ← C – 1, then PC ← PC + 2 + jdisp8 if C ≠ 0	
	saddr, $addr16	3	8	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if(saddr) ≠ 0	
NOP		1	2	No Operation	
EI		3	6	IE ← 1(Enable Interrupt)	
DI		3	6	IE ← 0(Disable Interrupt)	
HALT		1	2	Set HALT Mode	
STOP		1	2	Set STOP Mode	

Remark One instruction clock cycle is one cycle of the CPU clock (f_{CPU}), selected by the processor clock control register (PCC).

11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

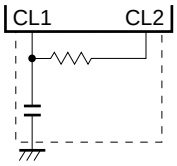
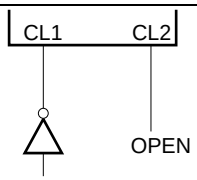
Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}, AV_{DD}	$V_{DD} = AV_{DD}$		–0.3 to +6.5	V
Input voltage	V_{I1}	Pins other than P50 to P53		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P50 to P53	With N-ch open drain	–0.3 to +13	V
			With an on-chip pull-up resistor	–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	μPD78912xA(A1), 78913xA(A1)	–4	mA
		Total for all pins		–14	mA
		Per pin	μPD78912xA(A2), 78913xA(A2)	–2	mA
		Total for all pins		–6	mA
Output current, low	I_{OL}	Per pin	μPD78912xA(A1), 78913xA(A1)	5	mA
		Total for all pins		80	mA
		Per pin	μPD78912xA(A2), 78913xA(A2)	2	mA
		Total for all pins		40	mA
Operating ambient temperature	T_A	μPD78912xA(A1), 78913xA(A1)		–40 to +110	°C
		μPD78912xA(A2), 78913xA(A2)		–40 to +125	°C
Storage temperature	T_{stg}			–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

System Clock Oscillator Characteristics

(V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78912xA(A1), 78913xA(A1)),
–40 to +125°C (μPD78912xA(A2), 78913xA(A2)))

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC resonator		Oscillation frequency (f_{CC})[Note]		2.0		4.0	MHz
External clock		CL1 input frequency (f_{CC})[Note 1]		1.0		5.0	MHz
		CL1 input high-/low-level width (t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC characteristics** for instruction execution time.

2. Time required to stabilize oscillation after a reset or STOP mode release. Use the resonator that stabilizes oscillation during the oscillation wait time.

Cautions 1. When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Construct the oscillator with R, C devices that are guaranteed to operate under the following temparature conditions.

μPD78912xA(A1), 78913xA(A1) : T_A = 110°C
μPD78912xA(A2), 78913xA(A2) : T_A = 125°C

DC Characteristics (V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78912xA(A1), 78913xA(A1)), –40 to +125°C (μPD78912xA(A2), 78913xA(A2))) (1/2)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin	μPD78912xA(A1), 78913xA(A1)				–1	mA
		Total for all pins					–7	mA
		Per pin	μPD78912xA(A2), 78913xA(A2)				–1	mA
		Total for all pins					–3	mA
Output current, low	I_{OL}	Per pin	μPD78912xA(A1), 78913xA(A1)				1.6	mA
		Total for all pins					40	mA
		Per pin	μPD78912xA(A2), 78913xA(A2)				1.6	mA
		Total for all pins					20	mA
Input voltage, high	V_{IH1}	Pins other than described below			0.7 V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P53	With N-ch open drain		0.7 V_{DD}		10	V
			With on-chip pull-up resistor		0.7 V_{DD}		V_{DD}	V
	V_{IH3}	$\overline{\text{RESET}}$, P20 to P25			0.8 V_{DD}		V_{DD}	V
	V_{IH4}	CL1, CL2			V_{DD}–0.1		V_{DD}	V
Input voltage, low	V_{IL1}	Pins other than described below			0		0.3 V_{DD}	V
	V_{IL2}	P50 to P53			0		0.3 V_{DD}	V
	V_{IL3}	$\overline{\text{RESET}}$, P20 to P25			0		0.2 V_{DD}	V
	V_{IL4}	CL1, CL2			0		0.1	V
Output voltage, high	V_{OH1}	I_{OH} = –1 mA			V_{DD}–2.0			V
	V_{OH2}	I_{OH} = –100 μA			V_{DD}–1.0			V
Output voltage, low	V_{OL1}	Pins other than P50 to P53	I_{OL} = 1.6 mA				2.0	V
			I_{OL} = 400 μA				1.0	V
	V_{OL2}	P50 to P53	I_{OL} = 1.6 mA				1.0	V
Input leakage current, high	I_{LIH1}	Pins other than CL1, CL2, or P50 to P53		V_{IN} = V_{DD}			10	μA
	I_{LIH2}	CL1, CL2					20	μA
	I_{LIH3}	P50 to P53 (N-ch open drain)		V_{IN} = 10 V			80	μA
Input leakage current, low	I_{LIL1}	Pins other than CL1, CL2, or P50 to P53		V_{IN} = 0 V			–10	μA
	I_{LIL2}	CL1, CL2					–20	μA
	I_{LIL3}	P50 to P53 (N-ch open drain)					–10[Note]	μA
Output leakage current, high	I_{LOH}	V_{OUT} = V_{DD}					10	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V					–10	μA

Note When pull-up resistors are not connected to P50 to P53 (specified by the mask option) and when port 5 is in input mode, a low-level input leakage current of –60 μA (MAX.) flows only for 1 cycle time after a read instruction has been executed to port 5.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78912xA(A1), 78913xA(A1)), –40 to +125°C (μPD78912xA(A2), 78913xA(A2))) (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Software pull-up resistor	R_1	V_{IN} = 0 V, for pins other than P50 to P53	50	100	300	kΩ
Mask option pull-up resistor	R_2	V_{IN} = 0 V, P50 to P53	10	30	100	kΩ
Power supply current	I_{DD1} Note 1	5.0-MHz crystal oscillation operating mode (C1 = C2 = 22pF) Note 3		1.8	8.0	mA
	I_{DD2} Note 1	5.0-MHz crystal oscillation HALT mode (C1 = C2 = 22pF) Note 3		0.8	5.0	mA
	I_{DD3} Note 1	STOP mode		0.1	1000	μA
	I_{DD4} Note 2	5.0-MHz crystal oscillation A/D operating mode (C1 = C2 = 22pF) Note 3		3.0	10	mA

Notes 1. The current flowing to the ports (including the current flowing through an on-chip pull-up resistor) and AV_{DD} current are not included.

2. The current flowing to the ports (including the current flowing through an on-chip pull-up resistor) is not included.

3. High-speed mode operation (when processor clock control register (PCC) is set to 00H.)

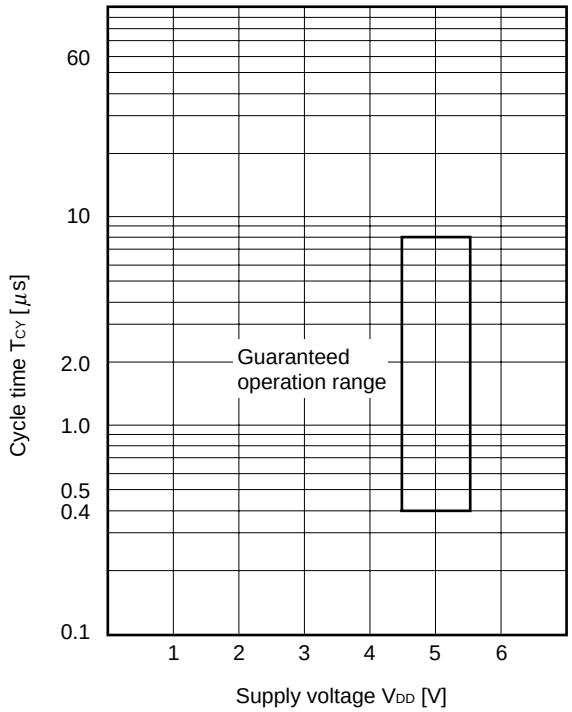
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation (V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78912xA(A1), 78913xA(A1)), –40 to +125°C (μPD78912xA(A2), 78913xA(A2)))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}		0.4		8	μs
TI80 input high-/low-level width	t_{TIH}, t_{TIL}		0.1			μs
TI80 input frequency	f_{TI}		0		4	MHz
Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP2	10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}		10			μs
CPT20 input high-/low-level width	t_{CPH}, t_{CPL}		10			μs

T_{CY} vs V_{DD}



(2) Serial interface (V_{DD} = 4.5 to 5.5 V, T_A = –40 to +110°C (μPD78912xA(A1), 78913xA(A1)), –40 to +125°C (μPD78912xA(A2), 78913xA(A2)))

(i) 3-wire serial I/O mode ($\overline{SCK20}$...Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY1}		800			ns
$\overline{SCK20}$ high-/low-level width	t_{KH1}, t_{KL1}		$t_{KCY1}/2 - 50$			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK1}		150			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{KSI1}		400			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	0		250	ns

Note R and C are the load resistance and load capacitance of the SO output line.

(ii) 3-wire serial I/O mode ($\overline{SCK20}$...External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK20}$ high-/low-level width	t_{KH2}, t_{KL2}		400			ns
SI20 setup time (to $\overline{SCK20}$↑)	t_{SIK2}		100			ns
SI20 hold time (from $\overline{SCK20}$↑)	t_{KSI2}		400			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	0		300	ns
SO20 setup time (for $\overline{SS20}$↓ when $\overline{SS20}$ is used)	t_{KAS2}				120	ns
SO20 disable time (for $\overline{SS20}$↑ when $\overline{SS20}$ is used)	t_{KDS2}				240	ns

Note R and C are the load resistance and load capacitance of the SO output line.

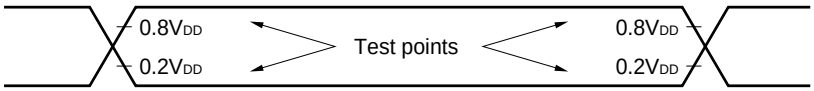
(iii) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					78125	bps

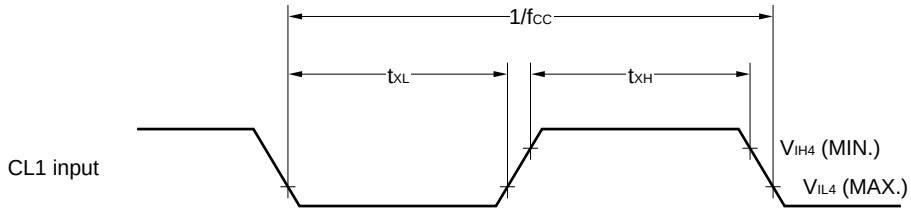
(iv) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{KCY3}		800			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}		400			ns
Transfer rate					39063	bps
ASCK20 rise/fall time	t_R, t_F				1	μs

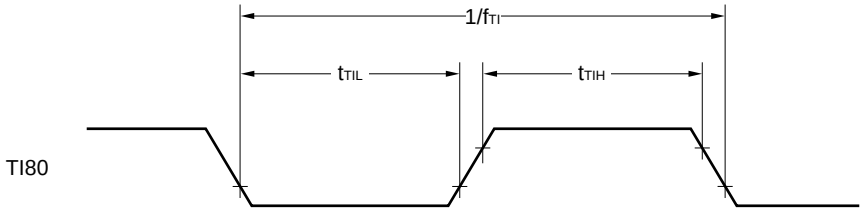
AC Timing Test Points (excluding CL1 input)



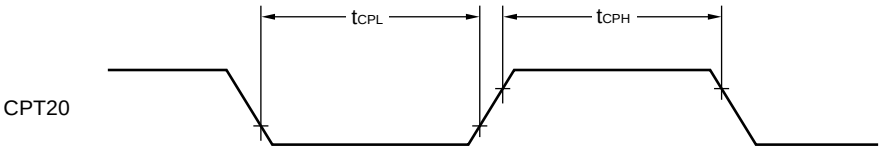
Clock Timing



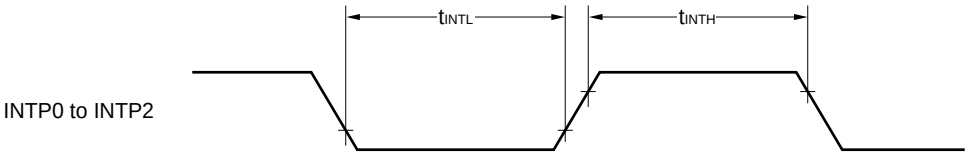
TI Timing



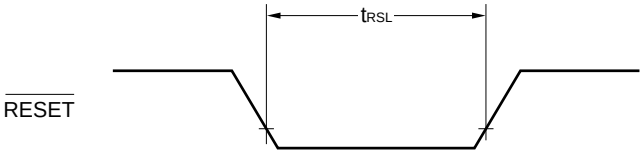
Capture Input Timing



Interrupt Input Timing

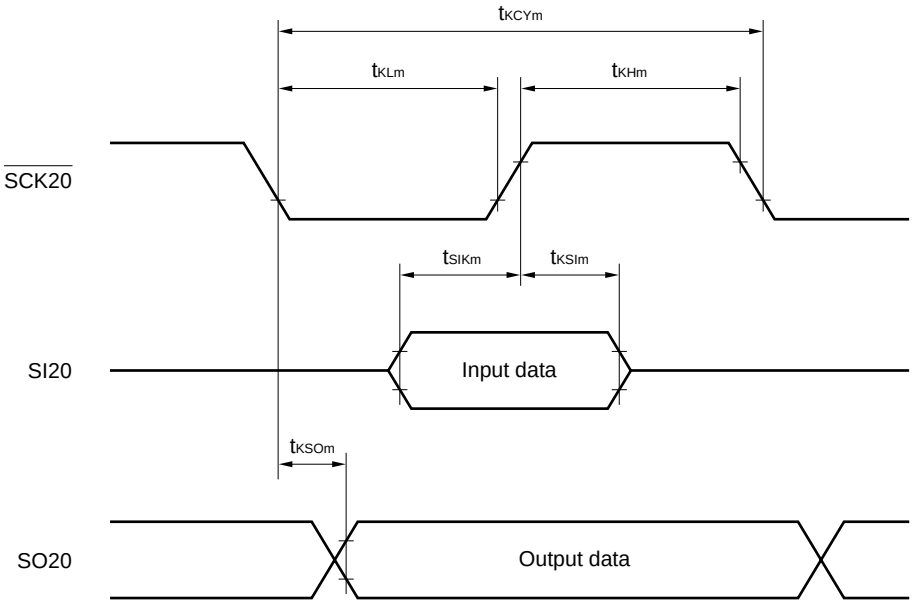


$\overline{\text{RESET}}$ Input Timing



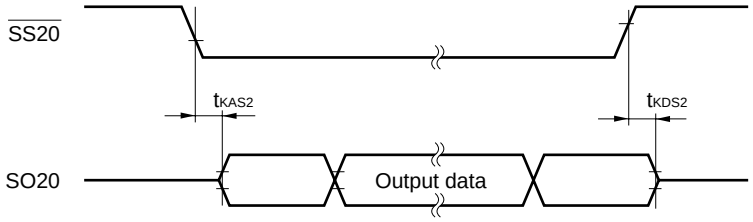
Serial Transfer Timing

3-wire serial I/O mode:

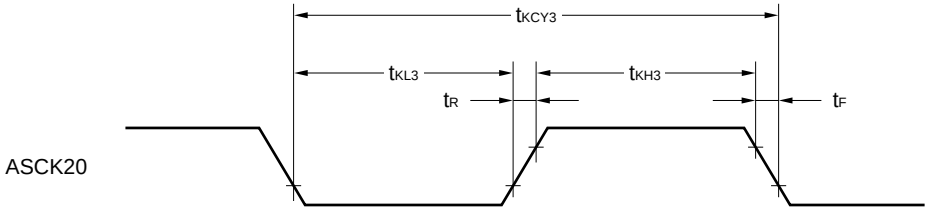


m = 1, 2

3-wire serial I/O mode (when $\overline{SS20}$ is used):



UART mode (external clock input):



8-Bit A/D Converter Characteristics (μPD78912xA(A1), 78912xA(A2) only)

(AV_{DD} = V_{DD} = 4.5 to 5.5 V, AV_{SS} = V_{SS} = 0 V, T_A = –40 to +110°C (μPD78912xA(A1)), –40 to +125°C (μPD78912xA(A2)))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note1,2]				±0.4	±1.0	%FSR
Conversion time	t_{CONV}		14		28	μs
Analog input voltage	V_{IAN}		0		AV_{DD}	V

Notes 1. Excludes quantization error (±0.2%FSR).

2. It is indicated as a ratio to the full-scale value (%FSR).

10-Bit A/D Converter Characteristics (μPD78913xA(A1), 78913xA(A2) only)

(AV_{DD} = V_{DD} = 4.5 to 5.5 V, AV_{SS} = V_{SS} = 0 V, T_A = –40 to +110°C (μPD78913xA(A1)), –40 to +125°C (μPD78913xA(A2)))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note1,2]				±0.4	±0.6	%FSR
Conversion time	t_{CONV}		14		28	μs
Zero-scale error[Note1,2]					±0.6	%FSR
Full-scale error[Note1,2]					±0.6	%FSR
Non-integral linearity error[Note1]	INL				±4.5	LSB
Non-differential linearity error[Note1]	DNL				±2.0	LSB
Analog input voltage	V_{IAN}		0		AV_{DD}	V

Notes 1. Excludes quantization error (±0.05%FSR).

2. It is indicated as a ratio to the full-scale value (%FSR).

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

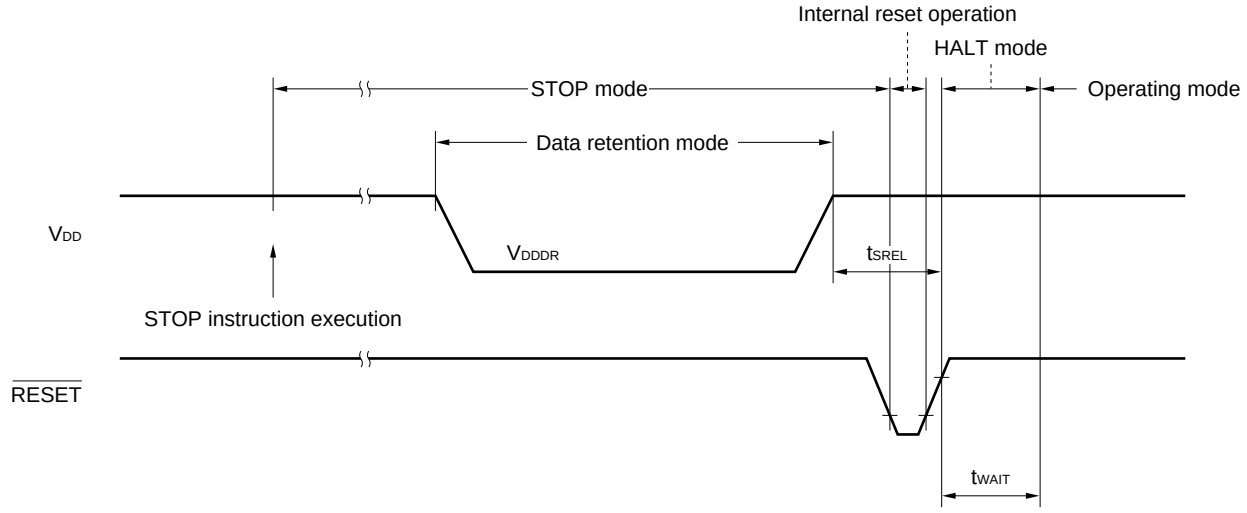
(T_A = –40 to +110°C (μPD78912xA(A1), 78913xA(A1)), –40 to +125°C (μPD78912xA(A2), 78913xA(A2)))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^7/f_{CC}$		ms
		Release by interrupt request		$2^7/f_{CC}$		ms

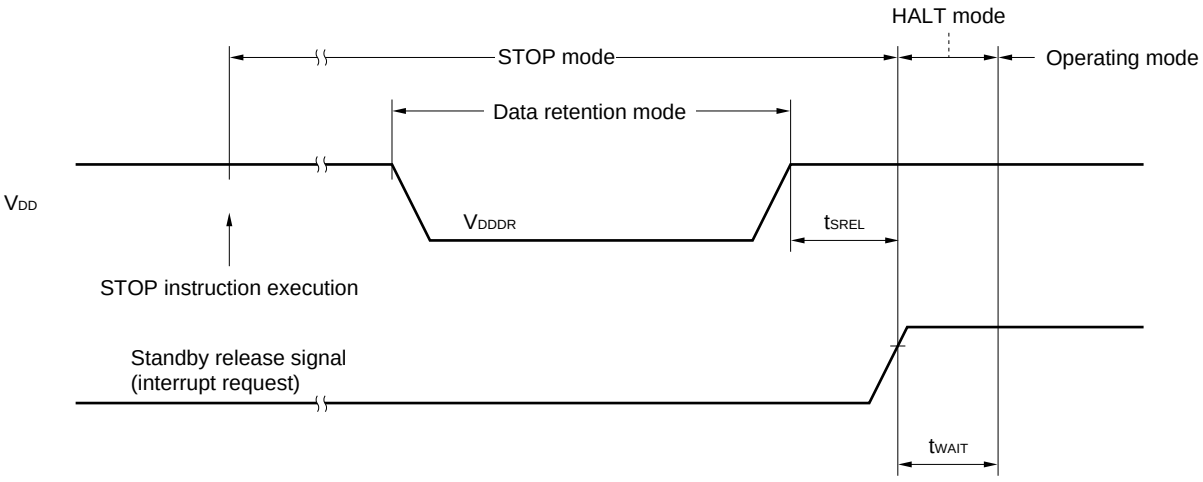
Note The oscillation stabilization wait time is the period during which the CPU operation is stopped to avoid unstable operation at the beginning of oscillation.

Remark f_{CC}: System clock oscillation frequency

Data Retention Timing (STOP mode release by $\overline{\text{RESET}}$)

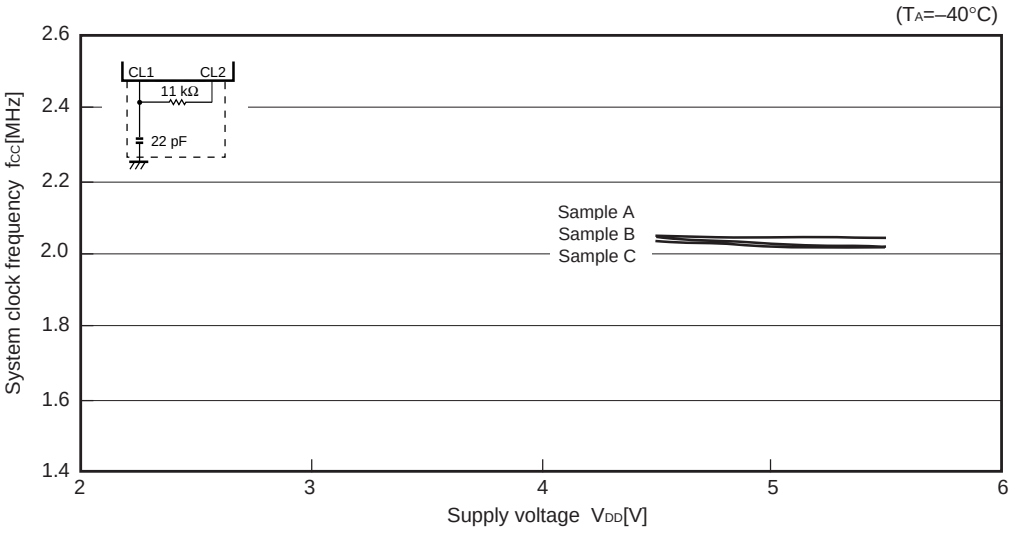


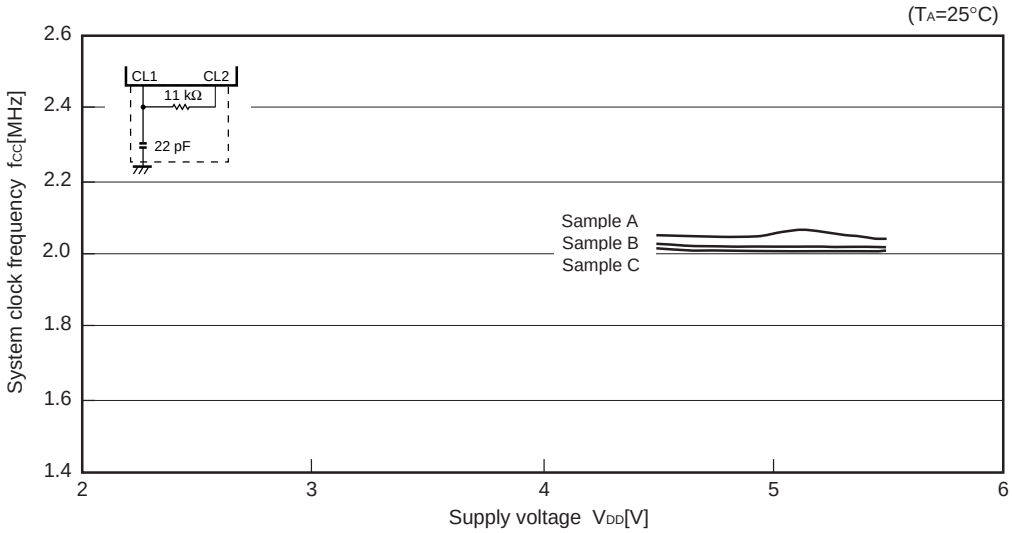
Data Retention Timing (Standby release signal: STOP mode release by interrupt signal)

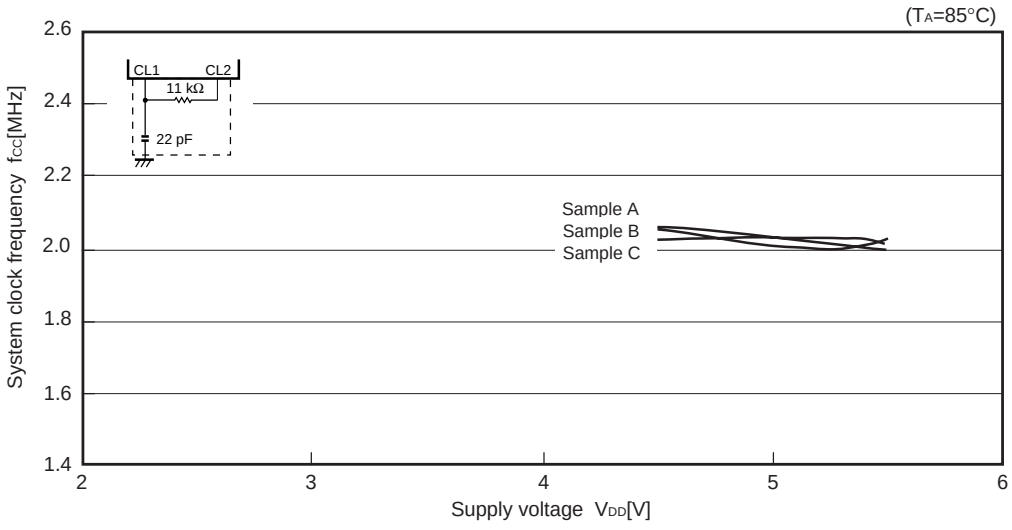


12. EXAMPLE OF RC OSCILLATOR FREQUENCY CHARACTERISTICS (REFERENCE VALUES)

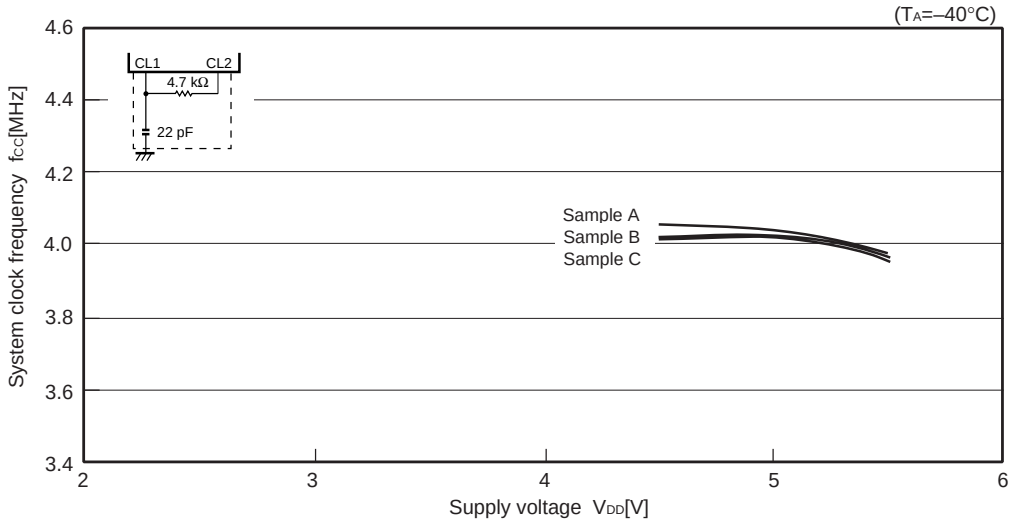
f_{CC} vs V_{DD} (RC Oscillation, R = 11 kΩ, C= 22 pF)

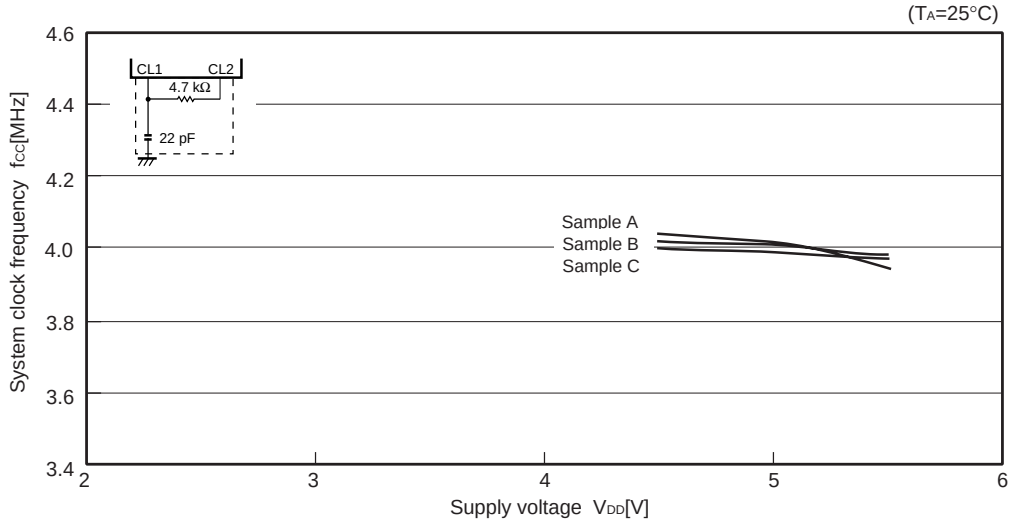


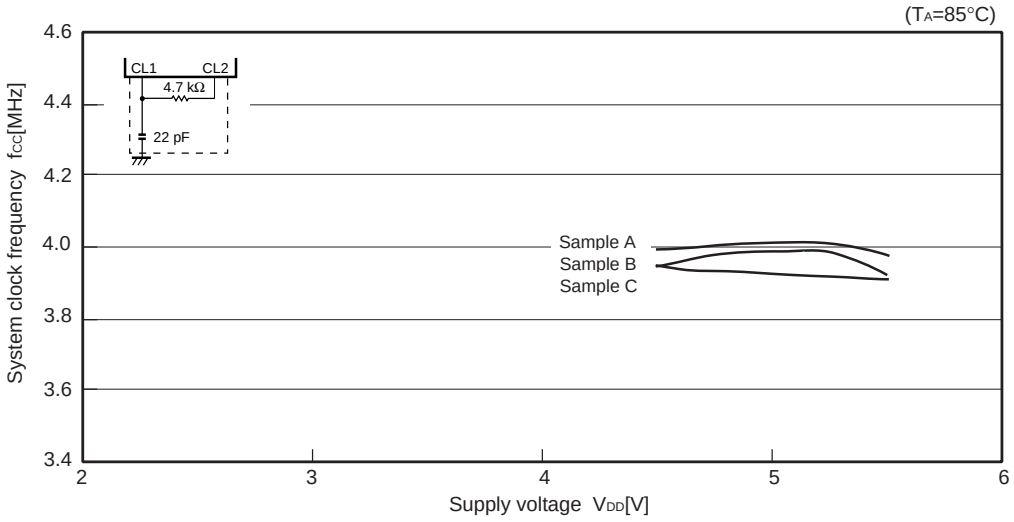




f_{CC} vs V_{DD} (RC Oscillation, R = 4.7 kΩ, C= 22 pF)

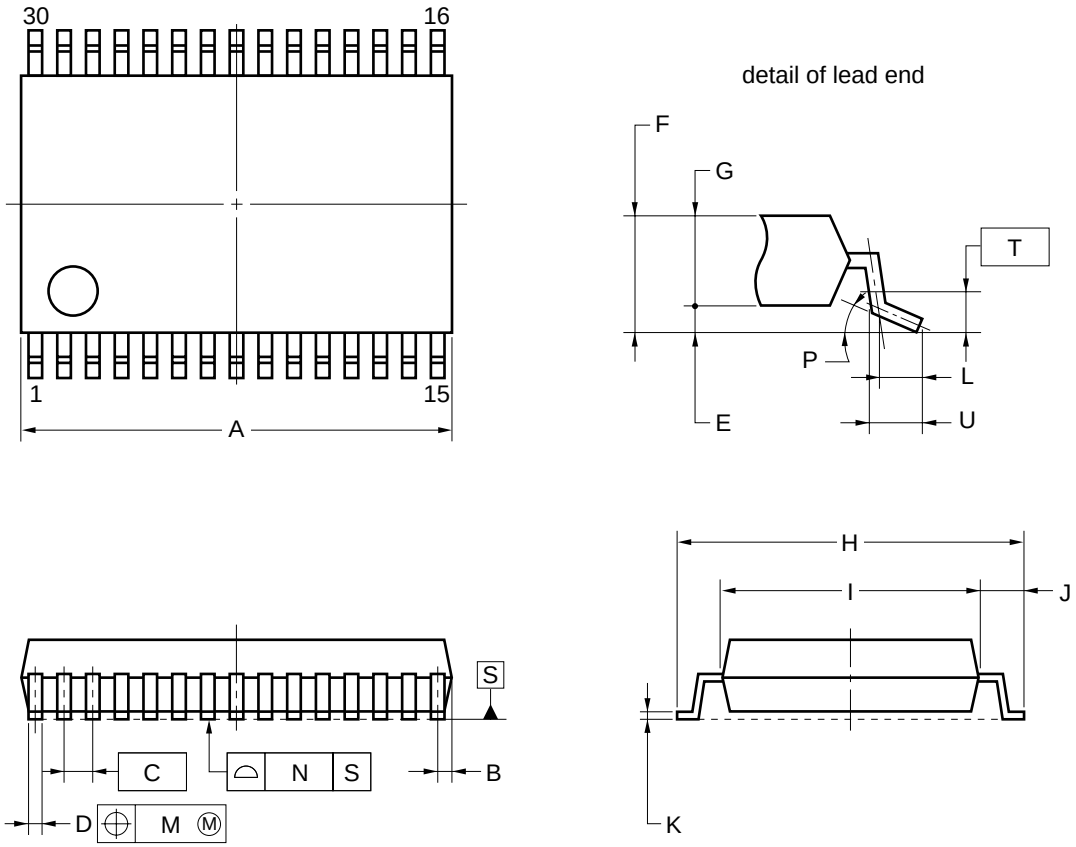






13. PACKAGE DRAWING

30-PIN PLASTIC SSOP (7.62 mm (300))



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.08}_{-0.07}$
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25
U	0.6±0.15

S30MC-65-5A4-2

14. RECOMMENDED SOLDERING CONDITIONS

The μPD78912xA(A1), 78913xA(A1), 78912xA(A2), and 78913xA(A2) should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 14-1. Surface Mounting Type Soldering Conditions

μPD789121AMC(A1)-xxx-5A4: 30-pin plastic SSOP (7.62 mm (300))
μPD789122AMC(A1)-xxx-5A4: 30-pin plastic SSOP (7.62 mm (300))
μPD789124AMC(A1)-xxx-5A4: 30-pin plastic SSOP (7.62 mm (300))
μPD789131AMC(A1)-xxx-5A4: 30-pin plastic SSOP (7.62 mm (300))
μPD789132AMC(A1)-xxx-5A4: 30-pin plastic SSOP (7.62 mm (300))
μPD789134AMC(A1)-xxx-5A4: 30-pin plastic SSOP (7.62 mm (300))
μPD789121AMC(A2)-xxx-5A4: 30-pin plastic SSOP (7.62 mm (300))
μPD789122AMC(A2)-xxx-5A4: 30-pin plastic SSOP (7.62 mm (300))
μPD789124AMC(A2)-xxx-5A4: 30-pin plastic SSOP (7.62 mm (300))
μPD789131AMC(A2)-xxx-5A4: 30-pin plastic SSOP (7.62 mm (300))
μPD789132AMC(A2)-xxx-5A4: 30-pin plastic SSOP (7.62 mm (300))
μPD789134AMC(A2)-xxx-5A4: 30-pin plastic SSOP (7.62 mm (300))

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher), Count: three times or less	IR35-00-3
VPS	Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher), Count: three times or less	VP15-00-3
Wave soldering	Solder bath temperature: 260°C Max., Time: 10 sec. Max., Count: once, Preheating temperature: 120°C Max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C Max., Time: 3 sec. Max. (per pin row)	–

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78912xA(A1), μPD78913xA(A1), μPD78912xA(A2), and μPD78913xA(A2).

Language Processing Software

RA78K0S[Notes 1, 2, 3]	Assembler package common to 78K/0S Series
CC78K0S[Notes 1, 2, 3]	C compiler package common to 78K/0S Series
DF789136[Notes 1, 2, 3]	Device file for μPD789124A, 789134A Subseries

Flash Memory Writing Tools

Flashpro III (Model number: FL-PR3[Note 4], PG-FP3)	Dedicated flash programmer for on-chip flash memory
FA-30MC[Note 4]	Flash memory writing adapter

Debugging Tools (1/2)

IE-78K0S-NS In-circuit emulator	In-circuit emulator serves to debug hardware and software when developing application systems using a 78K/0S Series product. It supports the ID78K0S-NS integrated debugger. Used in combination with an AC adapter, emulation probe, and interface adapter connecting to the host machine.
IE-70000-MC-PS-B AC adapter	Adapter used to supply power from a power outlet of 100 V AC to 240 V AC.
IE-70000-98-IF-C Interface adapter	Adapter when PC-9800 series PC (except notebook type) is used as the IE-78K0S-NS host machine (C bus supported).
IE-70000-CD-IF-A PC card interface	PC card and interface cable when notebook PC is used as the IE-78K0S-NS host machine (PCMCIA socket supported).
IE-70000-PC-IF-C Interface adapter	Adapter when using an IBM PC/AT™ or compatible as the IE-78K0S-NS host machine.
IE-70000-PCI-IF Interface adapter	Adapter when using PC that includes a PCI bus as the IE-78K0S-NS host machine.
IE-789136-NS-EM1 Emulation board	Board for emulation of the peripheral hardware peculiar to a device. Used in combination with an in-circuit emulator.
NP-36GS[Note 4]	Board used to connect the in-circuit emulator to the target system. For a 30-pin plastic SSOP (MC-5A4 type), used in combination with NGS-30.
NGS-30[Note 4] Conversion socket	Conversion socket used to connect the NP-36GS to the target system board designed to mount a 30-pin plastic SSOP (MC-5A4 type).

Notes 1. PC-9800 series (Japanese Windows™) based

2. IBM PC/AT or compatibles (Japanese/English Windows) based

3. HP9000 series 700™ (HP-UX™), SPARCstation™ (SunOS™, Solaris™), or NEWS™ (NEWS-OS™) based.

4. Products made by Naito Densei Machida Mfg. Co., Ltd. (Phone: +81-44-822-3813). Contact an NEC distributor regarding the purchase of these products.

Remark RA78K0S, CC78K0S, and SM78K0S are used in combination with the DF789136.

Debugging Tools (2/2)

SM78K0S[Notes 1, 2]	System simulator common to 78K/0S Series
ID78K0S-NS[Notes 1, 2]	Integrated debugger common to 78K/0S Series
DF789136[Notes 1, 2]	Device file for μPD789124A, 789134A Subseries

Real-time OS

MX78K0S[Notes 1, 2]	OS for 78K/0S Series

Notes 1. PC-9800 series (Japanese Windows) based.

2. IBM PC/AT or compatibles (Japanese/English Windows) based.

APPENDIX B RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD789121A, 122A, 124A, 131A, 132A, 134A, 121A(A), 122A(A), 124A(A), 131A(A), 132A(A), 134A(A) Data Sheet	U14678E
μPD78F9136A Data Sheet	U14690E
μPD789121A(A1), 122A(A1), 124A(A1), 131A(A1), 132A(A1), 134A(A1), 121A(A2), 122A(A2), 124A(A2), 131A(A2), 132A(A2), 134A(A2) Data Sheet	This manual
μPD789104A, 789114A, 789124A, 789134A Subseries User's Manual	U14643E
78K/0S Series User's Manual Instruction	U11047E
78K/0, 78K/0S Series Application Note Flash Memory Write	U14458E

Documents Related to Development Tools (User's Manuals)

Document Name		Document No.
RA78K0S Assembler Package	Operation	U11622E
	Assembly Language	U11599E
	Structured Assembly Language	U11623E
CC78K0S C Compiler	Operation	U11816E
	Language	U11817E
SM78K0S System Simulator Windows Based	Reference	U11489E
SM78K Series System Simulator	External Parts User Open Interface Specifications	U10092E
ID78K0S-NS Integrated Debugger Windows Based	Reference	U12901E
ID78K0-NS, ID78K0S-NS Integrated Debugger Ver.2.20 or Later Windows Based	Operation	U14910E
IE-78K0S-NS In-circuit Emulator		U13549E
IE-789136-NS-EM1 Emulation Board		U14363E

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No.
78K/0S Series OS MX78K0S	Fundamental	U12938E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Other Related Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E
Guide to Microcomputer-Related Products by Third Party	–

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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