NEC

MOS INTEGRATED CIRCUITS

μPD789166,167,176,177,166Y,167Y,176Y,177Y,166(A),167(A), 176(A),177(A),166Y(A),167Y(A),176Y(A),177Y(A)

8-BIT SINGLE-CHIP MICROCONTROLLERS

The μPD789166, 789167, 789176, and 789177 (hereafter, represented as μPD78916x and μPD78917x) are μPD789167, 789177 Subseries (small, general-purpose) in the 78K/0S Series. The μPD789166Y, 789167Y, 789176Y, and 789177Y (hereafter, represented as μPD78916xY and μPD78917xY) are μPD789167Y, 789177Y Subseries (small, general-purpose) in the 78K/0S Series.

A stricter quality assurance program (called special grade in NEC's grade classification) is applied to the μPD789166(A), 789167(A), 789176(A), 789177(A) (hereafter, represented as μPD78916x(A) and μPD78917x(A)), and μPD789166Y(A), 789167Y(A), 789176Y(A), 789177Y(A) (hereafter, represented as μPD78916xY(A) and μPD78917xY(A)), compared to the μPD78916x, 78917x, 78916xY, and 78917xY, which are classified as standard grade.

In addition, a flash memory version (μPD78F9177, 78F9177Y) that can operate within the same power supply voltage range as the mask ROM version, and a range of development tools are also being prepared.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD789167, 789177, 789167Y, 789177Y Subseries User's Manual: U14186E
78K/0S Series User's Manual Instruction: U11047E

FEATURES

- ROM and RAM sizes

Part Number \ Item	Program Memory (ROM)	Data Memory (Internal High-Speed RAM)
μPD789166, 789176, 789166Y, 789176Y, 789166(A), 789176(A), 789166Y(A), 789176Y(A)	16 Kbytes	512 bytes
μPD789167, 789177, 789167Y, 789177Y, 789167(A), 789177(A), 789167Y(A), 789177Y(A)	24 Kbytes	

★

- Minimum instruction execution time can be changed from high-speed (0.2 μs @10.0-MHZ operation with main system clock, V_{DD} = 4.5 to 5.5 V) to ultra-low-speed (122 μs @ 32.768-kHz operation with subsystem clock)
- 8-bit resolution A/D converter: 8 channels (μPD78916x, 78916xY, 78916x(A), 78916xY(A))
- 10-bit resolution A/D converter: 8 channels (μPD78917x, 78917xY, 78917x(A), 78917xY(A))
- On chip 16-bit multiplier
- I/O ports: 31
- Power supply voltage: V_{DD} = 1.8 to 5.5 V
- Serial interface: 2 channels
- 3-wire serial I/O mode / UART mode: 1 channel
- SMB(μPD78916xY, 78917xY, 78916xY(A), and 78917xY(A) only): 1 channel
- Timers: 6 channels
- 16-bit timer: 1 channel
- 8-bit timer/event counter: 2 channels
- 8-bit timer: 1 channel
- Watchdog timer: 1 channel
- Watch timer: 1 channel

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The mark ★ shows major revised points.

APPLICATIONS

Power windows, keyless entry, battery management unit, side air bags, etc

ORDERING INFORMATION

(1) μPD78916x, 78917x, 78916x(A), 78917x(A)

Part Number	Package	Quality grade
μPD789166GB-×××-8ES	44-pin plastic LQFP (10 × 10 mm)	Standard
μPD789167GB-×××-8ES	44-pin plastic LQFP (10 × 10 mm)	Standard
μPD789176GB-×××-8ES	44-pin plastic LQFP (10 × 10 mm)	Standard
μPD789177GB-×××-8ES	44-pin plastic LQFP (10 × 10 mm)	Standard
μPD789166GB(A)-×××-8ES	44-pin plastic LQFP (10 × 10 mm)	Special
μPD789167GB(A)-×××-8ES	44-pin plastic LQFP (10 × 10 mm)	Special
μPD789176GB(A)-×××-8ES	44-pin plastic LQFP (10 × 10 mm)	Special
μPD789177GB(A)-×××-8ES	44-pin plastic LQFP (10 × 10 mm)	Special

Remark ××× indicates ROM code suffix.

(2) μPD78916xY, 78917xY, 78916xY(A), 78917xY(A)

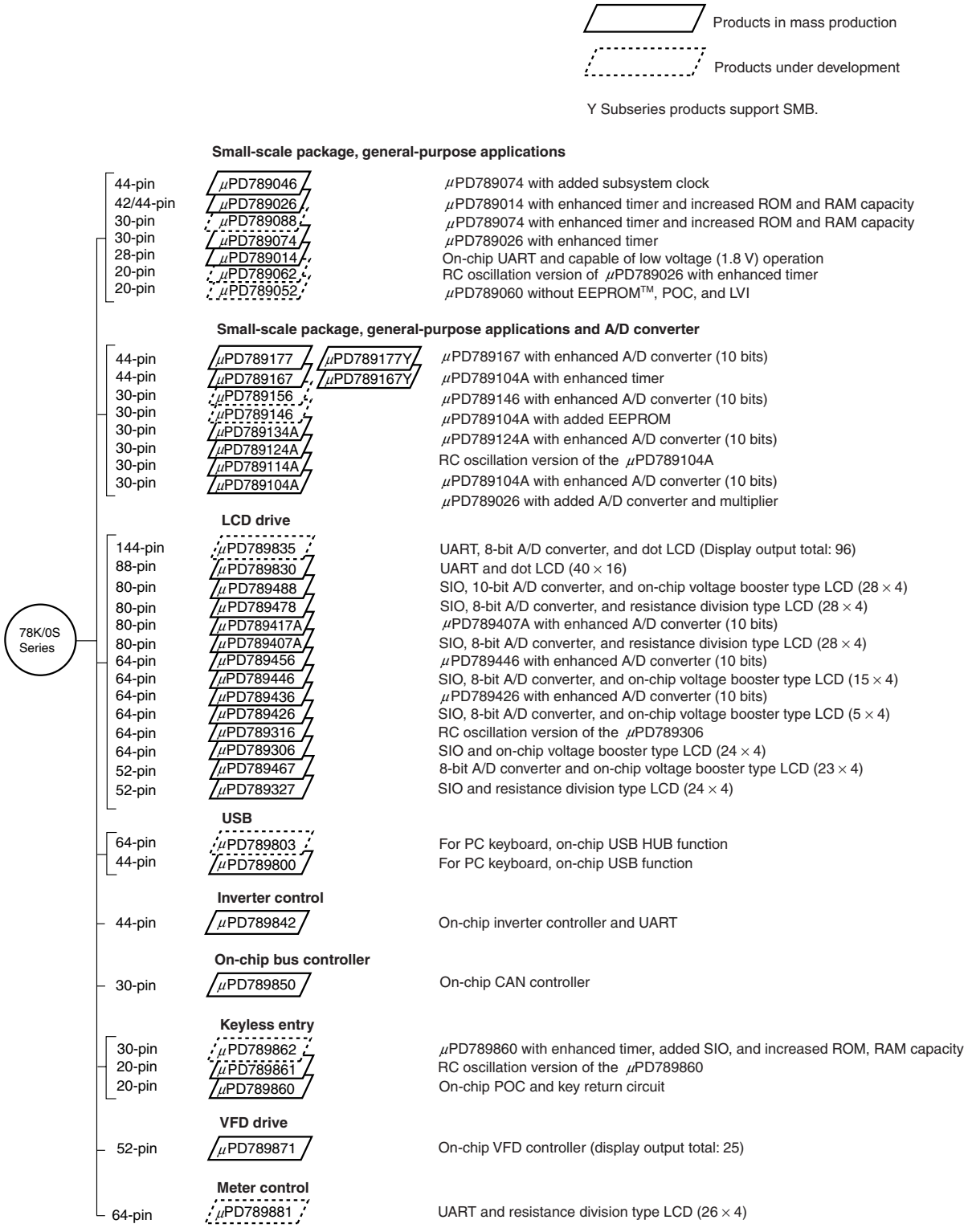
Part Number	Package	Quality grade
μPD789166YGB-×××-8ES	44-pin plastic LQFP (10 × 10 mm)	Standard
μPD789166YGA-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7 mm)	Standard
μPD789167YGB-×××-8ES	44-pin plastic LQFP (10 × 10 mm)	Standard
μPD789167YGA-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7 mm)	Standard
μPD789176YGB-×××-8ES	44-pin plastic LQFP (10 × 10 mm)	Standard
μPD789176YGA-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7 mm)	Standard
μPD789177YGB-×××-8ES	44-pin plastic LQFP (10 × 10 mm)	Standard
μPD789177YGA-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7 mm)	Standard
μPD789166YGA(A)-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7 mm)	Special
μPD789167YGA(A)-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7 mm)	Special
μPD789176YGA(A)-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7 mm)	Special
μPD789177YGA(A)-×××-9EU	48-pin plastic TQFP (fine pitch) (7 × 7 mm)	Special

Remark ××× indicates ROM code suffix.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

★ 78K/0S SERIES LINEUP

The products in the 78K/0S Series are listed below. The names enclosed in boxes are subseries names.



Remark VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major differences between subseries are shown below.

Series for LCD drive, general-purpose applications

Function / Subseries Name		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_{DD} MIN. Value	Remarks
			8-Bit	16-Bit	Watch	WDT						
Small-scale package, general-purpose applications	μPD789046	16 KB	1 ch	1 ch	1 ch	1 ch	–	–	1 ch (UART: 1 ch)	34	1.8 V	–
	μPD789026	4 KB to 16 KB			–							
	μPD789088	16 KB to 32 KB	3 ch							24		
	μPD789074	2 KB to 8 KB	1 ch									
	μPD789014	2 KB to 4 KB	2 ch	–						22		
	μPD789062	4 KB							–	14		RC oscillation version
	μPD789052											–
Small-scale package, general-purpose applications and A/D converter	μPD789177	16 KB to 24 KB	3 ch	1 ch	1 ch	1 ch	–	8 ch	1 ch (UART: 1 ch)	31	1.8 V	–
	μPD789167						8 ch	–				
	μPD789156	8 KB to 16 KB	1 ch		–		–	4 ch		20		On-chip EEPROM
	μPD789146						4 ch	–				
	μPD789134A	2 KB to 8 KB					–	4 ch				RC oscillation version
	μPD789124A						4 ch	–				
	μPD789114A						–	4 ch				–
	μPD789104A						4 ch	–				
LCD drive	μPD789835	24 KB to 60 KB	6 ch	–	1 ch	1 ch	3 ch	–	1 ch (UART: 1 ch)	37	1.8 V Note	Dot LCD supported
	μPD789830	24 KB	1 ch	1 ch			–			30	2.7 V	
	μPD789488	32 KB	3 ch					8 ch	2 ch (UART: 1 ch)	45	1.8 V	–
	μPD789478	24 KB to 32 KB					8 ch	–				
	μPD789417A	12 KB to 24 KB					–	7 ch	1 ch (UART: 1 ch)	43		
	μPD789407A						7 ch	–				
	μPD789456	12 KB to 16 KB	2 ch				–	6 ch		30		
	μPD789446						6 ch	–				
	μPD789436						–	6 ch		40		
	μPD789426						6 ch	–				
	μPD789316	8 KB to 16 KB					–		2 ch (UART: 1 ch)	23		RC oscillation version
	μPD789306											–
	μPD789467	4 KB to 24 KB		–			1 ch		–	18		
	μPD789327						–		1 ch	21		

Note Flash memory version: 3.0 V

Series for ASSP

Subseries Name \ Function		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	Serial Interface	I/O	V_{DD} MIN. Value	Remarks
			8-Bit	16-Bit	Watch	WDT						
USB	μPD789803	8 KB to 16 KB	2 ch	–	–	1 ch	–	–	2 ch (USB: 1 ch)	41	3.6 V	–
	μPD789800	8 KB								31	4.0 V	
Inverter control	μPD789842	8 KB to 16 KB	3 ch	**Note 1**	1 ch	1 ch	8 ch	–	1 ch (UART: 1 ch)	30	4.0 V	–
On-chip bus controller	μPD789850	16 KB	1 ch	1 ch	–	1 ch	4 ch	–	2 ch (UART: 1 ch)	18	4.0 V	–
Keyless entry	μPD789861	4 KB	2 ch	–	–	1 ch	–	–	–	14	1.8 V	RC oscillation version, on-chip EEPROM
	μPD789860											On-chip EEPROM
	μPD789862	16 KB	1 ch	2 ch					1 ch (UART: 1 ch)	22		
VFD drive	μPD789871	4 KB to 8 KB	3 ch	–	1 ch	1 ch	–	–	1 ch	33	2.7 V	–
Meter control	μPD789881	16 KB	2 ch	1 ch	–	1 ch	–	–	1 ch (UART: 1 ch)	28	2.7 V **Note 2**	–

Notes 1. 10-bit timer: 1 channel

2. Flash memory version: 3.0 V

OVERVIEW OF FUNCTIONS

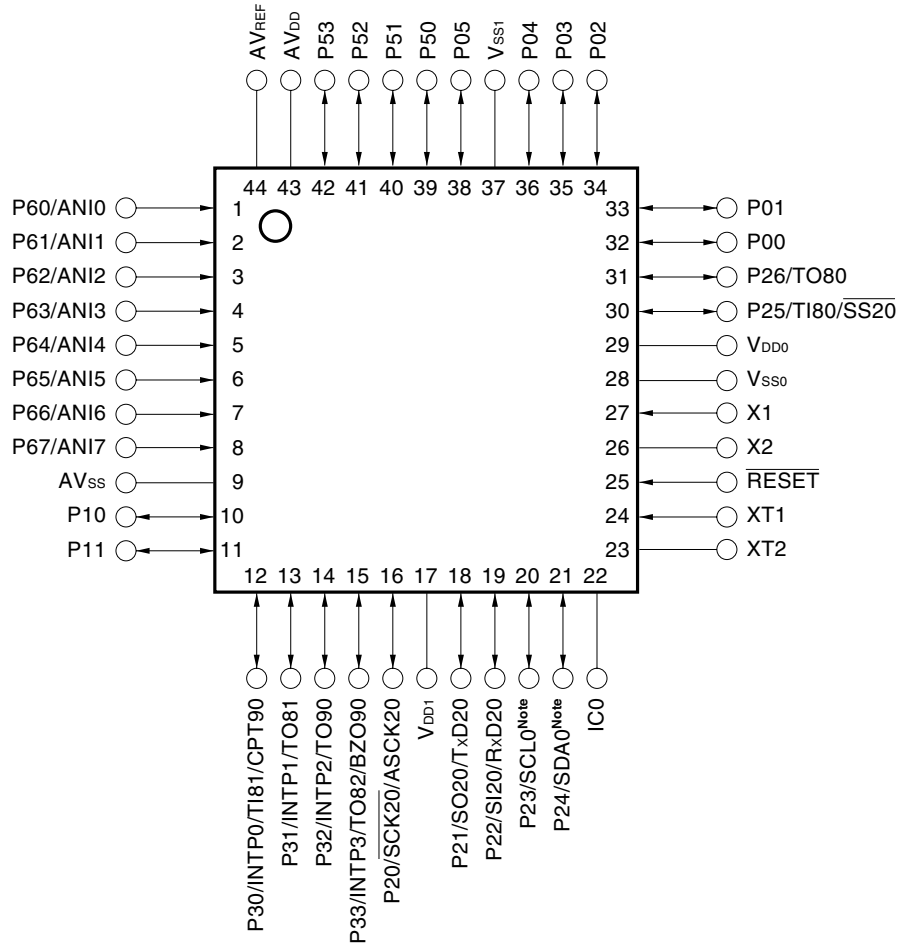
Item		μPD789166,789176 μPD789166Y,789176Y μPD789166(A),789176(A) μPD789166Y(A), 789176Y(A)	μPD789167,789177 μPD789167Y,789177Y μPD789167(A),789177(A) μPD789167Y(A), 789177Y(A)
Internal memory	ROM	16 KB	24 KB
	High-speed RAM	512 bytes	
★ Minimum instruction execution time		• 0.2/0.8 μs (@ 10.0-MHz operation with main system clock, V_{DD} = 4.5 to 5.5 V) • 122 μs (@ 32.768-kHz operation with subsystem clock)	
General-purpose registers		8 bits × 8 registers	
Instruction set		• 16-bit operations • Bit manipulations (set, reset, and test)	
Multiplier		8 bits × 8 bits = 16 bits	
I/O ports		Total: 31 • CMOS input: 8 • CMOS I/O: 17 • N-ch open-drain (12-V withstand voltage): 6	
A/D converters		• 8-bit resolution × 8 channels (μPD78916x, 78916xY, 78916x(A), 78916xY(A)) • 10-bit resolution × 8 channels (μPD78917x, 78917xY, 78917x(A), 78917xY(A))	
Serial interfaces		• 3-wire serial I/O / UART: 1 channel • SMB: 1 channel (μPD78916xY, 78917xY, 78916xY(A), 78917xY(A))	
Timers		• 16-bit timer: 1 channel • 8-bit timer/event counter: 2 channels • 8-bit timer: 1 channel • Watchdog timer: 1 channel • Watch timer: 1 channel	
Timer output		4 output (16-bit/8-bit timer alternate function: 1)	
Vectored interrupt sources	Maskable	Internal: 10, External: 4 (μPD78916x, 78917x, 78916x(A), 78917x(A))	
		Internal: 12, External: 4 (μPD78916xY, 78917xY, 78916xY(A), 78917xY(A))	
	Non-maskable	Internal: 1	
Power supply voltage		V_{DD} = 1.8 to 5.5 V	
Operating ambient temperature		T_A = –40 to +85°C	
Package		• 44-pin plastic LQFP (10 × 10 mm) • 48-pin plastic TQFP (fine pitch) (7 × 7 mm) (μPD78916xY, 78917xY, 78916xY(A), 78917xY(A) only)	

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- 44-pin plastic LQFP (10 × 10 mm)

  μPD789166GB-×××-8ES　　μPD789166GB(A)-×××-8ES
  μPD789167GB-×××-8ES　　μPD789167GB(A)-×××-8ES
  μPD789176GB-×××-8ES　　μPD789176GB(A)-×××-8ES
  μPD789177GB-×××-8ES　　μPD789177GB(A)-×××-8ES
  μPD789166YGB-×××-8ES
  μPD789167YGB-×××-8ES
  μPD789176YGB-×××-8ES
  μPD789177YGB-×××-8ES



Note The SCL0 and SDA0 pins are available in μPD78916xY and 78917xY products only.

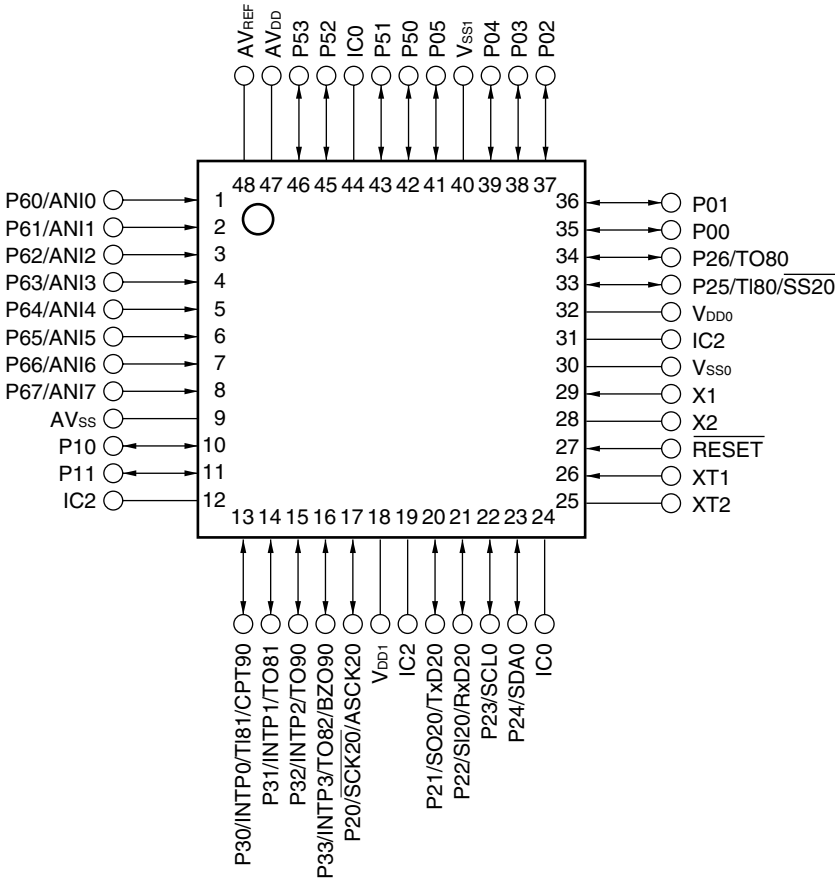
Cautions 1. Connect the IC0 (Internally Connected) pin directly to V_{SS0} or V_{SS1}.

2. Connect the AV_{DD} pin to V_{DD0}.

3. Connect the AV_{SS} pin to V_{SS0}.

- 48-pin plastic TQFP (fine pitch) (7 × 7 mm)

  μPD789166YGA-×××-9EU μPD789166YGA(A)-×××-9EU
  μPD789167YGA-×××-9EU μPD789167YGA(A)-×××-9EU
  μPD789176YGA-×××-9EU μPD789176YGA(A)-×××-9EU
  μPD789177YGA-×××-9EU μPD789177YGA(A)-×××-9EU



Cautions 1. Connect the IC0 (Internally Connected) pin directly to V_{SS0} or V_{SS1}.

2. Leave the IC2 pin open.

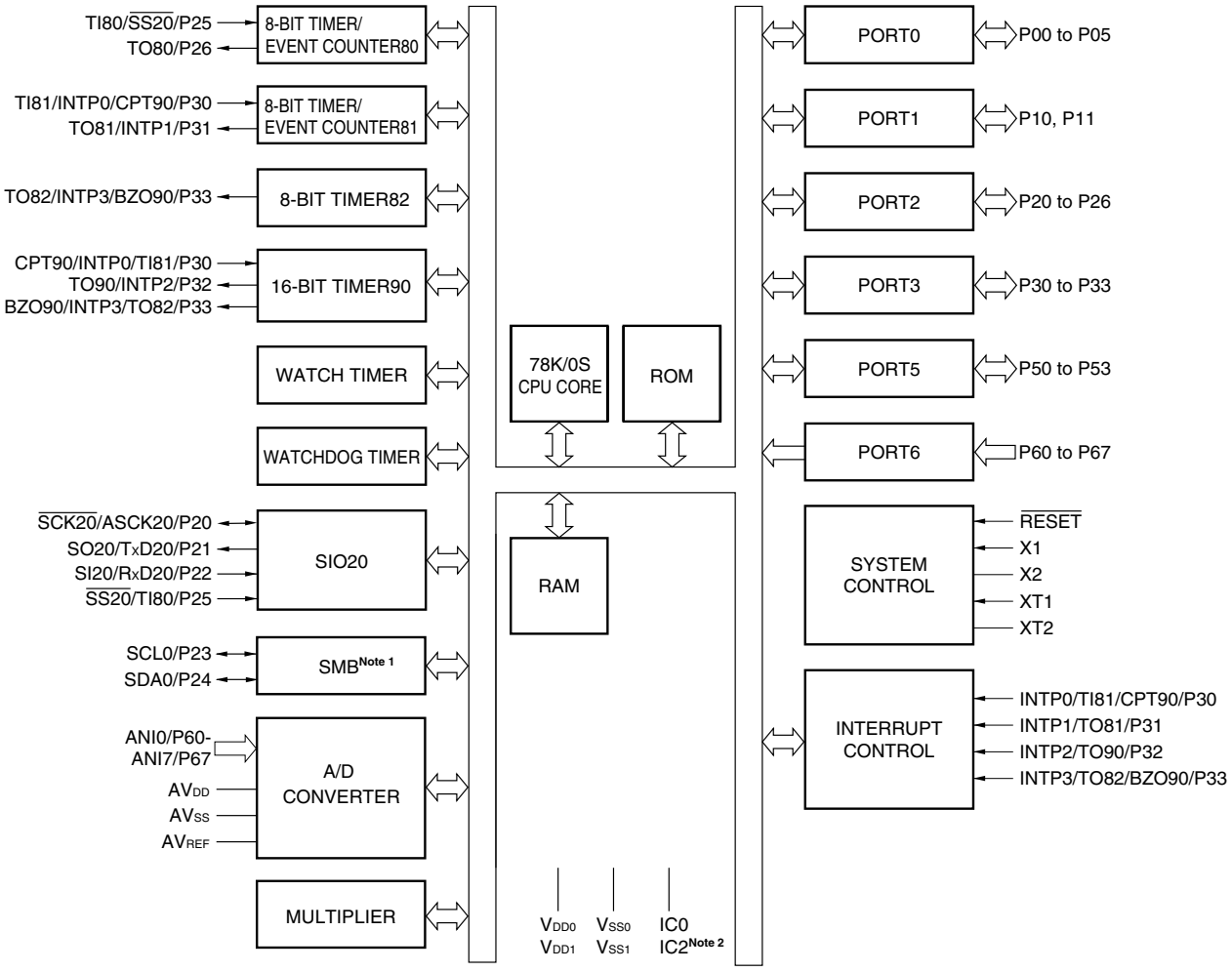
3. Connect the AV_{DD} pin to V_{DD0}.

4. Connect the AV_{SS} pin to V_{SS0}.

ANI0 to ANI7:	Analog input	$\overline{\text{RESET}}$:	Reset
ASCK20:	Asynchronous serial input	RxD20:	Receive data
AV_{DD}:	Analog power supply	$\overline{\text{SCK20}}$:	Serial clock (for SIO20)
AV_{REF}:	Analog reference voltage	SCL0[Note]:	Serial clock (for SMB0)
AV_{SS}:	Analog ground	SDA0[Note]:	Serial data
BZO90:	Buzzer output	SI20:	Serial input
CPT90:	Capture trigger input	SO20:	Serial output
IC0, IC2[Note]:	Internally connected	$\overline{\text{SS20}}$:	Chip select input
INTP0 to INTP3:	Interrupt from peripherals	TI80, TI81:	Timer input
P00 to P05:	Port 0	TO80 to TO82, TO90:	Timer output
P10, P11:	Port 1	TxD20:	Transmit data
P20 to P26:	Port 2	V_{DD0}, V_{DD1}:	Power supply
P30 to P33:	Port 3	V_{SS0}, V_{SS1}:	Ground
P50 to P53:	Port 5	X1, X2:	Crystal (main system clock)
P60 to P67:	Port 6	XT1, XT2:	Crystal (subsystem clock)

Note The IC2, SCL0, and SDA0 pins are available in μPD78916xY, 78917xY, 78916xY(A), and 78917xY(A) products only.

2. BLOCK DIAGRAM



Notes 1. SMB is available in μPD78916xY, 78917xY, 78916xY(A), and 78917xY(A) products only.

2. The IC2 pin is available in μPD78916xY, 78917xY, 78916xY(A), and 78917xY(A) products only.

Remark The internal ROM capacity varies depending on the product.

3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P05	I/O	Port 0 6-bit input/output port Input/output mode can be specified in 1-bit units When used as an input port, an on-chip pull-up resistor can be used by setting software.	Input	–
P10, P11	I/O	Port 1 2-bit input/output port Input/output mode can be specified in 1-bit units When used as an input port, an on-chip pull-up resistor can be used by setting software.	Input	–
P20	I/O	Port 2 7-bit input/output port Input/output mode can be specified in 1-bit units For P20 to P22, P25, and P26, an on-chip pull-up resistor can be used by setting software. Only P23 and P24 can be used as N-ch open-drain input/output port pins.	Input	$\overline{SCK20}$/ASCK20
P21				SO20/TxD20
P22				SI20/RxD20
P23				SCL0 Note
P24				SDA0 Note
P25				TI80/$\overline{SS20}$
P26				TO80
P30	I/O	Port 3 4-bit input/output port Input/output mode can be specified in 1-bit units An on-chip pull-up resistor can be used by setting software.	Input	INTP0/TI81/CPT90
P31				INTP1/TO81
P32				INTP2/TO90
P33				INTP3/TO82/BZO90
P50 to P53	I/O	Port 5 4-bit N-ch open-drain input/output port Input/output mode can be specified in 1-bit units An on-chip pull-up resistor can be specified by the mask option.	Input	–
P60 to P67	Input	Port 6 8-bit input-only port	Input	ANI0 to ANI7

Note μPD78916xY, 78917xY, 78916xY(A), and 78917xY(A) only

3.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P30/TI81/CPT90
INTP1				P31/TO81
INTP2				P32/TO90
INTP3				P33/TO82/BZO90
SI20	Input	Serial data input to serial interface	Input	P22/RxD20
SO20	Output	Serial data output from serial interface	Input	P21/TxD20
$\overline{\text{SCK20}}$	I/O	Serial clock input/output for serial interface	Input	P20/ASCK20
$\overline{\text{SS20}}$	Input	Chip select input to serial interface	Input	P25/TI80
ASCK20	Input	Serial clock input for asynchronous serial interface	Input	P20/$\overline{\text{SCK20}}$
RxD20	Input	Serial data input for asynchronous serial interface	Input	P22/SI20
TxD20	Output	Serial data output for asynchronous serial interface	Input	P21/SO20
SCL0**Note**	I/O	SMB0 clock input/output	Input	P23
SDA0**Note**	I/O	SMB0 data input/output	Input	P24
TI80	Input	External count clock input to 8-bit timer/event counter (TM80)	Input	P25/$\overline{\text{SS20}}$
TI81	Input	External count clock input to 8-bit timer/event counter (TM81)	Input	P30/INTP0/CPT90
TO80	Output	8-bit timer/event counter (TM80) output	Input	P26
TO81	Output	8-bit timer/event counter (TM81) output	Input	P31/INTP1
TO82	Output	8-bit timer (TM82) output	Input	P33/INTP3/BZO90
TO90	Output	16-bit timer (TM90) output	Input	P32/INTP2
BZO90	Output	16-bit timer Buzzer output	Input	P33/INTP3/TO82
CPT90	Input	Capture edge input	Input	P30/INTP0/TI81
ANI0 to ANI7	Input	A/D converter analog input	Input	P60 to P67
AV_{REF}	–	A/D converter reference voltage	–	–
AV_{SS}	–	A/D converter ground potential	–	–
AV_{DD}	–	A/D converter analog power supply	–	–
X1	Input	Connecting crystal resonator for main system clock oscillation	–	–
X2	–		–	–
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	–	–
XT2	–		–	–
V_{DD0}	–	Positive power supply	–	–
V_{DD1}	–	Positive power supply (other than ports)	–	–
V_{SS0}	–	Ground potential	–	–
V_{SS1}	–	Ground potential (other than ports)	–	–
$\overline{\text{RESET}}$	Input	System reset input	Input	–
IC0	–	Internally connected. Connect this pin directly to the V_{SS0} or V_{SS1} pin.	–	–
IC2**Note**	–	Internally connected. Leave this pin open.	–	–

Note μPD78916xY, 78917xY, 78916xY(A), 78917xY(A) only.

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

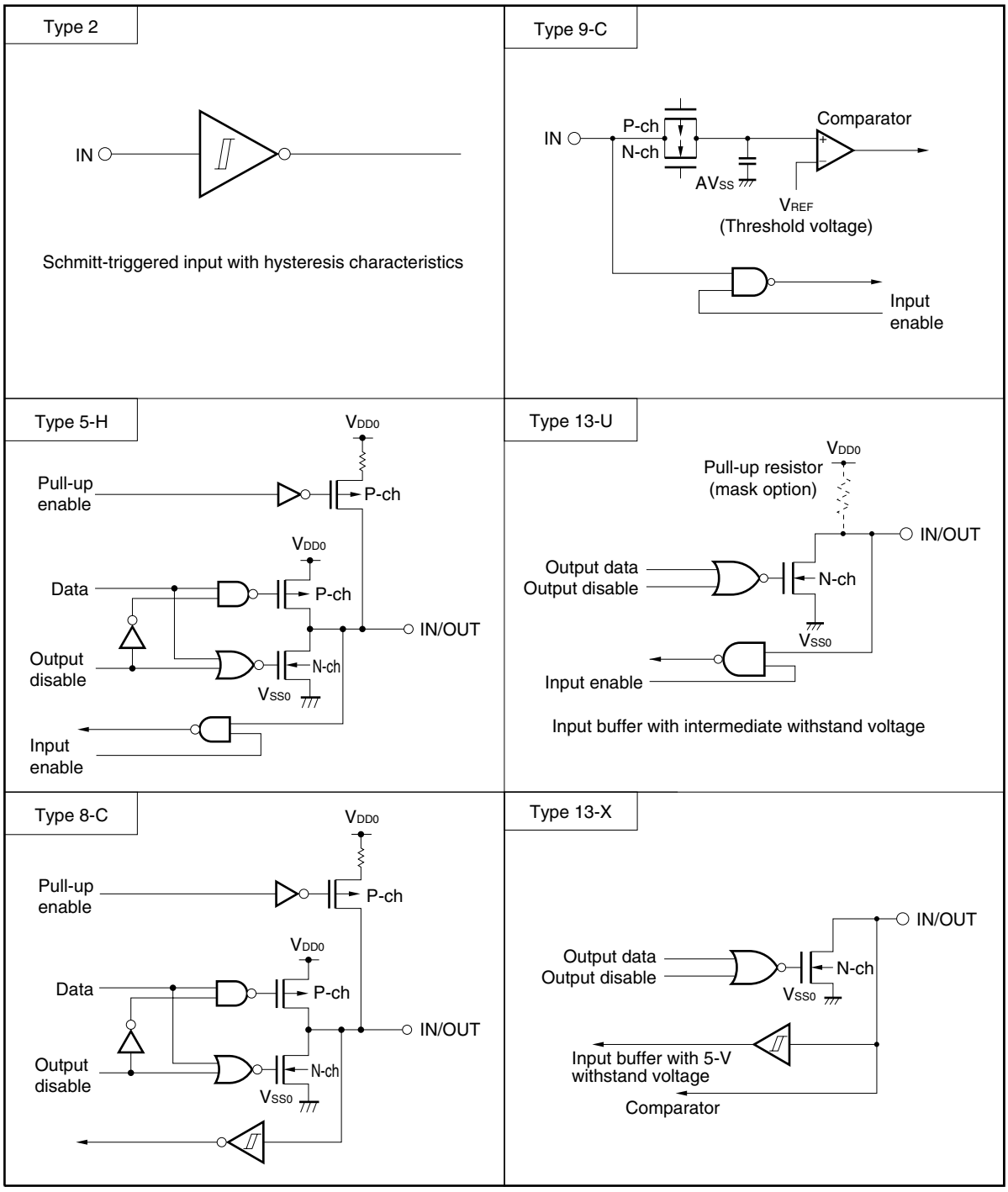
The input/output circuit type of each pin and recommended connection of unused pins is shown in Table 3-1. For the input/output circuit configuration of each type, refer to **Figure 3-1**.

Table 3-1. Types of Pin Input/Output Circuits

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00 to P05	5-H	I/O	Input: Independently connects to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via a resistor. Output: Leave open.
P10, P11			
P20/$\overline{SCK20}$/ASCK20	8-C		
P21/SO20/TxD20			
P22/SI20/RxD20			
P23/SCL0[Note]	13-X		Input: Independently connects to V_{DD0} or V_{DD1} via a resistor. Output: Leave open.
P24/SDA0[Note]			
P25/TI80/$\overline{SS20}$	8-C		Input: Independently connects to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1} via a resistor. Output: Leave open.
P26/TO80			
P30/INTP0/TI81/CPT90			Input: Independently connects to V_{SS0} or V_{SS1} via a resistor. Output: Leave open.
P31/INTP1/TO81			
P32/INTP2/TO90			
P33/INTP3/TO82/BZO90			
P50 to P53	13-U		Input: Independently connects to V_{DD0} or V_{DD1} via a resistor. Output: Leave open.
P60/ANI0 to P67/ANI7	9-C	Input	Connect directly to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1}.
★ AV_{REF}	–	–	Connect directly to V_{DD0}, V_{DD1}, V_{SS0}, or V_{SS1}.
★ AV_{DD}			Connect directly to V_{DD0} or V_{DD1}.
★ AV_{SS}			Connect directly to V_{SS0} or V_{SS1}.
XT1		Input	Connect to V_{SS0} or V_{SS1}.
XT2		–	Leave open.
$\overline{RESET}$	2	Input	–
IC0	–	–	Connect directly to V_{SS0} or V_{SS1}.
IC2[Note]			Leave open.

Note The IC2, SCL0, and SDA0 pins are available in μPD78916xY, 78917xY, 78916xY(A), and 78917xY(A) products only.

Figure 3-1. Pin Input/Output Circuits

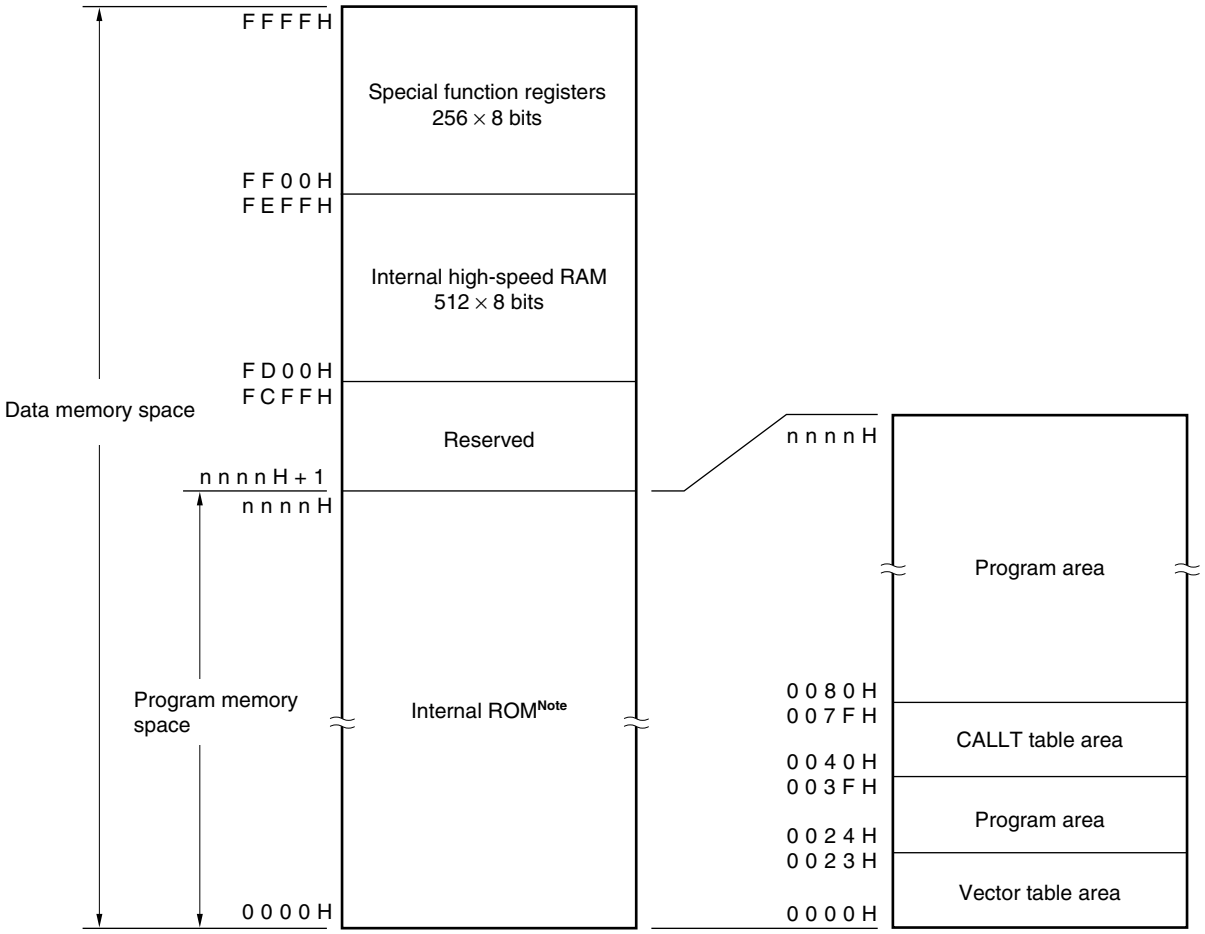


4. MEMORY SPACE

Products in the μPD78916x, 78917x, 78916xY, 78917xY, 78916x(A), 78917x(A), 78916xY(A), and 78917xY(A) can access up to 64 Kbytes of memory space.

Figure 4-1 shows the memory map.

Figure 4-1. Memory Map



Note The internal ROM capacity depends on the product. (See the following table.)

Part Number	Last Address of Internal ROM nnnnH
μPD789166, 789176, 789166Y, 789176Y, 789166(A), 789176(A), 789166Y(A), 789176Y(A)	3FFFH
μPD789167, 789177, 789167Y, 789177Y, 789167(A), 789177(A), 789167Y(A), 789177Y(A)	5FFFH

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

The following three types of I/O ports are available:

- CMOS Input: 8
- CMOS input/output: 17
- N-ch open-drain input/output: 6

Total: 31

Table 5-1. Port Functions

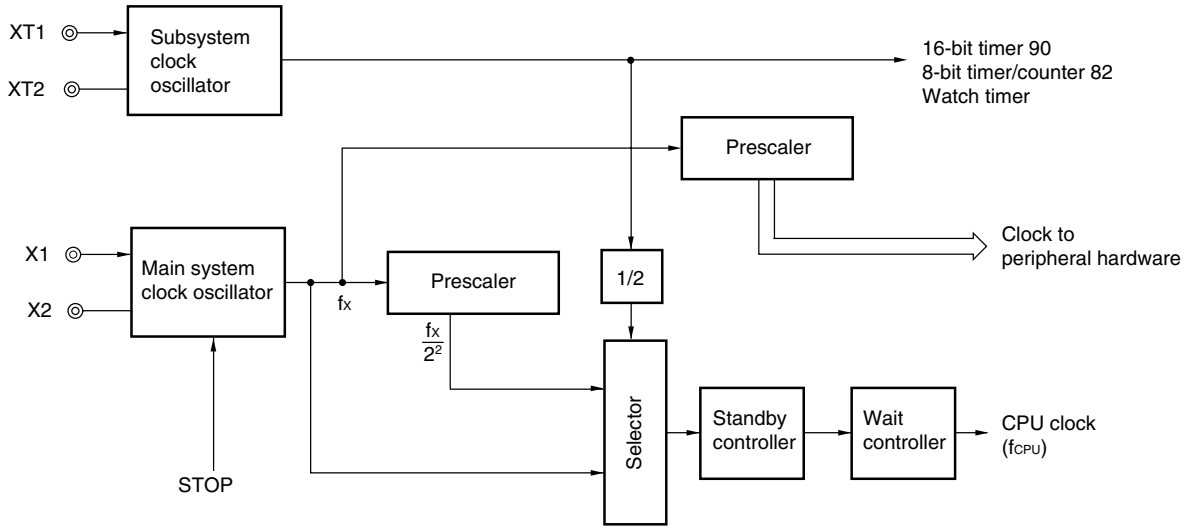
Port Name	Pin Name	Function
Port 0	P00 to P05	Input/output port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.
Port 1	P10, P11	Input/output port. Input/output can be specified in 1-bit units. When used as an input port, an on-chip pull-up resistor can be specified by means of software.
Port 2	P20 to P26	Input/output port. Input/output can be specified in 1-bit units. For P20 to P22, P25, and P26, an on-chip pull-up resistor can be specified by means of software. (P23 and P24 are N-ch open-drain I/O ports (with 5-V withstand voltage).)
Port 3	P30 to P33	Input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.
Port 5	P50 to P53	N-channel open-drain input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by the mask option.
Port 6	P60 to P67	Input-only port

5.2 Clock Generator

An on-chip system clock generator is provided.
The minimum instruction execution time can be changed.

★ • 0.2 μs/0.8 μs (@ 10.0-MHz operation with Main system clock, V_{DD} = 4.5 to 5.5 V)
• 122 μs (@ 32.768-kHz operation with Subsystem clock)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer

Six on-chip timers are provided.

- 16-bit timer 90 (TM90): 1 channel
- 8-bit timer/event counters 80, 81 (TM80, TM81): 2 channels
- 8-bit timer 82 (TM82): 1 channel
- Watch timer (WT): 1 channel
- Watchdog timer (WDT): 1 channel

Table 5-2. Timer Operation

		TM90	TM80	TM81	TM82	WT	WTM
Operation mode	Interval timer	–	1 channel	1 channel	1 channel	1 channel	1 channel
	External event counter	–	1 channel	1 channel	–	–	–
Function	Timer output	1 output	1 output	1 output	1 output	–	–
	Square wave output	–	1 output	1 output	1 output	–	–
	PWM output	–	1 output	1 output	1 output	–	–
	Buzzer output	1 output	–	–	–	–	–
	Capture	1 input	–	–	–	–	–
	Interrupt request	1	1	1	1	1	1

Figure 5-2. Block Diagram of 16-Bit Timer

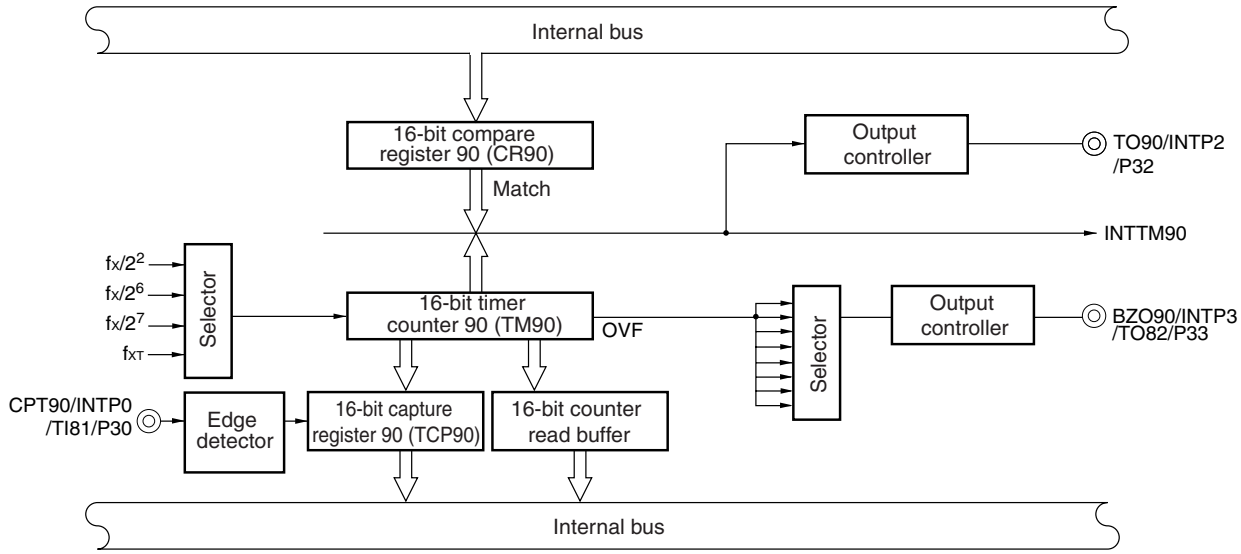


Figure 5-3. Block Diagram of 8-Bit Timer/Event Counter 80

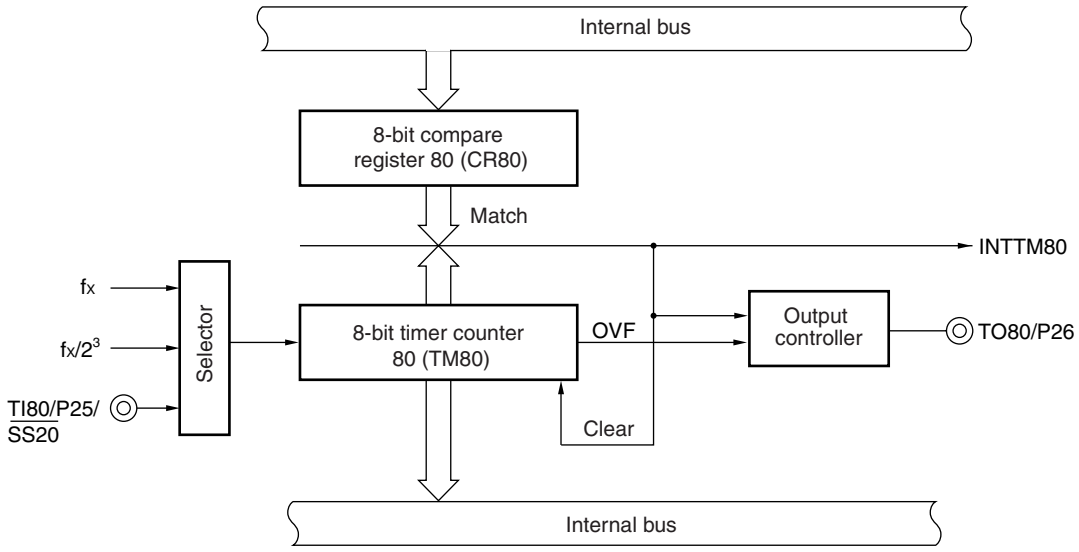


Figure 5-4. Block Diagram of 8-Bit Timer/Event Counter 81

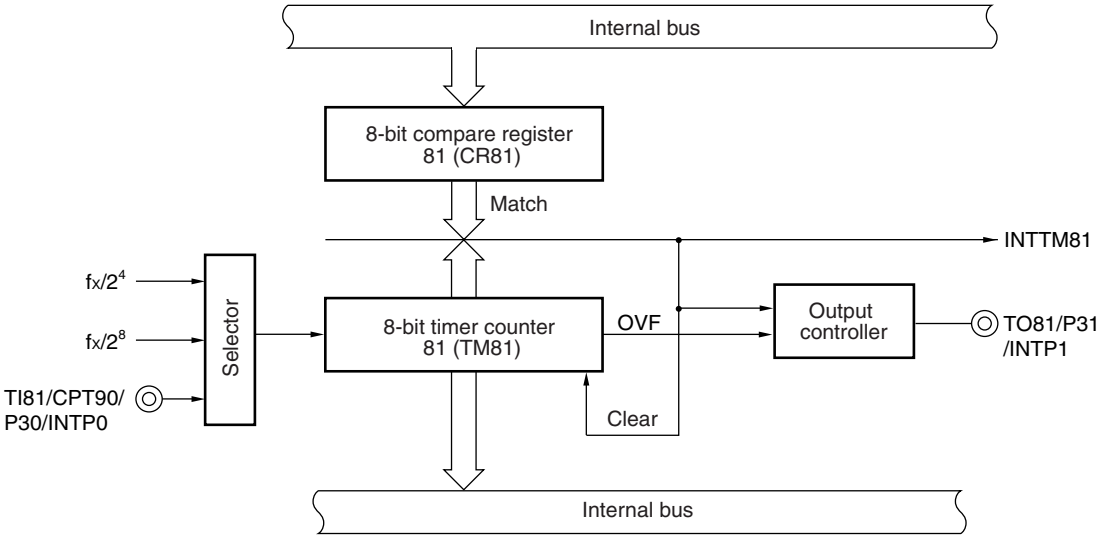


Figure 5-5. Block Diagram of 8-Bit Timer 82

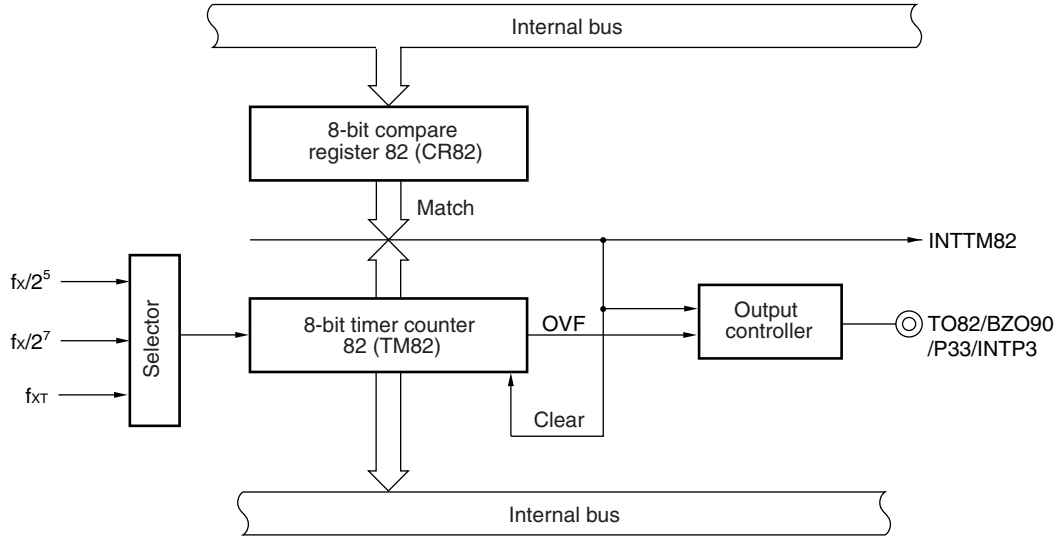
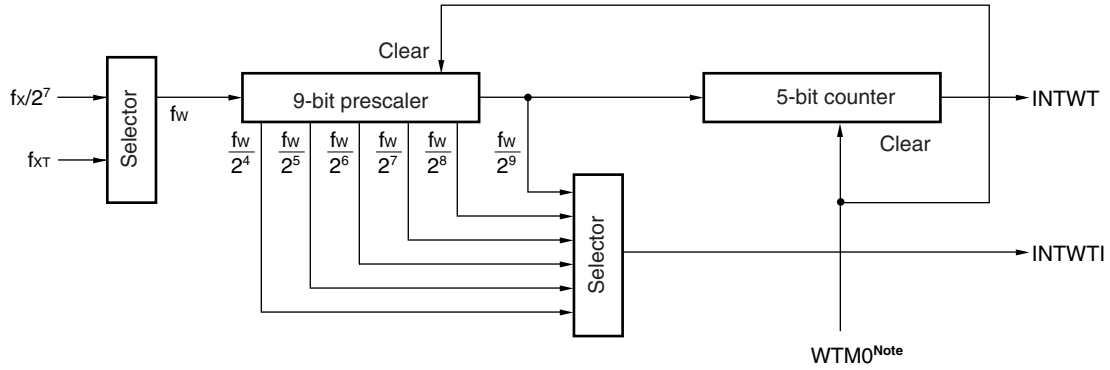
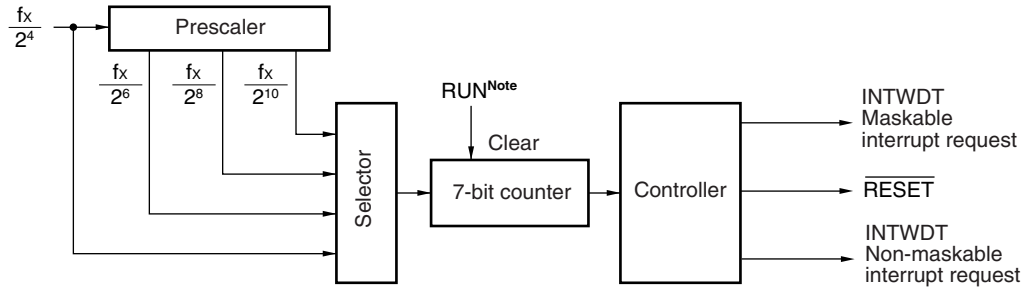


Figure 5-6. Block Diagram of Watch timer



Note Bit 0 of the Watch timer mode control register (WTM)

Figure 5-7. Watchdog Timer Block Diagram



Note Bit 7 of the Watchdog timer mode control register (WDTM)

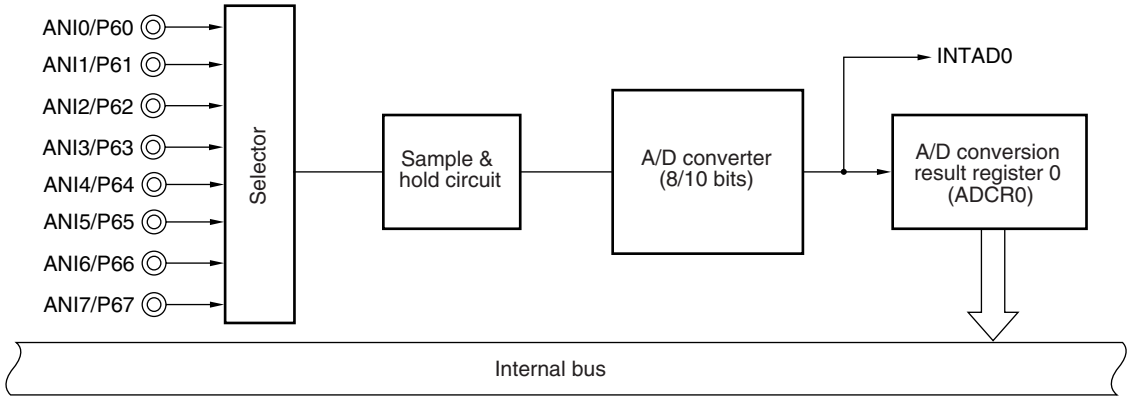
5.4 A/D Converter

The conversion resolution of the A/D converter differs depending on the product as shown below.

- 8-bit A/D converter × 8 channels ....μPD78916x, 78916xY, 78916x(A), 78916xY(A)
- 10-bit A/D converter × 8 channels ..μPD78917x, 78917xY, 78917x(A), 78917xY(A)

A/D conversion can only be started by software.

Figure 5-8. A/D Converter Block Diagram



5.5 Serial Interface

Two serial interface channels are incorporated.

- Serial interface SIO20: 1 channel
- Serial interface SMB[Note]: 1 channel

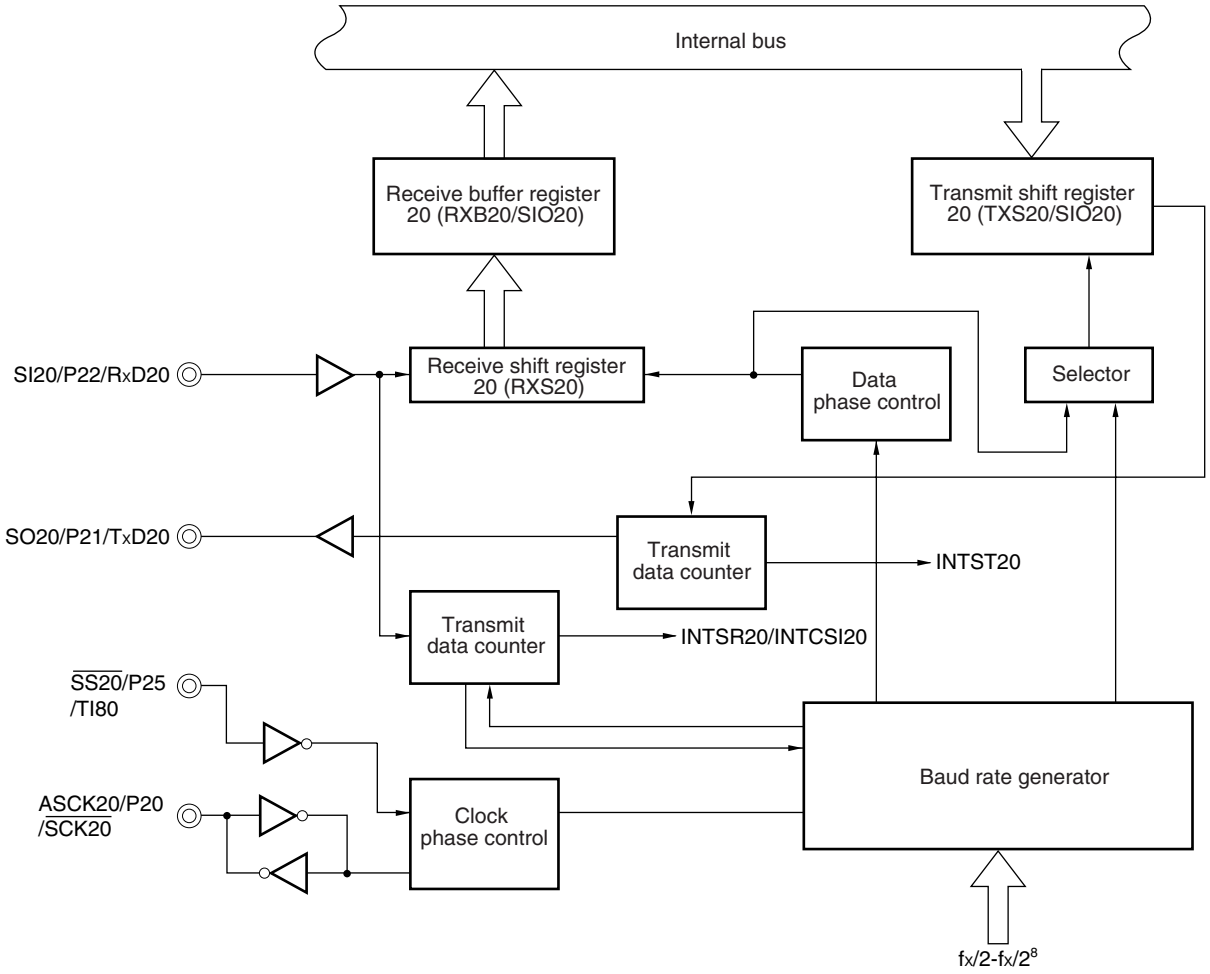
Note The SMB0 is available in μPD78916xY, 78917xY, 78916xY(A), and 78917xY(A) products only.

(1) Serial Interface SIO20

Serial interface 20 has the following three modes:

- Operation stop mode: Power consumption can be reduced.
- Asynchronous serial interface (UART) mode: A dedicated baud rate generator is incorporated.
- 3-wire serial I/O mode: A function to select the clock phase or data phase is incorporated.

Figure 5-9. Block Diagram of Serial Interface 20



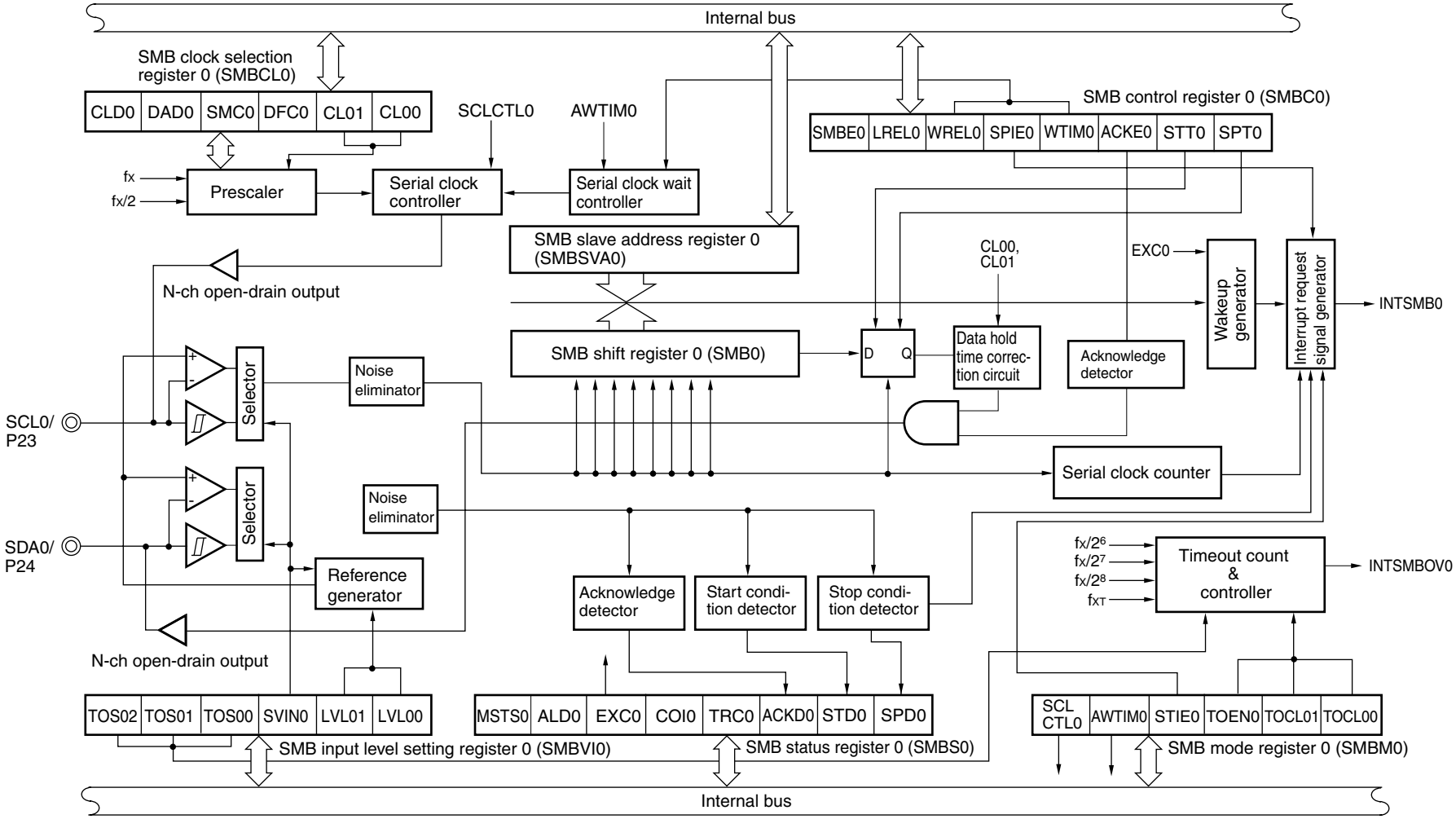
(2) Serial Interface SMB0

SMB0 has following two modes:

- Operation stop mode: Power consumption can be reduced.
- SMB mode: Supporting multi-master.

Figure 5-10 shows the block diagram of Serial Interface SMB0.

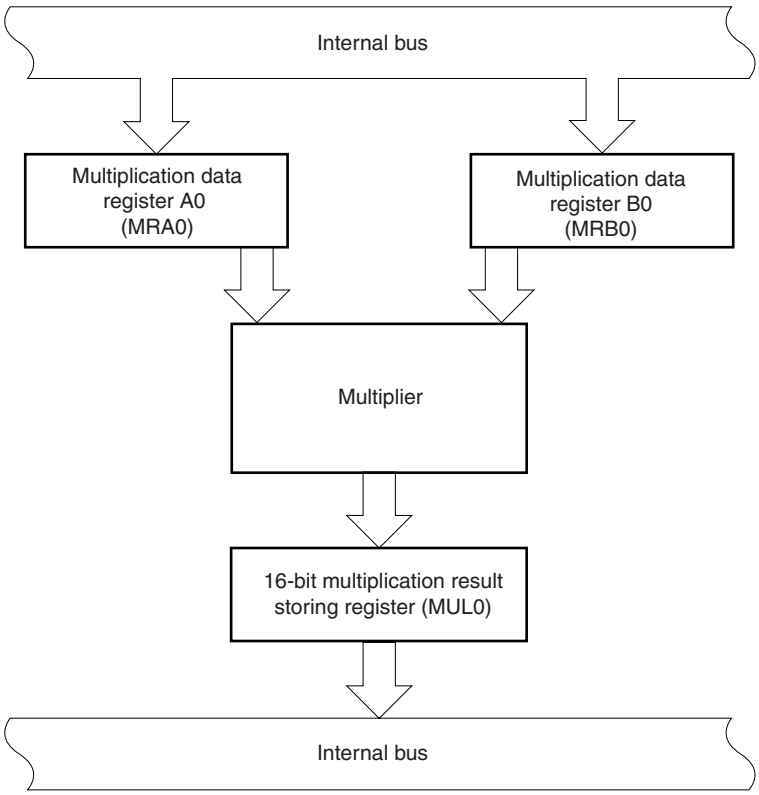
Figure 5-10. Block Diagram of SMB0



5.6 Multiplier

The calculation of 8 bits × 8 bits = 16 bits can be performed.

Figure 5-11. Multiplier Block Diagram



6. INTERRUPT FUNCTION

A total of 17 interrupt sources are provided, divided into the following two types.

- Non-maskable interrupts: 1 source
- Maskable interrupts: 16 sources

Table 6-1. Interrupt Source List

Interrupt Type	Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	–	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with the interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTSR20	End of serial interface 20 UART reception	Internal	000EH	(B)
		INTCSI20	End of serial interface 20 3-wire SIO transfer reception			
	6	INTST20	End of serial interface 20 UART transmission		0010H	
	7	INTWT	Watch timer interrupt		0012H	
	8	INTWTI	Interval timer interrupt		0014H	
	9	INTTM80	Generation of matching signal of 8-bit timer/event counter 80		0016H	
	10	INTTM81	Generation of matching signal of 8-bit timer/event counter 81		0018H	
	11	INTTM82	Generation of matching signal of 8-bit timer 82		001AH	
	12	INTTM90	Generation of matching signal of 16-bit timer 90		001CH	
	13	INTSMB0[Note 3]	SMB interrupt		001EH	
	14	INTSMBOV0[Note 3]	SMB timeout interrupt		0020H	
	15	INTAD0	A/D conversion completion signal		0022H	

Notes 1. Priority is the priority order when several maskable interrupt requests are generated at the same time. 0 is the highest order and 15 is the lowest order.

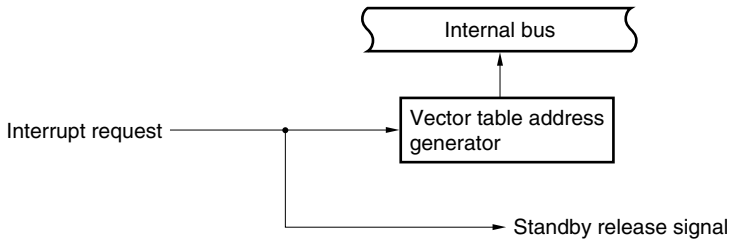
2. Basic configuration types (A), (B), and (C) correspond to (A), (B), and (C) in Figure 6-1.

3. μPD78916xY, 78917xY, 78916xY(A), 78917xy(A) only.

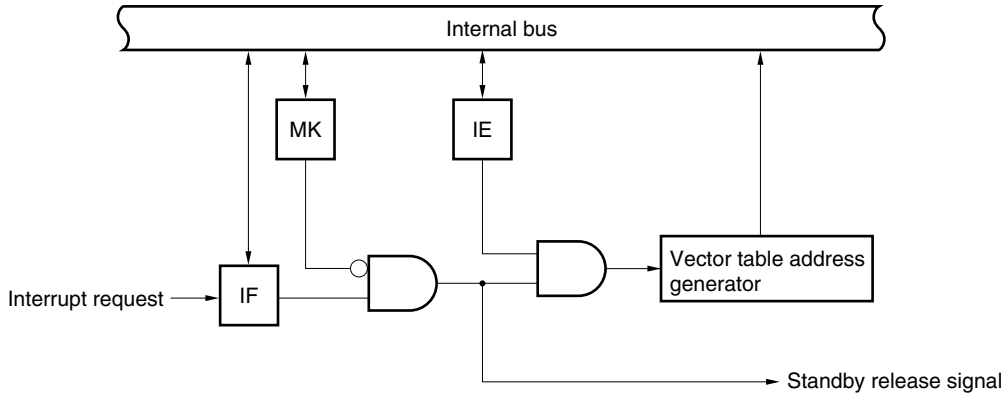
Remark As the interrupt source of the watchdog timer (INTWDT), either a non-maskable interrupt or a maskable interrupt (internal) can be selected.

Figure 6-1. Basic Configuration of Interrupt Function

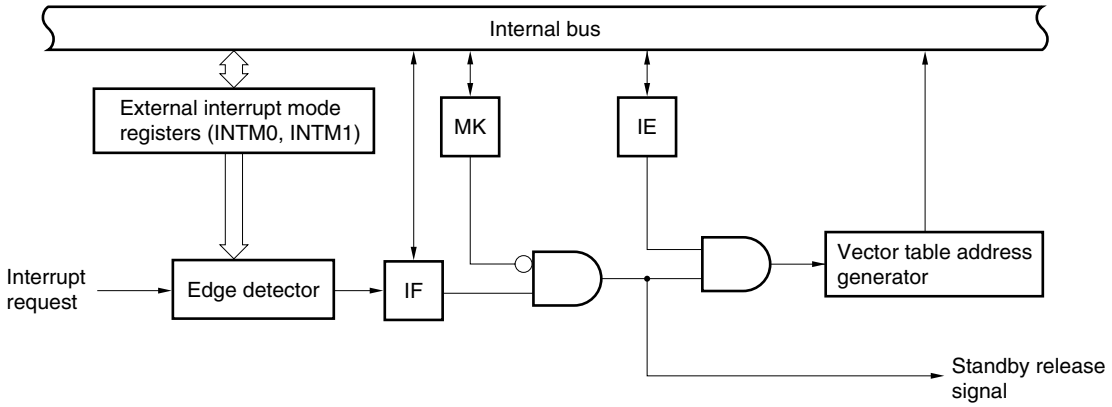
(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt



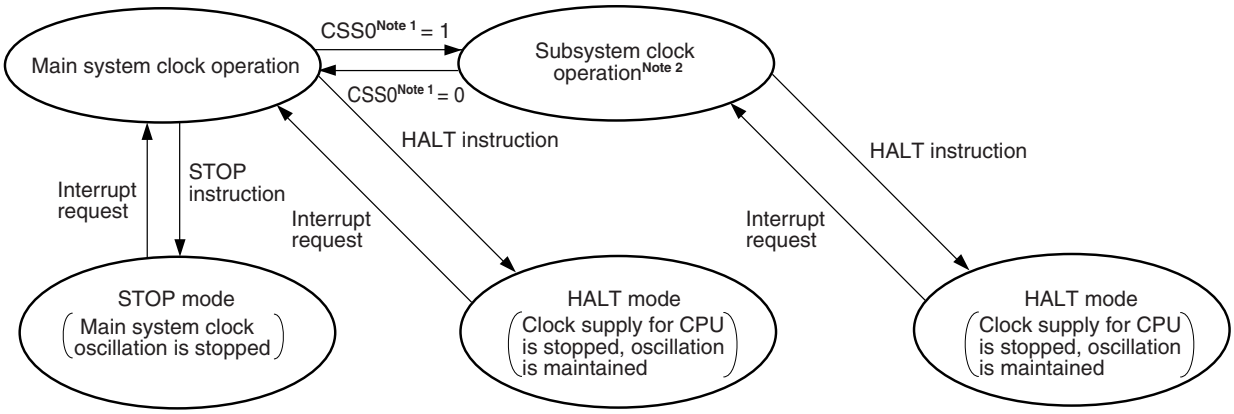
IF: Interrupt request flag
IE: Interrupt enable flag
MK: Interrupt mask flag

7. STANDBY FUNCTION

The following two standby functions are available for further reduction of system current consumption.

- HALT mode: In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.
- STOP mode: In this mode, oscillation of the system clock is stopped. All the operations performed on the system clock are suspended, resulting in extremely small power consumption.

Figure 7-1. Standby Function



Notes 1. Bit 4 of the sub-clock control register (CSS)

2. The current consumption can be reduced by stopping the main system clock.
When the CPU is operating on the subsystem clock, set bit 7 (MCC) of the processor clock control register (PCC) to stop the main system clock. The STOP instruction cannot be used.

Caution When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

8. RESET FUNCTION

The following two reset methods are available.

(1) External reset by the $\overline{\text{RESET}}$ pin
(2) Internal reset by watchdog timer detection runaway time.

9. MASK OPTION

The μPD78916x, 78917x, 78916xY, 78917xY, 78916x(A), 78917x(A) 78916xY(A), and 78917xY(A) have the following mask options.

- P50 to P53 mask options
  On-chip pull-up resistors can be selected.
  <1> Specify on-chip pull-up resistors in bit units
  <2> Do not specify on-chip pull-up resistors

10. INSTRUCTION SET OVERVIEW

This section lists the μPD78916x, 78917x, 78916xY, 78917xY, 78916x(A), 78917x(A) , 78916xY(A), and 78917xY(A) instruction set.

10.1 Conventions

10.1.1 Operand identifiers and description methods

Operands are described in the “Operand” column of each instruction in accordance with the description method of the instruction operand identifier (refer to the assembler specifications for detail). When there are two or more description methods, select one of them. Alphabetic letters in capitals and the symbols, #, !, $, and [ ], are keywords and must be described as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: Absolute address specification
- $: Relative address specification
- [ ]: Indirect address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to describe the #,!, $, or [ ] symbols.

For operand register identifiers, r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for description.

Table 10-1. Operand Identifiers and Description Methods

Identifier	Description Method
r rp sfr	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7), AX (RP0), BC (RP1), DE (RP2), HL (RP3) Special function register symbol
saddr saddrp	FE20H to FF1FH immediate data or label FE20H to FF1FH immediate data or label (even address only)
addr16 addr5	0000H to FFFFH immediate data or label (Only even addresses for 16-bit data transfer instructions) 0040H to 007FH immediate data or label (even address only)
word byte bit	16-bit immediate data or label 8-bit immediate data or label 3-bit immediate data or label

10.1.2 Descriptions of operation fields

A: A register; 8-bit accumulator
X: X register
B: B register
C: C register
D: D register
E: E register
H: H register
L: L register
AX: AX register pair; 16-bit accumulator
BC: BC register pair
DE: DE register pair
HL: HL register pair
PC: Program counter
SP: Stack pointer
PSW: Program status word
CY: Carry flag
AC: Auxiliary carry flag
Z: Zero flag
IE: Interrupt request enable flag
NMIS: Non-maskable interrupt servicing flag
( ): Memory contents indicated by address or register contents in parentheses
X_H, X_L: Higher 8 bits and lower 8 bits of 16-bit register
∧: Logical product (AND)
∨: Logical sum (OR)
∀: Exclusive OR
$\overline{\quad}$: Inverted data
addr16: 16-bit immediate data or label
jdisp8: Signed 8-bit data (displacement value)

10.1.3 Description of flag operation fields

(Blank): Not affected
0: Cleared to 0
1: Set to 1
×: Set/cleared according to the result
R: Previously saved value is restored

10.2 Operations

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
MOV	r. #byte	3	6	r ← byte			
	saddr, #byte	3	6	(saddr) ← byte			
	sfr, #byte	3	6	sfr ← byte			
	A, r Note 1	2	4	A ← r			
	r, A Note 1	2	4	r ← A			
	A, saddr	2	4	A ← (saddr)			
	saddr, A	2	4	(saddr) ← A			
	A, sfr	2	4	A ← sfr			
	sfr, A	2	4	sfr ← A			
	A, !addr16	3	8	A ← (addr16)			
	!addr16, A	3	8	(addr16) ← A			
	PSW, #byte	3	6	PSW ← byte	×	×	×
	A, PSW	2	4	A ← PSW			
	PSW, A	2	4	PSW ← A	×	×	×
	A, [DE]	1	6	A ← (DE)			
	[DE], A	1	6	(DE) ← A			
	A, [HL]	1	6	A ← (HL)			
	[HL], A	1	6	(HL) ← A			
	A, [HL + byte]	2	6	A ← (HL + byte)			
	[HL + byte], A	2	6	(HL + byte) ← A			
XCH	A, X	1	4	A ←→ X			
	A, r Note 2	2	6	A ←→ r			
	A, saddr	2	6	A ←→ (saddr)			
	A, sfr	2	6	A ←→ (sfr)			
	A, [DE]	1	8	A ←→ (DE)			
	A, [HL]	1	8	A ←→ (HL)			
	A, [HL + byte]	2	8	A ←→ (HL+byte)			
MOVW	rp, #word	3	6	rp ← word			
	AX, saddrp	2	6	AX ← (saddrp)			
	saddrp, AX	2	8	(saddrp) ← AX			
	AX, rp Note 3	1	4	AX ← rp			
	rp, AX Note 3	1	4	rp ← AX			

Notes 1. Except r = A

2. Except r = A, X

3. Only when rp = BC, DE, HL

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
XCHW	AX, rp[Note]	1	8	AX ←→ rp			
ADD	A, #byte	2	4	A, CY ← A + byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte	×	×	×
	A, r	2	4	A, CY ← A + r	×	×	×
	A, saddr	2	4	A, CY ← A + (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A + (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A + (HL + byte)	×	×	×
ADDC	A, #byte	2	4	A, CY ← A + byte + CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) + byte + CY	×	×	×
	A, r	2	4	A, CY ← A + r + CY	×	×	×
	A, saddr	2	4	A, CY ← A+ (saddr) + CY	×	×	×
	A, !addr16	3	8	A, CY ← A+ (addr16) +CY	×	×	×
	A, [HL]	1	6	A, CY ← A + (HL) + CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A+ (HL + byte) + CY	×	×	×
SUB	A, #byte	2	4	A, CY ← A – byte	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte	×	×	×
	A, r	2	4	A, CY ← A – r	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr)	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16)	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL)	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte)	×	×	×
SUBC	A, #byte	2	4	A, CY ← A – byte – CY	×	×	×
	saddr, #byte	3	6	(saddr), CY ← (saddr) – byte – CY	×	×	×
	A, r	2	4	A, CY ← A – r – CY	×	×	×
	A, saddr	2	4	A, CY ← A – (saddr) – CY	×	×	×
	A, !addr16	3	8	A, CY ← A – (addr16) – CY	×	×	×
	A, [HL]	1	6	A, CY ← A – (HL) – CY	×	×	×
	A, [HL + byte]	2	6	A, CY ← A – (HL + byte) – CY	×	×	×

Note Only when rp = BC, DE, HL

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
AND	A, #byte	2	4	A ← A ∧ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∧ byte	×		
	A, r	2	4	A ← A ∧ r	×		
	A, saddr	2	4	A ← A ∧ (saddr)	×		
	A, !addr16	3	8	A ← A ∧ (addr16)	×		
	A, [HL]	1	6	A ← A ∧ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∧ (HL + byte)	×		
OR	A, #byte	2	4	A ← A ∨ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ∨ byte	×		
	A, r	2	4	A ← A ∨ r	×		
	A, saddr	2	4	A ← A ∨ (saddr)	×		
	A, !addr16	3	8	A ← A ∨ (addr16)	×		
	A, [HL]	1	6	A ← A ∨ (HL)	×		
	A, [HL + byte]	2	6	A ← A ∨ (HL + byte)	×		
XOR	A, #byte	2	4	A ← A ⊻ byte	×		
	saddr, #byte	3	6	(saddr) ← (saddr) ⊻ byte	×		
	A, r	2	4	A ← A ⊻ r	×		
	A, saddr	2	4	A ← A ⊻ (saddr)	×		
	A, !addr16	3	8	A ← A ⊻ (addr16)	×		
	A, [HL]	1	6	A ← A ⊻ (HL)	×		
	A, [HL + byte]	2	6	A ← A ⊻ (HL + byte)	×		
CMP	A, #byte	2	4	A – byte	×	×	×
	saddr, #byte	3	6	(saddr) – byte	×	×	×
	A, r	2	4	A – r	×	×	×
	A, saddr	2	4	A – (saddr)	×	×	×
	A, !addr16	3	8	A – (addr16)	×	×	×
	A, [HL]	1	6	A – (HL)	×	×	×
	A, [HL + byte]	2	6	A – (HL + byte)	×	×	×
ADDW	AX, #word	3	6	AX, CY ← AX + word	×	×	×
SUBW	AX, #word	3	6	AX, CY ← AX – word	×	×	×
CMPW	AX, #word	3	6	AX – word	×	×	×
INC	r	2	4	r ← r + 1	×	×	
	saddr	2	4	(saddr) ← (saddr) + 1	×	×	
DEC	r	2	4	r ← r– 1	×	×	
	saddr	2	4	(saddr) ← (saddr) – 1	×	×	

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags		
					Z	AC	CY
INCW	rp	1	4	rp ← rp + 1			
DECW	rp	1	4	rp ← rp – 1			
ROR	A, 1	1	2	(CY, A_7 ← A_0, A_{m-1} ← A_m) × 1			×
ROL	A, 1	1	2	(CY, A_0 ← A_7, A_{m+1} ← A_m) × 1			×
RORC	A, 1	1	2	(CY ← A_0, A_7 ← CY, A_{m-1} ← A_m) × 1			×
ROLC	A, 1	1	2	(CY ← A_7, A_0 ← CY, A_{m+1} ← A_m) × 1			×
SET1	saddr.bit	3	6	(saddr.bit) ← 1			
	sfr.bit	3	6	sfr.bit ← 1			
	A.bit	2	4	A.bit ← 1			
	PSW.bit	3	6	PSW.bit ← 1	×	×	×
	[HL].bit	2	10	(HL).bit ← 1			
CLR1	saddr.bit	3	6	(saddr.bit) ← 0			
	sfr.bit	3	6	sfr.bit ← 0			
	A.bit	2	4	A.bit ← 0			
	PSW.bit	3	6	PSW.bit ← 0	×	×	×
	[HL].bit	2	10	(HL).bit ← 0			
SET1	CY	1	2	CY ← 1			1
CLR1	CY	1	2	CY ← 0			0
NOT1	CY	1	2	CY ← $\overline{CY}$			×
CALL	!addr16	3	6	(SP – 1) ← (PC + 3)$_H$, (SP – 2) ← (PC + 3)$_L$, PC ← addr16, SP ←SP – 2			
CALLT	[addr5]	1	8	(SP – 1) ← (PC + 1)$_H$, (SP – 2) ← (PC + 1)$_L$, PC_H ← (00000000, addr5 + 1) PC_L ← (00000000, addr5) SP ← SP – 2			
RET		1	6	PC_H ← (SP + 1), PC_L ← (SP), SP ← SP + 2			
RETI		1	8	PC_H ← (SP + 1), PC_L ← (SP), PSW ← (SP + 2), SP ← SP + 3, NMIS ← 0	R	R	R
PUSH	PSW	1	2	(SP – 1) ← PSW, SP ← SP – 1			
	rp	1	4	(SP – 1) ← rp_H, (SP – 2) ← rp_L, SP ← SP –– 2			
POP	PSW	1	4	PSW ← (SP), SP ← SP + 1	R	R	R
	rp	1	6	rp_H ← (SP + 1), rp_L ← (SP), SP ← SP + 2			
MOVW	SP, AX	2	8	SP ← AX			
	AX, SP	2	6	AX ← SP			

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

Mnemonic	Operand	Bytes	Clock	Operation	Flags
					Z AC CY
BR	!addr16	3	6	PC ← addr16	
	$addr16	2	6	PC ← PC + 2 + jdisp8	
	AX	1	6	PC_H ← A, PC_L ← X	
BC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 1	
BNC	$addr16	2	6	PC ← PC + 2 + jdisp8 if CY = 0	
BZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 1	
BNZ	$addr16	2	6	PC ← PC + 2 + jdisp8 if Z = 0	
BT	saddr.bit, $saddr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 1	
	sfr.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 1	
	A.bit, $saddr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 1	
	PSW.bit $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 1	
BF	saddr.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if (saddr. bit) = 0	
	sfr.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if sfr. bit = 0	
	A.bit, $addr16	3	8	PC ← PC + 3 + jdisp8 if A. bit = 0	
	PSW.bit, $addr16	4	10	PC ← PC + 4 + jdisp8 if PSW. bit = 0	
DBNZ	B, $addr16	2	6	B ← B – 1, then PC ← PC + 2 + jdisp8 if B ≠ 0	
	C, $addr16	2	6	C ← C – 1, then PC ← PC + 2 + jdisp8 if C ≠ 0	
	saddr, $addr16	3	8	(saddr) ← (saddr) – 1, then PC ← PC + 3 + jdisp8 if (saddr) ≠ 0	
NOP		1	2	No Operation	
EI		3	6	IE ← 1 (Enable Interrupt)	
DI		3	6	IE ← 0 (Disable Interrupt)	
HALT		1	2	Set HALT Mode	
STOP		1	2	Set Stop Mode	

Remark One clock of an instruction is one clock of the CPU clock (f_{CPU}) selected using the processor clock control register (PCC).

11. ELECTRICAL SPECIFICATIONS

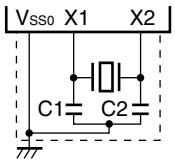
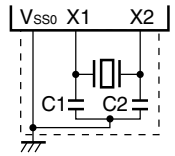
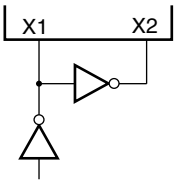
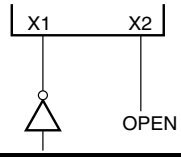
Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}	$AV_{DD} - 0.3\ V \le V_{DD} \le AV_{DD} + 0.3\ V$		−0.3 to +6.5	V
	AV_{DD}	$AV_{REF} \le AV_{DD} + 0.3\ V$			V
	AV_{REF}	$AV_{REF} \le V_{DD} + 0.3\ V$			V
Input voltage	V_{I1}	Pins other than P50 to P53, P23, P24		−0.3 to V_{DD} + 0.3	V
	V_{I2}	P23, P24		−0.3 to +5.5	V
	V_{I3}	P50 to P53	N-ch open drain	−0.3 to +13	V
			On-chip pull-up resistor	−0.3 to V_{DD} + 0.3	V
Output voltage	V_O			−0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	μPD78916x, 78917x, 78916xY, 78917xY	−10	mA
		Total for all pins		−30	mA
		Per pin	μPD78916x(A), 78917x(A), 78916xY(A), 78917xY(A)	−7	mA
		Total for all pins		−22	mA
Output current, low	I_{OL}	Per pin	μPD78916x, 78917x, 78916xY, 78917xY	30	mA
		Total for all pins		160	mA
		Per pin	μPD78916x(A), 78917x(A), 78916xY(A), 78917xY(A)	10	mA
		Total for all pins		120	mA
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

★ **Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)**

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1	V_{DD} = 4.5 to 5.5 V	1.0		10.0	MHz
			V_{DD} = 3.0 to 5.5 V	1.0		6.0	MHz
			V_{DD} = 1.8 to 5.5 V	1.0		5.0	MHz
		Oscillation stabilization timeNote 2	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)Note 1	V_{DD} = 4.5 to 5.5 V	1.0		10.0	MHz
			V_{DD} = 3.0 to 5.5 V	1.0		6.0	MHz
			V_{DD} = 1.8 to 5.5 V	1.0		5.0	MHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 5.5 V			10	ms
			V_{DD} = 1.8 to 5.5 V			30	ms
External clock		X1 input frequency (f_X)Note 1	V_{DD} = 4.5 to 5.5 V	1.0		10.0	MHz
			V_{DD} = 3.0 to 5.5 V	1.0		6.0	MHz
			V_{DD} = 1.8 to 5.5 V	1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 4.5 to 5.5 V	45		500	ns
			V_{DD} = 3.0 to 5.5 V	75		500	ns
			V_{DD} = 1.8 to 5.5 V	85		500	ns
		X1 input frequency (f_X)Note 1	V_{DD} = 2.7 to 5.5 V	1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 2.7 to 5.5 V	85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator that stabilizes oscillation within the oscillation wait time.

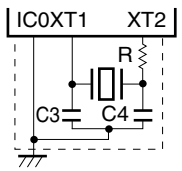
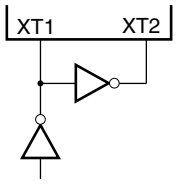
Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})[Note 1]		32	32.768	35	kHz
		Oscillation stabilization time[Note 2]	V_{DD} = 4.5 to 5.5 V		1.2	2	s
			V_{DD} = 1.8 to 5.5 V			10	s
External clock		XT1 input frequency (f_{XT})[Note 1]		32		35	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		14.3		15.6	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release. Use a resonator that stabilizes oscillation within the oscillation wait time.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS0}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = −40°C to +85°C, V_{DD} = 1.8 to 5.5 V) (1/3)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin	μPD78916x, 78917x, 78916xY, 78917xY				−1	mA
		Total for all pins					−15	mA
		Per pin	μPD78916x(A), 78917x(A), 78916xY(A), 78917xY(A)				−1	mA
		Total for all pins					−11	mA
Output current, low	I_{OL}	Per pin	μPD78916x, 78917x, 78916xY, 78917xY				10	mA
		Total for all pins					80	mA
		Per pin	μPD78916x(A), 78917x(A), 78916xY(A), 78917xY(A)				3	mA
		Total for all pins					60	mA
Input voltage, high	V_{IH1}	P00 to P05, P10, P11, P60 to P67		V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0.9 V_{DD}		V_{DD}	V
	V_{IH2}	P50 to P53	N-ch open drain	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		12	V
				V_{DD} = 1.8 to 5.5 V	0.9 V_{DD}		12	V
			On-chip pull-up resistor	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0.9 V_{DD}		V_{DD}	V
	V_{IH3}	$\overline{RESET}$, P20 to P26, P30 to P33		V_{DD} = 2.7 to 5.5 V	0.8 V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0.9 V_{DD}		V_{DD}	V
	V_{IH4}	X1, X2, XT1, XT2		V_{DD} = 4.5 to 5.5 V	V_{DD} − 0.5		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	V_{DD} − 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P05, P10, P11, P60 to P67		V_{DD} = 2.7 to 5.5 V	0		0.3 V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.1 V_{DD}	V
	V_{IL2}	P50 to P53		V_{DD} = 2.7 to 5.5 V	0		0.3 V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.1 V_{DD}	V
	V_{IL3}	$\overline{RESET}$, P20 to P26, P30 to P33		V_{DD} = 2.7 to 5.5 V	0		0.2 V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.1 V_{DD}	V
	V_{IL4}	X1, X2, XT1, XT2		V_{DD} = 4.5 to 5.5 V	0		0.4	V
				V_{DD} = 1.8 to 5.5 V	0		0.1	V
Output voltage, high	V_{OH}	Pins other than P23, P24, P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OH} = −1 mA		V_{DD} − 1.0			V
			V_{DD} = 1.8 to 5.5 V, I_{OH} = −100 μA		V_{DD} − 0.5			V
Output voltage, low	V_{OL1}	Pins other than P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA (μPD78916x, 78917x, 78916xY, 78917xY)				1.0	V
			V_{DD} = 4.5 to 5.5 V, I_{OL} = 3 mA (μPD78916x(A), 78917x(A), 78916xY(A), 78917xY(A))				1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 400 μA				0.5	V
	V_{OL2}	P50 to P53	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA (μPD78916x, 78917x, 78916xY, 78917xY)				1.0	V
			V_{DD} = 4.5 to 5.5 V, I_{OL} = 3 mA (μPD78916x(A), 78917x(A), 78916xY(A), 78917xY(A))				1.0	V
			V_{DD} = 1.8 to 5.5 V, I_{OL} = 1.6 mA				0.4	V

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (2/3)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input current leakage, high	I_{LIH1}	$V_I = V_{DD}$	Pins other than P50 to P53 (N-ch open-drain) X1, X2, XT1, and XT2			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_I = 12 V Note 1	P50 to P53 (N-ch open drain)			20	μA
Input current leakage, low	I_{LIL1}	V_I = 0 V	Pins other than P50 to P53 (N-ch open-drain) X1, X2, XT1, and XT2			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
	I_{LIL3}		P50 to P53 (N-ch open drain)			–3 Note 2	μA
Output current leakage, high	I_{LOH}	$V_O = V_{DD}$				3	μA
Output current leakage, low	I_{LOL}	V_O = 0 V				–3	μA
Software pull-up resistor	R_1	V_I = 0 V, for pins other than P23, P24, and P50 to P53		50	100	200	kΩ
Mask option pull-up resistor	R_2	V_I = 0 V, P50 to P53		15	30	60	kΩ

Notes 1. When pull-up resistors are not connected to P50 to P53 (specified by the mask option).

2. A low-level input leakage current of –60 μA(MAX.) flows only during the 1-cycle time after a read instruction is executed to P50 to P53 when on-chip pull-up resistors are not connected to P50 to P53 (specified by the mask option) and P50 to P53 are set to input mode. At times other than this, –3μA (MAX.) current flows.

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

★ **DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (3/3)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current	I_{DD1} Note 1	10.0-MHz crystal oscillation operating mode	V_{DD} = 5.0 V ± 10% Note 4		3.2	8.0	mA
		6.0-MHz crystal oscillation operating mode	V_{DD} = 5.0 V ± 10% Note 4		2.0	4.7	mA
		5.0-MHz crystal oscillation operating mode (C1 = C2 = 22pF)	V_{DD} = 5.0 V ± 10% Note 4		1.8	4.0	mA
			V_{DD} = 3.0 V ± 10% Note 5		0.6	1.2	mA
			V_{DD} = 2.0 V ± 10% Note 5		0.35	0.7	mA
	I_{DD2} Note 1	10.0-MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ± 10% Note 4		1.5	3.0	mA
		6.0-MHz Crystal oscillation HALT mode	V_{DD} = 5.0 V ± 10% Note 4		0.9	1.8	mA
		5.0-MHz crystal oscillation HALT mode (C1 = C2 = 22pF)	V_{DD} = 5.0 V ± 10% Note 4		0.75	1.5	mA
			V_{DD} = 3.0 V ± 10% Note 5		0.4	0.8	mA
			V_{DD} = 2.0 V ± 10% Note 5		0.25	0.5	mA
	I_{DD3} Note 1	32.768-kHz crystal oscillation operating mode Note 3 (C3 = C4 = 22pF, R = 220kΩ)	V_{DD} = 5.0 V ± 10%		25	90	μA
			V_{DD} = 3.0 V ± 10%		7.0	50	μA
			V_{DD} = 2.0 V ± 10%		3.5	30	μA
	I_{DD4} Note 1	32.768-kHz crystal oscillation HALT mode Note 3 (C3 = C4 = 22pF, R = 220kΩ)	V_{DD} = 5.0 V ± 10%		16	75	μA
			V_{DD} = 3.0 V ± 10%		4.5	35	μA
			V_{DD} = 2.0 V ± 10%		2.3	18	μA
	I_{DD5} Note 1	32.768-kHz crystal stop STOP mode	V_{DD} = 5.0 V ± 10%		0.1	10	μA
			V_{DD} = 3.0 V ± 10%		0.05	5.0	μA
			V_{DD} = 2.0 V ± 10%		0.05	3.0	μA
	I_{DD6} Note 2	10.0-MHz crystal oscillation A/D operating mode	V_{DD} = 5.0 V ± 10% Note 4		4.0	10.0	mA
		6.0-MHz crystal oscillation A/D operating mode	V_{DD} = 5.0 V ± 10% Note 4		2.8	6.7	mA
		5.0-MHz crystal oscillation A/D operating mode (C1 = C2 = 22pF)	V_{DD} = 5.0 V ± 10% Note 4		2.6	6.0	mA
			V_{DD} = 3.0 V ± 10% Note 4		1.4	3.2	mA
			V_{DD} = 2.0 V ± 10% Note 4		1.15	2.7	mA

Notes 1. The AV_{REF}ON (ADCS0 (bit 7 of ADM0; A/D converter mode register 0) = 1), AV_{DD}, and the port current (including the current flowing through the internal pull-up resistors) are not included.

2. The AV_{REF}On (ADCS0 =1) and port current (including the current flowing through the internal pull-up resistors) are not included. Refer to the A/D converter characteristics for the current flowing through AV_{REF}.

3. When the main system clock is stopped.

4. During high-speed mode operation (when the processor clock control register (PCC) is set to 00H.)

5. During low-speed mode operation (when PCC is set to 02H)

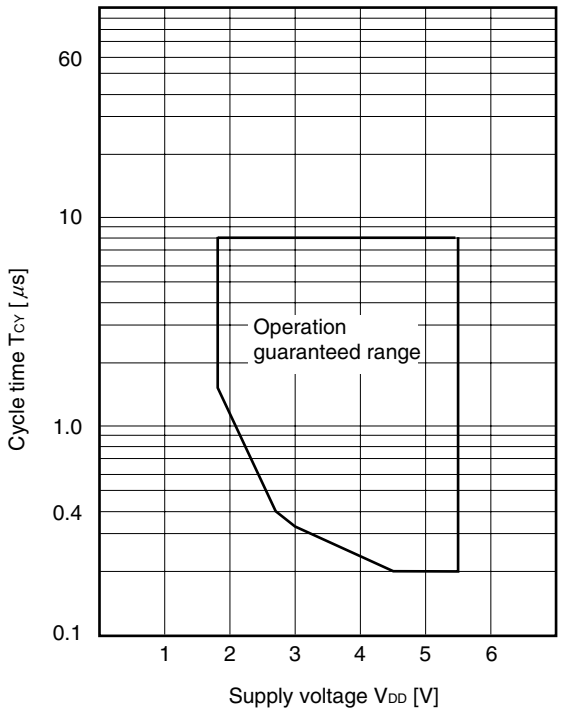
Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation (T_A = –40°C to +85°C, V_{DD} = 1.8 to 5.5 V)

	Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
★	Cycle time (minimum instruction execution time)	T_{CY}	Operation based on the main system clock	V_{DD} = 4.5 to 5.5 V	0.2		8	μs
				V_{DD} = 3.0 to 5.5 V	0.33		8	μs
				V_{DD} = 2.7 to 5.5 V	0.4		8	μs
				V_{DD} = 1.8 to 5.5 V	1.6		8	μs
			Operation based on the subsystem clock		114	122	125	μs
	TI80 and TI81 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V		0		4	MHz
			V_{DD} = 1.8 to 5.5 V		0		275	kHz
	TI80 and TI81 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V		0.1			μs
			V_{DD} = 1.8 to 5.5 V		1.8			μs
	Interrupt input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP3		10			μs
	$\overline{\text{RESET}}$ input low-level width	t_{RSL}			10			μs
	CPT90 input high-/low-level width	t_{CPH}, t_{CPL}			10			μs

★ **T_{CY} vs V_{DD} (main system clock)**



(2) Serial interface (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode ($\overline{SCK20}$...Internal clock)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		800			ns
		V_{DD} = 1.8 to 5.5 V		3200			ns
$\overline{SCK20}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 2.7 to 5.5 V		t_{KCY1}/2–50			ns
		V_{DD} = 1.8 to 5.5 V		t_{KCY1}/2–150			ns
SI20 setup time (to $\overline{SCK20}$ ↑)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
		V_{DD} = 1.8 to 5.5 V		500			ns
SI20 hold time (from $\overline{SCK20}$ ↑)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from $\overline{SCK20}$↓	t_{KSO1}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

(b) 3-wire serial I/O mode ($\overline{SCK20}$...External clock)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK20}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		900			ns
		V_{DD} = 1.8 to 5.5 V		3500			ns
$\overline{SCK20}$ high-/low-level width	t_{KH2}, t_{KL2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		1600			ns
SI20 setup time (to $\overline{SCK20}$ ↑)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
		V_{DD} = 1.8 to 5.5 V		150			ns
SI20 hold time (from $\overline{SCK20}$ ↑)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
		V_{DD} = 1.8 to 5.5 V		600			ns
SO20 output delay time from $\overline{SCK20}$ ↓	t_{KSO2}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
			V_{DD} = 1.8 to 5.5 V	0		1000	ns
SO20 setup time (when using $\overline{SS20}$, to $\overline{SS20}$ ↓)	t_{KAS2}	V_{DD} = 2.7 to 5.5 V				120	ns
		V_{DD} = 1.8 to 5.5 V				400	ns
SO20 disable time (when using $\overline{SS20}$, from $\overline{SS20}$ ↑)	t_{KDS2}	V_{DD} = 2.7 to 5.5 V				240	ns
		V_{DD} = 1.8 to 5.5 V				800	ns

Note R and C are the load resistance and load capacitance of the SO20 output line.

(c) UART mode (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 2.7 to 5.5 V			78125	bps
		V_{DD} = 1.8 to 5.5 V			19531	bps

(d) UART mode (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK20 cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V	900			ns
		V_{DD} = 1.8 to 5.5 V	3500			ns
ASCK20 high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 2.7 to 5.5 V	400			ns
		V_{DD} = 1.8 to 5.5 V	1600			ns
Transfer rate		V_{DD} = 2.7 to 5.5 V			39063	bps
		V_{DD} = 1.8 to 5.5 V			9766	bps
ASCK20 rise time, fall time	t_R, t_F				1	μs

(3) Serial interface SMB0 (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V) (μPD78916xY, 78917xY, 78916xY(A), 78917xY(A) only)

(a) DC Characteristics

	Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
★	Input voltage, high	V_{IH}	SCL0, SDA0 (at hysteresis)	V_{DD} = 2.7 to 5.5 V	0.8 V_{DD}		V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0.9 V_{DD}		V_{DD}	V
★	Input voltage, low	V_{IL}	SCL0, SDA0 (at hysteresis)	V_{DD} = 2.7 to 5.5 V	0		0.2 V_{DD}	V
				V_{DD} = 1.8 to 5.5 V	0		0.1 V_{DD}	V
	Output voltage, high	V_{OL}	SCL0, SDA0	V_{DD} = 4.5 to 5.5 V, I_{OL} = 10 mA (μPD78916xY, 78917xY)			1.0	V
				V_{DD} = 4.5 to 5.5 V, I_{OL} = 3 mA (μPD78916xY(A), 78917xY(A))			1.0	V
				V_{DD} = 1.8 to 5.5 V, I_{OL} = 400 μA			0.5	V
	Input current leakage, high	I_{LIH}	SCL0, SDA0	V_I = V_{DD}			3	μA
	Input current leakage, low	I_{LIL}	SCL0, SDA0	V_I = 0 V			–3	μA

(b) DC Characteristics (When using comparator)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input range	V_{SDA}, V_{SCL}	V_{DD} = 1.8 to 5.5 V	0		5.5	V
Transfer level	V_{ISDA}, V_{ISCL}	4.5 ≤ V_{DD} ≤ 5.5 V	0.72 V_{ISMB}	V_{ISMB}	1.28 V_{ISMB}	V
		3.3 ≤ V_{DD} < 4.5 V	0.78 V_{ISMB}	V_{ISMB}	1.22 V_{ISMB}	V
		2.7 ≤ V_{DD} < 3.3 V	0.75 V_{ISMB}	V_{ISMB}	1.25 V_{ISMB}	V
		1.8 ≤ V_{DD} < 2.7 V	0.90 V_{ISMB}	V_{ISMB}	1.45 V_{ISMB}	V
Input level threshold value	V_{ISMB}	LVL01, LVL00 = 0, 1		0.25 × V_{DD}		V
		LVL01, LVL00 = 1, 0		0.375 × V_{DD}		V
		LVL01, LVL00 = 1, 1		0.5 × V_{DD}		V

Note V_{ISMB} is an input level threshold value selected by bits LVL00 and LVL01 (bits 0 and 1 of SMB input level setting register 0 (SMBVI0)).

According to the SMB standard (V1.1), the maximum value of low-level input voltage is 0.8 V, and the minimum value of high-level input voltage, 2.1 V. To satisfy these conditions, set LVL01 and LVL00 as follows;

- When V_{DD} = 1.8 to 3.3 V: LVL01, LVL00 = 1, 1 (0.5 × V_{DD})
- When V_{DD} = 3.3 to 4.5 V: LVL01, LVL00 = 1, 0 (0.375 × V_{DD})
- When V_{DD} = 4.5 to 5.5 V: LVL01, LVL00 = 0, 1 (0.25 × V_{DD})

"LVL01, LVL00 = 0, 0" is not available since this setting does not satisfy the SMB standard (V1.1).

(c) AC Characteristics

Parameter		Symbol	SMB Mode		Standard Mode I^2C Bus		High-speed Mode I^2C Bus		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f_{CLK}	10	100	0	100	0	400	kHz
Bus free time (between stop and start condition)		t_{BUF}	4.7	–	4.7	–	1.3	–	μs
Hold time[Note1]		$t_{HD:STA}$	4.0	–	4.0	–	0.6	–	μs
Start/restart condition setup time		$t_{SU:STA}$	4.7	–	4.7	–	0.6	–	μs
Stop condition setup time		$t_{SU:STO}$	4.0	–	4.0	–	0.6	–	μs
Data hold time	When using CBUS-compatible master	$t_{HD:DAT}$	–	–	5	–	–	–	μs
	When using SMB/IIC bus		300	–	–	–	0[Note 2]	900[Note 3]	ns
Data setup time		$t_{SU:DAT}$	250	–	250	–	100[Note 4]	–	ns
SCL0 clock low-level width		t_{LOW}	4.7	–	4.7	–	1.3	–	μs
SCL0 clock high-level width		t_{HIGH}	4.0	50	4.0	–	0.6	–	μs
SCL0 and SDA0 signal fall time		t_F	–	300	–	300	–	300	ns
SCL0 and SDA0 signal rise time		t_R	–	1000	–	1000	–	300	ns
Spike pulse width controlled by input filter		t_{SP}	–	–	–	–	0	50	ns
Timeout		$t_{TIMEOUT}$	25	35	–	–	–	–	ms
Total extended time of SCL0 clock low-level period (slave)		$t_{LOW:SEXT}$	–	25	–	–	–	–	ms
Total extended time of cumulative clock low-level period (master)		$t_{LOW:MEXT}$	–	10	–	–	–	–	ms
Capacitive load per each bus line		Cb	–	–	–	400	–	400	pF

Notes 1. In the start condition, the first clock pulse is generated after this hold time.

2. To fill in the undefined area of the SCL0 falling edge, it is necessary for the device to internally provide at least 300 ns of hold time for the SDA0 signal (which is $V_{IHmin.}$ of the SCL0 signal).

3. If the device does not extend the SCL0 signal low hold time (t_{LOW}), only maximum data hold time $t_{HD:DAT}$ needs to be fulfilled.

4. The high-speed mode I^2C bus is available in the SMB mode and the standard mode I^2C bus system. At this time, the conditions described below must be satisfied.

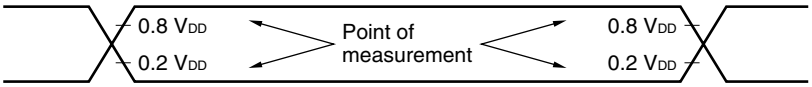
If the device extends the SCL0 signal low state hold time

$t_{SU:DAT} \geq 250$ ns

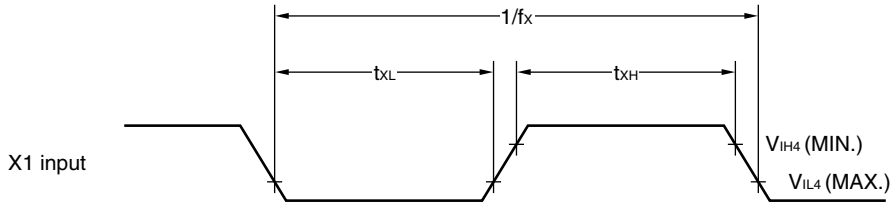
If the device extends the SCL0 signal low state hold time

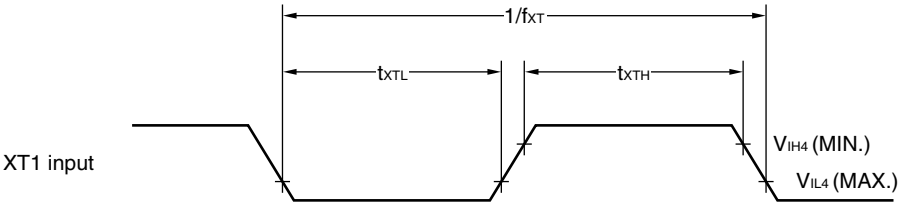
Be sure to transmit the next data bit to the SDA0 line before the SCL0 line is released ($t_{Rmax.}$+ $t_{SU:DAT}$ = 1000 + 250 = 1250 ns by the SMB mode or the standard mode I^2C bus specification).

AC Timing Measurement Points (excluding the X1 and XT1 inputs)

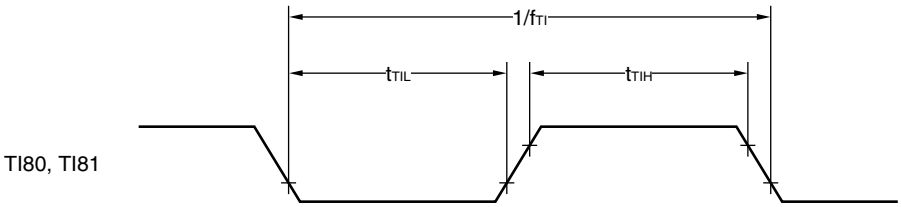


Clock Timing

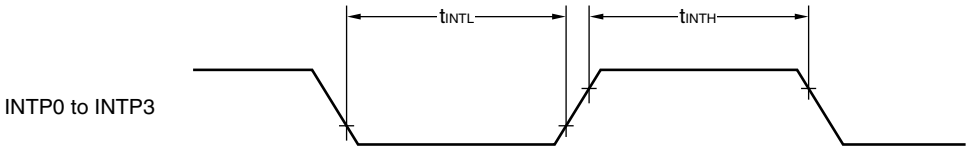




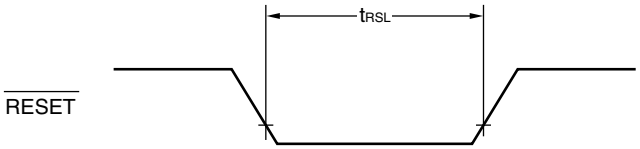
TI Timing



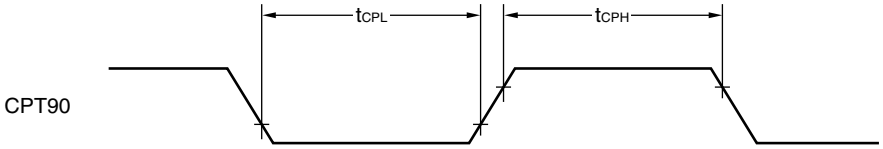
Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing

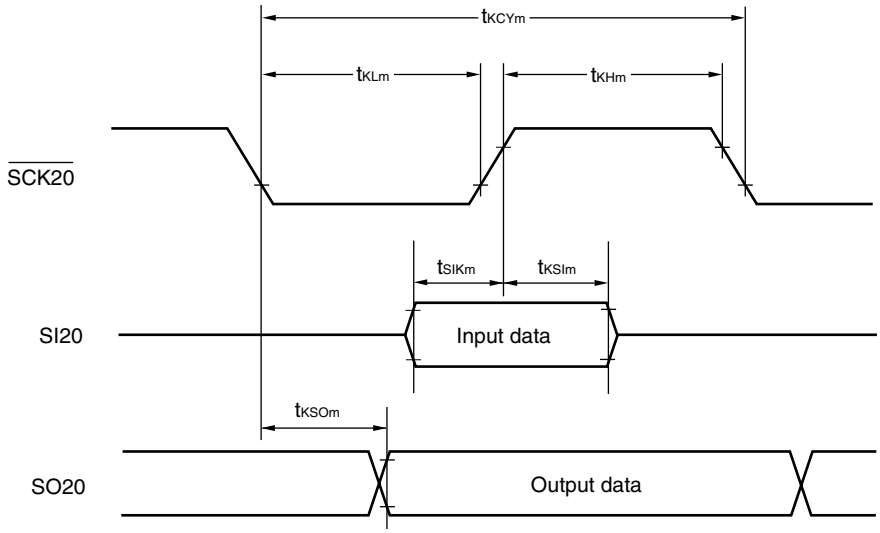


CPT90 Input Timing



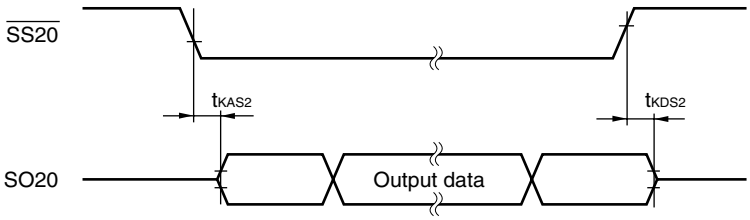
Serial Transfer Timing

3-wire serial I/O mode:

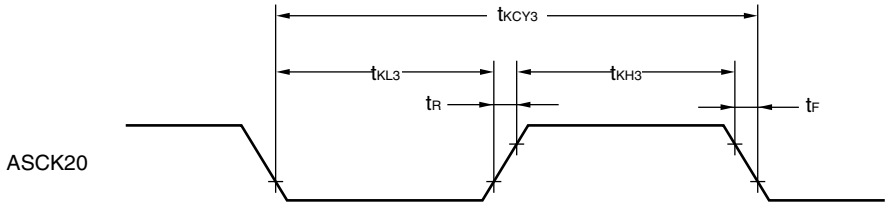


Remark m = 1, 2

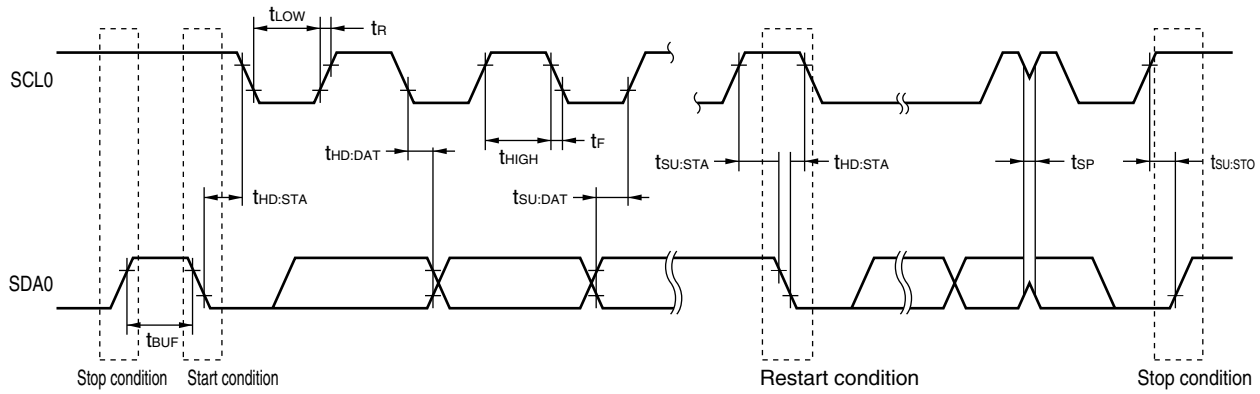
3-wire serial I/O mode (when using $\overline{SS20}$):



UART mode (external clock input):



SMB mode:



8-Bit A/D Converter Characteristics (μPD78916x, 78916xY, 78916x(A), 78916xY(A))

(T_A = –40 to +85°C, 1.8 ≤ AV_{REF} ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	Resolution			8	8	8	bit
	Overall error[Note]		2.7 ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.4	±0.6	%FSR
			1.8 ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.8	±1.2	%FSR
★	Conversion time	t_{CONV}	4.5 ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	12		100	μs
			2.7 ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	14		100	μs
			1.8 ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	28		100	μs
	Analog input voltage	V_{IAN}		0		AV_{REF}	V
	Reference voltage	AV_{REF}		1.8		AV_{DD}	V
	Resistance between AV_{REF} and AV_{SS}	R_{ADREF}		20	40		kΩ

Note Excludes quantization error (±0.2%FSR).

Remark FSR: Full scale range

10-Bit A/D Converter Characteristics (μPD78917x, 78917xY, 78917x(A), 78917xY(A))

(T_A = –40 to +85°C, 1.8 ≤ AV_{REF} ≤ AV_{DD} = V_{DD} ≤ 5.5 V, AV_{SS} = V_{SS} = 0 V)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	Resolution			10	10	10	bit
	Overall error[Note]		4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.2	±0.4	%FSR
			2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.4	±0.6	%FSR
			1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V		±0.8	±1.2	%FSR
★	Conversion time	t_{CONV}	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	12		100	μs
			2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	14		100	μs
			1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V	28		100	μs
	Zero-scale error[Note]		4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.4	%FSR
			2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.6	%FSR
			1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.2	%FSR
	Full-scale error[Note]		4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.4	%FSR
			2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±0.6	%FSR
			1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.2	%FSR
	Integral linearity error[Note]	INL	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±2.5	LSB
			2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±4.5	LSB
			1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±8.5	LSB
	Differential linearity error[Note]	DNL	4.5 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±1.5	LSB
			2.7 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±2.0	LSB
			1.8 V ≤ AV_{REF} ≤ AV_{DD} ≤ 5.5 V			±3.5	LSB
	Analog input voltage	V_{IAN}		0		AV_{REF}	V
	Reference voltage	AV_{REF}		1.8		AV_{DD}	V
	Resistance between AV_{REF} and AV_{SS}	R_{AIREF}		20	40		kΩ

Note Excludes quantization error (±0.05%FSR).

Remark FSR: Full scale range

Data Memory Stop Mode Low Power Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

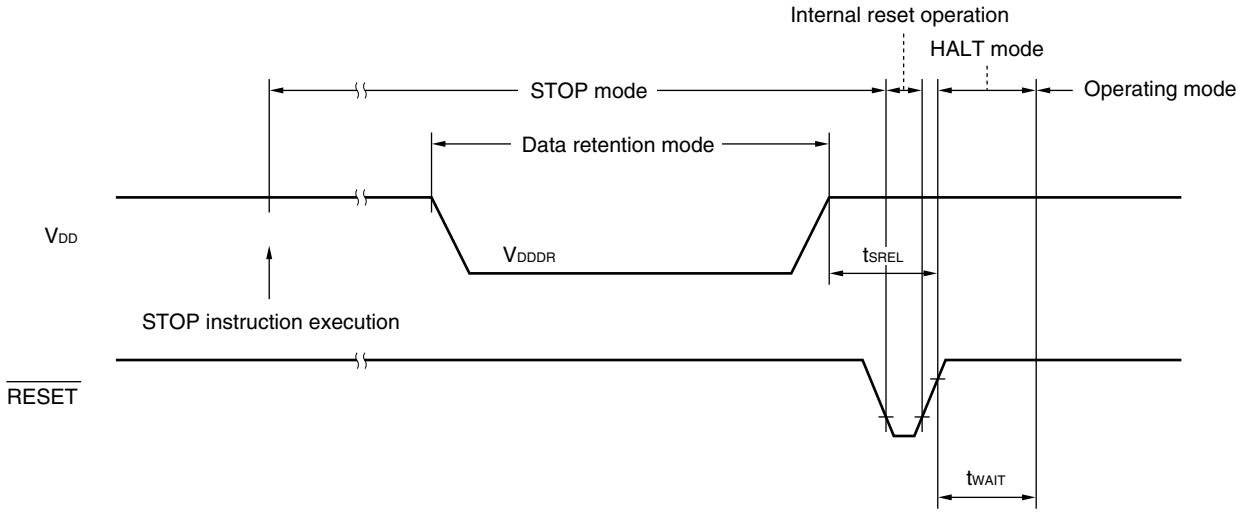
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.8		5.5	V
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time[Note 1]	t_{WAIT}	Release by $\overline{RESET}$		$2^{15}/f_X$		s
		Release by interrupt request		**Note 2**		s

Notes 1. The oscillation stabilization time is the time the CPU operation is stopped to prevent unstable operation when oscillation starts.

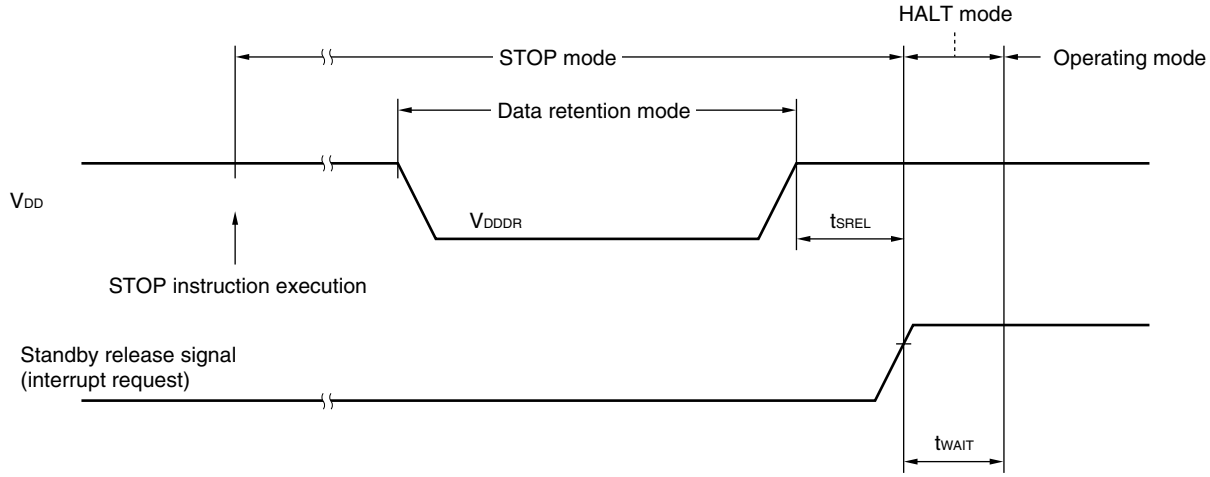
2. By using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register (OSTS), $2^{12}/f_X$, $2^{15}/f_X$, or $2^{17}/f_X$ can be selected.

Remark f_X: Main system clock oscillation frequency

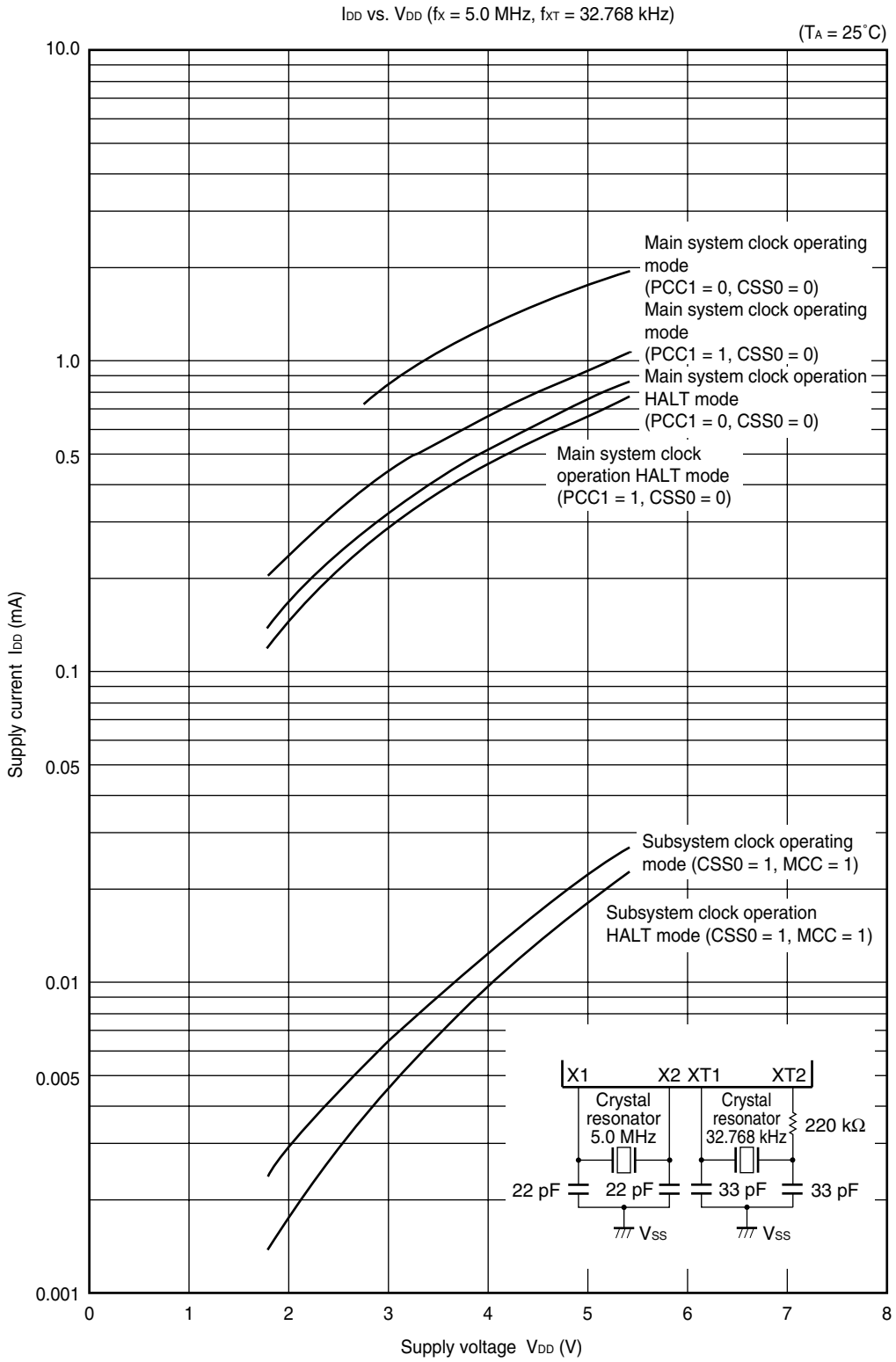
Data Retention Timing (STOP Mode Release by $\overline{RESET}$)

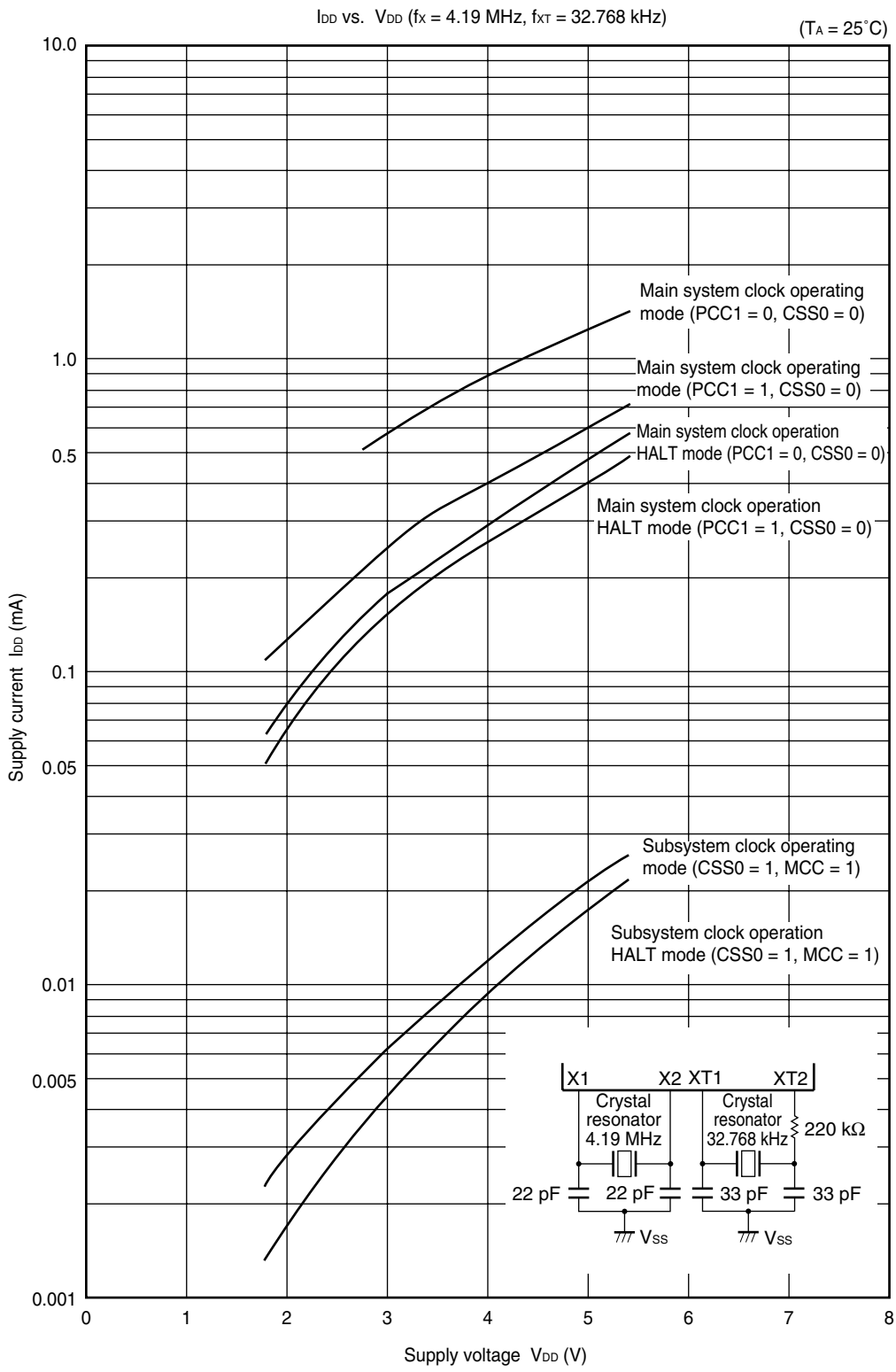


Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



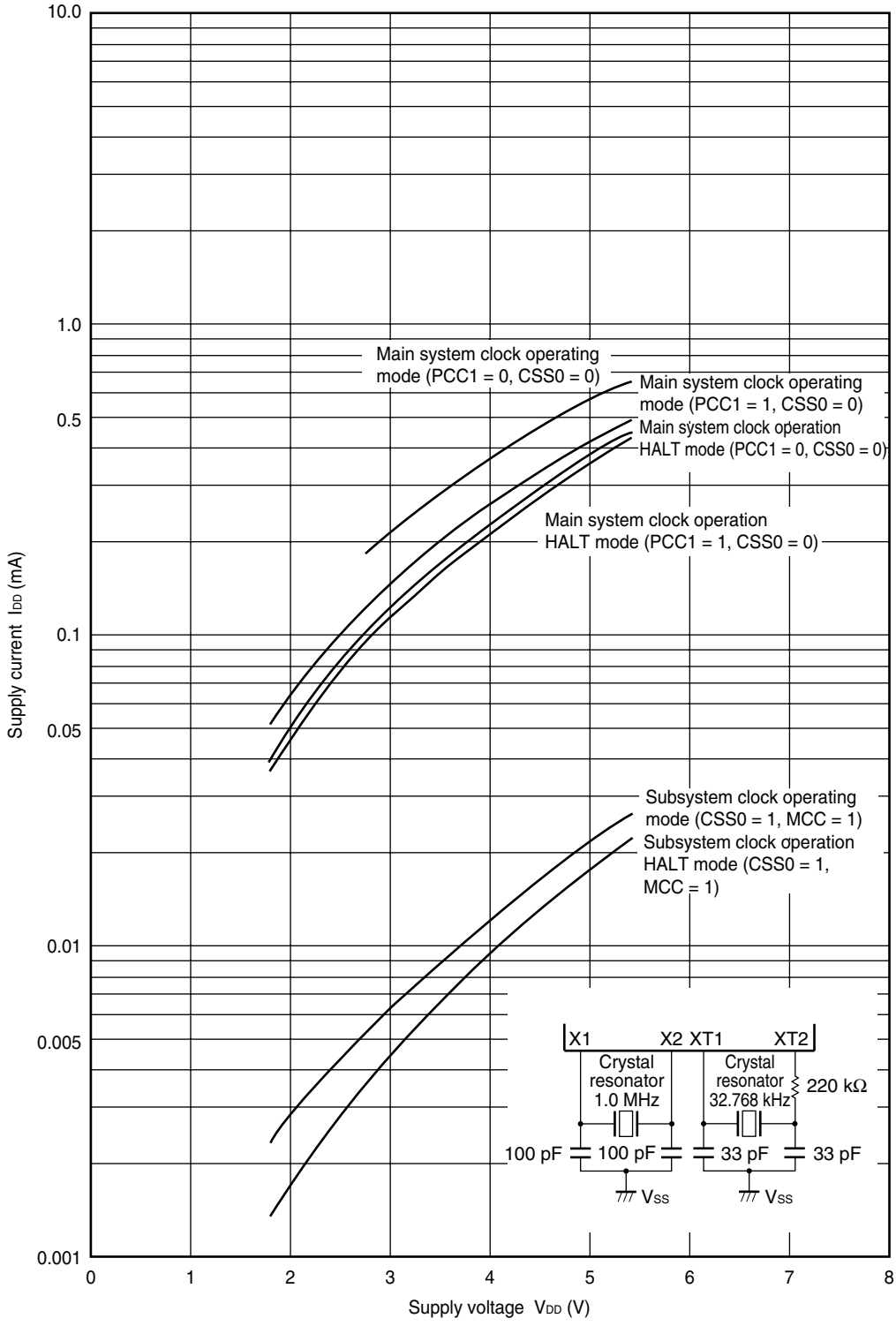
12. CHARACTERISTICS CURVES




IDD vs. VDD (fX = 4.19 MHz, fXT = 32.768 kHz)
(TA = 25°C)
Supply current IDD (mA)
Supply voltage VDD (V)
10.0
1.0
0.5
0.1
0.05
0.01
0.005
0.001
0
1
2
3
4
5
6
7
8
Main system clock operating mode (PCC1 = 0, CSS0 = 0)
Main system clock operating mode (PCC1 = 1, CSS0 = 0)
Main system clock operation HALT mode (PCC1 = 0, CSS0 = 0)
Main system clock operation HALT mode (PCC1 = 1, CSS0 = 0)
Subsystem clock operating mode (CSS0 = 1, MCC = 1)
Subsystem clock operation HALT mode (CSS0 = 1, MCC = 1)
X1
X2
XT1
XT2
Crystal resonator 4.19 MHz
Crystal resonator 32.768 kHz
220 kΩ
22 pF
22 pF
33 pF
33 pF
VSS
VSS

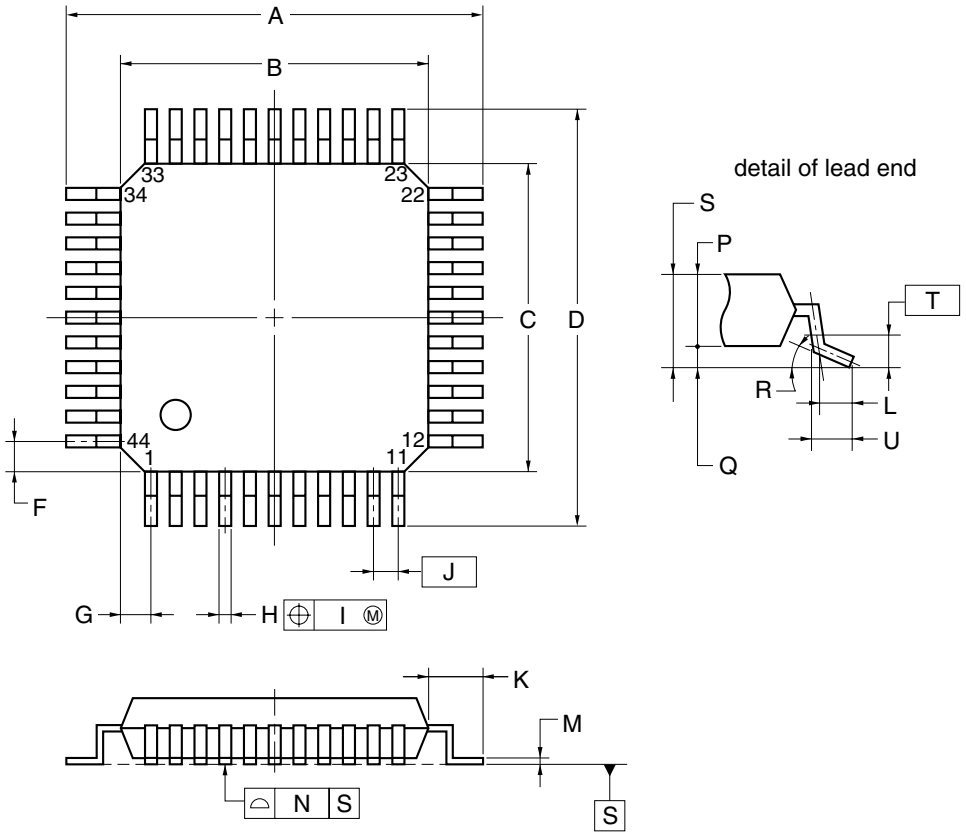
I_{DD} vs. V_{DD} (f_X = 1.0 MHz, f_{XT} = 32.768 kHz)

(T_A = 25°C)



13. PACKAGE DRAWING

44 PIN PLASTIC QFP (10x10)



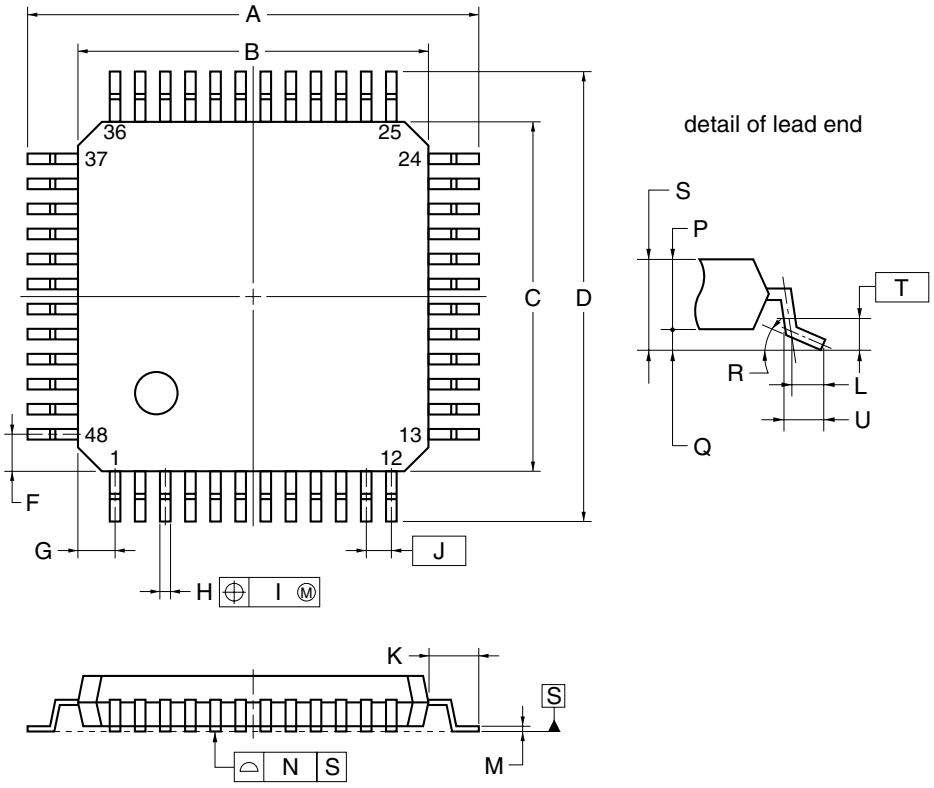
NOTE

Each lead centerline is located within 0.16 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	12.0±0.2
B	10.0±0.2
C	10.0±0.2
D	12.0±0.2
F	1.0
G	1.0
H	$0.37^{+0.08}_{-0.07}$
I	0.2
J	0.8 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.06}$
N	0.10
P	1.4±0.05
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.6 MAX.
U	0.6±0.15

S44GB-80-8ES-1

48-PIN PLASTIC TQFP (FINE PITCH) (7x7)



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.0±0.2
B	7.0±0.2
C	7.0±0.2
D	9.0±0.2
F	0.75
G	0.75
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.0±0.1
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.27 MAX.

P48GA-50-9EU

14. RECOMMENDED SOLDERING CONDITIONS

The μPD78916x, 78917x, 78916xY, 78917xY, 78916x(A), 78917x(A), 78916xY(A), and 78917xY(A) should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 14-1. Surface Mounting Type Soldering Conditions (1/2)

μPD789166GB-×××-8ES: 44-pin plastic LQFP (10 × 10 mm)
μPD789167GB-×××-8ES: 44-pin plastic LQFP (10 × 10 mm)
μPD789176GB-×××-8ES: 44-pin plastic LQFP (10 × 10 mm)
μPD789177GB-×××-8ES: 44-pin plastic LQFP (10 × 10 mm)
μPD789166YGB-×××-8ES: 44-pin plastic LQFP (10 × 10 mm)
μPD789167YGB-×××-8ES: 44-pin plastic LQFP (10 × 10 mm)
μPD789176YGB-×××-8ES: 44-pin plastic LQFP (10 × 10 mm)
μPD789177YGB-×××-8ES: 44-pin plastic LQFP (10 × 10 mm)
μPD789166GB(A)-×××-8ES: 44-pin plastic LQFP (10 × 10 mm)
μPD789167GB(A)-×××-8ES: 44-pin plastic LQFP (10 × 10 mm)
μPD789176GB(A)-×××-8ES: 44-pin plastic LQFP (10 × 10 mm)
μPD789177GB(A)-×××-8ES: 44-pin plastic LQFP (10 × 10 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Caution Do not use different soldering methods together (except for partial heating).

Table 14-1. Surface Mounting Type Soldering Conditions (2/2)

μPD789166YGA-×××-9EU: 48-pin plastic TQFP (7 × 7 mm)
μPD789167YGA-×××-9EU: 48-pin plastic TQFP (7 × 7 mm)
μPD789176YGA-×××-9EU: 48-pin plastic TQFP (7 × 7 mm)
μPD789177YGA-×××-9EU: 48-pin plastic TQFP (7 × 7 mm)
μPD789166YGA(A)-×××-9EU: 48-pin plastic TQFP (7 × 7 mm)
μPD789167YGA(A)-×××-9EU: 48-pin plastic TQFP (7 × 7 mm)
μPD789176YGA(A)-×××-9EU: 48-pin plastic TQFP (7 × 7 mm)
μPD789177YGA(A)-×××-9EU: 48-pin plastic TQFP (7 × 7 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less, Number of days:3[Note] (After that, prebaking is necessary at 125°C for 10 hours)	IR35-103-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Twice or less, Number of days:3[Note] (After that, prebaking is necessary at 125°C for 10 hours)	VP15-103-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note The number of days for storage at 25°C, 65% RH MAX after the dry pack has been opened.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for developing systems using the μPD78916x, 78917x, 78916xY, 78917xY, 78916x(A), 78917x(A), 78916xY(A), and 78917xY(A).

Language Processing Software

RA78K0S[Notes 1, 2, 3]	Assembler package common to 78K/0S Series
CC78K0S[Notes 1, 2, 3]	C compiler package common to 78K/0S Series
DF789177[Notes 1, 2, 3]	Device file for μPD78916x, 78917x, 78916xY, 78917xY, 78916x(A), 78917x(A), 78916xY(A), and 78917xY(A)
CC78K0S-L[Notes 1, 2, 3]	C compiler library source file common to 78K/0S Series

Flash Memory Writing Tools

Flashpro lll (Part No.: FL-PR3[Note 4], PG-FP3)	Flash programmer dedicated for on-chip flash memory microcontrollers
FA-44GB-8ES[Note 4]	Flash memory programming adapter for 44-pin plastic LQFP (GB-8ES type)
FA-48GA	Flash memory programming adapter for 48-pin plastic TQFP (fine pitch) (GA-9EU type)

★ **Debugging Tools (1/2)**

IE-78K0S-NS In-circuit emulator		In-circuit emulator used to debug hardware or software when application systems which use the 78K/0S Series are developed. The IE-78K0S-NS supports an integrated debugger (ID78K0S-NS). The IE-78K0S-NS is used in combination with an interface adapter for connection to an AC adapter, emulation probe, or host machine.
IE-78K0S-NS-A In-circuit emulator		The debugging function is enhanced by the addition of a coverage function and the tracer function and timer function are also enhanced.
IE-70000-MC-PS-B AC adapter		Adapter used to supply power from a 100- to 240-V AC outlet
IE-70000-98-IF-C Interface adapter		Adapter required when using the PC-9800 series (excluding notebook PCs) as the host machine (C bus supported)
IE-70000-CD-IF-A PC card/interface		PC card and interface cable required when using a notebook PC as the host machine (PCMCIA socket supported)
IE-70000-PC-IF-C Interface adapter		Adapter required when using an IBM PC/AT™ or compatible as the host machine (ISA bus supported)
IE-70000-PCI-IF-A Interface adapter		Adapter required when using a PC equipped with a PCI bus as the host machine
IE-789177-NS-EM1 Emulation board		Emulation board used to emulate the peripheral hardware specific to the device. This is used in combination with the in-circuit emulator.
NP-44GB-TQ[Note 4] Emulation probe		Board to connect an in-circuit emulator to the target system. This is used in combination with the TGB-044SAP.
	TGB-044SAP[Note 5] conversion socket	Conversion socket to connect the target system board on which a 44-pin plastic LQFP can be mounted and the NP-44GB-TQ

★ **Debugging Tools (2/2)**

NP-48GA[Note 4] Emulation probe		Board to connect an in-circuit emulator to the target system. This is used in combination with the TGA-048SDP.
	TGA-048SDP[Note 5] conversion socket	Conversion socket to connect the target system board on which a 48-pin plastic TQFP (fine pitch) can be mounted and the NP-48GA
SM78K0S[Notes 1, 2]		System simulator common to 78K/0S Series
ID78K0S-NS[Notes 1, 2]		Integrated debugger common to 78K/0S Series
DF789177[Notes 1, 2]		Device file for μPD78916x, 78917x, 78916xY, 78917xY, 78916x(A), 78917x(A), 78916xY(A), and 78917xY(A)

Notes 1. Based on the PC-9800 series (MS-DOS™ + Windows™)

2. Based on IBM PC/AT and compatibles (Japanese Windows/English Windows)

3. Based on the HP9000 series 700™ (HP-UX™), and SPARCstation™ (SunOS™, Solaris™)

4. Product made by and available from Naito Densei Machida Mfg. Co., Ltd. (+81-45-475-4191).

5. Product made by TOKYO ELETECH CORPORATION.
Refer to: Daimaru Kogyo, Ltd.
Tokyo Electronic Division (+81-3-3820-7112)
Osaka Electronic Division (+81-6-6244-6672)

Remark The RA78K0S, CC78K0S, ID78K0S-NS, and SM78K0S can be used in combination with the DF789177.

APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD789166, 167, 176, 177, 166Y, 167Y, 176Y, 177Y, 166(A), 167(A), 176(A), 177(A), 166Y(A), 167Y(A), 176Y(A), 177Y(A) Data Sheet	This manual
μPD78F9177, 78F9177Y Data Sheet	U14022E
μPD789167, 789177, 789167Y, 789177Y Subseries User's Manual	U14186E
78K/0S Series Instruction User's Manual	U11047E

Document Related to Development Tools (User's Manuals)

Document Name		Document No.
RA78K0S Assembler Package	Operation	U14876E
	Language	U14877E
	Structured Assembly Language	U11623E
CC78K0S C Compiler	Operation	U14871E
	Language	U14872E
SM78K0S, SM78K0 System Simulator Ver. 2.10 or Later	Operation (Windows Based)	U14611E
SM78K Series System Simulator Ver. 2.10 or Later	External Part User Open Interface Specifications	U15006E
ID78K0-NS, ID78K0S-NS Integrated Debugger Ver. 2.20 or Later	Operation (Windows Based)	U14910E
Project Manager Ver. 3.12 or later (Windows-based)		U14610E

Documents Related to Embedded Software (User's Manuals)

Document Name	Document No.
IE-78K0S-NS In-Circuit Emulator	U13549E
IE-78K0S-NS-A In-Circuit Emulator	U15207E
IE-789177-NS-EM1 Emulation Board	U14621E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Other Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE -Products & Packages-	X13769E
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Device	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

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[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Fax: 11-6462-6829

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