NEC

MOS INTEGRATED CIRCUITS

μPD784935A,784936A,784937A,784938A

16-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD784935A, 784936A, 784937A, and 784938A are members of the μPD784938A Subseries in the 78K/IV Series. These microcontrollers are based on the μPD784908 Subseries but are provided with the higher internal ROM and RAM capacities and a ROM correction function.

In addition, a flash memory version, μPD78F4938A, that can operate in the same power supply voltage range as the mask ROM version, and various development tools are also available.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD784938A Subseries User's Manual - Hardware: U13987E
78K/IV Series User's Manual - Instructions: U10905E

FEATURES

- 78K/IV Series
- Minimum instruction execution time:
  320 ns (fxx = 6.29 MHz)
  160 ns (fxx = 12.5 MHz)
- I/O ports: 80 pins
- Timers/counters: 16-bit timer/event counter × 1 unit
  8-/16-bit timer/event counter × 2 units
  8-/16-bit timer × 1 unit
- Serial interface: 4 channels
  - UART/IOE (3-wire serial I/O): 2 channels
  - CSI (3-wire serial I/O): 2 channels
- PWM output: 2 outputs
- Standby function
  HALT/STOP/IDLE mode
- Clock division function
- External expansion function
- Internal ROM correction function
- Watchdog timer: 1 channel
- Clock output function:
  Selectable from f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, and $f_{CLK}/16$
- A/D converter: 8-bit resolution × 8 channels
- IEBus™ controller
- Watch timer
- Low power consumption
- Supply voltage:
  - V_{DD} = 4.0 to 5.5 V (@12.58 MHz operation)
  - V_{DD} = 3.0 to 5.5 V (@6.29 MHz operation)

APPLICATION

Car audio, etc.

Unless otherwise specified, the μPD784938A is treated as the representative model in this document.

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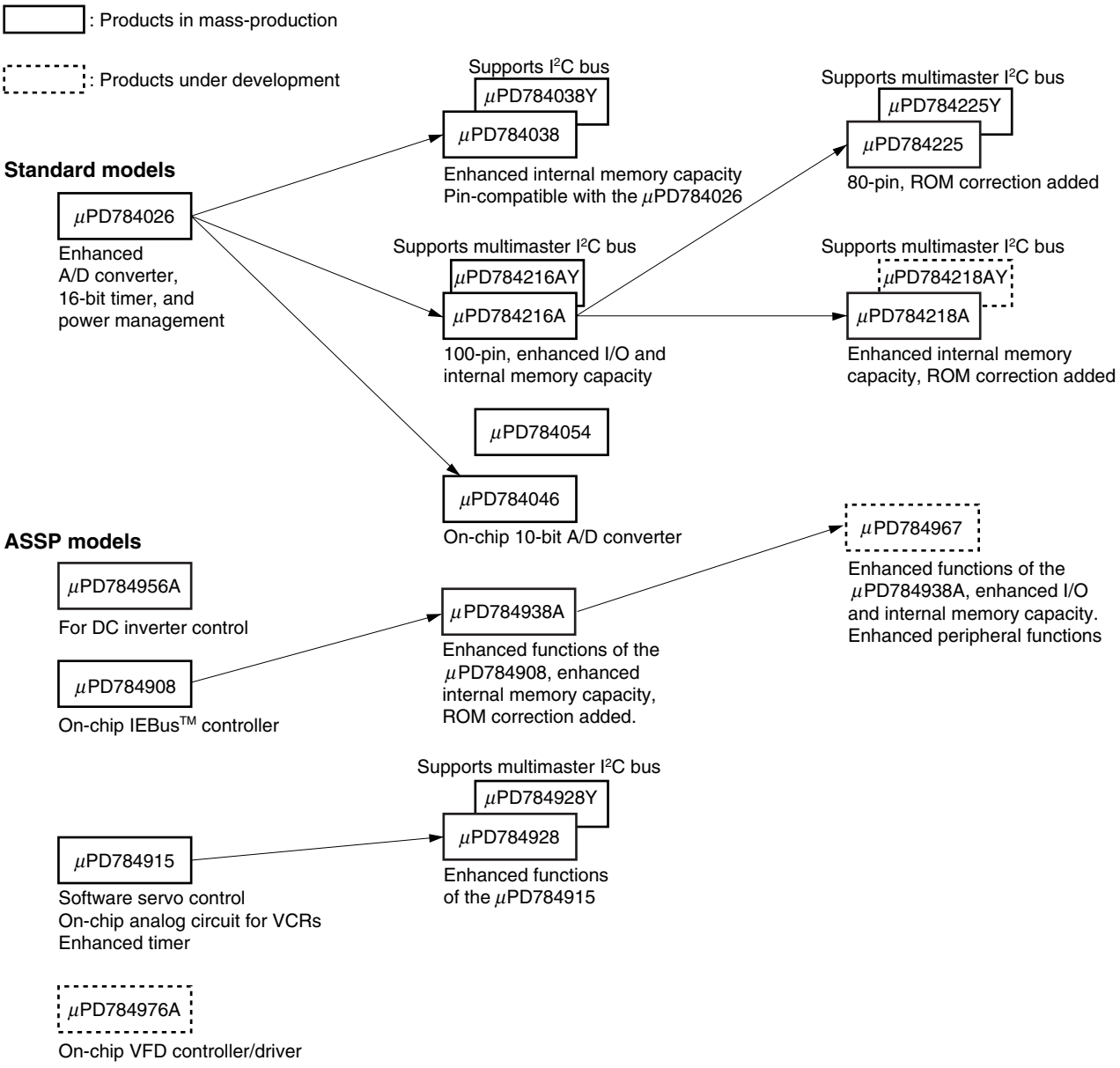
The mark ★ shows major revised points.

ORDERING INFORMATION

Part Number	Package	Internal ROM (bytes)	Internal RAM (bytes)
μPD784935AGF-×××-3BA	100-pin plastic QFP (14 × 20)	96 KB	5120 bytes
μPD784936AGF-×××-3BA	100-pin plastic QFP (14 × 20)	128 KB	6656 bytes
μPD784937AGF-×××-3BA	100-pin plastic QFP (14 × 20)	192 KB	8192 bytes
★ μPD784938AGF-×××-3BA	100-pin plastic QFP (14 × 20)	256 KB	10496 bytes

Remark ××× indicates ROM code suffix.

★ 78K/IV Series Product Development



FUNCTION LIST

(1/2)

Item \ Part Number		μPD784935A	μPD784936A	μPD784937A	μPD784938A
Number of basic instructions (mnemonics)		113			
General-purpose registers		8 bits × 32 registers × 8 banks, or 16 bits × 8 registers × 8 banks (memory map)			
Minimum instruction execution time		320 ns/636 ns/1.27 μs/2.54 μs (@6.29 MHz operation) 160 ns/320 ns/636 ns/1.27 μs (@12.58 MHz operation)			
Internal memory	ROM	96 KB	128 KB	192 KB	256 KB
	RAM	5120 bytes	6656 bytes	8192 bytes	10496 bytes
Memory space		1 MB with program and data spaces combined			
I/O port	Total	80 pins			
	Input	8 pins			
	I/O	72 pins			
Pins with ancillary function[Note]	LED direct drive output	24 pins			
	Transistor direct drive	8 pins			
	N-ch open drain drive	4 pins			
Real-time output port		4 bits × 2, or 8 bits × 1			
IEBus controller		Internal (simple version)			
Timer/counter		Timer/event counter 0: (16 bits) Timer counter × 1 Capture register × 1 Compare register × 2 Pulse output possible • Toggle output • PWM/PPG output • One-shot pulse output			
		Timer/event counter 1: (16 bits) Timer counter × 1 Capture register × 1 Capture/compare register × 1 Compare register × 1 Real-time output port			
		Timer/event counter 2: (16 bits) Timer counter × 1 Capture register × 1 Capture/compare register × 1 Compare register × 1 Pulse output possible • Toggle output • PWM/PPG output			
		Timer 3 (16 bits): Timer counter × 1 Compare register × 1			
Watch timer		Generates interrupt request at 0.5-second intervals (internal watch clock oscillator provided) Main clock (12.58 MHz) or watch clock (32.7 kHz) selectable as input clock			
Clock output		Selectable from f_{CLK}, $f_{CLK}/2$, $f_{CLK}/4$, $f_{CLK}/8$, or $f_{CLK}/16$ (also usable as 1-bit output port)			
PWM output		12-bit resolution × 2 channels			
Serial interface		UART/IOE (3-wire serial I/O): 2 channels (with internal baud rate generator) CSI (3-wire serial I/O): 2 channels			
A/D converter		8-bit resolution × 8 channels			
Watchdog timer		1 channel			
ROM correction function		Internal (4 points of correction addresses can be set.)			
External expansion function		Provided (up to 1 MB)			

Note Pins with ancillary functions are included in the I/O pins.

(2/2)

Item \ Part Number		μPD784935A	μPD784936A	μPD784937A	μPD784938A
Standby		HALT/STOP/IDLE mode			
Interrupt	Hardware source	27 (internal: 20, external: 7 (sampling clock variable input: 1))			
	Software source	BRK instruction, BRKCS instruction, operand error			
	Non-maskable	Internal: 1, external: 1			
	Maskable	Internal: 19, external: 6			
		Four programmable priority levels Three types of processing formats: Vectored interrupt/macro service/context switching			
Supply voltage		• V_{DD} = 4.0 to 5.5 V (@12.58 MHz operation) • V_{DD} = 3.0 to 5.5 V (@6.29 MHz operation)			
★ Package		100-pin plastic QFP (14 × 20)			

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1. DIFFERENCES BETWEEN PRODUCTS IN μPD784938A SUBSERIES

The only difference between the μPD784935A, 784936A, 784937A, and 784938A is the internal memory capacity.

The μPD78F4938A has a 256 KB flash memory in the place of the mask ROM of the above models. Table 1-1 shows the differences between these models.

★ **Table 1-1. Differences Between Products in μPD784938A Subseries**

Item \ Part Number	μPD784935A	μPD784936A	μPD784937A	μPD784938A	μPD78F4938A
Internal ROM	96 KB	128 KB	192 KB	256 KB	
	Mask ROM				Flash memory
Internal RAM	5120 bytes	6656 bytes	8192 bytes	10496 bytes	
Regulator	Provided				None
Electrical specifications	Refer to the Data Sheet of each product.				
Internal memory size switching register[Note]	None				Provided
IC pin	Provided				None
V_{PP} pin	None				Provided

Note The internal flash memory capacity and internal RAM capacity can be changed by using the internal memory size switching register (IMS).

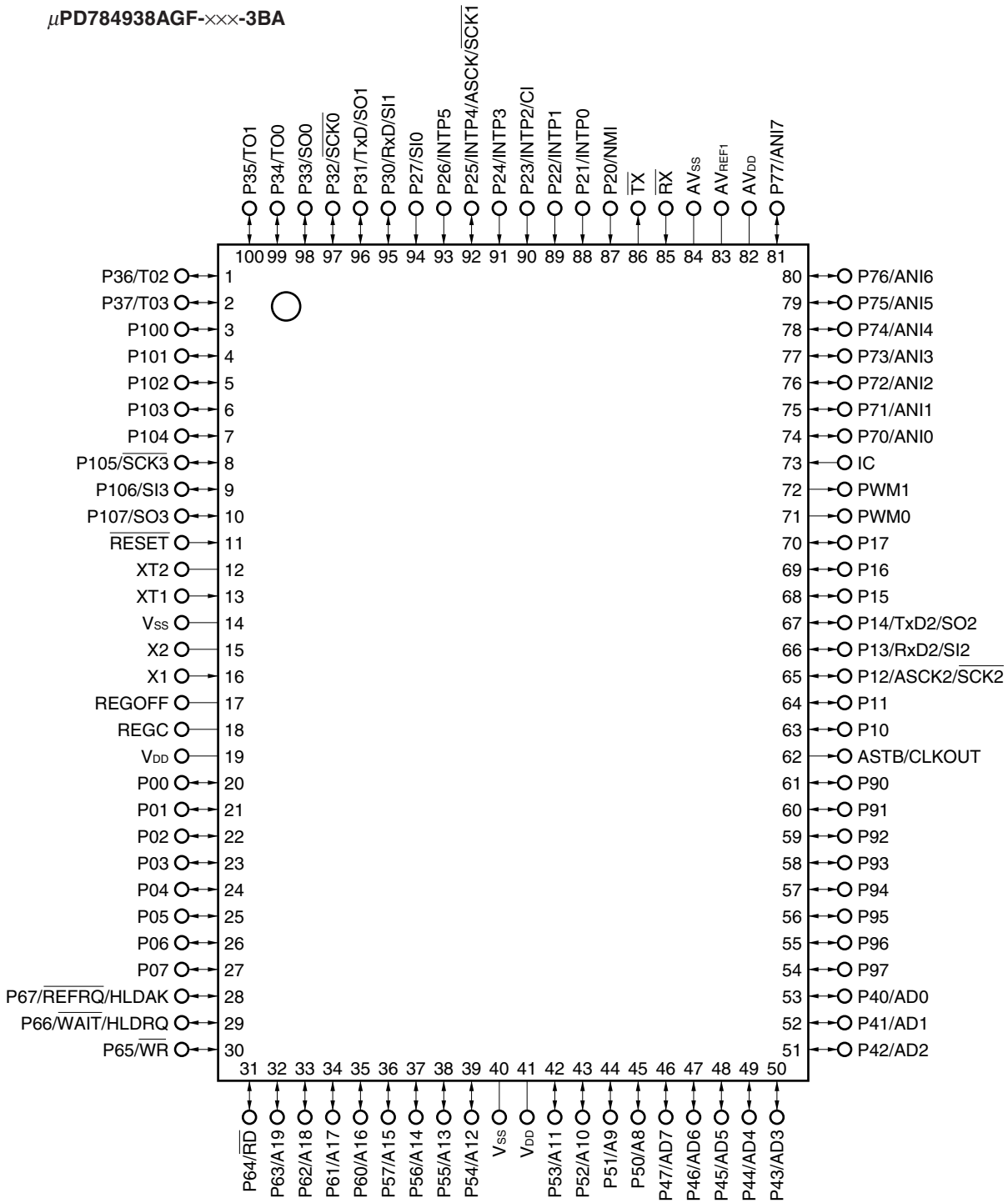
2. MAJOR DIFFERENCES BETWEEN μPD784908, μPD784038, AND μPD78098 SUBSERIES

Item \ Series Name		μPD784938A Subseries	μPD784908 Subseries	μPD784038 Subseries	μPD78098 Subseries
Number of basic instructions (mnemonics)		113			63
Minimum instruction execution time		160 ns (@12.5 MHz operation, internally)		125 ns (@32 MHz operation)	480 ns (@6.29 MHz operation)
Memory space (program data)		1 MB			60 KB
Timer/counter		16-bit timer/event counter × 1 8-/16-bit timer/event counter × 2 8-/16-bit timer × 1 Watch timer		16-bit timer/ event counter × 1 8-/16-bit timer/ event counter × 2 8-/16-bit timer × 1	16-bit timer/ event counter × 1 8-bit timer/ event counter × 2 Watch timer
		Single clock Watch clock provided for watch operation.		Single clock	Dual clock
Serial interface		UART/IOE (3-wire serial I/O): 2 channels (baud rate generator) CSI (3-wire serial I/O): 2 channels		UART/IOE (3-wire serial I/O): 2 channels CSI (3-wire serial I/O, 2-wire serial I/O): 1 channel	UART (3-wire serial I/O): 1 channel CSI/SBI (3-wire serial I/O): 1 channel CSI (3-wire serial I/O): 1 channel
PWM output		12-bit resolution × 2 channels			None
D/A converter		None		8-bit resolution × 2 channels	
Interrupt	Hardware source	27 sources		24 sources	23 sources (with two test flags)
	Internal	20 sources		17 sources	14 sources
	External	7 sources		7 sources	7 sources
External expansion function		Provided (up to 1 MB)			None
IEBus controller		Internal (simple version)		Not provided	Internal (complete hardware)
ROM correction		Internal (4 points can be set.)	Not provided		
Supply voltage		V_{DD} = 4.0 to 5.5 V	V_{DD} = 3.5 to 5.5 V (mask ROM versions) V_{DD} = 4.0 to 5.5 V (PROM versions)	V_{DD} = 2.7 to 5.5 V	V_{DD} = 2.7 to 6.0 V
★ Package		100-pin plastic QFP (14 × 20)	100-pin plastic QFP (14 × 20)	80-pin plastic QFP (14 × 14) 80-pin plastic TQFP (fine pitch) (14 × 14) 80-pin plastic WQFN (14 × 14): μPD78P4038 only	80-pin plastic TQFP (fine pitch) (14 × 14) 80-pin plastic WQFN (14 × 14): μPD78P098A only

Note Pins with ancillary functions are included in the I/O pins.

3. PIN CONFIGURATION (Top View)

- **100-pin plastic QFP (14 × 20)**
  μPD784935AGF-×××-3BA
  μPD784936AGF-×××-3BA
  μPD784937AGF-×××-3BA
★ **μPD784938AGF-×××-3BA**



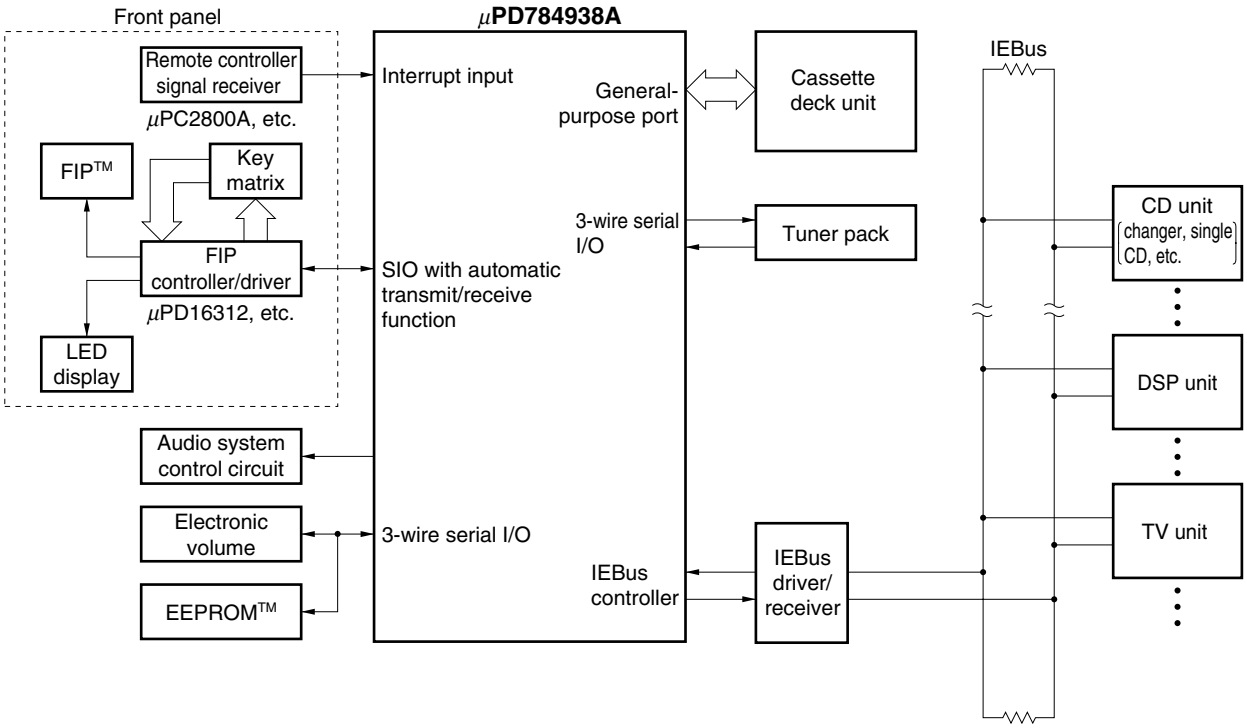
Cautions 1. Connect the IC (Internally Connected) pin directly to V_{SS}.

2. Connect the AV_{DD} pin directly to V_{DD}.

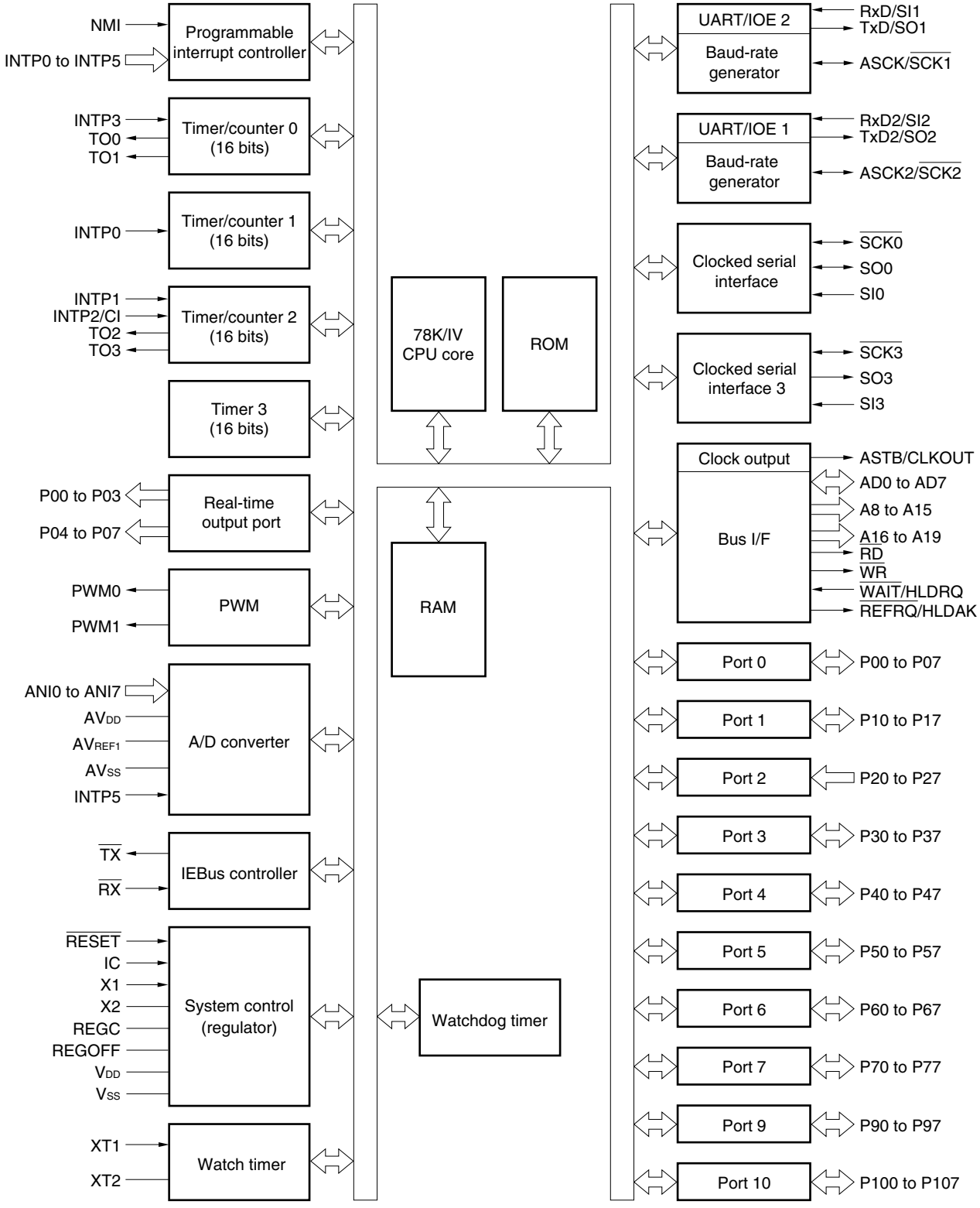
3. Connect the AV_{SS} pin directly to V_{SS}.

A8 to A19:	Address Bus
AD0 to AD7:	Address/Data Bus
ANI0 to ANI7:	Analog Input
ASCK, ASCK2:	Asynchronous Serial Clock
ASTB:	Address Strobe
AV_{DD}:	Analog Power Supply
AV_{REF1}:	Reference Voltage
AV_{SS}:	Analog Ground
CI:	Clock Input
CLKOUT:	Clock Output
HLDAK:	Hold Acknowledge
HLDRQ:	Hold Request
IC:	Internally Connected
INTP0 to INTP5:	Interrupt from Peripherals
NMI:	Non-maskable interrupt
P00 to P07:	Port0
P10 to P17:	Port1
P20 to P27:	Port2
P30 to P37:	Port3
P40 to P47:	Port4
P50 to P57:	Port5
P60 to P67:	Port6
P70 to P77:	Port7
P90 to P97:	Port9
P100 to P107:	Port10
PWM0, PWM1:	Pulse Width Modulation Output
$\overline{RD}$:	Read Strobe
$\overline{REFRQ}$:	Refresh Request
REGC:	Regulator Capacitance
REGOFF:	Regulator Off
$\overline{RESET}$:	Reset
$\overline{RX}$:	IEBus Receive Data
RxD, RxD2:	Receive Data
$\overline{SCK0}$ to $\overline{SCK3}$:	Serial Clock
SI0 to SI3:	Serial Input
SO0 to SO3:	Serial Output
TO0 to TO3:	Timer Output
$\overline{TX}$:	IEBus Transmit Data
TxD, TxD2:	Transmit Data
V_{DD}:	Power Supply
V_{SS}:	Ground
$\overline{WAIT}$:	Wait
$\overline{WR}$:	Write Strobe
X1, X2:	Crystal (Main System Clock)
XT1, XT2:	Crystal (Watch)

4. SYSTEM CONFIGURATION EXAMPLE (car audio system (tuner and deck))



5. BLOCK DIAGRAM



Remark The internal ROM and RAM capacities vary depending on the product.

6. PIN FUNCTIONS

6.1 Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function
P00 to P07	Input/ output	—	Port 0 (P0): • 8-bit I/O port. • Can be used as real-time output port (4 bits × 2). • Input/output can be specified in 1-bit units. • An on-chip pull-up resistor can be specified by means of software for pins in input mode. • Can drive transistor.
P10	Input/ output	—	Port 1 (P1): • 8-bit I/O port. • Input/output can be specified in 1-bit units. • An on-chip pull-up resistor can be specified by means of software for pins in input mode. • Can drive LED.
P11		—	
P12		ASCK2/$\overline{\text{SCK2}}$	
P13		RxD2/SI2	
P14		TxD2/SO2	
P15 to 17		—	
P20	Input	NMI	Port 2 (P2): • 8-bit input port. • P20 cannot be used as general-purpose port pin (non-maskable interrupt). However, input level can be checked by interrupt routine. • An on-chip pull-up resistor can be specified for P22 to P27 by means of software in 6-bit units. • P25/INTP4/ASCK/$\overline{\text{SCK1}}$ pin operates as $\overline{\text{SCK1}}$ I/O pin if so specified by CSIM1.
P21		INTP0	
P22		INTP1	
P23		INTP2/CI	
P24		INTP3	
P25		INTP4/ASCK/$\overline{\text{SCK1}}$	
P26		INTP5	
P27		SI0	
P30	Input/ output	RxD/SI1	Port 3 (P3): • 8-bit I/O port. • Input/output can be specified in 1-bit units. • An on-chip pull-up resistor can be specified by means of software for pins in input mode. • P32 and P33 can be specified for N-ch open-drain connection.
P31		TxD/SO1	
P32		$\overline{\text{SCK0}}$	
P33		SO0	
P34 to P37		TO0 to TO3	
P40 to P47	Input/ output	AD0 to AD7	Port 4 (P4): • 8-bit I/O port. • Input/output can be specified in 1-bit units. • An on-chip pull-up resistor can be specified by means of software for pins in input mode. • Can drive LED.
P50 to P57	Input/ output	A8 to A15	Port 5 (P5): • 8-bit I/O port. • Input/output can be specified in 1-bit units. • An on-chip pull-up resistor can be specified by means of software for pins in input mode. • Can drive LED.
P60 to P63	Input/ output	A16 to A19	Port 6 (P6): • 8-bit I/O port. • Input/output can be specified in 1-bit units. • An on-chip pull-up resistor can be specified by means of software for pins in input mode.
P64		$\overline{\text{RD}}$	
P65		$\overline{\text{WR}}$	
P66		$\overline{\text{WAIT}}$/HLDRQ	
P67		$\overline{\text{REFRQ}}$/HLDAK	

6.1 Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
P70 to P77	Input/ output	ANI0 to ANI7	Port 7 (P7): • 8-bit I/O port. • Input/output can be specified in 1-bit units.
P90 to P97	Input/ output	—	Port 9 (P9): • 8-bit I/O port. • Input/output can be specified in 1-bit units. • An on-chip pull-up resistor can be specified by means of software for pins in input mode.
P100 to P104	Input/ output	—	Port 10 (P10): • 8-bit I/O port. • Input/output can be specified in 1-bit units. • An on-chip pull-up resistor can be specified by means of software for pins in input mode. • P105 and P107 can be specified for N-ch open-drain connection.
P105		$\overline{\text{SCK3}}$	
P106		SI3	
P107		SO3	

6.2 Non-Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function	
TO0 to TO3	Output	P34 to P37	Timer output	
CI	Input	P23/INTP2	Count clock input to timer/counter 2	
RxD	Input	P30/SI1	Serial data input (UART0)	
RxD2		P13/SI2	Serial data input (UART2)	
TxD	Output	P31/SO1	Serial data output (UART0)	
TxD2		P14/SO2	Serial data output (UART2)	
ASCK	Input	P25/INTP4/$\overline{\text{SCK1}}$	Baud rate clock input (UART0)	
ASCK2		P12/$\overline{\text{SCK2}}$	Baud rate clock input (UART2)	
SI0	Input	P27	Serial data input (3-wire serial I/O0)	
SI1		P30/RxD	Serial data input (3-wire serial I/O1)	
SI2		P13/RxD2	Serial data input (3-wire serial I/O2)	
SI3		P106	Serial data input (3-wire serial I/O3)	
SO0	Output	P33	Serial data output (3-wire serial I/O0)	
SO1		P31/TxD	Serial data output (3-wire serial I/O1)	
SO2		P14/TxD2	Serial data output (3-wire serial I/O2)	
SO3		P107	Serial data output (3-wire serial I/O3)	
$\overline{\text{SCK0}}$	Input/	P32	Serial clock input/output (3-wire serial I/O0)	
$\overline{\text{SCK1}}$	output	P25/INTP4/ASCK	Serial clock input/output (3-wire serial I/O1)	
$\overline{\text{SCK2}}$		P12/ASCK2	Serial clock input/output (3-wire serial I/O2)	
$\overline{\text{SCK3}}$		P105	Serial clock input/output (3-wire serial I/O3)	
NMI	Input	P20	External interrupt requests	—
INTP0		P21		• Count clock input to timer/counter 1 • Capture trigger signal of CR11 or CR12
INTP1		P22		• Count clock input to timer/counter 2 • Capture trigger signal of CR22
INTP2		P23/CI		• Count clock input to timer/counter 2 • Capture trigger signal of CR21
INTP3		P24		• Count clock input to timer/counter 0 • Capture trigger signal of CR02
INTP4		P25/ASCK/$\overline{\text{SCK1}}$		—
INTP5		P26		Conversion start trigger input of A/D converter
AD0 to AD7	Input/ output	P40 to P47	Time-division address/data bus (external memory connection)	
A8 to A15	Output	P50 to P57	Higher address bus (external memory connection)	
A16 to A19	Output	P60 to P63	Higher address for address extension (external memory connection)	
$\overline{\text{RD}}$	Output	P64	Read strobe to external memory	
$\overline{\text{WR}}$	Output	P65	Write strobe to external memory	
$\overline{\text{WAIT}}$	Input	P66/HLDRQ	Wait insertion	
$\overline{\text{REFRQ}}$	Output	P67/HLDAK	Refresh pulse output to external pseudo-static memory	
HLDRQ	Input	P66/$\overline{\text{WAIT}}$	Bus hold request input	
HLDAK	Output	P67/$\overline{\text{REFRQ}}$	Bus hold acknowledge output	
ASTB	Output	CLKOUT	Latch timing output of time-division address (A0 to A7) (when external memory is accessed)	

6.2 Non-Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
CLKOUT	Output	ASTB	Clock output
PWM0	Output	—	PWM output 0
PWM1	Output	—	PWM output 1
$\overline{RX}$	Input	—	Data input (IEBus)
$\overline{TX}$	Output	—	Data output (IEBus)
REGC	—	—	Capacitor connection for regulation output stabilization/power supply when regulator is stopped
REGOFF	—	—	Regulator operation specification signal
$\overline{RESET}$	Input	—	Chip reset
X1	Input	—	Crystal connection for system clock oscillation (clock can be also input to X1.)
X2	—		
XT1	Input	—	Watch clock connection
XT2	—	—	
ANI0 to ANI7	Input	P70 to P77	Analog voltage input for A/D converter
AV_{REF1}	—	—	Application of reference voltage for A/D converter
AV_{DD}			Positive power supply for A/D converter
AV_{SS}			GND for A/D converter
V_{DD}			Positive power supply
V_{SS}			GND
IC	Input		Internally connected. Connect this pin directly to V_{SS} (this pin is used to test the IC.)

6.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 6-1.

For the input/output circuit configuration of each type, refer to **Figure 6-1**.

Table 6-1. Types of Pin Input/Output Circuits (1/2)

Pin Name	Input/output Circuit Type	I/O	Recommended Connection of Unused Pins
P00 to P07	5-A	Input/output	Input: Connect to V_{DD}.
P10, P11			Output: Leave open.
P12/ASCK2/$\overline{SCK2}$	8-A		
P13/RxD2/SI2	5-A		
P14/TxD2/SO2			
P15 to P17			
P20/NMI	2	Input	Connect to V_{DD} or V_{SS}.
P21/INTP0			
P22/INTP1	2-A		Connect to V_{DD}.
P23/INTP2/CI			
P24/INTP3			
P25/INTP4/ASCK/$\overline{SCK1}$	8-A	Input/output	Input: Connect to V_{DD}.
			Output: Leave open.
P26/INTP5	2-A	Input	Connect to V_{DD}.
P27/SI0			
P30/RxD/SI1	5-A	Input/output	Input: Connect to V_{DD}.
P31/TxD/SO1			Output: Leave open.
P32/$\overline{SCK0}$	10-A		
P33/SO0			
P34/TO0 to P37/TO3	5-A		
P40/AD0 to P47/AD7			
P50/A8 to P57/A15			
P60/A16 to P63/A19			
P64/$\overline{RD}$			
P65/$\overline{WR}$			
P66/$\overline{WAIT}$/HLDRQ			
P67/$\overline{REFRQ}$/HLDAK			
P70/ANI0 to P77/ANI7	20	Input/output	Input: Connect to V_{DD} or V_{SS}.
P90 to P97	5-A		Output: Leave open.
P100 to P104			
P105/$\overline{SCK3}$	10-A		
P106/SI3	8-A		
P107/SO3	10-A		
ASTB/CLKOUT	4	Output	Leave open.
$\overline{RESET}$	2	Input	—
IC	1		Connect directly to V_{SS}.
XT2	—	—	Leave open.
XT1	—	Input	Connect directly to V_{SS}.

Table 6-1. Types of Pin Input/Output Circuits (2/2)

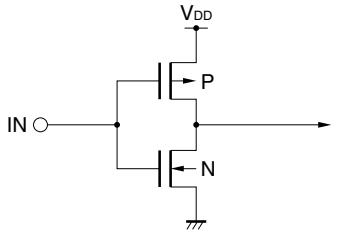
Pin Name	Input/output Circuit Type	I/O	Recommended Connection of Unused Pins
REGOFF	1	—	Connect directly to V_{DD}.
REGC	—	—	Connect to V_{DD}.
PWM0, PWM1	3	Output	Leave open.
$\overline{RX}$	1	Input	Connect to V_{DD} or V_{SS}.
$\overline{TX}$	3	Output	Leave open.
AV_{REF1}	—	—	Connect to V_{SS}.
AV_{SS}			
AV_{DD}			Connect to V_{DD}.

Caution Connect an I/O pin to V_{DD} via a resistor of several 10 kΩ if the I/O mode of the pin is unstable (especially if the voltage on the reset pin is higher than the low-level input voltage on power application or if the mode is changed between input and output by software).

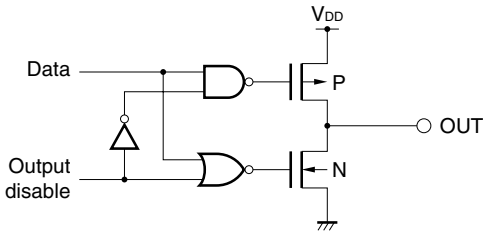
Remark The circuit type numbers are common for the 78K series and are not always sequential for one product (some circuits are not provided).

Figure 6-1. Pin Input/Output Circuits (1/2)

Type 1

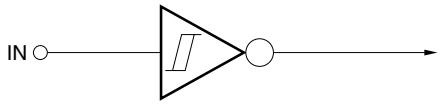


Type 4



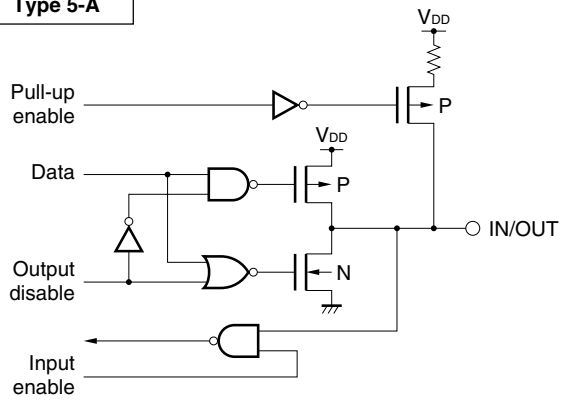
Push-pull output that can go into a high-impedance state (both P-ch and N-ch are off).

Type 2

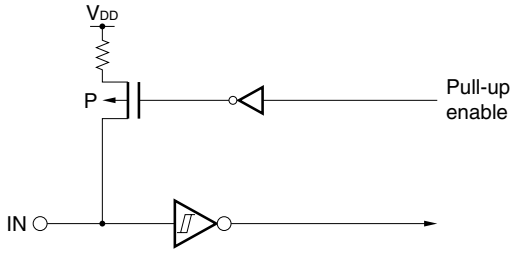


Schmitt triggered input with hysteresis characteristics

Type 5-A

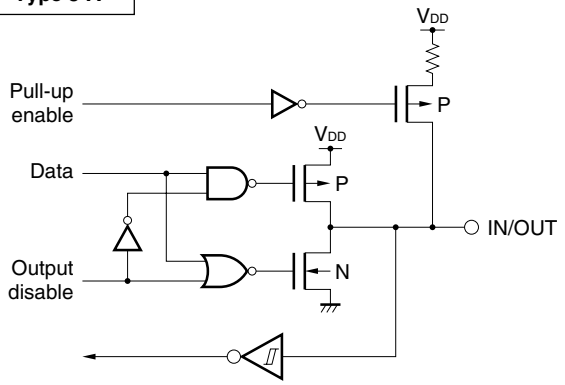


Type 2-A

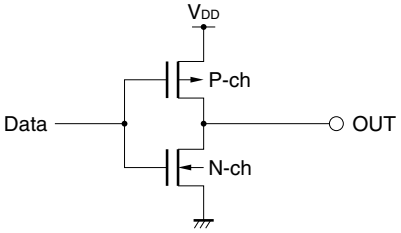


Schmitt triggered input with hysteresis characteristics

Type 8-A



Type 3



Type 10-A

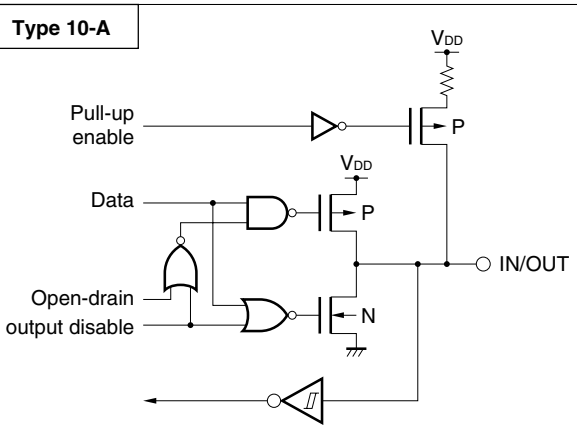
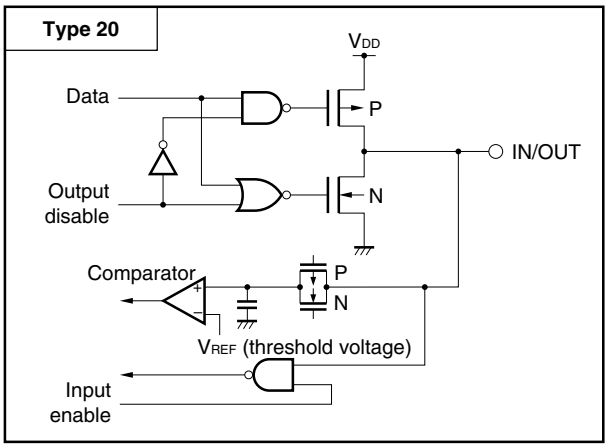


Figure 6-1. Pin Input/Output Circuits (2/2)



7. CPU ARCHITECTURE

7.1 Memory Space

A memory space of 1 MB can be accessed. Mapping of the internal data area (special function registers and internal RAM) can be selected by using the LOCATION instruction. The LOCATION instruction must be always executed after the reset signal has been cleared, and must not be used more than once.

(1) When LOCATION 0H instruction is executed

- **Internal memory**

  The internal data area and internal ROM area are as follows:

Part Number	Internal Data Area	Internal ROM Area
μPD784935A	0EB00H to 0FFFFH	00000H to 0EAFFH 10000H to 17FFFH
μPD784936A	0E500H to 0FFFFH	00000H to 0E4FFH 10000H to 1FFFFH
μPD784937A	0DF00H to 0FFFFH	00000H to 0DEFFH 10000H to 2FFFFH
★ μPD784938A	0D600H to 0FFFFH	00000H to 0D5FFH 10000H to 3FFFFH

Caution The following area of the internal ROM that overlaps the internal data area cannot be used when the LOCATION 0H instruction is executed.

Part Number	Unusable Area
μPD784935A	0EB00H to 0FFFFH (5376 bytes)
μPD784936A	0E500H to 0FFFFH (6192 bytes)
μPD784937A	0DF00H to 0FFFFH (8448 bytes)
★ μPD784938A	0D600H to 0FFFFH

- **External memory**

  The external memory is accessed in the external memory expansion mode.

(2) When LOCATION 0FH instruction is executed

- **Internal memory**

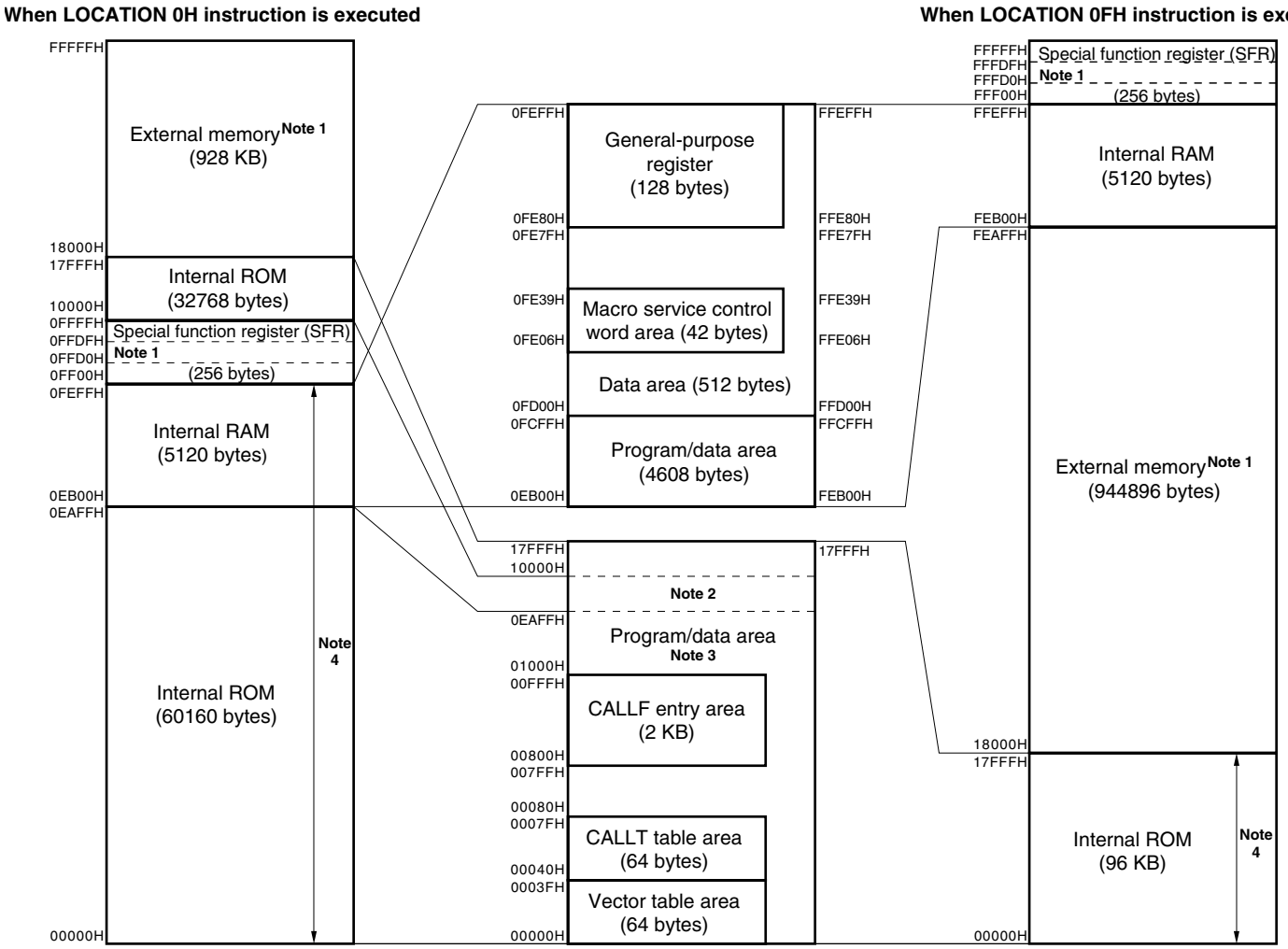
  The internal data area and internal ROM area are as follows:

Part Number	Internal Data Area	Internal ROM Area
μPD784935A	FEB00H to FFFFFH	00000H to 17FFFH
μPD784936A	FE500H to FFFFFH	00000H to 1FFFFH
μPD784937A	FDF00H to FFFFFH	00000H to 2FFFFH
★ μPD784938A	FD600H to FFFFFH	00000H to 3FFFFH

- **External memory**

  The external memory is accessed in the external memory expansion mode.

Figure 7-1. Memory Map of μPD784935A



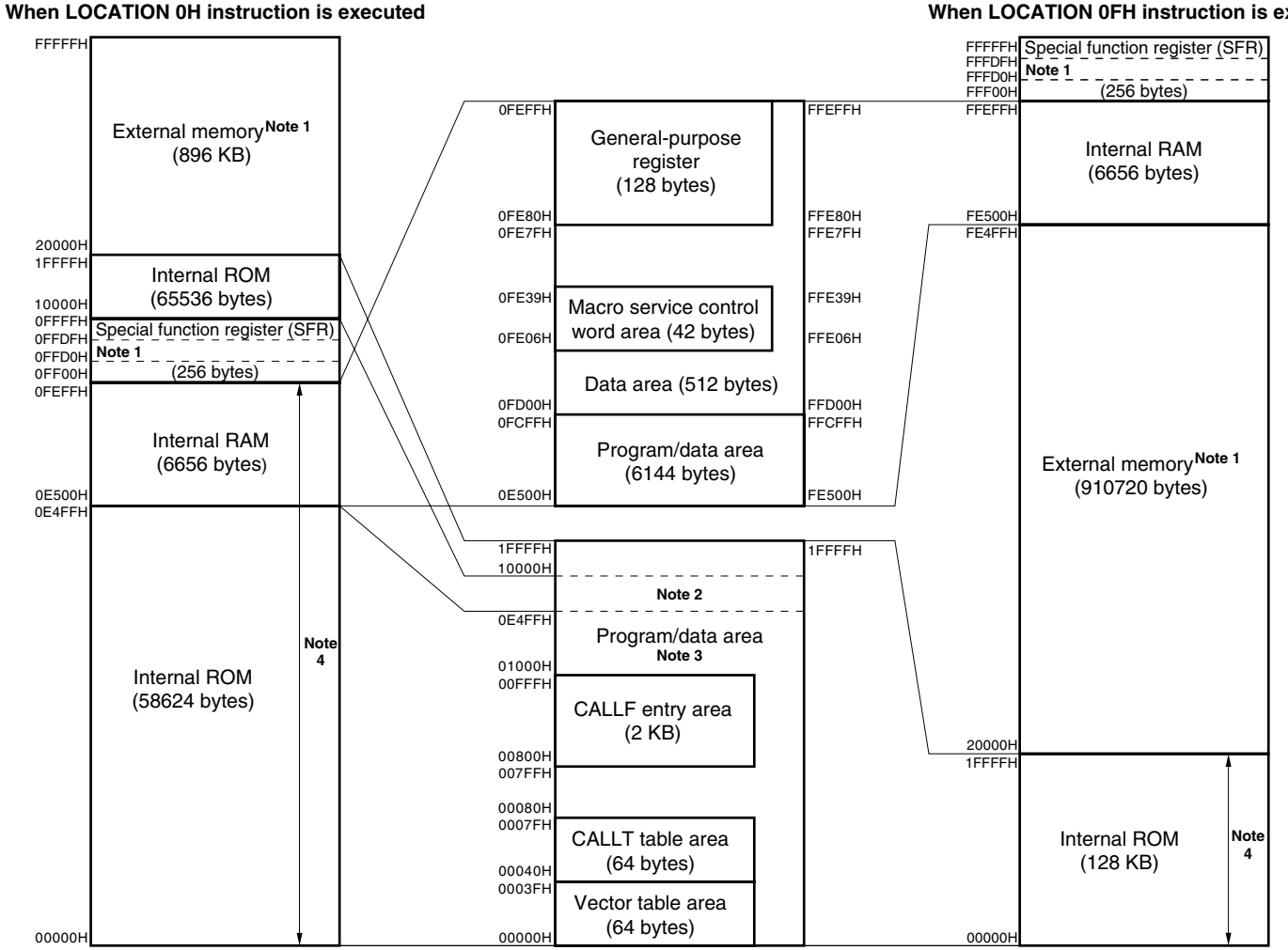
Notes 1. Accessed in the external memory expansion mode.

2. 5376 bytes in this area can be used as an internal ROM area only when the LOCATION 0FH instruction is executed.

3. When LOCATION 0H instruction is executed: 92928 bytes, when LOCATION 0FH instruction is executed: 98304 bytes

4. Base area, or entry area used in the case of reset or interrupt. However, the internal RAM is excluded in the case of reset.

Figure 7-2. Memory Map of μPD784936A



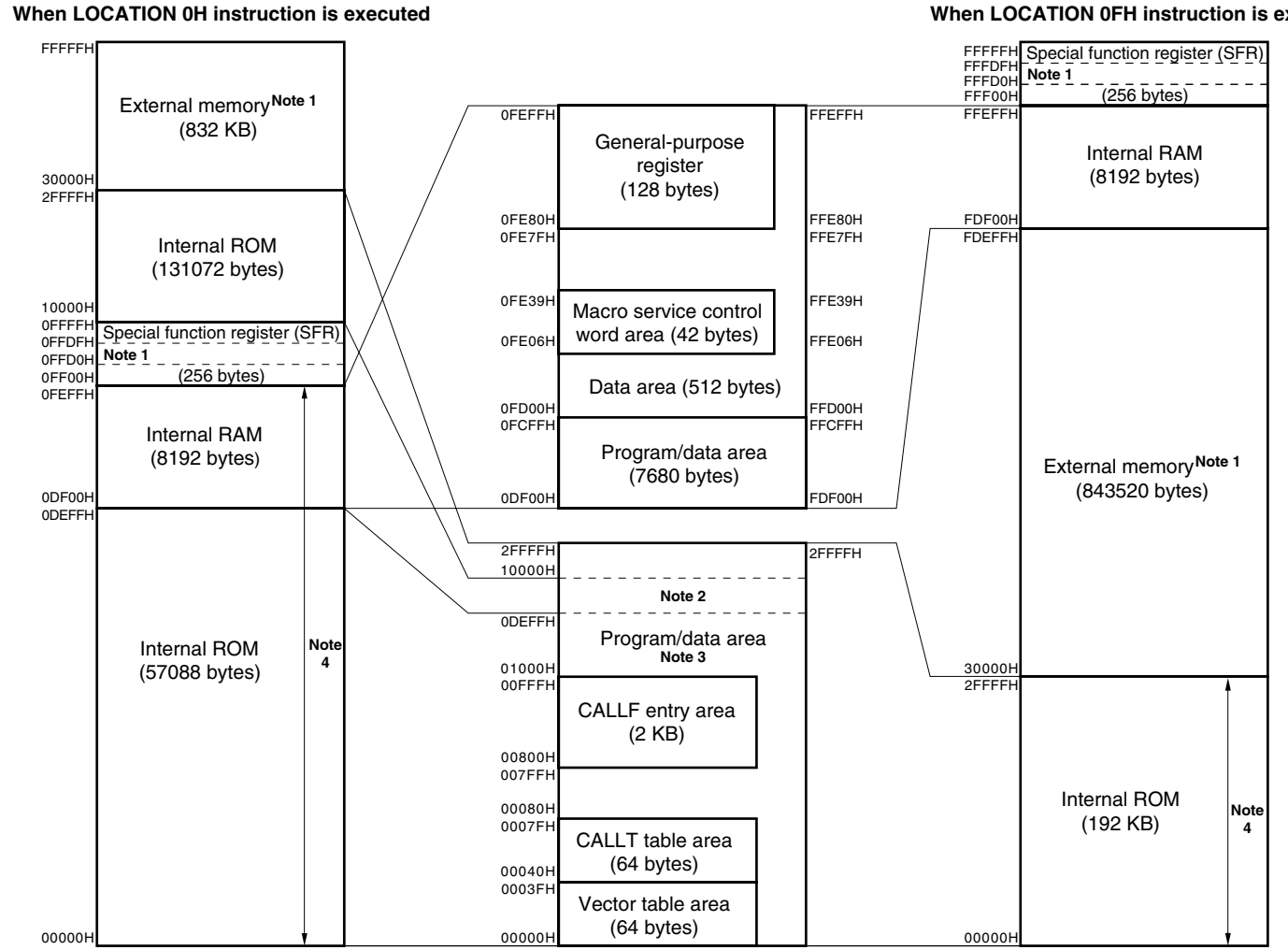
Notes 1. Accessed in the external memory expansion mode.

2. 6912 bytes in this area can be used as an internal ROM area only when the LOCATION 0FH instruction is executed.

3. When LOCATION 0H instruction is executed: 124160 bytes, when LOCATION 0FH instruction is executed: 131072 bytes

4. Base area, or entry area used in the case of reset or interrupt. However, the internal RAM is excluded in the case of reset.

Figure 7-3. Memory Map of μPD784937A



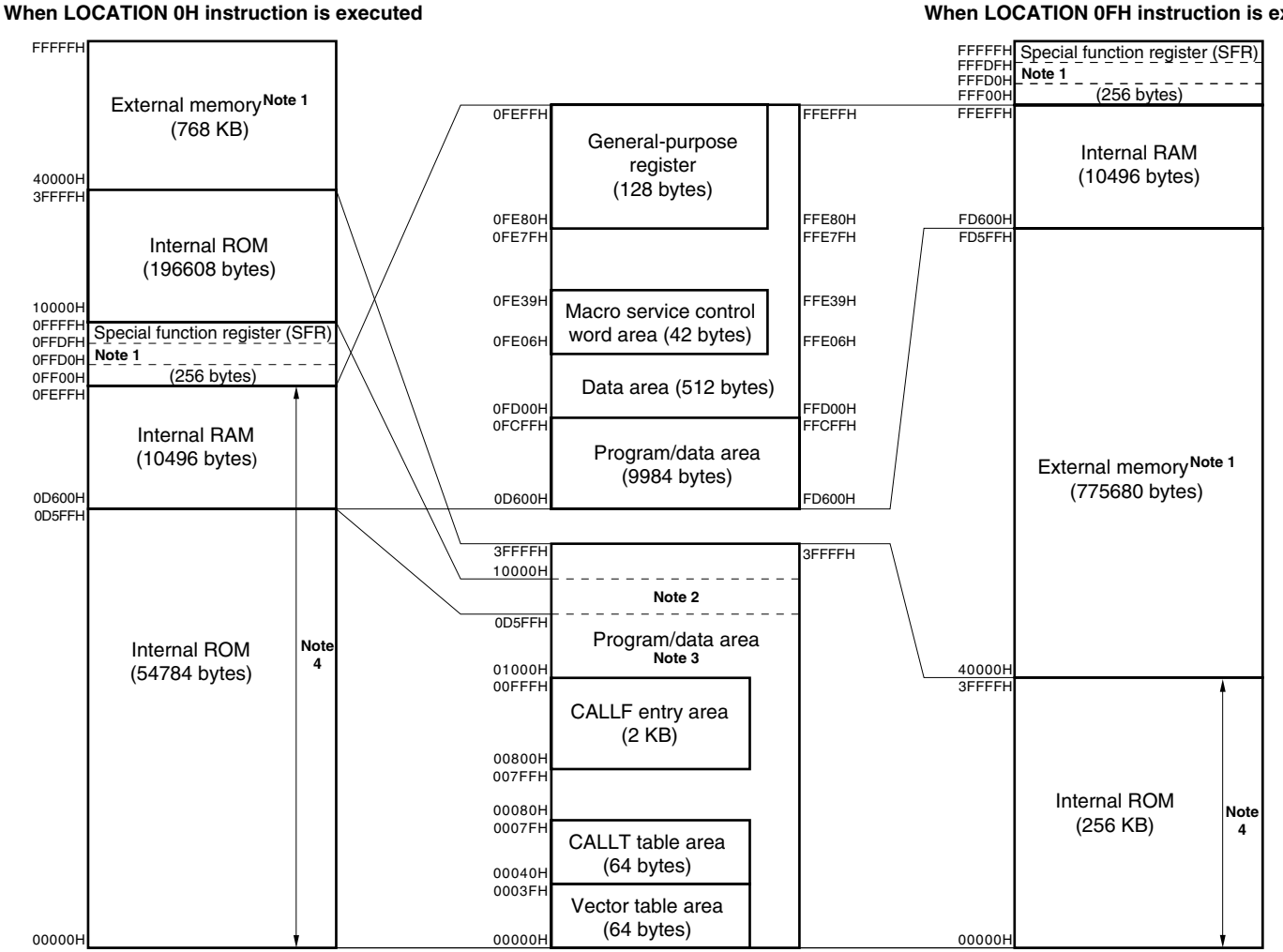
Notes 1. Accessed in the external memory expansion mode.

2. 8448 bytes in this area can be used as an internal ROM area only when the LOCATION 0FH instruction is executed.

3. When LOCATION 0H instruction is executed: 188160 bytes, when LOCATION 0FH instruction is executed: 196608 bytes

4. Base area, or entry area used in the case of reset or interrupt. However, the internal RAM is excluded in the case of reset.

Figure 7-4. Memory Map of μPD784938A



Notes 1. Accessed in the external memory expansion mode.

2. 10752 bytes in this area can be used as an internal ROM area only when the LOCATION 0FH instruction is executed.

3. When LOCATION 0H instruction is executed: 251392 bytes, when LOCATION 0FH instruction is executed: 262144 bytes

4. Base area, or entry area used in the case of reset or interrupt. However, the internal RAM is excluded in the case of reset.

7.2 CPU Registers

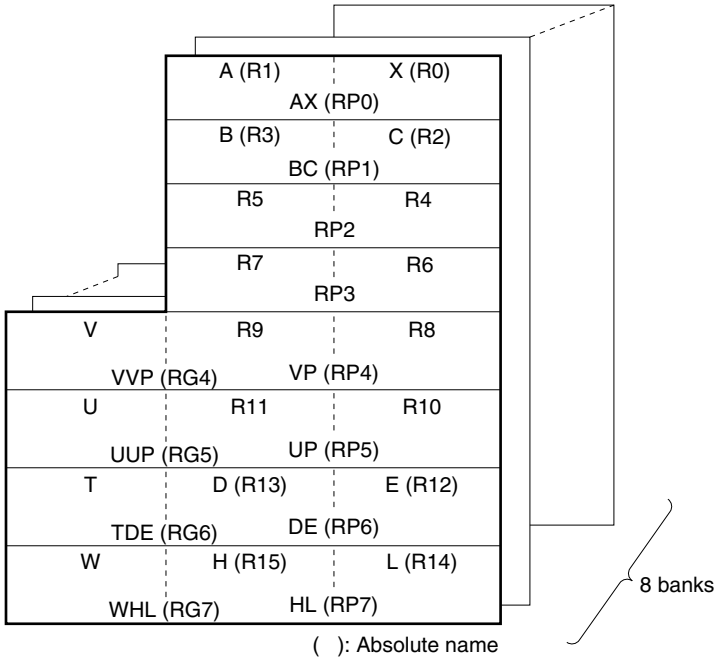
7.2.1 General-purpose registers

Sixteen 8-bit general-purpose registers are available. Two 8-bit general-purpose registers can be used in combination as a 16-bit general-purpose register. Four of the 16-bit registers can be used in combination with an 8-bit register for address extension as 24-bit address specification registers.

Eight banks of register sets are available, which can be selected by software or using the context switching function.

The general-purpose registers, except registers V, U, T, and W for address extension, are mapped to the internal RAM.

Figure 7-5. General-Purpose Register Format



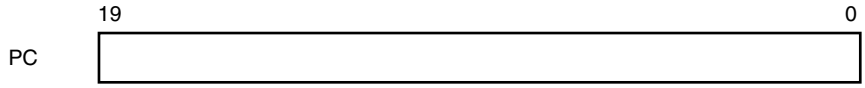
Caution R4, R5, R6, R7, RP2, and RP3 can be used as X, A, C, B, AX, and BC registers, respectively, by setting the RSS bit of PSW to 1. However, use this function only when using a program written for the 78K/III series.

7.2.2 Control registers

(1) Program counter (PC)

The contents of this 20-bit counter are automatically updated as a program is executed.

Figure 7-6. Format of Program Counter (PC)



(2) Program status word (PSW)

This register holds the status of the CPU. Its contents are automatically updated as a program is executed.

Figure 7-7. Format of Program Status Word (PSW)

		15	14	13	12	11	10	9	8
PSW	PSWH	UF	RBS2	RBS1	RBS0	–	–	–	–
		7	6	5	4	3	2	1	0
	PSWL	S	Z	RSS[Note]	AC	IE	P/V	0	CY

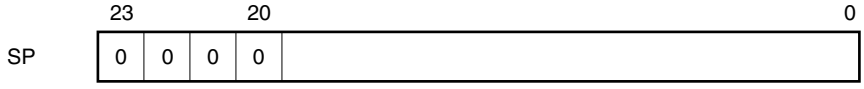
Note This flag is used to maintain compatibility with the 78K/III series. Keep this flag cleared to 0 except when using the software written for the 78K/III series.

(3) Stack pointer (SP)

This is a 24-bit pointer that holds the first address of the stack.

Be sure to write 0 to the higher 4 bits of this pointer.

Figure 7-8. Format of Stack Pointer (SP)



7.2.3 Special function registers (SFRs)

The special function registers (SFRs) are registers having a special function, such as the mode registers and control registers of the on-chip peripheral hardware, and are mapped to a 256-byte space of addresses 0FF00H to 0FFFFH[Note].

Note This is the case when the LOCATION 0H instruction is executed. They are mapped to FFF00H to FFFFFH when the LOCATION 0FH instruction is executed.

Caution Do not access an address in this area to which no SFR is allocated. If such an address is accessed by mistake, the μPD784938A may be deadlocked. The deadlock status can be released only by a reset.

Table 7-1 lists the special function registers (SFRs). The meanings of the symbols in this table are as follows:

- Abbreviation ..... Abbreviation of the SFR. This abbreviation is reserved for use with NEC's assembler (RA78K4). With the C compiler (CC78K4), this abbreviation can be used as an sfr variable when the #pragma sfr command is used.
- R/W ..... Indicates whether the SFR can be read or written.
  - R/W: Read/Write
  - R: Read only
  - W: Write only
- Bit Units for Manipulation ..... Indicates the bit units in which the SFR can be manipulated. An SFR that can be manipulated in 16-bit units can be written as operand sfrp. When specifying the SFR using an address, use the even address.
  An SFR that can be manipulated in 1-bit units can be written with a bit manipulation instruction.
- After Reset ..... Indicates the status of the register when the $\overline{\text{RESET}}$ signal is input.

Table 7-1. Special Function Register (SFR) List (1/4)

Address[Note]	Special Function Register (SFR) Name	Abbreviation		R/W	Bit Units for Manipulation			After Reset
					1 bit	8 bits	16 bits	
0FF00H	Port 0	P0		R/W	√	√	—	Undefined
0FF01H	Port 1	P1			√	√	—	
0FF02H	Port 2	P2		R	√	√	—	
0FF03H	Port 3	P3		R/W	√	√	—	
0FF04H	Port 4	P4			√	√	—	
0FF05H	Port 5	P5			√	√	—	
0FF06H	Port 6	P6			√	√	—	00H
0FF07H	Port 7	P7			√	√	—	Undefined
0FF09H	Port 9	P9			√	√	—	
0FF0AH	Port 10	P10			√	√	—	
0FF0EH	Port 0 buffer register L	P0L			√	√	—	
0FF0FH	Port 0 buffer register H	P0H			√	√	—	
0FF10H	Compare register (timer/counter 0)	CR00			—	—	√	
0FF12H	Capture/compare register (timer/counter 0)	CR01			—	—	√	
0FF14H	Compare register L (timer/counter 1)	CR10	CR10W		—	√	√	
0FF15H	Compare register H (timer/counter 1)	—			—	—		
0FF16H	Capture/compare register L (timer/counter 1)	CR11	CR11W		—	√	√	
0FF17H	Capture/compare register H (timer/counter 1)	—			—	—		
0FF18H	Compare register L (timer/counter 2)	CR20	CR20W		—	√	√	
0FF19H	Compare register H (timer/counter 2)	—			—	—		
0FF1AH	Capture/compare register L (timer/counter 2)	CR21	CR21W		—	√	√	
0FF1BH	Capture/compare register H (timer/counter 2)	—			—	—		
0FF1CH	Compare register L (timer 3)	CR30	CR30W		—	√	√	
0FF1DH	Compare register H (timer 3)	—			—	—		
0FF20H	Port 0 mode register	PM0			√	√	—	FFH
0FF21H	Port 1 mode register	PM1			√	√	—	
0FF23H	Port 3 mode register	PM3			√	√	—	
0FF24H	Port 4 mode register	PM4			√	√	—	
0FF25H	Port 5 mode register	PM5			√	√	—	
0FF26H	Port 6 mode register	PM6			√	√	—	
0FF27H	Port 7 mode register	PM7			√	√	—	
0FF29H	Port 9 mode register	PM9			√	√	—	
0FF2AH	Port 10 mode register	PM10			√	√	—	
0FF2EH	Real-time output port control register	RTPC			√	√	—	00H
0FF30H	Capture/compare control register 0	CRC0			—	√	—	10H
0FF31H	Timer output control register	TOC			√	√	—	00H
0FF32H	Capture/compare control register 1	CRC1			—	√	—	
0FF33H	Capture/compare control register 2	CRC2			—	√	—	10H

Note This is the case when the LOCATION 0H instruction is executed. When the LOCATION 0FH instruction is executed, “F0000H” is added to this value.

Table 7-1. Special Function Register (SFR) List (2/4)

Address[Note]	Special Function Register (SFR) Name	Abbreviation		R/W	Bit Units for Manipulation			After Reset
					1 bit	8 bits	16 bits	
0FF36H	Capture register (timer/counter 0)	CR02		R	—	—	√	0000H
0FF38H	Capture register L (timer/counter 1)	CR12	CR12W		—	√	√	
0FF39H	Capture register H (timer/counter 1)	—			—	—		
0FF3AH	Capture register L (timer/counter 2)	CR22	CR22W		—	√	√	
0FF3BH	Capture register H (timer/counter 2)	—			—	—		
0FF41H	Port 1 mode control register	PMC1		R/W	√	√	—	00H
0FF43H	Port 3 mode control register	PMC3			√	√	—	
0FF4AH	Port 10 mode control register	PMC10			√	√	—	
0FF4EH	Pull-up resistor option register L	PUOL			√	√	—	
0FF4FH	Pull-up resistor option register H	PUOH			√	√	—	
0FF50H	Timer register 0	TM0		R	—	—	√	0000H
0FF51H					—	—		
0FF52H	Timer register 1	TM1	TM1W		—	√	√	
0FF53H		—			—	—		
0FF54H	Timer register 2	TM2	TM2W		—	√	√	
0FF55H		—			—	—		
0FF56H	Timer register 3	TM3	TM3W		—	√	√	
0FF57H		—			—	—		
0FF5CH	Prescaler mode register 0	PRM0		R/W	—	√	—	11H
0FF5DH	Timer control register 0	TMC0			√	√	—	00H
0FF5EH	Prescaler mode register 1	PRM1			—	√	—	11H
0FF5FH	Timer control register 1	TMC1			√	√	—	00H
0FF68H	A/D converter mode register	ADM			√	√	—	00H
0FF6AH	A/D conversion result register	ADCR		R	—	√	—	Undefined
0FF6CH	A/D current cut select register	IEAD		R/W	√	√	—	00H
0FF6FH	Watch timer mode register	WM			√	√	—	
0FF70H	PWM control register	PWMC			√	√	—	05H
0FF71H	PWM prescaler register	PWPR			—	√	—	00H
0FF72H	PWM modulo register 0	PWM0			—	—	√	Undefined
0FF74H	PWM modulo register 1	PWM1			—	—	√	
0FF78H	ROM correction control register	CORC			√	√	—	00H
0FF79H	ROM correction address pointer H	CORAH			—	√	—	
0FF7AH	ROM correction address pointer L	CORAL			—	—	√	0000H
0FF7DH	One-shot pulse output control register	OSPC			√	√	—	00H
0FF80H	Clocked serial interface mode register 3	CSIM3			√	√	—	
0FF82H	Clocked serial interface mode register	CSIM			√	√	—	
0FF84H	Clocked serial interface mode register 1	CSIM1			√	√	—	
0FF85H	Clocked serial interface mode register 2	CSIM2			√	√	—	
0FF86H	Serial shift register	SIO			—	√	—	Undefined

Note This is the case when the LOCATION 0H instruction is executed. When the LOCATION 0FH instruction is executed, “F0000H” is added to this value.

Table 7-1. Special Function Register (SFR) List (3/4)

Address[Note 1]	Special Function Register (SFR) Name	Abbreviation	R/W	Bit Units for Manipulation			After Reset
				1 bit	8 bits	16 bits	
0FF88H	Asynchronous serial interface mode register	ASIM	R/W	√	√	—	00H
0FF89H	Asynchronous serial interface mode register 2	ASIM2		√	√	—	
0FF8AH	Asynchronous serial interface status register	ASIS	R	√	√	—	
0FF8BH	Asynchronous serial interface status register 2	ASIS2		√	√	—	
0FF8CH	Serial receive buffer: UART0	RXB		—	√	—	Undefined
	Serial transmit shift register: UART0	TXS	W	—	√	—	
	Serial shift register: IOE1	SIO1	R/W	—	√	—	
0FF8DH	Serial receive buffer: UART2	RXB2	R	—	√	—	
	Serial transmit shift register: UART2	TXS2	W	—	√	—	
	Serial shift register: IOE2	SIO2	R/W	—	√	—	
0FF8EH	Serial shift register 3: IOE3	SIO3		—	√	—	
0FF90H	Baud rate generator control register	BRGC		—	√	—	00H
0FF91H	Baud rate generator control register 2	BRGC2		—	√	—	
0FFA0H	External interrupt mode register 0	INTM0		√	√	—	
0FFA1H	External interrupt mode register 1	INTM1		√	√	—	
0FFA4H	Sampling clock select register	SCS0		—	√	—	
0FFA8H	In-service priority register	ISPR	R	√	√	—	
0FFAAH	Interrupt mode control register	IMC	R/W	√	√	—	80H
0FFACH	Interrupt mask register 0L	MK0L (MK0)		√	√	√	FFFFH
0FFADH	Interrupt mask register 0H	MK0H		√	√		
0FFAEH	Interrupt mask register 1L	MK1L (MK1)		√	√	√	
0FFAFH	Interrupt mask register 1H	MK1H		√	√		
0FFB0H	Bus control register	BCR		√	√	—	00H
0FFB2H	Unit address register	UAR		—	—	√	0000H
0FFB4H	Slave address register	SAR		—	—	√	
0FFB6H	Partner address register	PAR	R	—	—	√	
0FFB8H	Control data register	CDR	R/W	—	√	—	01H
0FFB9H	Message length register	DLR		—	√	—	
0FFBAH	Data register	DR		—	√	—	00H
0FFBBH	Unit status register	USR	R	√	√	—	
0FFBCH	Interrupt status register	ISR	R/W	√	√	—	
0FFBDH	Slave status register	SSR	R	√	√	—	41H
0FFBEH	Success count register	SCR		—	√	—	01H
0FFBFH	Communication count register	CCR		—	√	—	20H
0FFC0H	Standby control register	STBC	R/W	—	√ Note 2	—	30H
0FFC2H	Watchdog timer mode register	WDM		—	√ Note 2	—	00H

Notes 1. This is the case when the LOCATION 0H instruction is executed. When the LOCATION 0FH instruction is executed, “F0000H” is added to this value.

2. Data can be written to these registers only by using dedicated instructions MOV STBC, #byte and MOV MDM, #byte. Other instructions cannot be used.

Table 7-1. Special Function Register (SFR) List (4/4)

Address[Note 1]	Special Function Register (SFR) Name	Abbreviation	R/W	Bit Units for Manipulation			After Reset
				1 bit	8 bits	16 bits	
0FFC4H	Memory expansion mode register	MM	R/W	√	√	—	20H
0FFC5H	Hold mode register	HLDM		√	√	—	00H
0FFC6H	Clock output mode register	CLOM		√	√	—	
0FFC7H	Programmable wait control register 1	PWC1		—	√	—	AAH
0FFC8H	Programmable wait control register 2	PWC2		—	—	√	AAAAH
0FFCCH	Refresh mode register	RFM		√	√	—	00H
0FFCDH	Refresh area specification register	RFA		√	√	—	
0FFCFH	Oscillation stabilization time specification register	OSTS		—	√	—	
0FFD0H-0FFDFH	External SFR area	—		√	√	—	—
0FFE0H	Interrupt control register (INTP0)	PIC0		√	√	—	43H
0FFE1H	Interrupt control register (INTP1)	PIC1		√	√	—	
0FFE2H	Interrupt control register (INTP2)	PIC2		√	√	—	
0FFE3H	Interrupt control register (INTT3)	PIC3		√	√	—	
0FFE4H	Interrupt control register (INTC00)	CIC00		√	√	—	
0FFE5H	Interrupt control register (INTC01)	CIC01		√	√	—	
0FFE6H	Interrupt control register (INTC10)	CIC10		√	√	—	
0FFE7H	Interrupt control register (INTC11)	CIC11		√	√	—	
0FFE8H	Interrupt control register (INTC20)	CIC20		√	√	—	
0FFE9H	Interrupt control register (INTC21)	CIC21		√	√	—	
0FFEAH	Interrupt control register (INTC30)	CIC30		√	√	—	
0FFEBH	Interrupt control register (INTP4)	PIC4		√	√	—	
0FFECH	Interrupt control register (INTP5)	PIC5		√	√	—	
0FFEDH	Interrupt control register (INTAD)	ADIC		√	√	—	
0FFEEH	Interrupt control register (INTSER)	SERIC		√	√	—	
0FFEFH	Interrupt control register (INTSR)	SRIC		√	√	—	
	Interrupt control register (INTCSI1)	CSIIC1		√	√	—	
0FFF0H	Interrupt control register (INTST)	STIC		√	√	—	
0FFF1H	Interrupt control register (INTCSI)	CSIIC		√	√	—	
0FFF2H	Interrupt control register (INTSER2)	SERIC2		√	√	—	
0FFF3H	Interrupt control register (INTSR2)	SRIC2		√	√	—	
	Interrupt control register (INTCSI2)	CSIIC2		√	√	—	
0FFF4H	Interrupt control register (INTST2)	STIC2		√	√	—	
0FFF6H	Interrupt control register (INTIE1)	IEIC1		√	√	—	
0FFF7H	Interrupt control register (INTIE2)	IEIC2		√	√	—	
0FFF8H	Interrupt control register (INTW)	WIC		√	√	—	
0FFF9H	Interrupt control register (INTCSI3)	CSIIC3		√	√	—	
0FFFCH	Internal memory size switching register[Note 2]	IMS		—	√	—	FFH

Notes 1. This is the case when the LOCATION 0H instruction is executed. When the LOCATION 0FH instruction is executed, “F0000H” is added to this value.

2. Writing this register is meaningful only with the μPD78F4938A.

8. PERIPHERAL HARDWARE FUNCTIONS

8.1 Ports

The ports shown in Figure 8-1 are provided for various control operations. The function of each port is as shown in Table 8-1. On-chip pull-up resistors can be specified for ports 0 to 6, 9, and 10 by means of software.

Figure 8-1. Port Configuration

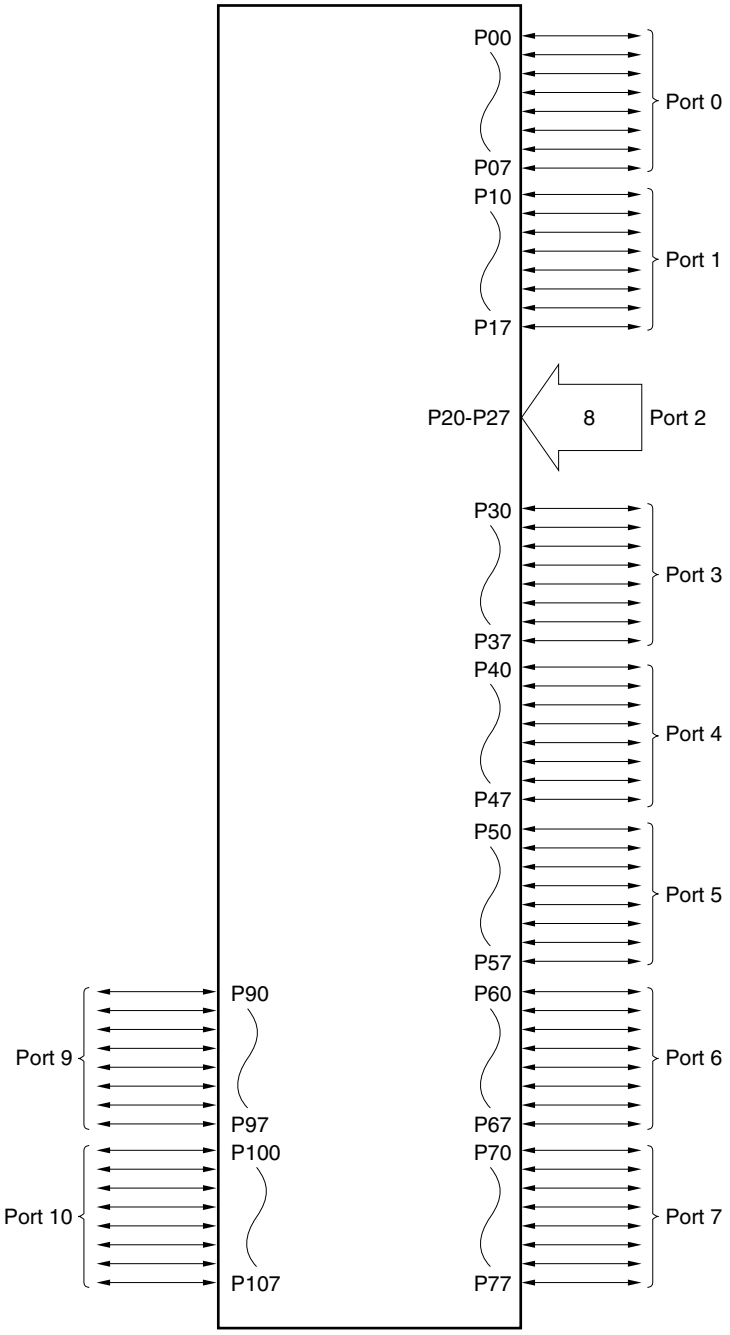


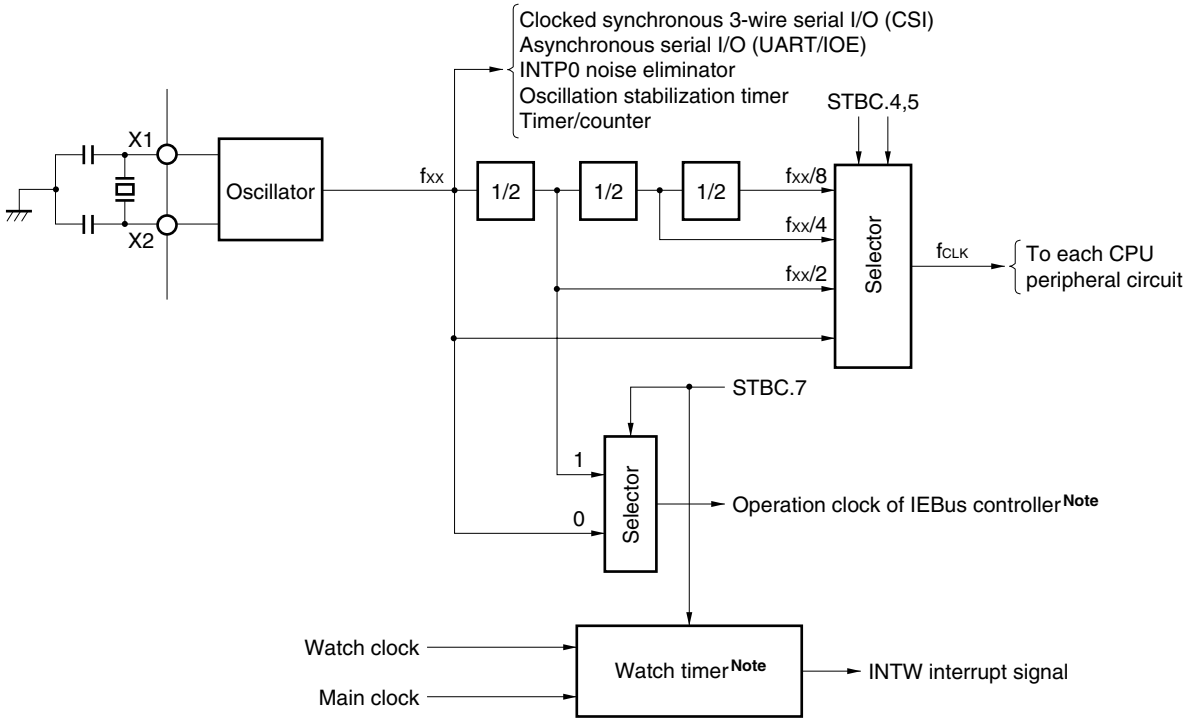
Table 8-1. Port Functions

Port Name	Pin Name	Function	Software Specification of Pull-up Resistor
Port 0	P00 to P07	• Input/output can be specified in 1-bit units. • Can also operate as a 4-bit real-time output port (P00 to P03, P04 to P07). • Can drive a transistor.	Pull-up resistors can be specified for the pins in input mode all at once.
Port 1	P10 to P17	• Input/output can be specified in 1-bit units. • Can drive an LED.	Pull-up resistors can be specified for the pins in input mode all at once.
Port 2	P20 to P27	• Input port	Pull-up resistors can be specified in 6-bit units (P22 to P27).
Port 3	P30 to P37	• Input/output can be specified in 1-bit units. • P32/$\overline{\text{SCK0}}$ and P33/SO0 pins can be used as N-ch open-drain pins.	Pull-up resistors can be specified for the pins in input mode all at once.
Port 4	P40 to P47	• Input/output can be specified in 1-bit units. • Can drive an LED.	Pull-up resistors can be specified for the pins in input mode all at once.
Port 5	P50 to P57	• Input/output can be specified in 1-bit units. • Can drive an LED.	Pull-up resistors can be specified for the pins in input mode all at once.
Port 6	P60 to P67	• Input/output can be specified in 1-bit units.	Pull-up resistors can be specified for the pins in input mode all at once.
Port 7	P70 to P77	• Input/output can be specified in 1-bit units.	—
Port 9	P90 to P97	• Input/output can be specified in 1-bit units.	Pull-up resistors can be specified for the pins in input mode all at once.
Port 10	P100 to P107	• Input/output can be specified in 1-bit units. • P105/$\overline{\text{SCK3}}$ pin and P107/SO3 pin can be used as N-ch open-drain pins.	Pull-up resistors can be specified for the pins in input mode all at once.

8.2 Clock Generator

This circuit generates a clock necessary for operation. It is also provided with a frequency divider. When high-speed operation is not necessary, the power consumption can be lowered by reducing the internal operating frequency.

Figure 8-2. Block Diagram of Clock Generator

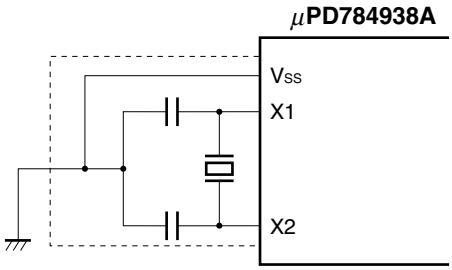


Note Be sure to set bit 7 of the standby control register (STBC) to 1 when using the main clock.

Remark f_{XX}: Oscillation frequency
f_{CLK}: Internal operating frequency

Figure 8-3. Example of Using Oscillator

Crystal/ceramic oscillation



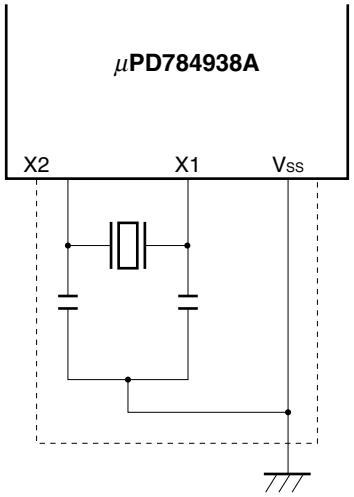
Caution When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as VSS.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

The subsystem oscillator has a low amplification factor so as to lower the current consumption and is more susceptible to noise than the main system clock oscillator. When using the subsystem clock circuit, therefore, utmost care must be exercised in wiring the circuit.

If the oscillator does not operate correctly, the microcontroller cannot operate correctly, either. Consult the oscillator manufacturer if you need an oscillation frequency at high accuracy.

Figure 8-4. Notes on Connecting Resonator



Cautions 1. Keep the oscillator as close to the X1 and X2 (XT1 and XT2) pins as possible.

2. Do not pass any other signal lines through the region indicated by the dotted line.

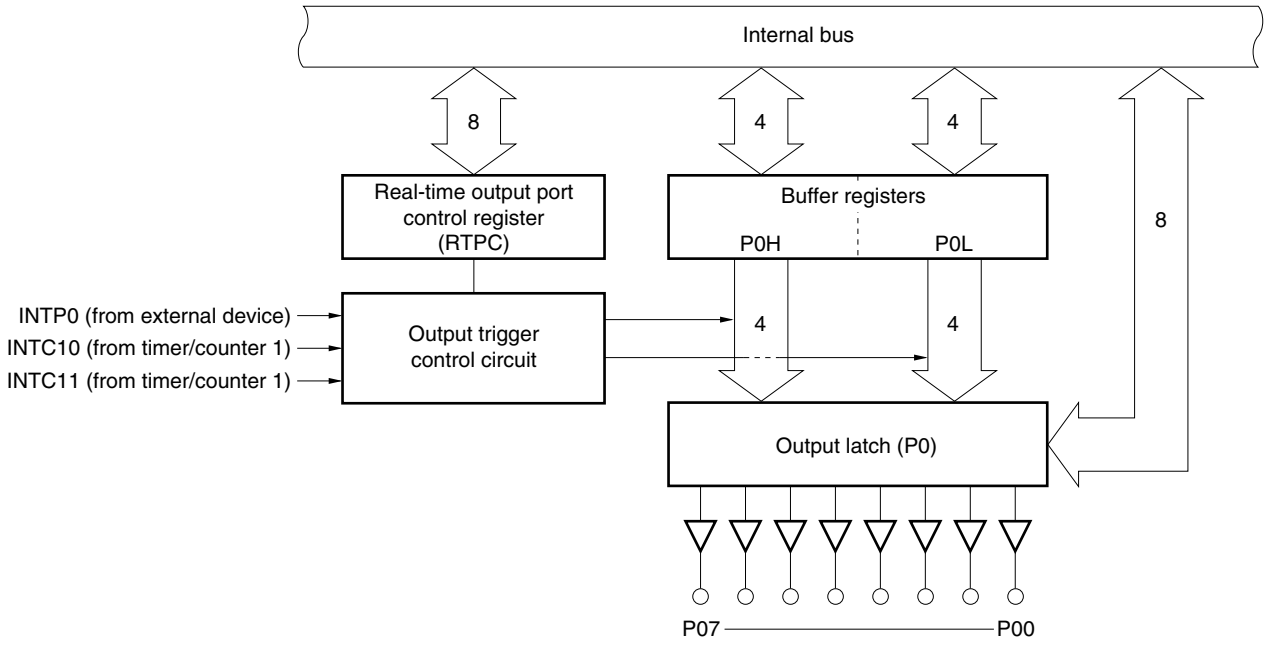
8.3 Real-Time Output Port

The real-time output port outputs the data stored in the buffer in synchronization with the match interrupt of timer/counter 1 or an external interrupt. As a result, it can output pulses without jitter.

Therefore, this port is ideal for applications where different patterns are output at different intervals (such as open loop control of a stepper motor).

The real-time output port consists mainly of port 0 and the port 0 buffer registers (P0H and P0L) as shown in Figure 8-5.

Figure 8-5. Block Diagram of Real-Time Output Port



8.4 Timers/Counters

Three timer/event counters and one timer are provided.

In addition, because seven interrupt requests are supported, the timer/counters and timer can be used as seven timer/counters.

Table 8-2. Operations of Timers/Counters

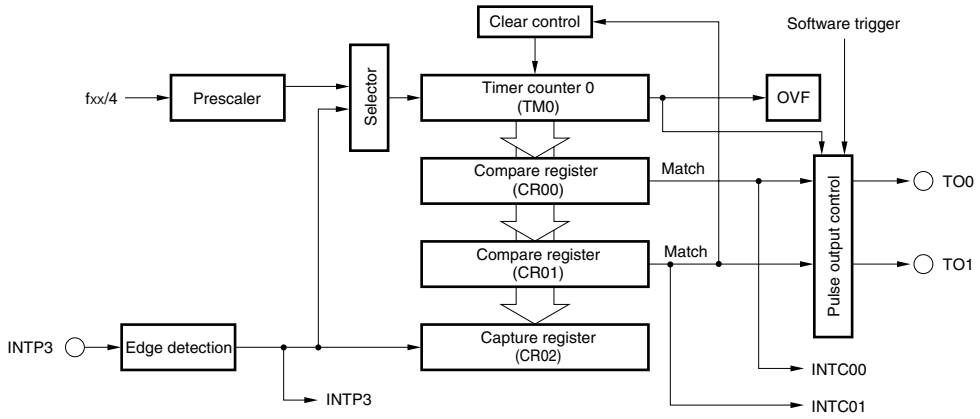
Item \ Name		Timer/Event Counter 0	Timer/Event Counter 1	Timer/Event Counter 2	Timer 3
Count width	8 bits	—	√	√	√
	16 bits	√	√	√	√
Operation mode	Interval timer	2ch	2ch	2ch	1ch
	External event counter	√	√	√	—
	One-shot timer	—	—	√	—
Function	Timer output	2ch	—	2ch	—
	Toggle output	√	—	√	—
	PWM/PPG output	√	—	√	—
	One-shot pulse output[Note]	√	—	—	—
	Real-time output	—	√	—	—
	Pulse width measurement	1 input	1 input	2 inputs	—
	Number of interrupt requests	2	2	2	1

Note The one-shot pulse output function is used to make a pulse output level active by software and inactive by hardware (interrupt request signal).

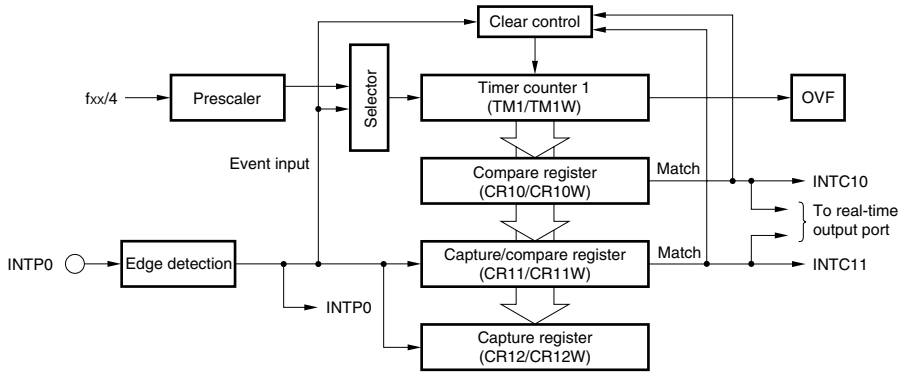
This function is different from the one-shot timer function of timer/event counter 2 in nature.

Figure 8-6. Block Diagram of Timers/Counters

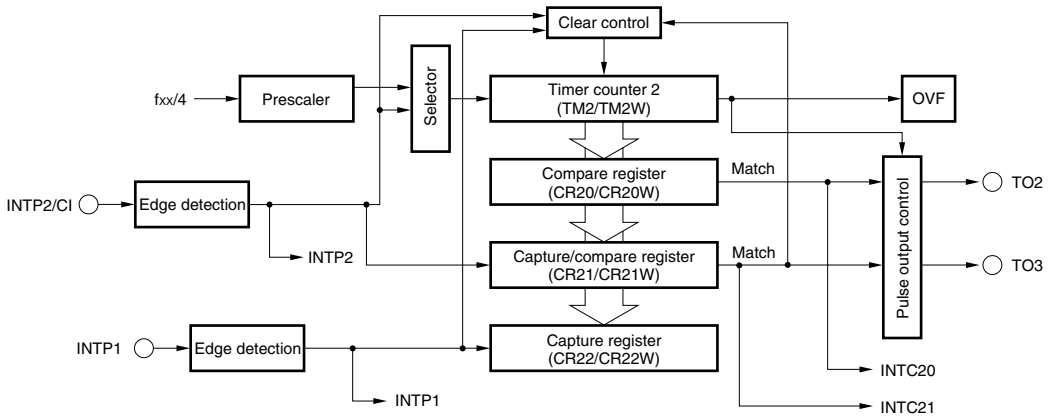
Timer/event counter 0



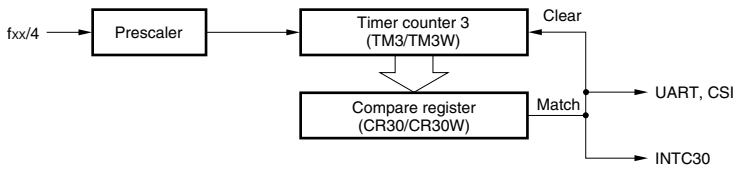
Timer/event counter 1



Timer/event counter 2



Timer 3



Remark OVF: Overflow flag

8.5 Watch Timer

The count clock to be input to the watch timer can be selected from the main clock (12.58 MHz) or watch clock (32.768 kHz) by using a control register. The watch clock is input only to the watch timer and not to the CPU or other peripheral circuits. Therefore, the operation speed of the CPU cannot be slowed down by the watch clock.

The watch timer generates an interrupt signal (INTW) at intervals of 0.5 seconds[Note] by dividing the count clock. At the same time, it also sets an interrupt request flag (WIF) (bit 7 of the interrupt control register (WIC)).

The interval of generating INTW can be changed to about 1 ms by changing the mode (fast forward mode: 512 times faster than the normal mode).

When the main clock is selected as the count clock, the watch timer stops its operation in the STOP mode and IDLE mode. In the HALT mode, however, it continues operating. When the watch clock is selected as the count clock, the watch timer can continue operating in any of the STOP, IDLE, and HALT modes. The operation of the watch clock oscillator is controlled by the watch timer mode register (WM).

The watch timer of the μPD784938A does not have a buzzer output function.

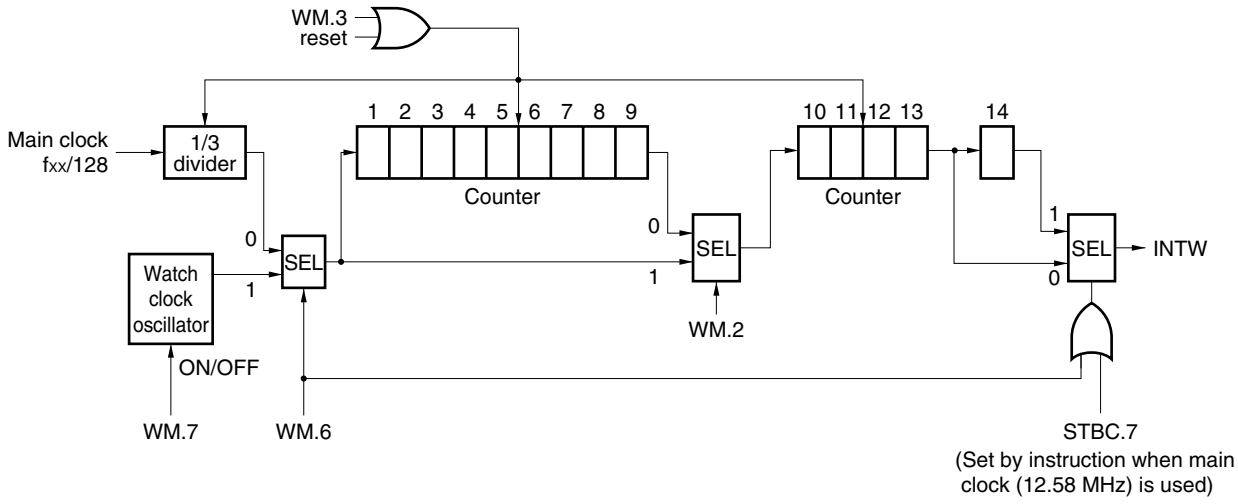
Note This doesn't mean the first INTW occurs within 0.5 seconds after the operation has been enabled.

Table 8-3. Relation Between Count Clock and Watch Timer Operation

Selection of Count Clock	Normal Operation Mode	Types of Standby Modes		
		HALT mode	STOP mode	IDLE mode
Main clock	Can operate	Can operate	Stops	Stops
Watch clock	Can operate	Can operate	Can operate	Can operate

The watch timer consists of a frequency divider that divides the count clock by three and a counter that divides the output of the frequency divider by 2^{14}. As the count clock, select a signal resulting from dividing the internal system clock by 128 or the signal from the watch clock oscillator.

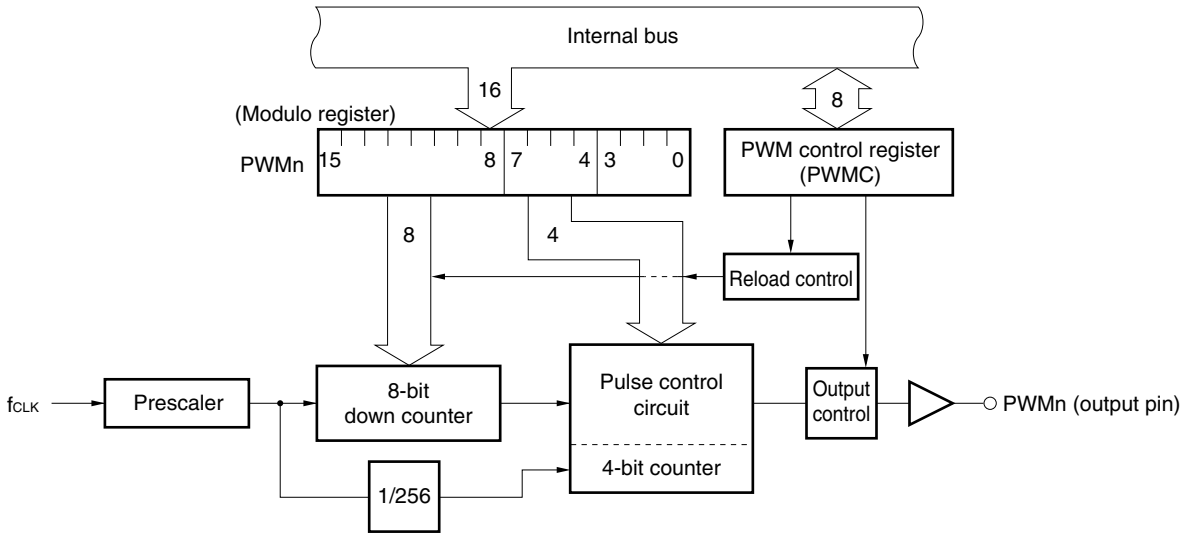
Figure 8-7. Block Diagram of Watch Timer



8.6 PWM Output (PWM0, PWM11)

Two PWM (pulse width modulation) output circuits with a resolution of 12 bits are provided. The active level of each PWM output channel can be selected independently of the other channel. The PWM output is ideal for controlling the speed of a DC motor.

Figure 8-8. Block Diagram of PWM Output Unit



Remark n = 0 or 1

8.7 A/D Converter

An analog-to-digital (A/D) converter having 8 multiplexed analog input lines (ANI0 to ANI7) is provided.

This A/D converter is of the successive approximation type, and the result of conversion is stored in an 8-bit A/D conversion result register (ADCR). Therefore, conversion can be carried out with a high accuracy.

The A/D conversion operation can be started in the following two modes:

- Hardware start: Conversion is started by trigger input (INTP5).
- Software start: Conversion is started by setting a bit of the A/D converter mode register (ADM).

After the conversion has been started, the following two operation modes can be selected.

- Scan mode: Two or more analog input pins are sequentially selected to convert multiple signals.
- Select mode: Only one analog input pin is used to successively convert one signal.

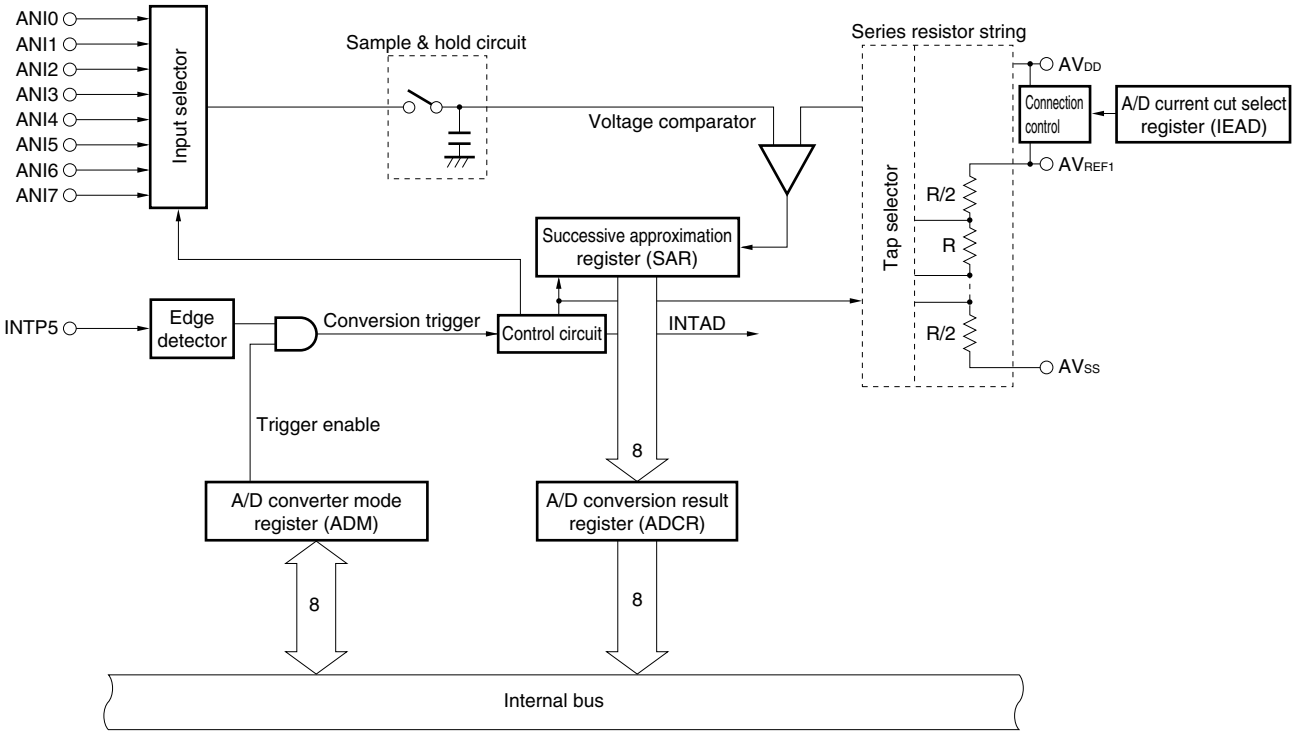
These operations modes are selected and conversion is stopped by ADM.

When the result of conversion is transferred to ADCR, the interrupt request INTAD is generated. By using this interrupt and a macro service, the converted values can be successively transferred to memory.

Cautions 1. Apply the same voltage as the supply voltage (AV_{DD}) to the reference voltage input pin (AV_{REF1}) of this product.

2. When port 7 is used both as an output port and A/D input lines, do not manipulate the output port while A/D conversion is in progress.

Figure 8-9. Block Diagram of A/D Converter



8.8 Serial Interface

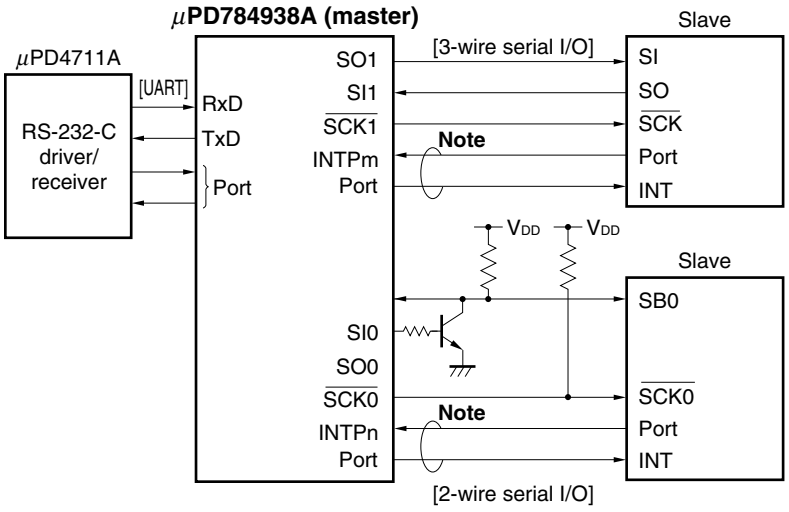
Four independent serial interface channels are provided.

- Asynchronous serial interface (UART)/3-wire serial I/O (IOE) × 2
- Clocked serial interface (CSI) × 2
  - 3-wire serial I/O (IOE)

Therefore, communication with an external device and internal, local communication within the system can be performed simultaneously (refer to **Figure 8-10**).

Figure 8-10. Example of Serial Interface

UART + 3-wire serial I/O + 2-wire serial I/O



Note Handshake line

8.8.1 Asynchronous serial interface/3-wire serial I/O (UART/IOE)

Two serial interface channels that can select an asynchronous serial interface mode and 3-wire serial I/O mode are available.

(1) Asynchronous serial interface mode

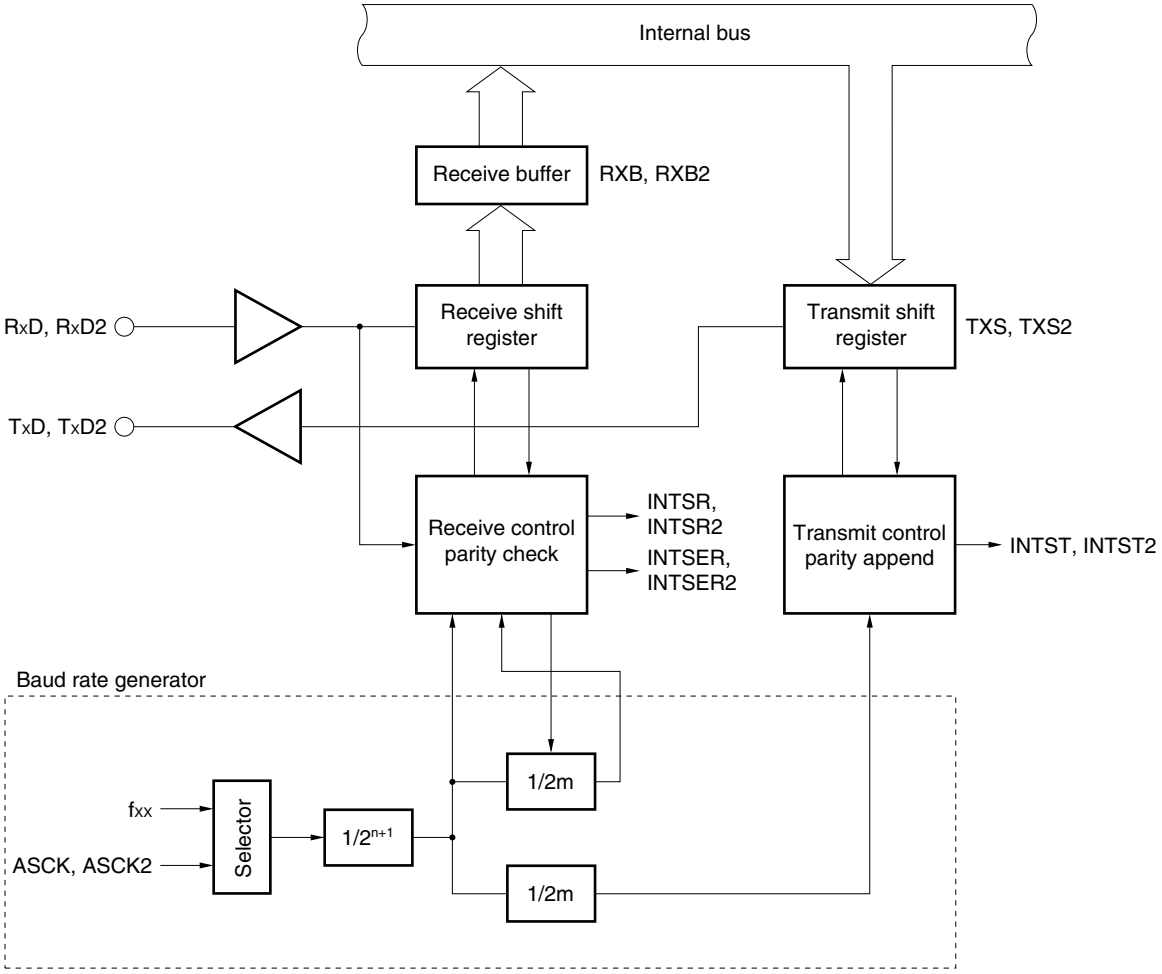
In this mode, 1-byte data is transmitted or received after a start bit.

Because an internal baud rate generator is available, communication can be performed at a wide range of baud rates.

In addition, the baud rate can be defined by dividing the clock input to the ASCK pin.

When the baud generator is used, a MIDI Standard baud rate (31.25 kbps) can be also obtained.

Figure 8-11. Block Diagram in Asynchronous Serial Interface Mode



Remark fxx: Oscillation frequency
n = 0 to 11
m = 16 to 30

(2) 3-wire serial I/O mode

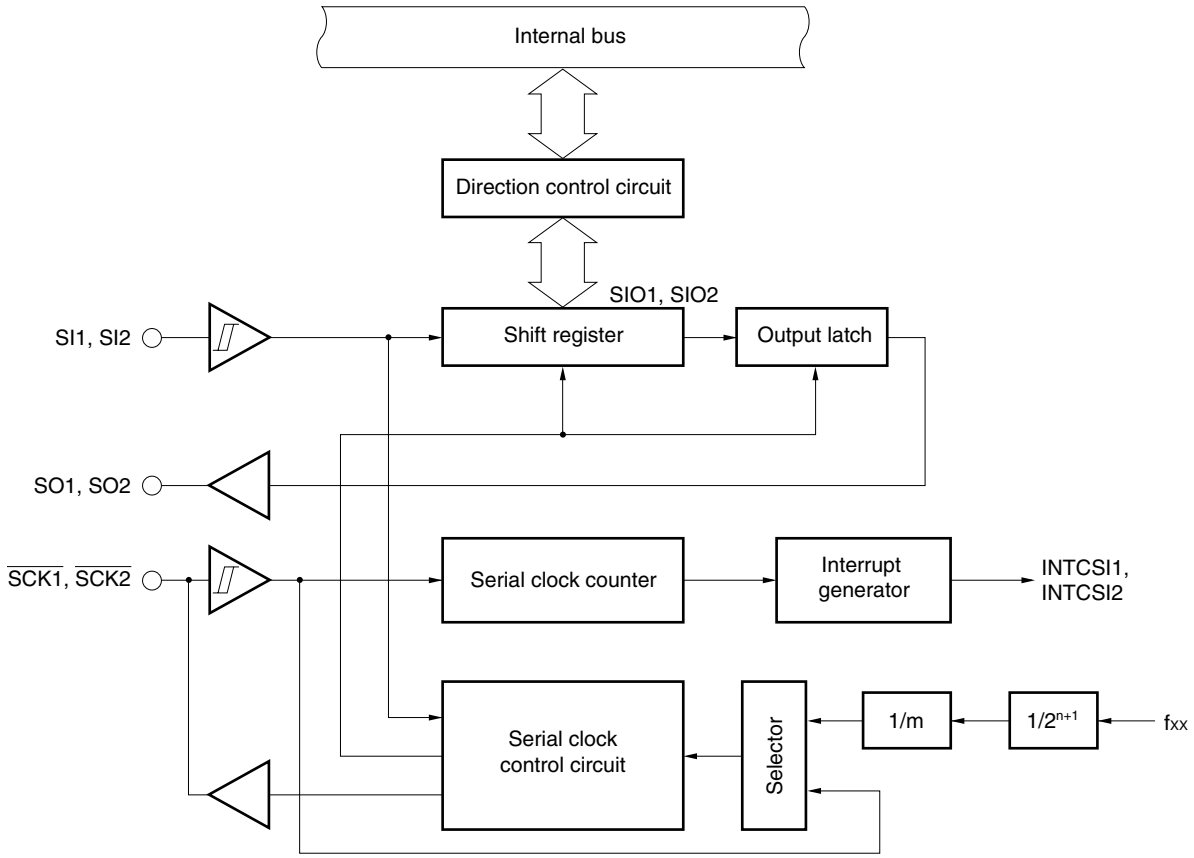
In this mode, the master device makes the serial clock active and starts transmission. One byte of data is communicated in synchronization with this clock.

This interface mode is to communicate with a device with a conventional clocked serial interface.

Basically, communication is established by using three lines: serial clock ($\overline{SCK}$) and serial data (SI and SO).

Generally, a handshake line is necessary for checking the communication status.

Figure 8-12. Block Diagram in 3-Wire Serial I/O Mode

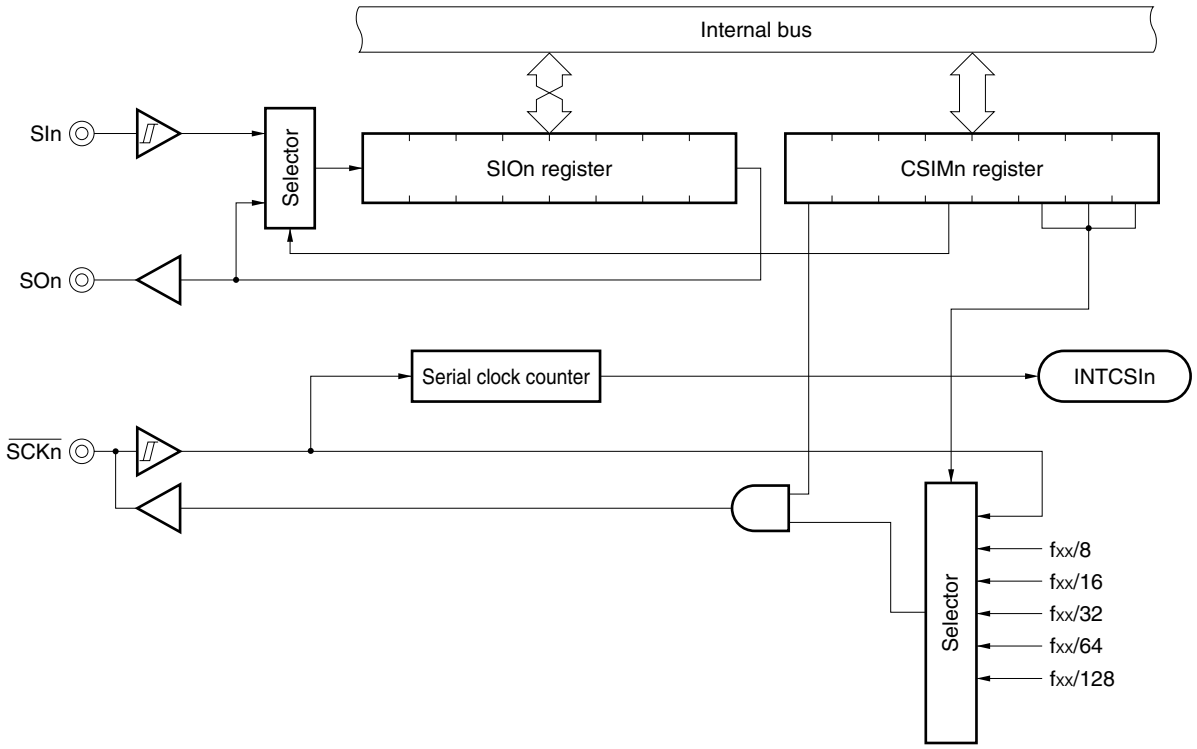


Remark fxx: Oscillation frequency
n = 0 to 11
m = 1, or 16 to 30

8.8.2 Clocked serial interface (CSI)

In this mode, the master device makes the serial clock active and starts transmission. One byte of data is communicated in synchronization with this clock.

Figure 8-13. Block Diagram of Clocked Serial Interface



Remark fxx: Oscillation frequency
n = 0 or 3

- **3-wire serial I/O mode**

  This mode is used to communicate with a device having a conventional clocked serial interface.

  Basically, communication is performed by using three lines: serial clock ($\overline{SCKn}$) and serial data (SIn and SOn) (n = 0 or 3).

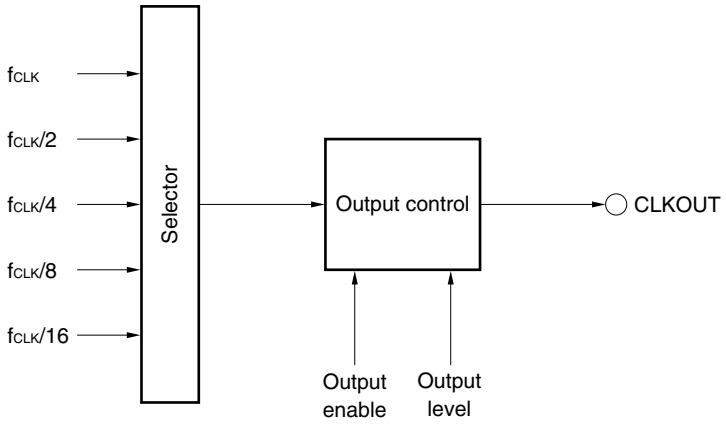
  Generally, a handshake line is necessary for checking the communication status.

8.9 Clock Output Function

The operating clock of the CPU can be divided and output to an external device. The line that outputs the divided clock can be also used as a 1-bit port.

When this function is used, the local bus interface cannot be used, because the ASTB and CLKOUT pins are multiplexed.

Figure 8-14. Block Diagram of Clock Output Function



8.10 Edge Detection Function

The interrupt input pins (NMI and INTP0 to INTP5) are used to input trigger signals for the on-chip hardware units, as well as to input interrupt requests. Because these pins operate at the edge of an input signal, they are provided with a function to detect edges. In addition, these pins also have a noise eliminator function to prevent erroneous detection of an edge due to noise.

Table 8-4. Noise Elimination of Interrupt Input Pins

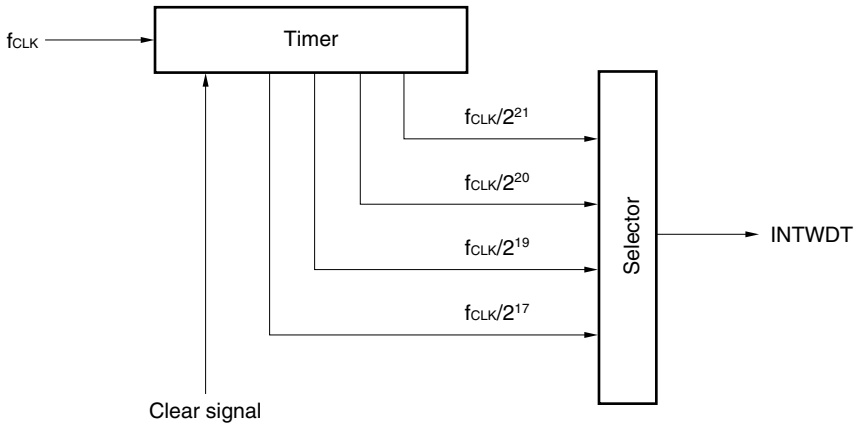
Pin Name	Detectable Edge	Noise Rejection
NMI	Either rising or falling edge	By analog delay
INTP0 to INTP3	Either or both rising or falling edge	By clock sampling[Note]
INTP4, INTP5		By analog delay

Note INTP0 can select a sampling clock.

8.11 Watchdog Timer

A watchdog timer is provided to detect inadvertent program loop of the CPU. This watchdog timer generates a non-maskable interrupt request unless it is cleared by software within specified interval time. Once the watchdog timer has been enabled to operate, it cannot be stopped by software. It can be specified whether the interrupt request from the watchdog timer or the interrupt request from the NMI pin takes precedence.

Figure 8-15. Block Diagram of Watchdog Timer



8.12 Simplified IEBus Controller

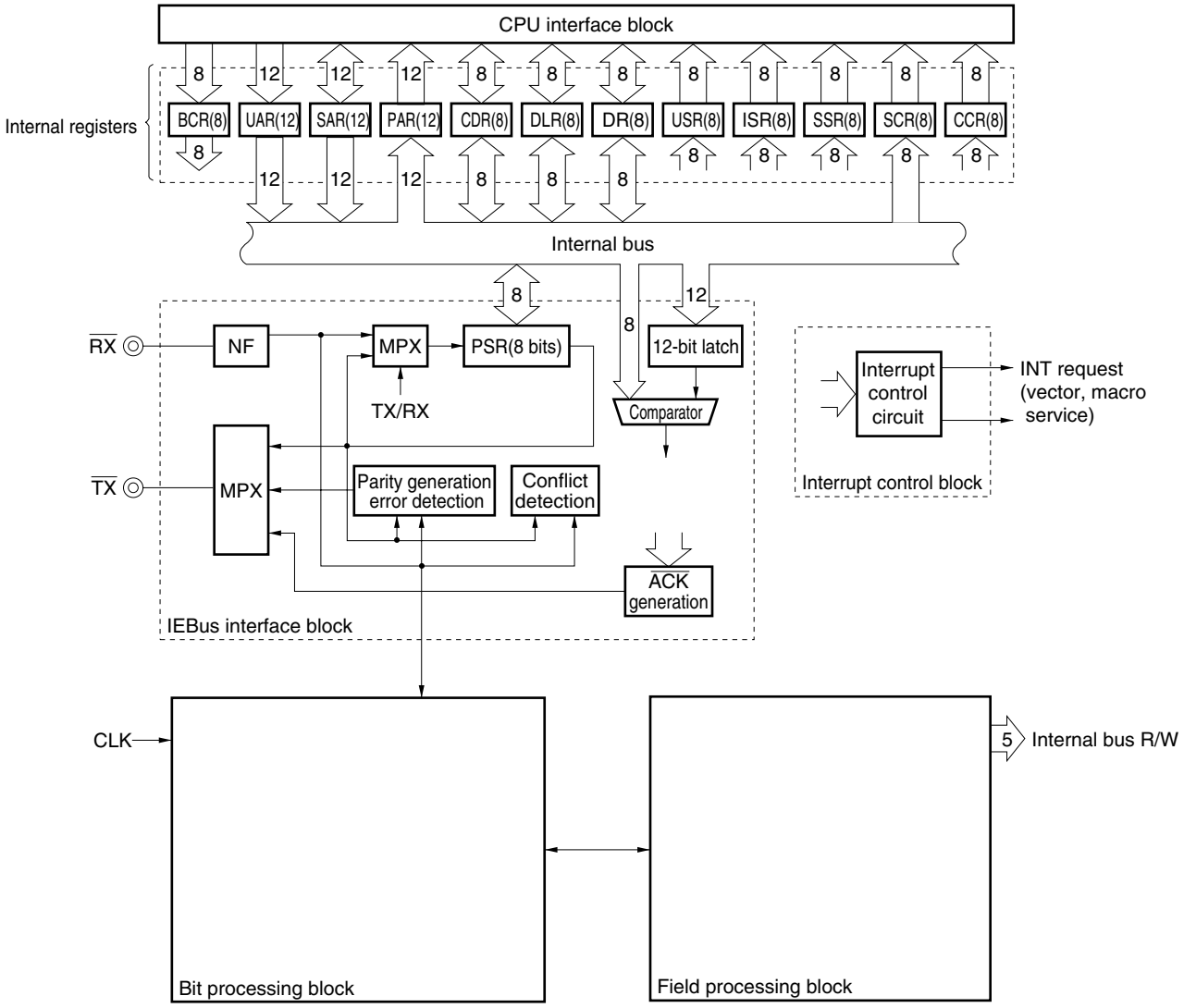
The μPD784938A has a newly developed IEBus controller. The functions of this controller are limited compared with the IEBus interface function (provided to the 78K/0 Series) of conventional microcontrollers.

Table 8-5 compares the simplified IEBus interface of the μPD784938A and the conventional IEBus interface.

Table 8-5. Comparison Between Conventional IEBus Interface and Simplified IEBus Interface

Item	Conventional Model (IEBus of 78K/0)	Simplified IEBus
Communication mode	Mode 0, mode 1, mode 2	Fixed to mode 1
Internal system clock	6.0 (6.29) MHz	
Internal buffer size	Transmit buffer: 33 bytes (FIFO) Receive buffer: 40 bytes (FIFO) Up to 4 frames can be received.	Transmit/receive register: 1 byte
CPU processing	Preprocessing before start of communication (data setting) Setting and managing each communication status Data write to transmit buffer Data read from receive buffer	Preprocessing before start of communication (data setting) Setting and managing each communication status 1-byte data write processing 1-byte data read processing Management of transmission such as slave status Multiple frame management, re-master request processing
Hardware processing	Bit processing (modulation/demodulation, error detection) Field processing (generation/management) Arbitration result detection Parity processing (generation/error detection) Automatic returning of $\overline{\text{ACK}}$/NACK Automatic data re-transmission processing Automatic re-master processing Automatic transmission processing such as slave status Multiple frame reception processing	Bit processing (modulation/demodulation, error detection) Field processing (generation/management) Arbitration result detection Parity processing (generation/error detection) Automatic returning of $\overline{\text{ACK}}$/NACK Automatic data re-transmission processing

Figure 8-16. Block Diagram of IEBus Controller



- **Hardware configuration and function**

  The IEBus internally consists of the following six blocks:

  - CPU interface block
  - Interrupt control block
  - Internal registers
  - Bit processing block
  - Field processing block
  - IEBus interface block

  <CPU interface block>

  This control block interfaces the CPU (78K/IV) with the IEBus.

  <Interrupt control block>

  This block passes interrupt request signals from the IEBus to the CPU.

  <Internal registers>

  These registers specify the data in each field of the control register that controls the IEBus.

  <Bit processing block>

  This block generates and disassembles bit timing, and mainly consists of a bit sequence ROM, 8-bit preset timer, and decision unit.

  <Field processing block>

  This block generates each field in a communication frame, and mainly consists of a field sequence ROM, 4-bit down counter, and decision unit.

  <IEBus interface block>

  This block is used to interface with an external driver/receiver, and mainly consists of a noise filter, shift register, conflict detection unit, parity detection unit, parity generator, and $\overline{\text{ACK}}$/NACK generator.

9. INTERRUPT FUNCTION

To service an interrupt, the three servicing formats shown in Table 9-1 can be selected in software.

Table 9-1. Interrupt Request Servicing

Servicing Mode	Main Body of Servicing Routine	Servicing	Contents of PC and PSW
Vectored interrupt	Software	Branches to and executes servicing routine (any servicing).	Saves to and restores from stack.
Context switching		Automatically selects register bank, and branches to and executes servicing routine (any servicing).	Saves to or restores from fixed area in register bank.
Macro service	Firmware	Executes data transfer between memory and I/O (servicing is fixed).	Held

9.1 Interrupt Sources

The sources of interrupts include the 27 sources listed in Table 9-2, execution of the BRK or BRKCS instruction, and operand errors.

Four interrupt priority levels can be selected, so that nesting of interrupts can be controlled and that two or more interrupt requests that are simultaneously generated can be controlled. When a macro service is used, however, nesting always progresses (is not kept pending).

The default priority determines the priorities of the servicing of two or more interrupt requests that are generated at the same time (fixed priorities) (refer to **Table 9-2**).

Table 9-2. Interrupt Sources

Type	Default Priority	Source		Internal/ External	Macro Service
		Name	Trigger		
Software	—	BRK instruction	Execution of instruction	—	—
		BRKCS instruction	Execution of instruction		
		Operand error	If result of exclusive-OR of operands byte and $\overline{\text{byte}}$ is not FFH when MOV STBC, #byte, MOV WDM, #byte, or LOCATION instruction is executed		
Non-maskable	—	NMI	Detection of pin input edge	External	—
		WDT	Overflow of watchdog timer	Internal	
Maskable	0 (highest)	INTP0	Detection of pin input edge (TM1/TM1W capture trigger)	External	√
	1	INTP1	Detection of pin input edge (TM2/TM2W capture trigger)		
	2	INTP2	Detection of pin input edge (TM2/TM2W event counter input)		
	3	INTP3	Detection of pin input edge (TM0 capture trigger)		
	4	INTC00	Generation of TM0 to CR00 matching signal	Internal	√
	5	INTC01	Generation of TM0 to CR01 matching signal		
	6	INTC10	Generation of TM1 to CR10 matching signal (in 8-bit operation mode) Generation of TM1W to CR10W matching signal (in 16-bit operation mode)		
	7	INTC11	Generation of TM1 to CR11 matching signal (in 8-bit operation mode) Generation of TM1W to CR11W matching signal (in 16-bit operation mode)		
	8	INTC20	Generation of TM2 to CR20 matching signal (in 8-bit operation mode) Generation of TM2W to CR20W matching signal (in 16-bit operation mode)		
	9	INTC21	Generation of TM2 to CR21 matching signal (in 8-bit operation mode) Generation of TM2W to CR21W matching signal (in 16-bit operation mode)		
	10	INTC30	Generation of TM3 to CR30 matching signal (in 8-bit operation mode) Generation of TM3W to CR30W matching signal (in 16-bit operation mode)		
	11	INTP4	Detection of pin input edge	External	√
	12	INTP5	Detection of pin input edge		
	13	INTAD	End of A/D conversion (transfer of ADCR)	Internal	√
	14	INTSER	Occurrence of ASI0 reception error		—
	15	INTSR	End of ASI0 reception or end of CSI1 transfer		√
		INTCSI1			
	16	INTST	End of ASI0 transmission		
	17	INTCSI	End of CSI0 transfer		
	18	INTSER2	Occurrence of ASI2 reception error		—
	19	INTSR2	End of ASI2 reception or end of CSI2 transfer		√
		INTCSI2			
	20	INTST2	End of ASI2 transmission		
	21	INTIE1	IEBus data access request		
	22	INTIE2	Occurrence of IEBus communication error and start/end of communication		
	23	INTW	Watch timer output		
	24 (lowest)	INTCSI3	End of CSI3 transfer		

Remark ASI : Asynchronous serial interface
CSI : Clocked serial interface

9.2 Vectored Interrupt

If an interrupt occurs, execution branches to the interrupt routine, using the contents of the vector table address corresponding to the interrupt source as the branch destination address.

The following operations are performed so that the CPU executes interrupt servicing.

- When execution branches: Saves the status of the CPU (contents of PC and PSW) to stack
- When execution returns: Restores the status of the CPU (contents of PC and PSW) from stack

To return execution from an interrupt routine to the main routine, the RETI instruction is used.

The branch destination address must be in the range 0 to FFFFH.

Table 9-3. Vector Table Address

Interrupt Source	Vector Table Address
BRK instruction	003EH
Operand error	003CH
NMI	0002H
WDT	0004H
INTP0	0006H
INTP1	0008H
INTP2	000AH
INTP3	000CH
INTC00	000EH
INTC01	0010H
INTC10	0012H
INTC11	0014H
INTC20	0016H
INTC21	0018H
INTC30	001AH
INTP4	001CH
INTP5	001EH
INTAD	0020H
INTSER	0022H
INTSR	0024H
INTCSI1	
INTST	0026H
INTCSI	0028H
INTSER2	002AH
INTSR2	002CH
INTCSI2	
INTST2	002EH

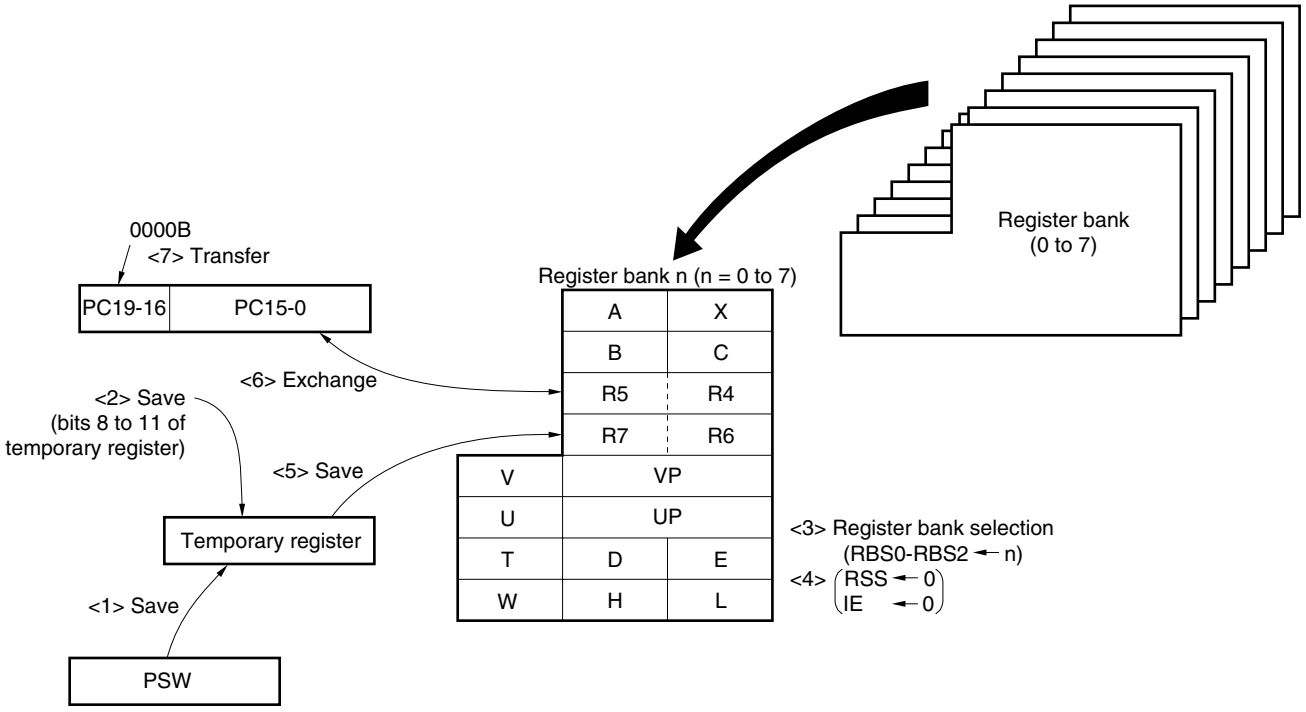
Interrupt Source	Vector Table Address
INTIE1	0032H
INTIE2	0034H
INTW	0036H
INTCSI3	0038H

9.3 Context Switching

Context switching is a function used to select a specific register bank by hardware when an interrupt request is generated or when the BRKCS instruction is executed. Program execution then branches to the vector address stored in advance in the register bank and, at the same time, the current contents of the program counter (PC) and program status word (PSW) are temporarily stored in the register bank.

The branch destination address is in the range 0 to FFFFH.

Figure 9-1. Context Switching Operation When an Interrupt Request Is Generated

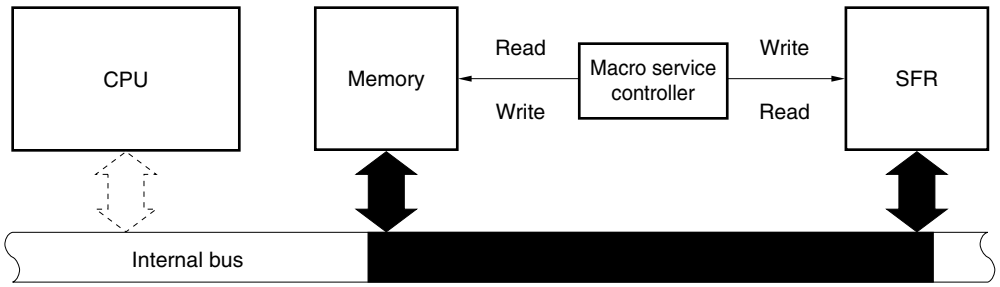


9.4 Macro Service

A macro service is a function used to transfer data between memory and a special function register (SFR) without the intervention of the CPU. A macro service controller accesses memory and SFR in the same transfer cycle, and directly transfers data without loading it.

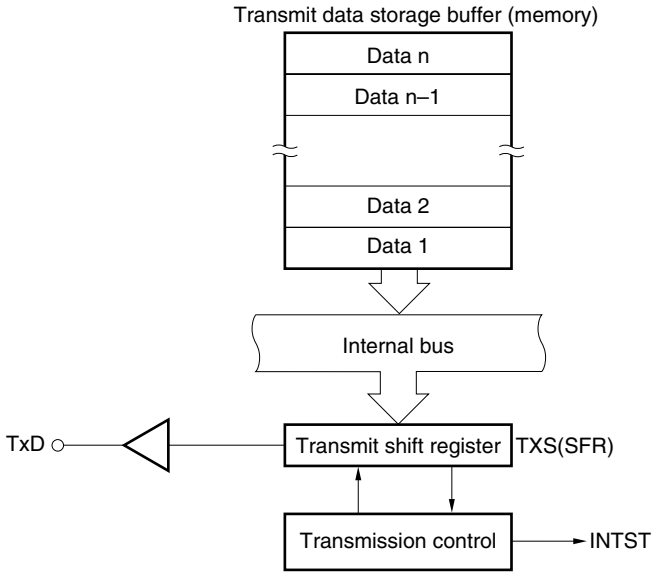
Because it is not necessary to save or restore the status of the CPU or to load data, data can be transferred at high speed using this function.

Figure 9-2. Macro Service



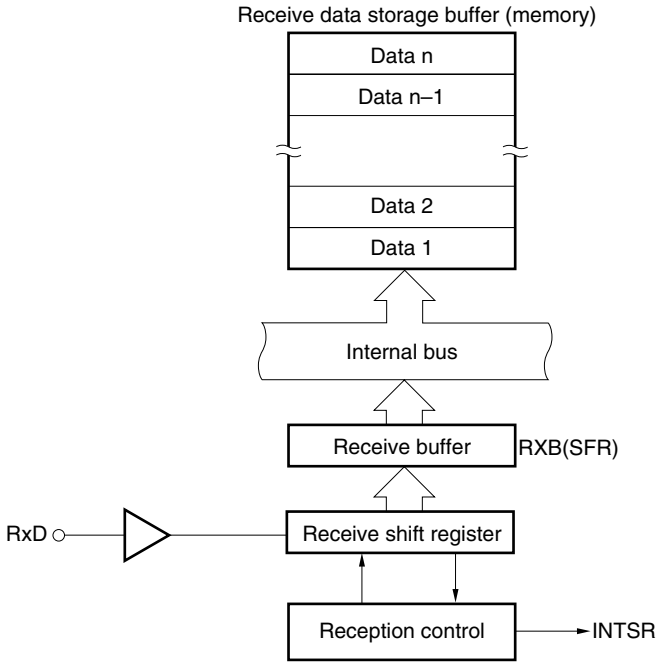
9.5 Application Examples of Macro Service

(1) Transmit operation of serial interface



Each time a macro service request (INTST) is generated, the next transmit data is transferred from memory to TXS. When data n (last byte) is transferred to TXS (when the transmit data storage buffer becomes empty), a vectored interrupt request (INTST) is generated.

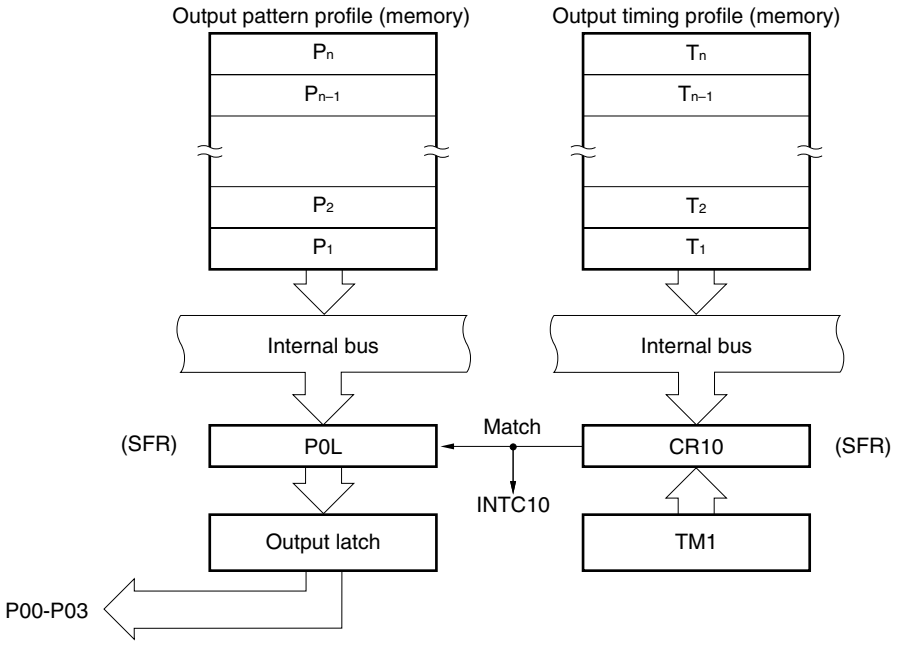
(2) Receive operation of serial interface



Each time a macro service request (INTSR) is generated, the receive data is transferred from RXB to memory. When data n (last byte) is transferred to memory (when no more vacant area is available in the receive data storage buffer), a vectored interrupt request (INTSR) is generated.

(3) Real-time output port

INTC10 and INTC11 are used as the output triggers of the real-time output port. The macro service corresponding to these interrupts can set the next output pattern and interval at the same time. Therefore, INTC10 and INTC11 can control two stepper motors independently. The real-time output port can be also used to control PWM and a DC motor.

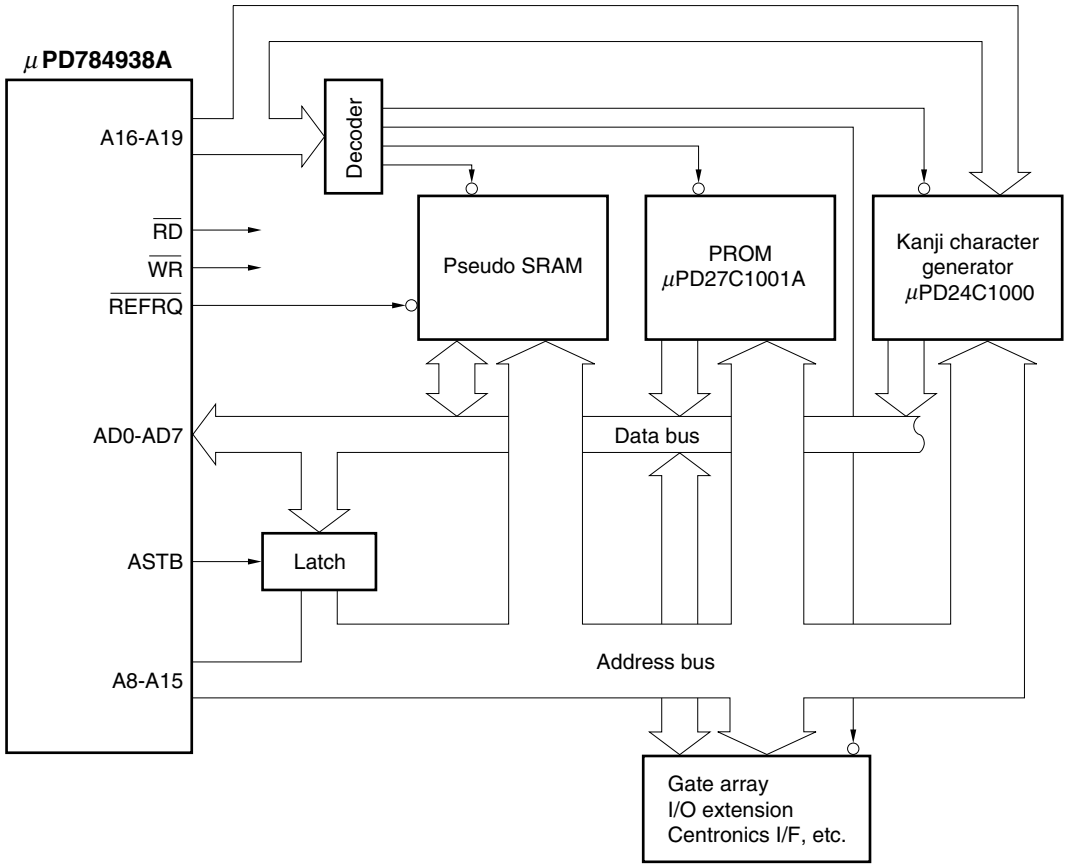


Each time a macro service request (INTC10) is generated, the pattern and timing are transferred to a buffer register (P0L) and a compare register (CR10), respectively. If the contents of the timer register 1 (TM1) coincide with those of CR10, the next INTC10 is generated, and at the same time, the contents of P0L are sent to the output latch. When Tn (last byte) is transferred, a vectored interrupt request (INTC10) is generated. The same applies to INTC11.

10. LOCAL BUS INTERFACE

The local bus interface is used to connect an external memory or I/O (memory mapped I/O), supporting a memory space of 1 MB (refer to **Figure 10-1**).

Figure 10-1. Example of Local Bus Interface



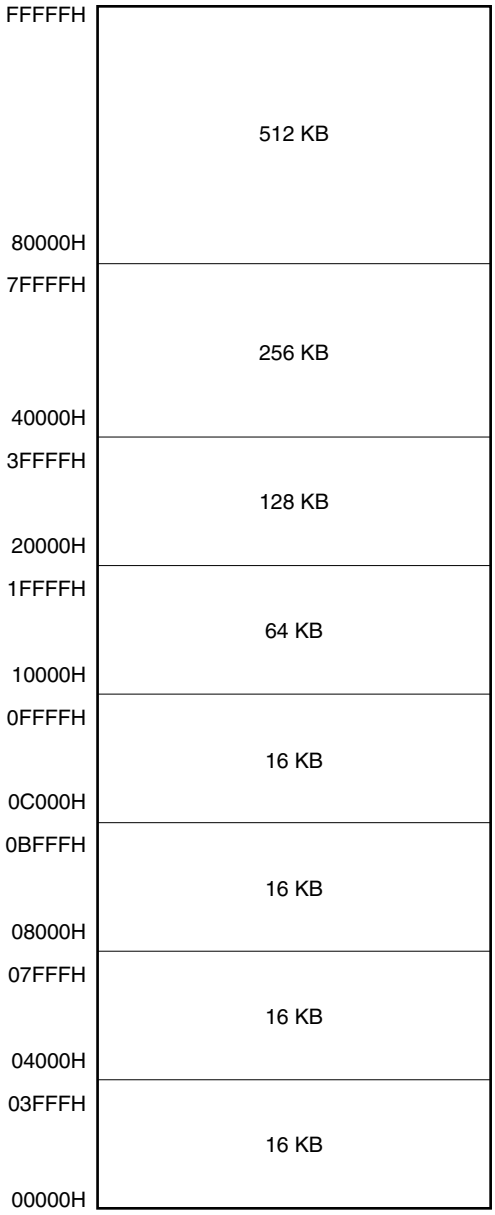
10.1 Memory Expansion

The memory space can be expanded in seven steps, from 256 bytes to 1 MB, by connecting an external program memory or data memory.

10.2 Memory Space

The 1 MB memory space is divided into eight areas by logical addresses. Each of these areas can be controlled by using the programmable wait function and pseudo static RAM refresh function.

Figure 10-2. Memory Space



10.3 Programmable Wait

The memory space can be divided into eight areas. Wait cycles can be inserted while the $\overline{RD}$ and $\overline{WR}$ signals are active for each of these areas independently. Therefore, even when memory with a different access times is connected, the efficiency of the entire system does not drop.

In addition, an address wait function that extends the active period of the ASTB signal to ensure the lapse of address decode time is also available (this function can be used on the entire memory space).

10.4 Pseudo Static RAM Refresh Function

The refresh operations include the following operations:

- Pulse refresh
  A bus cycle that outputs a refresh pulse to the $\overline{REFRQ}$ pin is inserted at specific intervals. The memory is divided into eight areas. When a specified area is accessed, the refresh pulse can be output from the $\overline{REFRQ}$ pin, so that the ordinary memory access is not kept waiting by the refresh cycle.
- Power-down self-refresh
  The contents of the pseudo static RAM are retained by outputting a low level to the $\overline{REFRQ}$ pin in the standby mode.

10.5 Bus Hold Function

The bus hold function facilitates connection of a DMA controller. When a bus hold request signal (HLDRQ) is received from an external bus master, and once the bus cycle under execution is completed, the address bus, address/data bus, and ASTB, $\overline{RD}$, and $\overline{WR}$ pins go into a high-impedance state. The bus hold acknowledge signal (HLDAK) is made active, and the bus is released to the external bus master.

When the bus hold function is used, the external wait function and pseudo static RAM refresh function cannot be used.

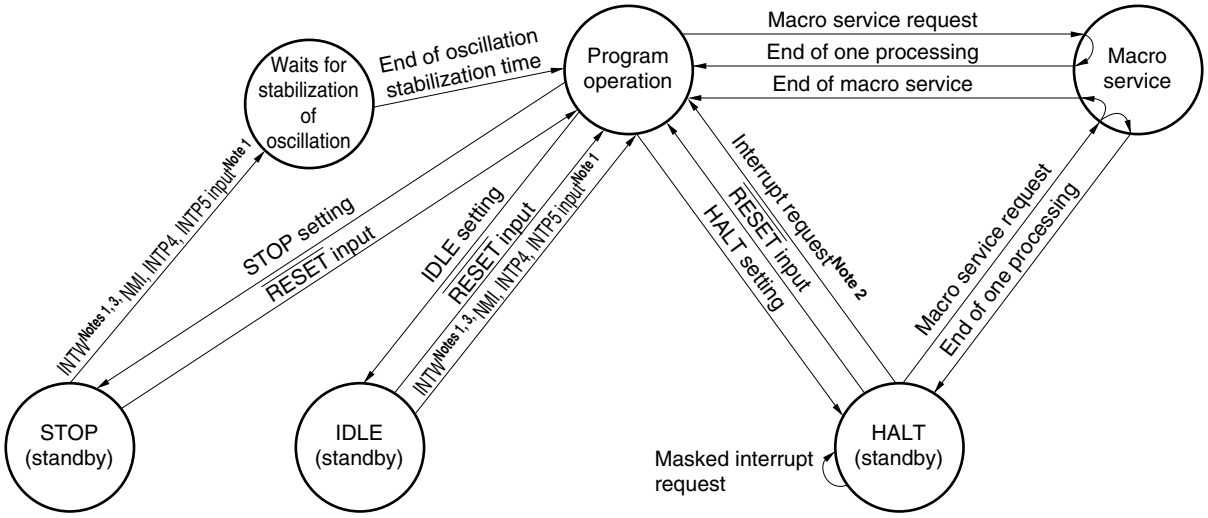
11. STANDBY FUNCTION

The standby function is used to reduce the power consumption of the chip and can be used in the following modes:

- HALT mode: In this mode, the operation clock of the CPU is stopped. This mode can reduce the average power consumption when used in combination with the normal operation mode for intermittent operation.
- IDLE mode: In this mode, the operation of the oscillator continues but the other circuits of the system are stopped. The power consumption in this mode is close to that in the STOP mode, but the time required for the program execution to restore to the normal status from this mode is equivalent to the time in the HALT mode.
- STOP mode: In this mode, the oscillator is stopped. All the operations of the chip are stopped, so that the power consumption is minimized with only leakage current flowing.

These modes are programmable.
A macro service can be started from the HALT mode.

Figure 11-1. Status Transition in Standby Mode



Notes 1. When INTW, INTP4, and INTP5 are not masked
2. Only interrupt requests that are not masked
3. Subclock operation

Remark Only an externally input NMI is valid. The watchdog timer cannot be used to release a standby mode (STOP/HALT/IDLE).

12. RESET FUNCTION

When a low level is input to the $\overline{\text{RESET}}$ pin, the internal hardware is initialized (reset status).

When the $\overline{\text{RESET}}$ pin goes high, the following data is written to the program counter (PC):

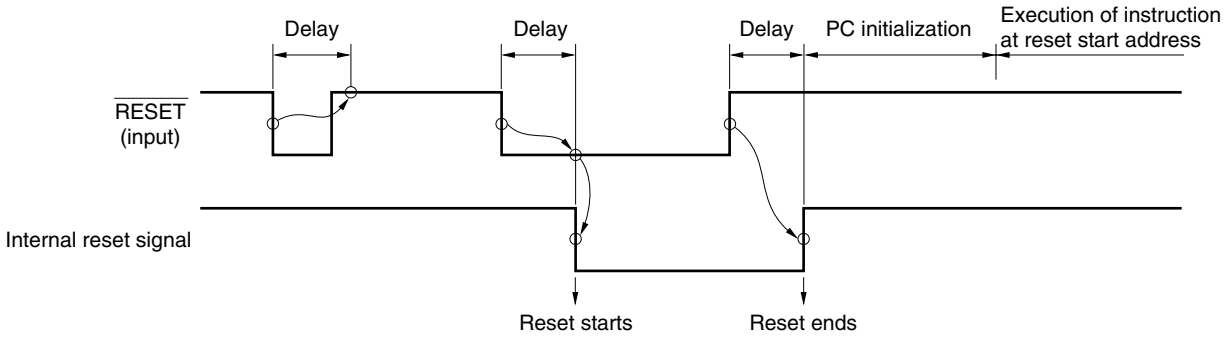
- Lower 8 bits of PC: Contents of address 0000H
- Middle 8 bits of PC: Contents of address 0001H
- Higher 4 bits of PC: 0

The contents of the PC are used as a branch destination address, and program execution is started from that address. Therefore, execution can be reset and started from any address.

Set the contents of each register in software as necessary.

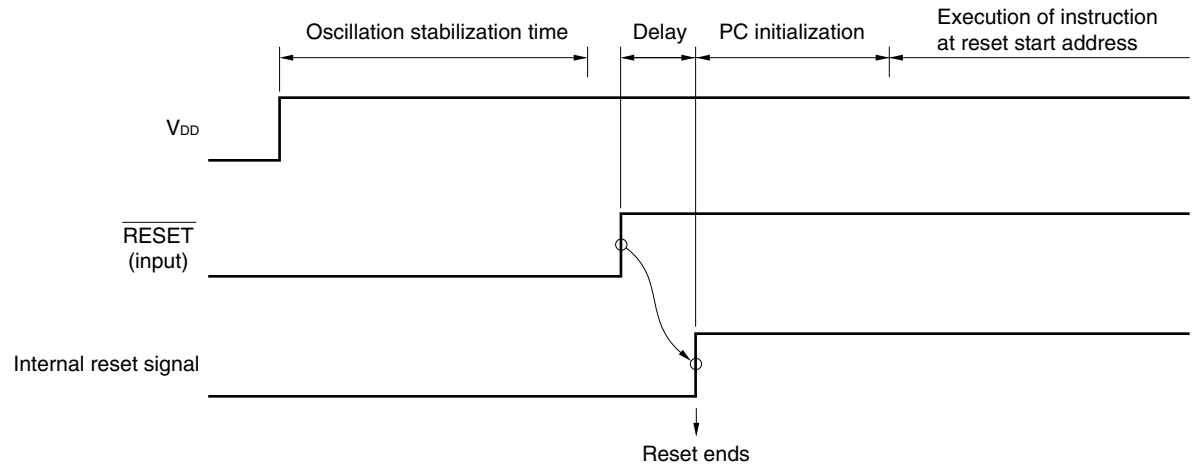
The $\overline{\text{RESET}}$ input circuit has a noise eliminator to prevent malfunctioning due to noise. This noise eliminator is a sampling circuit using analog delay.

Figure 12-1. Reception of $\overline{\text{RESET}}$ Signal



Keep the $\overline{\text{RESET}}$ signal active until the oscillation stabilization time (about 40 ms) has elapsed when the reset operation is performed on power application.

Figure 12-2. Reset Operation on Power Application



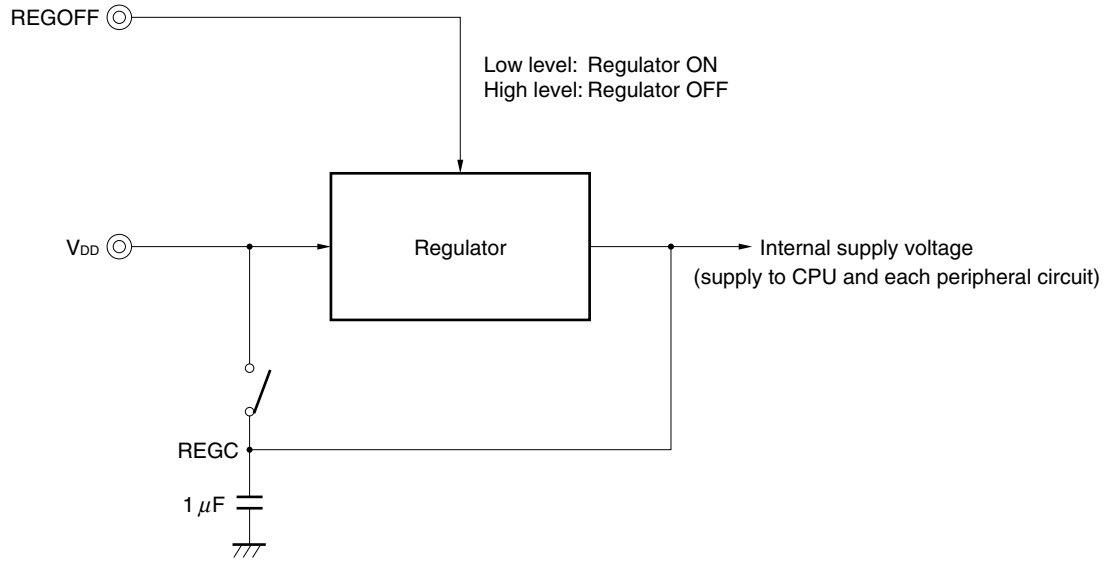
13. REGULATOR

The μPD784938A has a regulator (circuit that helps the internal circuitry operate at a low voltage) to reduce the power consumption of the device. The operation of this regulator is controlled by the input level of the REGOFF pin. When the REGOFF pin goes high, the regulator is turned OFF; when it goes low, the regulator is turned ON. When the regulator is ON, operation at a low voltage become possible. In the μPD784938A, operation with the regulator turned on (REGOFF pin = low level) is recommended.

To stabilize the output voltage of the regulator, connect a capacitor of 1 μF to the REGC pin (regulator stabilization capacitor connecting pin).

When the regulator is stopped, apply the same level as V_{DD} to the REGC pin. Figure 13-1 shows the peripheral circuits of the regulator.

Figure 13-1. Block Diagram of Regulator Peripheral



- **Processing of REGC pin**

When regulator operates	Connect capacitor (1 μF) to stabilize regulator.
When regulator stops	Supply V_{DD}.

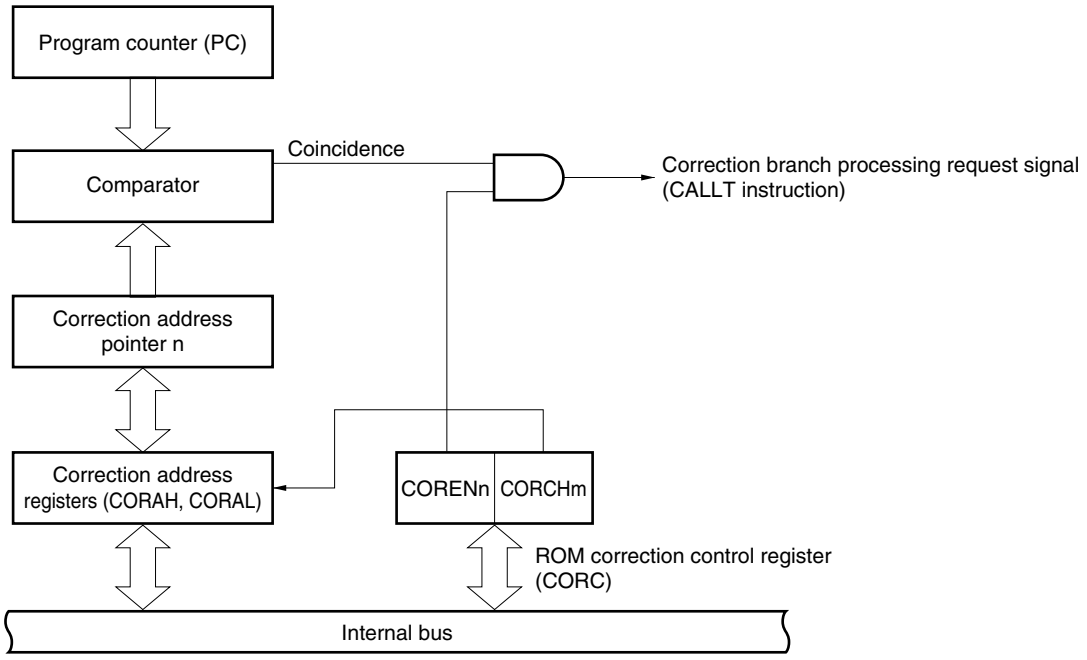
14. ROM CORRECTION

ROM correction is a function to replace part of a program in the internal ROM with a program in the internal RAM for execution.

By using this function, bugs found in the internal ROM can be avoided or the program flow can be changed.

ROM correction can be used at up to four places in the internal ROM (program).

Figure 14-1. Block Diagram of ROM Correction Function



Remark n = 0 to 3, m = 0 or 1

15. INSTRUCTION SET

(1) 8-bit instructions (( ) indicates a combination implemented by using A as r.)

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, SHR, SHL, SOR4, ROL4, DBNZ, PUSH, POP, MOVM, XCHM, CMPME, CMPMNE, CMPMNC, CMPMC, MOVBK, XCHBK, CMPBKE, CMPBKNE, CMPBKNC, CMPBKC

Table 15-1. 8-Bit Instructions and Addressing

First Operand \ Second Operand	#byte	A	r r'	saddr saddr'	sfr	!addr16 !!addr24	mem [saddrp] [%saddrg]	r3 PSWL PSWH	[WHL+] [WHL–]	n	None[Note 2]
A	(MOV) ADD[Note 1]	(MOV) (XCH) (ADD)[Note 1]	MOV XCH (ADD)[Note 1]	(MOV)[Note 6] (XCH)[Note 6] (ADD)[Notes 1, 6]	MOV (XCH) (ADD)[Note 1]	(MOV) (XCH) ADD[Note 1]	MOV XCH ADD[Note 1]	MOV	(MOV) (XCH) (ADD)[Note 1]		
r	MOV ADD[Note 1]	(MOV) (XCH) (ADD)[Note 1]	MOV XCH ADD[Note 1]	MOV XCH ADD[Note 1]	MOV XCH ADD[Note 1]	MOV XCH				ROR[Note 3]	MULU DIVUW INC DEC
saddr	MOV ADD[Note 1]	(MOV)[Note 6] (ADD)[Note 1]	MOV ADD[Note 1]	MOV XCH ADD[Note 1]							INC DEC DBNZ
sfr	MOV ADD[Note 1]	MOV (ADD)[Note 1]	MOV ADD[Note 1]								PUSH POP
!addr16 !!addr24	MOV	(MOV) ADD[Note 1]	MOV								
mem [saddrp] [%saddrg]		MOV ADD[Note 1]									
mem3											ROR4 ROL4
r3 PSWL PSWH	MOV	MOV									
B, C											DBNZ
STBC, WDM	MOV										
[TDE+] [TDE–]		(MOV) (ADD)[Note 1] MOVM[Note 4]							MOVBK[Note 5]		

Notes 1. The operand of ADDC, SUB, SUBC, AND, OR, XOR, and CMP is the same as that of ADD.

2. Either the second operand is not used or the second operand is not an operand address.

3. The operand of ROL, RORC, ROLC, SHR, and SHL is the same as that of ROR.

4. The operand of XCHM, CMPME, CMPMNE, CMPMNC, and CMPMC is the same as that of MOVM.

5. The operand of XCHBK, CMPBKE, CMPBKNE, CMPBKNC, and CMPBKC is the same as that of MOVBK.

6. If saddr is saddr2 in this combination, the code length of some instructions is short.

(2) 16-bit instructions (( ) indicates a combination implemented by using AX as rp.)

MOVW, XCHW, ADDW, SUBW, CMPW, MULUW, MULW, DIVUX, INCW, DECW, SHRW, SHLW, PUSH, POP, ADDWG, SUBWG, PUSHU, POPU, MOVTBLW, MACW, MACSW, SACW

Table 15-2. 16-Bit Instructions and Addressing

First Operand \ Second Operand	#word	AX	rp rp'	saddrp saddrp'	sfrp	!addr16 !!addr24	mem [saddrp] [%saddrg]	[WHL+]	byte	n	None[Note 2]
AX	(MOVW) ADDW[Note 1]	(MOVW) (XCHW) (ADD)[Note 1]	(MOVW) (XCHW) (ADDW)[Note 1]	(MOVW)[Note 3] (XCHW)[Note 3] (ADDW)[Notes 1, 3]	MOVW (XCHW) (ADDW)[Note 1]	(MOVW) XCHW	MOVW XCHW	(MOVW) (XCHW)			
rp	MOVW ADDW[Note 1]	(MOVW) (XCHW) (ADDW)[Note 1]	MOVW XCHW ADDW[Note 1]	MOVW XCHW ADDW[Note 1]	MOVW XCHW ADDW[Note 1]	MOVW				SHRW SHLW	MULW[Note 4] INCW DECW
saddrp	MOVW ADDW[Note 1]	(MOVW)[Note 3] (ADDW)[Note 1]	MOVW ADDW[Note 1]	MOVW XCHW ADDW[Note 1]							INCW DECW
sfrp	MOVW ADDW[Note 1]	MOVW (ADDW)[Note 1]	MOVW ADDW[Note 1]								PUSH POP
!addr16 !!addr24	MOVW	(MOVW)	MOVW						MOVTBLW		
mem [saddrp] [%saddrg]		MOVW									
PSW											PUSH POP
SP	ADDWG SUBWG										
post											PUSH POP PUSHU POPU
[TDE+]		(MOVW)						SACW			
byte											MACW MACSW

Notes 1. The operand of SUBW and CMPW is the same as that of ADDW.

2. Either the second operand is not used or the second operand is not an operand address.

3. If saddrp is saddrp2 in this combination, the code length of some instructions is short.

4. The operand of MULUW and DIVUX is the same as that of MULW.

(3) 24-bit instructions (( ) indicates a combination implemented by using WHL as rg.)

MOVG, ADDG, SUBG, INCG, DECG, PUSH, POP

Table 15-3. 24-Bit Instructions and Addressing

First Operand \ Second Operand	#imm24	WHL	rg rg'	saddrg	!!addr24	mem1	[%saddrg]	SP	None[Note 2]
WHL	(MOVG) (ADDG) (SUBG)	(MOVG) (ADDG) (SUBG)	(MOVG) (ADDG) (SUBG)	(MOVG) ADDG SUBG	(MOVG)	MOVG	MOVG	MOVG	
rg	MOVG ADDG SUBG	(MOVG) (ADDG) (SUBG)	MOVG ADDG SUBG	MOVG	MOVG				INCG DECG PUSH POP
saddrg		(MOVG)	MOVG						
!!addr24		(MOVG)	MOVG						
mem1		MOVG							
[%saddrg]		MOVG							
SP	MOVG	MOVG							INCG DECG

Note Either the second operand is not used or the second operand is not an operand address.

(4) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR, BFSET

Table 15-4. Bit Manipulation Instructions and Addressing

Second Operand / First Operand	CY	saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit	/saddr.bit /sfr.bit /A.bit /X.bit /PSWL.bit /PSWH.bit /mem2.bit /!addr16.bit /!!addr24.bit	None[Note]
CY		MOV1 AND1 OR1 XOR1	AND1 OR1	NOT1 SET1 CLR1
saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit	MOV1			NOT1 SET1 CLR1 BF BT BTCLR BFSET

Note Either the second operand is not used or the second operand is not an operand address.

(5) Call/return instructions/branch instructions

CALL, CALLF, CALLT, BRK, RET, RETI, RETB, RETCS, RETCSB, BRKCS, BR, BNZ, BNE, BZ, BE, BNC, BNL, BC, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, BH, BF, BT, BTCLR, BFSET, DBNZ

Table 15-5. Call/return and Branch Instructions and Addressing

Operand of Instruction Address	$addr20	$!addr20	!addr16	!!addr20	rp	rg	[rp]	[rg]	!addr11	[addr5]	RBn	None[Note]
Basic instruction	BC[Note] BR	CALL BR	CALL BR RETCS RETCSB	CALL BR	CALL BR	CALL BR	CALL BR	CALL BR	CALLF	CALLF	BRKCS	BRK RET RETI RETB
Compound instruction	BF BT BTCLR BFSET DBNZ											

Note The operand of BNZ, BNE, BZ, BE, BNC, BNL, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, and BH is the same as that of BC.

(6) Other instructions

ADJBA, ADJBS, CVTBW, LOCATION, SEL, NOT, EI, DI, SWRS

★ 16. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.3 to +6.5	V
	AV_{DD}		–0.3 to V_{DD} + 0.3	V
	AV_{SS}		–0.3 to V_{SS} + 0.3	V
	AV_{REF1}	A/D converter reference voltage input	–0.3 to V_{DD} + 0.3	V
Input voltage	V_{I1}		–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{IAN}	Analog input voltage	AV_{SS} – 0.3 to AV_{REF1} + 0.3	V
Output voltage	V_O		–0.3 to V_{DD} + 0.3	V
Output current, low	I_{OL}	Per pin	10	mA
		Total of all pins of ports 0, 3, 6, 10 and the P54 to P57 pins	50	mA
		Total of all pins of ports 1, 4, 7, 9, and the P50 to P53, PWM0, PWM1, and $\overline{TX}$ pins	50	mA
Output current, high	I_{OH}	Per pin	–6	mA
		Total of all pins of ports 0, 3, 6, 10 and the P54 to P57 pins	–30	mA
		Total of all pins of ports 1, 4, 7, 9, and the P50 to P53, PWM0, PWM1, and $\overline{TX}$ pins	–30	mA
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

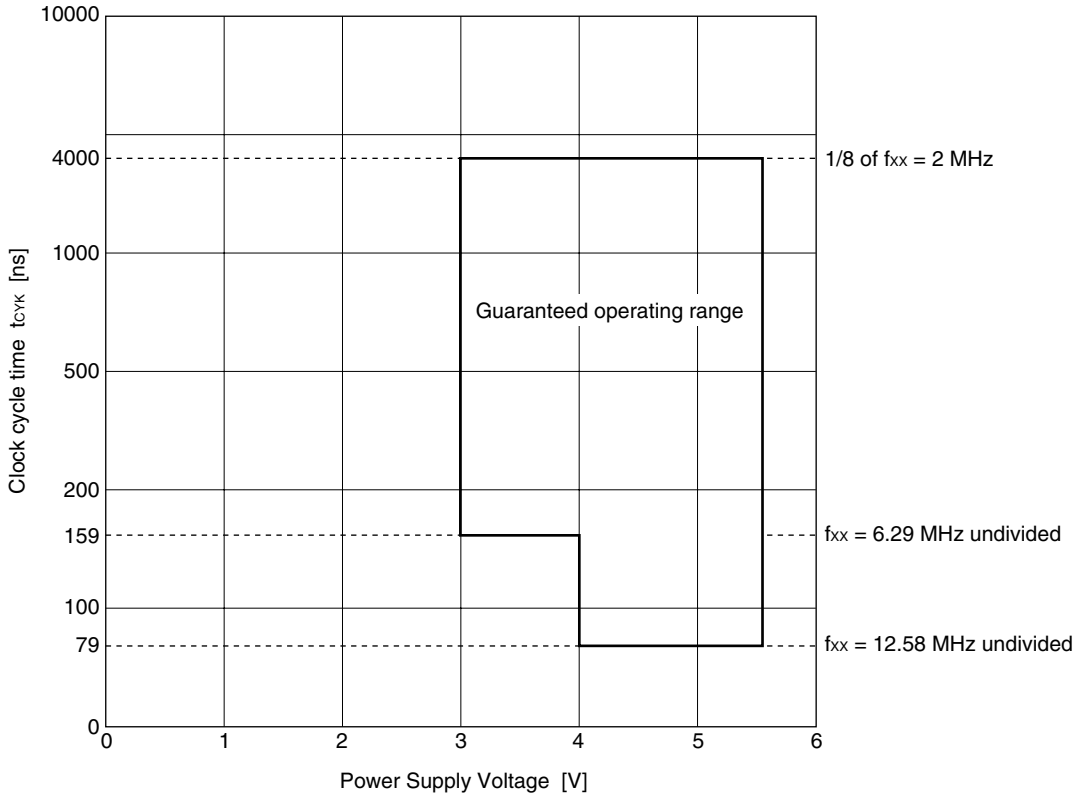
Operating Conditions

- Clock frequency

Clock Frequency	Supply Voltage
2 MHz ≤ f_{XX} ≤ 12.58 MHz	4.0 ≤ V_{DD} ≤ 5.5 V
2 MHz ≤ f_{XX} ≤ 6.29 MHz	3.0 ≤ V_{DD} ≤ 5.5 V

- Operating ambient temperature (T_A): –40 to +85°C
- Power supply voltage and clock cycle time: Refer to **Figure 16-1**
- Selection of internal regulator operation (REGOFF pin: low-level input)

Figure 16-1. Power Supply Voltage and Clock Cycle Time



Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz			15	pF
Output capacitance	C_{OUT}	Unmeasured pins returned to 0 V.			15	pF
I/O capacitance	C_{IO}				15	pF

Main Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 3.0 to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
Oscillator frequency	f_{XX}	Ceramic resonator or recommended resonator	4.0 ≤ V_{DD} ≤ 5.5 V	2.0	12.58	MHz
			3.0 ≤ V_{DD} ≤ 5.5 V	2.0	6.29	MHz

Caution When using the main clock oscillator, wire as follows to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Remarks 1. Connect a 12.582912 MHz or 6.291456 MHz oscillator to operate the internal clock timer with the main clock.

2. For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 3.0 to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillator frequency	f_{XT}	Ceramic resonator or crystal resonator	32	32.768	35	KHz
Oscillation stabilization time	f_{sxt}	4.5 ≤ V_{DD} ≤ 5.5 V		1.2	2	s
					10	s
Oscillation hold voltage	V_{DDXT}		3.0		5.5	V
Watch timer operating voltage	V_{DDW}		3.0		5.5	V

DC Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, low[Note]	V_{IL1}	P10, P11, P13 to P17, P30, P31, P34 to P37, P70 to P77, P90 to P97, P100 to P104, X1, X2, XT1, XT2		–0.3		$0.3V_{DD}$	V
	V_{IL2}	P12, P20 to P27, P32, P33, P105 to P107 $\overline{RESET}$		–0.3		$0.2V_{DD}$	V
	V_{IL3}	P00 to P07, P40 to P47,	4.5 ≤ V_{DD} ≤ 5.5 V	–0.3		0.8	V
	V_{IL4}	P50 to P57, P60 to P67		–0.3		$0.2V_{DD}$	V
Input voltage, high	V_{IH1}	P10, P11, P13 to P17, P30, P31, P34 to P37, P70 to P77, P90 to P97, P100 to P104, X1, X2, XT1, XT2		$0.7V_{DD}$		V_{DD}+0.3	V
	V_{IH2}	P12, P20 to P27, P32, P33, P105 to P107 $\overline{RESET}$		$0.8V_{DD}$		V_{DD}+0.3	V
	V_{IH3}	P00 to P07, P40 to P47,	4.5 ≤ V_{DD} ≤ 5.5 V	2.2		V_{DD}+0.3	V
	V_{IH4}	P50 to P57, P60 to P67		$0.7V_{DD}$		$0.3V_{DD}$	V
Output voltage, low	V_{OL1}	I_{OL} = 20 μA				0.1	V
		I_{OL} = 100 μA				0.2	V
		I_{OL} = 2 mA				0.4	V
	V_{OL2}	I_{OL} = 8 mA, P10 to P17, P40 to P47, P50 to P57	4.5 ≤ V_{DD} ≤ 5.5 V			1.0	V
Output voltage, high	V_{OH1}	I_{OH} = –20 μA		V_{DD}–0.1			V
		I_{OL} = –100 μA		V_{DD}–0.2			V
		I_{OL} = –2 mA		V_{DD}–1.0			V
	V_{OH2}	I_{OL} = –5 mA, P10 to P17, P40 to P47, P50 to P57	4.5 V ≤ V_{DD} ≤ 5.5 V	V_{DD}–2.4			V
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	For pins other than X1, X2, XT1, and XT2			10	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
Input leakage current, high	I_{LIH1}	V_{IN} = V_{DD}	For pins other than X1, X2, XT1, and XT2			10	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
Output leakage current, low	I_{LOL1}	V_{OUT} = 0 V				–10	μA
Output leakage current, high	I_{LOH1}	V_{OUT} = V_{DD}				10	μA

Note These values are valid when the pull-up resistor is off.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Power supply current	I_{DD1}	Operating mode	f_{XX} = 12.58 MHz, 4.0 V ≤ V_{DD} ≤ 5.5 V		10	20	mA
			f_{XX} = 6.29 MHz, 3.0 V ≤ V_{DD} ≤ 5.5 V		5	10	mA
	I_{DD2}	HALT mode	f_{XX} = 12.58 MHz, when peripheral clock stops[Note], 4.0 V ≤ V_{DD} ≤ 5.5 V		2	4	mA
			f_{XX} = 6.29 MHz, when peripheral clock stops[Note], 3.0 V ≤ V_{DD} ≤ 5.5 V		1.2	2.4	mA
	I_{DD3}	IDLE mode	f_{XX} = 12.58 MHz, 4.0 ≤ V_{DD} ≤ 5.5 V		0.6	1.2	mA
			f_{XX} = 6.29 MHz, 3.0 V ≤ V_{DD} ≤ 5.5 V		0.3	0.6	mA
Data hold voltage	V_{DDDR}	STOP mode		2.5		5.5	V
Data hold current	I_{DDDR}	STOP mode	V_{DD} = 2.5 V, subclock stops		2	10	μA
			V_{DD} = 5.5 V, subclock stops		10	50	μA
Pull-up resistor	R_L	V_{IN} = 0 V		15	40	80	kΩ

Note When the main system clock: f_{CLK} = f_{XX}/8 is selected (set by the standby control register (STBC)) and the watch timer is operating.

Remark These values are valid when the internal regulator is on (REGOFF pin = low-level input).

AC Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(1) Read/write operation (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time	t_{CYK}	4.0 ≤ V_{DD} ≤ 5.5 V	79			ns
		V_{DD} = 3.0 V	159			ns
Address setup time (to ASTB↓)	t_{SAST}	V_{DD} = 5.0 V	(0.5+a) T–11			ns
		V_{DD} = 3.0 V	(0.5+a) T–15			ns
Address hold time (from ASTB↓)	t_{HSTLA}	V_{DD} = 5.0 V	0.5T–19			ns
		V_{DD} = 3.0 V	0.5T–24			ns
ASTB high-level width	t_{WSTH}	V_{DD} = 5.0 V	(0.5+a) T–17			ns
		V_{DD} = 3.0 V	(0.5+a) T–40			ns
Address hold time (from $\overline{RD}$↑)	t_{HRA}	V_{DD} = 5.0 V	0.5T–14			ns
		V_{DD} = 3.0 V	0.5T–14			ns
Delay from address to $\overline{RD}$↓	t_{DAR}	V_{DD} = 5.0 V	(1+a) T–5			ns
		V_{DD} = 3.0 V	(1+a) T–10			ns
Address float time (from $\overline{RD}$↓)	t_{FAR}				0	ns
Data input time from address	t_{DAID}	V_{DD} = 5.0 V			(2.5+a+n) T–37	ns
		V_{DD} = 3.0 V			(2.5+a+n) T–52	ns
Data input time from ASTB↓	t_{DSTID}	V_{DD} = 5.0 V			(2+n) T–35	ns
		V_{DD} = 3.0 V			(2+n) T–50	ns
Data input time from $\overline{RD}$↓	t_{DRID}	V_{DD} = 5.0 V			(1.5+n) T–40	ns
		V_{DD} = 3.0 V			(1.5+n) T–50	ns
Delay from ASTB ↓ to $\overline{RD}$↓	t_{DSTR}	V_{DD} = 5.0 V	0.5T–9			ns
		V_{DD} = 3.0 V	0.5T–9			ns
Data hold time (from $\overline{RD}$↑)	t_{HRID}		0			ns
Address active time from $\overline{RD}$↑	t_{DRA}	V_{DD} = 5.0 V	0.5T–2			ns
		V_{DD} = 3.0 V	0.5T–12			ns
Delay from $\overline{RD}$↑ to ASTB↑	t_{DRST}	V_{DD} = 5.0 V	0.5T–9			ns
		V_{DD} = 3.0 V	0.5T–9			ns
$\overline{RD}$ low-level width	t_{WRL}	V_{DD} = 5.0 V	(1.5+n) T–25			ns
		V_{DD} = 3.0 V	(1.5+n) T–30			ns

Remarks 1. T: t_{CYK} = 1/f_{CLK} (f_{CLK}: internal system clock cycle)

2. a: 1 during address wait; otherwise 0

3. n: Number of wait states (n ≥ 0)

4. Calculated as T = 79 ns (min.) @ V_{DD} = 5.0 V

5. Calculated as T = 159 ns (min.) @ V_{DD} = 3.0 V

AC Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(1) Read/write operation (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Delay from address to $\overline{WR}$↓	t_{DAW}	V_{DD} = 5.0 V	(1+a) T–5			ns
		V_{DD} = 3.0 V	(1+a) T–10			ns
Address hold time (from $\overline{WR}$↑)	t_{HWA}	V_{DD} = 5.0 V	0.5T–14			ns
		V_{DD} = 3.0 V	0.5T–14			ns
Delay from ASTB ↓ to data output	t_{DSTOD}	V_{DD} = 5.0 V			0.5T+15	ns
		V_{DD} = 3.0 V			0.5T+20	ns
Data output time from $\overline{WR}$↓	t_{DWOD}				15	ns
Delay from ASTB ↓ to $\overline{WR}$↓	t_{DSTW}	V_{DD} = 5.0 V	0.5T–9			ns
		V_{DD} = 3.0 V	0.5T–9			ns
Data setup time (to $\overline{WR}$↑)	t_{SODWR}	V_{DD} = 5.0 V	(1.5+n) T–20			ns
		V_{DD} = 3.0 V	(1.5+n) T–25			ns
Data hold time (from $\overline{WR}$↑)	t_{HWOD}	V_{DD} = 5.0 V	0.5T–14			ns
		V_{DD} = 3.0 V	0.5T–14			ns
Delay from $\overline{WR}$ ↑ to ASTB↑	t_{DWST}	V_{DD} = 5.0 V	0.5T–9			ns
		V_{DD} = 3.0 V	0.5T–9			ns
$\overline{WR}$ low-level width	t_{WWL}	V_{DD} = 5.0 V	(1.5+n) T–25			ns
		V_{DD} = 3.0 V	(1.5+n) T–30			ns

Remarks 1. T: t_{CYK} = 1/f_{CLK} (f_{CLK}: internal system clock cycle)

2. a: 1 during address wait; otherwise 0

3. n: Number of wait states (n ≥ 0)

4. Calculated as T = 79 ns (min.) @ V_{DD} = 5.0 V

5. Calculated as T = 159 ns (min.) @ V_{DD} = 3.0 V

AC Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(2) External wait timing

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{WAIT}$↓ input time from address	t_{DAWT}	V_{DD} = 5.0 V			(2+a) T–40	ns
		V_{DD} = 3.0 V			(2+a) T–60	ns
$\overline{WAIT}$↓ input time from ASTB↓	t_{DSTWT}	V_{DD} = 5.0 V			1.5T–40	ns
		V_{DD} = 3.0 V			1.5T–60	ns
$\overline{WAIT}$ hold time from ASTB ↓	t_{HSTWTH}	V_{DD} = 5.0 V	(0.5+n) T+5			ns
		V_{DD} = 3.0 V	(0.5+n) T+10			ns
Delay from ASTB↓ to $\overline{WAIT}$↑	t_{DSTWTH}	V_{DD} = 5.0 V			(1.5+a) T–40	ns
		V_{DD} = 3.0 V			(1.5+a) T–60	ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{DRWTL}	V_{DD} = 5.0 V			T–40	ns
		V_{DD} = 3.0 V			T–60	ns
$\overline{WAIT}$ hold time from $\overline{RD}$↓	t_{HRWT}	V_{DD} = 5.0 V	nT+5			ns
		V_{DD} = 3.0 V	nT+10			ns
Delay from $\overline{RD}$↓ to $\overline{WAIT}$↑	t_{DRWTH}	V_{DD} = 5.0 V			(1+n) T–40	ns
		V_{DD} = 3.0 V			(1+n) T–60	ns
Data input time from $\overline{WAIT}$↑	t_{DWTID}	V_{DD} = 5.0 V			0.5T–5	ns
		V_{DD} = 3.0 V			0.5T–10	ns
Delay from $\overline{WAIT}$↑ to $\overline{RD}$↑	t_{DWTR}	V_{DD} = 5.0 V	0.5T			ns
		V_{DD} = 3.0 V	0.5T			ns
Delay from $\overline{WAIT}$↑ to $\overline{WR}$↑	t_{DWTW}	V_{DD} = 5.0 V	0.5T			ns
		V_{DD} = 3.0 V	0.5T			ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{DWWTL}	V_{DD} = 5.0 V			T–40	ns
		V_{DD} = 3.0 V			T–60	ns
$\overline{WAIT}$ hold time from $\overline{WR}$↓	t_{HWWT}	V_{DD} = 5.0 V	nT+5			ns
		V_{DD} = 3.0 V	nT+10			ns
Delay from $\overline{WR}$↓ to $\overline{WAIT}$↑	t_{DWWTH}	V_{DD} = 5.0 V			(1+n) T–40	ns
		V_{DD} = 3.0 V			(1+n) T–60	ns

Remarks 1. T: t_{CYK} = 1/f_{CLK} (f_{CLK}: internal system clock cycle)

2. a: 1 during address wait; otherwise 0

3. n: Number of wait states (n ≥ 0)

4. Calculated as T = 79 ns (min.) @ V_{DD} = 5.0 V

5. Calculated as T = 159 ns (min.) @ V_{DD} = 3.0 V

AC Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(3) Bus hold/refresh timing

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Delay from HLDRQ↑ to float	t_{FHQC}	V_{DD} = 5.0 V			(2+4+a+n) T+50	ns
		V_{DD} = 3.0 V			(2+4+a+n) T+50	ns
Delay from HLDRQ↑ to HLDAK↑	$t_{DHQHHAH}$	V_{DD} = 5.0 V			(3+4+a+n) T+30	ns
		V_{DD} = 3.0 V			(3+4+a+n) T+40	ns
Delay from float to HLDAK↑	t_{DCFHA}	V_{DD} = 5.0 V			T+30	ns
		V_{DD} = 3.0 V			T+30	ns
Delay from HLDRQ↓ to HLDAK↓	$t_{DHQLHAL}$	V_{DD} = 5.0 V			2T+40	ns
		V_{DD} = 3.0 V			2T+60	ns
Delay from HLDAK↓ to active	t_{DHAC}	V_{DD} = 5.0 V	T–20			ns
		V_{DD} = 3.0 V	T–30			ns
Random read/write cycle time	t_{RC}	V_{DD} = 5.0 V	3T			ns
		V_{DD} = 3.0 V	3T			ns
$\overline{REFRQ}$ low-level pulse width	t_{WRFQL}	V_{DD} = 5.0 V	1.5T–25			ns
		V_{DD} = 3.0 V	1.5T–30			ns
Delay from ASTB↓ to $\overline{REFRQ}$	t_{DSTRFQ}	V_{DD} = 5.0 V	0.5T–9			ns
		V_{DD} = 3.0 V	0.5T–9			ns
Delay from RD↑ to $\overline{REFRQ}$	t_{DRRFQ}	V_{DD} = 5.0 V	1.5T–9			ns
		V_{DD} = 3.0 V	1.5T–9			ns
Delay from WR↑ to $\overline{REFRQ}$	t_{DWRFQ}	V_{DD} = 5.0 V	1.5T–9			ns
		V_{DD} = 3.0 V	1.5T–9			ns
Delay from $\overline{REFRQ}$↑ to ASTB	t_{DRFQST}	V_{DD} = 5.0 V	0.5T–9			ns
		V_{DD} = 3.0 V	0.5T–9			ns
$\overline{REFRQ}$ high-level pulse width	t_{WRFQH}	V_{DD} = 5.0 V	1.5T–25			ns
		V_{DD} = 3.0 V	1.5T–30			ns

Remarks 1. T: t_{CYK} = 1/f_{CLK} (f_{CLK}: internal system clock cycle)

2. a: 1 during address wait; otherwise 0

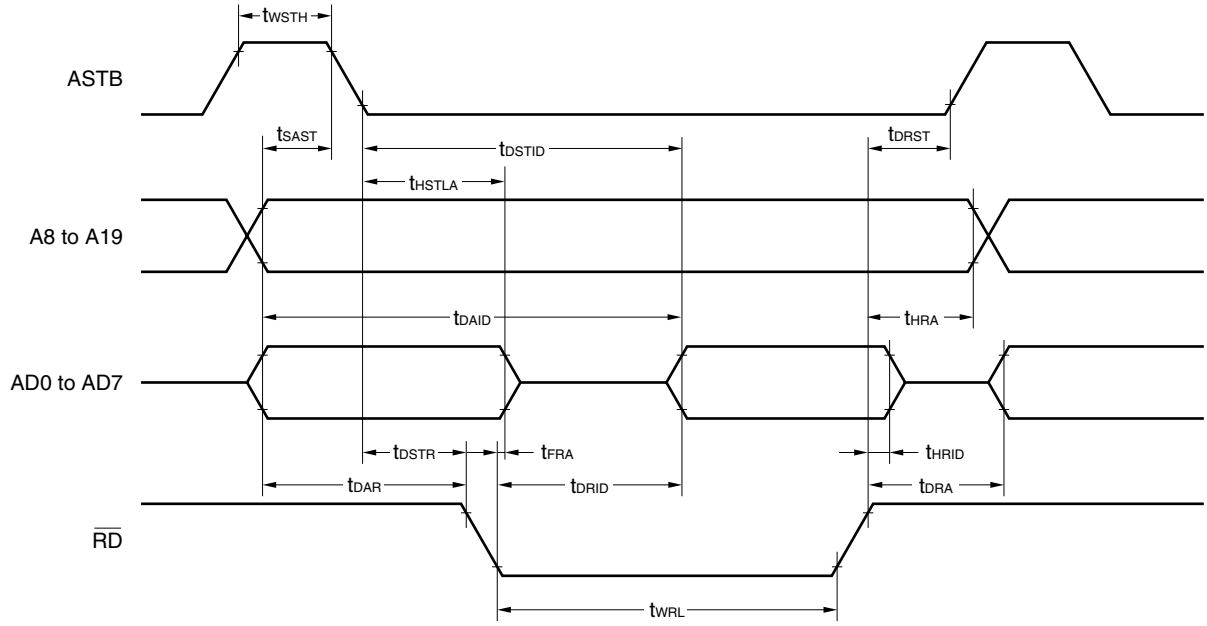
3. n: Number of wait states (n ≥ 0)

4. Calculated as T = 79 ns (min.) @ V_{DD} = 5.0 V

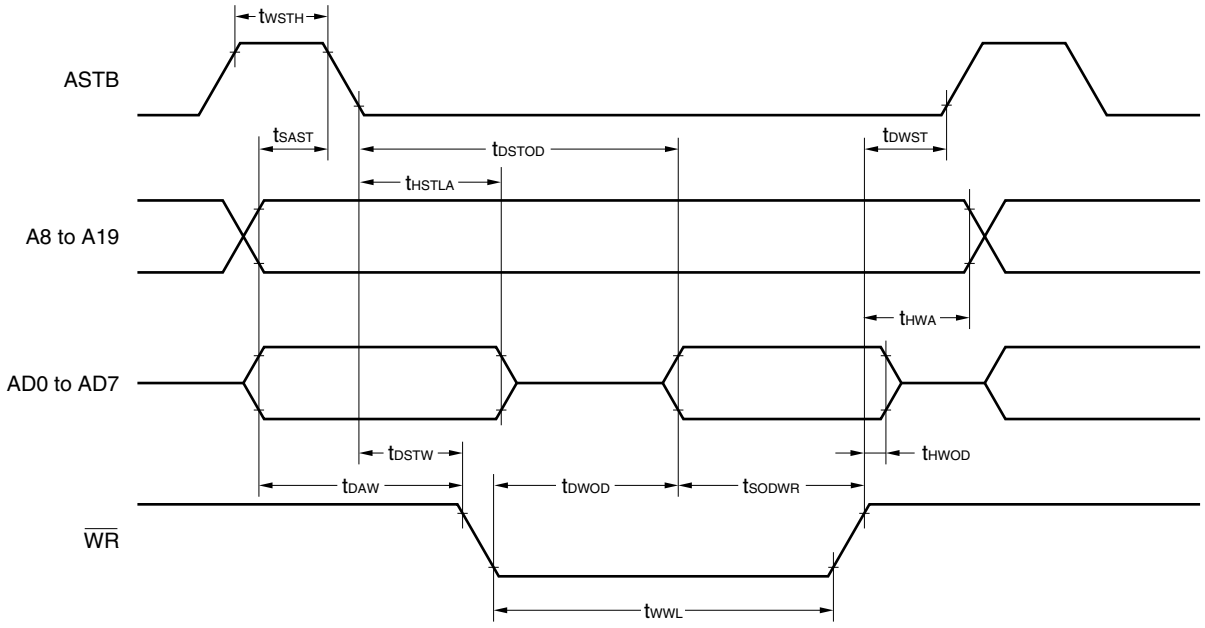
5. Calculated as T = 159 ns (min.) @ V_{DD} = 3.0 V

Timing Waveform

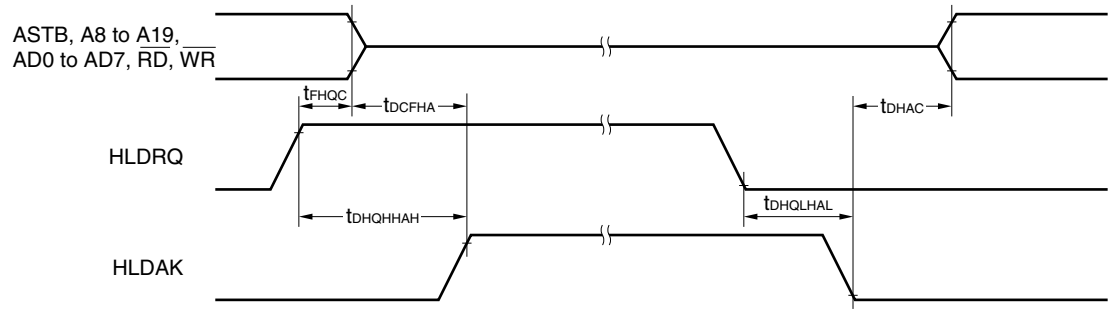
(1) Read operation



(2) Write operation

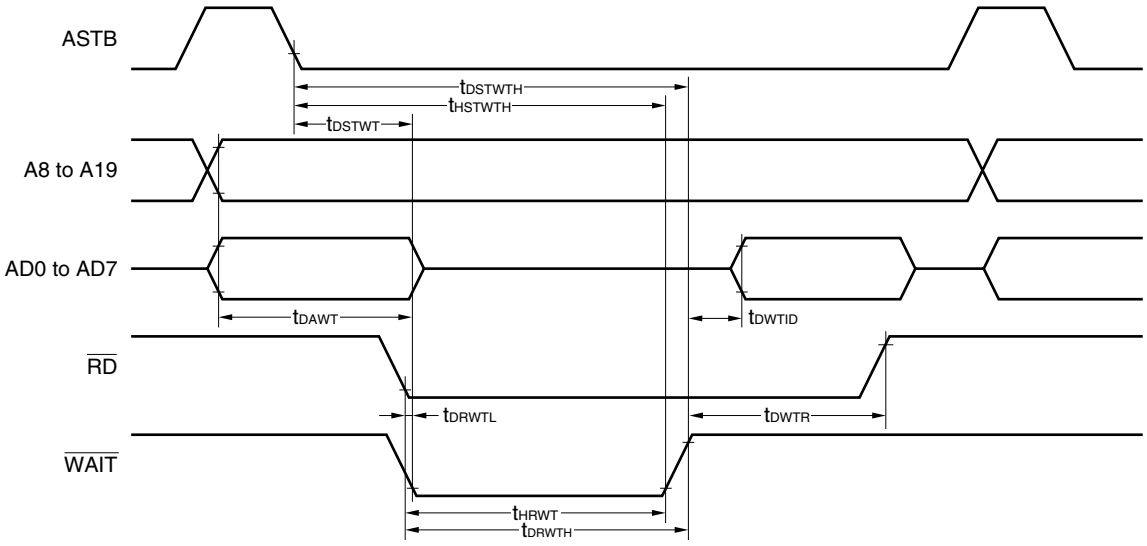


Hold Timing

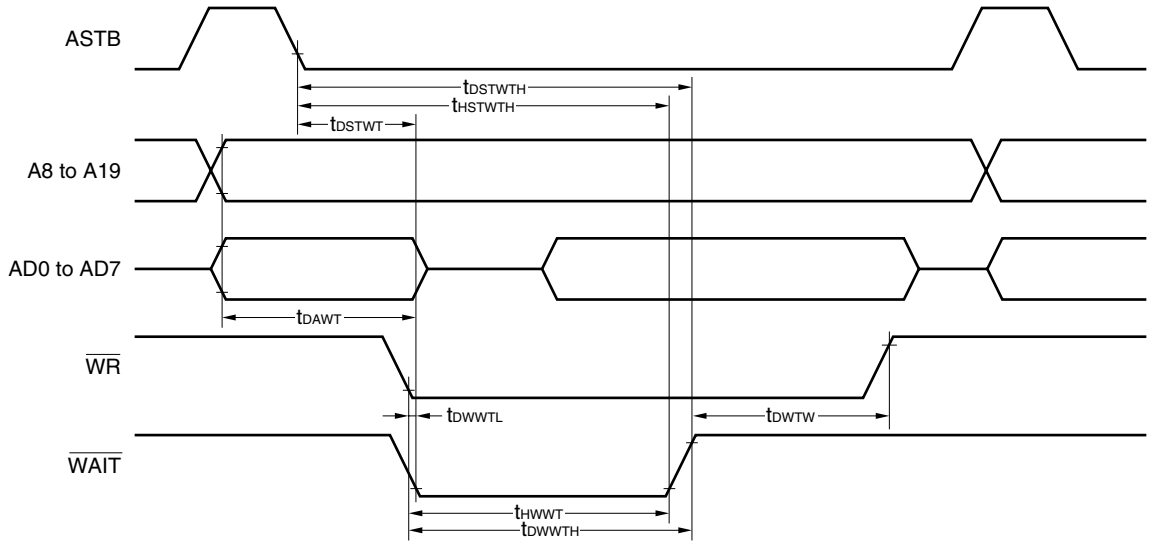


External Wait Signal Input Timing

(1) Read operation

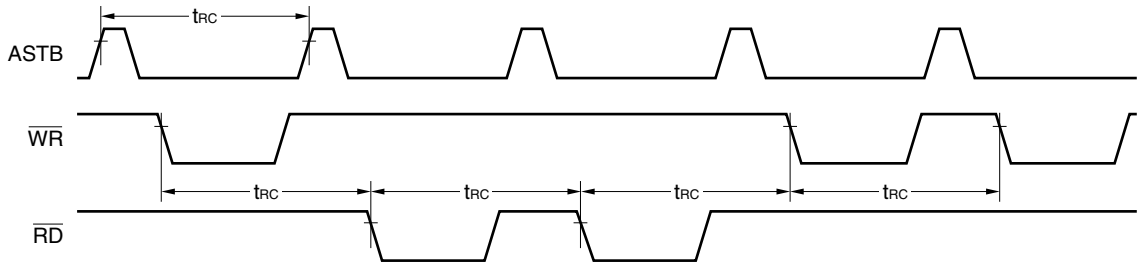


(2) Write operation

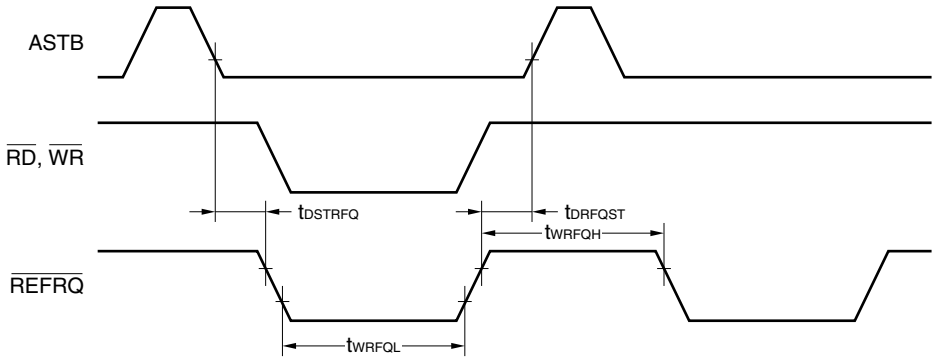


Refresh Timing Waveform

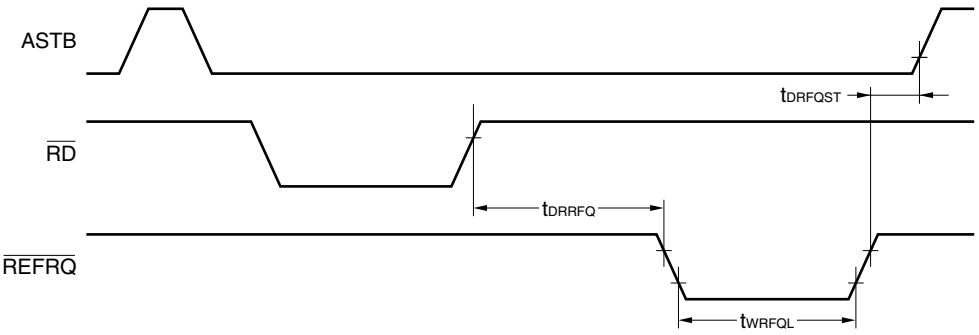
(1) Random read/write cycle



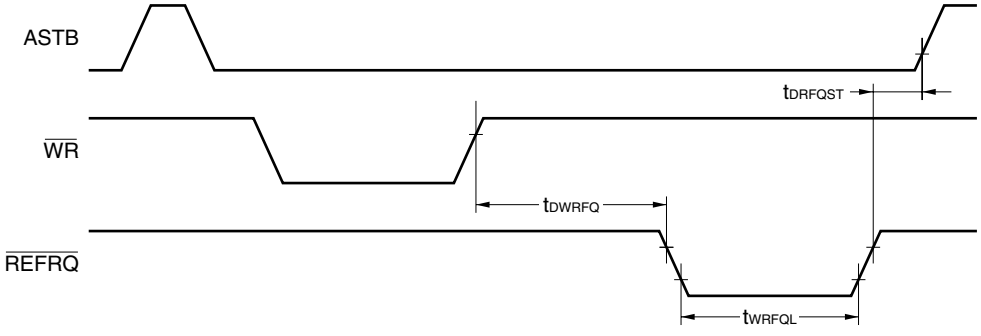
(2) When refresh memory is accessed for a read and write at the same time



(3) Refresh after a read



(4) Refresh after a write



Serial Operation (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(a) CSI0, CSI3 3-wire serial I/O mode ($\overline{SCK0}$, $\overline{SCK3}$ ... External clock input)

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
$\overline{SCK}$ cycle time ($\overline{SCK0}$, $\overline{SCK3}$)	t_{CYSK0}, t_{CYSK3}	SO0 and SO3 are CMOS outputs	f_{CLK} = f_{XX}	8/f_{XX}		ns
			Except f_{CLK} = f_{XX}	4/f_{CLK}		ns
$\overline{SCK}$ low-level width ($\overline{SCK0}$, $\overline{SCK3}$)	t_{WSKL0}, t_{WSKL3}	SO0 and SO3 are CMOS outputs	f_{CLK} = f_{XX}	4/f_{XX}–40		ns
			Except f_{CLK} = f_{XX}	2/f_{CLK}–40		ns
$\overline{SCK}$ high-level width ($\overline{SCK0}$, $\overline{SCK3}$)	t_{WSKH0}, t_{WSKH3}	SO0 and SO3 are CMOS outputs	f_{CLK} = f_{XX}	4/f_{XX}–40		ns
			Except f_{CLK} = f_{XX}	2/f_{CLK}–40		ns
SI0, SI3 setup time (to $\overline{SCK0}$, $\overline{SCK3}$↑)	t_{SSSK0}, t_{SSSK3}			80		ns
SI0, SI3 hold time (from $\overline{SCK0}$, $\overline{SCK3}$↑)	t_{HSSK0}, t_{HSSK3}			1/f_{CLK}+80		ns
Output delay time from $\overline{SCK0}$, $\overline{SCK3}$↓	t_{DBSK0}, t_{DBSK3}	CMOS output		0	1/f_{CLK}+150	ns
		N-ch Open-drain output R_L = 1 kΩ		0	1/f_{CLK}+400	ns
SO0, SO3 output hold time (from $\overline{SCK0}$, $\overline{SCK3}$↑)	t_{HSBSK0}, t_{HSBSK3}	When data is transferred		0.5t_{CYSK0}–40, 0.5t_{CYSK3}–40		ns

Remarks 1. The values in this table are those when CL = 100 pF.

2. f_{XX}: External oscillator frequency (f_{XX} = 12.58 MHz or f_{XX} = 6.29 MHz)

3. f_{CLK}: System clock oscillation frequency (selectable from f_{XX}, f_{XX}/2, f_{XX}/4, and f_{XX}/8 by the standby control register (STBC))

(b) CSI0, CSI3 3-wire serial I/O mode ($\overline{SCK0}$, $\overline{SCK3}$ ... Internal clock output)

Parameter	Symbol	Conditions		MIN.	MAX.	Unit
$\overline{SCK}$ cycle time ($\overline{SCK0}$, $\overline{SCK3}$)	t_{CYSK0}, t_{CYSK3}	SO0 and SO3 are CMOS outputs	Except f_{CLK} = f_{XX}/8	8/f_{XX}		ns
			f_{CLK} = f_{XX}/8	16/f_{XX}		ns
$\overline{SCK}$ low-level width ($\overline{SCK0}$, $\overline{SCK3}$)	t_{WSKL0}, t_{WSKL3}	SO0 and SO3 are CMOS outputs	Except f_{CLK} = f_{XX}/8	4/f_{XX}–40		ns
			f_{CLK} = f_{XX}/8	8/f_{XX}–40		ns
$\overline{SCK}$ high-level width ($\overline{SCK0}$, $\overline{SCK3}$)	t_{WSKH0}, t_{WSKH3}	SO0 and SO3 are CMOS outputs	Except f_{CLK} = f_{XX}/8	4/f_{XX}–40		ns
			f_{CLK} = f_{XX}/8	8/f_{XX}–40		ns
SI0, SI3 setup time (to $\overline{SCK0}$, $\overline{SCK3}$↑)	t_{SSSK0}, t_{SSSK3}			80		ns
SI0, SI3 hold time (from $\overline{SCK0}$, $\overline{SCK3}$↑)	t_{HSSK0}, t_{HSSK3}			80		ns
Output delay time from $\overline{SCK0}$, $\overline{SCK3}$↓	t_{DBSK0}, t_{DBSK3}	CMOS output		0	150	ns
		N-ch Open-drain output R_L = 1 kΩ		0	400	ns
SO0, SO3 output hold time (from $\overline{SCK0}$, $\overline{SCK3}$↑)	t_{HSBSK0}, t_{HSBSK3}	When data is transferred		0.5t_{CYSK0}–40, 0.5t_{CYSK3}–40		ns

Remarks 1. The values in this table are those when CL = 100 pF.

2. f_{XX}: External oscillator frequency (f_{XX} = 12.58 MHz or f_{XX} = 6.29 MHz)

3. f_{CLK}: System clock oscillation frequency (selectable from f_{XX}, f_{XX}/2, f_{XX}/4, and f_{XX}/8 by the standby control register (STBC))

Serial Operation (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(c) UART0, UART3 (asynchronous serial interface mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK0, ASCK2 cycle time	t_{CYASK}	4.0 ≤ V_{DD} ≤ 5.5 V	160			ns
			320			ns
ASCK0, ASCK2 low-level width	t_{WASKL}	4.0 ≤ V_{DD} ≤ 5.5 V	65			ns
			120			ns
ASCK0, ASCK2 high-level width	t_{WASKH}	4.0 ≤ V_{DD} ≤ 5.5 V	65			ns
			120			ns

Serial Operation (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(d) IOE1, IOE2 3-wire serial I/O mode ($\overline{SCK1}$, $\overline{SCK2}$ ... External clock input)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCK}$ cycle time ($\overline{SCK1}$, $\overline{SCK2}$)	t_{CYSK1}	4.0 ≤ V_{DD} ≤ 5.5 V	640		ns
	t_{CYSK2}		1280		ns
$\overline{SCK}$ low-level width ($\overline{SCK1}$, $\overline{SCK2}$)	t_{WSKL1},	4.0 ≤ V_{DD} ≤ 5.5 V	280		ns
	t_{WSKL2}		600		ns
$\overline{SCK}$ high-level width ($\overline{SCK1}$, $\overline{SCK2}$)	t_{WSKH1},	4.0 ≤ V_{DD} ≤ 5.5 V	280		ns
	t_{WSKH2}		600		ns
SI1, SI2 setup time (to $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{SSSK1}, t_{SSSK2}		40		ns
SI1, SI2 hold time (from $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{HSSK1}, t_{HSSK2}		40		ns
Output delay time from $\overline{SCK1}$, $\overline{SCK2}$↓	t_{DSOSK1}, t_{DSOSK2}		0	50	ns
SO1, SO2 output hold time (from $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{HSOSK1}, t_{HSOSK2}	When data is transferred	$0.5t_{CYSK1}$–40, $0.5t_{CYSK2}$–40		ns

Remarks 1. The values in this table are those when CL = 100 pF.

2. T: Selected serial clock cycle. The minimum value is 8/fxx.

(e) IOE1, IOE2 3-wire serial I/O mode ($\overline{SCK1}$, $\overline{SCK2}$ ... Internal clock output)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCK}$ cycle time ($\overline{SCK1}$, $\overline{SCK2}$)	t_{CYSK1} t_{CYSK2}		T		ns
$\overline{SCK}$ low-level width ($\overline{SCK1}$, $\overline{SCK2}$)	t_{WSKL1}, t_{WSKL2}		0.5T–40		ns
$\overline{SCK}$ high-level width ($\overline{SCK1}$, $\overline{SCK2}$)	t_{WSKH1}, t_{WSKH2}		0.5T–40		ns
SI1, SI2 setup time (to $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{SSSK1}, t_{SSSK2}		40		ns
SI1, SI2 hold time (from $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{HSSK1}, t_{HSSK2}		40		ns
Output delay time from $\overline{SCK1}$, $\overline{SCK2}$↓	t_{DSOSK1}, t_{DSOSK2}		0	50	ns
SO1, SO2 output hold time (from $\overline{SCK1}$, $\overline{SCK2}$↑)	t_{HSOSK1}, t_{HSOSK2}	When data is transferred	$0.5t_{CYSK1}$–40, $0.5t_{CYSK2}$–40		ns

Remarks 1. The values in this table are those when CL = 100 pF.

2. T: Selected serial clock cycle. The minimum value is 8/fxx.

Other Operations (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
NMI high-/low-level width	t_{WNIL} t_{WNIH}		10			μs
INTP0 high-/low-level width	t_{WIT0L} t_{WIT0H}		$4t_{CYSMP}$			s
INTP0 to INTP3, CI high-/low-level width	t_{WIT1L} t_{WIT1H}		$4t_{CYCPU}$			s
INTP4, INTP5 high-/low-level width	t_{WIT2L} t_{WIT2H}		10			μs
$\overline{\text{RESET}}$ high-/low-level width[Note]	t_{WRSL} t_{WRSH}		10			μs

Note When the power is turned on or when STOP mode is released by reset, secure the oscillation stabilization wait time while the $\overline{\text{RESET}}$ is at a low-level width.
When the power is turned on, be sure to activate V_{DD} in the $\overline{\text{RESET}}$ = low-level state.

Remark t_{CYSMP}: Sampling clock set by software
t_{CYCPU}: CPU clock set by software in the CPU

Clock Output Operation (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CLKOUT cycle time	t_{CYCL}	nT	79		32000	ns
CLKOUT low-level width	t_{CLL}	$4.5 \le V_{DD} \le 5.5$ V	0.5T–10			ns
			0.5T–20			ns
CLKOUT high-level width	t_{CLH}	$4.5 \le V_{DD} \le 5.5$ V	0.5T–10			ns
			0.5T–20			ns
CLKOUT rise time	t_{CLR}	$4.5 \le V_{DD} \le 5.5$ V			10	ns
		$3.0 \le V_{DD} \le 4.5$ V			20	ns
CLKOUT fall time	t_{CLF}	$4.5 \le V_{DD} \le 5.5$ V			10	ns
		$3.0 \le V_{DD} \le 4.5$ V			20	ns

Remark n: Division ratio of clock output frequency, T: $t_{CYK} = 1/f_{CLK}$ (system clock cycle time)

IEBus Controller Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IEBus system clock frequency	f_s	Mode 1		6.29		MHz

Remark Although the system clock frequency in the IEBus specifications is 6.0 MHz, in the μPD784938A, operation at 6.29 MHz is also guaranteed. Note, however, that operation at 6.0 MHz and 6.29 MHz cannot be used together.

A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = AV_{REF1} = 3.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

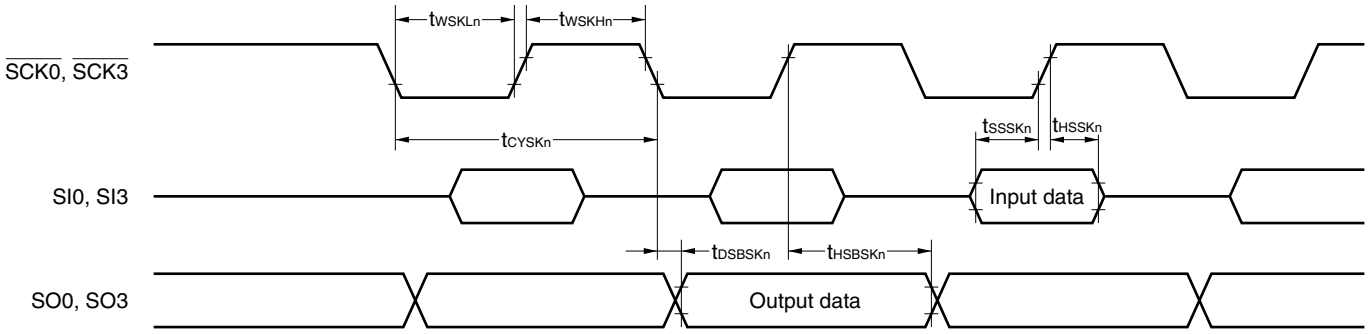
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution				8			bit
Overall error[Note]		IEAD = 00H	6.29 MHz ≤ f_{XX} ≤ 12.58 MHz and other than FR = 1			0.6	%FSR[Note 2]
			6.29 MHz ≤ f_{XX} ≤ 12.58 MHz and FR = 1			1.5	%FSR[Note 2]
		IEAD = 01H	4.5 ≤ V_{DD} ≤ 5.5 V		1	2.2	%FSR[Note 2]
			3.0 ≤ V_{DD} ≤ 5.5 V		1.4	2.6	%FSR[Note 2]
Quantization error						±1/2	LSB
Conversion time	t_{CONV}	FR = 1 : 120 t_{CYK}		9.5		480	μs
		FR = 0 : 240 t_{CYK}		19.1		960	μs
Sampling time	t_{SAMP}	FR = 1 : 18 t_{CYK}		1.4		72	μs
		FR = 0 : 36 t_{CYK}		2.9		144	μs
Analog input voltage	V_{IAN}			AV_{SS}		AV_{REF1}	V
Analog input impedance	R_{AN}				1000		MΩ
Reference voltage	AV_{REF1}			3.0		AV_{DD}	V
AV_{REF1} resistor	R_{AVREF1}			3.0	10		kΩ
AV_{REF1} current	AI_{REF1}				0.5	1.5	mA
AV_{DD} current	AI_{DD1}				2.0	5.0	mA
	AI_{DD2}					20	mA

Notes 1. Excludes quantization error (±1/2 LSB).

2. It is indicated as a ratio (%FSR) to the full-scale value.

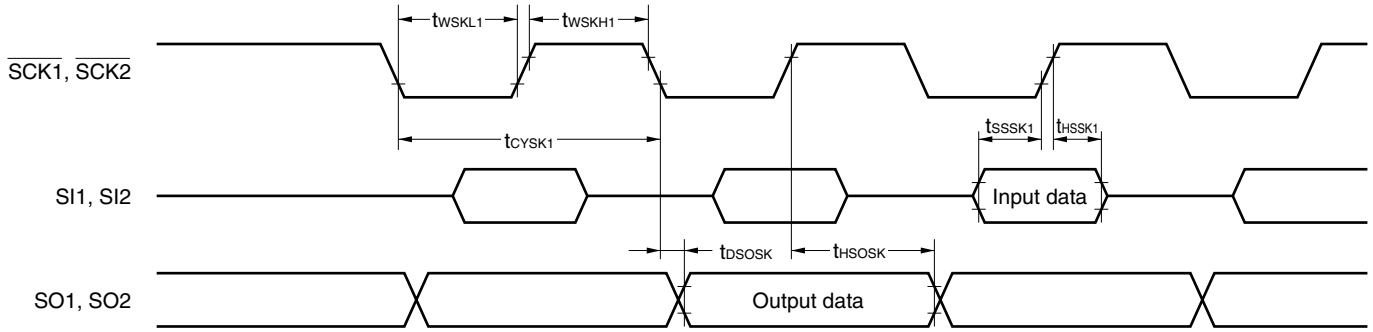
Caution The analog input pins of the μPD784938A function alternately as the port 7 pins (I/O port pins). However when using the A/D converter, it is necessary to set all the pins of port 7 to input mode in order to prevent data from being inverted by the output port operation, thus degrading the A/D conversion accuracy. At this time, pins cannot be used as output ports even though they are not used as A/D analog input port.

Serial Operation (CSI, CSI3)

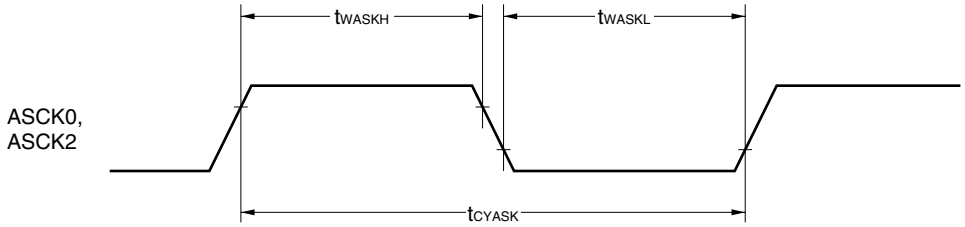


n = 0, 3

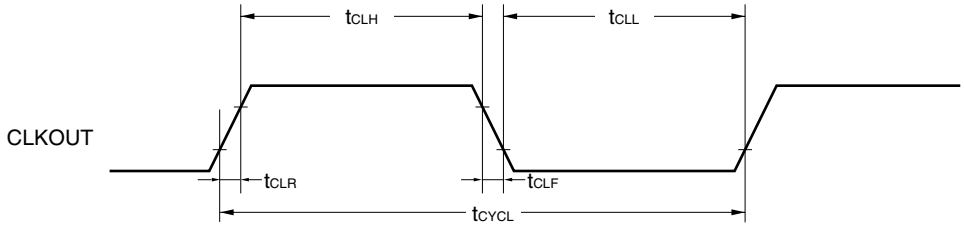
Serial Operation (IOE1, IOE2)



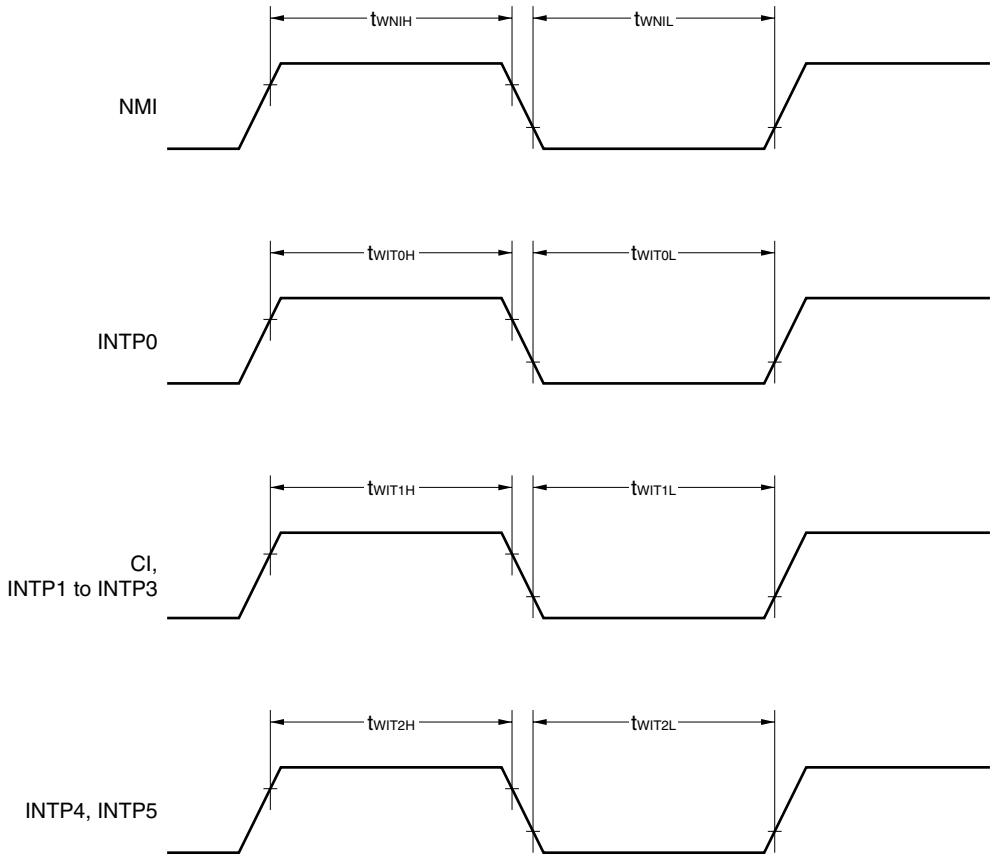
Serial Operation (UART0, UART2)



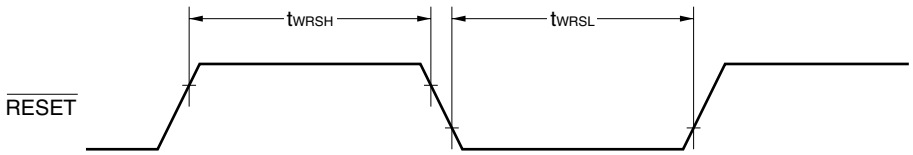
Clock Output Timing



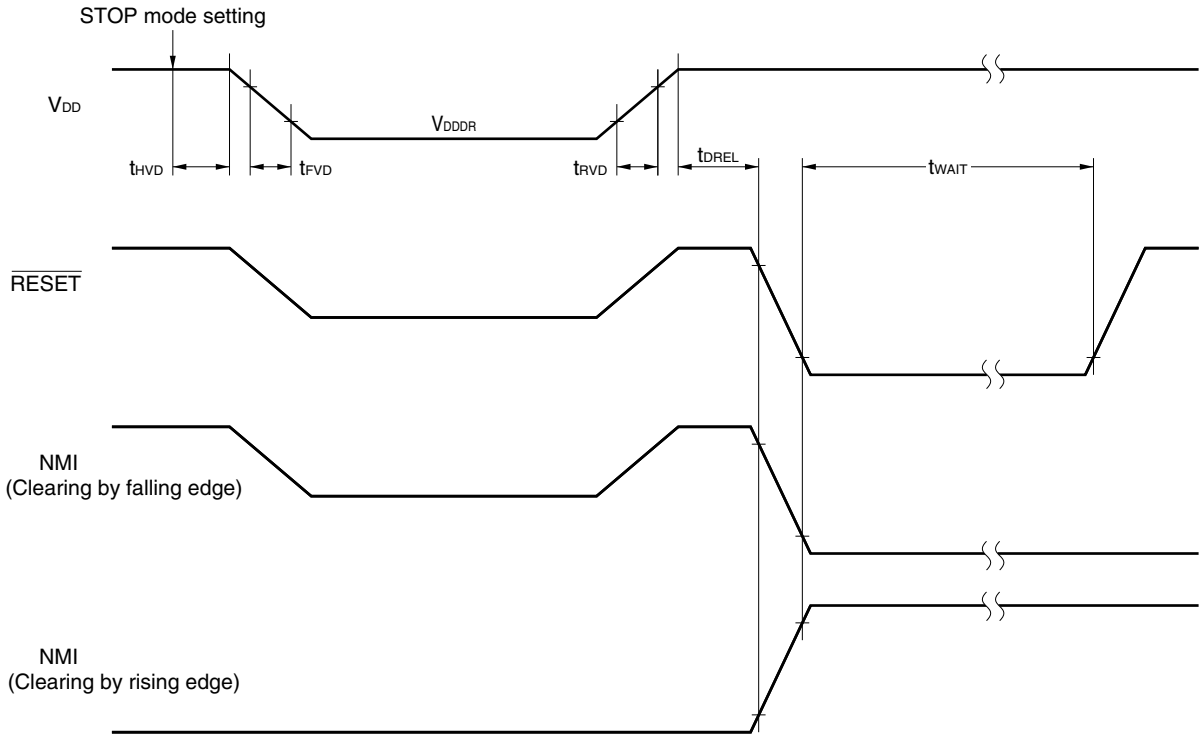
Interrupt Request Input Timing



Reset Input Timing

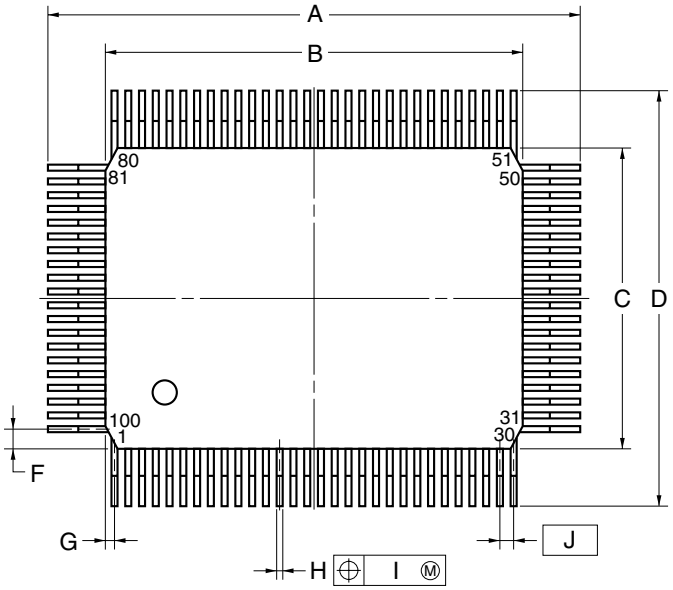


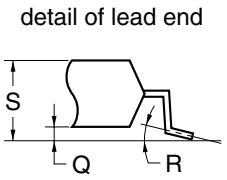
Data Retention Characteristics

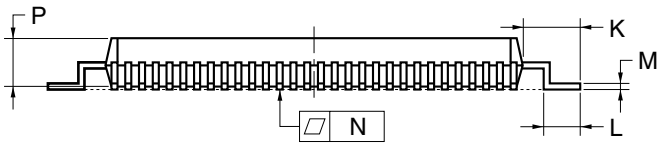


17. PACKAGE DRAWINGS

100PIN PLASTIC QFP (14x20)







NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7±0.1	$0.106^{+0.005}_{-0.004}$
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P100GF-65-3BA1-3

Remark The external dimensions and material of the ES version are the same as those of the mass-produced version.

★ 18. RECOMMENDED SOLDERING CONDITIONS

The μPD784938A should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 18-1. Surface Mounting Type Soldering Conditions

μPD784935AGF-×××-3BA: 100-pin plastic QFP (14 × 20)
μPD784936AGF-×××-3BA: 100-pin plastic QFP (14 × 20)
μPD784937AGF-×××-3BA: 100-pin plastic QFP (14 × 20)
μPD784938AGF-×××-3BA: 100-pin plastic QFP (14 × 20)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher), Count: two times or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher), Count: two times or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C Max., Time: 10 sec. Max., Count: once, Preheating temperature: 120°C Max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C Max., Time: 3 sec. Max. (per pin row)	–

Caution Do not use different soldering methods together (except for partial heating).

★ APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD784938A.
Also refer to **(5) Cautions on using development tools**.

(1) Language processing software

RA78K4	Assembler package common to 78K/IV Series
CC78K4	C compiler package common to 78K/IV Series
DF784937	Device file for μPD784938A Subseries
CC78K4-L	C compiler library source file common to 78K/IV Series

(2) Flash memory writing tools

Flashpro III[Note] (PG-FP III)	Flash programmer for microcontroller with flash memory
FA-100GF	Flash memory writing adapter for 100-pin plastic QFP (GF-3BA type). Wiring must be performed according to the product used.

Note Under development

(3) Debugging tools

- **When IE-78K4-NS in-circuit emulator is used**

IE-78K4-NS	In-circuit emulator common to 78K/IV Series
IE-70000-MC-PS-B	Power supply unit for IE-78K4-NS
IE-70000-98-IF-C	Interface adapter used when PC-9800 series (except notebook type) is used as host machine
IE-70000-CD-IF-C	PC card and cable used when PC-9800 series notebook type PC is used as host machine
IE-70000-PC-IF-C	Interface adapter used when IBM PC/AT™ or compatible is used as host machine
IE-784937-NS-EM1	Emulation board to emulate μPD784938A Subseries
NP-100GF	Emulation probe for 100-pin plastic QFP (GF-3BA type)
EV-9200GF-100	Socket to be mounted on a target system board made for 100-pin plastic QFP (GF-3BA type)
ID78K4-NS	Integrated debugger for IE-78K4-NS
SM78K4	System simulator common to 78K/IV Series
DF784937	Device file for μPD784938A Subseries

- **When IE-784000-R in-circuit emulator is used**

IE-784000-R	In-circuit emulator common to 78K/IV Series
IE-70000-98-IF-B IE-70000-98-IF-C	Interface adapter used when PC-9800 series (except notebook type) is used as host machine
IE-70000-98N-IF	Interface adapter and cable used when PC-9800 series notebook type PC is used as host machine
IE-70000-PC-IF-B IE-70000-PC-IF-C	Interface adapter used when IBM PC/AT or compatible is used as host machine
IE-78000-R-SV3	Interface adapter and cable used when EWS is used as host machine
IE-784937-NS-EM1	Emulation board to emulate μPD784938A Subseries
IE-784000-R-EM	Emulation board common to 78K/IV Series
IE-78K4-R-EX2	Emulation probe conversion board necessary when using IE-784937-NS-EM1 on IE-784000-R. Not necessary when using IE-784937-R-EM1
EP-78064GF-R	Emulation probe for 100-pin plastic QFP (GF-3BA type)
EV-9200GF-100	Socket to be mounted on a target system board made for 100-pin plastic QFP (GF-3BA type)
ID78K4	Integrated debugger for IE-784000-R
SM78K4	System simulator common to 78K/IV Series
DF784937	Device file for μPD784938A Subseries

(4) Real-time OS

RX78K/IV	Real-time OS for 78K/IV Series
MX78K4	OS for 78K/IV Series

(5) Cautions on using development tools

- The ID78K4-NS, ID78K4, and SM78K4 are used in combination with the DF784937.
- The CC78K4 and RX78K/IV are used in combination with the RA78K4 or DF784937.
- The Flashpro III, FA-100GF, and NP-100GF are products made by Naito Densei Machida Mfg. Co, Ltd (TEL +81-44-822-3813).
- The host machine and OS suitable for each software are as follows:

Host Machine [OS] / Software	PC	EWS
	PC-9800 series [Windows] IBM PC/AT and compatibles [Japanese/English Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K4	√ Note	√
CC78K4	√ Note	√
ID78K4-NS	√	—
ID78K4	√	√
SM78K4	√	—
RX78K/IV	√ Note	√
MX78K4	√ Note	√

Note DOS-based software

APPENDIX B. RELATED DOCUMENTS

- **Documents related to devices**

Document Name	Document Number
μPD784935A, 784936A, 784937A, 784938A Data Sheet	This document
μPD78F4937 Preliminary Product Information	U13573E
μPD784938A Subseries User's Manual - Hardware	U13987E
78K/IV Series User's Manual - Instructions	U10905E
78K/IV Series Application Note - Software basics	U10095E

- **Documents related to development tools (user's manuals)**

Document Name		Document Number
RA78K4 Assembler Package	Language	U11162E
	Operation	U11334E
RA78K4 Structured Assembler Preprocessor		U11743E
CC78K4 C Compiler	Language	U11571E
	Operation	U11572E
IE-78K4-NS		U13556E
IE-784000-R		U12903E
IE-784937-R-EM1		Planned
IE-784937-NS-EM1		Planned
EP-78064		EEU-1469
SM78K4 System Simulator - Windows Based	Reference	U10093E
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092E
ID78K4-NS Integrated Debugger	Reference	U12796E
ID78K4 Integrated Debugger - Windows Based	Reference	U10440E
ID78K4 Integrated Debugger - HP-UX, SunOS, NEWS-OS Based	Reference	U11960E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

- **Documents related to embedded software (user's manuals)**

Document Name		Document Number
78K/IV Series Real-Time OS	Fundamental	U10603E
	Installation	U10604E

- **Other documents**

Document Name	Document Number
★ SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	U10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
United Square, Singapore
Tel: 65-253-8311
Fax: 65-250-3583

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