

16/8-BIT SINGLE-CHIP MICROCONTROLLERS

The μ PD784216Y is based on the μ PD784216 with an I²C bus control function added, and is ideal for audio visual applications.

A flash memory version, the μ PD78F4216Y, which can operate in the same voltage range as the mask ROM version, and various development tools are under development.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μ PD784216, 784216Y Subseries User's Manual Hardware: U12015E

78K/IV Series User's Manual Instructions: U10905E

FEATURES

- 78K/IV Series
- Inherits peripheral functions of μ PD78078Y Subseries
- Pin-compatible with μ PD784216 Subseries
- Minimum instruction execution time
 - 160 ns
 - (@ $f_{XX} = 12.5$ -MHz operation with main system clock)
 - 61 μ s
 - (@ $f_{XT} = 32.768$ -kHz operation with subsystem clock)
- I/O port: 86 pins
- Timer/counter: 16-bit timer/counter \times 1 unit
8-bit timer/counter \times 6 units
- Serial interface: 3 channels
 - UART/IOE (3-wire serial I/O): 2 channels
 - CSI (3-wire serial I/O, multi-master I²C bus supported)
 - : 1 channel
- Standby function
 - HALT/STOP/IDLE mode
 - In power-saving mode: HALT/IDLE mode (with subsystem clock)
- Clock division function
- Watch timer: 1 channel
- Watchdog timer: 1 channel
- Clock output function
 - Selectable from f_{XX} , $f_{XX}/2$, $f_{XX}/2^2$, $f_{XX}/2^3$, $f_{XX}/2^4$, $f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$, f_{XT}
- Buzzer output function
 - Selectable from $f_{XX}/2^{10}$, $f_{XX}/2^{11}$, $f_{XX}/2^{12}$, $f_{XX}/2^{13}$
- A/D converter: 8-bit resolution \times 8 channels
- D/A converter: 8-bit resolution \times 2 channels
- ★ • Supply voltage: $V_{DD} = 2.2$ to 5.5 V

APPLICATIONS

Cellular phones, PHS, cordless telephones, CD-ROM, AV equipment

Unless otherwise specified, references in this document to the μ PD784216Y refer to the μ PD784214Y, μ PD784215Y, and μ PD784216Y.

The information in this document is subject to change without notice.

The mark ★ shows major revised points.

ORDERING INFORMATION

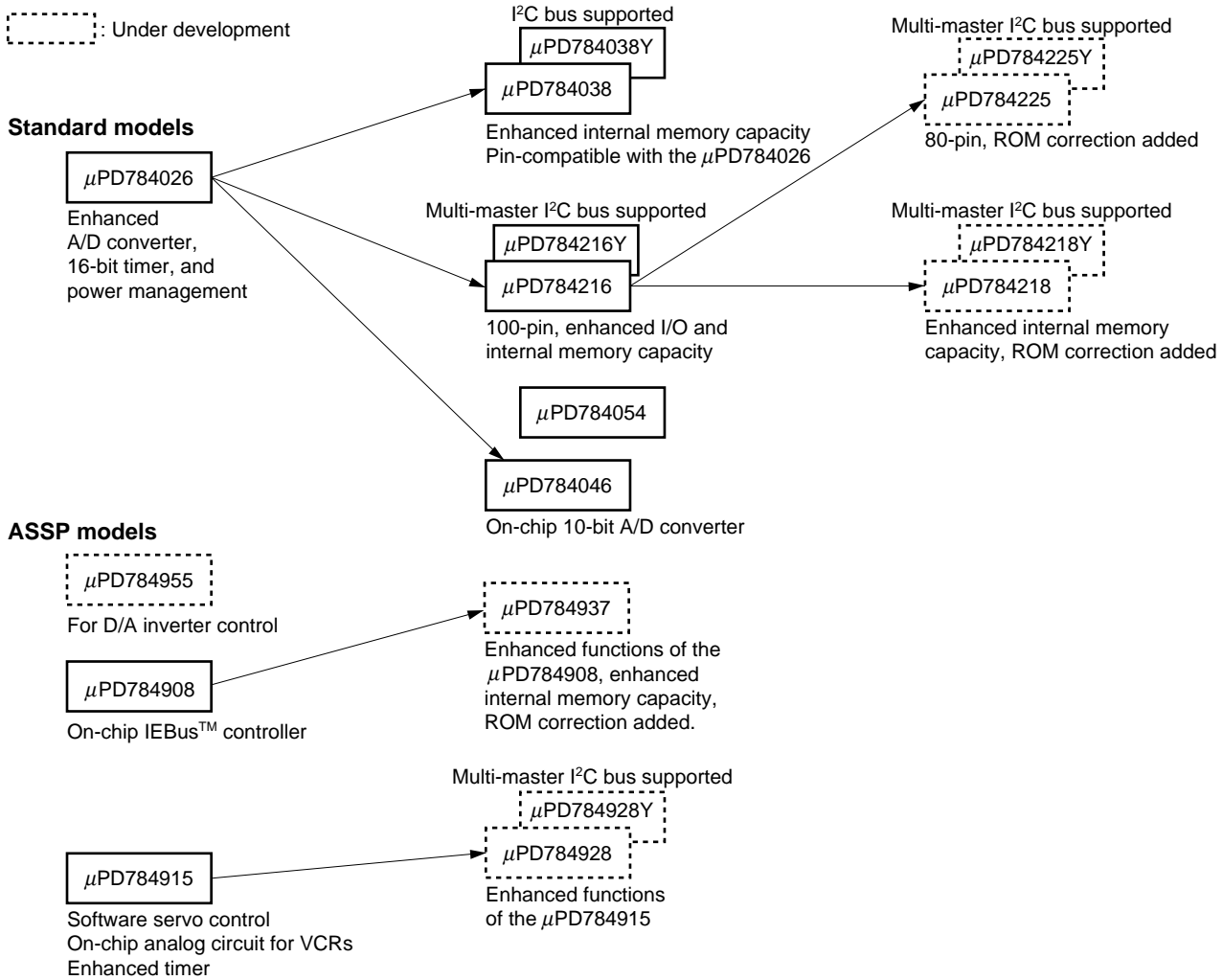
| | Part Number | Package | Internal ROM (bytes) | Internal RAM (bytes) |
|---|----------------------|--|----------------------|----------------------|
| ★ | μPD784214YGC-xxx-8EU | 100-pin plastic LQFP (fine pitch) (14 × 14 mm) | 96 K | 3584 |
| | μPD784214YGF-xxx-3BA | 100-pin plastic QFP (14 × 20 mm) | 96 K | 3584 |
| ★ | μPD784215YGC-xxx-8EU | 100-pin plastic LQFP (fine pitch) (14 × 14 mm) | 128 K | 5120 |
| | μPD784215YGF-xxx-3BA | 100-pin plastic QFP (14 × 20 mm) | 128 K | 5120 |
| ★ | μPD784216YGC-xxx-8EU | 100-pin plastic LQFP (fine pitch) (14 × 14 mm) | 128 K | 8192 |
| | μPD784216YGF-xxx-3BA | 100-pin plastic QFP (14 × 20 mm) | 128 K | 8192 |

Remark xxx indicates ROM code suffix.

★ **78K/IV SERIES LINEUP**

: Under mass production

: Under development



FUNCTIONS (1/2)

| Part Number | | μPD784214Y | μPD784215Y | μPD784216Y |
|---|----------------------------|---|--|--|
| Item | | | | |
| Number of basic instructions (mnemonics) | | 113 | | |
| General-purpose register | | 8 bits × 16 registers × 8 banks, or 16 bits × 8 registers × 8 banks (memory mapping) | | |
| Minimum instruction execution time | | <ul style="list-style-type: none"> • 160 ns/320 ns/640 ns/1280 ns/2560 ns (@ f_{xx} = 12.5-MHz operation with main system clock) • 61 μs (@ f_{XT} = 32.768-kHz operation with subsystem clock) | | |
| Internal memory | ROM | 96 Kbytes | 128 Kbytes | |
| | RAM | 3584 bytes | 5120 bytes | 8192 bytes |
| Memory space | | 1 Mbytes with program and data spaces combined | | |
| I/O port | Total | 86 | | |
| | CMOS input | 8 | | |
| | CMOS I/O | 72 | | |
| | N-ch open-drain I/O | 6 | | |
| Pins with ancillary functions <small>Note</small> | Pins with pull-up resistor | 70 | | |
| | LED direct drive output | 22 | | |
| | Middle-voltage pin | 6 | | |
| Real-time output port | | 4 bits × 2, or 8 bits × 1 | | |
| Timer/counter | | Timer/counter: (16-bit) | Timer register × 1 Capture/compare register × 2 | Pulse output <ul style="list-style-type: none"> • PPG output • Square wave output • One-shot pulse output |
| | | Timer/counter 1: (8-bit) | Timer register × 1 Compare register × 1 | Pulse output <ul style="list-style-type: none"> • PWM output • Square wave output |
| | | Timer/counter 2: (8-bit) | Timer register × 1 Compare register × 1 | Pulse output <ul style="list-style-type: none"> • PWM output • Square wave output |
| | | Timer/counter 5: (8-bit) | Timer register × 1 Compare register × 1 | Pulse output <ul style="list-style-type: none"> • PWM output • Square wave output |
| | | Timer/counter 6: (8-bit) | Timer register × 1 Compare register × 1 | Pulse output <ul style="list-style-type: none"> • PWM output • Square wave output |
| | | Timer/counter 7: (8-bit) | Timer register × 1 Compare register × 1 | Pulse output <ul style="list-style-type: none"> • PWM output • Square wave output |
| | | Timer/counter 8: (8-bit) | Timer register × 1 Compare register × 1 | Pulse output <ul style="list-style-type: none"> • PWM output • Square wave output |
| Serial interface | | <ul style="list-style-type: none"> • UART/IOE (3-wire serial I/O): 2 channels (on-chip baud rate generator) • CSI (3-wire serial I/O, multi-master I²C bus supported): 1 channel | | |
| A/D converter | | 8-bit resolution × 8 channels | | |
| D/A converter | | 8-bit resolution × 2 channels | | |

Note The pins with ancillary functions are included in the I/O pins.

FUNCTIONS (2/2)

| Part Number | | μPD784214Y | μPD784215Y | μPD784216Y |
|------------------|-----------------|---|------------|------------|
| Clock output | | Selectable from f_{xx} , $f_{xx}/2$, $f_{xx}/2^2$, $f_{xx}/2^3$, $f_{xx}/2^4$, $f_{xx}/2^5$, $f_{xx}/2^6$, $f_{xx}/2^7$, f_{XT} | | |
| Buzzer output | | Selectable from $f_{xx}/2^{10}$, $f_{xx}/2^{11}$, $f_{xx}/2^{12}$, $f_{xx}/2^{13}$ | | |
| Watch timer | | 1 channel | | |
| Watchdog timer | | 1 channel | | |
| Standby | | <ul style="list-style-type: none"> • HALT/STOP/IDLE modes • In low-power consumption mode (with subsystem clock): HALT/IDLE mode | | |
| Interrupt | Hardware source | 29 (internal: 20, external: 9) | | |
| | Software source | BRK instruction, BRKCS instruction, operand error | | |
| | Non-maskable | Internal: 1, external: 1 | | |
| | Maskable | Internal: 19, external: 8 | | |
| | | <ul style="list-style-type: none"> • 4 programmable priority levels • 3 service modes: vectored interrupt/macro service/context switching | | |
| ★ Supply voltage | | $V_{DD} = 2.2$ to 5.5 V | | |
| ★ Package | | 100-pin plastic LQFP (fine pitch) (14 × 14 mm) 100-pin plastic QFP (14 × 20 mm) | | |

CONTENTS

| | |
|--|-----------|
| 1. DIFFERENCES AMONG MODELS IN μPD784216Y SUBSERIES..... | 7 |
| 2. MAJOR DIFFERENCES FROM μPD78078Y SUBSERIES | 8 |
| 3. PIN CONFIGURATION (Top View) | 9 |
| 4. BLOCK DIAGRAM | 12 |
| 5. PIN FUNCTION | 13 |
| 5.1 Port Pins..... | 13 |
| 5.2 Non-port Pins | 15 |
| 5.3 Pin I/O Circuits and Recommended Connections of Unused Pins | 17 |
| 6. CPU ARCHITECTURE | 20 |
| 6.1 Memory Space | 20 |
| 6.2 CPU Registers | 24 |
| 6.2.1 General-purpose registers | 24 |
| 6.2.2 Control registers | 25 |
| 6.2.3 Special function registers (SFRs) | 26 |
| 7. PERIPHERAL HARDWARE FUNCTIONS | 31 |
| 7.1 Ports..... | 31 |
| 7.2 Clock Generation Circuit | 32 |
| 7.3 Real-Time Output Port..... | 34 |
| 7.4 Timer/Counter | 35 |
| 7.5 A/D Converter | 37 |
| 7.6 D/A Converter | 38 |
| 7.7 Serial Interface | 39 |
| 7.7.1 Asynchronous serial interface/3-wire serial I/O (UART/IOE) | 40 |
| 7.7.2 Clocked serial interface (CSI) | 42 |
| 7.8 Clock Output Function | 43 |
| 7.9 Buzzer Output Function | 44 |
| 7.10 Edge Detection Function | 44 |
| 7.11 Watch Timer | 44 |
| 7.12 Watchdog Timer | 45 |
| 8. INTERRUPT FUNCTION..... | 46 |
| 8.1 Interrupt Sources | 46 |
| 8.2 Vectored Interrupt | 48 |
| 8.3 Context Switching..... | 49 |
| 8.4 Macro Service | 49 |
| 8.5 Application Example of Macro Service..... | 50 |

9. LOCAL BUS INTERFACE 51
 9.1 Memory Expansion 52
 9.2 Programmable Wait 52

10. STANDBY FUNCTION 53

11. RESET FUNCTION 55

12. INSTRUCTION SET 56

★ 13. ELECTRICAL SPECIFICATIONS..... 61

14. PACKAGE DRAWINGS 80

★ 15. RECOMMENDED SOLDERING CONDITIONS 82

APPENDIX A DEVELOPMENT TOOLS 83

APPENDIX B. RELATED DOCUMENTS 86

1. DIFFERENCES AMONG MODELS IN μPD784216Y SUBSERIES

The only difference among the μPD784214Y, 784215Y, and 784216Y lies in the internal memory capacity.

The μPD78F4216Y is provided with a 128-Kbyte flash memory instead of the mask ROM of the above models. These differences are summarized in Table 1-1.

★

Table 1-1. Differences among Models in μPD784216Y Subseries

| Part Number Item | μPD784214Y | μPD784215Y | μPD784216Y | μPD78F4216Y |
|---|--|--------------------------|------------|--------------------------------|
| Internal ROM | 96 Kbytes (mask ROM) | 128 Kbytes (mask ROM) | | 128 Kbytes (Flash memory) |
| Internal RAM | 3584 bytes | 5120 bytes | 8192 bytes | |
| Internal memory size switching register (IMS) | None | | | Provided Note |
| Supply voltage | V _{DD} = 2.2 to 5.5 V | | | V _{DD} = 2.7 to 5.5 V |
| Electrical specifications | Refer to the Data Sheet for each device. | | | |
| Recommended soldering conditions | | | | |
| TEST pin | Provided | | | None |
| V _{PP} pin | None | | | Provided |

Note Internal flash memory capacity and internal RAM capacity can be changed using the internal memory size switching register (IMS).

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations on the commercial samples (not engineering samples) of the mask ROM version.

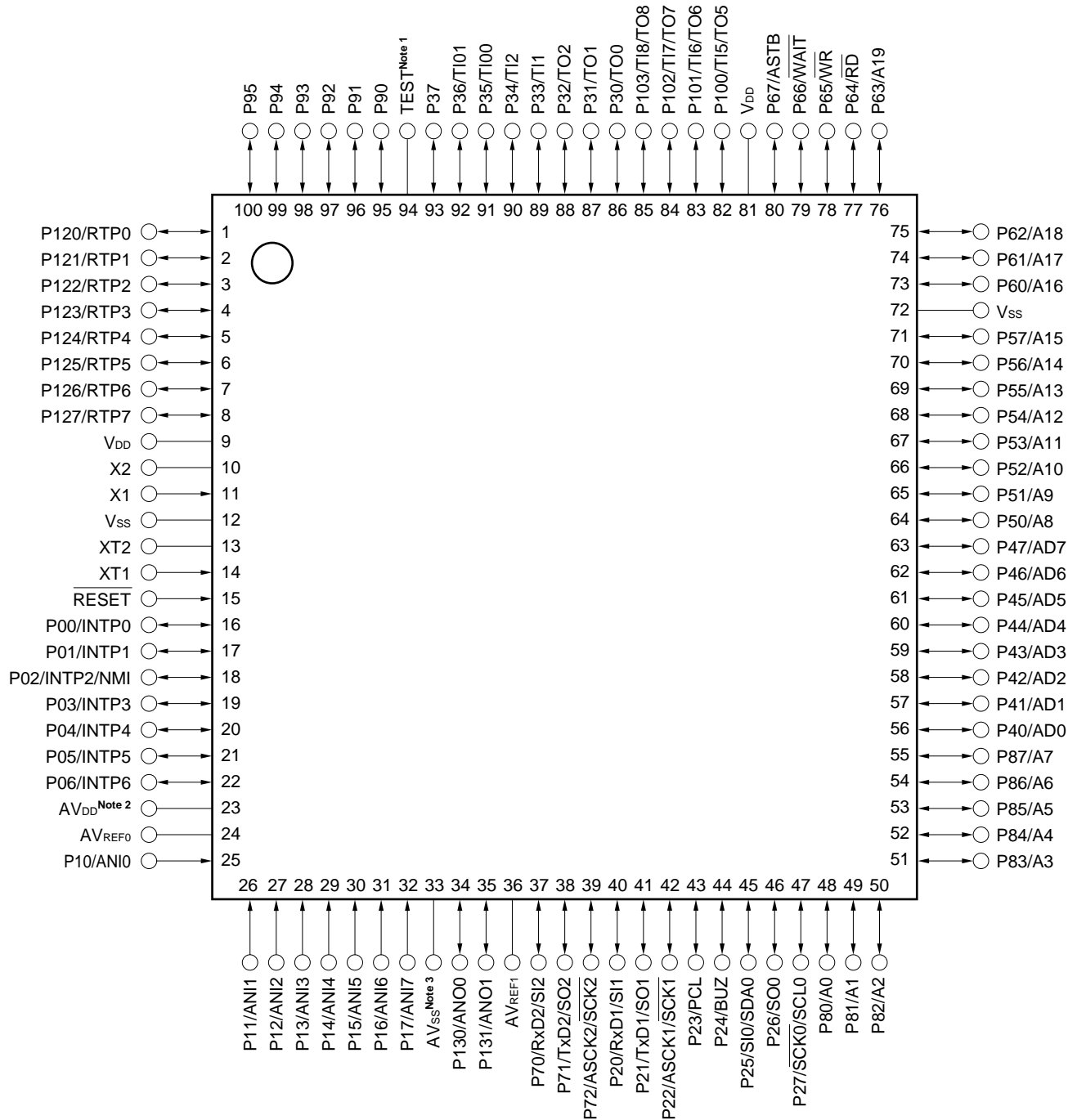
2. MAJOR DIFFERENCES FROM μPD78078Y SUBSERIES

| Series Name | | μPD784216Y Subseries | μPD78078Y Subseries |
|---|----------------------------|---|---|
| Item | | | |
| CPU | | 16-bit CPU | 8-bit CPU |
| Minimum instruction execution time | With main system clock | 160 ns (@ 12.5-MHz operation) | 400 ns (@ 5.0-MHz operation) |
| | With subsystem clock | 61 μs (@ 32.768-kHz operation) | 122 μs (@ 32.768-kHz operation) |
| Memory space | | 1 Mbytes | 64 Kbytes |
| I/O port | Total | 86 | 88 |
| | CMOS input | 8 | 2 |
| | CMOS I/O | 72 | 78 |
| | N-ch open-drain I/O | 6 | 8 |
| Pins with ancillary functions Note | Pins with pull-up resistor | 70 | 86 |
| | LED direct drive output | 22 | 16 |
| | Middle-voltage pin | 6 | 8 |
| Timer/counter | | <ul style="list-style-type: none"> • 16-bit timer/counter × 1 unit • 8-bit timer/counter × 6 units | <ul style="list-style-type: none"> • 16-bit timer/counter × 1 unit • 8-bit timer/counter × 4 units |
| Serial interface | | <ul style="list-style-type: none"> • UART/IOE (3-wire serial I/O) × 2 channels • CSI (3-wire serial I/O, multi-master I²C bus supported) × 1 channel | <ul style="list-style-type: none"> • UART/IOE (3-wire serial I/O) × 1 channel • CSI (3-wire serial I/O, 2-wire serial I/O, I²C bus) × 1 channel • CSI (3-wire serial I/O, 3-wire serial I/O with automatic transmit/receive function) × 1 channel |
| Interrupt | NMI pin | Provided | None |
| | Macro service | Provided | None |
| | Context switching | Provided | None |
| | Programmable priority | 4 levels | None |
| ★ Standby function | | HALT/STOP/IDLE modes In low-power consumption mode: HALT/IDLE modes | HALT/STOP modes |
| ★ Package | | <ul style="list-style-type: none"> • 100-pin plastic LQFP (fine pitch) (14 × 14 mm) • 100-pin plastic QFP (14 × 20 mm) | <ul style="list-style-type: none"> • 100-pin plastic LQFP (fine pitch) (14 × 14 mm) • 100-pin plastic QFP (14 × 20 mm) • 100-pin ceramic WQFN (14 × 20 mm) (μPD78P078Y only) |

Note The pins with ancillary functions are included in the I/O pins.

3. PIN CONFIGURATION (Top View)

- ★ • 100-pin plastic LQFP (fine pitch) (14 × 14 mm)
- μPD784214YGC-xxx-8EU
- μPD784215YGC-xxx-8EU
- μPD784216YGC-xxx-8EU



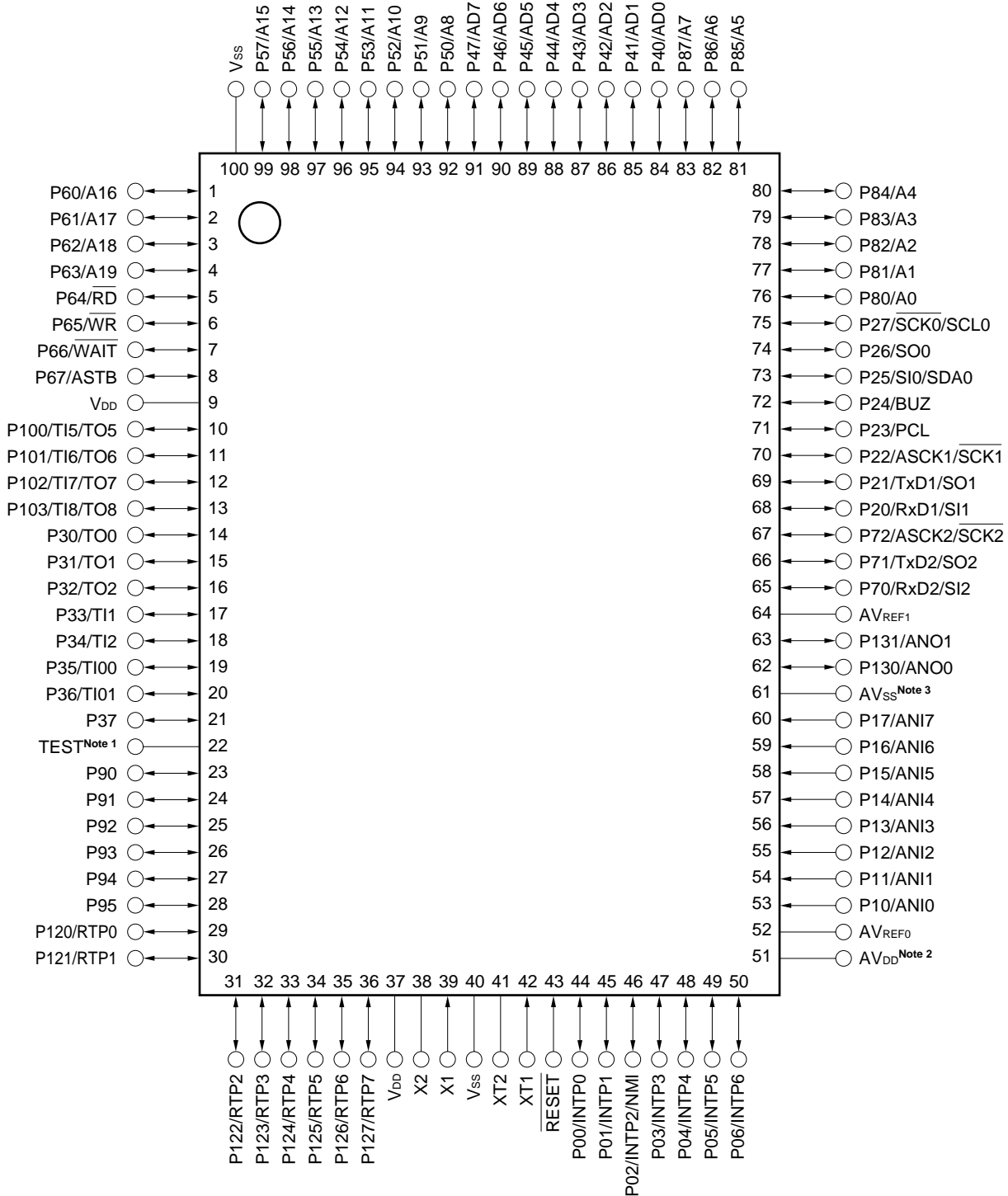
- Notes**
1. Connect the TEST pin directly to Vss.
 2. Connect the AV_{DD} pin to V_{DD}.
 3. Connect the AV_{SS} pin to Vss.

• 100-pin plastic QFP (14 × 20 mm)

μPD784214YGF-xxx-3BA

μPD784215YGF-xxx-3BA

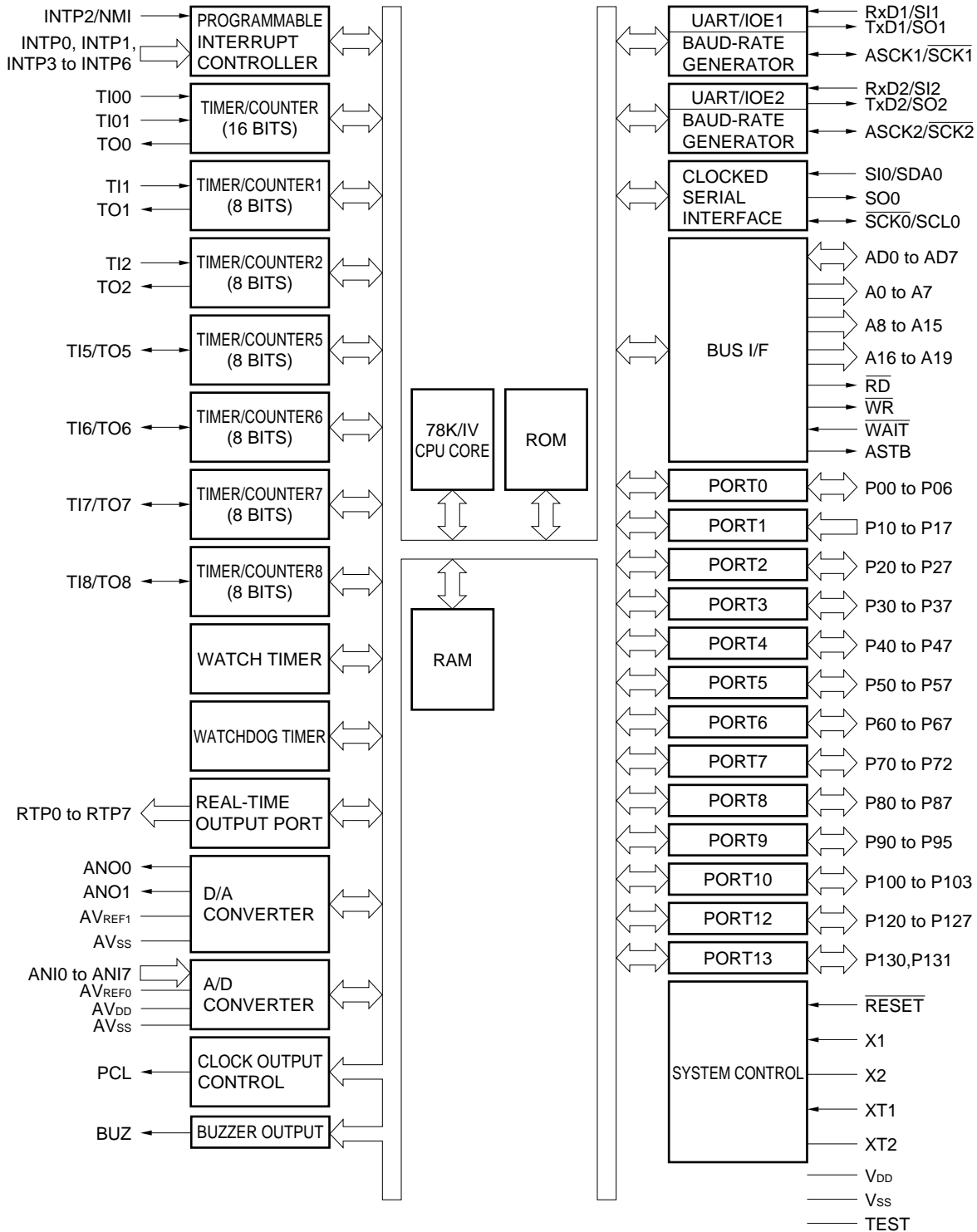
μPD784216YGF-xxx-3BA



- Notes**
1. Connect the TEST pin directly to V_{SS}.
 2. Connect the AV_{DD} pin to V_{DD}.
 3. Connect the AV_{SS} pin to V_{SS}.

| | | | |
|-----------------|----------------------------|--|-----------------------------|
| A0 to A19: | Address Bus | P130, P131: | Port13 |
| AD0 to AD7: | Address/Data Bus | PCL: | Programmable Clock |
| ANI0 to ANI7: | Analog Input | \overline{RD} : | Read Strobe |
| ANO0, ANO1: | Analog Output | \overline{RESET} : | Reset |
| ASCK1, ASCK2: | Asynchronous Serial Clock | RTP0 to RTP7: | Real-time Output Port |
| ASTB: | Address Strobe | RxD1, RxD2: | Receive Data |
| AVDD: | Analog Power Supply | $\overline{SCK0}$ to $\overline{SCK2}$: | Serial Clock |
| AVREF0, AVREF1: | Analog Reference Voltage | SCL0: | Serial Clock |
| AVSS: | Analog Ground | SDA0: | Serial Data |
| BUZ: | Buzzer Clock | SI0 to SI2: | Serial Input |
| INTP0 to INTP6: | Interrupt from Peripherals | SO0 to SO2: | Serial Output |
| NMI: | Non-maskable Interrupt | TEST: | Test |
| P00 to P06: | Port0 | TI00, TI01, | |
| P10 to P17: | Port1 | TI1, TI2, TI5 to TI8: | Timer Input |
| P20 to P27: | Port2 | TO0 to TO2, TO5 to TO8: | Timer Output |
| P30 to P37: | Port3 | TxD1, TxD2: | Transmit Data |
| P40 to P47: | Port4 | VDD: | Power Supply |
| P50 to P57: | Port5 | VSS: | Ground |
| P60 to P67: | Port6 | \overline{WAIT} : | Wait |
| P70 to P72: | Port7 | \overline{WR} : | Write Strobe |
| P80 to P87: | Port8 | X1, X2: | Crystal (Main System Clock) |
| P90 to P95: | Port9 | XT1, XT2: | Crystal (Subsystem Clock) |
| P100 to P103: | Port10 | | |
| P120 to P127: | Port12 | | |

4. BLOCK DIAGRAM



Remark The internal ROM and RAM capacities differ depending on the product.

5. PIN FUNCTION

5.1 Port Pins (1/2)

| Pin Name | I/O | Alternate Function | Function |
|------------|-------|--------------------|---|
| P00 | I/O | INTP0 | Port 0 (P0): <ul style="list-style-type: none"> • 7-bit I/O port • Input/output can be specified in 1-bit units. • Whether specifying input mode or output mode, an on-chip pull-up resistor can be specified in 1-bit units by means of software. |
| P01 | | INTP1 | |
| P02 | | INTP2/NMI | |
| P03 | | INTP3 | |
| P04 | | INTP4 | |
| P05 | | INTP5 | |
| P06 | | INTP6 | |
| P10 to P17 | Input | ANI0 to ANI7 | Port 1 (P1): <ul style="list-style-type: none"> • 8-bit input port |
| P20 | I/O | RxD1/SI1 | Port 2 (P2): <ul style="list-style-type: none"> • 8-bit I/O port • Input/output can be specified in 1-bit units. • Whether specifying input mode or output mode, an on-chip pull-up resistor can be specified in 1-bit units by means of software. |
| P21 | | TxD1/SO1 | |
| P22 | | ASCK1/SCK1 | |
| P23 | | PCL | |
| P24 | | BUZ | |
| P25 | | SI0/SDA0 | |
| P26 | | SO0 | |
| P27 | | SCK0/SCL0 | |
| P30 | I/O | TO0 | Port 3 (P3): <ul style="list-style-type: none"> • 8-bit I/O port • Input/output can be specified in 1-bit units. • Whether specifying input mode or output mode, an on-chip pull-up resistor can be specified in 1-bit units by means of software. |
| P31 | | TO1 | |
| P32 | | TO2 | |
| P33 | | TI1 | |
| P34 | | TI2 | |
| P35 | | TI00 | |
| P36 | | TI01 | |
| P37 | | — | |
| P40 to P47 | I/O | AD0 to AD7 | Port 4 (P4): <ul style="list-style-type: none"> • 8-bit I/O port • Input/output can be specified in 1-bit units. • All pins set in input mode can be connected to on-chip pull-up resistors by means of software. • Can drive LEDs. |
| P50 to P57 | I/O | A8 to A15 | Port 5 (P5): <ul style="list-style-type: none"> • 8-bit I/O port • Input/output can be specified in 1-bit units. • All pins set in input mode can be connected to on-chip pull-up resistors by means of software. • Can drive LEDs. |

5.1 Port Pins (2/2)

| Pin Name | I/O | Alternate Function | Function |
|----------------|-----|--------------------------|---|
| P60 | I/O | A16 | Port 6 (P6): <ul style="list-style-type: none"> • 8-bit I/O port • Input/output can be specified in 1-bit units. • All pins set in input mode can be connected to on-chip pull-up resistors by means of software. |
| P61 | | A17 | |
| P62 | | A18 | |
| P63 | | A19 | |
| P64 | | \overline{RD} | |
| P65 | | \overline{WR} | |
| P66 | | \overline{WAIT} | |
| P67 | | ASTB | |
| P70 | I/O | RxD2/SI2 | Port 7 (P7): <ul style="list-style-type: none"> • 3-bit I/O port • Input/output can be specified in 1-bit units. • Whether specifying input mode or output mode, an on-chip pull-up resistor can be specified in 1-bit units by means of software. |
| ★ P71 | | TxD2/SO2 | |
| P72 | | ASCK2/ $\overline{SCK2}$ | |
| ★ P80 to P87 | I/O | A0 to A7 | Port 8 (P8): <ul style="list-style-type: none"> • 8-bit I/O port • Input/output can be specified in 1-bit units. • Whether specifying input mode or output mode, an on-chip pull-up resistor can be specified in 1-bit units by means of software. • Interrupt control flag (KRIF) is set to 1 when falling edge is detected at a pin of this port. |
| P90 to P95 | I/O | — | Port 9 (P9): <ul style="list-style-type: none"> • N-ch open-drain middle-voltage I/O port • 6-bit I/O port • Input/output can be specified in 1-bit units. • Can directly drive LEDs. |
| P100 | I/O | TI5/TO5 | Port 10 (P10): <ul style="list-style-type: none"> • 4-bit I/O port • Input/output can be specified in 1-bit units. • Whether specifying input mode or output mode, an on-chip pull-up resistor can be specified in 1-bit units by means of software. |
| ★ P101 | | TI6/TO6 | |
| P102 | | TI7/TO7 | |
| P103 | | TI8/TO8 | |
| ★ P120 to P127 | I/O | RTP0 to RTP7 | Port 12 (P12): <ul style="list-style-type: none"> • 8-bit I/O port • Input/output can be specified in 1-bit units. • Whether specifying input mode or output mode, an on-chip pull-up resistor can be specified in 1-bit units by means of software. |
| P130, P131 | I/O | ANO0, ANO1 | Port 13 (P13): <ul style="list-style-type: none"> • 2-bit I/O port • Input/output can be specified in 1-bit units. |

5.2 Non-port Pins (1/2)

| Pin Name | I/O | Alternate Function | Function |
|--------------------------|--------|-------------------------------|---|
| TI00 | Input | P35 | External count clock input to 16-bit timer register |
| TI01 | | P36 | Capture trigger signal input to capture/compare register 00 |
| TI1 | | P33 | External count clock input to 8-bit timer register 1 |
| TI2 | | P34 | External count clock input to 8-bit timer register 2 |
| TI5 | | P100/TO5 | External count clock input to 8-bit timer register 5 |
| TI6 | | P101/TO6 | External count clock input to 8-bit timer register 6 |
| TI7 | | P102/TO7 | External count clock input to 8-bit timer register 7 |
| TI8 | | P103/TO8 | External count clock input to 8-bit timer register 8 |
| TO0 | Output | P30 | 16-bit timer output (shared by 14-bit PWM output) |
| TO1 | | P31 | 8-bit timer output (shared by 8-bit PWM output) |
| TO2 | | P32 | |
| TO5 | | P100/TO5 | |
| TO6 | | P101/TO6 | |
| TO7 | | P102/TO7 | |
| TO8 | | P103/TO8 | |
| RxD1 | Input | P20/SI1 | Serial data input (UART1) |
| RxD2 | | P70/SI2 | Serial data input (UART2) |
| TxD1 | Output | P21/SO1 | Serial data output (UART1) |
| TxD2 | | P71/SO2 | Serial data output (UART2) |
| ASCK1 | Input | P22/ $\overline{\text{SCK1}}$ | Baud rate clock input (UART1) |
| ASCK2 | | P72/ $\overline{\text{SCK2}}$ | Baud rate clock input (UART2) |
| SI0 | Input | P25/SDA0 | Serial data input (3-wire serial clock I/O0) |
| SI1 | | P20/RxD1 | Serial data input (3-wire serial clock I/O1) |
| SI2 | | P70/RxD2 | Serial data input (3-wire serial clock I/O2) |
| SO0 | Output | P26 | Serial data output (3-wire serial I/O0) |
| SO1 | | P21/TxD1 | Serial data output (3-wire serial I/O1) |
| SO2 | | P71/TxD2 | Serial data output (3-wire serial I/O2) |
| SDA0 | I/O | P25/SI0 | Serial data input/output (I ² C bus) |
| $\overline{\text{SCK0}}$ | I/O | P27 | Serial clock input/output (3-wire serial I/O0) |
| $\overline{\text{SCK1}}$ | | P22/ASCK1 | Serial clock input/output (3-wire serial I/O1) |
| $\overline{\text{SCK2}}$ | | P72/ASCK2 | Serial clock input/output (3-wire serial I/O2) |
| SCL0 | | P27/ $\overline{\text{SCK0}}$ | Serial data input/output (I ² C bus) |
| NMI | Input | P02/INTP2 | Non-maskable interrupt request input |
| INTP0 | | P00 | External interrupt request input |
| INTP1 | | P01 | |
| INTP2 | | P02/NMI | |
| INTP3 | | P03 | |
| INTP4 | | P04 | |
| INTP5 | | P05 | |
| INTP6 | P06 | | |

5.2 Non-port Pins (2/2)

| Pin Name | I/O | Alternate Function | Function |
|---------------------------|--------|--------------------|--|
| PCL | Output | P23 | Clock output (for trimming main system clock and subsystem clock) |
| BUZ | Output | P24 | Buzzer output |
| RTP0 to RTP7 | Output | P120 to P127 | Real-time output port that outputs data in synchronization with trigger |
| AD0 to AD7 | I/O | P40 to P47 | Lower address/data bus for expanding memory externally |
| A0 to A7 | Output | P80 to P87 | Lower address bus for expanding memory externally |
| A8 to A15 | | P50 to P57 | Middle address bus for expanding memory externally |
| A16 to A19 | | P60 to P63 | Higher address bus for expanding memory externally |
| $\overline{\text{RD}}$ | Output | P64 | Strobe signal output for read operation of external memory |
| $\overline{\text{WR}}$ | | P65 | Strobe signal output for write operation of external memory |
| $\overline{\text{WAIT}}$ | Input | P66 | To insert wait state(s) when external memory is accessed |
| ASTB | Output | P67 | Strobe output to externally latch address information output to ports 4 through 6 and port 8 to access external memory |
| $\overline{\text{RESET}}$ | Input | — | System reset input |
| X1 | Input | — | Crystal connection for main system clock oscillation |
| X2 | — | | |
| XT1 | Input | — | Crystal connection for subsystem clock oscillation |
| XT2 | — | | |
| ANI0 to ANI7 | Input | P10 to P17 | Analog voltage input for A/D converter |
| ANO0, ANO1 | Output | P130, P131 | Analog voltage output for D/A converter |
| AV_{REF0} | — | — | To apply reference voltage for A/D converter |
| AV_{REF1} | | | To apply reference voltage for D/A converter |
| AV_{DD} | | | Positive power supply for A/D converter. Connect to V_{DD} . |
| AV_{SS} | | | GND for A/D converter and D/A converter. Connect to V_{SS} . |
| V_{DD} | | | Positive power supply |
| V_{SS} | | | GND |
| TEST | | | Connect directly to V_{SS} (this pin is for IC test). |

5.3 Pin I/O Circuits and Recommended Connections of Unused Pins

The input/output circuit type of each pin and recommended connections of unused pins are shown in Table 5-1.

For each type of input/output circuit, refer to Figure 5-1.

Table 5-1. Type of Pin Input/Output Circuits and Recommended Connections of Unused Pins (1/2)

| Pin Name | I/O Circuit Type | I/O | Recommended Connections of Unused Pins |
|------------------------|------------------|-------|--|
| P00/INTP0 | 8-A | I/O | Input: Independently connect to V _{SS} via a resistor Output: Leave open |
| P01/INTP1 | | | |
| P02/INTP2/NMI | | | |
| P03/INTP3 to P06/INTP6 | | | |
| P10/ANI0 to P17/ANI7 | 9 | Input | Connect to V _{SS} or V _{DD} |
| P20/RxD1/SI1 | 10-A | I/O | Input: Independently connect to V _{SS} via a resistor Output: Leave open |
| P21/TxD1/SO1 | | | |
| P22/ASCK1/SCK1 | | | |
| P23/PCL | | | |
| P24/BUZ | | | |
| P25/SDA0/SI0 | | | |
| P26/SO0 | | | |
| P27/SCL0/SCK0 | | | |
| P30/TO0 to P32/TO2 | | | |
| P33/TI1, P34/TI2 | | | |
| P35/TI00, P36/TI01 | | | |
| P37 | | | |
| P40/AD0 to P47/AD7 | 5-A | | |
| P50/A8 to P57/A15 | | | |
| P60/A16 to P63/A19 | | | |
| P64/RD | | | |
| P65/WR | | | |
| P66/WAIT | | | |
| P67/ASTB | | | |
| P70/RxD2/SI2 | 8-A | | |
| P71/TxD2/SO2 | | | |
| P72/ASCK2/SCK2 | | | |
| P80/A0 to P87/A7 | | | |
| P90 to P95 | 13-D | | |
| P100/TI5/TO5 | 8-A | | |
| P101/TI6/TO6 | | | |
| P102/TI7/TO7 | | | |
| P103/TI8/TO8 | | | |
| P120/RTP0 to P127/RTP7 | | | |
| P130/ANO0, P131/ANO1 | 12-A | | |

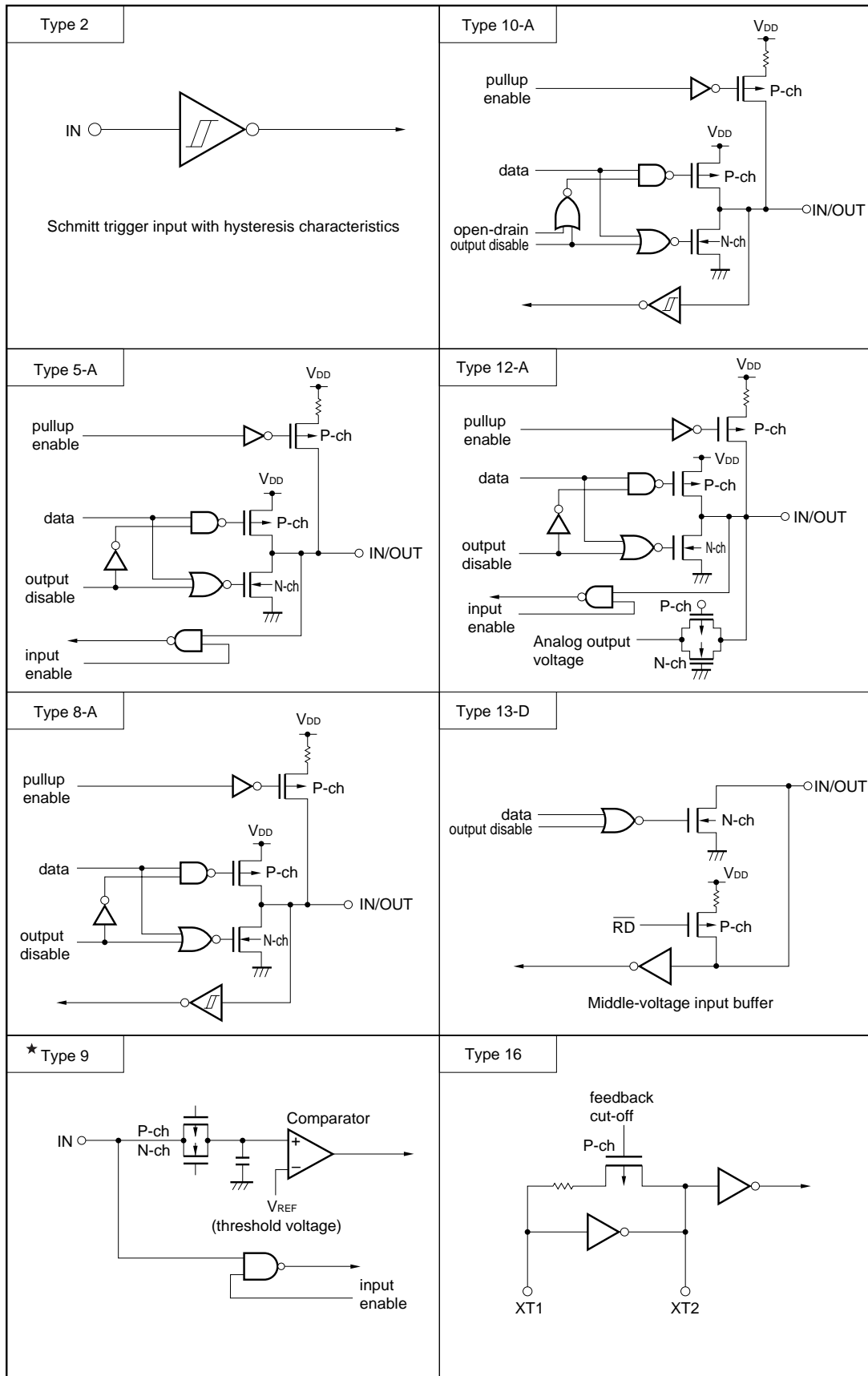
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Table 5-1. Types of Pin Input/Output Circuits and Recommended Connections of Unused Pins (2/2)

| Pin Name | I/O Circuit Type | I/O | Recommended Connections of Unused Pins |
|--------------------|------------------|-------|--|
| RESET | 2 | Input | — |
| XT1 | 16 | — | Connect to V _{SS} |
| XT2 | | | Leave open |
| AV _{REF0} | — | — | Connect to V _{SS} |
| AV _{REF1} | | | Connect to V _{DD} |
| AV _{DD} | | | |
| AV _{SS} | | | Connect to V _{SS} |
| TEST | | | Connect directly to V _{SS} |
| | | | |

Remark Because the circuit type numbers are standardized among the 78K Series products, they are not sequential in some models (i.e., some circuits are not provided).

Figure 5-1. Types of Pin I/O Circuits



6. CPU ARCHITECTURE

6.1 Memory Space

A memory space of 1 Mbyte can be accessed. Mapping of the internal data area (special function registers and internal RAM) can be specified by the LOCATION instruction. The LOCATION instruction must be always executed after reset cancellation, and must not be used more than once.

(1) When LOCATION 0 instruction is executed

- **Internal memory**

The internal data area and internal ROM area are mapped as follows:

| Part Number | Internal Data Area | Internal ROM Area |
|-------------|--------------------|--------------------------------------|
| μPD784214Y | 0F100H to 0FFFFH | 00000H to 0F0FFH 10000H to 17FFFH |
| μPD784215Y | 0EB00H to 0FFFFH | 00000H to 0EAFH 10000H to 1FFFFH |
| μPD784216Y | 0DF00H to 0FFFFH | 00000H to 0DEFFH 10000H to 1FFFFH |

Caution The following areas that overlap the internal data area of the internal ROM cannot be used when the LOCATION 0 instruction is executed.

| Part Number | Unusable Area |
|-------------|-------------------------------|
| μPD784214Y | 0F100H to 0FFFFH (3840 bytes) |
| μPD784215Y | 0EB00H to 0FFFFH (5376 bytes) |
| μPD784216Y | 0DF00H to 0FFFFH (8448 bytes) |

- **External memory**

The external memory is accessed in external memory expansion mode.

(2) When LOCATION 0FH instruction is executed

- **Internal memory**

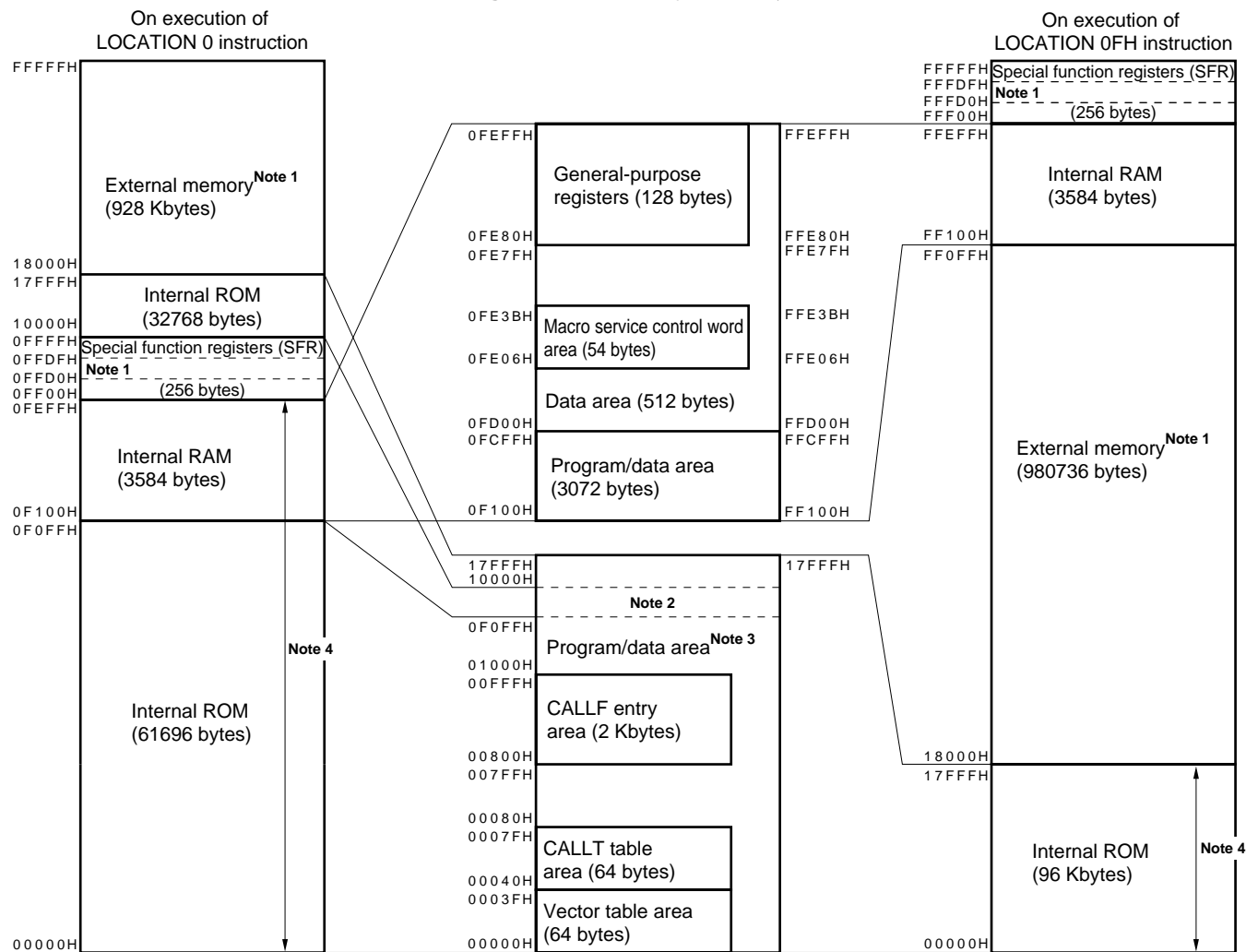
The internal data area and internal ROM area are mapped as follows:

| Part Number | Internal Data Area | Internal ROM Area |
|-------------|--------------------|-------------------|
| μPD784214Y | FF100H to FFFFFH | 00000H to 17FFFH |
| μPD784215Y | FEB00H to FFFFFH | 00000H to 1FFFFH |
| μPD784216Y | FDF00H to FFFFFH | 00000H to 1FFFFH |

- **External memory**

The external memory is accessed in external memory expansion mode.

Figure 6-1. Memory Map of μPD784214Y



- Notes**
1. Accessed in external memory expansion mode.
 2. This 3840-byte area can be used as an internal ROM only when the LOCATION 0FH instruction is executed.
 3. On execution of LOCATION 0 instruction: 94464 bytes, on execution of LOCATION 0FH instruction: 98304 bytes
 4. Base area and entry area for reset or interrupt. However, the internal RAM area is not used as a reset entry area.

Figure 6-2. Memory Map of μ PD784215Y

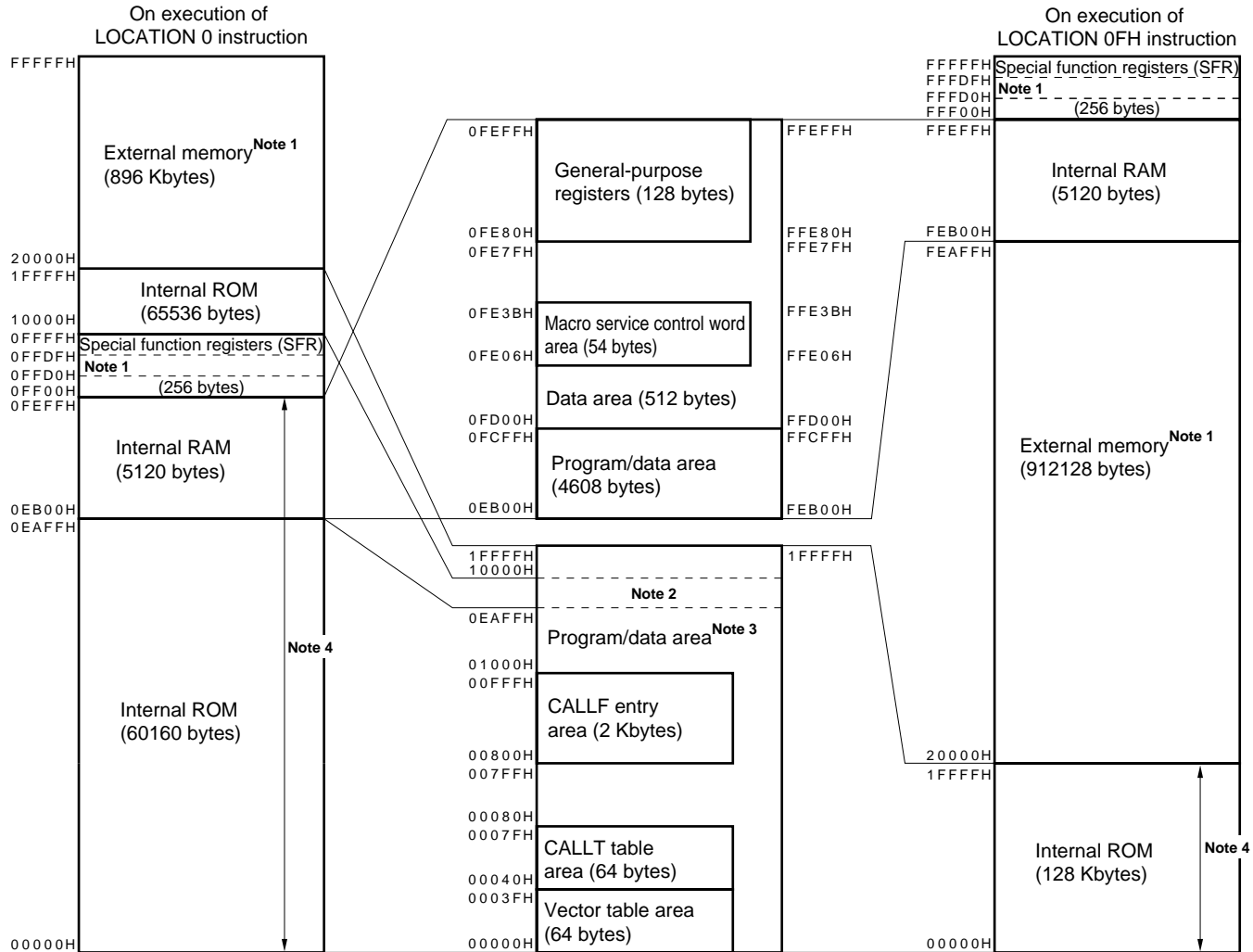
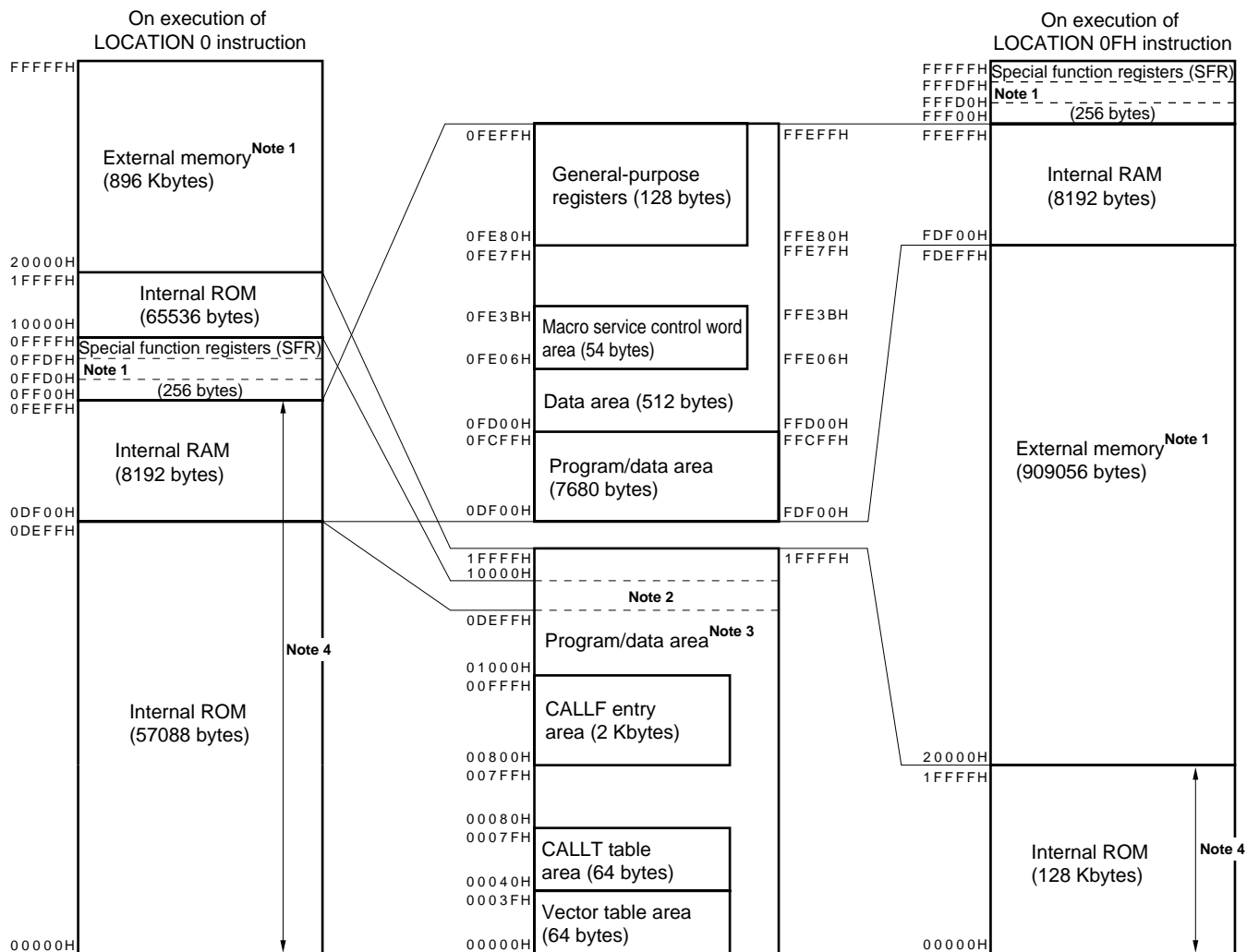


Figure 6-3. Memory Map of μPD784216Y



- Notes**
1. Accessed in external memory expansion mode.
 2. This 8448-byte area can be used as an internal ROM only when the LOCATION 0FH instruction is executed.
 3. On execution of LOCATION 0 instruction: 122624 bytes, on execution of LOCATION 0FH instruction: 131072 bytes.
 4. Base area and entry area for reset or interrupt. However, the internal RAM area is not used as a reset entry area.

6.2 CPU Registers

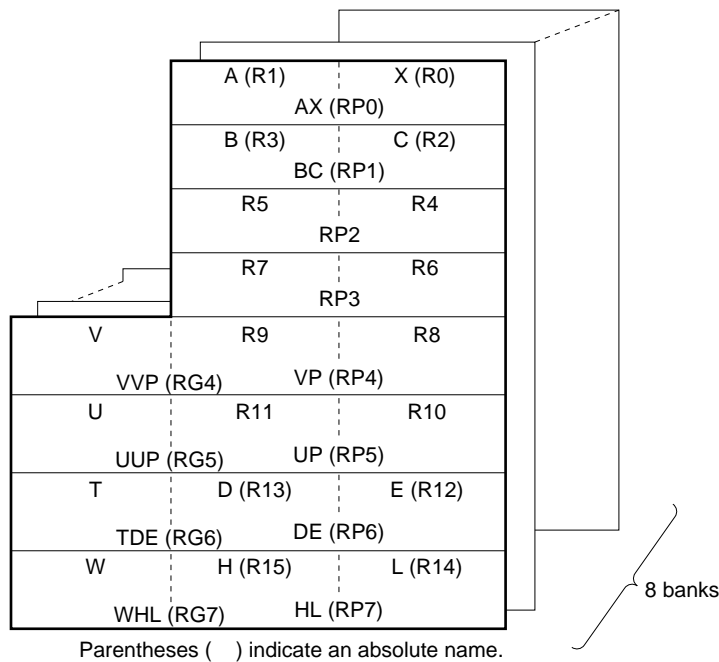
6.2.1 General-purpose registers

Sixteen 8-bit general-purpose registers are available. Two 8-bit registers can be also used in pairs as a 16-bit register. Of the 16-bit registers, four can be used in combination with an 8-bit register for address expansion as 24-bit address specification registers.

Eight banks of these register sets are available which can be selected by using software or the context switching function.

The general-purpose registers except V, U, T, and W registers for address expansion are mapped to the internal RAM.

Figure 6-4. General-Purpose Register Format



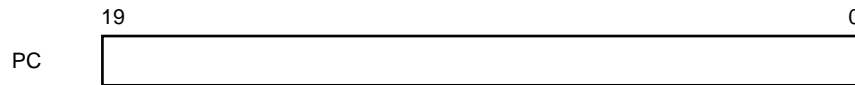
Caution Registers R4, R5, R6, R7, RP2, and RP3 can be used as X, A, C, B, AX, and BC registers, respectively, by setting the RSS bit of the PSW to 1. However, use this function only for recycling the program of the 78K/III Series.

6.2.2 Control registers

(1) Program counter (PC)

The program counter is a 20-bit register whose contents are automatically updated when the program is executed.

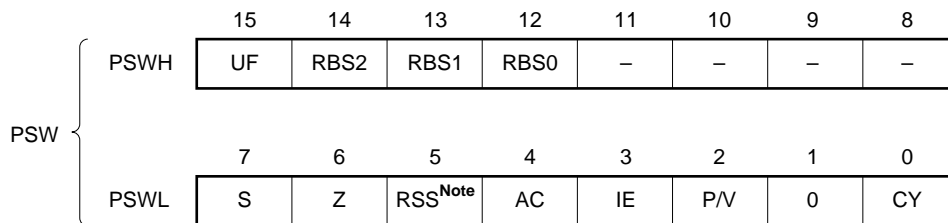
Figure 6-5. Program Counter (PC) Format



(2) Program status word (PSW)

This register holds the statuses of the CPU. Its contents are automatically updated when the program is executed.

Figure 6-6. Program Status Word (PSW) Format

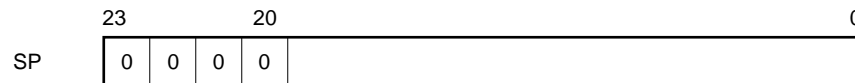


Note This flag is provided to maintain compatibility with the 78K/III Series. Be sure to clear this flag to 0, except when the software for the 78K/III Series is used.

(3) Stack pointer (SP)

This is a 24-bit pointer that holds the first address of the stack. Be sure to write 0 to the higher 4 bits of this pointer.

Figure 6-7. Stack Pointer (SP) Format



6.2.3 Special function registers (SFRs)

The special function registers, such as the mode registers and control registers of the internal peripheral hardware, are registers to which special functions are allocated. These registers are mapped to a 256-byte space of addresses 0FF00H through 0FFFFH **Note**.

Note On execution of the LOCATION 0 instruction. FFF00H through FFFFFH on execution of the LOCATION 0FH instruction.

Caution Do not access an address in this area to which no SFR is allocated. If such an address is accessed by mistake, the μPD784216 may be in the deadlock status. This deadlock status can be cleared only by inputting the RESET signal.

Table 6-1 lists the special function registers (SFRs). The meanings of the symbols in this table are as follows:

- Symbol Symbol indicating an SFR. This symbol is reserved for NEC's assembler (RA78K4). It can be used as sfr variable by the #pragma sfr command with the C compiler (CC78K4).
- R/W Indicates whether the SFR is read-only, write-only, or read/write.
 R/W: Read/write
 R: Read-only
 W: Write-only
- Bit units for manipulation .. Bit units in which the value of the SFR can be manipulated.
 SFRs that can be manipulated in 16-bit units can be described as the operand sfrp of an instruction. To specify the address of this SFR, describe an even address.
 SFRs that can be manipulated in 1-bit units can be described as the operand of a bit manipulation instruction.
- After reset Indicates the status of the register when the $\overline{\text{RESET}}$ signal has been input.

Table 6-1. Special Function Register (SFR) List (1/4)

| Address ^{Note 1} | Special Function Register (SFR) Name | Symbol | R/W | Bit Units for Manipulation | | | After Reset |
|---------------------------|---|--------|-----|----------------------------|--------|---------|-----------------------|
| | | | | 1 bit | 8 bits | 16 bits | |
| 0FF00H | Port 0 | P0 | R/W | √ | √ | — | 00H ^{Note 2} |
| 0FF01H | Port 1 | P1 | R | √ | √ | — | |
| 0FF02H | Port 2 | P2 | R/W | √ | √ | — | |
| 0FF03H | Port 3 | P3 | | √ | √ | — | |
| 0FF04H | Port 4 | P4 | | √ | √ | — | |
| 0FF05H | Port 5 | P5 | | √ | √ | — | |
| 0FF06H | Port 6 | P6 | | √ | √ | — | |
| 0FF07H | Port 7 | P7 | | √ | √ | — | |
| 0FF08H | Port 8 | P8 | | √ | √ | — | |
| 0FF09H | Port 9 | P9 | | √ | √ | — | |
| 0FF0AH | Port 10 | P10 | | √ | √ | — | |
| 0FF0CH | Port 12 | P12 | | √ | √ | — | |
| 0FF0DH | Port 13 | P13 | √ | √ | — | | |
| 0FF10H | 16-bit timer register | TM0 | R | — | — | √ | |
| 0FF11H | | | | | | | |
| 0FF12H | Capture/compare register 00 (16-bit timer/counter) | CR00 | R/W | — | — | √ | |
| 0FF13H | | | | | | | |
| 0FF14H | Capture/compare register 01 (16-bit timer/counter) | CR01 | | — | — | √ | |
| 0FF15H | | | | | | | |
| 0FF16H | Capture/compare control register 0 | CRC0 | | √ | √ | — | 00H |
| 0FF18H | 16-bit timer mode control register | TMC0 | | √ | √ | — | |
| 0FF1AH | 16-bit timer output control register | TOC0 | | √ | √ | — | |
| 0FF1CH | Prescaler mode register 0 | PRM0 | | √ | √ | — | FFH |
| 0FF20H | Port mode 0 register | PM0 | | √ | √ | — | |
| 0FF22H | Port mode 2 register | PM2 | | √ | √ | — | |
| 0FF23H | Port mode 3 register | PM3 | | √ | √ | — | |
| 0FF24H | Port mode 4 register | PM4 | | √ | √ | — | |
| 0FF25H | Port mode 5 register | PM5 | | √ | √ | — | |
| 0FF26H | Port mode 6 register | PM6 | | √ | √ | — | |
| 0FF27H | Port mode 7 register | PM7 | | √ | √ | — | |
| 0FF28H | Port mode 8 register | PM8 | | √ | √ | — | |
| 0FF29H | Port mode 9 register | PM9 | | √ | √ | — | |
| 0FF2AH | Port mode 10 register | PM10 | | √ | √ | — | |
| 0FF2CH | Port mode 12 register | PM12 | | √ | √ | — | |
| 0FF2DH | Port mode 13 register | PM13 | | √ | √ | — | |

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- Notes**
1. When the LOCATION 0 instruction is executed. Add "F0000H" to this value when the LOCATION 0FH instruction is executed.
 2. Because each port is initialized to input mode after reset, "00H" is not actually read. The output latch is initialized to "0".

Table 6-1. Special Function Register (SFR) List (2/4)

| Address ^{Note} | Special Function Register (SFR) Name | Symbol | | R/W | Bit Units for Manipulation | | | After Reset |
|-------------------------|---|--------|-------|-----|----------------------------|--------|---------|-------------|
| | | | | | 1 bit | 8 bits | 16 bits | |
| 0FF30H | Pull-up resistor option register 0 | PU0 | | R/W | √ | √ | — | 00H |
| 0FF32H | Pull-up resistor option register 2 | PU2 | | | √ | √ | — | |
| 0FF33H | Pull-up resistor option register 3 | PU3 | | | √ | √ | — | |
| 0FF37H | Pull-up resistor option register 7 | PU7 | | | √ | √ | — | |
| 0FF38H | Pull-up resistor option register 8 | PU8 | | | √ | √ | — | |
| 0FF3AH | Pull-up resistor option register 10 | PU10 | | | √ | √ | — | |
| 0FF3CH | Pull-up resistor option register 12 | PU12 | | | √ | √ | — | |
| 0FF40H | Clock output control register | CKS | | | √ | √ | — | |
| 0FF42H | Port function control register | PF2 | | | √ | √ | — | |
| 0FF4EH | Pull-up resistor option register | PUO | | | √ | √ | — | |
| 0FF50H | 8-bit timer register 1 | TM1 | TM1W | R | — | √ | √ | 0000H |
| 0FF51H | 8-bit timer register 2 | TM2 | | | — | √ | | |
| 0FF52H | Compare register 10 (8-bit timer/counter 1) | CR10 | CR1W | R/W | — | √ | √ | |
| 0FF53H | Compare register 20 (8-bit timer/counter 2) | CR20 | | | — | √ | | |
| 0FF54H | 8-bit timer mode control register 1 | TMC1 | TMC1W | | √ | √ | √ | |
| 0FF55H | 8-bit timer mode control register 2 | TMC2 | | | √ | √ | | |
| ★ 0FF56H | Prescaler mode register 1 | PRM1 | PRM1W | | √ | √ | √ | |
| ★ 0FF57H | Prescaler mode register 2 | PRM2 | | | √ | √ | | |
| 0FF60H | 8-bit timer register 5 | TM5 | TM5W | R | — | √ | √ | |
| 0FF61H | 8-bit timer register 6 | TM6 | | | — | √ | | |
| 0FF62H | 8-bit timer register 7 | TM7 | TM7W | | — | √ | √ | |
| 0FF63H | 8-bit timer register 8 | TM8 | | | — | √ | | |
| 0FF64H | Compare register 50 (8-bit timer/counter 5) | CR50 | CR5W | R/W | — | √ | √ | |
| 0FF65H | Compare register 60 (8-bit timer/counter 6) | CR60 | | | — | √ | | |
| 0FF66H | Compare register 70 (8-bit timer/counter 7) | CR70 | CR7W | | — | √ | √ | |
| 0FF67H | Compare register 80 (8-bit timer/counter 8) | CR80 | | | — | √ | | |
| 0FF68H | 8-bit timer mode control register 5 | TMC5 | TMC5W | | √ | √ | √ | |
| 0FF69H | 8-bit timer mode control register 6 | TMC6 | | | √ | √ | | |
| 0FF6AH | 8-bit timer mode control register 7 | TMC7 | TMC7W | | √ | √ | √ | |
| 0FF6BH | 8-bit timer mode control register 8 | TMC8 | | | √ | √ | | |
| ★ 0FF6CH | Prescaler mode register 5 | PRM5 | PRM5W | | √ | √ | √ | |
| ★ 0FF6DH | Prescaler mode register 6 | PRM6 | | | √ | √ | | |
| ★ 0FF6EH | Prescaler mode register 7 | PRM7 | PRM7W | | √ | √ | √ | |
| ★ 0FF6FH | Prescaler mode register 8 | PRM8 | | | √ | √ | | |
| 0FF70H | Asynchronous serial interface mode register 1 | ASIM1 | | R | √ | √ | — | 00H |
| 0FF71H | Asynchronous serial interface mode register 2 | ASIM2 | | | √ | √ | — | |
| ★ 0FF72H | Asynchronous serial interface status register 1 | ASIS1 | | | √ | √ | — | |
| ★ 0FF73H | Asynchronous serial interface status register 2 | ASIS2 | | | √ | √ | — | |

Note When the LOCATION 0 instruction is executed. Add “F0000H” to this value when the LOCATION 0FH instruction is executed.

Table 6-1. Special Function Register (SFR) List (3/4)

| Address ^{Note} | Special Function Register (SFR) Name | Symbol | R/W | Bit Units for Manipulation | | | After Reset | | | |
|-------------------------|---|--------|-----|----------------------------|--------|---------|-------------|---|-----------|-----|
| | | | | 1 bit | 8 bits | 16 bits | | | | |
| 0FF74H | Transmit shift register 1 | TXS1 | W | — | √ | — | FFH | | | |
| | Receive buffer register 1 | RXB1 | R | — | √ | — | | | | |
| 0FF75H | Transmit shift register 2 | TXS2 | W | — | √ | — | FFH | | | |
| | Receive buffer register 2 | RXB2 | R | — | √ | — | | | | |
| ★ 0FF76H | Baud rate generator control register 1 | BRGC1 | R/W | √ | √ | — | 00H | | | |
| ★ 0FF77H | Baud rate generator control register 2 | BRGC2 | | √ | √ | — | | | | |
| 0FF7AH | Oscillation mode select register | CC | | √ | √ | — | | | | |
| 0FF80H | A/D converter mode register | ADM | | √ | √ | — | | | | |
| 0FF81H | A/D converter input select register | ADIS | | √ | √ | — | | | | |
| 0FF83H | A/D conversion result register | ADCR | | R | — | √ | | — | Undefined | |
| 0FF84H | D/A conversion value setting register 0 | DACS0 | R/W | √ | √ | — | 00H | | | |
| 0FF85H | D/A conversion value setting register 1 | DACS1 | | √ | √ | — | | | | |
| 0FF86H | D/A converter mode register 0 | DAM0 | | √ | √ | — | | | | |
| 0FF87H | D/A converter mode register 1 | DAM1 | | √ | √ | — | | | | |
| 0FF8CH | External bus type select register | EBTS | | √ | √ | — | | | | |
| 0FF90H | Serial operation mode register 0 | CSIM0 | | √ | √ | — | | | | |
| 0FF91H | Serial operation mode register 1 | CSIM1 | | √ | √ | — | | | | |
| 0FF92H | Serial operation mode register 2 | CSIM2 | | √ | √ | — | | | | |
| 0FF94H | Serial I/O shift register 0 | SIO0 | | — | √ | — | | | | |
| 0FF95H | Serial I/O shift register 1 | SIO1 | | — | √ | — | | | | |
| 0FF96H | Serial I/O shift register 2 | SIO2 | | — | √ | — | | | | |
| 0FF98H | Real-time output buffer register L | RTBL | | — | √ | — | | | | |
| 0FF99H | Real-time output buffer register H | RTBH | | — | √ | — | | | | |
| 0FF9AH | Real-time output port mode register | RTPM | | √ | √ | — | | | | |
| 0FF9BH | Real-time output port control register | RTPC | | √ | √ | — | | | | |
| 0FF9CH | Watch timer mode control register | WTM | | √ | √ | — | | | | |
| 0FFA0H | External interrupt rising edge enable register | EGP0 | | √ | √ | — | | | | |
| 0FFA2H | External interrupt falling edge enable register | EGN0 | | √ | √ | — | | | | |
| 0FFA8H | In-service priority register | ISPR | | R | √ | √ | | — | | |
| 0FFA9H | Interrupt select control register | SNMI | | R/W | √ | √ | | — | 80H | |
| 0FFAAH | Interrupt mode control register | IMC | | | √ | √ | | — | | |
| 0FFACH | Interrupt mask flag register 0L | MK0L | | | MK0 | √ | | √ | | √ |
| 0FFADH | Interrupt mask flag register 0H | MK0H | | | | | | | | |
| 0FFAEH | Interrupt mask flag register 1L | MK1L | | | MK1 | √ | | √ | | √ |
| 0FFAFH | Interrupt mask flag register 1H | MK1H | | | | | | | | |
| ★ 0FFB0H | I ² C bus control register | IICC0 | | | √ | √ | | — | | 00H |
| ★ 0FFB2H | Prescaler mode register for serial clock | SRPM0 | √ | | √ | — | | | | |
| 0FFB4H | Slave address register | SVA0 | √ | √ | — | | | | | |

Note When the LOCATION 0 instruction is executed. Add "F0000H" to this value when the LOCATION 0FH instruction is executed.

Table 6-1. Special Function Register (SFR) List (4/4)

| Address ^{Note} | Special Function Register (SFR) Name | Symbol | R/W | Bit Units for Manipulation | | | After Reset | |
|-------------------------|---|--------|-----|----------------------------|--------|---------|-------------|-----|
| | | | | 1 bit | 8 bits | 16 bits | | |
| ★ 0FFB6H | I ² C bus status register | IICS0 | R | √ | √ | — | 00H | |
| 0FFB8H | Serial shift register | IIC0 | R/W | √ | √ | — | | |
| 0FFC0H | Standby control register | STBC | | — | √ | — | | 30H |
| 0FFC2H | Watchdog timer mode register | WDM | | — | √ | — | | 00H |
| 0FFC4H | Memory expansion mode register | MM | | √ | √ | — | | 20H |
| ★ 0FFC7H | Programmable wait control register 1 | PWC1 | | √ | √ | — | AAH | |
| ★ 0FFCEH | Clock status register | PCS | R | √ | √ | — | 32H | |
| ★ 0FFCFH | Oscillation stabilization time specification register | OSTS | R/W | √ | √ | — | 00H | |
| 0FFD0H to 0FFDFH | External SFR area | — | | √ | √ | — | — | |
| 0FFE0H | Interrupt control register (INTWDTM) | WDTIC | | √ | √ | — | 43H | |
| 0FFE1H | Interrupt control register (INTP0) | PIC0 | | √ | √ | — | | |
| 0FFE2H | Interrupt control register (INTP1) | PIC1 | | √ | √ | — | | |
| 0FFE3H | Interrupt control register (INTP2) | PIC2 | | √ | √ | — | | |
| 0FFE4H | Interrupt control register (INTP3) | PIC3 | | √ | √ | — | | |
| 0FFE5H | Interrupt control register (INTP4) | PIC4 | | √ | √ | — | | |
| 0FFE6H | Interrupt control register (INTP5) | PIC5 | | √ | √ | — | | |
| 0FFE7H | Interrupt control register (INTP6) | PIC6 | | √ | √ | — | | |
| 0FFE8H | Interrupt control register (INTCSI0) | CSIIC0 | | √ | √ | — | | |
| 0FFE9H | Interrupt control register (INTIIC0/INTSER1) | SERIC1 | | √ | √ | — | | |
| 0FFEAH | Interrupt control register (INTSR1/INTCSI1) | SRIC1 | | √ | √ | — | | |
| 0FFEBH | Interrupt control register (INTST1) | STIC1 | | √ | √ | — | | |
| 0FFECH | Interrupt control register (INTSER2) | SERIC2 | | √ | √ | — | | |
| 0FFEDH | Interrupt control register (INTSR2/INTCSI2) | SRIC2 | | √ | √ | — | | |
| 0FFEEH | Interrupt control register (INTST2) | STIC2 | | √ | √ | — | | |
| 0FFEFH | Interrupt control register (INTTM3) | TMIC3 | | √ | √ | — | | |
| 0FFF0H | Interrupt control register (INTTM00) | TMIC00 | | √ | √ | — | | |
| 0FFF1H | Interrupt control register (INTTM01) | TMIC01 | | √ | √ | — | | |
| 0FFF2H | Interrupt control register (INTTM1) | TMIC1 | | √ | √ | — | | |
| 0FFF3H | Interrupt control register (INTTM2) | TMIC2 | | √ | √ | — | | |
| 0FFF4H | Interrupt control register (INTAD) | ADIC | | √ | √ | — | | |
| 0FFF5H | Interrupt control register (INTTM5) | TMIC5 | | √ | √ | — | | |
| 0FFF6H | Interrupt control register (INTTM6) | TMIC6 | | √ | √ | — | | |
| 0FFF7H | Interrupt control register (INTTM7) | TMIC7 | | √ | √ | — | | |
| 0FFF8H | Interrupt control register (INTTM8) | TMIC8 | | √ | √ | — | | |
| 0FFF9H | Interrupt control register (INTWT) | WTIC | | √ | √ | — | | |
| 0FFFAH | Interrupt control register (INTKR) | KRIC | | √ | √ | — | | |

Note When the LOCATION 0 instruction is executed. Add "F000H" to this value when the LOCATION 0FH instruction is executed.

7. PERIPHERAL HARDWARE FUNCTIONS

7.1 Ports

The ports shown in Figure 7-1 are provided to make various control operations possible. Table 7-1 shows the function of each port. Ports 0, 2 through 8, 10 and 12 can be connected to internal pull-up resistors by software when inputting.

Figure 7-1. Port Configuration

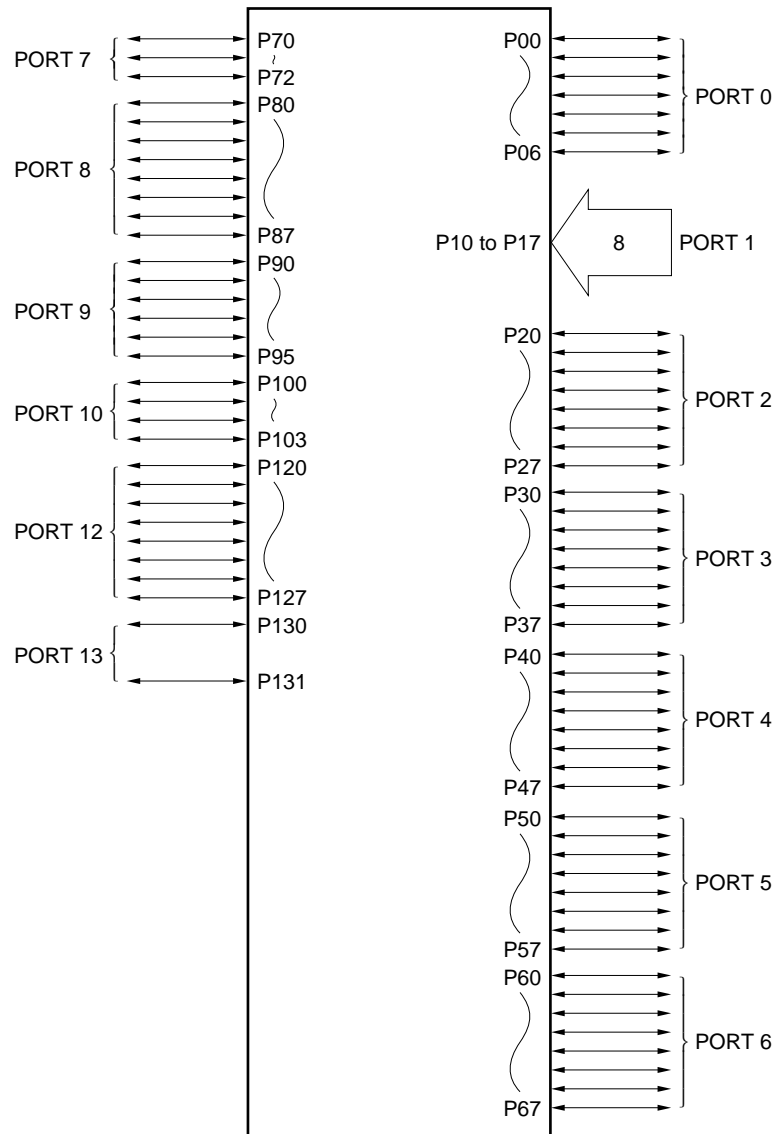


Table 7-1. Port Functions

| Port Name | Pin Name | Function | Specification of Pull-up Resistor Connection by Software |
|-----------|--------------|--|--|
| Port 0 | P00 to P06 | • Can be set in input or output mode in 1-bit units | Can be specified in 1-bit units |
| Port 1 | P10 to P17 | • Input port | — |
| Port 2 | P20 to P27 | • Can be set in input or output mode in 1-bit units | Can be specified in 1-bit units |
| Port 3 | P30 to P37 | • Can be set in input or output mode in 1-bit units | Can be specified in 1-bit units |
| Port 4 | P40 to P47 | • Can be set in input or output mode in 1-bit units • Can directly drive LEDs | Can be specified in 1-port units |
| Port 5 | P50 to P57 | • Can be set in input or output mode in 1-bit units • Can directly drive LEDs | Can be specified in 1-port units |
| Port 6 | P60 to P67 | • Can be set in input or output mode in 1-bit units | Can be specified in 1-port units |
| Port 7 | P70 to P72 | • Can be set in input or output mode in 1-bit units | Can be specified in 1-bit units |
| Port 8 | P80 to P87 | • Can be set in input or output mode in 1-bit units | Can be specified in 1-bit units |
| Port 9 | P90 to P95 | • N-ch open-drain I/O port • Can be set in input or output mode in 1-bit units • Can directly drive LEDs | — |
| Port 10 | P100 to P103 | • Can be set in input or output mode in 1-bit units | Can be specified in 1-bit units |
| Port 12 | P120 to P127 | • Can be set in input or output mode in 1-bit units | Can be specified in 1-bit units |
| Port 13 | P130, P131 | • Can be set in input or output mode in 1-bit units | — |

7.2 Clock Generation Circuit

An on-chip clock generation circuit necessary for operation is provided. This clock generation circuit has a frequency divider. If high-speed operation is not necessary, the internal operating frequency can be lowered by the frequency divider to reduce the current consumption.

Figure 7-2. Block Diagram of Clock Generation Circuit

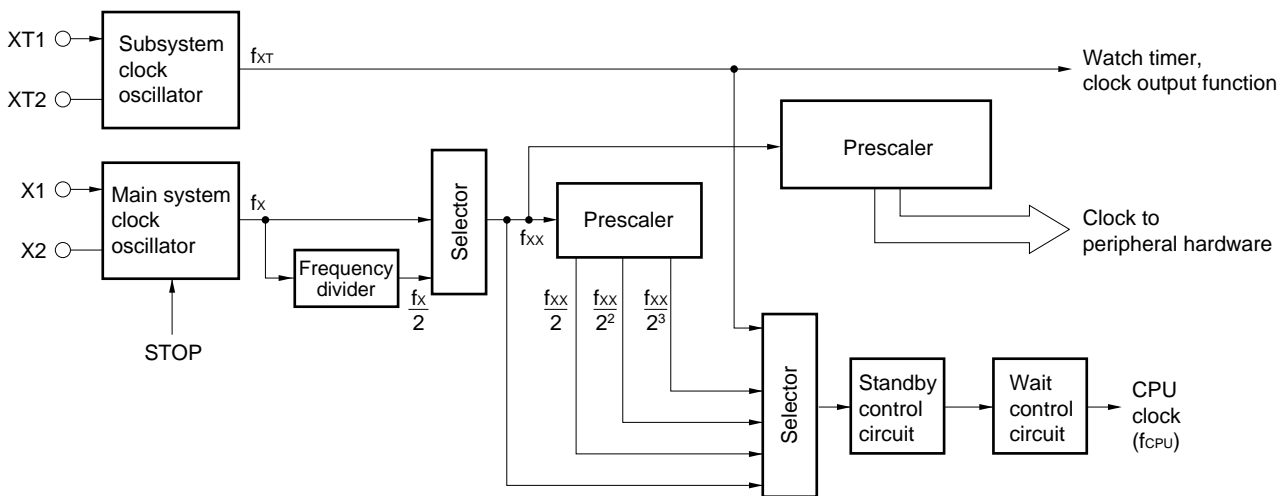


Figure 7-3. Example of Using Main System Clock Oscillator

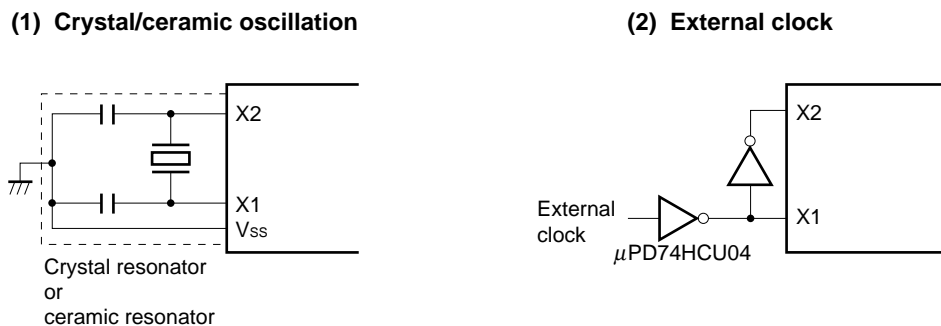
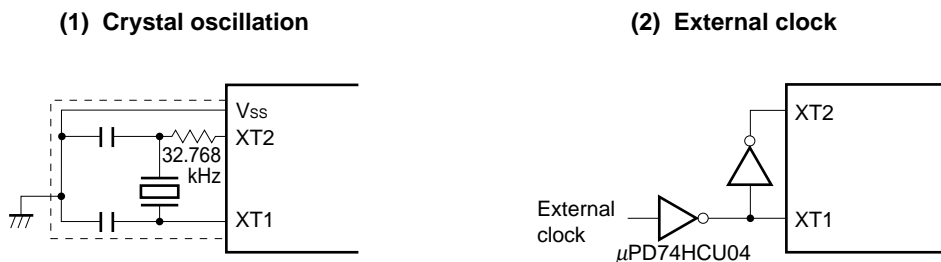


Figure 7-4. Example of Using Subsystem Clock Oscillator



Caution When using the main system clock and subsystem clock oscillator, wire the broken-lines portions in Figures 7-3 and 7-4 as follows to avoid adverse influence from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always keep the ground point of the oscillator capacitor to the same potential as Vss. Do not ground the capacitor to a ground pattern in which a high current flows.
- Do not fetch signals from the oscillator.

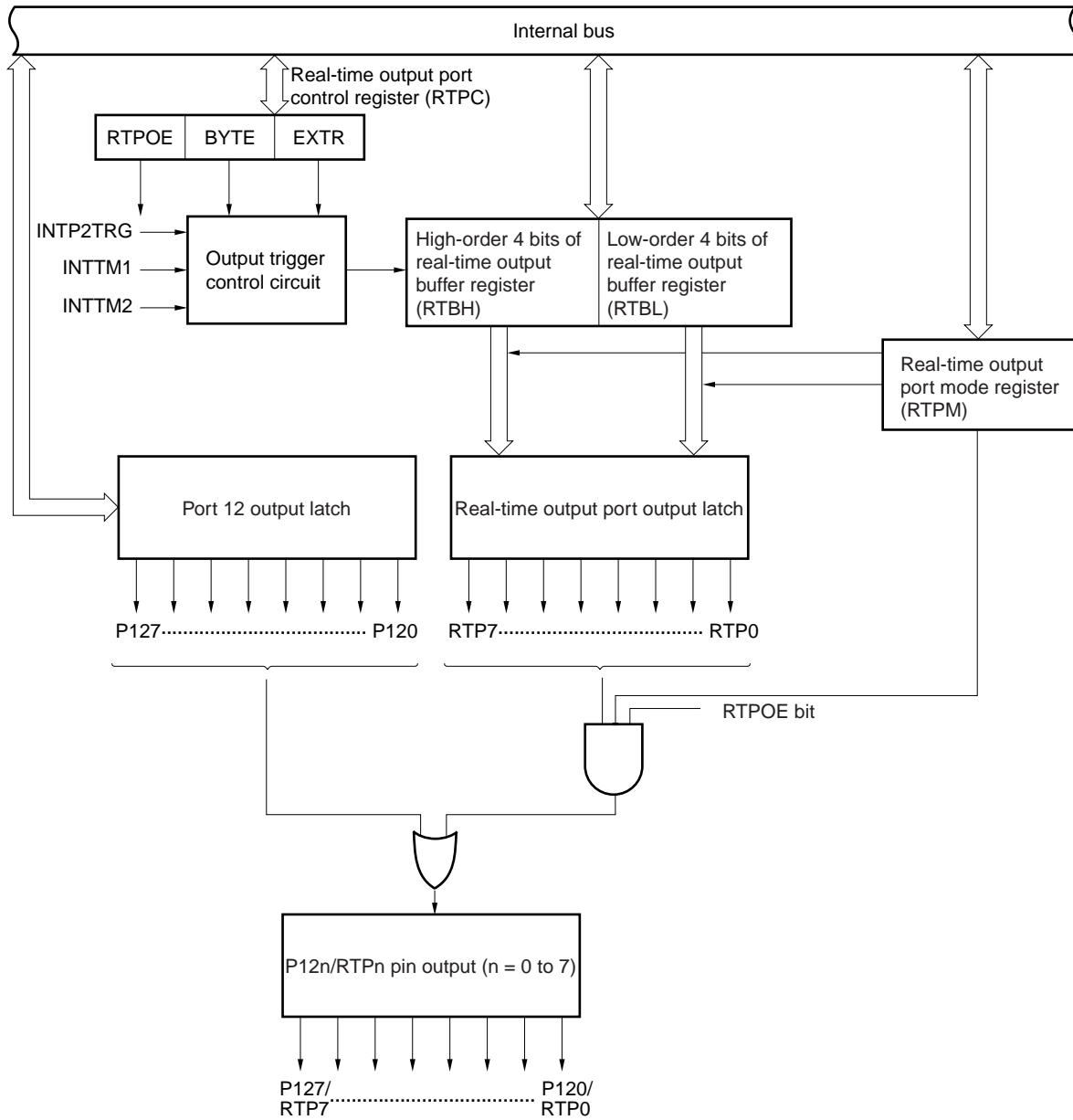
Note that the subsystem clock oscillator has a low amplification factor to reduce the current consumption.

7.3 Real-Time Output Port

The real-time output function is to transfer data set in advance to the real-time output buffer register to the output latch as soon as the timer interrupt or external interrupt has occurred in order to output the data to an external device. The pins that output the data to the external device constitute a port called a real-time output port.

Because the real-time output port can output signals without jitter, it is ideal for controlling a stepping motor.

★ Figure 7-5. Block Diagram of Real-Time Output Port



7.4 Timer/Counter

One unit of 16-bit timers/counters and six units of 8-bit timers/counters are provided.

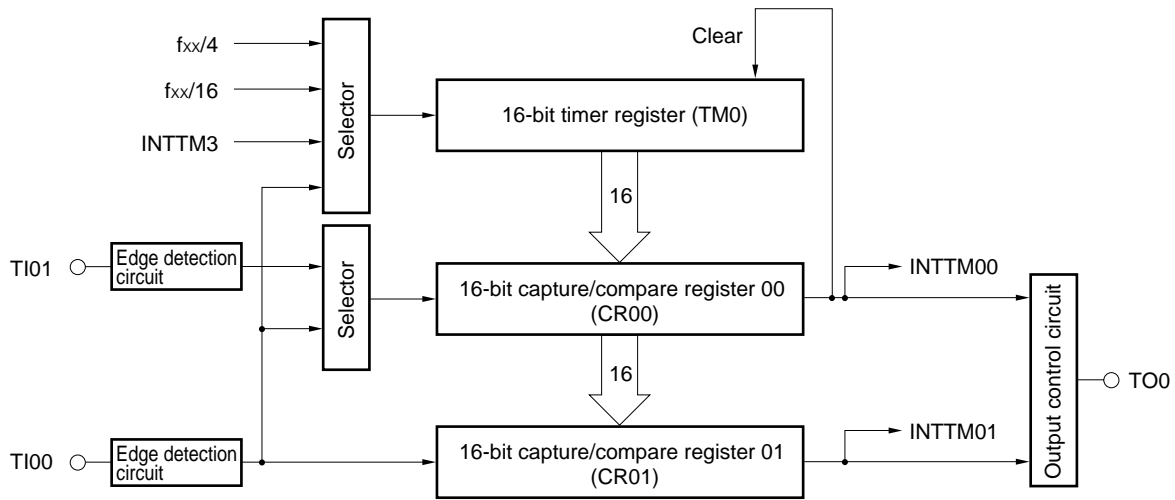
Because a total of eight interrupt requests are supported, these timers/counters can be used as eight units of timers/counters.

Table 7-2. Operations of Timers/Counters

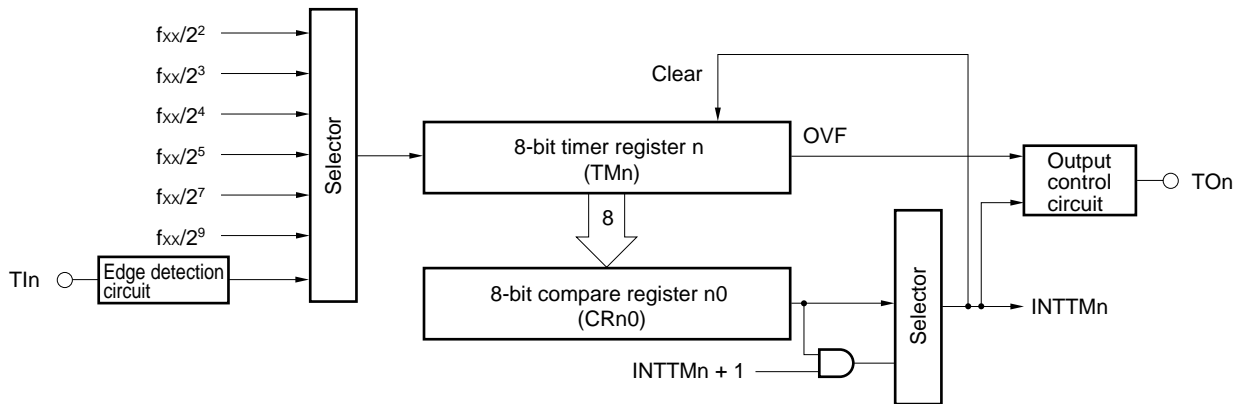
| Item | | Name | 16-Bit | 8-Bit | 8-Bit | 8-Bit | 8-Bit | 8-Bit | 8-Bit |
|----------------|------------------------------|------|-------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| | | | Timer/ Counter | Timer/ Counter 1 | Timer/ Counter 2 | Timer/ Counter 5 | Timer/ Counter 6 | Timer/ Counter 7 | Timer/ Counter 8 |
| Count width | 8 bits | | — | √ | √ | √ | √ | √ | √ |
| | 16 bits | | √ | √ | √ | √ | √ | √ | √ |
| Operation mode | Interval timer | | 1ch | 1ch | 1ch | 1ch | 1ch | 1ch | 1ch |
| | External event counter | | √ | √ | √ | √ | √ | √ | √ |
| Function | Timer output | | 1ch | 1ch | 1ch | 1ch | 1ch | 1ch | 1ch |
| | PPG output | | √ | — | — | — | — | — | — |
| | PWM output | | — | √ | √ | √ | √ | √ | √ |
| | Square wave output | | √ | √ | √ | √ | √ | √ | √ |
| | One-shot pulse output | | √ | — | — | — | — | — | — |
| | Pulse width measurement | | 2 inputs | — | — | — | — | — | — |
| | Number of interrupt requests | | 2 | 1 | 1 | 1 | 1 | 1 | 1 |

Figure 7-6. Block Diagram of Timers/Counters

16-bit timer/counter

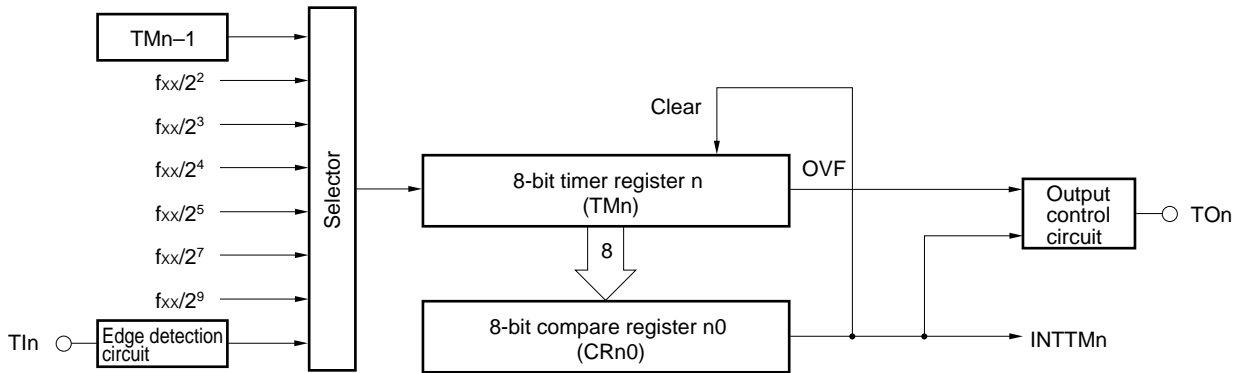


8-bit timer/counter 1, 5, 7



- Remarks 1. $n = 1, 5, 7$
- 2. OVF: overflow flag

8-bit timer/counter 2, 6, 8



- Remarks 1. $n = 2, 6, 8$
- 2. OVF: overflow flag

7.5 A/D Converter

An A/D converter converts an analog input variable into a digital signal. This microcontroller is provided with an A/D converter with a resolution of 8 bits and 8 channels (ANI0 through ANI7).

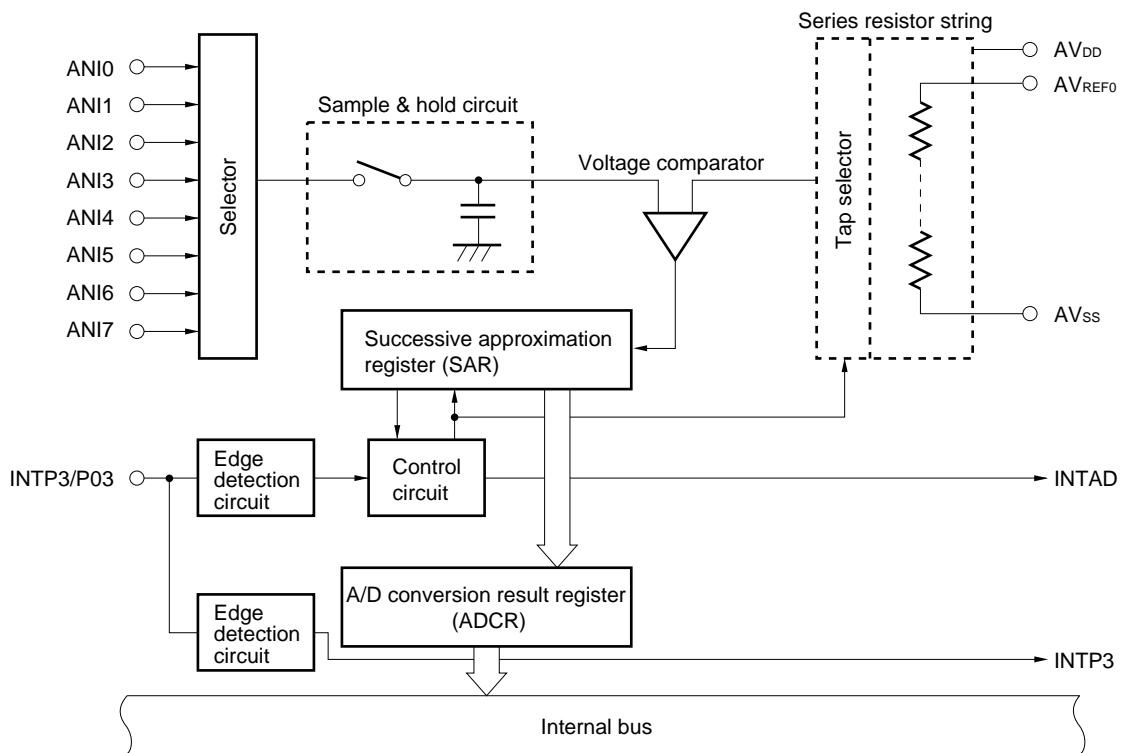
This A/D converter is of successive approximation type and the result of conversion is stored to an 8-bit A/D conversion result register (ADCR).

The A/D converter can be started in the following two ways:

- Hardware start
Conversion is started by trigger input (P03).
- Software start
Conversion is started by setting the A/D converter mode register (ADM).

One analog input channel is selected from ANI0 through ANI7 for A/D conversion. When A/D conversion is started by means of hardware start, conversion is stopped after it has been completed. When conversion is started by means of software start, A/D conversion is repeatedly executed, and each time conversion has been completed, an interrupt request (INTAD) is generated.

Figure 7-7. Block Diagram of A/D Converter



7.6 D/A Converter

A D/A converter converts an input digital signal into an analog voltage. This microcontroller is provided with a voltage output type D/A converter with a resolution of 8 bits and two channels.

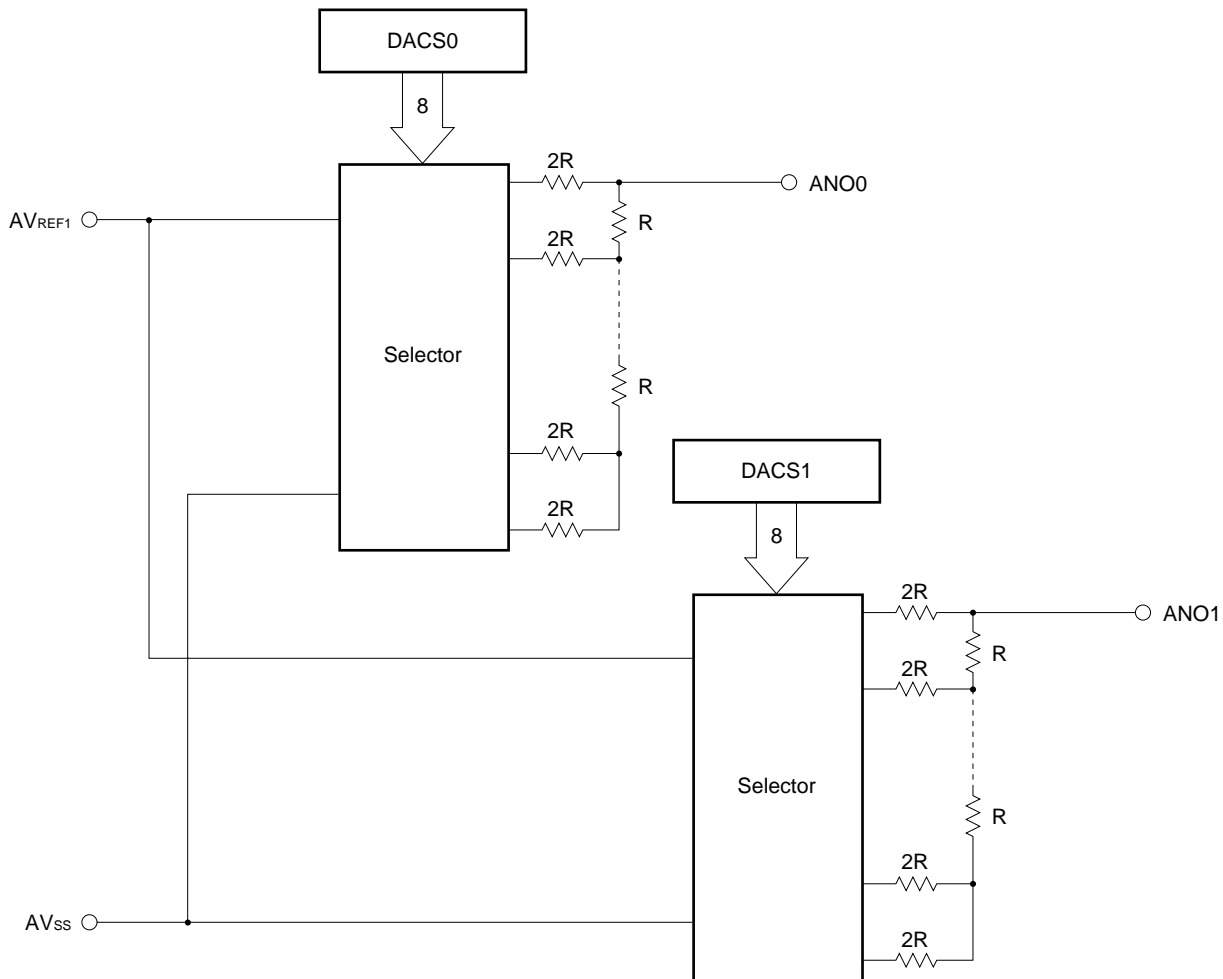
The conversion method is of R-2R resistor ladder type.

D/A conversion is started by setting DACE0 of the D/A converter mode register 0 (DAM0) and DACE1 of the D/A converter mode register 1 (DAM1).

The D/A converter operates in the following two modes:

- Normal mode
The converter outputs an analog voltage immediately after it has completed D/A conversion.
- Real-time output mode
The converter outputs an analog voltage in synchronization with an output trigger after it has completed D/A conversion.

Figure 7-8. Block Diagram of D/A Converter



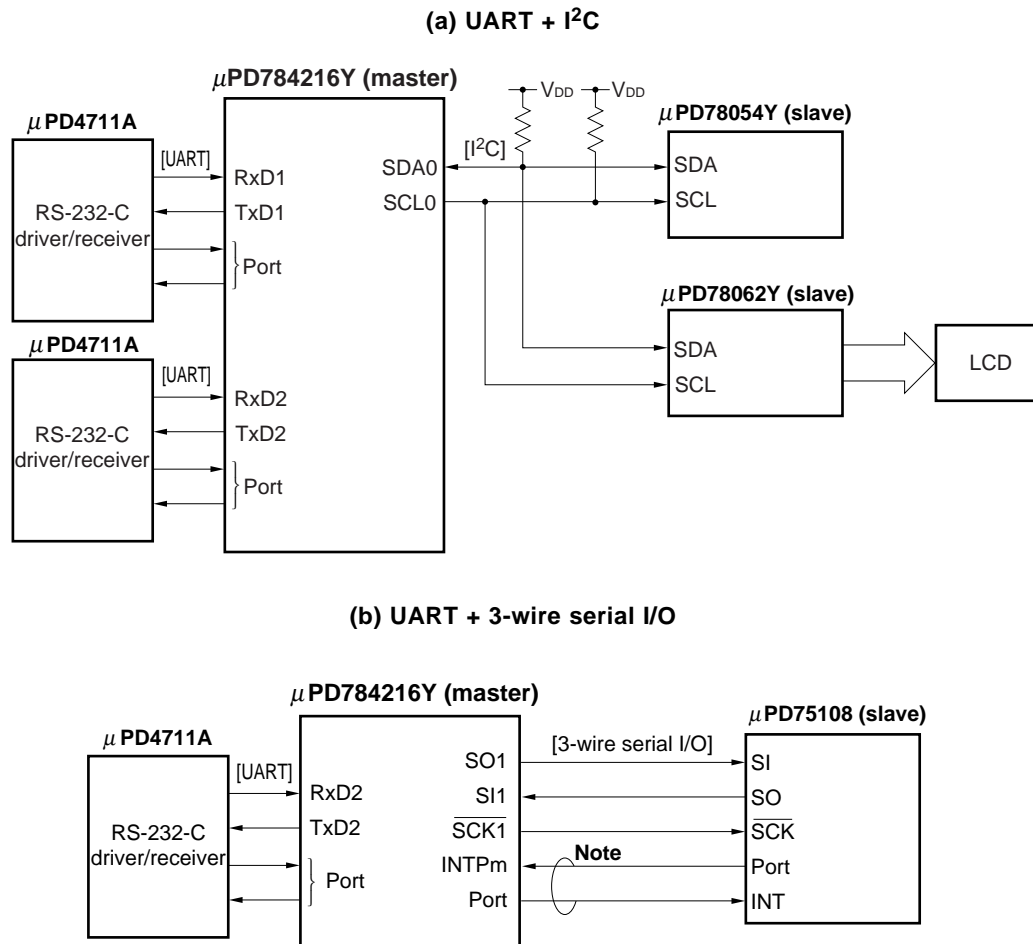
7.7 Serial Interface

Three independent serial interface channels are provided.

- Asynchronous serial interface (UART)/3-wire serial I/O (IOE) × 2
- Clocked serial interface (CSI) × 1
 - 3-wire serial I/O (IOE)
 - I²C bus interface

Therefore, communication with an external system and local communication within the system can be simultaneously executed (refer to Figure 7-9).

Figure 7-9. Example of Serial Interface



Note Handshake line

7.7.1 Asynchronous serial interface/3-wire serial I/O (UART/IOE)

Two channels of serial interfaces that can select an asynchronous serial interface mode and 3-wire serial I/O mode are provided.

(1) Asynchronous serial interface mode

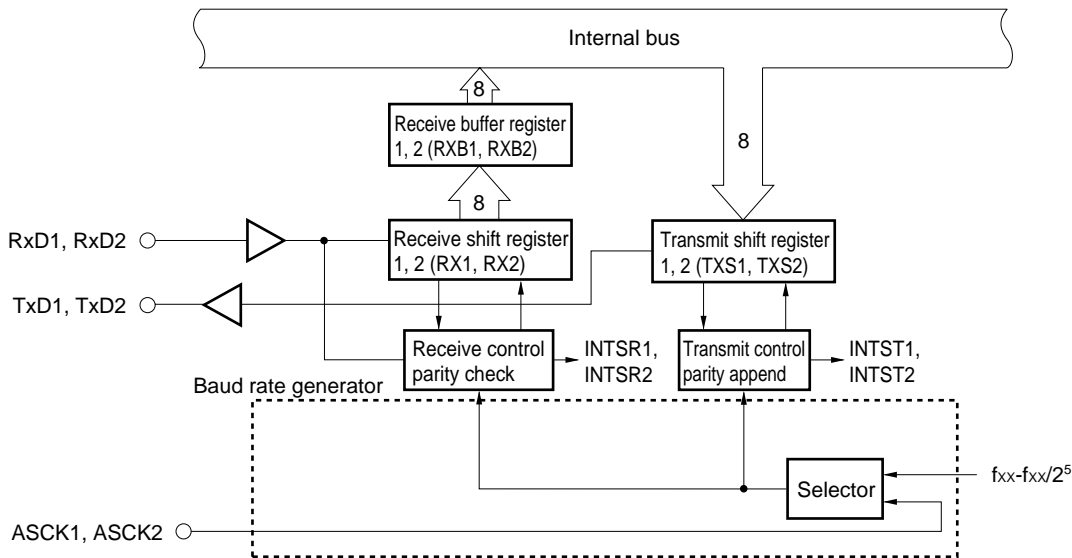
In this mode, data of 1 byte following the start bit is transmitted or received.

Because an on-chip baud rate generator is provided, a wide range of baud rates can be set.

Moreover, the clock input to the ASCK pin can be divided to define a baud rate.

When the baud rate generator is used, a baud rate conforming to the MIDI standard (31.25 kbps) can be also obtained.

★ **Figure 7-10. Block Diagram in Asynchronous Serial Interface Mode**



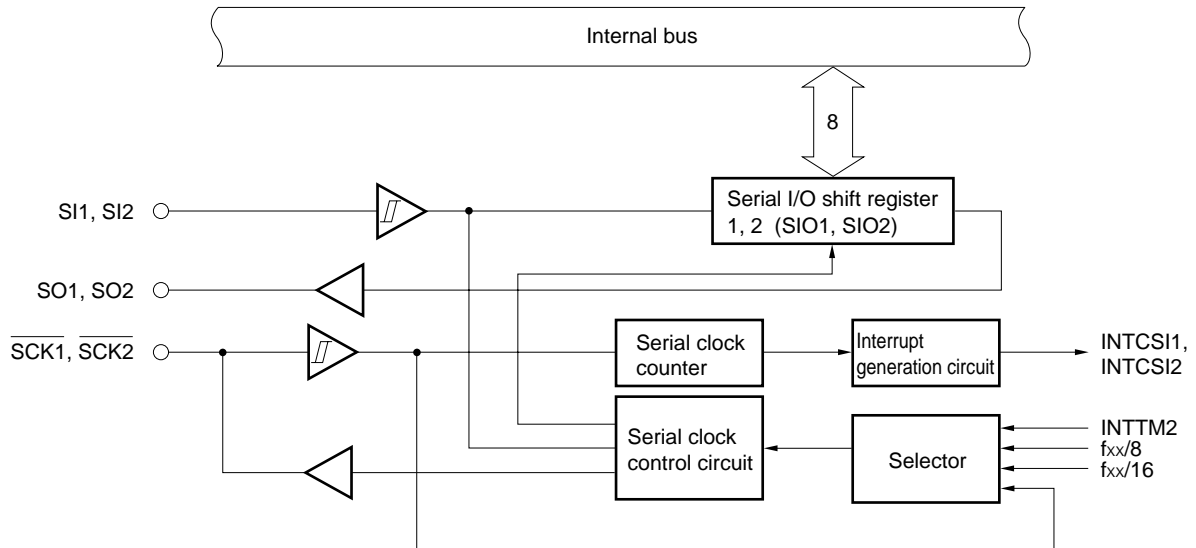
(2) 3-wire serial I/O mode

In this mode, the master device starts transfer by making the serial clock active and transfers 1-byte data in synchronization with this clock.

This mode is used to communicate with a device having the conventional clocked serial interface. Basically, communication is established by using three lines: serial clocks ($\overline{SCK1}$ and $\overline{SCK2}$), serial data inputs (SI1 and SI2), and serial data outputs (SO1 and SO2). To connect two or more devices, a handshake line is necessary.

★

Figure 7-11. Block Diagram in 3-wire Serial I/O Mode



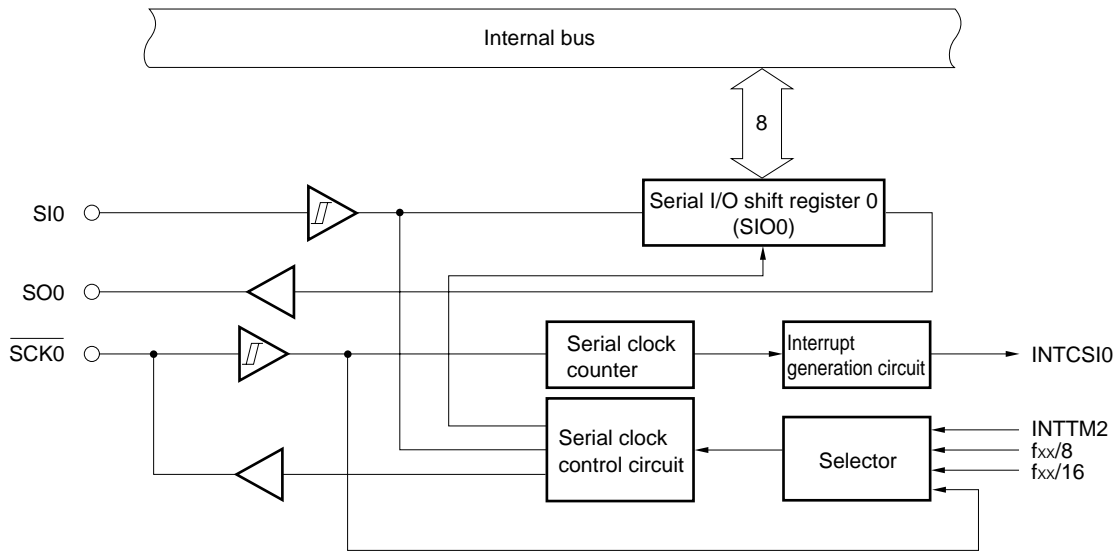
7.7.2 Clocked serial interface (CSI)

In this mode, the master device starts transfer by making the serial clock active and communicates 1-byte data in synchronization with this clock.

(1) 3-wire serial I/O mode

This mode is to communicate with devices having the conventional clocked serial interface. Basically, communication is established in this mode with three lines: one serial clock ($\overline{\text{SCK0}}$) and two serial data (SI0 and SO0) lines. Generally, a handshake line is necessary to check the reception status.

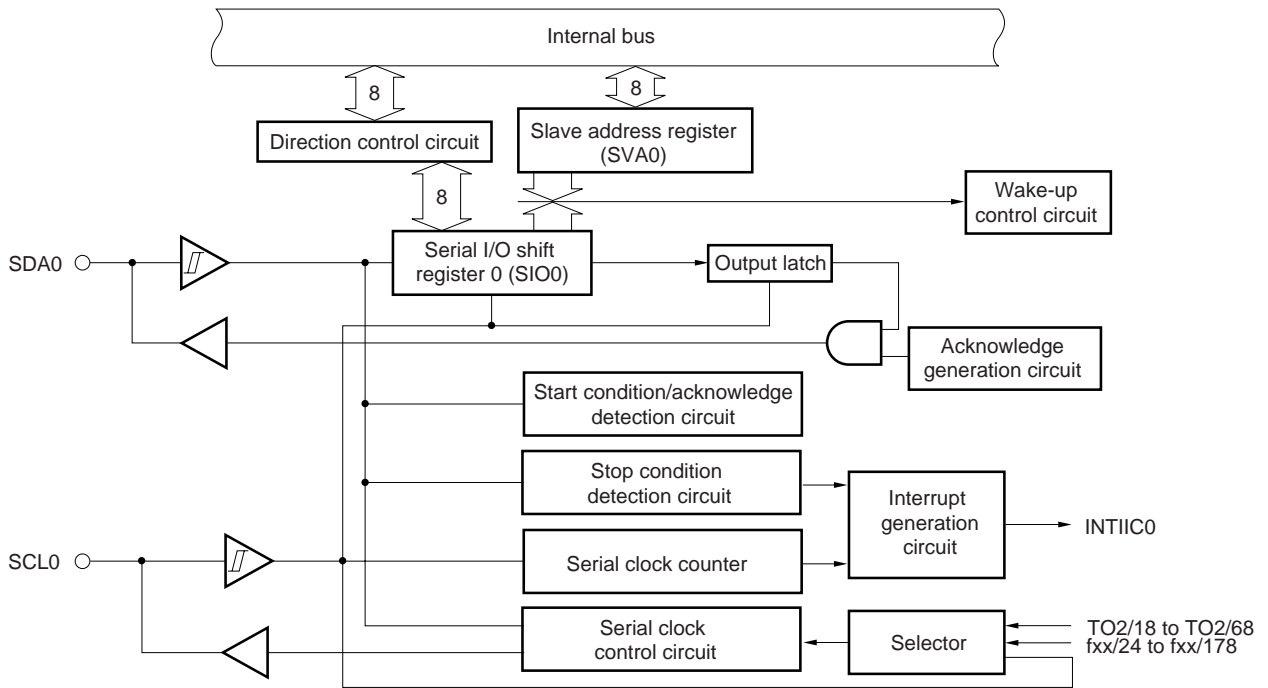
★ **Figure 7-12. Block Diagram in 3-wire Serial I/O Mode**



(2) I²C bus (Inter IC) bus mode (supporting multi-master)

This mode is for communication with devices conforming to the I²C bus format. This mode is for transferring 8-bit data between two or more devices by using two lines: a serial clock (SCL0) and a serial data bus (SDA0). During transfer, a "start condition", "data", and "stop condition" can be output onto the serial data bus. During reception, these data are automatically detected by hardware.

Figure 7-13. Block Diagram of I²C Bus Mode

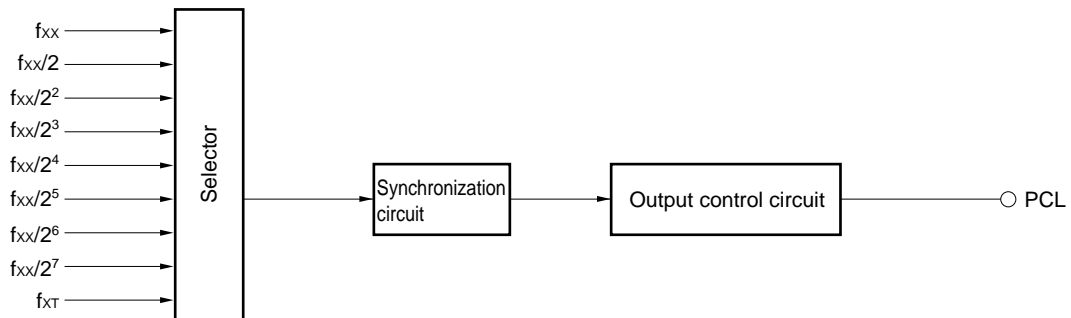


7.8 Clock Output Function

Clocks of the following frequencies can be output as clock output.

- 97.7 kHz/195 kHz/391 kHz/781 kHz/1.56 MHz/3.13 MHz/6.25 MHz/12.5 MHz (@ 12.5-MHz operation with main system clock)
- 32.768 kHz (@ 32.768-kHz operation with subsystem clock)

Figure 7-14. Block Diagram of Clock Output Function

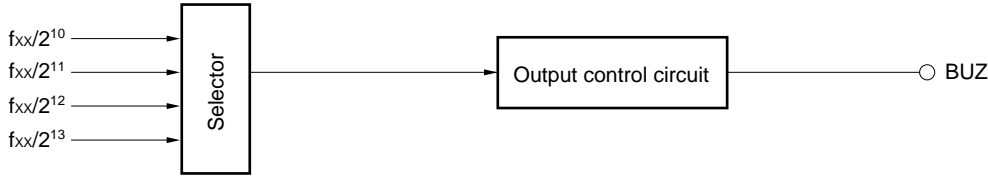


7.9 Buzzer Output Function

Clocks of the following frequencies can be output as buzzer output.

- 1.5 kHz/3.1 kHz/6.1 kHz/12.2 kHz (@ 12.5-MHz operation with main system clock)

Figure 7-15. Block Diagram of Buzzer Output Function



7.10 Edge Detection Function

The interrupt input pins (INTP0, INTP1, NMI/INTP2, INTP3 through INTP6) are used not only to input interrupt requests but also to input trigger signals to the internal hardware units. Because these pins operate at an edge of the input signal, they have a function to detect an edge. Moreover, a noise reduction function is also provided to prevent erroneous detection due to noise.

| Pin Name | Detectable Edge | Noise Reduction |
|---------------------|--|-----------------|
| NMI | Either or both of rising and falling edges | By analog delay |
| INTP0 through INTP6 | | |

7.11 Watch Timer

The watch timer has the following functions:

- Watch timer
- Interval timer

The watch timer and interval timer functions can be used at the same time.

(1) Watch timer

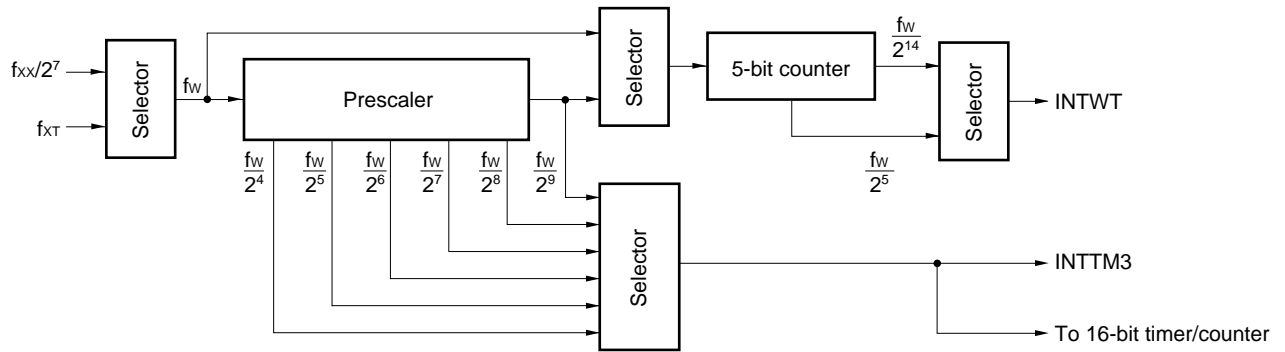
The watch timer sets the WTIF flag of the interrupt control register (WTIC) at time intervals of 0.5 seconds by using the 32.768-kHz subsystem clock.

(2) Interval timer

The interval timer generates an interrupt request (INTTM3) at predetermined time intervals.

★

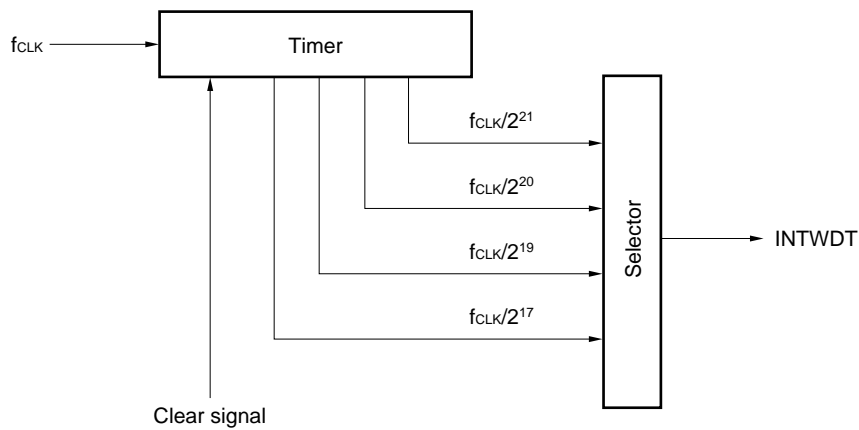
Figure 7-16. Block Diagram of Watch Timer



7.12 Watchdog Timer

A watchdog timer is provided to detect a CPU runaway. This watchdog timer generates a non-maskable or maskable interrupt unless it is cleared by software within a specified interval time. Once enabled to operate, the watchdog timer cannot be stopped by software. Whether the interrupt by the watchdog timer or the interrupt input from the NMI pin takes precedence can be specified.

Figure 7-17. Block Diagram of Watchdog Timer



Remark f_{CLK} : Internal system clock (f_{xx} to $f_{xx}/8$)

8. INTERRUPT FUNCTION

As the servicing in response to an interrupt request, the three types shown in Table 8-1 can be selected by program.

Table 8-1. Servicing of Interrupt Request

| Servicing Mode | Entity of Servicing | Servicing | Contents of PC and PSW |
|--------------------|---------------------|--|---|
| Vectored interrupt | Software | Branches and executes servicing routine (servicing is arbitrary) | Saves to and restores from stack |
| Context switching | | Automatically switches register bank, branches and executes servicing routine (servicing is arbitrary) | Saves to or restores from fixed area in register bank |
| Macro service | Firmware | Executes data transfer between memory and I/O (servicing is fixed) | Retained |

8.1 Interrupt Sources

Table 8-2 shows the interrupt sources available. As shown, interrupts are generated by 29 types of sources, execution of the BRK instruction, BRKCS instruction, or an operand error.

The priority of interrupt servicing can be set to four levels, so that nesting can be controlled during interrupt servicing and that which of the two or more interrupts that simultaneously occur should be serviced first. When the macro service function is used, however, nesting always proceeds.

The default priority is the priority (fixed) of the service that is performed if two or more interrupt requests, having the same priority, simultaneously generate (refer to **Table 8-2**).

Table 8-2. Interrupt Sources

| Type | Default Priority | Source | | Internal/ External | Macro Service |
|--------------------|------------------|---|---|--------------------|---------------|
| | | Name | Trigger | | |
| ★ ★ Software | — | BRK instruction | Instruction execution | — | — |
| | | BRKCS instruction | Instruction execution | | |
| | | Operand error | If result of exclusive OR between operands byte and byte is not FFH when MOV STBC, #byte instruction, MOV WDM, #byte instruction, or LOCATION instruction is executed | | |
| Non-maskable | — | NMI | Pin input edge detection | External | — |
| | | INTWDT | Overflow of watchdog timer | Internal | |
| Maskable | 0 (highest) | INTWDTM | Overflow of watchdog timer | Internal | √ |
| | 1 | INTP0 | Pin input edge detection | External | |
| | 2 | INTP1 | | | |
| | 3 | INTP2 | | | |
| | 4 | INTP3 | | | |
| | 5 | INTP4 | | | |
| | 6 | INTP5 | | | |
| | 7 | INTP6 | | | |
| | 8 | INTIIC0 | End of I ² C bus transfer by CSI0 | Internal | |
| | | INTCSI0 | End of 3-wire transfer by CSI0 | | |
| | 9 | INTSER1 | Occurrence of UART reception error in ASI1 | | |
| | 10 | INTSR1 | End of UART reception by ASI1 | | |
| | | INTCSI1 | End of 3-wire transfer by CSI1 | | |
| | 11 | INTST1 | End of UART transmission by ASI1 | | |
| | 12 | INTSER2 | Occurrence of UART reception error in ASI2 | | |
| | 13 | INTSR2 | End of UART reception by ASI2 | | |
| | | INTCSI2 | End of 3-wire transfer by CSI2 | | |
| | 14 | INTST2 | End of UART transmission by ASI2 | | |
| | 15 | INTTM3 | Reference time interval signal from watch timer | | |
| | 16 | INTTM00 | Signal indicating coincidence between 16-bit timer register and capture/compare register (CR00) | | |
| | | | Signal indicating coincidence between 16-bit timer register and capture/compare register (CR01) | | |
| | 17 | INTTM01 | Signal indicating coincidence between 16-bit timer register and capture/compare register (CR01) | | |
| | 18 | INTTM1 | Occurrence of coincidence signal of 8-bit timer/counter 1 | | |
| | 19 | INTTM2 | Occurrence of coincidence signal of 8-bit timer/counter 2 | | |
| | 20 | INTAD | End of conversion by A/D converter | | |
| | 21 | INTTM5 | Occurrence of coincidence signal of 8-bit timer/counter 5 | | |
| | 22 | INTTM6 | Occurrence of coincidence signal of 8-bit timer/counter 6 | | |
| 23 | INTTM7 | Occurrence of coincidence signal of 8-bit timer/counter 7 | | | |
| 24 | INTTM8 | Occurrence of coincidence signal of 8-bit timer/counter 8 | | | |
| 25 | INTWT | Overflow of watch timer | | | |
| 26 (lowest) | INTKR | Detection of falling edge of port 8 | External | | |

Remark ASI: Asynchronous Serial Interface
 CSI: Clocked Serial Interface

8.2 Vectored Interrupt

Execution branches to a servicing routine by using the memory contents of a vector table address corresponding to the interrupt source as the address of the branch destination.

So that the CPU performs interrupt servicing, the following operations are performed:

- On branching: Saves the status of the CPU (contents of PC and PSW) to stack
- On returning: Restores the status of the CPU (contents of PC and PSW) from stack

To return to the main routine from an interrupt service routine, the RETI instruction is used. The branch destination address is in a range of 0 to FFFFH.

Table 8-3. Vector Table Address

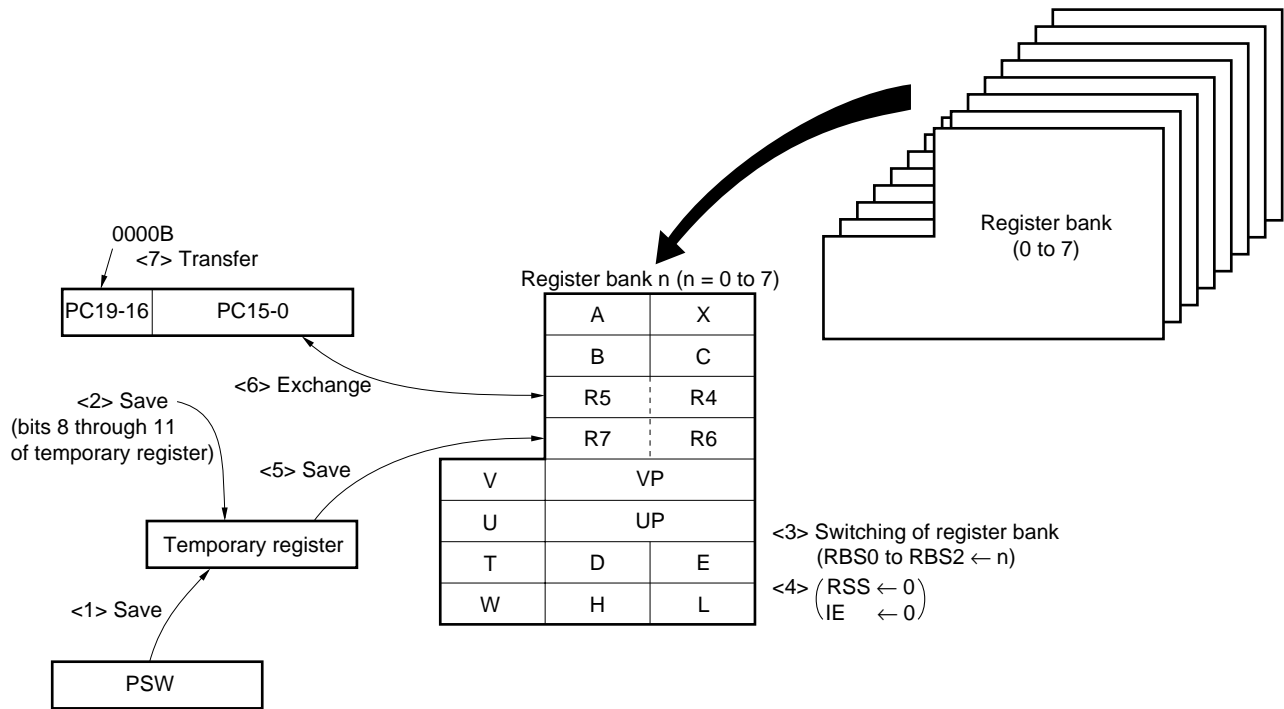
| Interrupt Source | Vector Table Address | Interrupt Source | Vector Table Address |
|-------------------------|----------------------|------------------|----------------------|
| BRK instruction | 003EH | INTST1 | 001CH |
| ★ TRAP0 (operand error) | 003CH | INTSER2 | 001EH |
| NMI | 0002H | INSR2 | 0020H |
| INTWDT (non-maskable) | 0004H | INTCSI2 | |
| INTWDTM (maskable) | 0006H | INTST2 | 0022H |
| INTP0 | 0008H | INTTM3 | 0024H |
| INTP1 | 000AH | INTTM00 | 0026H |
| INTP2 | 000CH | INTTM01 | 0028H |
| INTP3 | 000EH | INTTM1 | 002AH |
| INTP4 | 0010H | INTTM2 | 002CH |
| INTP5 | 0012H | INTAD | 002EH |
| INTP6 | 0014H | INTTM5 | 0030H |
| INTIIC0 | 0016H | INTTM6 | 0032H |
| INTCSI0 | | INTTM7 | 0034H |
| INTSER0 | 0018H | INTTM8 | 0036H |
| INTSR1 | 001AH | INTWT | 0038H |
| INTCSI1 | | INTKR | 003AH |

8.3 Context Switching

When an interrupt request is generated or when the BRKCS instruction is executed, a predetermined register bank is selected by hardware. Context switching is a function that branches execution to a vector address stored in advance in the register bank, and to stack the current contents of the program counter (PC) and program status word (PSW) to the register bank.

The branch address is in a range of 0 to FFFFH.

Figure 8-1. Context Switching Operation When Interrupt Request Is Generated

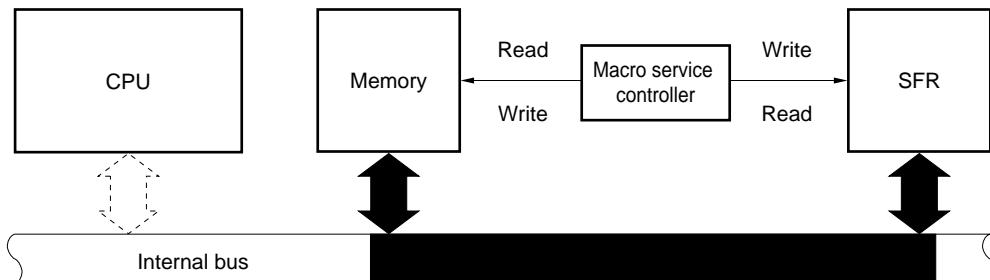


8.4 Macro Service

This function is to transfer data between memory and a special function register (SFR) without intervention by the CPU. A macro service controller accesses the memory and SFR in the same transfer cycle and directly transfers data without loading it.

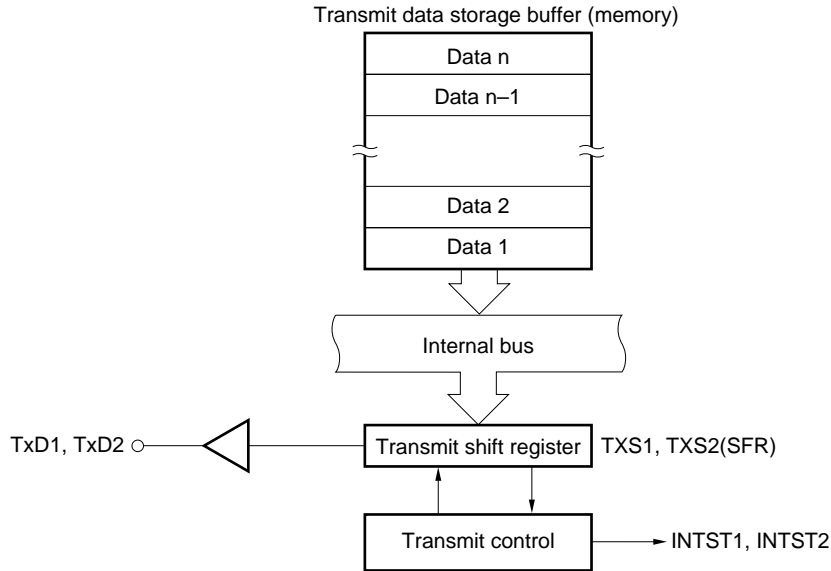
Because this function does not save or restore the status of the CPU, or load data, data can be transferred at high speeds.

Figure 8-2. Macro Service



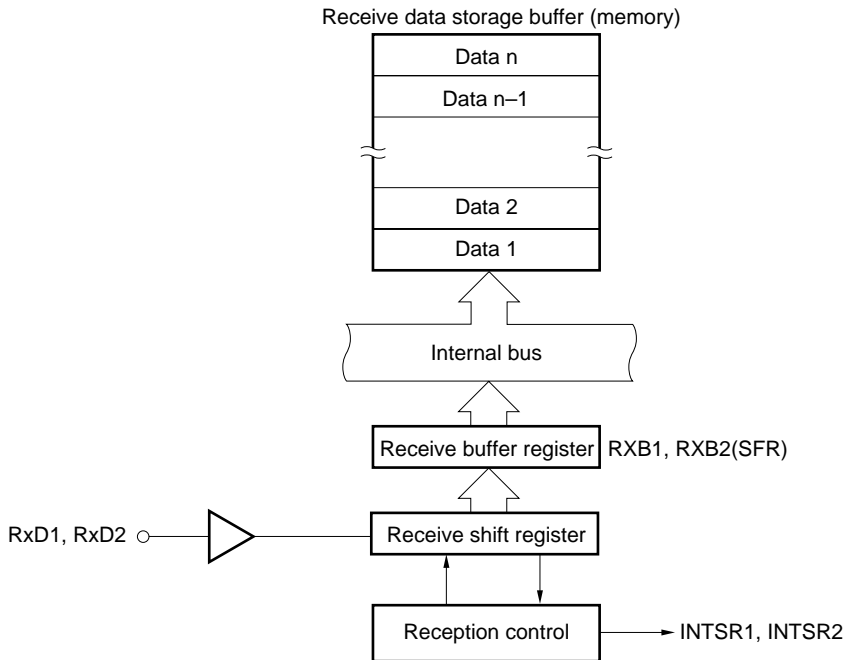
8.5 Application Example of Macro Service

(1) Transmission of serial interface



Each time macro service requests INTST1 and INTST2 are generated, the next transmit data is transferred from memory to TXS1 and TXS2. When data n (last byte) has been transferred to TXS1 and TXS2 (when the transmit data storage buffer has become empty), vectored interrupt requests INTST1 and INTST2 are generated.

(2) Reception of serial interface



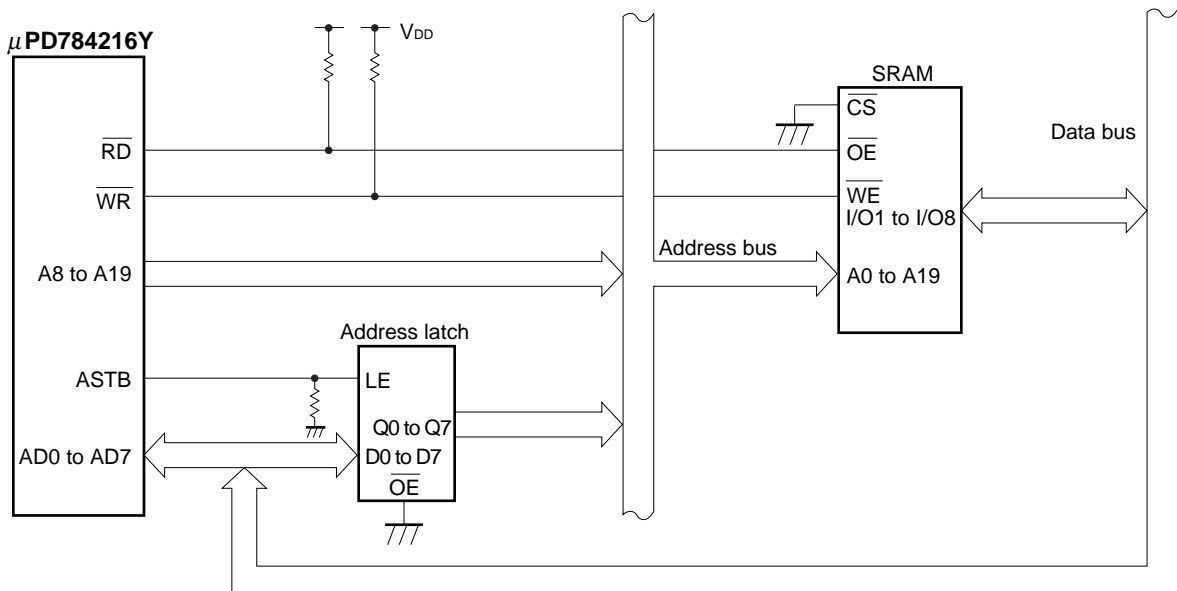
Each time macro service requests INTSR1 and INTSR2 are generated, the receive data is transferred from RXB1 and RXB2 to memory. When data n (last byte) has been transferred to memory (when the receive data storage buffer has become full), vectored interrupt requests INTSR1 and INTSR2 are generated.

9. LOCAL BUS INTERFACE

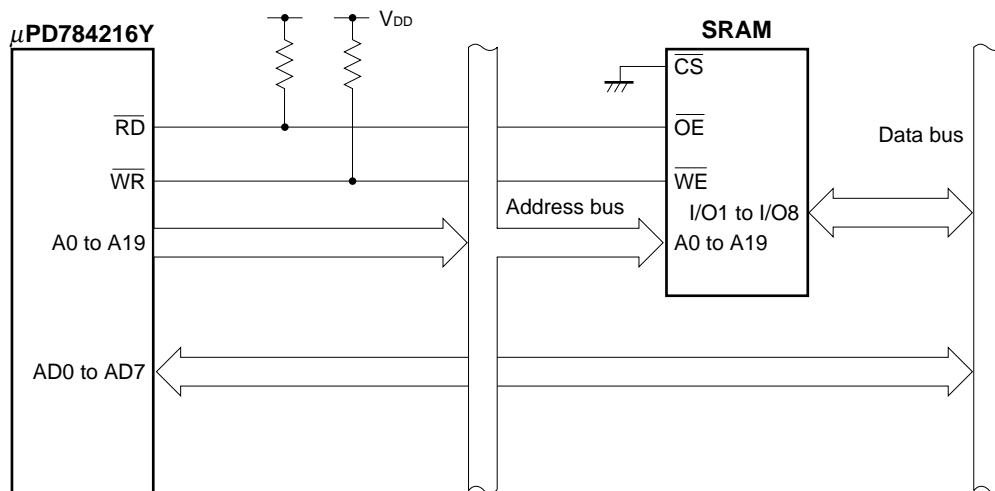
The local bus interface can connect an external memory or I/O (memory mapped I/O) and support a memory space of 1 Mbyte (refer to Figure 9-1).

Figure 9-1. Example of Local Bus Interface

(a) Multiplexed bus mode



(b) Separate bus mode



9.1 Memory Expansion

External program memory and data memory can be connected in two stages: 256 Kbytes and 1 Mbytes.

To connect the external memory, ports 4 through 6 and port 8 are used.

The external memory can be connected in the following two modes:

- Multiplexed bus mode: The external memory is connected by using a time-division address/data bus. The number of ports used when the external memory is connected can be reduced in this mode.
- Separate bus mode: The external memory is connected by using an address bus and data bus independent of each other. Because an external latch circuit is not necessary, this mode is useful for reducing the number of components and mounting area on the printed wiring board.

9.2 Programmable Wait

Wait state(s) can be inserted to the memory space (00000H through FFFFFH) while the \overline{RD} and \overline{WR} signals are active.

In addition, there is an address wait function that extends the active period of the ASTB signal to gain the address decode time.

10. STANDBY FUNCTION

This function is to reduce the power consumption of the chip, and can be used in the following modes:

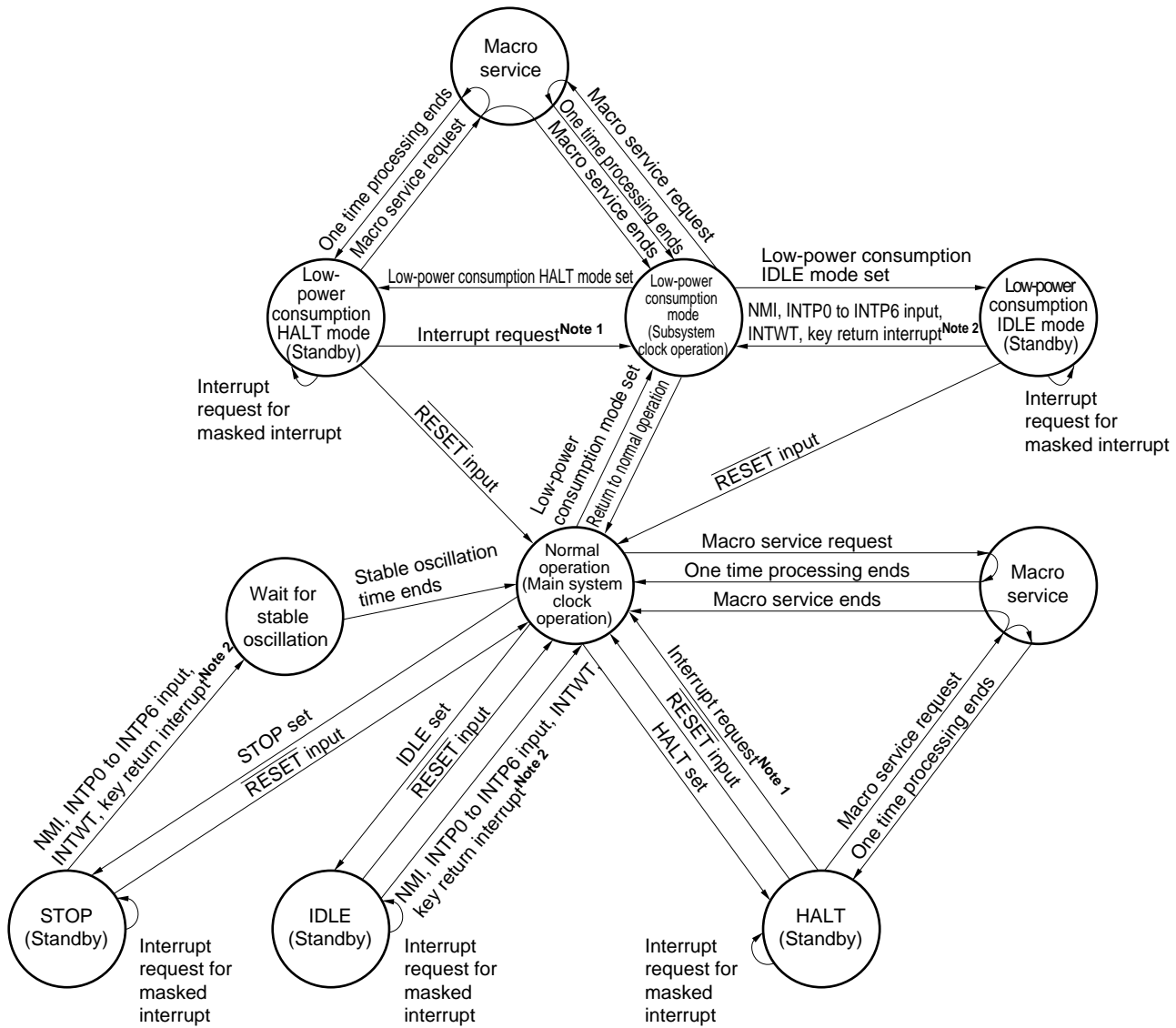
- HALT mode: Stops supply of the operating clock to the CPU. This mode is used in combination with the normal operation mode for intermittent operation to reduce the average power consumption.
- IDLE mode: Stops the entire system with the oscillator continuing operation. The power consumption in this mode is close to that in the STOP mode. However, the time required to restore the normal program operation from this mode is almost the same as that from the HALT mode.
- STOP mode: Stops the main system clock and thereby to stop all the internal operations of the chip. Consequently, the power consumption is minimized with only leakage current flowing.
- Low-power consumption mode: The main system clock is stopped with the subsystem clock used as the system clock. The CPU can operate on the subsystem clock to reduce the current consumption.
- Low-power consumption HALT mode: This is a standby function in the low-power consumption mode and stops the operation clock of the CPU, to reduce the power consumption of the entire system.
- Low-power consumption IDLE mode: This is a standby function in the low-power consumption mode and stops the entire system except the oscillator, to reduce the power consumption of the entire system.

These modes are programmable.

- ★ The macro service can be started from the HALT mode or low-power consumption HALT mode. After macro service processing is executed, the system returns to the HALT mode again.
The transition of the standby status is shown in Figure 10-1.

★

Figure 10-1. Standby Function State Transitions



- Notes**
1. Only unmasked interrupt requests
 2. Only unmasked INTP0 to INTP6, INTWT, key return interrupt (P80 to P87)

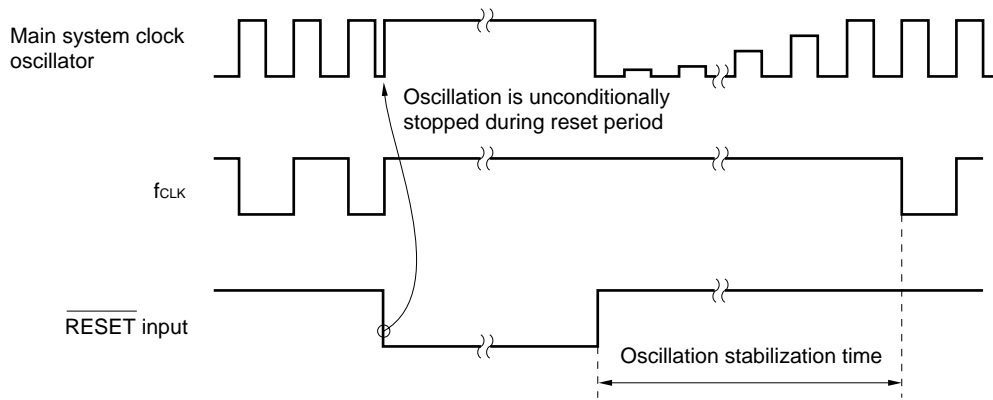
Remark NMI is valid only for an external input.
The watchdog timer cannot be used for the release of standby (HALT mode/STOP mode/IDLE mode).

11. RESET FUNCTION

When a low-level signal is input to the $\overline{\text{RESET}}$ pin, the system is reset, and each hardware unit is initialized (reset). During the reset period, oscillation of the main system clock is unconditionally stopped. Consequently, the current consumption of the entire system can be reduced.

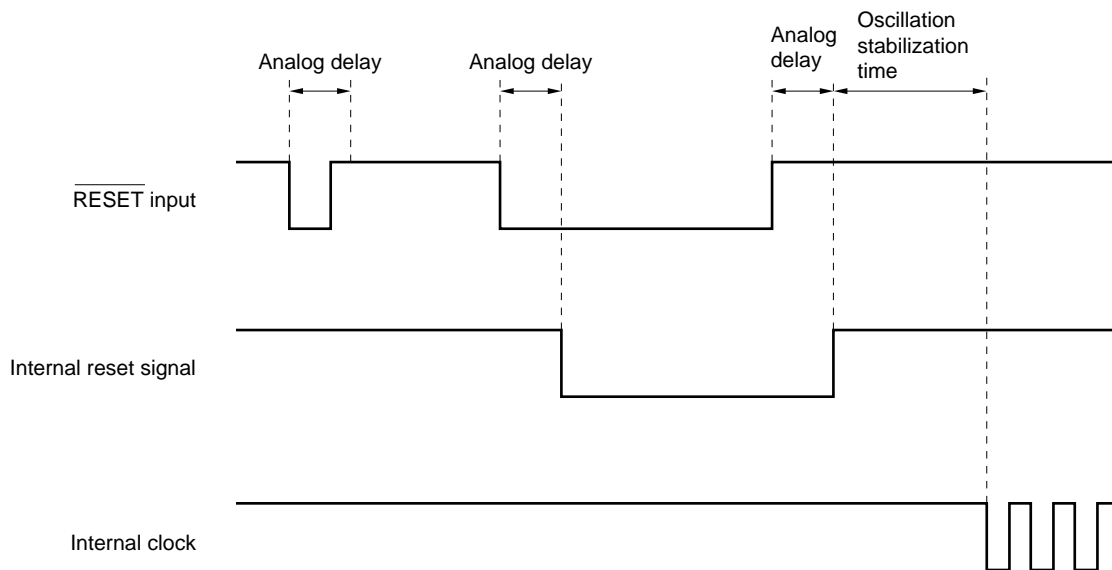
- ★ When the $\overline{\text{RESET}}$ signal goes high, the reset status is cleared, oscillation stabilization time (84.0 ms at 12.5-MHz operation) elapses, the contents of the reset vector table are set to the program counter (PC), execution branches to an address set to the PC, and program execution is started from that branch address. Therefore, the program can be reset and started from any address.

Figure 11-1. Oscillation of Main System Clock during Reset Period



The $\overline{\text{RESET}}$ input pin has an analog delay noise elimination circuit to prevent malfunctioning due to noise.

Figure 11-2. Acknowledgement of Reset Signal



12. INSTRUCTION SET

- (1) 8-bit instructions (The instructions in parentheses are combinations realized by describing A as r)
 MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, SHR, SHL, ROR4, ROL4, DBNZ, PUSH, POP, MOV_M, XCH_M, CMP_{ME}, CMP_{MNE}, CMP_{MNC},
 ★ CMP_{MC}, MOV_{BK}, XCH_{BK}, CMP_{BKE}, CMP_{BKNE}, CMP_{BKNC}, CMP_{BKC}

Table 12-1. Instruction List by 8-Bit Addressing

| Second Operand First Operand | #byte | A | r r' | saddr saddr' | sfr | !addr16 !!addr24 | mem [saddrp] [%saddrg] | r3 PSWL PSWH | [WHL+] [WHL-] | n | None ^{Note 2} |
|---------------------------------|--------------------------------|--|---------------------------------------|--|---|---|-------------------------------------|--------------------|---|-----------------------|-----------------------------|
| A | (MOV) ADD ^{Note 1} | (MOV) (XCH) (ADD) ^{Note 1} | MOV XCH (ADD) ^{Note 1} | (MOV) ^{Note 6} (XCH) ^{Note 6} (ADD) ^{Notes 1,6} | MOV (XCH) (ADD) ^{Note 1} | (MOV) (XCH) ADD ^{Note 1} | MOV XCH ADD ^{Note 1} | MOV | (MOV) (XCH) (ADD) ^{Note 1} | | |
| r | MOV ADD ^{Note 1} | (MOV) (XCH) (ADD) ^{Note 1} | MOV XCH ADD ^{Note 1} | MOV XCH ADD ^{Note 1} | MOV XCH ADD ^{Note 1} | MOV XCH | | | | ROR ^{Note 3} | MULU DIVUW INC DEC |
| saddr | MOV ADD ^{Note 1} | (MOV) ^{Note 6} (ADD) ^{Note 1} | MOV ADD ^{Note 1} | MOV XCH ADD ^{Note 1} | | | | | | | INC DEC DBNZ |
| ★ sfr | MOV ADD ^{Note 1} | MOV (ADD) ^{Note 1} | MOV ADD ^{Note 1} | | | | | | | | PUSH POP |
| !addr16 !!addr24 | MOV | (MOV) ADD ^{Note 1} | MOV | | | | | | | | |
| mem [saddrp] [%saddrg] | | MOV ADD ^{Note 1} | | | | | | | | | |
| mem3 | | | | | | | | | | | ROR4 ROL4 |
| r3 PSWL PSWH | MOV | MOV | | | | | | | | | |
| B, C | | | | | | | | | | | DBNZ |
| STBC, WDM | MOV | | | | | | | | | | |
| [TDE+] [TDE-] | | (MOV) (ADD) ^{Note 1} MOV _M ^{Note 4} | | | | | | | MOV _{BK} ^{Note 5} | | |

- Notes**
1. The operands of ADDC, SUB, SUBC, AND, OR, XOR, and CMP are the same as that of ADD.
 2. Either the second operand is not used, or the second operand is not an operand address.
 3. The operands of ROL, RORC, ROLC, SHR, and SHL are the same as that of ROR.
 4. The operands of XCH_M, CMP_{ME}, CMP_{MNE}, CMP_{MNC}, and CMP_{MC} are the same as that of MOV_M.
 5. The operands of XCH_{BK}, CMP_{BKE}, CMP_{BKNE}, CMP_{BKNC}, and CMP_{BKC} are the same as that of MOV_{BK}.
 6. The code length of some instructions having saddr2 as saddr in this combination is short.

(2) 16-bit instructions (The instructions in parentheses are combinations realized by describing AX as rp)

MOVW, XCHW, ADDW, SUBW, CMPW, MULUW, MULW, DIVUX, INCW, DECW, SHRW, SHLW, PUSH, POP, ADDWG, SUBWG, PUSHU, POPU, MOVTLBW, MACW, MACSW, SACW

Table 12-2. Instruction List by 16-Bit Addressing

| Second Operand First Operand | #word | AX | rp rp' | saddrp saddrp' | sfrp | !addr16 !!addr24 | mem [saddrp] [%saddrg] | [WHL+] | byte | n | None ^{Note 2} |
|---------------------------------|----------------------------------|--|--|--|--|---------------------|------------------------------|------------------|---------|--------------|--|
| AX | (MOVW) ADDW ^{Note 1} | (MOVW) (XCHW) (ADD) ^{Note 1} | (MOVW) (XCHW) (ADDW) ^{Note 1} | (MOVW) ^{Note 3} (XCHW) ^{Note 3} (ADDW) ^{Note 1,3} | MOVW (XCHW) (ADDW) ^{Note 1} | (MOVW) XCHW | MOVW XCHW | (MOVW) (XCHW) | | | |
| rp | MOVW ADDW ^{Note 1} | (MOVW) (XCHW) (ADDW) ^{Note 1} | MOVW XCHW ADDW ^{Note 1} | MOVW XCHW ADDW ^{Note 1} | MOVW XCHW ADDW ^{Note 1} | MOVW | | | | SHRW SHLW | MULW ^{Note 4} INCW DECW |
| saddrp | MOVW ADDW ^{Note 1} | (MOVW) ^{Note 3} (ADDW) ^{Note 1} | MOVW ADDW ^{Note 1} | MOVW XCHW ADDW ^{Note 1} | | | | | | | INCW DECW |
| sfrp | MOVW ADDW ^{Note 1} | (MOVW) (ADDW) ^{Note 1} | MOVW ADDW ^{Note 1} | | | | | | | | PUSH POP |
| !addr16 !!addr24 | MOVW | (MOVW) | MOVW | | | | | | MOVTLBW | | |
| mem [saddrp] [%saddrg] | | MOVW | | | | | | | | | |
| PSW | | | | | | | | | | | PUSH POP |
| SP | ADDWG SUBWG | | | | | | | | | | |
| post | | | | | | | | | | | PUSH POP PUSHU POPU |
| [TDE+] | | (MOVW) | | | | | | SACW | | | |
| byte | | | | | | | | | | | MACW MACSW |

- Notes**
1. The operands of SUBW and CMPW are the same as that of ADDW.
 2. Either the second operand is not used, or the second operand is not an operand address.
 3. The code length of some instructions having saddrp2 as saddrp in this combination is short.
 4. The operands of MULUW and DIVUX are the same as that of MULW.

(3) 24-bit instructions (The instructions in parentheses are combinations realized by describing WHL as rg)

MOVG, ADDG, SUBG, INCG, DECG, PUSH, POP

Table 12-3. Instruction List by 24-Bit Addressing

| Second Operand First Operand | #imm24 | WHL | rg rg' | saddrg | !!addr24 | mem1 | [%saddrg] | SP | None Note |
|---------------------------------|----------------------------|----------------------------|----------------------------|------------------------|----------|------|-----------|------|-----------------------------|
| WHL | (MOVG) (ADDG) (SUBG) | (MOVG) (ADDG) (SUBG) | (MOVG) (ADDG) (SUBG) | (MOVG) ADDG SUBG | (MOVG) | MOVG | MOVG | MOVG | |
| rg | MOVG ADDG SUBG | (MOVG) (ADDG) (SUBG) | MOVG ADDG SUBG | MOVG | MOVG | | | | INCG DECG PUSH POP |
| saddrg | | (MOVG) | MOVG | | | | | | |
| !!addr24 | | (MOVG) | MOVG | | | | | | |
| mem1 | | MOVG | | | | | | | |
| [%saddrg] | | MOVG | | | | | | | |
| SP | MOVG | MOVG | | | | | | | INCG DECG |

Note Either the second operand is not used, or the second operand is not an operand address.

(4) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR, BFSET

Table 12-4. Instruction List by Bit Manipulation Instruction Addressing

| Second Operand First Operand | CY | saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit | /saddr.bit /sfr. bit /A.bit /X.bit /PSWL.bit /PSWH.bit /mem2.bit /!addr16.bit /!!addr24.bit | None Note |
|---|------|---|---|--|
| CY | | MOV1 AND1 OR1 XOR1 | AND1 OR1 | NOT1 SET1 CLR1 |
| saddr.bit sfr.bit A.bit X.bit PSWL.bit PSWH.bit mem2.bit !addr16.bit !!addr24.bit | MOV1 | | | NOT1 SET1 CLR1 BF BT BTCLR BFSET |

Note Either the second operand is not used, or the second operand is not an operand address.

(5) Call and return/branch instructions

CALL, CALLF, CALLT, BRK, RET, RETI, RETB, RETCS, RETCSB, BRKCS, BR, BNZ, BNE, BZ, BE, BNC, BNL, BC, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, BH, BF, BT, BTCLR, BFSET, DBNZ

Table 12-5. Instruction List by Call and Return/Branch Instruction Addressing

| Operand of Instruction Address | \$addr20 | !addr20 | !addr16 | !!addr20 | rp | rg | [rp] | [rg] | !addr11 | [addr5] | RBn | None |
|--------------------------------|------------------------------------|------------|-------------------------------|------------|------------|------------|------------|------------|----------------|---------|-------|----------------------------|
| Basic instruction | BC ^{Note} BR | CALL BR | CALL BR RETCS RETCSB | CALL BR | CALL BR | CALL BR | CALL BR | CALL BR | CALLF CALLF | | BRKCS | BRK RET RETI RETB |
| Compound instruction | BF BT BTCLR BFSET DBNZ | | | | | | | | | | | |

Note The operands of BNZ, BNE, BZ, BE, BNC, BNL, BL, BNV, BPO, BV, BPE, BP, BN, BLT, BGE, BLE, BGT, BNH, and BH are the same as that of BC.

(6) Other instructions

ADJBA, ADJBS, CVTBW, LOCATION, SEL, NOT, EI, DI, SWRS

★ 13. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

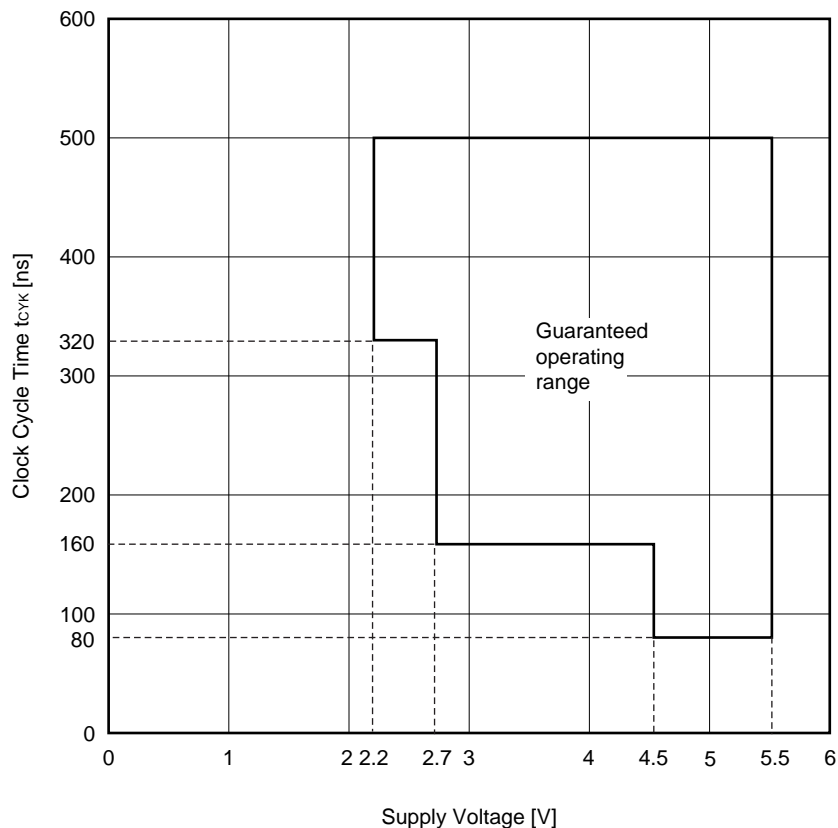
| Parameter | Symbol | Conditions | Ratings | Unit |
|-------------------------------|--------------------|---------------------------------------|--|------|
| Supply voltage | V _{DD} | | -0.3 to +6.5 | V |
| | AV _{DD} | | -0.3 to V _{DD} + 0.3 | V |
| | AV _{SS} | | -0.3 to V _{SS} + 0.3 | V |
| | AV _{REF0} | A/D converter reference voltage input | -0.3 to V _{DD} + 0.3 | V |
| | AV _{REF1} | D/A converter reference voltage input | -0.3 to V _{DD} + 0.3 | V |
| Input voltage | V _{I1} | Other than P90 to P95 | -0.3 to V _{DD} + 0.3 | V |
| | V _{I2} | P90 to P95 N-ch open drain | -0.3 to +12 | V |
| Analog input voltage | V _{AN} | Analog input pin | AV _{SS} - 0.3 to AV _{REF0} + 0.3 | V |
| Output voltage | V _O | | -0.3 to V _{DD} + 0.3 | V |
| Output current, low | I _{OL} | Per pin | 15 | mA |
| | | Total of P2, P4 to P8 | 75 | mA |
| | | Total of P0, P3, P9, P10, P12, P13 | 75 | mA |
| Output current, high | I _{OH} | Per pin | -10 | mA |
| | | Total of P2, P4 to P8 | -50 | mA |
| | | Total of P0, P3, P9, P10, P12, P13 | -50 | mA |
| Operating ambient temperature | T _A | | -40 to +85 | °C |
| Storage temperature | T _{stg} | | -65 to +150 | °C |

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Operating Conditions

- Operating ambient temperature (T_A): -40 to +85°C
- Power supply voltage and clock cycle time: see **Figure 13-1**

Figure 13-1. Power Supply Voltage and Clock Cycle Time



CAPACITANCE (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|--------------------|-----------------|--|-------------------|------|------|------|----|
| Input capacitance | C _i | f = 1 MHz Unmeasured pins returned to 0 V. | Other than Port 9 | | | 15 | pF |
| | | | Port 9 | | | 20 | pF |
| Output capacitance | C _o | f = 1 MHz Unmeasured pins returned to 0 V. | Other than Port 9 | | | 15 | pF |
| | | | Port 9 | | | 20 | pF |
| I/O capacitance | C _{io} | f = 1 MHz Unmeasured pins returned to 0 V. | Other than Port 9 | | | 15 | pF |
| | | | Port 9 | | | 20 | pF |

Main System Clock Oscillator Characteristics (T_A = -40 to +85°C)

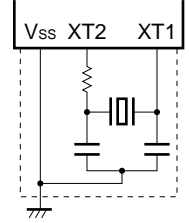
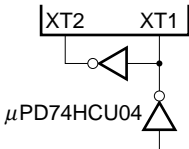
| Resonator | Recommended Circuit | Parameter | Test Conditions | MIN. | TYP. | MAX. | Unit |
|--|---------------------|--|---------------------------------|------|------|------|------|
| Ceramic resonator or crystal resonator | | Oscillation frequency (f _x) | 4.5 V ≤ V _{DD} ≤ 5.5 V | 2 | | 12.5 | MHz |
| | | | 2.7 V ≤ V _{DD} < 4.5 V | 2 | | 6.25 | |
| | | | 2.2 V ≤ V _{DD} < 2.7 V | 2 | | 3 | |
| External clock | | X1 input frequency (f _x) | 4.5 V ≤ V _{DD} ≤ 5.5 V | 2 | | 25 | MHz |
| | | | 2.7 V ≤ V _{DD} < 4.5 V | 2 | | 12.5 | |
| | | | 2.2 V ≤ V _{DD} < 2.7 V | 2 | | 6.25 | |
| | | X1 input high/low-level width (t _{wXH} , t _{wXL}) | | 35 | | 250 | ns |
| | | X1 input rising/falling time (t _{xR} , t _{xF}) | 4.5 V ≤ V _{DD} ≤ 5.5 V | 0 | | 5 | ns |
| | | | 2.7 V ≤ V _{DD} < 4.5 V | 0 | | 10 | |
| 2.2 V ≤ V _{DD} < 2.7 V | 0 | | | 20 | | | |

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always keep the ground point of the oscillator capacitor the same potential as V_{SS}.
- Do not ground the capacitor to a ground pattern in which a high current flows.
- Do not fetch signals from the oscillator.

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched back to the main system clock after the oscillation stabilization time is secured by the program.

Subsystem Clock Oscillator Characteristics (T_A = -40 to +85°C)

| Resonator | Recommended Circuit | Parameter | Test Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------|---|---|---------------------------------|------|--------|------|------|
| Crystal resonator |  | Oscillation frequency (f _{XT}) | | 32 | 32.768 | 35 | kHz |
| | | Oscillation stabilization time ^{Note} | 4.5 V ≤ V _{DD} ≤ 5.5 V | | 1.2 | 2 | s |
| | | | 2.2 V ≤ V _{DD} < 4.5 V | | | 10 | |
| External clock |  | XT1 input frequency (f _{XT}) | | 32 | | 35 | kHz |
| | | XT1 input high/low-level width (t _{XTH} , t _{XTL}) | | 5 | | 15 | μs |

Note Time required to stabilize oscillation after V_{DD} reaches oscillator voltage MIN.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
 - Do not cross the wiring with the other signal lines.
 - Do not route the wiring near a signal line through which a high fluctuating current flows.
 - Always keep the ground point of the oscillator capacitor the same potential as V_{SS}.
 - Do not ground the capacitor to a ground pattern in which a high current flows.
 - Do not fetch signals from the oscillator.
2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched back to the main system clock after the oscillation stabilization time is secured by the program.

DC Characteristics (T_A = -40 to +85°C, V_{DD} = AV_{DD} = 2.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V) (1/2)

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|------------------------------|-------------------|--|--------------------------------|----------------------|--------------------|------|
| Input voltage, low | V _{IL1} | Note | 0 | | 0.3V _{DD} | V |
| | V _{IL2} | Total of P00 to P06, P20, P22, P33, P34, P70, P72, P100 to P103, $\overline{\text{RESET}}$ | 0 | | 0.2V _{DD} | V |
| | V _{IL3} | P90 to P95 (N-ch open drain) | 0 | | 0.3V _{DD} | V |
| | V _{IL4} | Total of P10 to P17, P130, P131 | 0 | | 0.3V _{DD} | V |
| | V _{IL5} | Total of X1, X2, XT1, XT2 | 0 | | 0.2V _{DD} | V |
| | V _{IL6} | P25, P27 | 0 | | 0.3V _{DD} | V |
| Input voltage, high | V _{IH1} | Note | 0.7V _{DD} | | V _{DD} | V |
| | V _{IH2} | Total of P00 to P06, P20, P22, P33, P34, P70, P72, P100 to P103, $\overline{\text{RESET}}$ | 0.8V _{DD} | | V _{DD} | V |
| | V _{IH3} | P90 to P95 (N-ch open drain) | 0.7V _{DD} | | 12 | V |
| | V _{IH4} | Total of P10 to P17, P130, P131 | 0.7V _{DD} | | V _{DD} | V |
| | V _{IH5} | Total of X1, X2, XT1, XT2 | 0.8V _{DD} | | V _{DD} | V |
| | V _{IH6} | P25, P27 | 0.7V _{DD} | | V _{DD} | V |
| Output voltage, low | V _{OL1} | For pins other than P40 to P47, P50 to P57, P90 to P95 I _{OL} = 1.6 mA | V _{DD} = 4.5 to 5.5 V | | 0.4 | V |
| | | Total of P40 to P47, P50 to P57 I _{OL} = 8 mA | V _{DD} = 4.5 to 5.5 V | | 1.0 | V |
| | | P90 to P95 I _{OL} = 15 mA | V _{DD} = 4.5 to 5.5 V | 0.4 | 2.0 | V |
| | V _{OL2} | I _{OL} = 400 μA | | | 0.5 | V |
| Output voltage, high | V _{OH1} | I _{OH} = -1 mA | V _{DD} = 4.5 to 5.5 V | V _{DD} -1.0 | | V |
| | | I _{OH} = -100 μA | | V _{DD} -0.5 | | V |
| Input leakage current, low | I _{LIL1} | V _{IN} = 0 V | Except X1, X2, XT1, XT2 | | -3 | μA |
| | I _{LIL2} | | | X1, X2, XT1, XT2 | | -20 |
| Input leakage current, high | I _{LIH1} | V _{IN} = V _{DD} | Except X1, X2, XT1, XT2 | | 3 | μA |
| | I _{LIH2} | | | X1, X2, XT1, XT2 | | 20 |
| Output leakage current, low | I _{LOL1} | V _{OUT} = 0 V | | | -3 | μA |
| Output leakage current, high | I _{LOH1} | V _{OUT} = V _{DD} | | | 3 | μA |

Note P21, P23, P24, P26, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P60 to P67, P71, P80 to P87, P120 to P127

DC Characteristics (T_A = -40 to +85°C, V_{DD} = AV_{DD} = 2.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V) (2/2)

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit | |
|------------------------|-----------------------|---|---|------|------|------|----|
| Supply current | I _{DD1} | Operation mode | f _{XX} = 12.5 MHz | | 20 | 40 | mA |
| | | | f _{XX} = 6 MHz, 2.7 V ≤ V _{DD} ≤ 3.3 V | | 8 | 17 | mA |
| | | | f _{XX} = 3 MHz, 2.2 V ≤ V _{DD} < 2.7 V | | 4 | 8 | mA |
| | I _{DD2} | HALT mode | f _{XX} = 12.5 MHz | | 8 | 20 | mA |
| | | | f _{XX} = 6 MHz, 2.7 V ≤ V _{DD} ≤ 3.3 V | | 3 | 8 | mA |
| | | | f _{XX} = 3 MHz, 2.2 V ≤ V _{DD} < 2.7 V | | 1.3 | 3.5 | mA |
| | I _{DD3} | IDLE mode | f _{XX} = 12.5 MHz | | 1 | 2.5 | mA |
| | | | f _{XX} = 6 MHz, 2.7 V ≤ V _{DD} ≤ 3.3 V | | 0.5 | 1.3 | mA |
| | | | f _{XX} = 3 MHz, 2.2 V ≤ V _{DD} < 2.7 V | | 0.3 | 0.9 | mA |
| | I _{DD4} | Operation mode Note | f _{XX} = 32 kHz | | 100 | 200 | μA |
| | | | f _{XX} = 32 kHz, 2.7 V ≤ V _{DD} ≤ 3.3 V | | 55 | 110 | μA |
| | | | f _{XX} = 32 kHz, 2.2 V ≤ V _{DD} < 2.7 V | | 50 | 100 | μA |
| | I _{DD5} | HALT mode Note | f _{XX} = 32 kHz | | 80 | 160 | μA |
| | | | f _{XX} = 32 kHz, 2.7 V ≤ V _{DD} ≤ 3.3 V | | 40 | 80 | μA |
| | | | f _{XX} = 32 kHz, 2.2 V ≤ V _{DD} < 2.7 V | | 35 | 70 | μA |
| I _{DD6} | IDLE mode Note | f _{XX} = 32 kHz | | 75 | 150 | μA | |
| | | f _{XX} = 32 kHz, 2.7 V ≤ V _{DD} ≤ 3.3 V | | 35 | 70 | μA | |
| | | f _{XX} = 32 kHz, 2.2 V ≤ V _{DD} < 2.7 V | | 30 | 60 | μA | |
| Data retention voltage | V _{DDDR} | HALT, IDLE modes | 2.2 | | 5.5 | V | |
| Data retention current | I _{DDDR} | STOP mode | V _{DD} = 2.2 V | | 2 | 10 | μA |
| | | | V _{DD} = 4.5 to 5.5 V | | 10 | 50 | μA |
| Pull-up resistor | R _L | V _{IN} = 0 V | 10 | 30 | 100 | kΩ | |

Note When main system clock is stopped

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics (T_A = -40 to +85°C, V_{DD} = AV_{DD} = 2.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

(1) Read/write operation (1/2)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|--------------------|---------------------------------|----------------------|------|------|------|------|
| Cycle time (Minimum instruction execution time) | t _{CYK} | 4.5 V ≤ V _{DD} ≤ 5.5 V | | 80 | | | ns |
| | | 2.7 V ≤ V _{DD} < 4.5 V | | 160 | | | ns |
| | | 2.2 V ≤ V _{DD} < 2.7 V | | 320 | | | ns |
| Address setup time (to ASTB↓) | t _{SAST} | V _{DD} = 5.0 V | (0.5 + a) T - 11 | 29 | | | ns |
| | | V _{DD} = 3.0 V | (0.5 + a) T - 15 | 65 | | | ns |
| Address hold time (from ASTB↓) | t _{HSTLA} | V _{DD} = 5.0 V | 0.5T - 19 | 21 | | | ns |
| | | V _{DD} = 3.0 V | 0.5T - 24 | 56 | | | ns |
| ASTB high-level width | t _{WSTH} | V _{DD} = 5.0 V | (0.5 + a) T - 17 | 23 | | | ns |
| | | V _{DD} = 3.0 V | (0.5 + a) T - 40 | 40 | | | ns |
| Address hold time (from RD↑) | t _{HRA} | V _{DD} = 5.0 V | 0.5T - 14 | 26 | | | ns |
| | | V _{DD} = 3.0 V | 0.5T - 14 | 66 | | | ns |
| RD↓ delay time from address | t _{DAR} | V _{DD} = 5.0 V | (1 + a) T - 24 | 56 | | | ns |
| | | V _{DD} = 3.0 V | (1 + a) T - 24 | 136 | | | ns |
| Address float time (from RD↓) | t _{FRA} | | | 0 | | | ns |
| Data input time from address | t _{DAID} | V _{DD} = 5.0 V | (2.5 + a + n) T - 37 | | | 403 | ns |
| | | V _{DD} = 3.0 V | (2.5 + a + n) T - 52 | | | 828 | ns |
| Data input time from ASTB↓ | t _{DSTID} | V _{DD} = 5.0 V | (2 + n) T - 35 | | | 285 | ns |
| | | V _{DD} = 3.0 V | (2 + n) T - 50 | | | 590 | ns |
| Data input time from RD↓ | t _{DRID} | V _{DD} = 5.0 V | (1.5 + n) T - 40 | | | 240 | ns |
| | | V _{DD} = 3.0 V | (1.5 + n) T - 50 | | | 510 | ns |
| RD↓ delay time from ASTB↓ | t _{DSTR} | V _{DD} = 5.0 V | 0.5T - 9 | 31 | | | ns |
| | | V _{DD} = 3.0 V | 0.5T - 9 | 71 | | | ns |
| Data hold time (from RD↑) | t _{HRID} | | | 0 | | | ns |
| Address active time from RD↑ | t _{DRA} | V _{DD} = 5.0 V | 0.5T - 2 | 38 | | | ns |
| | | V _{DD} = 3.0 V | 0.5T - 12 | 68 | | | ns |
| ASTB↑ delay time from RD↑ | t _{DRST} | V _{DD} = 5.0 V | 0.5T - 9 | 31 | | | ns |
| | | V _{DD} = 3.0 V | 0.5T - 9 | 71 | | | ns |
| RD low-level width | t _{WRL} | V _{DD} = 5.0 V | (1.5 + n) T - 25 | 95 | | | ns |
| | | V _{DD} = 3.0 V | (1.5 + n) T - 30 | 210 | | | ns |
| WR↓ delay time from address | t _{DAW} | V _{DD} = 5.0 V | (1 + a) T - 24 | 56 | | | ns |
| | | V _{DD} = 3.0 V | (1 + a) T - 24 | 136 | | | ns |
| Address hold time (from WR↑) | t _{HWA} | V _{DD} = 5.0 V | 0.5T - 14 | 26 | | | ns |
| | | V _{DD} = 3.0 V | 0.5T - 14 | 66 | | | ns |
| Data output delay time from ASTB↓ | t _{DSTOD} | V _{DD} = 5.0 V | 0.5T + 15 | | | 55 | ns |
| | | V _{DD} = 3.0 V | 0.5T + 20 | | | 100 | ns |

Remark T: t_{CYK} = 1/f_{XX} (f_{XX}: main system clock frequency)
a: 1 (during address wait), otherwise, 0
n: Number of wait states (n ≥ 0)

AC Characteristics

(1) Read/write operation (2/2)

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|--|-------------|-------------------------|--------------------|------|------|------|------|
| Data output delay time $\overline{WR}\downarrow$ | t_{DWOD} | | | | 10 | 62 | ns |
| $\overline{WR}\downarrow$ delay time from $ASTB\downarrow$ | t_{DSTW} | $V_{DD} = 5.0\text{ V}$ | $0.5T - 9$ | 31 | | | ns |
| | | $V_{DD} = 3.0\text{ V}$ | $0.5T - 9$ | 71 | | | ns |
| Data setup time (to $\overline{WR}\uparrow$) | t_{SODWR} | $V_{DD} = 5.0\text{ V}$ | $(1.5 + n) T - 20$ | 100 | | | ns |
| | | $V_{DD} = 3.0\text{ V}$ | $(1.5 + n) T - 25$ | 215 | | | ns |
| Data hold time (from $\overline{WR}\uparrow$) | t_{HWOD} | $V_{DD} = 5.0\text{ V}$ | $0.5T - 14$ | 26 | | | ns |
| | | $V_{DD} = 3.0\text{ V}$ | $0.5T - 14$ | 66 | | | ns |
| $ASTB\uparrow$ delay time (from $\overline{WR}\uparrow$) | t_{DWST} | $V_{DD} = 5.0\text{ V}$ | $0.5T - 9$ | 31 | | | ns |
| | | $V_{DD} = 3.0\text{ V}$ | $0.5T - 9$ | 71 | | | ns |
| \overline{WD} low-level width | t_{WWL} | $V_{DD} = 5.0\text{ V}$ | $(1.5 + n) T - 25$ | 95 | | | ns |
| | | $V_{DD} = 3.0\text{ V}$ | $(1.5 + n) T - 30$ | 210 | | | ns |

Remark T: $t_{CYK} = 1/f_{XX}$ (f_{XX} : main system clock frequency)

a: 1 (during address wait), otherwise, 0

n: Number of wait states ($n \geq 0$)

AC Characteristics

(2) External wait timing

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---------------------|-------------------------|------------------|------|------|------|------|
| $\overline{\text{WAIT}}\downarrow$ input time from address | t _{DAWT} | V _{DD} = 5.0 V | (2 + a) T – 40 | | | 200 | ns |
| | | V _{DD} = 3.0 V | (2 + a) T – 60 | | | 420 | ns |
| $\overline{\text{WAIT}}\downarrow$ input time from $\overline{\text{ASTB}}\downarrow$ | t _{DSTWT} | V _{DD} = 5.0 V | 1.5T – 40 | | | 80 | ns |
| | | V _{DD} = 3.0 V | 1.5T – 60 | | | 180 | ns |
| $\overline{\text{WAIT}}$ hold time from $\overline{\text{ASTB}}\downarrow$ | t _{HSTWT} | V _{DD} = 5.0 V | (0.5 + n) T + 5 | 125 | | | ns |
| | | V _{DD} = 3.0 V | (0.5 + n) T + 10 | 250 | | | ns |
| $\overline{\text{WAIT}}\uparrow$ delay time from $\overline{\text{ASTB}}\downarrow$ | t _{DSTWTH} | V _{DD} = 5.0 V | (1.5 + n) T – 40 | | | 240 | ns |
| | | V _{DD} = 3.0 V | (1.5 + n) T – 60 | | | 500 | ns |
| $\overline{\text{WAIT}}\downarrow$ input time from $\overline{\text{RD}}\downarrow$ | t _{DRWTL} | V _{DD} = 5.0 V | T – 40 | | | 40 | ns |
| | | V _{DD} = 3.0 V | T – 60 | | | 100 | ns |
| $\overline{\text{WAIT}}\downarrow$ hold time from $\overline{\text{RD}}\downarrow$ | t _{HRWT} | V _{DD} = 5.0 V | nT + 5 | 85 | | | ns |
| | | V _{DD} = 3.0 V | nT + 10 | 170 | | | ns |
| $\overline{\text{WAIT}}\uparrow$ delay time from $\overline{\text{RD}}\downarrow$ | t _{DRWTH} | V _{DD} = 5.0 V | (1 + n) T – 40 | | | 200 | ns |
| | | V _{DD} = 3.0 V | (1 + n) T – 60 | | | 420 | ns |
| Data input time from $\overline{\text{WAIT}}\uparrow$ | t _{DWTID} | V _{DD} = 5.0 V | 0.5T – 5 | | | 35 | ns |
| | | V _{DD} = 3.0 V | 0.5T – 10 | | | 70 | ns |
| $\overline{\text{RD}}\uparrow$ delay time from $\overline{\text{WAIT}}\uparrow$ | t _{DWTR} | V _{DD} = 5.0 V | 0.5T | 40 | | | ns |
| | | V _{DD} = 3.0 V | 0.5T | 80 | | | ns |
| $\overline{\text{WR}}\uparrow$ delay time from $\overline{\text{WAIT}}\uparrow$ | t _{DWTW} | V _{DD} = 5.0 V | 0.5T | 40 | | | ns |
| | | V _{DD} = 3.0 V | 0.5T | 80 | | | ns |
| $\overline{\text{WAIT}}\downarrow$ input time from $\overline{\text{WR}}\downarrow$ | t _{DWWTL} | V _{DD} = 5.0 V | T – 40 | | | 40 | ns |
| | | V _{DD} = 3.0 V | T – 60 | | | 100 | ns |
| $\overline{\text{WAIT}}$ hold time from $\overline{\text{WR}}\downarrow$ | t _{HWWT} | V _{DD} = 5.0 V | nT + 5 | 85 | | | ns |
| | | V _{DD} = 3.0 V | nT + 10 | 170 | | | ns |
| $\overline{\text{WAIT}}\uparrow$ delay time from $\overline{\text{WR}}\downarrow$ | t _{DWWTH} | V _{DD} = 5.0 V | (1 + n) T – 40 | | | 200 | ns |
| | | V _{DD} = 3.0 V | (1 + n) T – 60 | | | 420 | ns |

Remark T: t_{CYK} = 1/f_{XX} (f_{XX}: main system clock frequency)

a: 1 (during address wait), otherwise, 0

n: Number of wait states (n ≥ 0)

Serial Operation ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = AV_{DD} = 2.2$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V)

(a) 3-wire serial I/O mode ($\overline{\text{SCK}}$: internal clock output)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|-------------------|---|------|------|------|------|
| Serial clock cycle time ($\overline{\text{SCK}}$) | t_{KCY1} | $2.7 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$ | 800 | | | ns |
| | | | 3200 | | | ns |
| Serial clock high/low-level width ($\overline{\text{SCK}}$) | t_{KH1} | $2.7 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$ | 350 | | | ns |
| | t_{KL1} | | 1500 | | | ns |
| SI setup time (to $\overline{\text{SCK}}\uparrow$) | t_{SIK1} | $2.7 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$ | 10 | | | ns |
| | | | 30 | | | ns |
| SI hold time (from $\overline{\text{SCK}}\uparrow$) | t_{KSI1} | | 40 | | | ns |
| SO output delay time (from $\overline{\text{SCK}}\downarrow$) | t_{KSO1} | | | | 30 | ns |

(b) 3-wire serial I/O mode ($\overline{\text{SCK}}$: external clock input)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|-------------------|---|------|------|------|------|
| Serial clock cycle time ($\overline{\text{SCK}}$) | t_{KCY2} | $2.7 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$ | 800 | | | ns |
| | | | 3200 | | | ns |
| Serial clock high/low-level width ($\overline{\text{SCK}}$) | t_{KH2} | $2.7 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$ | 400 | | | ns |
| | t_{KL2} | | 1600 | | | ns |
| SI setup time (to $\overline{\text{SCK}}\uparrow$) | t_{SIK2} | $2.7 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$ | 10 | | | ns |
| | | | 30 | | | ns |
| SI hold time (from $\overline{\text{SCK}}\uparrow$) | t_{KSI2} | | 40 | | | ns |
| SO output delay time (from $\overline{\text{SCK}}\downarrow$) | t_{KSO2} | | | | 30 | ns |

(c) UART mode

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---------------------------|-------------------|---|------|------|------|------|
| ASCK cycle time | t_{KCY3} | $4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$ | 417 | | | ns |
| | | $2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$ | 833 | | | ns |
| | | | 1667 | | | ns |
| ASCK high/low-level width | t_{KH3} | $4.5 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$ | 208 | | | ns |
| | t_{KL3} | $2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$ | 416 | | | ns |
| | | | 833 | | | ns |

(d) I²C bus mode

| Parameter | | Symbol | Standard Mode | | High-Speed Mode | | Unit |
|---|-----------------------------------|-----------------------|-----------------|------|--------------------------|-------------------|------|
| | | | MIN. | MAX. | MIN. | MAX. | |
| SCL0 clock frequency | | f _{CLK} | 0 | 100 | 0 | 400 | kHz |
| Bus free time (between stop and start conditions) | | t _{BUF} | 4.7 | — | 1.3 | — | μs |
| Hold time Note1 | | t _{HD : STA} | 4.0 | — | 0.6 | — | μs |
| Low-level width of SCL0 clock | | t _{LOW} | 4.7 | — | 1.3 | — | μs |
| High-level width of SCL0 clock | | t _{HIGH} | 4.0 | — | 0.6 | — | μs |
| Setup time of start/restart conditions | | t _{SU : STA} | 4.7 | — | 0.6 | — | μs |
| Data hold time | When using CBUS-compatible master | t _{HD : DAT} | 5.0 | — | — | — | μs |
| | When using I ² C bus | | 0 Note 2 | — | 0 Note 2 | 0.9 Note 3 | μs |
| Data setup time | | t _{SU : DAT} | 250 | — | 100 Note 4 | — | ns |
| Rising time of SDA0 and SCL0 signals | | t _r | — | 1000 | 20 + 0.1Cb Note 5 | 300 | ns |
| Falling time of SDA0 and SCL0 signals | | t _f | — | 300 | 20 + 0.1Cb Note 5 | 300 | ns |
| Setup time of stop condition | | t _{SU : STO} | 4.0 | — | 0.6 | — | μs |
| Pulse width of spike restricted by input filter | | t _{SP} | — | — | 0 | 50 | ns |
| Load capacitance of each bus line | | C _b | — | 400 | — | 400 | pF |

- Notes**
- For the start condition, the first clock pulse is generated after the hold time.
 - To fill the undefined area of the SCL0 falling edge, it is necessary for the device to provide an internal SDA0 signal (on V_{IHmin}.) with at least 300 ns of hold time.
 - If the device does not extend the SCL0 signal low hold time (t_{LOW}), only maximum data hold time t_{HD : DAT} needs to be satisfied.
 - The high-speed mode I²C bus can be used in a standard mode I²C bus system. In this case, the conditions described below must be satisfied.
 - If the device does not extend the SCL0 signal low state hold time
t_{SU : DAT} ≥ 250 ns
 - If the device extends the SCL0 signal low state hold time
Be sure to transmit the data bit to the SDA0 line before the SCL0 line is released
(t_{rmax} + t_{SU : DAT} = 1250 ns by standard mode I²C bus specification)
 - C_b : total capacitance per one bus line (unit : pF)

Other Operations (T_A = -40 to +85°C, V_{DD} = AV_{DD} = 2.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---------------------------------|-------------------|----------------|------|------|------|------|
| NMI high/low-level width | t _{WNIL} | | 10 | | | μs |
| | t _{WNIH} | | | | | |
| INTP input high/low-level width | t _{WITL} | INTP0 to INTP6 | 10 | | | μs |
| | t _{WITL} | | | | | |
| RESET high/low-level width | t _{WRSL} | | 10 | | | μs |
| | t _{WRSH} | | | | | |

Clock Output Operation (T_A = -40 to +85°C, V_{DD} = AV_{DD} = 2.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--------------------------|-------------------|---|------|------|-------|------|
| PCL cycle time | t _{CYCL} | V _{DD} = 4.5 to 5.5 V, nT | 80 | | 31250 | ns |
| PCL high/low-level width | t _{CLL} | V _{DD} = 4.5 to 5.5 V, 0.5T – 10 | 30 | | 15615 | ns |
| | t _{CLH} | | | | | |
| PCL rising/falling time | t _{CLR} | 4.5 V ≤ V _{DD} ≤ 5.5 V | | | 5 | ns |
| | t _{CLF} | 2.7 V ≤ V _{DD} < 4.5 V | | | 10 | ns |
| | | 2.2 V ≤ V _{DD} < 2.7 V | | | 20 | ns |

Remark T: t_{cyk} = 1/f_{xx} (f_{xx}: main system clock frequency)

n: Divided frequency ratio set by software in the CPU

- When using the main system clock: n = 1, 2, 4, 8, 16, 32, 64, 128
- When using the subsystem clock: n = 1

A/D Converter Characteristics (T_A = -40 to +85°C, V_{DD} = AV_{DD} = 2.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|--|---------------------|---|--------------------|------|--------------------|------|
| Resolution | | | 8 | 8 | 8 | bit |
| Total error Note | | 2.7 V ≤ AV _{REF0} ≤ AV _{DD} | | | 1.2 | % |
| | | 2.2 V ≤ AV _{REF0} < 2.7 V (only when AV _{REF0} = AV _{DD}) | | | 1.6 | % |
| Conversion time | t _{CONV} | | 14 | | 144 | μs |
| Sampling time | t _{SAMP} | | 24/f _{XX} | | | μs |
| Analog input voltage | V _{IAN} | | AV _{SS} | | AV _{REF0} | V |
| Reference voltage | AV _{REF0} | | 2.2 | | AV _{DD} | V |
| Resistance between AV _{REF0} and AV _{SS} | R _{AVREF0} | | | 29.4 | | kΩ |

Note Quantization error (±1/2 LSB) is not included.

Remark f_{xx}: Main system clock frequency

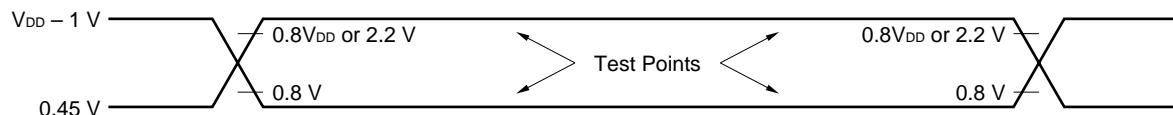
D/A Converter Characteristics (T_A = -40 to +85°C, V_{DD} = AV_{DD} = 2.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | |
|----------------------------|--------------------|---|------------------------------------|------|-----------------|------|----|
| Resolution | | | 8 | 8 | 8 | bit | |
| Total error | | R = 2 MΩ, 2.2 V < AV _{REF1} ≤ 5.5 V | | | 1.2 | % | |
| | | R = 4 MΩ, 2.2 V < AV _{REF1} ≤ 5.5 V | | | 0.8 | % | |
| | | R = 10 MΩ, 2.2 V < AV _{REF1} ≤ 5.5 V | | | 0.6 | % | |
| Settling time | | Load conditions: C = 30 pF | 4.5 V ≤ AV _{REF1} ≤ 5.5 V | | | 10 | μs |
| | | | 2.7 V ≤ AV _{REF1} < 4.5 V | | | 15 | μs |
| | | | 2.2 V ≤ AV _{REF1} < 2.7 V | | | 20 | μs |
| Output resistance | R _O | DACS0, 1 = 7 FH | | 5.3 | | kΩ | |
| Reference voltage | AV _{REF1} | | 2.2 | | V _{DD} | V | |
| AV _{REF1} current | AI _{REF1} | For only 1 channel | | | 2.5 | mA | |

Data Retention Characteristics (T_A = -40 to +85°C, V_{DD} = AV_{DD} = 2.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

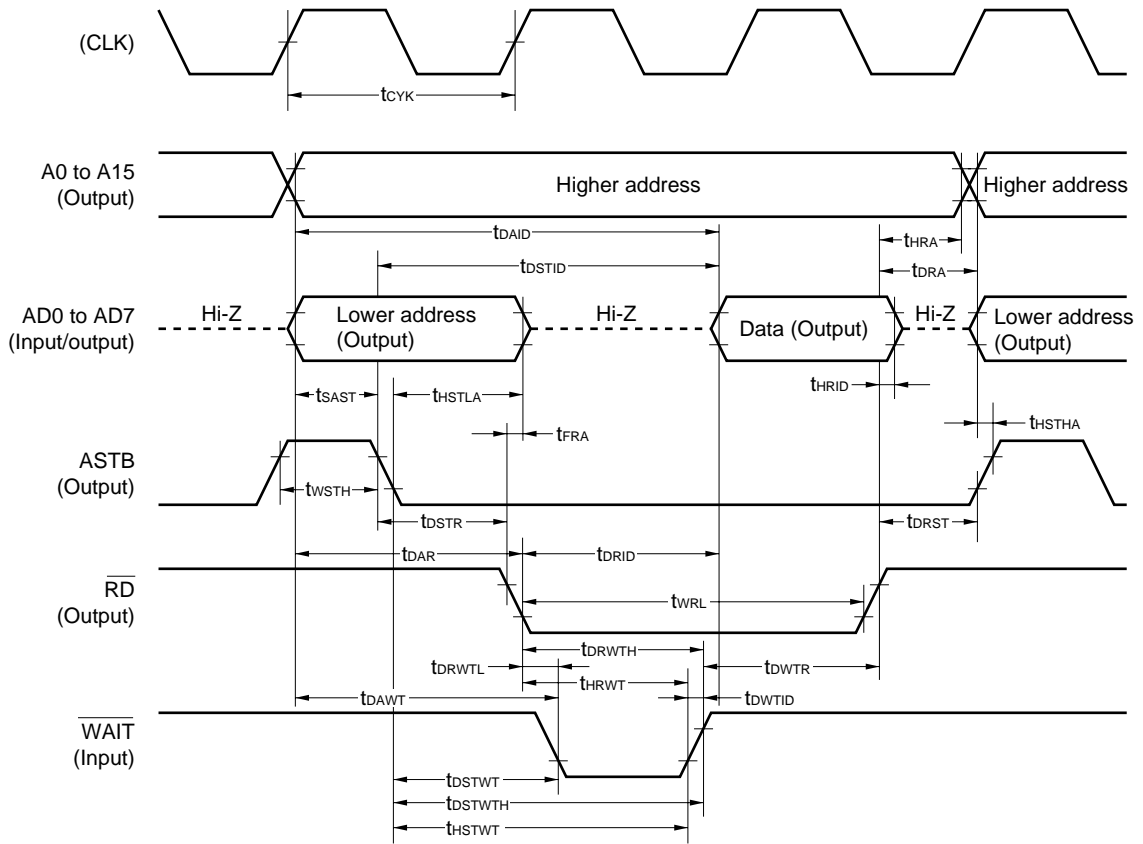
| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|-------------------|-----------------------------------|----------------------|------|----------------------|------|
| Data retention voltage | V _{DDDR} | STOP mode | 2.2 | | 5.5 | V |
| Data retention current | I _{DDDR} | V _{DDDR} = +4.5 to 5.5 V | | 10 | 50 | μA |
| | | V _{DDDR} = +2.5 V | | 2 | 10 | μA |
| V _{DD} rising time | t _{RVD} | | 200 | | | μs |
| V _{DD} falling time | t _{FVD} | | 200 | | | μs |
| V _{DD} hold time (from STOP mode setting) | t _{HVD} | | 0 | | | ms |
| STOP release signal input time | t _{DREL} | | 0 | | | ms |
| Oscillation stabilization wait time | t _{WAIT} | Crystal resonator | 30 | | | ms |
| | | Ceramic resonator | 5 | | | ms |
| Low-level input voltage | V _{IL} | RESET, P00/INTP0 to P06/INTP6 | 0 | | 0.1V _{DDDR} | V |
| High-level input voltage | V _{IH} | | 0.9V _{DDDR} | | V _{DDDR} | V |

AC Timing Test Points



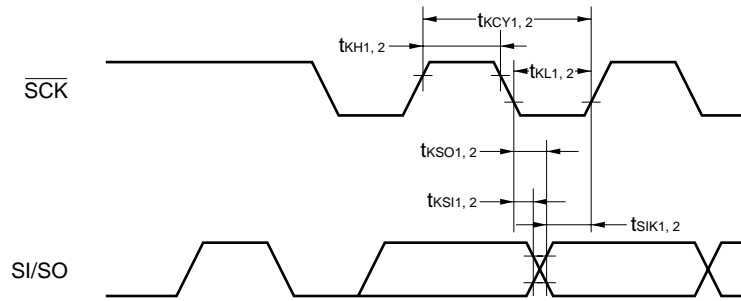
Timing Wave Form

(1) Read operation

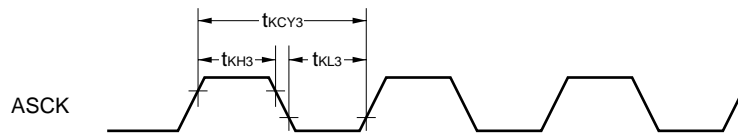


Serial Operation

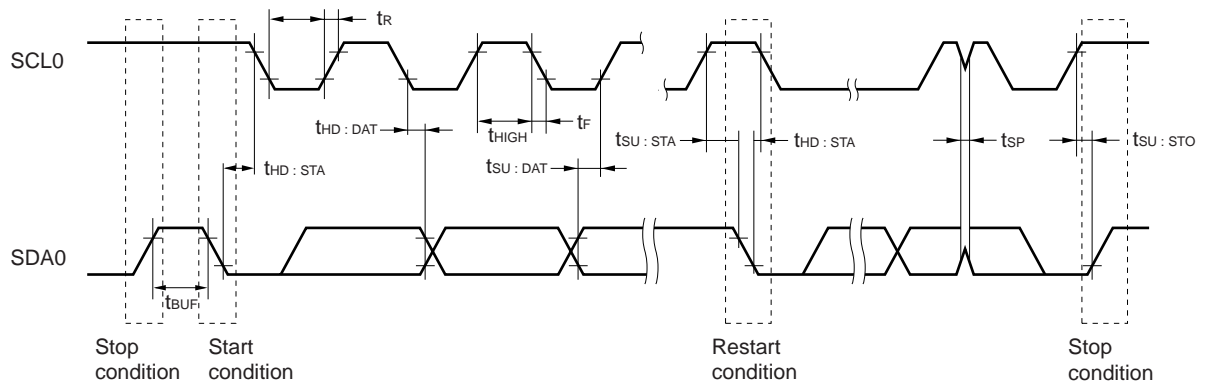
(1) 3-wire serial I/O mode



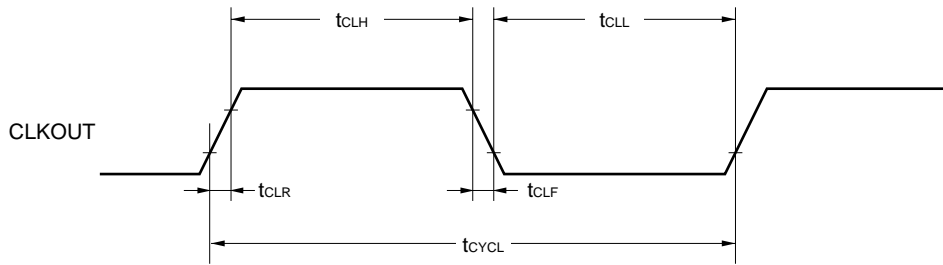
(2) UART mode



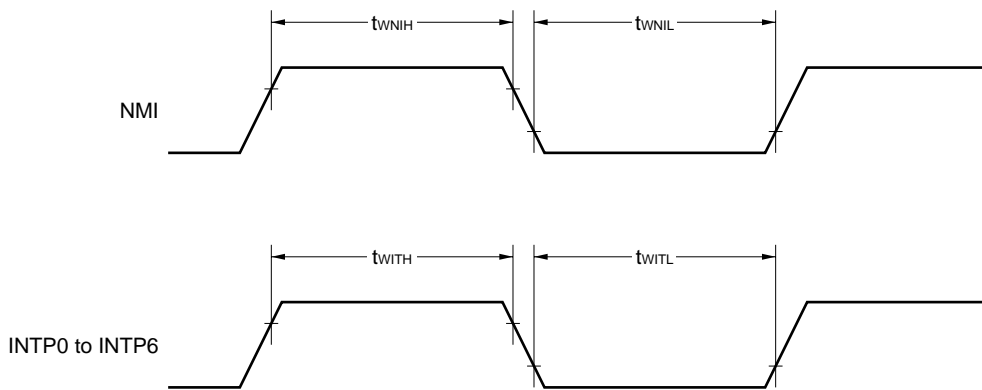
(3) I²C bus mode



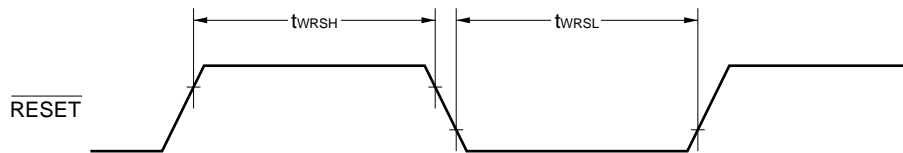
Clock Output Timing



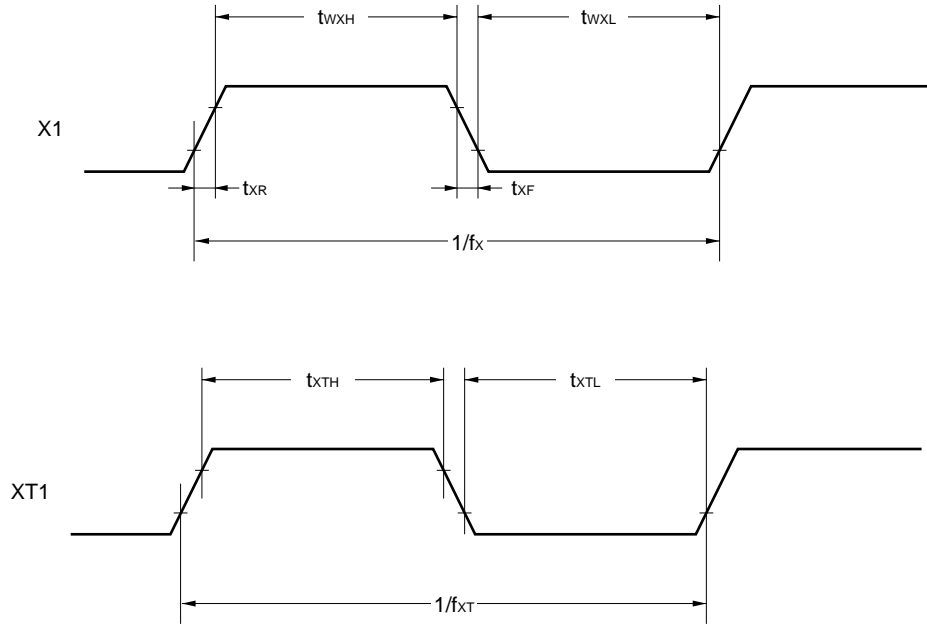
Interrupt Input Timing



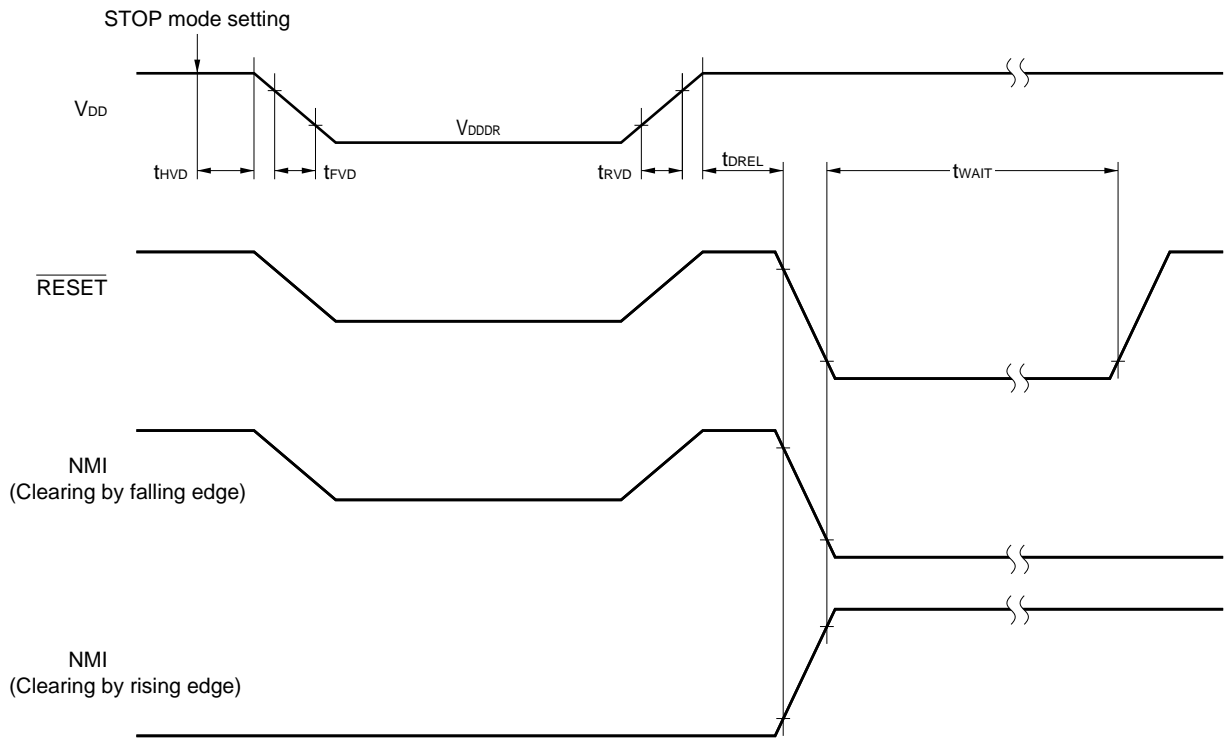
Reset Input Timing



Clock Timing

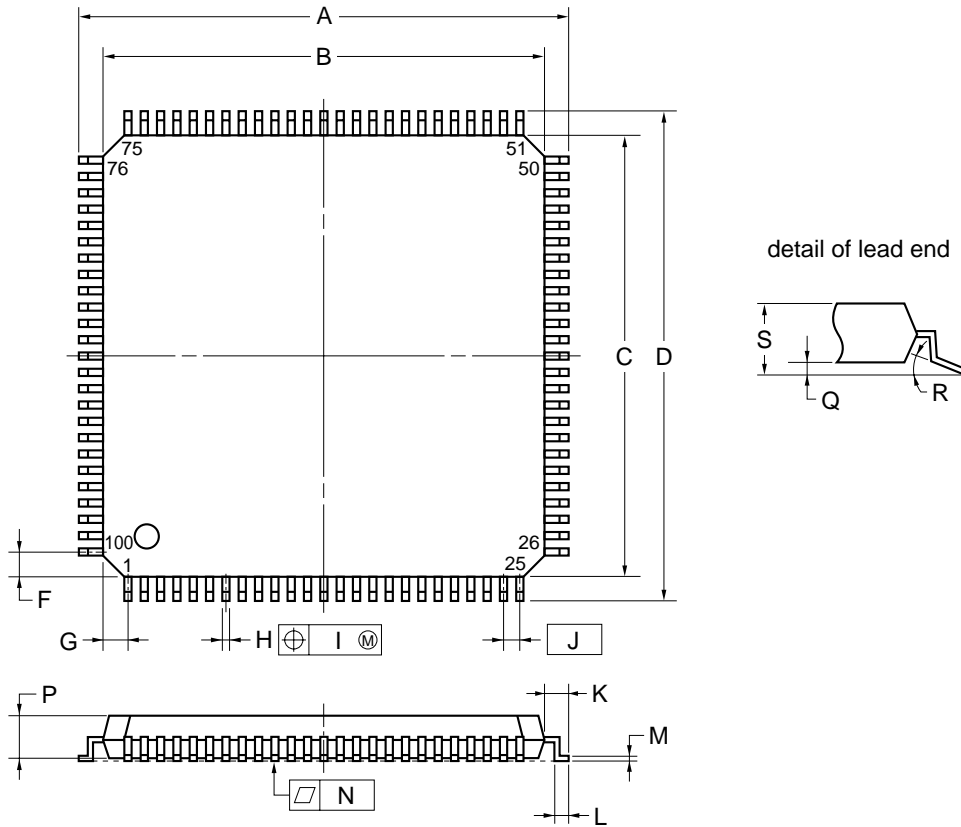


Data Retention Characteristics



★ 14. PACKAGE DRAWINGS

100 PIN PLASTIC LQFP (FINE PITCH) (14×14)



NOTE

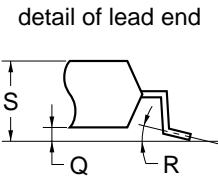
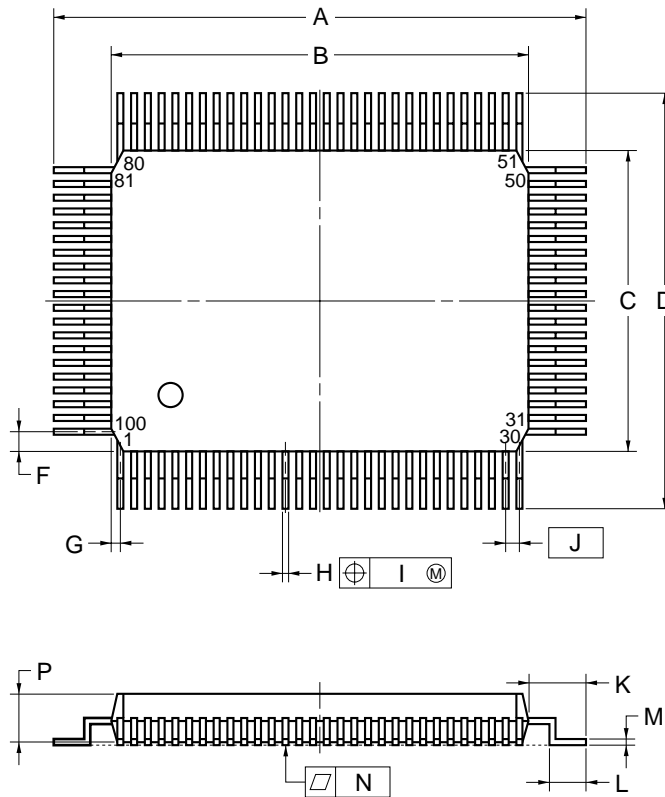
Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|------|--|---|
| A | 16.00±0.20 | 0.630±0.008 |
| B | 14.00±0.20 | 0.551 ^{+0.009} _{-0.008} |
| C | 14.00±0.20 | 0.551 ^{+0.009} _{-0.008} |
| D | 16.00±0.20 | 0.630±0.008 |
| F | 1.00 | 0.039 |
| G | 1.00 | 0.039 |
| H | 0.22 ^{+0.05} _{-0.04} | 0.009±0.002 |
| I | 0.08 | 0.003 |
| J | 0.50 (T.P.) | 0.020 (T.P.) |
| K | 1.00±0.20 | 0.039 ^{+0.009} _{-0.008} |
| L | 0.50±0.20 | 0.020 ^{+0.008} _{-0.009} |
| M | 0.17 ^{+0.03} _{-0.07} | 0.007 ^{+0.001} _{-0.003} |
| N | 0.08 | 0.003 |
| P | 1.40±0.05 | 0.055±0.002 |
| Q | 0.10±0.05 | 0.004±0.002 |
| R | 3° ^{+7°} _{-3°} | 3° ^{+7°} _{-3°} |
| S | 1.60 MAX. | 0.063 MAX. |

S100GC-50-8EU

Remark The external dimensions and material of the ES version are the same as those of the mass-produced version.

100PIN PLASTIC QFP (14x20)



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|------|--|---|
| A | 23.6±0.4 | 0.929±0.016 |
| B | 20.0±0.2 | 0.795 ^{+0.009} _{-0.008} |
| C | 14.0±0.2 | 0.551 ^{+0.009} _{-0.008} |
| D | 17.6±0.4 | 0.693±0.016 |
| F | 0.8 | 0.031 |
| G | 0.6 | 0.024 |
| H | 0.30±0.10 | 0.012 ^{+0.004} _{-0.005} |
| I | 0.15 | 0.006 |
| J | 0.65 (T.P.) | 0.026 (T.P.) |
| K | 1.8±0.2 | 0.071 ^{+0.008} _{-0.009} |
| L | 0.8±0.2 | 0.031 ^{+0.009} _{-0.008} |
| M | 0.15 ^{+0.10} _{-0.05} | 0.006 ^{+0.004} _{-0.003} |
| N | 0.10 | 0.004 |
| P | 2.7±0.1 | 0.106 ^{+0.005} _{-0.004} |
| Q | 0.1±0.1 | 0.004±0.004 |
| R | 5°±5° | 5°±5° |
| S | 3.0 MAX. | 0.119 MAX. |

P100GF-65-3BA1-3

Remark The external dimensions and material of the ES version are the same as those of the mass-produced version.

★ 15. RECOMMENDED SOLDERING CONDITIONS

The μPD784216Y should be soldered and mounted under the following recommended conditions. For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 15-1. Soldering Conditions for Surface Mount Type

- (1) μPD784214YGC-xxx-8EU: 100-pin plastic LQFP (Fine pitch) (14 × 14 mm)
- μPD784215YGC-xxx-8EU: 100-pin plastic LQFP (Fine pitch) (14 × 14 mm)
- μPD784216YGC-xxx-8EU: 100-pin plastic LQFP (Fine pitch) (14 × 14 mm)

| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
|------------------|---|------------------------------|
| Infrared reflow | Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher), Count: two times or less | IR35-00-2 |
| VPS | Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher), Count: two times or less | VP-15-00-2 |
| Partial heating | Pin temperature: 300°C Max., Time: 3 sec. Max. (per pin row) | — |

Caution Do not use different soldering methods together (except for partial heating).

- (2) μPD784214YGF-xxx-3BA: 100-pin plastic QFP (Fine pitch) (14 × 20 mm)
- μPD784215YGF-xxx-3BA: 100-pin plastic QFP (Fine pitch) (14 × 20 mm)
- μPD784216YGF-xxx-3BA: 100-pin plastic QFP (Fine pitch) (14 × 20 mm)

| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
|------------------|---|------------------------------|
| Infrared reflow | Package peak temperature: 235°C, Time: 30 sec. Max. (at 210°C or higher), Count: two times or less | IR35-00-2 |
| VPS | Package peak temperature: 215°C, Time: 40 sec. Max. (at 200°C or higher), Count: two times or less | VP15-00-2 |
| Wave soldering | Solder bath temperature: 260°C Max., Time: 10 sec. Max., Count: once, Preheating temperature: 120°C Max. (package surface temperature) | WS60-00-1 |
| Partial heating | Pin temperature: 300°C Max., Time: 3 sec. Max. (per pin row) | — |

Caution Do not use different soldering methods together (except for partial heating).

★ APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD784216Y. Also refer to (5) **Cautions on Using Development Tools.**

(1) Language Processing Software

| | |
|----------|--|
| RA78K4 | Assembler package common to 78K/IV Series |
| CC78K4 | C compiler package common to 78K/IV Series |
| DF784218 | Device file common to μPD784216Y Subseries |
| CC78K4-L | C compiler library source file common to 78K/IV Series |

(2) Flash Memory Writing Tools

| | |
|--|--|
| Flashpro II (Model number: FL-PR2), Flashpro III (Model number: FL-PR3, PG-FP3) | Dedicated flash programmer for microcontroller incorporating flash memory |
| FA-100GF | Adapter for writing 100-pin plastic QFP (GF-3BA type) flash memory. Connection must be performed depending on the target product. |
| FA-100GC | Adapter for writing 100-pin plastic LQFP (GC-8EU type) flash memory. Connection must be performed depending on the target product. |
| Flashpro II controller, Flashpro III controller | Control program that runs on a personal computer and is attached to Flashpro II, Flashpro III. Operates on Windows™95, etc. |

(3) Debugging Tools

- When IE-78K4-NS in-circuit emulator is used

| | |
|------------------------------|---|
| IE-78K4-NS | In-circuit emulator common to 78K/IV Series |
| IE-70000-MC-PS-B | Power supply unit for IE-78K4-NS |
| IE-70000-98-IF-C | Interface adapter used when PC-9800 series PC (except notebook type) is used as host machine (C bus supported) |
| IE-70000-CD-IF-A Note | PC card and cable when PC-9800 series notebook PC is used as host machine (PCMCIA socket supported) |
| IE-70000-PC-IF-C | Interface adapter when using IBM PC/AT™ compatibles as host machine (ISA bus supported) |
| IE-70000-PCI-IF Note | Interface adapter when using PC that incorporates PCI bus as host machine |
| IE-784225-NS-EM1 | Emulation board to emulate μPD784216Y Subseries |
| NP-100GF | Emulation probe for 100-pin plastic QFP (GF-3BA type) |
| NP-100GC | Emulation probe for 100-pin plastic LQFP (GC-8EU type) |
| EV-9200GF-100 | Socket to be mounted on a target system board made for 100-pin plastic QFP (GF-3BA type) |
| TGC-100SDW | Conversion adapter to connect the NP-100GC and a target system board on which a 100-pin plastic LQFP (GC-8EU type) can be mounted |
| ID78K4-NS | Integrated debugger for IE-78K4-NS |
| SM78K4 | System simulator common to 78K/IV Series |
| DF784218 | Device file common to μPD784216Y Subseries |

Note Under development

- **When IE-784000-R in-circuit emulator is used**

| | |
|-------------------------------------|--|
| IE-784000-R | In-circuit emulator common to 78K/IV Series |
| IE-70000-98-IF-C | Interface adapter used when PC-9800 series PC (except notebook type) is used as host machine (C bus supported) |
| IE-70000-98N-IF | Interface adapter and cable used when PC-9800 series notebook type PC is used as host machine |
| IE-70000-PC-IF-C | Interface adapter when using IBM PC/AT and compatibles as host machine (ISA bus supported) |
| IE-70000-PCI-IF ^{Note} | Interface adapter when using PC that incorporates PCI bus as host machine |
| IE-78000-R-SV3 | Interface adapter and cable used when EWS is used as host machine |
| IE-784225-NS-EM1 IE-784216-R-EM1 | Emulation board to emulate μPD784216Y Subseries |
| IE-784000-R-EM | Emulation board common to 78K/IV Series |
| IE-78K4-R-EX3 | Emulation probe conversion board necessary when using IE-784225-NS-EM1 on IE-784000-R. Not necessary when IE-784216-R-EM1 is used. |
| EP-78064GF-R | Emulation probe for 100-pin plastic QFP (GF-3BA type) |
| EP-78064GC-R | Emulation probe for 100-pin plastic LQFP (GC-8EU type) |
| EV-9200GF-100 | Socket to be mounted on a target system board made for 100-pin plastic QFP (GF-3BA type) |
| TGC-100SDW | Conversion adapter to connect the NP-100GC and a target system board on which a 100-pin plastic LQFP (GC-8EU type) can be mounted |
| ID78K4 | Integrated debugger for IE-784000-R |
| SM78K4 | System simulator common to 78K/IV Series |
| DF784218 | Device file common to μPD784216Y Subseries |

Note Under development

(4) Real-time OS

| | |
|----------|--------------------------------|
| RX78K/IV | Real-time OS for 78K/IV Series |
| MX78K4 | OS for 78K/IV Series |

(5) Cautions on Using Development Tools

- The ID78K4-NS, ID78K4, and SM78K4 are used in combination with the DF784218.
- The CC78K4 and RX78K/IV are used in combination with the RA78K4 and DF784218.
- The FL-PR2, FL-PR3, FA-100GF, FA-100GC, NP-100GF, and NP-100GC are products made by Naitou Densai Machidaseisakusho Co., Ltd. (TEL: +81-44-822-3813). Contact an NEC distributor regarding the purchase of these products.
- The TGC-100SDW is a product made by TOKYO ELETECH CORPORATION.
- For further information, contact Daimaru Kogyo, Ltd.
Tokyo Electronic Components Division (TEL: +81-3-3820-7112)
Osaka Electronic Components Division (TEL: +81-6-244-6672)
- For third party development tools, see the **78K/IV Series Selection Guide (U13355E)**.
- The host machine and OS suitable for each software are as follows:

| Host Machine [OS] Software | PC | EWS |
|----------------------------------|---|--|
| | PC-9800 series [Windows] IBM PC/AT and compatibles [Japanese/English Windows] | HP9000 Series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™] |
| RA78K4 | √ Note | √ |
| CC78K4 | √ Note | √ |
| ID78K4-NS | √ | — |
| ID78K4 | √ | √ |
| SM78K4 | √ | — |
| RX78K/IV | √ Note | √ |
| MX78K4 | √ Note | √ |

Note DOS-based software

★ APPENDIX B. RELATED DOCUMENTS

Documents related to device

| Document Name | Document No. | |
|--|--------------|---------------|
| | Japanese | English |
| μPD784214Y, 784215Y, 784216Y Data Sheet | U11725J | This document |
| μPD78F4216Y Data Sheet | U11824J | U11824E |
| μPD784216, 784216Y Subseries User's Manual Hardware | U12015J | U12015E |
| μPD784216Y Subseries Special Function Register Table | U12046J | – |
| 78K/IV Series User's Manual Instructions | U10905J | U10905E |
| 78K/IV Series Instruction Table | U10594J | – |
| 78K/IV Series Instruction Set | U10595J | – |
| 78K/IV Series Application Note Software Basics | U10095J | U10095E |

Documents related to development tool (User's Manual)

| Document Name | | Document No. | |
|--|--|--------------|----------------|
| | | Japanese | English |
| RA78K4 Assembler Package | Language | U11162J | U11162E |
| | Operation | U11334J | U11334E |
| RA78K Structured Assembler Preprocessor | | U11743J | U11743E |
| CC78K4 C Compiler | Language | U11571J | U11571E |
| | Operation | U11572J | U11572E |
| IE-78K4-NS | | U13356J | U13356E |
| IE-784000-R | | U12903J | U12903E |
| IE-784218-R-EM1 | | U12155J | U12155E |
| IE-784225-NS-EM1 | | U13742J | To be prepared |
| EP-78064 | | EEU-934 | EEU-1469 |
| SM78K4 System Simulator Windows Based | Reference | U10093J | U10093E |
| SM78K Series System Simulator | External Part User Open Interface Specifications | U10092J | U10092E |
| ID78K4-NS Integrated Debugger PC Based | Reference | U12796J | U12796E |
| ID78K4 Integrated Debugger Windows Based | Reference | U10440J | U10440E |
| ID78K4 Integrated Debugger HP-UX, SunOS, NEWS-OS based | Reference | U11960J | U11960E |

Caution The contents of the above related documents are subject to change without notice. Be sure to use the latest edition of a document for designing.

Documents related to embedded software (User's Manual)

| Document Name | | Document No. | |
|----------------------------|--------------|--------------|---------|
| | | Japanese | English |
| 78K/IV Series Real-Time OS | Fundamental | U10603J | U10603E |
| | Installation | U10604J | U10604E |
| | Debugger | U10364J | – |

Other documents

| Document Name | Document No. | |
|--|--------------|----------|
| | Japanese | English |
| NEC IC Package Manual (CD ROM) | – | C13388E |
| Semiconductor Device Mounting Technology Manual | C10535J | C10535E |
| Quality Grades on NEC Semiconductor Devices | C11531J | C11531E |
| NEC Semiconductor Device Reliability/Quality Control System | C10983J | C10983E |
| Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD) | C11892J | C11892E |
| Guide to Quality Assurance for Semiconductor Devices | – | MEI-1202 |
| Guide to Microcontroller-Related Products by Third Parties | U11416J | – |

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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Fax: 408-588-6130
800-729-9288

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Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.

Milton Keynes, UK
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Fax: 01908-670-290

NEC Electronics Italiana s.r.l.

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Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.