DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD78233,78234,78237,78238

8-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD78233, 78234, 78237 and 78238 are 78K/II series products. The 78K/II is an 8-bit single-chip microcomputer which can access the memory space of 1M-byte with an external expansion.

Functions are described in detail in the following user's manuals, which should be read when carrying out design work.

μPD78234 Series User's Manual Hardware Volume : IEU-718
78K/II Series User's Manual Instruction Volume : IEU-754

FEATURES

- High-speed instruction executiong (12 MHz operation) : 333 ns (μPD78234, 78238)
  500 ns (μPD78233, 78237)
- On-chip memory
  - ROM : 16K bytes (μPD78234)
    32K bytes (μPD78238)
    Not incorporated (μPD78233, 78237)
  - RAM : 640 bytes (μPD78233, 78234)
    1024 bytes (μPD78237, 78238)
- I/O pin : 64 pins (μPD78234, 78238)
  46 pins (μPD78233, 78237)
- A/D converter (analog 8 inputs)
- D/A converter (analog 2 outputs)
- PWM output (2 outputs)

APPLICATION

LBP engine, typewriter, HDD, FDD, PPC, FAX, electronic musical instrument, inverter, camera, air-conditioner, etc. ★

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The mark ★ shows major revised points.

6427525 0086100 968

ORDERING INFORMATION

Ordering Code	Package	Internal ROM	Internal RAM
μPD78233GC-3B9	80-pin plastic QFP (□14 mm)	None	640
μPD78233GJ-5BG	94-pin plastic QFP (□20 mm)	None	640
μPD78233LQ	84-pin plastic QFJ (□1150 mil)	None	640
μPD78234GC-xxx-3B9	80-pin plastic QFP (□14 mm)	16K	640
μPD78234GJ-xxx-5BG	94-pin plastic QFP (□20 mm)	16K	640
μPD78234LQ-xxx	84-pin plastic QFJ (□1150 mil)	16K	640
μPD78237GC-3B9	80-pin plastic QFP (□14 mm)	None	1024
μPD78237GJ-5BG	94-pin plastic QFP (□20 mm)	None	1024
μPD78237LQ	84-pin plastic QFJ (□1150 mil)	None	1024
μPD78238GC-xxx-3B9	80-pin plastic QFP (□14 mm)	32K	1024
μPD78238GJ-xxx-5BG	94-pin plastic QFP (□20 mm)	32K	1024
μPD78238LQ-xxx	84-pin plastic QFJ (□1150 mil)	32K	1024

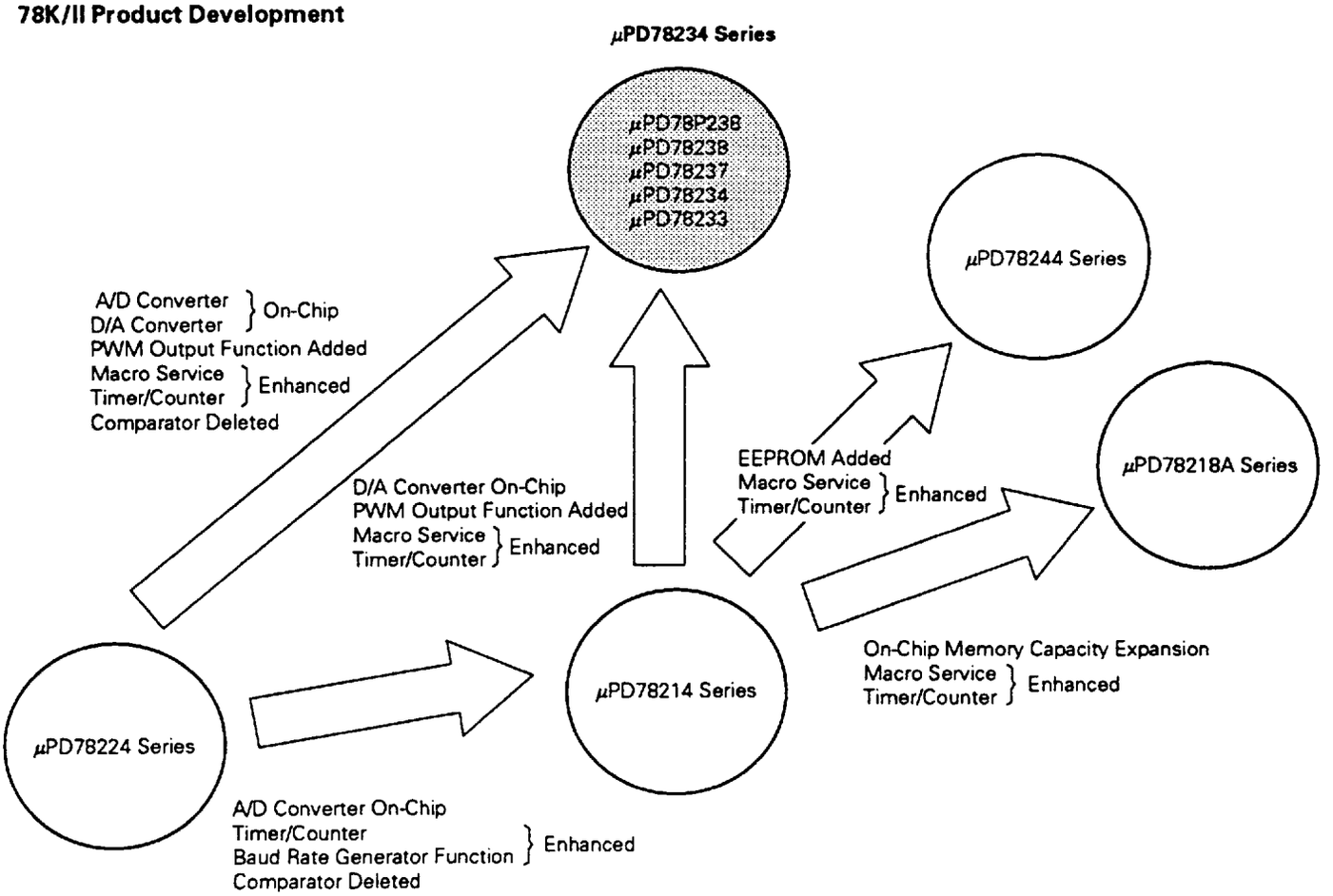
Remarks "xxx" is a ROM code number.

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semicondcutor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

78K/II Product Development



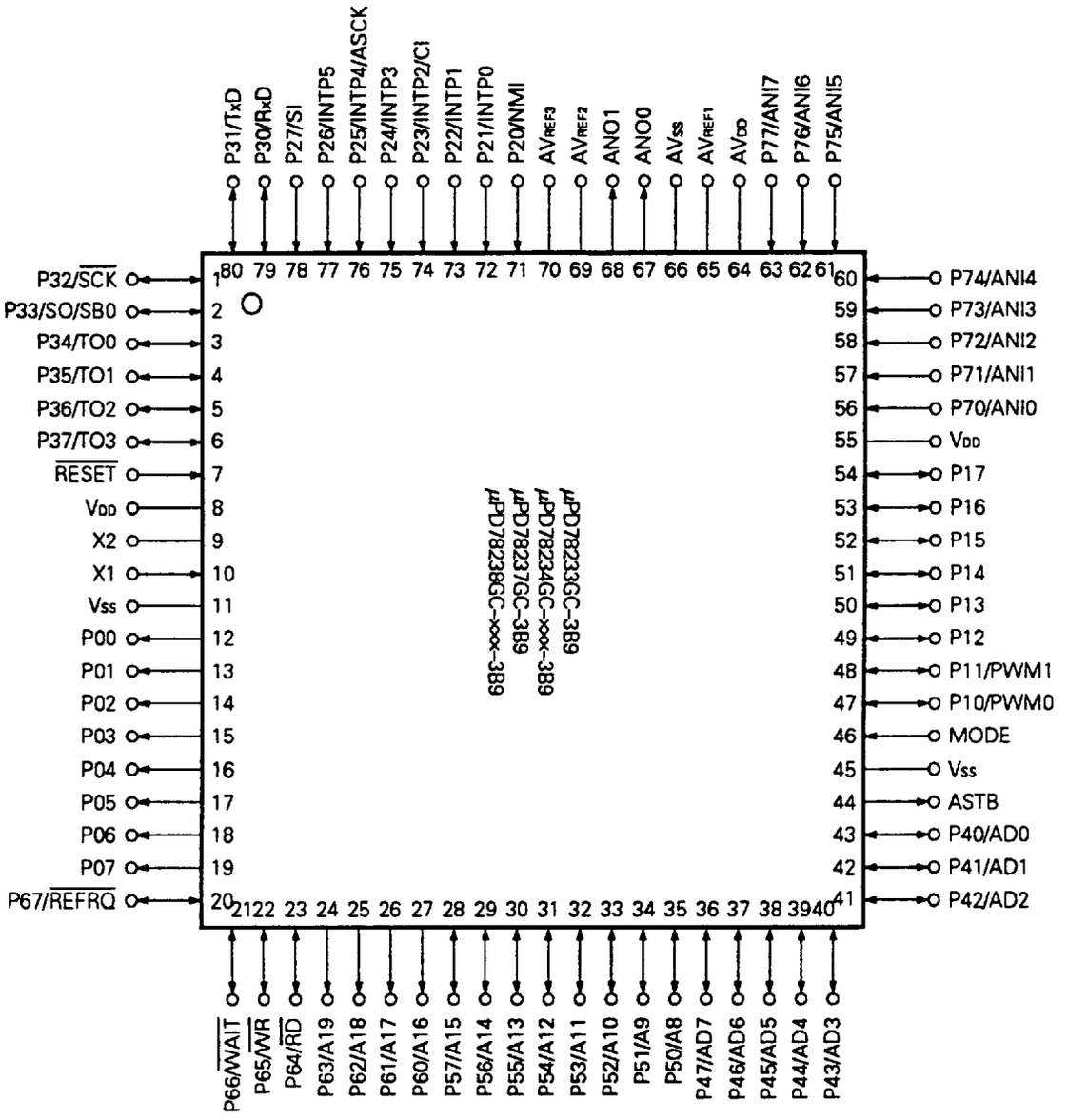
FUNCTION LIST

Item			μPD78233	μPD78234	μPD78237	μPD78238
No. of basic instructions (Mnemonic)			65			
Minimum instruction execution time (at 12 MHz operation)			500 ns	333 ns	500 ns	333 ns
On-chip memory capacity		ROM	None	16K bytes	None	32K bytes
		RAM	640 bytes		1024 bytes	
Memory space			Program memory: 64K bytes, data memory: 1M bytes			
I/O pins		Input	16			
		Output	12			
		Input/output	18	36	18	36
		Total	46	64	46	64
	Pins with additional function*	Pin with pull-up resistor	24	42	24	42
		LED direct drive output	8	24	8	24
		Transister direct drive output	8			
Real-time output port			4 bits × 2 or 8 bits × 1			
General register			8 bits × 8 bits × 4 banks (memory mapping)			
Timer/counter			16-bit timer/counter: Timer register × 1, Capture register × 1, Compare register × 2; Pulse output enabled (Toggle output, PWM/PPG output, One-shot pulse output)			
			8-bit timer/counter 1: Timer register × 1, Capture/compare register × 1, Compare register × 1; Pulse output enabled (Real-time output: 4 bits × 2)			
			8-bit timer/counter 2: Timer register × 1, Capture register × 1, Compare register × 2; Pulse output enabled (Toggle output, PWM/PPG output)			
			8-bit timer/counter 3: Timer register × 1, Compare register × 1			
PWM output function			12-bit resolution × 2 channels (PWM frequency: 23.4 kHz)			
Serial interface			UART :1 channel (specialized baud rate generator incorporated) CSI (3-wire serial I/O, SBI) :1 channel			
A/D converter			8-bit resolution × 8 channels			
D/A converter			8-bit resolution × 2 channels			
Interrrupt			19 sources (external 7, internal 12) + BRK instruction Priority order of 2 levels (programmable) 2 types of sevicing (vectored interrupt, macro service)			
Instruction set			16-bit operation Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8bits) Bit manipulation BCD adjustment, others			
Package			80-pin plastic QFP (□14 mm) 94-pin plastic QFP (□20 mm) 84-pin plastic QFJ (□1150 mil)			

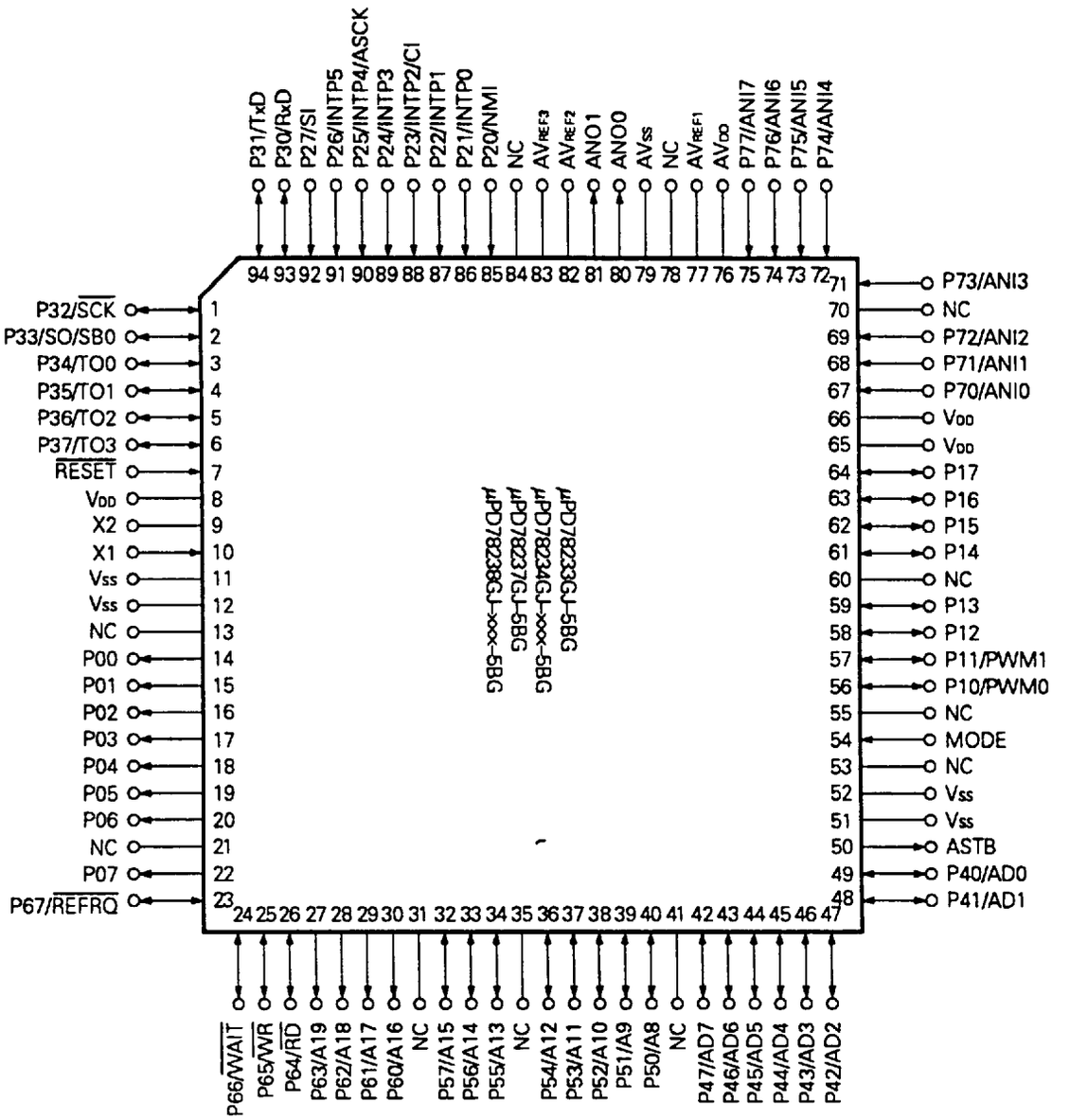
* Pins with additional function included in the I/O pin.

PIN CONFIGURATION (TOP VIEW)

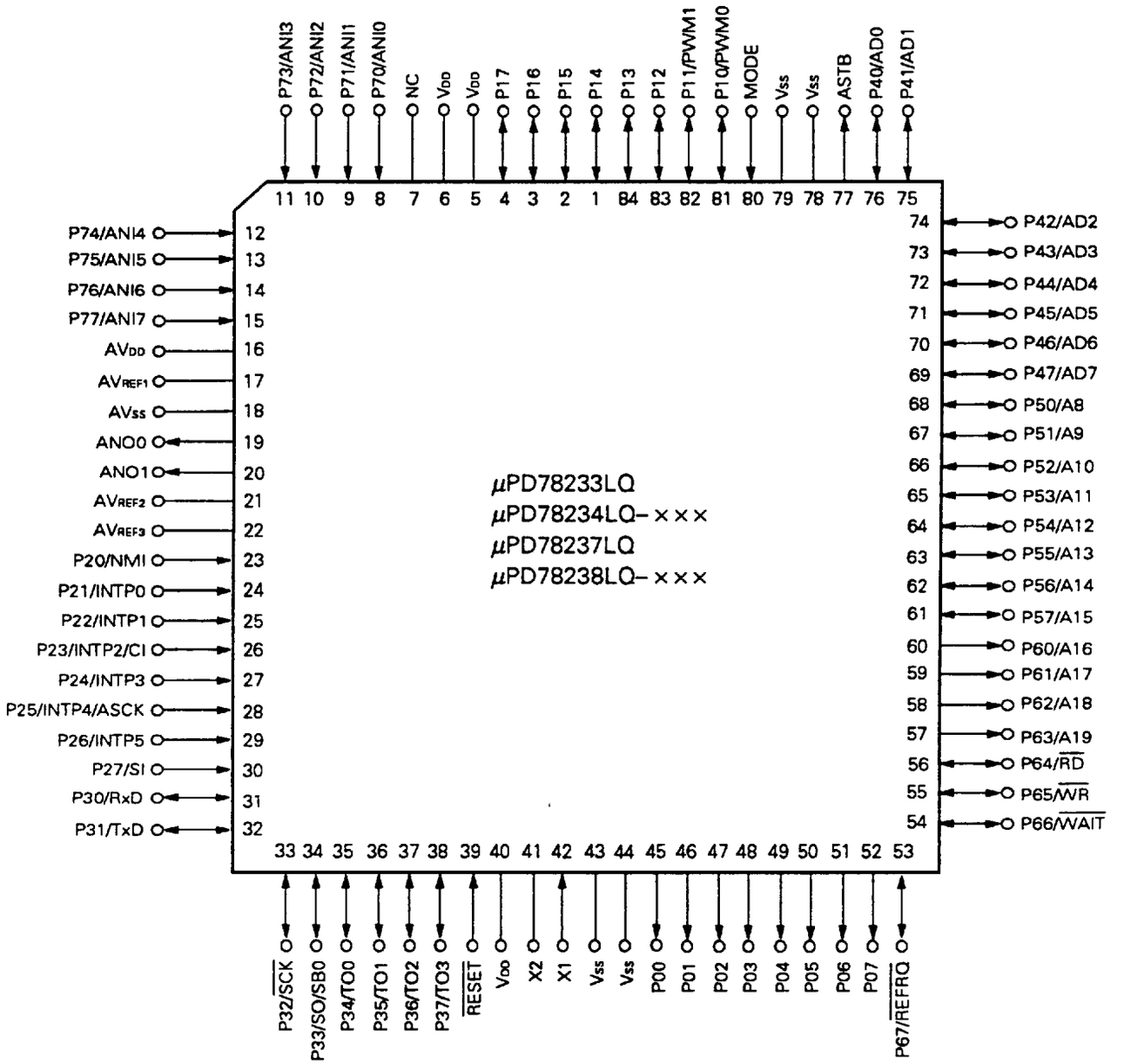
80-Pin Plastic QFP (□14 mm)



94-Pin Plastic QFP (□20 mm)

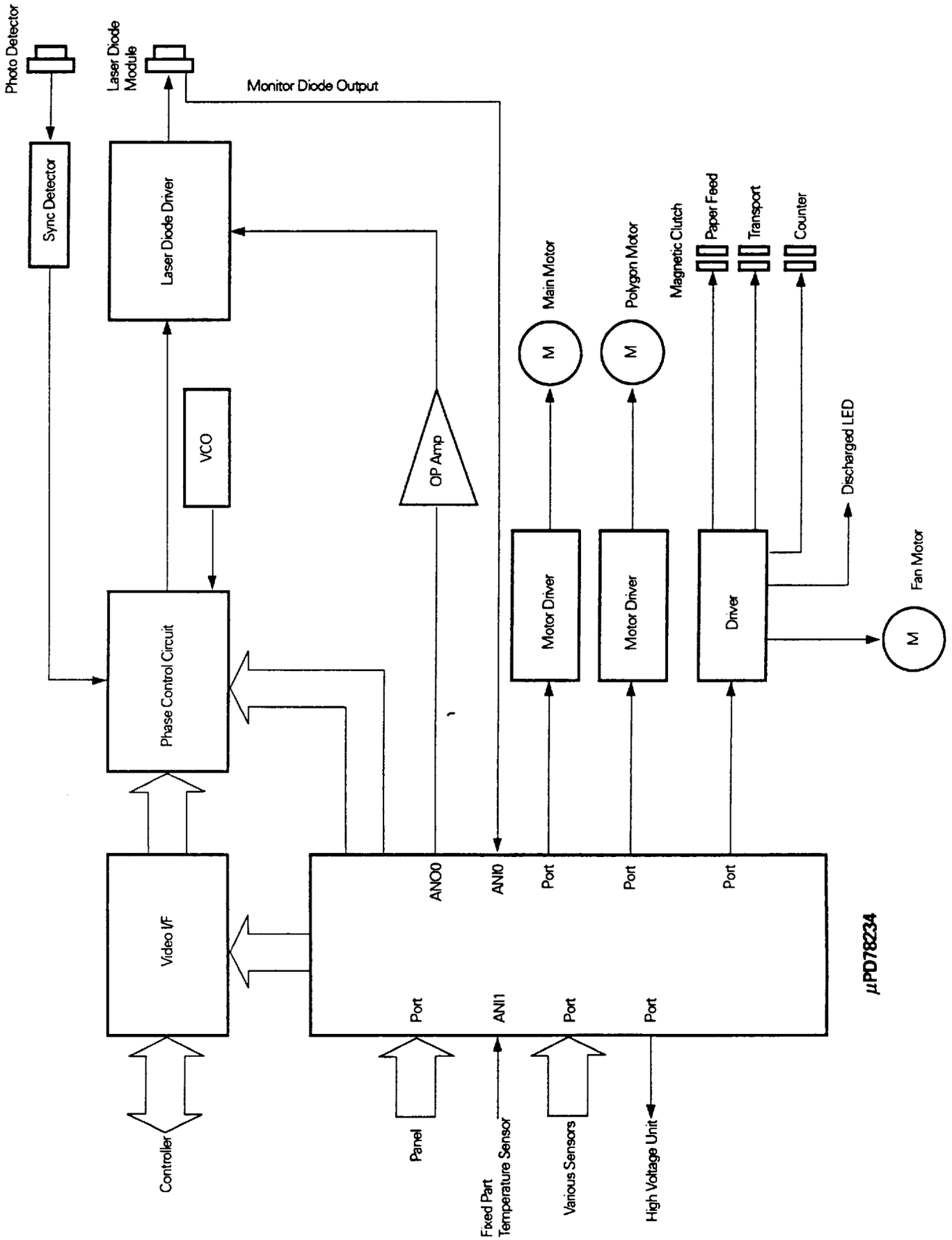


84-Pin Plastic QFJ (□1150 mil)

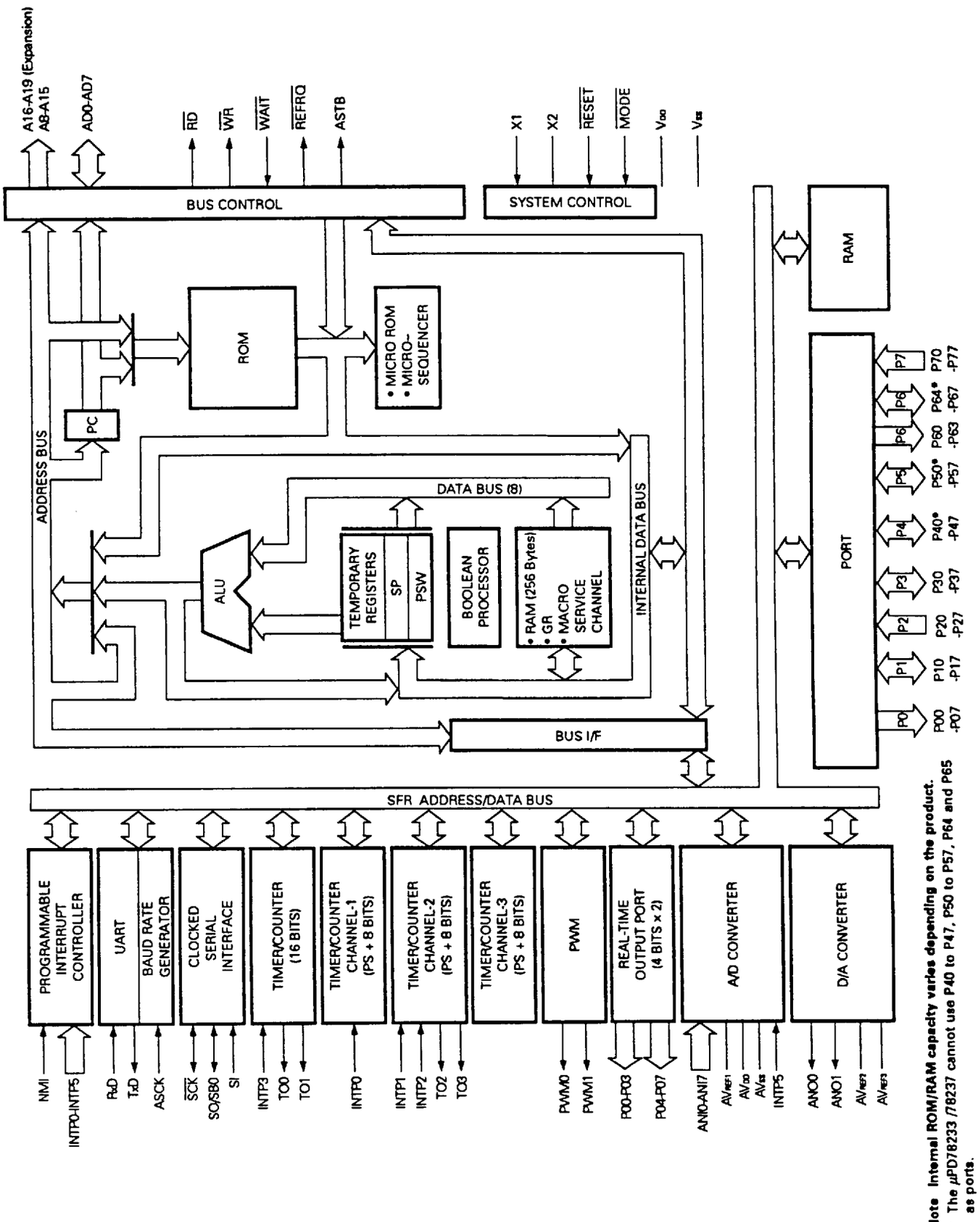


P00 to P07	:	Port 0
P10 to P17	:	Port 1
P20 to P27	:	Port 2
P30 to P37	:	Port 3
P40 to P47	:	Port 4
P50 to P57	:	Port 5
P60 to P67	:	Port 6
P70 to P77	:	Port 7
TO0 to TO3	:	Timer Output
CI	:	Clock Input
RxD	:	Receive Data
TxD	:	Transmit Data
$\overline{SCK}$	:	Serial Clock
ASCK	:	Asynchronous Serial Clock
SB0	:	Serial Bus
SI	:	Serial Input
SO	:	Serial Output
PWM0, PWM1	:	Pulse Width Modulation Output
NMI	:	Non-maskable Interrupt
INTP0 to INTP5	:	Interrupt From Peripherals
AD0 to AD7	:	Address/Data Bus
A8 to A19	:	Address Bus
$\overline{RD}$	:	Read Strobe
$\overline{WR}$	:	Write Strobe
$\overline{WAIT}$	:	Wait
ASTB	:	Address Strobe
$\overline{REFRQ}$	:	Refresh Request
$\overline{RESET}$	:	Reset
X1, X2	:	Crystal
MODE	:	Mode
ANI0 to ANI7	:	Analog Input
ANO0, ANO1	:	Analog Output
AV_{REF1} to AV_{REF3}	:	Reference Voltage
AV_{DD}	:	Analog Power Supply
AV_{SS}	:	Analog Ground
V_{DD}	:	Power Supply
Vss	:	Ground
NC	:	Non-connection

SYSTEM CONFIGURATION EXAMPLE (LBP ENGINE)



INTERNAL BLOCK DIAGRAM



Note Internal ROM/RAM capacity varies depending on the product.

- **The μPD78233 /78237 cannot use P40 to P47, P50 to P57, P64 and P65 as ports.**

CONTENTS

1. PIN FUNCTIONS

1.1 PORTS

Pin Name	I/O	Dual-Function Pin	Function	
P00 to P07	Output	——	Port 0 (P0): Can be used as a real-time output port (4 bits × 2) Transistor drive capability.	
P10	Input/output	PWM0	Port 1 (P1): The input/output specifiable bit-wise. Input mode pins specifiable for on-chip pull-up resistor connection as a batch by software. LED drive capability.	
P11		PWM1		
P12 to P17		——		
P20	Input	NMI	Port 2 (P2): P20 cannot be used as a general-purpose port. (Non-maskable interrupt) However, the input level can be confirmed in the interrupt routine. The connection of the on-chip pull-up resistor can be specified as a 6-bit unit for P22 to P27 by software.	
P21		INTP0		
P22		INTP1		
P23		INTP2/CI		
P24		INTP3		
P25		INTP4/ASCK		
P26		INTP5		
P27		SI		
P30	Input/output	RxD	Port 3 (P3): The input/output specifiable bit-wise. Input mode pins specifiable for on-chip pull-up resistor connection as a batch by software.	
P31		TxD		
P32		$\overline{SCK}$		
P33		SO/SB0		
P34 to P37		TO0 to TO3		
P40 to P47*	Input/output	AD0 to AD7	Port 4 (P4): The input/output specifiable as an 8-bit unit. The connection of the on-chip pull-up resistor specifiable as a 8-bit unit by software.	LED drive capability
P50 to P57*	Input/output	A8 to A15	Port 5 (P5): The input/output specifiable bit-wise. Input mode pins specifiable for on-chip pull-up resistor connection as a batch by software.	
P60 to P63	Output	A16 to A19	Port 6 (P6): P64 to P67 enables to specify the input/output bit-wise. The connection of the on-chip pull-up resistor can be specified as a batch for P64 to P67 by software.	
P64*	Input/output	$\overline{RD}$		
P65*		$\overline{WR}$		
P66		$\overline{WAIT}$		
P67		$\overline{REFRQ}$		
P70 to P77	Input	ANI0 to ANI7	Port 7 (P7)	

* The μPD78233/78237 cannot use P40 to P47, P50 to P57, P64 and P65 as ports.

1.2 OTHER PORTS

Pin Name	I/O	Function	Dual-Function Pin
TO0 to TO3	Output	Timer output	P34 to P37
CI	Input	Count clock input to 8-bit timer/counter 2	P23 /INTP2
RxD	Input	Serial data input (UART)	P30
TxD	Output	Serial data output (UART)	P31
ASCK	Input	Baud rate clock input (UART)	P25/INTP4
SB0	Input /output	Serial data input/output (SBI)	P33/SO
SI	Input	Serial data input (3-wire serial I/O)	P27
SO	Output	Serial data output (3-wire serial I/O)	P33/SB0
$\overline{SCK}$	Input /output	Serial clock input/output (SBI, 3-wire serial I/O)	P32
NMI	Input	External interrupt request	P20
INTP0			P21
INTP1			P22
INTP2			P23/CI
INTP3			P24
INTP4			P25/ASCK
INTP5			P26
AD0 to AD7	Input /output	Time multiplexing address/data bus (external memory connection)	P40 to P47*
A8 to A15	Output	Upper address bus (external memory connection)	P50 to P57*
A16 to A19	Output	Upper address when extending address (external memory connection)	P60 to P63
$\overline{RD}$	Output	Read strobe into external memory	P64*
$\overline{WR}$	Output	Write strobe into external memory	P65*
$\overline{WAIT}$	Input	Wait insertion	P66
ASTB	Output	Time multiplexing address (A0 to A7) latch timing output (at external memory accessed)	—
$\overline{REFRQ}$	Output	Refresh pulse output into external pseudo-static memory	P67
$\overline{RESET}$	Input	Chip reset	—
X1	Input	Crystal connection for system clock oscillation (capability of clock input to X1)	—
X2	—		
MODE	Input	ROM-less operating specification (external access of the same space as internal ROM). This is used by high level in μPD78233, μPD78237 and by low level in μPD78234, μPD78238.	—
ANI0 to ANI7	Input	Analog voltage input for A/D converter	P70 to P77
ANO0, ANO1	Output	Analog voltage output for D/A converter	—
AV_{REF1}	—	Reference voltage apply for A/D converter	—
AV_{REF2}, AV_{REF3}		Reference voltage apply for D/A converter	
AV_{DD}		Positive power supply for A/D converter	
AV_{SS}		GND for A/D converter	
V_{DD}		Positive power supply	
V_{SS}		GND	
NC		Not connected internally	

* The μPD78233/78237 cannot use P40 to P47, P50 to P57, P64 and P65 as ports.

1.3 PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 1-1. For the input/output circuit configuration of each type, see Fig. 1-1.

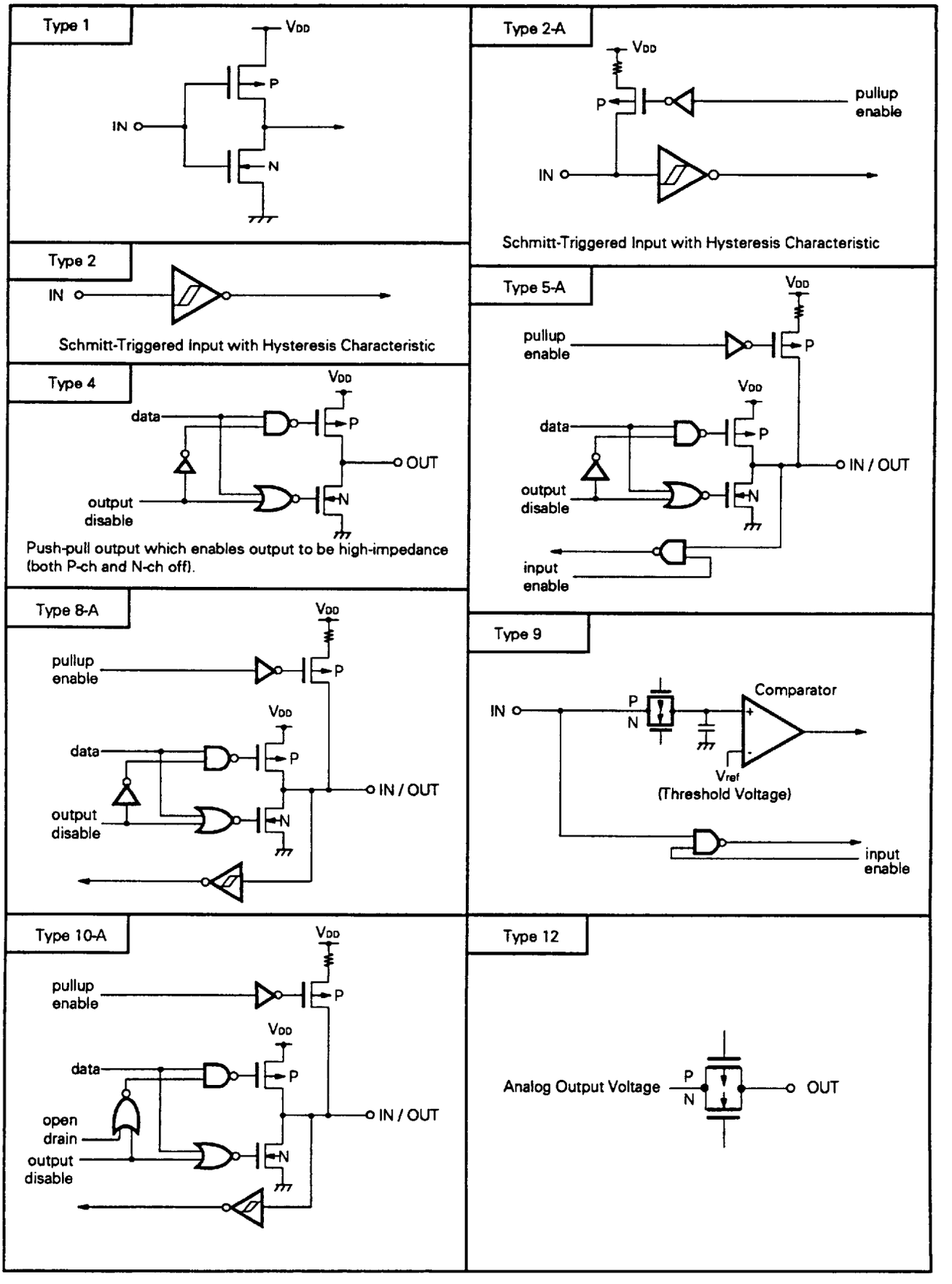
Table 1-1 Input/Output Circuit Type of Each Pin and Recommended Connection of Unused Pins

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection when not Used
P00 to P07	4	Output	Leave open.
P10 to P17	5-A	Input/output	Input : Connected to V_{DD}. Output : Leave open.
P20/NMI	2	Input	Connected to V_{DD} or Vss.
P21/INTP0			
P22/INTP1	2-A		Connected to V_{DD}.
P23/INTP2/CI			
P24/INTP3			
P25/INTP4/ASCK			
P26/INTP5			
P27/SI			
P30/RxD	5-A	Input/output	Input : Connected to V_{DD}. Output : Leave open.
P31/TxD			
P32/$\overline{SCK}$	8-A		
P33/SB0/SO	10-A		
P34/TO0 to P37/TO3	5-A		
P40/AD0 to P47/AD7			
P50/A8 to P57/A15			
P60/A16 to P63/A19	4	Output	Leave open.
P64/$\overline{RD}$	5-A	Input/output	Input : Connected to V_{DD}. Output : Leave open.
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/$\overline{REFRQ}$			
P70/ANI0 to P77/ANI7	9	Input	Connected to Vss.
ANO0, ANO1	12	Output	Leave open.
ASTB	4		
$\overline{RESET}$	2	Input	———
MODE	1		
AV_{REF1} to AV_{REF3}	———		Connected to Vss.
AVss			
AV_{DD}			Connected to V_{DD}.

Remarks The type numbers are standardized by 78K series, therefore they are not always consecutive numbers in each product. (Some circuit is not incorporated.)

Note **If the input and output modes are not stable on the pin which has an input/output dual-function, connect to V_{DD} via tens of kΩ resistor. (Especially, if the reset input pin exceeds the low-level input voltage at power-on or in case of change the input/output by software.)** ★

Fig. 1-1 Pin Input/Output Circuits



2. INTERNAL BLOCK FUNCTION

2.1 MEMORY SPACE

The μPD78233, 78234, 78237 and 78238 can access a 1M-byte memory space. Figs. 2-1 and 2-2 show that memory space. The program memory mapping depends on the MODE pin status.

(1) μPD78233 (MODE = H)

The program memory is mapped into the external memory(64640 bytes: 00000H to 0FC7FH). This area is shareable with a data memory.

The data memory has been mapped into the internal RAM (640 bytes: 0FC80H to 0FEFFH). In the 1M-byte extended mode, the external memory (960K bytes: 10000H to FFFFFH) is mapped as the expansion data memory.

(2) μPD78234 (MODE = L)

The program memory has been mapped onto the internal ROM (16K bytes: 00000H to 03FFFH) and the external memory (48256 bytes: 04000H to 0FC7FH). The external memory is accessed by the external memory expansion mode. The mapping area into the external memory is shareable with the data memory.

The data memory has been mapped into the internal RAM (640 bytes: 0FC80H to 0FEFFH). In the 1M-byte expansion mode, the external memory (960K bytes: 10000H to FFFFFH) is mapped as a expansion data memory.

(3) μPD78237 (MODE = H)

The program memory is mapped onto the external memory (64256 bytes: 00000H to 0FAFFH). This area is shareable with a data memory.

The data memory has been mapped onto the internal RAM (1024 bytes: 0FB00H to 0FEFFH). In the 1M-byte extended mode, the external memory (960K bytes: 10000H to FFFFFH) is mapped as an expansion data memory.

(4) μPD78238 (MODE = L)

The program memory has been mapped onto the internal ROM (32K bytes: 00000H to 07FFFH) and the external memory (31488 bytes: 08000H to 0FAFFH). The external memory is accessed by the external memory expansion mode. The mapping area into the external memory is shareable with the data memory.

The data memory has been mapped onto the internal RAM (1024 bytes: 0FB00H to 0FEFFH). In the 1M-byte extended mode, the external memory (960K bytes: 10000H to FFFFFH) is mapped as an expansion data memory.

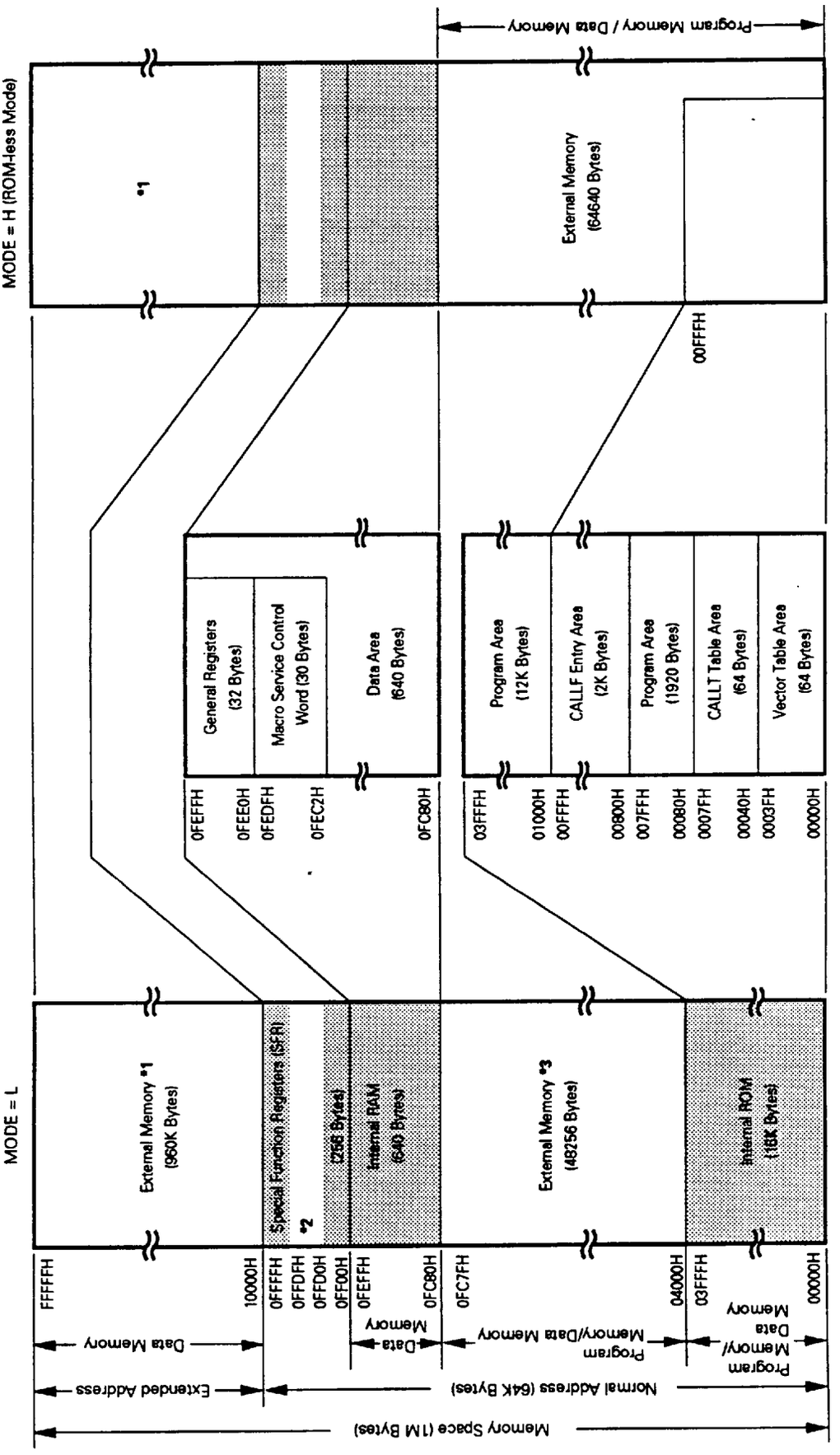


Fig. 2-1 μPD78233/78234 Memory Map

* 1. Accessed by 1M-byte extended mode.
2. Accessed by external memory expansion mode.
3. μPD78233 only when MODE = H

Shaded area denotes internal memory.

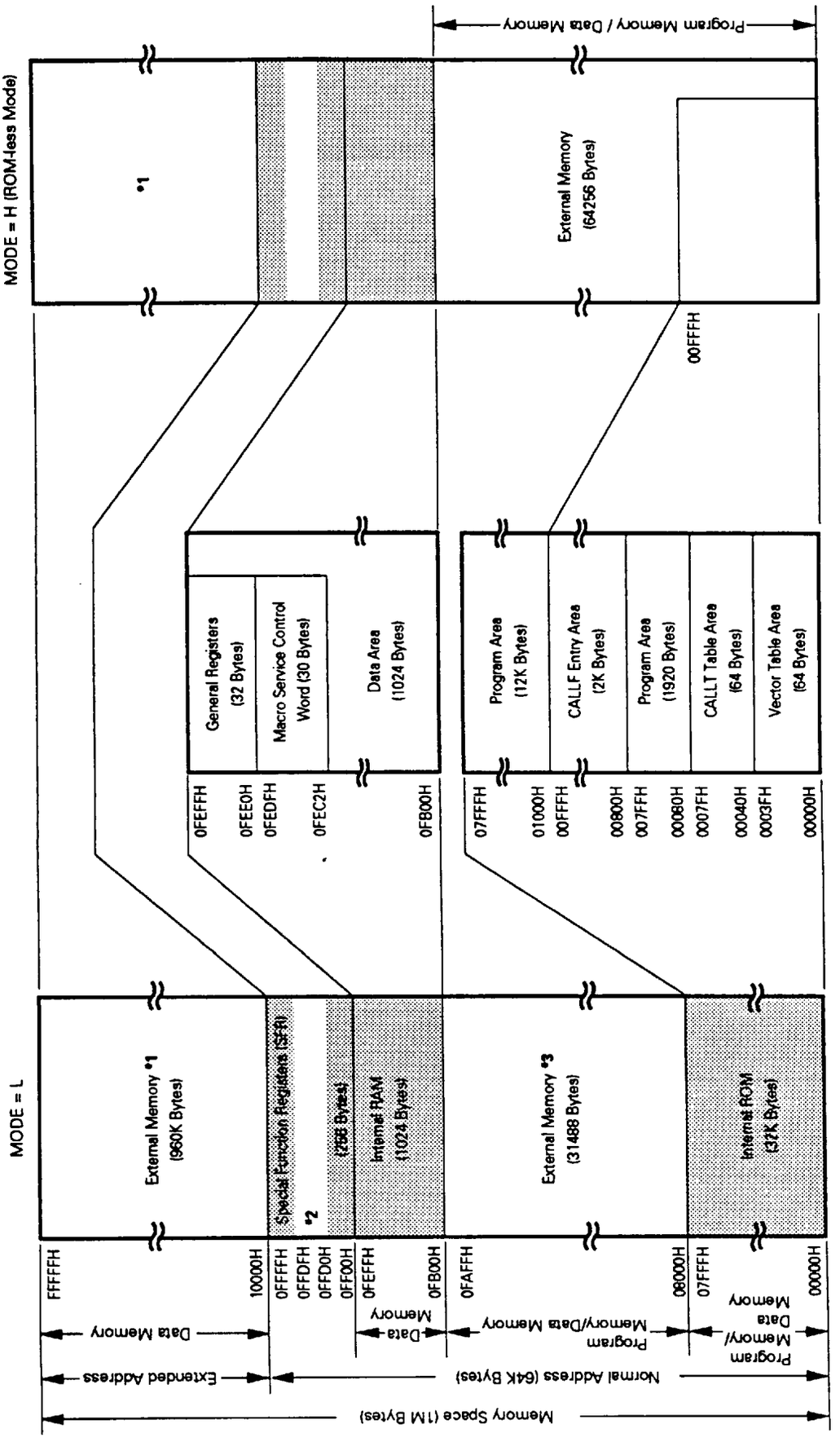


Fig. 2-2 μPD78237/78238 Memory Map

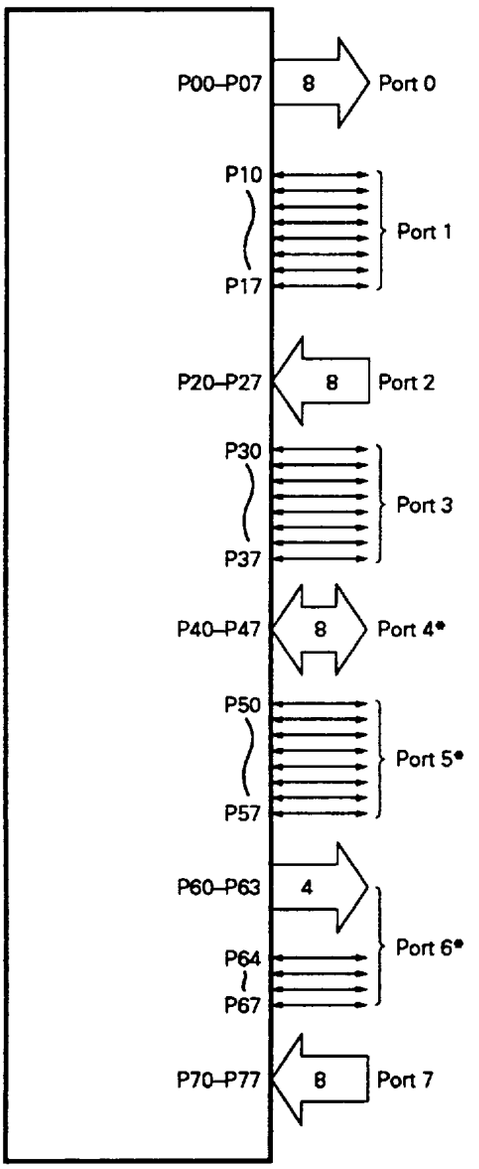
Shaded area denotes internal memory.

* 1. Accessed by 1M-byte extended mode.
  2. Accessed by external memory expansion mode.
  3. μPD78237 only when MODE = H

2.2 PORT

The μPD78233, 78234, 78237 and 78238 are equipped with ports as Fig. 2-3, operable for various controls. The function of each port describes Table 2-1. The port 1 to port 6 can be specified to use the internal pull-up resistor by software at input.

Fig. 2-3 Port Configuration



* The μPD78233/78237 cannot use P40 to P47, P50 to P57, P64 and P65 as ports.

Table 2-1 Port Function

Name	Pin Name	Function	Designation of Software Pull-Up
Port 0	P00 to P07	Outputs or high-impedance specifiable as an 8-bit unit. Also operable as 4-bit real-time output (P00 to P03, P04 to P07). Transistor drive capability.	———
Port 1	P10 to P17	Input or output specifiable bit-wise. LED drive capability.	Input mode pins specifiable as a batch
Port 2	P20 to P27	Input port	6-bit unit (P22 to P27)
Port 3	P30 to P37	Input or output specifiable bit-wise.	Input mode pins specifiable as a batch
Port 4*	P40 to P47	Input or output specifiable as an 8-bit unit. LED drive capability.	8-bit unit
Port 5*	P50 to P57	Input or output specifiable bit-wise. LED drive capability.	Input mode pins specifiable as a batch
Port 6*	P60 to P63	Output port	———
	P64 to P67	Input or output specifiable bit-wise.	Input mode pins specifiable as a batch
Port 7	P70 to P77	Input port	———

* The μPD78233/78237 cannot use P40 to P47, P50 to P57, P64 and P65 as ports.

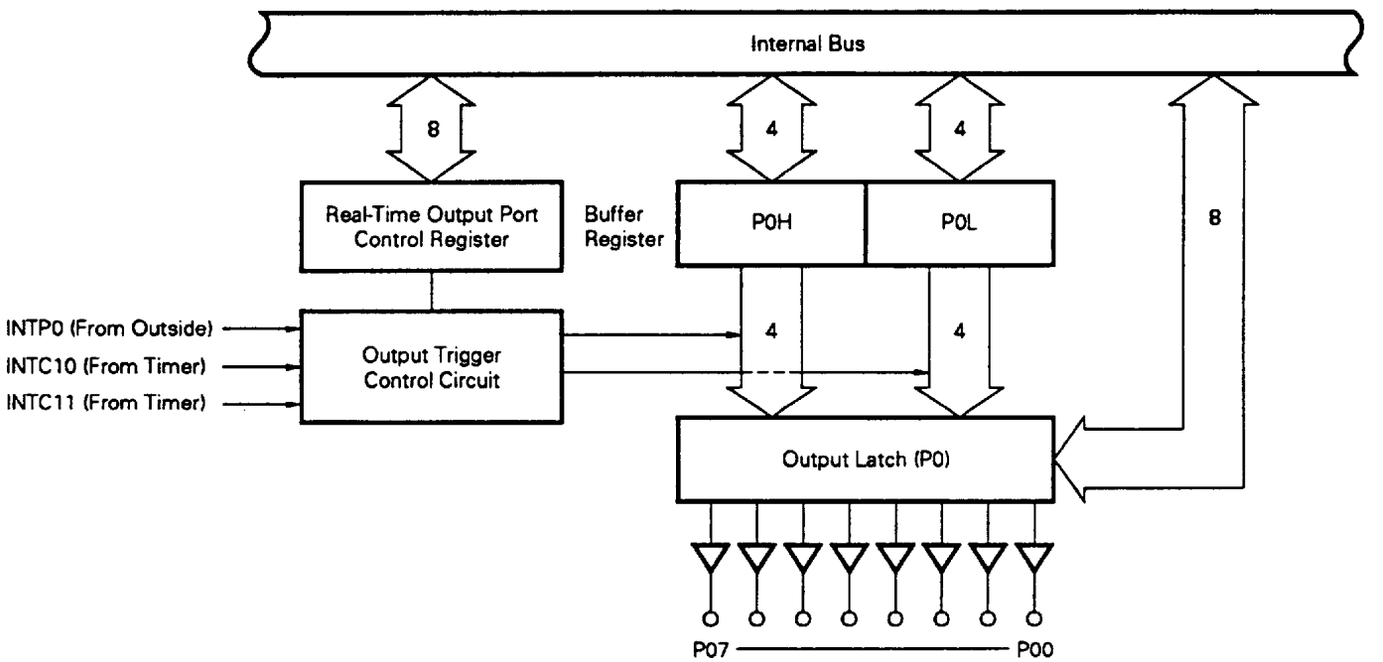
2.3 REAL-TIME OUTPUT PORT

The real-time output port outputs the data stored in the buffer in synchronization with a timer match interrupt or external interrupt. Therefore, a pulse output without jitter can be acquired.

Accordingly, this is suitable for the application (open loop control of a stepping motor etc.) which outputs any pattern at any interval.

As Fig. 2-4, the port 0 and buffer register are the core of the configuration.

Fig. 2-4 Real-Time Output Port Block Diagram



2.4 TIMER/COUNTER UNIT

The μPD78233, 78234, 78237 and 78238 incorporate one channel of a 16-bit timer/ counter unit and 3 channels of an 8-bit timer/counter unit.

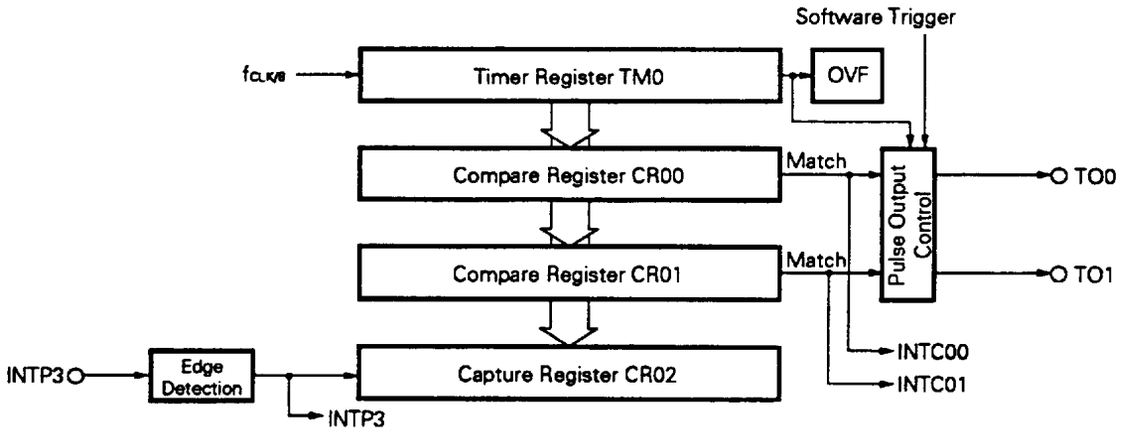
Table 2-2 Types and Functions for Timer/Counter

Type & Function \ Unit		16-Bit Timer/ Counter	8-Bit Timer/ Counter 1	8-Bit Timer/ Counter 2	8-Bit Timer/ Counter 3
Type	Interval timer	2ch	2ch	2ch	1ch
	External event counter	—	—	○	—
	One-shot timer	—	—	○	—
Function	Timer output	2ch	—	2ch	—
	Toggle output	○	—	○	—
	PWM/PPG output	○	—	○	—
	One-shot pulse output	○	—	—	—
	Real-time output	—	○	—	—
	Pulse amplitude measurement	○	○	○	—
	Number of interrupt requests	2	2	2	1
	Clock source of serial interface	—	—	—	○

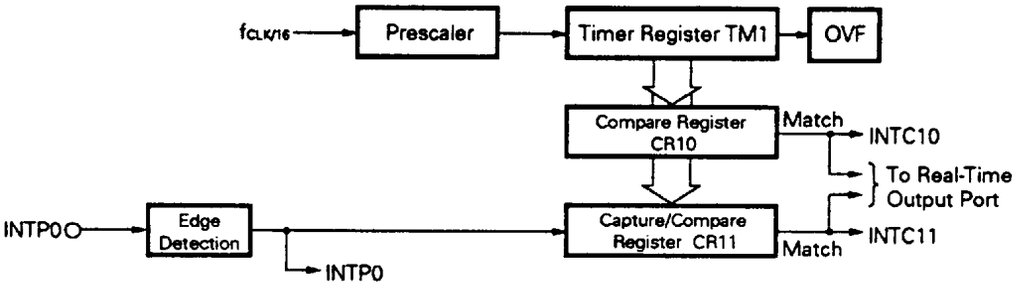
As 7 interrupt requests are supported in total, this functions as the timer of the 7 channels.

Fig. 2-5 Timer/Counter Unit Block Diagram

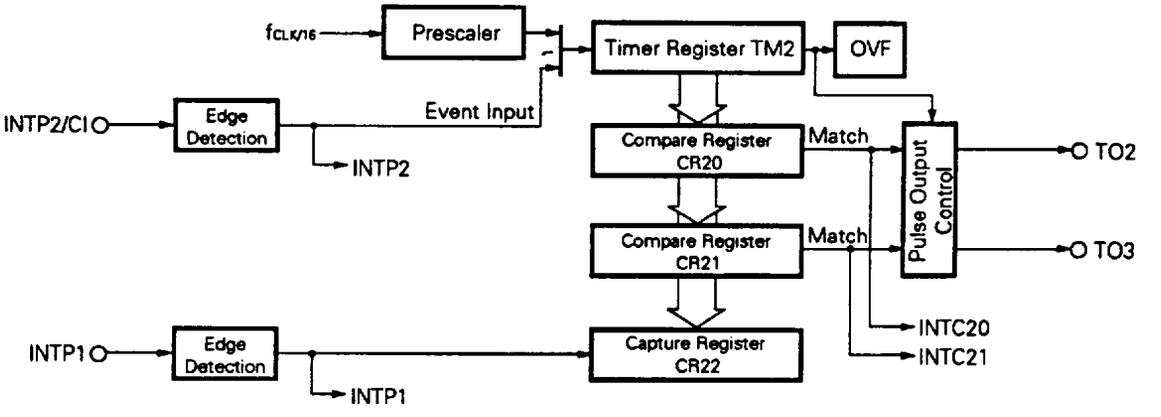
16-bit timer/counter unit



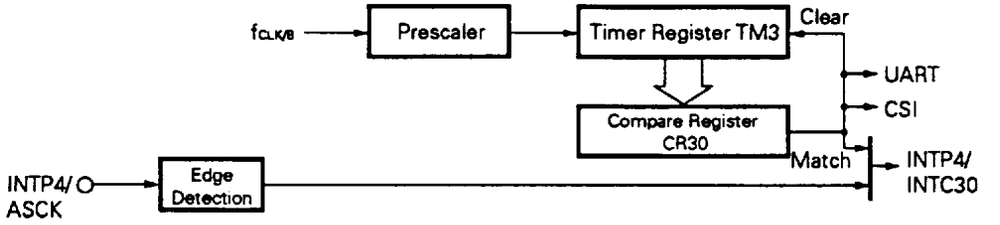
8-bit timer/counter unit 1



8-bit timer/counter unit 2



8-bit timer/counter unit 3

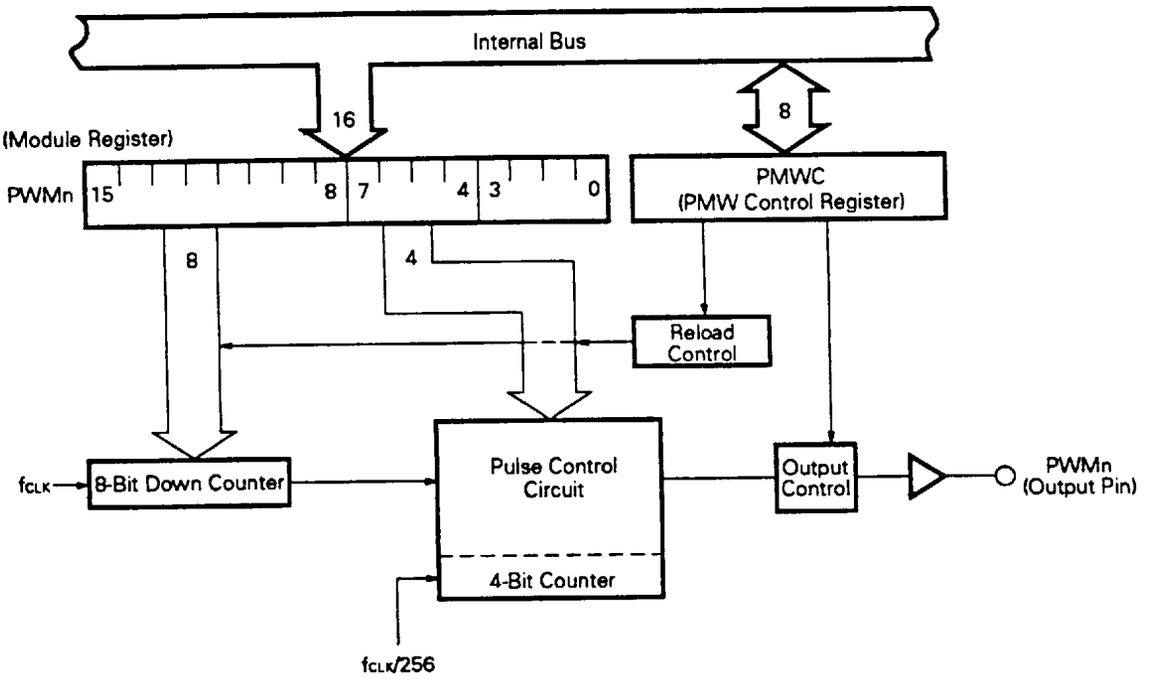


OVF : Overflow Flag

2.5 PWM OUTPUT (PWM0, PWM1)

The μPD78233, 78234, 78237 and 78238 have an on-chip 12-bit resolution PWM (Pulse Width Modulation) with 23.4 kHz repeat frequency (f_{CLK} = 6 MHz) output circuit for two channels. The active level of these channels can be selected independently as high or low level. This output is perfect for DC motor speed control.

Fig. 2-6 PWM Output Unit Block Diagram (n = 0, 1)



2.6 A/D CONVERTER

An analog/digital (A/D) converter with 8 multiplexed analog inputs (ANI0 to ANI7) is incorporated.

The conversion is a successive approximation and the conversion result is stored in the 8-bit A/D conversion result register (ADCR). Therefore, the conversion can be executed at high speed and accuracy (converting time: approximately 20 μs at 12 MHz operation).

This prepares the following modes to start the A/D converting operation.

- ○ Hardware start: Starts the conversion with a trigger input (INTP5).
- ○ Software start : Starts the conversion by setting a bit of A/D converter mode register (ADM).

Also, the following modes are prepared for the operation after started.

- ○ Scan mode : Selects analog inputs one after another and acquires the converted data from all pins.
- ○ Select mode : Fixes analog inputs to one pin and acquires the continuous conversion value.

When stopping the above modes and the converting operation, all of them are specified by ADM.

The interrupt request (INTAD) occurs when the converted result is sent to ADCR (except for software start select mode). Therefore, by a macro service, the converted values can be sent into the memory continuously.

Table 2-3 INTAD Generation Mode

	Scan Mode	Select Mode
Hardware start	○	○
Software start	○	—

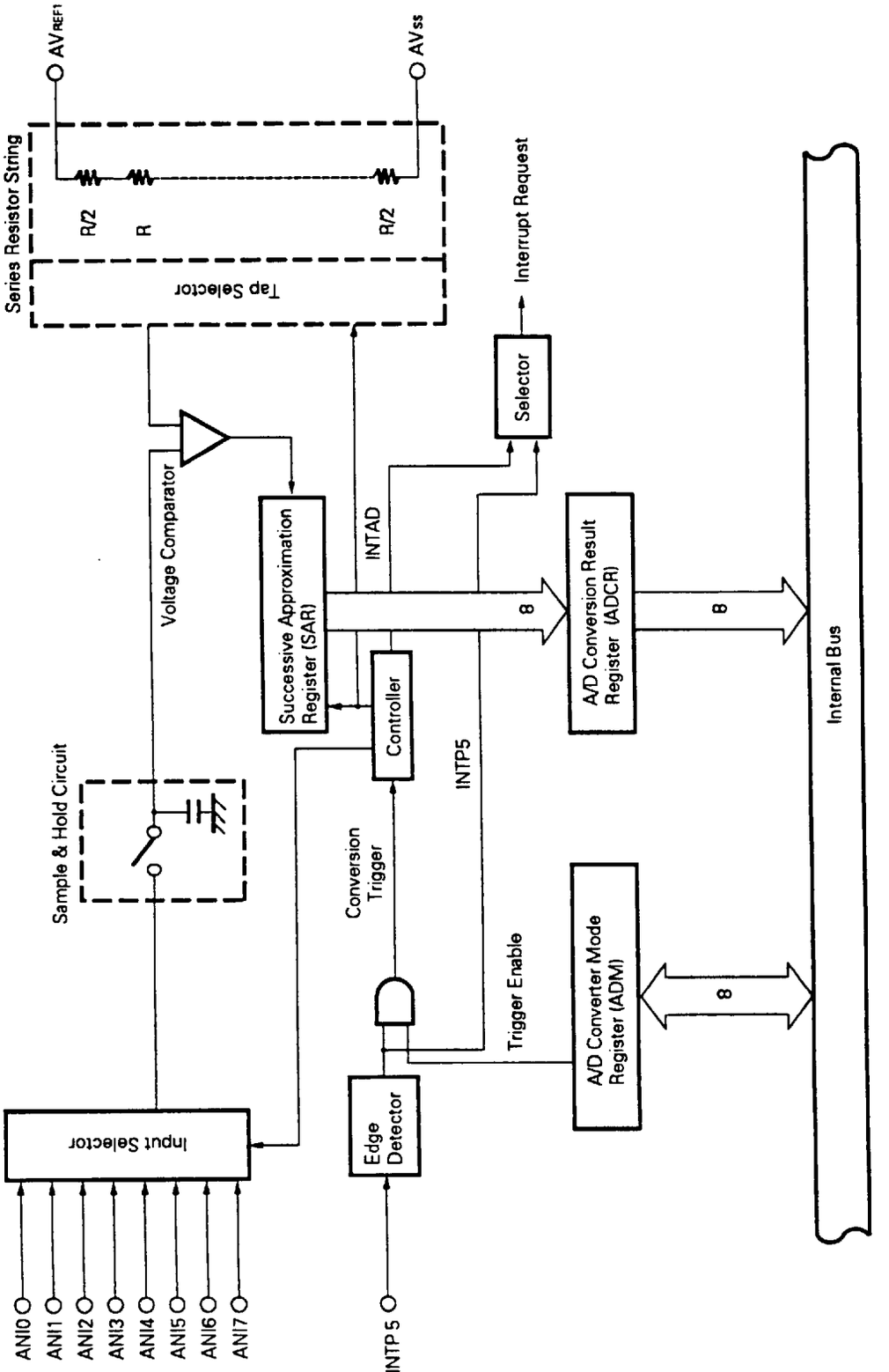


Fig. 2-7 A/D Converter Block Diagram

2.7 D/A CONVERTER

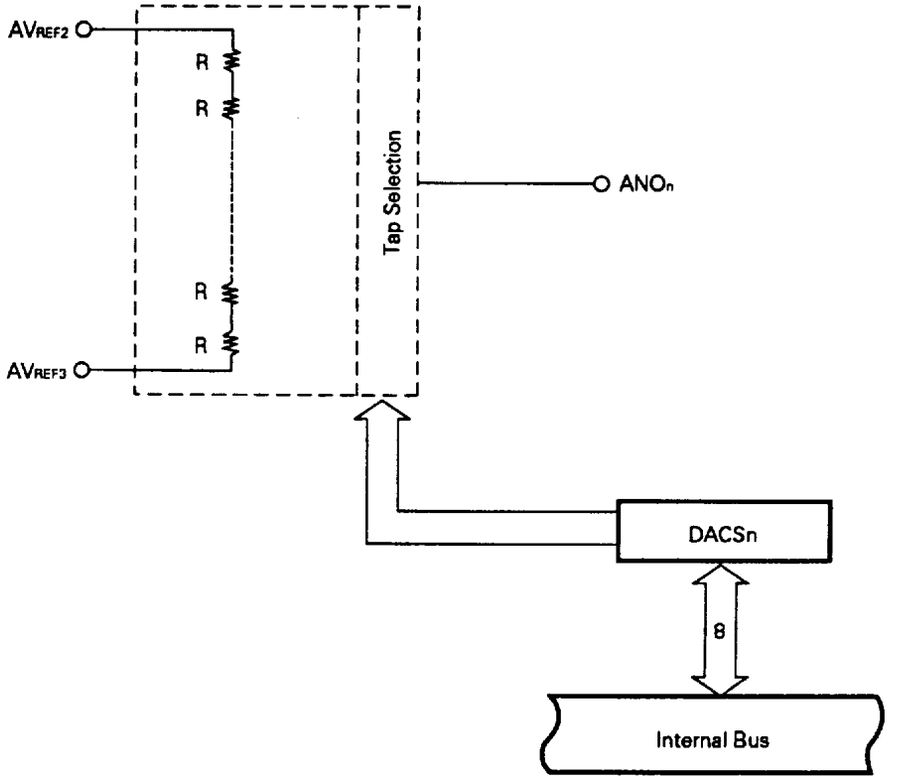
Two 8-bit resolution voltage output type digital/analog (D/A) converters are incorporated.

The conversion method is resistance string. The value to be output is written in 8-bit D/A conversion value setting register DACSn and the analog value is output to the ANOn pin. The voltage applied to the AV_{REF2} pin and AV_{REF3} pin determines the output voltage range.

Since the output impedance is high, a current cannot be taken from the output. When the load impedance is low, use by inserting a buffer amp between the output and the load.

The ANOn pin becomes high impedance during the period the $\overline{RESET}$ signal is low level. After reset is cleared, the DACSn register becomes 0.

Fig. 2-8 D/A Converter Block Diagram (n = 0, 1)



2.8 SERIAL INTERFACE

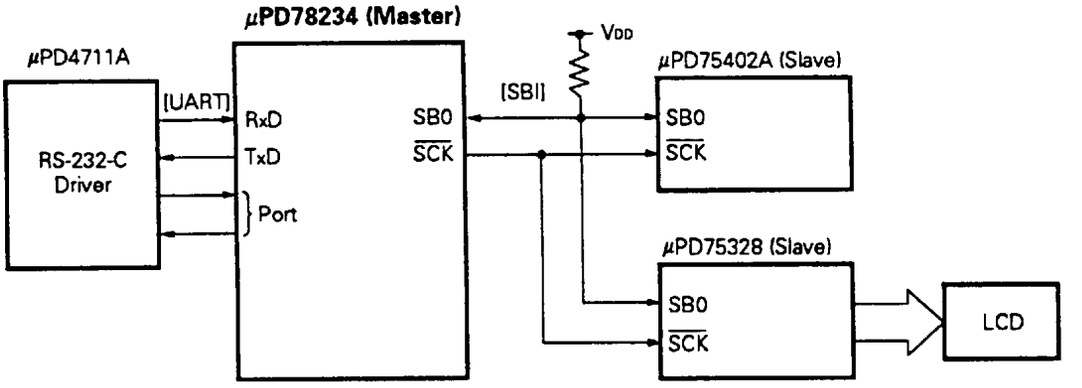
The μPD78233, 78234, 78237 and 78238 are equipped with 2 independent channels for serial interfaces.

- ○ Asynchronous serial interface (UART)
- ○ Clocked serial interface
  - • 3-wire serial I/O
  - • Serial bus interface (SBI)

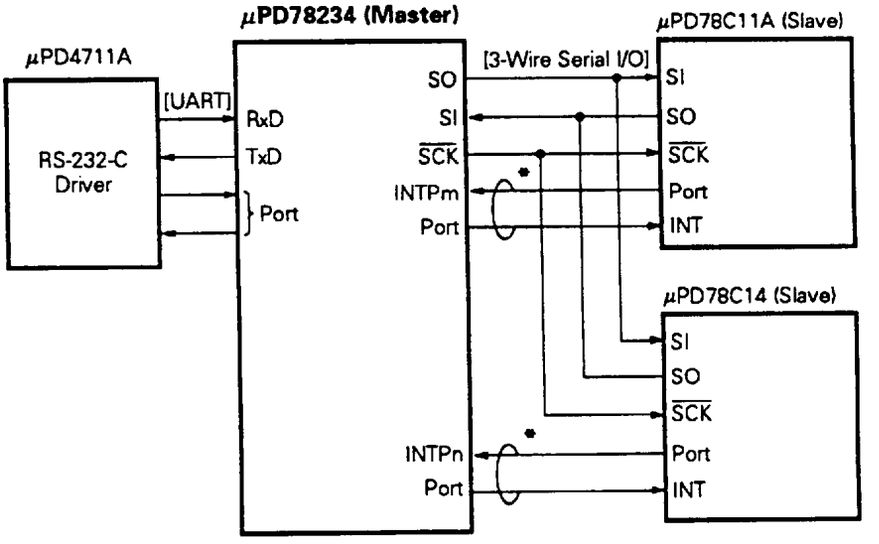
This enables both a communication with the external system and a local communication in the system simultaneously (see Fig. 2-9).

Fig. 2-9 Example of Serial Interface

(a) UART + SBI



(b) UART + 3-wire serial I/O



* Handshake line

2.8.1 Asynchronous Serial Interface

A UART (Universal Asynchronous Receiver Transmitter) has been incorporated as an asynchronous serial interface. This is the method to transmit the one byte data following the start bit.

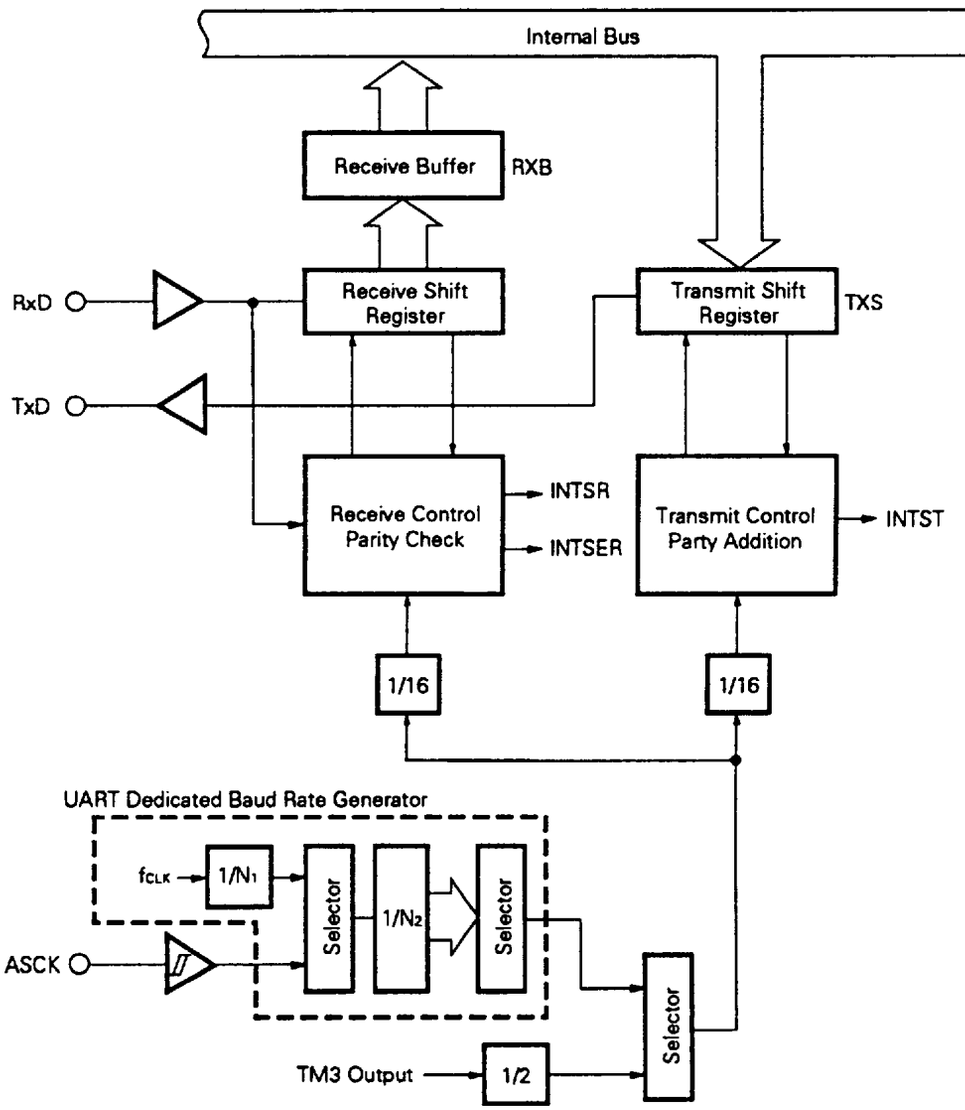
As UART dedicated baud rate generator is incorporated, communications are possible with a wide range of any baud rate.

Also, the baud rate can be defined by dividing the input clock for the ASCK pin.

Moreover, a baud rate can be generated with 8-bit timer/ counter 3.

If the UART dedicated baud rate generator is used, the baud rate (31.25 kbps) of the MIDI specification can be acquired.

Fig. 2-10 Asynchronous Serial Interface Block Diagram

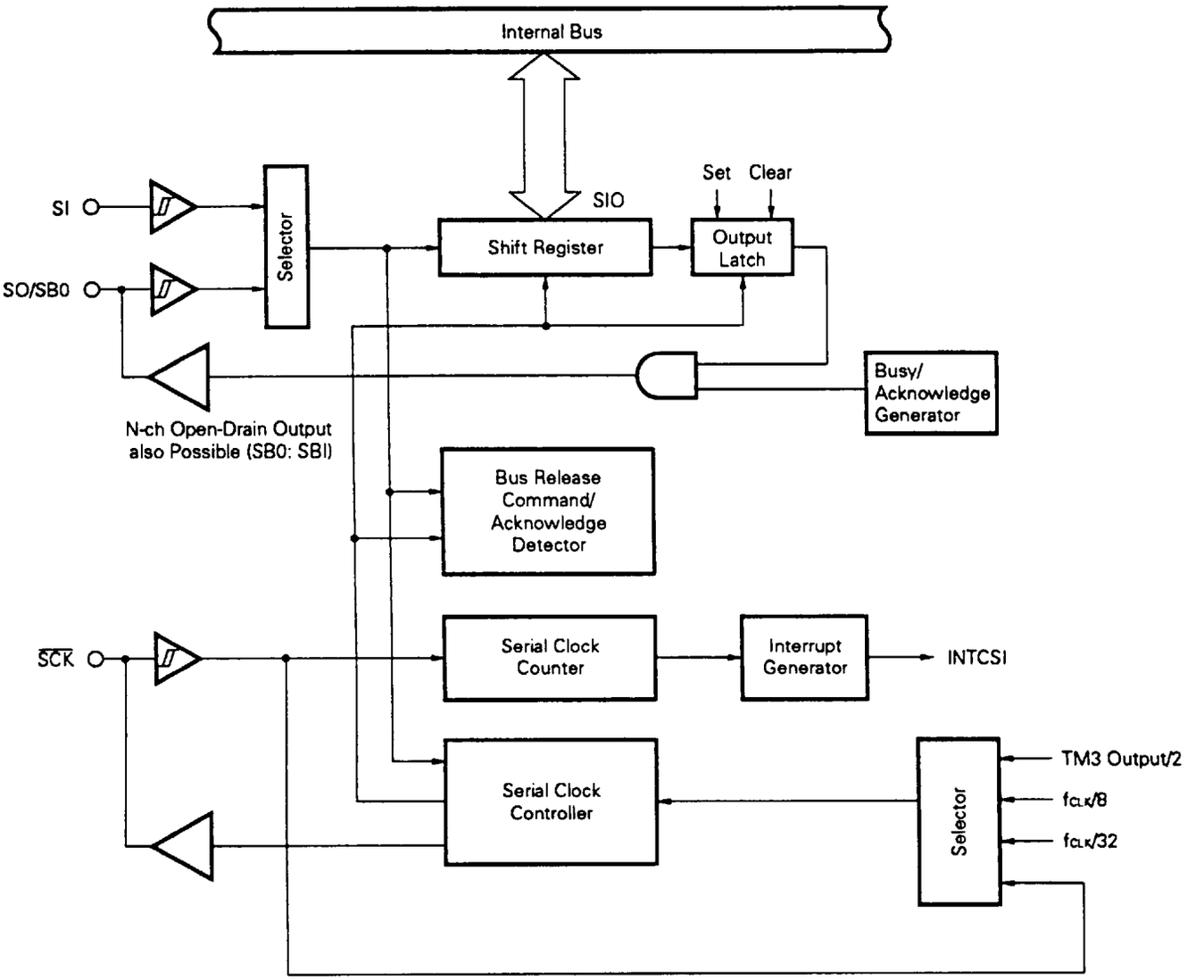


f_{CLK} : Internal system clock frequency (system clock frequency / 2)

2.8.2 Clocked Serial Interface

This is a method to communicate one byte data in synchronization with the serial clock which is activated by master device and starts to transmit.

Fig. 2-11 Clocked Serial Interface Block Diagram



f_{CLK} : Internal system clock frequency (system clock frequency / 2)

(1) 3-wire serial I/O

This is a interface to communicate with a device which incorporates a conventional clocked serial interface.

Basically, the communication is made through 3 wires of serial clock ($\overline{SCK}$) and serial data (SI, SO). In case of connecting with multiple device, the handshake line is required.

(2) SBI

This can communicate with a multiple device through 2 wires of serial clock ($\overline{SCK}$) and serial bus (SB0) and this is a NEC standard serial interface.

The master device outputs "address" from the SB0 pin and selects the communicated slave device. Then, "command" and "data" are transmitted and received between the master and slave.

3. INTERNAL/EXTERNAL CONTROL FUNCTION

3.1 INTERRUPT

The interrupt request servicing can be selected from 2 service modes in the following table.

Table 3-1 Interrupt Request Servicing

Service Mode	Servicing Subject	Service	PC, PSW Contents
Vectored interrupt	Software	Branches to service routine, and executes (any service contents)	With save and return
Macro service	Firmware	Data transmission etc. between memory and I/O (fixed service contents)	Hold

3.1.1 Interrupt Source

The interrupt source includes the 19 types and a BRK instruction execution as shown in Table 3-2.

The priority of the interrupt servicing can be set to 2 levels (high and low priority levels). Therefore, it can separate the levels of the nest control which the interrupt is in progress and the interrupt request which occurs simultaneously (see **Figs. 3-1, 3-2**). But the nesting advances certainly in the macro service (not held).

The default priority is the priority level (fixed) to service the interrupt requests which occur at the same level simultaneously (see **Fig. 3-2**).

Table 3-2 Interrupt Source

Type	Default Priority	Source		Internal/ External	Macro Service
		Name	Trigger		
Software	—	BRK	Instruction execution	—	—
Non-maskable		NMI	Pin input edge detection	External	
Maskable	0 (highest)	INTP0	Pin input edge detection (TM1 capture trigger)		○
	1	INTP1	Pin input edge detection (TM2 capture trigger)		
	2	INTP2	Pin input edge detection (TM2 event counter input)		
	3	INTP3	Pin input edge detection (TM0 capture trigger)		
	4	INTC00	TM0 to CR00 match signal generation	Internal	
	5	INTC01	TM0 to CR01 match signal generation		
	6	INTC10	TM1 to CR10 match signal generation		
	7	INTC11	TM1 to CR11 match signal generation		
	8	INTC21	TM2 to CR21 match signal generation		
	9	INTP4	Pin input edge detection	External	
		INTC30	TM3 to CR30 match signal generation	Internal	
	10	INTP5	Pin input edge detection	External	
		INTAD	A/D converter conversion termination (transfer to ADCR)	Internal	
	11	INTC20	TM2 to CR20 match signal generation		
	12	INTSER	ASI receive error generation		—
	13	INTSR	ASI receive termination		○
	14	INTST	ASI transmit termination		
	15 (lowest)	INTCSI	CSI transfer termination		

TM0 : 16-bit timer
TM1 to TM3 : 8-bit timer
ASI : Asynchronous serial interface
CSI : Clocked serial interface

Fig. 3-1 Servicing Example for Another Interrupt Request Occurrence while an Interrupt Servicing

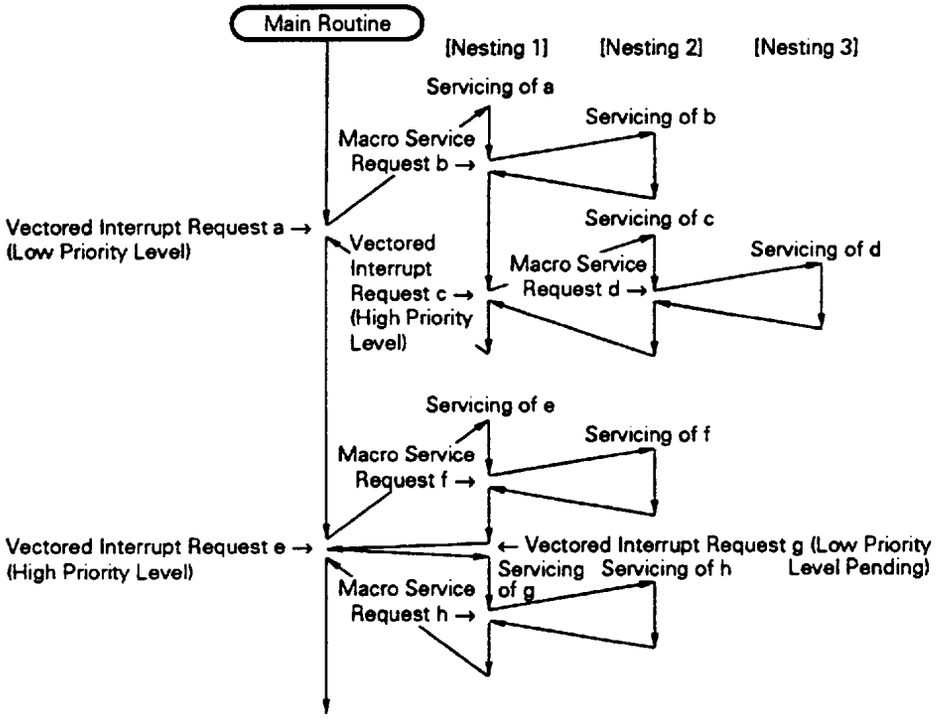
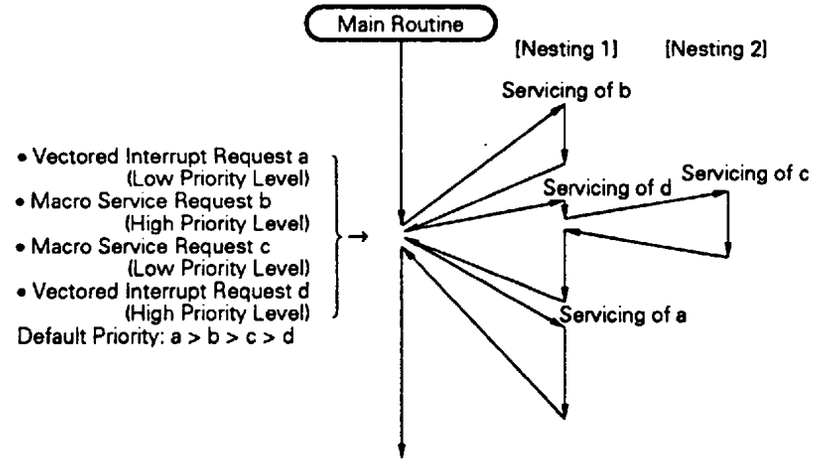


Fig. 3-2 Servicing Example for Simultaneous Occurred Interrupt Request



3.1.2 Vectored Interrupt

The memory contents of the vector table address, which corresponds to the interrupt source, is branched into the processing routine as a destination address.

As the CPU executes the interrupt servicing, the following operations occur.

- O When branch: Saving the CPU status (PC, PSW contents) to the stack.
- O When return : Returning the CPU status (PC, PSW contents) from the stack.

The RETI instruction executes returning to the main routine from the processing routine.

Table 3-3 Vector Table Address

Interrupt Source	Vector Table Address
BRK	003EH
NMI	0002H
INTP0	0006H
INTP1	0008H
INTP2	000AH
INTP3	000CH
INTC00	0014H
INTC01	0016H
INTC10	0018H
INTC11	001AH

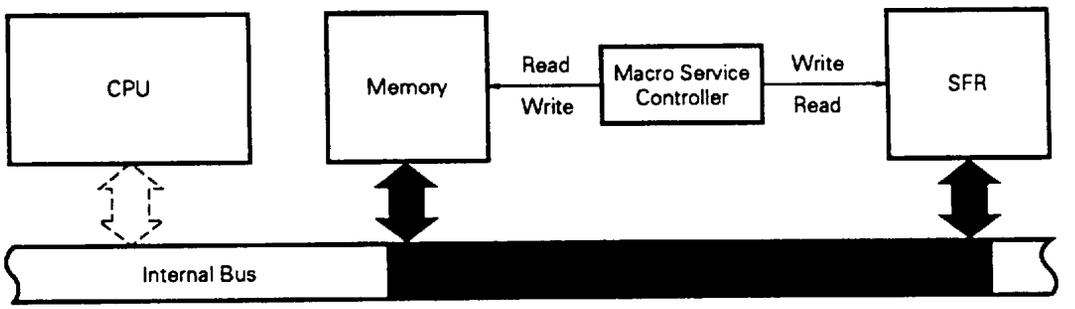
Interrupt Source	Vector Table Address
INTC21	001CH
INTP4	000EH
INTC30	
INTP5	0010H
INTAD	
INTC20	0012H
INTSER	0020H
INTSR	0022H
INTST	0024H
INTCSI	0026H

3.1.3 Macro Service

This is a function to transfer the data between the memory special functional registers (SFR) without CPU operation. The macro service controller accesses the memory and SFR during the same transfer cycle, and transfers directly without data collection.

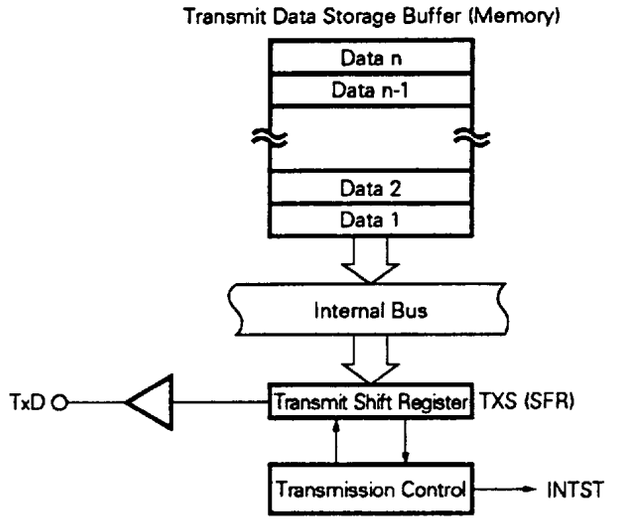
The high-speed data transfer is enabled because no data is saved, returned nor fetched.

Fig. 3-3 Macro Service



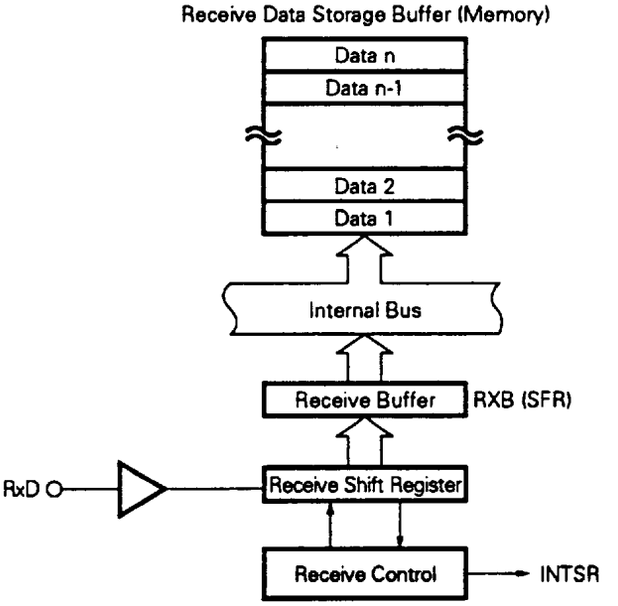
3.1.4 Macro Service Application Example

(1) Transmit operation of serial interface



Whenever the macro service request INTST is generated, the next send data is transferred to TXS from the memory. When the data n (last byte) is transferred to TXS (The transmit data storage buffer becomes empty.), a vectored interrupt request INTST is generated.

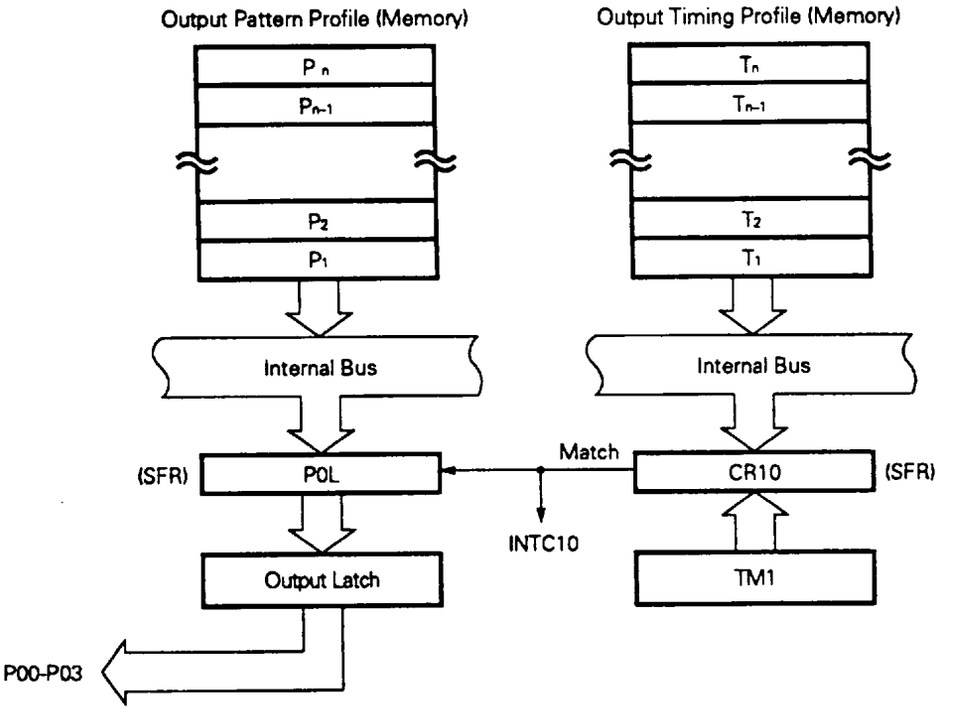
(2) Receive operation of serial interface



Whenever the macro service request INTSR is generated, the receive data is transferred to the memory from RXB. When the data n (last byte) is transferred to the memory (The receive data storage buffer becomes empty.), the vectored interrupt request INTSR is generated.

(3) Real-time output port

The INTC10 and INTC11 become output triggers of the real-time output port. In the macro service to them, the next output pattern and interval can be set simultaneously. Therefore, the INTC10 and INTC11 can control 2 system stepping motor independently. Also, it can be applied to control a PWM or DC motor, etc.



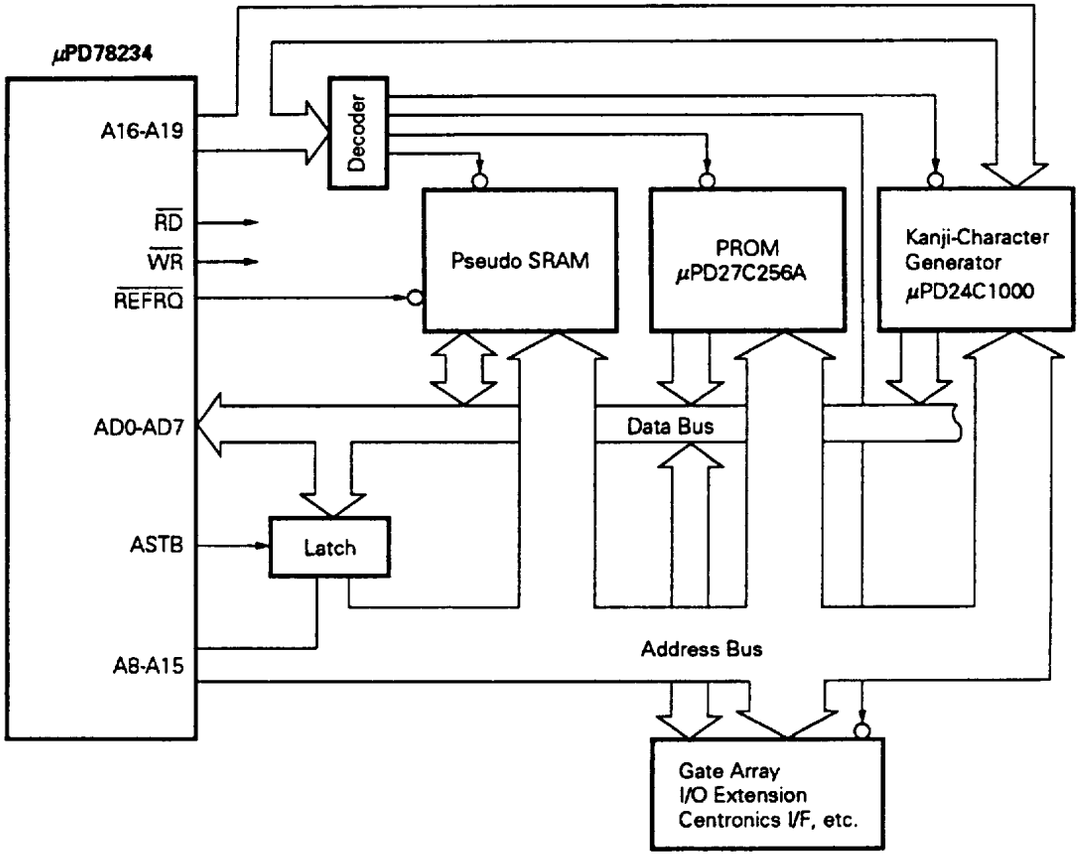
Whenever the macro service request INTC10 is generated, the pattern and timing are transferred to P0L and CR10 respectively. When the contents of the TM1 match with the contents of the CR10, the next INTC10 is generated and the contents of the P0L is sent to the output latch. If Tn (last byte) is sent to CR10, a vectored interrupt request INTC10 is generated.

The same operation is available for INTC11 (different point: CR10 → CR11, P0L → P0H, P00 to P03 → P04 to P07).

3.2 LOCAL BUS INTERFACE

A memory and an I/O (memory mapped I/O) can be connected externally and the 1M-byte memory space is supported (see **Figs. 2-1, 2-2**).

Fig. 3-4 Local Bus Interface Example



3.2.1 Memory Expansion

The following modes have been prepared as a memory expansion function.

- ○ External memory expansion mode:
  Expands the program memory and data memory to 48256 bytes externally. But this area can be used unconditionally under the ROM-less mode (MODE=H).
- ○ 1M-byte expansion mode:
  Expands the data memory by 960K bytes and become a 1M-byte memory space.

3.2.2 Programmable Wait

A wait can be independently inserted to the memory mapped on both a normal address (μPD78233, 78234: 00000H to 0FC7FH, μPD78237, 78238: 00000H to 0FAFFH) and an extended address (10000H to FFFFFH). Therefore, the efficiency of the entire system is not decreased.

3.2.3 Pseudo-Static RAM Refresh Function

The refresh operations are as follows.

- ○ Pulse refresh:
  Outputs the refresh pulse to $\overline{\text{REFRQ}}$ pin in synchronization with a bus cycle.
- ○ Power-down self refresh:
  Outputs a low-level to the $\overline{\text{REFRQ}}$ pin in the standby mode and holds the contents of pseudo-static RAM.

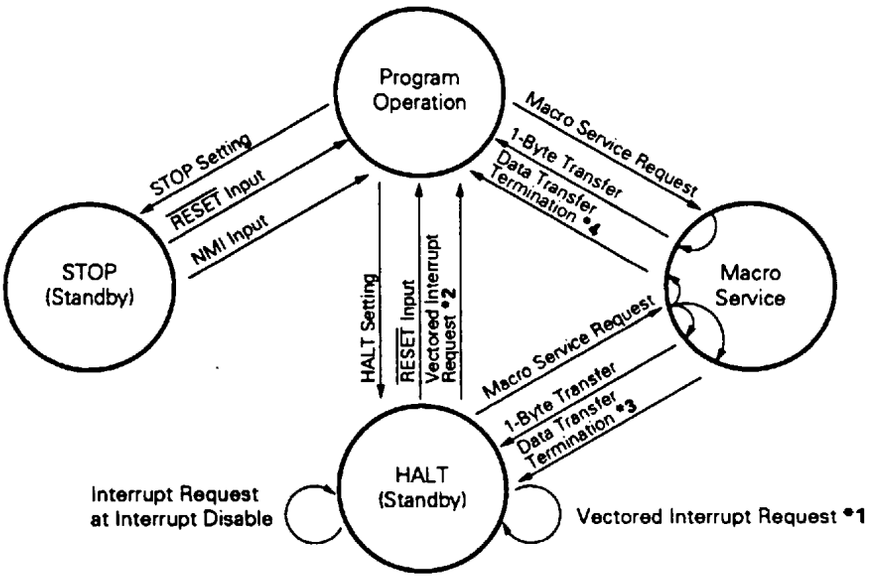
3.3 STANDBY

This is a function to reduce the power consumption of the chip. The following modes have been prepared.

- O HALT mode: Stops the operation clock of the CPU. The average power consumption is reduced by the normal operation and the intermittent operation during normal operations.
- O STOP mode: Stops the oscillator. This stops all operation in the chip and makes the minute power consumption status only with leakage current.

These modes are programmable.
Also, the macro service is started from the HALT mode.

Fig. 3-5 Standby Status Flow



* 1. In case a vectored interrupt request is a low priority level (status to disable interrupt of a low priority sequence under the HALT setting).
2. In case a vectored interrupt request is a high priority level or the status to enable interrupt of a low priority sequence under the HALT setting.
3. In case a macro service is a low priority level (status to disable interrupt of a low priority sequence under the HALT setting).
4. In case a macro service is a high priority level or the status to enable interrupt of a low priority sequence under the HALT setting.

3.4 RESET

When a low level is input to the $\overline{\text{RESET}}$ pin, the internal hardware is initialized (reset state).

When the $\overline{\text{RESET}}$ input becomes from a low level to a high level, the following data is set in the program counter (PC).

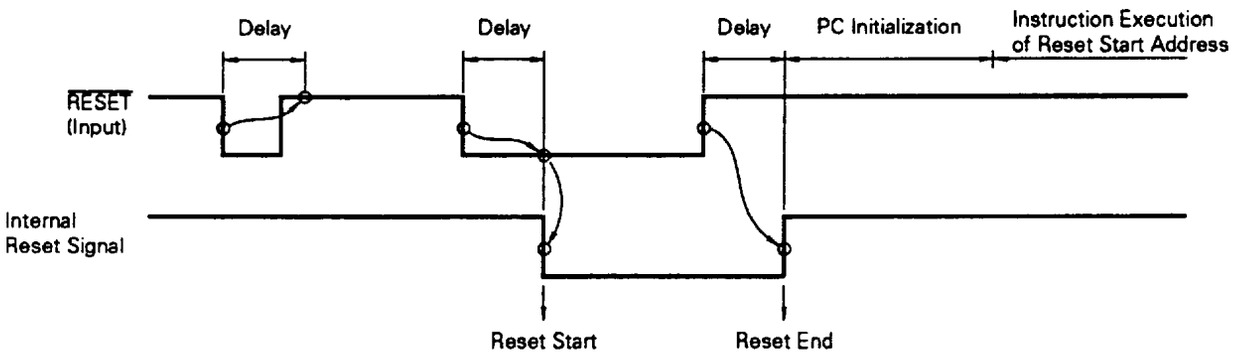
- Lower 8 bits of PC: Contents of 0000H address
- Upper 8 bits of PC: Contents of 0001H address

The contents of the PC set the destination address and the program starts to be executed from the address. Therefore, it can start from any address by reset start.

Please set the program for the contents of each register as required.

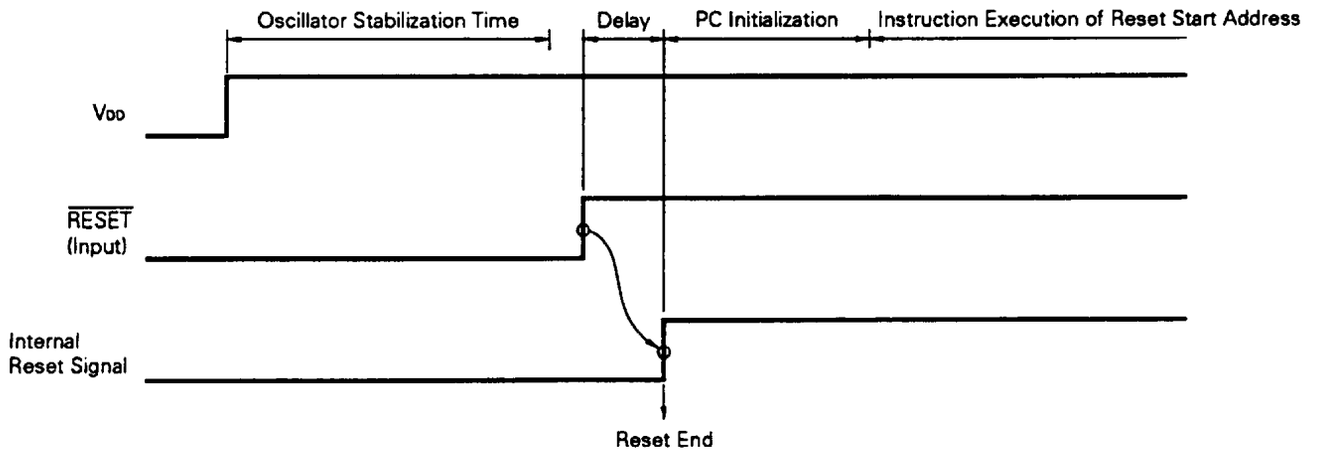
A noise eliminator has been incorporated the $\overline{\text{RESET}}$ input circuit to prevent any error from noise. This noise eliminator circuit is a sampling circuit based on analog delay.

Fig. 3-6 Reset Acknowledge



Set the $\overline{\text{RESET}}$ signal active in the reset operation at power-on until oscillator stabilization time (approx. 40 ms) elapses.

Fig. 3-7 Reset Operation at Power-On



4. INSTRUCTION SET ★

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, SHR, SHL, ROR4, ROL4, DBNZ, PUSH, POP

Table 4-1 8-Bit Instructions Classified by Addressing

1st Operand \ 2nd Operand	#byte	A	r r'	saddr saddr'	sfr	mem	& mem	!addr16	&!addr16	PSW	n	None*2
A	ADD*1		MOV XCH	MOV XCH ADD*1	MOV XCH ADD*1	MOV XCH ADD*1	MOV XCH ADD*1	MOV	MOV	MOV		
r	MOV		MOV XCH ADD*1								ROL ROLC ROR RORC SHR SHL	MULU DIVUW INC DEC
r1												DBNZ
saddr	MOV ADD*1	MOV		MOV XCH ADD*1								INC DBNZ DEC
sfr	MOV ADD*1	MOV										PUSH POP
mem & mem		MOV										
mem1 & mem1												ROR4 ROL4
!addr16		MOV										
&!addr16		MOV										
PSW	MOV	MOV										PUSH POP
STBC	MOV											

* 1. ADDC, SUB, SUBC, AND, OR, XOR and CMP are the same as ADD.
2. There is no 2nd operand or the 2nd operand is not an operand address.

(2) 16-bit instructions

MOVW, ADDW, SUBW, CMPW, INCW, DECW, SHRW, SHLW, PUSH, POP

Table 4-2 16-Bit Instructions Classified by Addressing

1st Operand \ 2nd Operand	#word	AX	rp rp'	saddrp	sfrp	mem1	& mem1	SP	n	None
AX	ADDW SUBW CMPW		ADDW SUBW CMPW	MOVW ADDW SUBW CMPW	MOVW ADDW SUBW CMPW	MOVW	MOVW	MOVW		
rp	MOVW		MOVW						SHLW SHRW	INCW DECW PUSH POP
saddrp	MOVW	MOVW								
sfrp	MOVW	MOVW								
mem1 & mem1		MOVW								
SP	MOVW	MOVW								INCW DECW

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

Table 4-3 Bit Manipulation Instructions Classified by Addressing

1st Operand \ 2nd Operand	CY	A.bit	/A.bit	X.bit	/X.bit	saddr.bit	/saddr. bit	sfr.bit	/sfr.bit	PSW.bit	/PSW bit	None*
CY		MOV1 AND1 OR1 XOR1	AND1 OR1	MOV1 AND1 OR1 XOR1	AND1 OR1	MOV1 AND1 OR1 XOR1	AND1 OR1	MOV1 AND1 OR1 XOR1	AND1 OR1	MOV1 AND1 OR1 XOR1	AND1 OR1	SET1 CLR1 NOT1
A.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR
X.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR
saddr.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR
sfr.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR
PSW.bit	MOV1											SET1 CLR1 NOT1 BT BF BTCLR

* There is no 2nd operand or the 2nd operand is not an operand address.

(4) Call/branch instructions

CALL, CALLF, CALLT, BR, BC, BT, BF, BTCLR, DBNZ, BL, BNC, BNL, BZ, BE, BNZ, BNE

Table 4-4 Call/Branch Instructions Classified by Addressing

Instruction Addressing Operand	$addr16	!addr16	rp	!addr11	[addr5]
Basic instruction	BR BC*	CALL BR	CALL BR	CALLF	CALLT
Compound instruction	BT BF BTCLR DBNZ				

* BL, BNC, BNL, BZ, BE, BNZ and BNE are the same as BC.

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, NOP, EI, DI, SEL

5. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		−0.5 to +7.0	V
	AV_{DD}		AV_{SS} to V_{DD} +0.5	V
	AV_{SS}		−0.5 to +0.5	V
Input voltage	V_I		−0.5 to V_{DD} +0.5	V
Output voltage	V_O		−0.5 to V_{DD} +0.5	V
Output current low	I_{OL}	1 pin	15	mA
		All output pins total	100	mA
Output current high	I_{OH}	1 pin	−10	mA
		All output pins total	−50	mA
A/D converter reference input voltage	AV_{REF1}		−0.5 to V_{DD} +0.3	V
D/A converter reference input voltage	AV_{REF2}		−0.5 to V_{DD} +0.3	V
	AV_{REF3}		−0.5 to V_{DD} +0.3	V
Operating temperature	T_{opt}		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

Note **Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter, or even momentarily. In other words, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute ratings are not exceeded.** ★

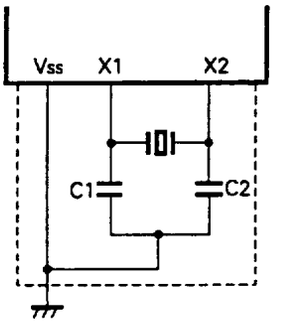
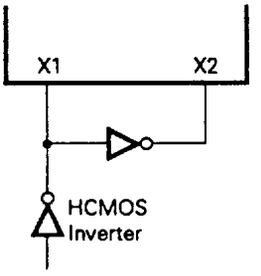
OPERATING CONDITIONS

CLOCK FREQUENCY	OPERATING TEMPERATURE (T_{opt})	SUPPLY VOLTAGE (V_{DD})
4 MHz ≤ fxx ≤ 12 MHz	−40 to +85 °C	+5.0 V ±10 %

CAPACITANCE (Ta = 25 °C, V_{DD} = V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_I	f = 1 MHz unmeasured pins returned to 0 V.			20	pF
Output capacitance	C_O				20	pF
I/O capacitance	C_{IO}				20	pF

OSCILLATOR CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	MIN.	MAX.	UNIT
Ceramic resonator or crystal resonator		Oscillator frequency (fxx)	4	12	MHz
External clock		X1 input frequency (fx)	4	12	MHz
		X1 input rising/falling time (t_{XR}, t_{XF})	0	30	ns
		X1 input high/low level width (t_{WXH}, t_{WXL})	30	130	ns

Note When the clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a dotted line to prevent the influence of wiring capacitance, etc.

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as V_{SS}. Do not connect to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

RECOMMENDED OSCILLATION CIRCUIT CONSTANTS

(1) μPD78233, 78234

CERAMIC RESONATOR

MANUFACTURER	FREQUENCY [MHz]	PRODUCT NAME	RECOMMENDED CONSTANTS	
			C1 [pF]	C2 [pF]
Murata Mfg. Co., Ltd.	12	CSA12.0MT	30	30
		CST12.0MT*	Built-in capacitor type	
Kyocera Corporation	12	KBR12.0M	33	33
Matsushita Electronics Component Co., Ltd.	12	EFOGC1205C4 EFOEC1205C4	Built-in capacitor type	

* Production discontinued.

CRYSTAL RESONATOR

MANUFACTURER	FREQUENCY [MHz]	PRODUCT NAME	RECOMMENDED CONSTANTS	
			C1 [pF]	C2 [pF]
Kinseki, Ltd.	12	HC-49/U	18	18

(2) μPD78238 ★

CERAMIC OSCILLATOR

MANUFACTURER	FREQUENCY [MHz]	PRODUCT NAME	RECOMMENDED CONSTANTS	
			C1 [pF]	C2 [pF]
Murata Mfg. Co., Ltd.	12	CSA12.0MT	30	30
		CST12.0MTW	Built-in capacitor type	
Matsushita Electronics Component Co., Ltd.	12	EFOGC1205C4 EFOEC1205C4	Built-in capacitor type	

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = AV_{DD} = +5 V ±10 %, V_{SS} = AV_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input voltage low	V_{IL}		0		0.8	V
Input voltage high	V_{IH1}	Pins except for *1	2.2		V_{DD}	V
	V_{IH2}	Pin of *1	0.8V_{DD}		V_{DD}	V
Output voltage low	V_{OL1}	I_{OL} = 2.0 mA			0.45	V
	V_{OL2}	I_{OL} = 8.0 mA *2			1.0	V
Output voltage high	V_{OH1}	I_{OH} = –1.0 mA	V_{DD}–1.0			V
	V_{OH2}	I_{OH} = –100 μA	V_{DD}–0.5			V
	V_{OH3}	I_{OH} = –5.0 mA *3	2.0			V
Input leakage current	I_{LI}	0 V ≤ V_I ≤ V_{DD}			±10	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}			±10	μA
X1 input current low	I_{IL}	0 V ≤ V_I ≤ V_{IL}			–100	μA
X1 input current high	I_{IH}	V_{IH2} ≤ V_I ≤ V_{DD}			100	μA
V_{DD} supply current	I_{DD1}	Operating mode f_{XX} = 12 MHz		20	40	mA
	I_{DD2}	HALT mode f_{XX} = 12 MHz		7	20	mA
Data retention voltage	V_{DDDR}	STOP mode	2.5		5.5	V
Data retention current	I_{DDDR}	STOP mode V_{DDDR} = 2.5 V			10	μA
		STOP mode V_{DDDR} = 5 V ±10 %			20	μA
Pull-up resistor	R_L	V_I = 0 V	15	40	80	kΩ

* 1. X1, X2, $\overline{\text{RESET}}$, P20/NMI, P21/INTP0, P22/INTP1, P23/INTP2/CI, P24/INTP3, P25/INTP4/ASCK, P26/INTP5, P27/SI, P32/$\overline{\text{SCK}}$, P33/SO/SB0, MODE pins

2. P10 to P17, P40/AD0 to P47/AD7, P50/A8 to P57/A15 pins

3. P00 to P07 pins

AC CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = +5 V ±10 %, V_{SS} = 0 V)
READ/WRITE OPERATION (1/2)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT	
X1 input clock cycle time	t_{CYX}		82	250	ns	
Address setup time (to ASTB↓)	t_{SAST} •		52		ns	
Address hold time (from ASTB↓)•	t_{HSTA}		25		ns	
Address hold time (from $\overline{RD}$↑)	t_{HRA}		30		ns	
Address hold time (from $\overline{WR}$↑)	t_{HWA}		30		ns	
$\overline{RD}$↓ delay time from address	t_{DAR} •		129		ns	
Address float time (from $\overline{RD}$↓)	t_{FAR} •		11		ns	
Data input time from address	t_{DAID} •	No. of waits = 0		228	ns	
Data input time from ASTB↓	t_{DSTID} •	No. of waits = 0		181	ns	
Data input time from $\overline{RD}$↓	t_{DRID} •	No. of waits = 0		100	ns	
$\overline{RD}$↓ delay time from ASTB↓	t_{DSTR} •		52		ns	
Data hold time (from $\overline{RD}$↑)	t_{HRID}		0		ns	
Address active time from $\overline{RD}$↑	t_{DRA} •		124		ns	
ASTB↑ delay time from $\overline{RD}$↑	t_{DRST} •		124		ns	
$\overline{RD}$ low-level width	t_{WRL} •	No. of waits = 0	124		ns	
ASTB high-level width	t_{WSTH} •		52		ns	
$\overline{WR}$↓ delay time from address	t_{DAW} •		129		ns	
Data output time from ASTB↓	t_{DSTOD} •			142	ns	
Data output time from $\overline{WR}$↓	t_{DWOD}			60	ns	
$\overline{WR}$↓ delay time from ASTB↓	t_{DSTW1} •	Refreshing disabled	52		ns	★
	t_{DSTW2} •	Refreshing enabled	129		ns	
Data setup time (to $\overline{WR}$↑)	t_{SODWR} •	No. of waits = 0	146		ns	
Data setup time (to $\overline{WR}$↓)	t_{SODWF} •	Refreshing enabled	22		ns	
Data hold time (from $\overline{WR}$↑) •	t_{HWOD}		20		ns	
ASTB↑ delay time from $\overline{WR}$↑	t_{DWST} •		42		ns	
$\overline{WR}$ low-level width	t_{WWL1} •	Refreshing disabled No. of waits = 0	196		ns	★
	t_{WWL2} •	Refreshing enabled No. of waits = 0	114		ns	
$\overline{WAIT}$↓ input time from address	t_{DAWT} •			146	ns	
$\overline{WAIT}$↓ input time from ASTB↓	t_{DSTWT} •			84	ns	

* The hold time includes the time to hold the V_{OH} and V_{OL} under the load conditions of C_L = 100 pF and R_L = 2 kΩ.

Remarks 1. The values in the above table are based on "f_{XX} = 12 MHz and C_L = 100 pF".
2. For a parameter with a dot (•) in the SYMBOL column, refer to **DEFINITION OF t_{CYX} DEPENDENT BUS TIMINGS** as well.

READ/WRITE OPERATION (2/2)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
$\overline{WAIT}$ hold time from ASTB↓		t_{HSTWT} •	No. of external waits = 1	174		ns
$\overline{WAIT}$↑ delay time from ASTB↓		t_{DSTWTH} •	No. of external waits = 1		273	ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓		t_{DRWTL} •			22	ns
$\overline{WAIT}$ hold time from $\overline{RD}$↓		t_{HRWT} •	No. of external waits = 1	87		ns
$\overline{WAIT}$↑ delay time from $\overline{RD}$↓		t_{DRWTH} •	No. of external waits = 1		186	ns
Data input time from $\overline{WAIT}$↑		t_{DWTID} •			62	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑		t_{DWTW} •		154		ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑		t_{DWTR} •		72		ns
$\overline{WAIT}$ input time from $\overline{WR}$↓ (Refreshing disabled)		t_{DWWTL} •			22	ns
$\overline{WAIT}$ hold time from $\overline{WR}$↓	Refreshing disabled	t_{HWWT1} •	No. of external waits = 1	87		ns
	Refreshing enabled	t_{HWWT2} •	No. of external waits = 1	5		ns
$\overline{WAIT}$↑ delay time from $\overline{WR}$↓	Refreshing disabled	t_{DWWTH1} •	No. of external waits = 1		186	ns
	Refreshing enabled	t_{DWWTH2} •	No. of external waits = 1		104	ns
$\overline{REFRQ}$↓ delay time from $\overline{RD}$↑		t_{DRRFQ} •		154		ns
$\overline{REFRQ}$↓ delay time from $\overline{WR}$↑		t_{DWRFQ} •		72		ns
$\overline{REFRQ}$ low-level width		t_{WRFQL} •		120		ns
ASTB↑ delay time from $\overline{REFRQ}$↑		t_{DRFQST} •		280		ns

Remarks 1. The values in the above table are based on "f_{XX} = 12 MHz and C_L = 100 pF".

2. For a parameter with a dot (•) in the SYMBOL column, refer to **DEFINITION OF t_{CYX} DEPENDENT BUS TIMINGS** as well.

SERIAL OPERATION

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	MAX.	UNIT
Serial clock cycle time	t_{CYSK}	Input	External clock	1.0		μs
		Output	Internally divided by 16	1.3		μs
			Internally divided by 64	5.3		μs
Serial clock low-level width	t_{WSKL}	Input	External clock	420		ns
		Output	Internally divided by 16	556		ns
			Internally divided by 64	2.5		μs
Serial clock high-level width	t_{WSKH}	Input	External clock	420		ns
		Output	Internally divided by 16	556		ns
			Internally divided by 64	2.5		μs
SI, SB0 setup time (to $\overline{SCK}\uparrow$)	t_{SSSK}			150		ns
SI, SB0 hold time (from $\overline{SCK}\uparrow$)	t_{HSSK}			400		ns
SO/SB0 output delay time (from $\overline{SCK}\downarrow$)	t_{DSSSK1}	CMOS push-pull output (3-wire serial I/O mode)		0	300	ns
	t_{DSSSK2}	Open-drain output (SBI mode), R_L = 1 kΩ		0	800	ns
SB0 high hold time (from $\overline{SCK}\uparrow$)	t_{HSSSK}	SBI mode		4		t_{CYX}
SB0 low setup time (to $\overline{SCK}\downarrow$)	t_{SSSSK}			4		t_{CYX}
SB0 low-level width	t_{WSSL}			4		t_{CYX}
SB0 high-level width	t_{WSSH}			4		t_{CYX}

Remarks The values in the above table are based on "f_{XX} = 12 MHz and C_L = 100 pF".

OTHER OPERATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
NMI low-level width	t_{WNIL}		10		μs
NMI high-level width	t_{WNIH}		10		μs
INTP0 to INTP5 low-level width	t_{WITL}		24		t_{CYX}
INTP0 to INTP5 high-level width	t_{WITH}		24		t_{CYX}
$\overline{RESET}$ low-level width	t_{WRSL}		10		μs
$\overline{RESET}$ high-level width	t_{WRSH}		10		μs

EXTERNAL CLOCK TIMING

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
X1 input low-level width	t_{WXL}		30	130	ns
X1 input high-level width	t_{WXH}		30	130	ns
X1 input rise time	t_{XR}		0	30	ns
X1 input fall time	t_{XF}		0	30	ns
X1 input clock cycle time	t_{CYX}		82	250	ns

A/D CONVERTER CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = AV_{DD} = +5 V ±10 %, V_{SS} = AV_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Resolution			8			bit
Overall error *1		4.0 V ≤ AV_{REF1} ≤ AV_{DD} T_a = −10 to +70°C			0.4	%
		3.4 V ≤ AV_{REF1} ≤ AV_{DD}			0.8	%
		4.0 V ≤ AV_{REF1} ≤ AV_{DD}			0.6	%
Quantization error					±1/2	LSB
Conversion time	t_{CONV}	The FR bit of ADM is to be "0"	360			t_{CYX}
		The FR bit of ADM is to be "1"	240			t_{CYX}
Sampling time	t_{SAMP}	The FR bit of ADM is to be "0"	72			t_{CYX}
		The FR bit of ADM is to be "1"	48			t_{CYX}
Analog input voltage	V_{IAN}		−0.3		AV_{REF1} +0.3	V
Analog input impedance	R_{AN}			1000		MΩ
Reference voltage	AV_{REF1}		3.4		AV_{DD}	V
AV_{REF} current	AI_{REF1}	f_{XX} = 12 MHz		1.5	3.0	mA
		*2		0.7	1.5	mA
AV_{DD} power current	AI_{DD1}	f_{XX} = 12 MHz		1.4	3.0	mA
	AI_{DD2}	*3		10	20	μA

* 1. Quantization error is not included. Represented by the ratio to full-scale value.
2. When ADM register CS bit is 0
3. When ADM register CS bit is 0 and STOP mode is set