PRELIMINARY DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD780993(A)

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD780993(A) is a μPD780993 Subseries product of the 78K/0 Series.

This microcontroller incorporates an automotive multiplex communication interface, 8-bit resolution A/D converter, timer, serial interface, interrupt function, and various other peripheral hardware.

The μPD78F0994, a product with on-chip flash memory that can operate in the same power supply voltage range as the mask ROM version, and various development tools are also available.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD780993 Subseries User's Manual: U13316E
78K/0 Series User's Manual Instruction: U12326E

FEATURES

- On-chip automotive multiplex communication interface: 1 channel
- Direct battery voltage input (P50 to P57, P60 to P67) is possible by means of input current limitation
- Internal ROM and RAM
  - Internal ROM: 24 KB
  - Internal high-speed RAM: 768 bytes
- Minimum instruction execution time can be selected from high-speed (0.24 μs) to low-speed (3.81 μs)
- I/O ports: 49 (including 16 ports that can be connected directly from the car battery by means of input current limitation)
- 8-bit resolution A/D converter: 8 channels
- Serial interface: 3 channels (including the automotive multiplex communication interface)
- Timer: 5 channels
- Supply voltage: V_{DD} = 4.0 to 5.5 V

APPLICATIONS

Automotive multiplex communication control for body electrical systems

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Printed in Japan

The mark ★ shows major revised points.

★ **ORDERING INFORMATION**

Part Number	Package	Quality Grade
μPD780993GK(A)-×××-8A8	64-pin plastic LQFP (12 × 12 mm)	Special
μPD780993GK(A)-×××-9ET[Note]	64-pin plastic TQFP (12 × 12 mm)	Special

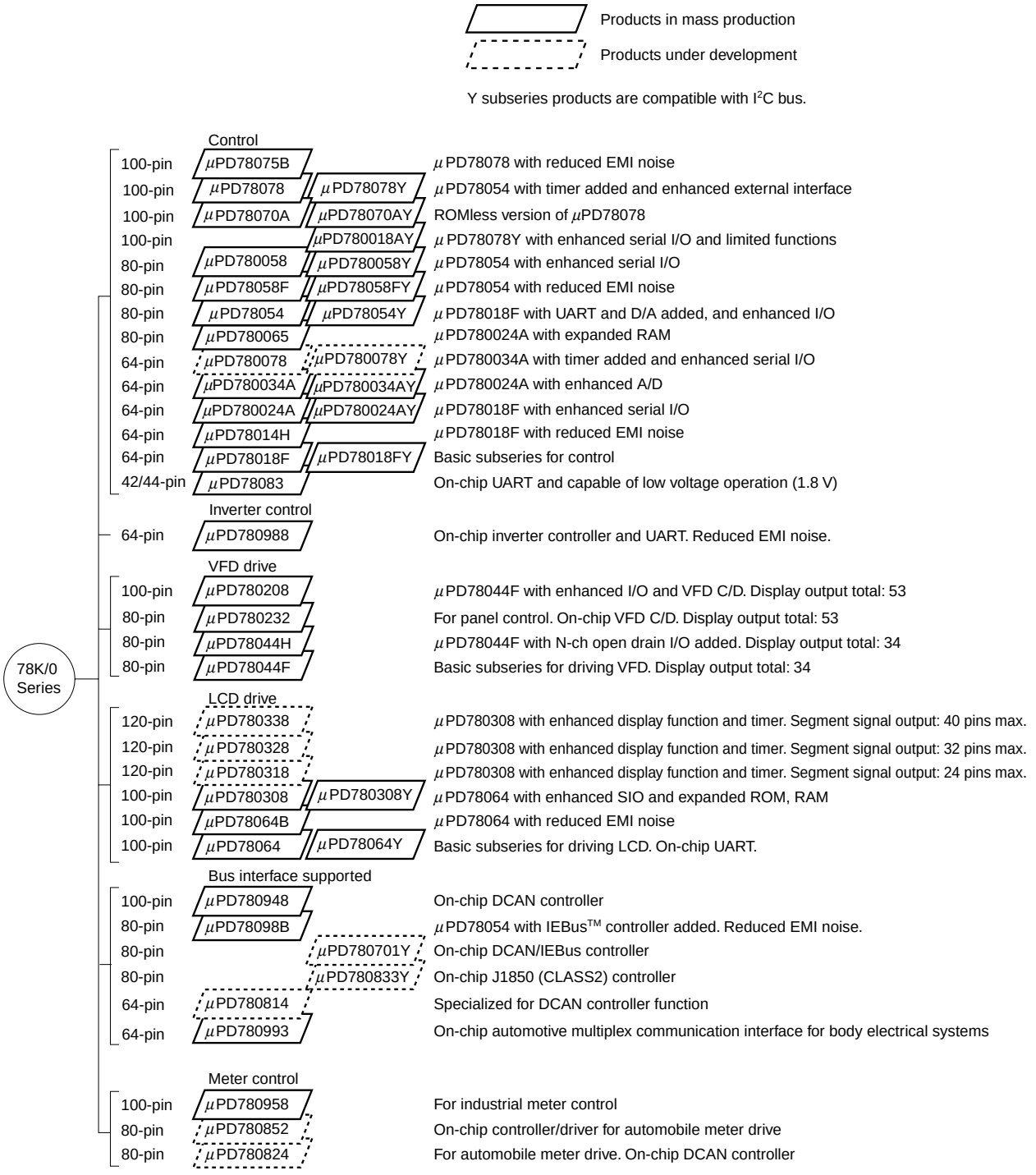
Note Under development

Remark ××× indicates ROM code suffix.

Please refer to the **Quality Grades on NEC Semiconductor Devices (C11531E)** published by NEC Corporation to know the specification of quality grade on the device and its recommended applications.

★ **78K/0 SERIES LINEUP**

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.



Remark VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major functional differences among the subseries are listed below.

Subseries Name \ Function		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-bit	16-bit	Watch	WDT							
Control	μPD78075B	32 K to 40 K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	88	1.8 V	Yes
	μPD78078	48 K to 60 K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24 K to 60 K	2 ch							3 ch (time division UART: 1 ch)	68	1.8 V	
	μPD78058F	48 K to 60 K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16 K to 60 K										2.0 V	
	μPD780065	40 K to 48 K							–	4 ch (UART: 1 ch)	60	2.7 V	
	μPD780078	48 K to 60 K		2 ch			–	8 ch		3 ch (UART: 2 ch)	52	1.8 V	
	μPD780034A	8 K to 32 K		1 ch						3 ch (UART: 1 ch)	51		
	μPD780024A						8ch	–					
	μPD78014H									2 ch	53		
	μPD78018F	8 K to 60 K											
	μPD78083	8 K to 16 K		–	–					1 ch (UART: 1 ch)	33		–
Inverter control	μPD780988	32 K to 60 K	3 ch	**Note**	–	1 ch	–	8 ch	–	3 ch (UART: 2 ch)	47	4.0 V	Yes
VFD drive	μPD780208	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	2 ch	74	2.7 V	–
	μPD780232	16 K to 24 K	3 ch	–	–		4 ch			2 ch	40	4.5 V	
	μPD78044H	32 K to 48 K	2 ch	1 ch	1 ch		8 ch			1 ch	68	2.7 V	
	μPD78044F	16 K to 40 K								2 ch			
LCD drive	μPD780338	48 K to 60 K	3 ch	2 ch	1 ch	1 ch	–	10 ch	1 ch	2 ch (UART: 1 ch)	54	1.8 V	–
	μPD780328	48 K to 60 K									62		
	μPD780318	48 K to 60 K									70		
	μPD780308	48 K to 60 K	2 ch	1 ch			8 ch	–	–	3 ch (time division UART: 1 ch)	57	2.0 V	
	μPD78064B	32 K								2 ch (UART: 1 ch)			
	μPD78064	16 K to 32 K											
Bus interface supported	μPD780948	60 K	2 ch	2 ch	1 ch	1 ch	8 ch	–	–	3 ch (UART: 1 ch)	79	4.0 V	Yes
	μPD78098B	40 K to 60 K		1 ch					2 ch		69	2.7 V	–
	μPD780814	32 K to 60 K		2 ch			12 ch		–	2 ch (UART: 1 ch)	46	4.0 V	
	μPD780993	24 K	3 ch	1 ch	–		8 ch			3 ch (UART: 1 ch)	49		
Meter control	μPD780958	48 K to 60 K	4 ch	2 ch	–	1 ch	–	–	–	2 ch (UART: 1 ch)	69	2.2 V	–
Dashboard control	μPD780852	32 K to 40 K	3 ch	1 ch	1 ch	1 ch	5 ch	–	–	3 ch (UART: 1 ch)	56	4.0 V	–
	μPD780824	32 K to 60 K								2 ch (UART: 1 ch)	59		

Note 16-bit timer: 2 channels

10-bit timer: 1 channel

OVERVIEW OF FUNCTIONS

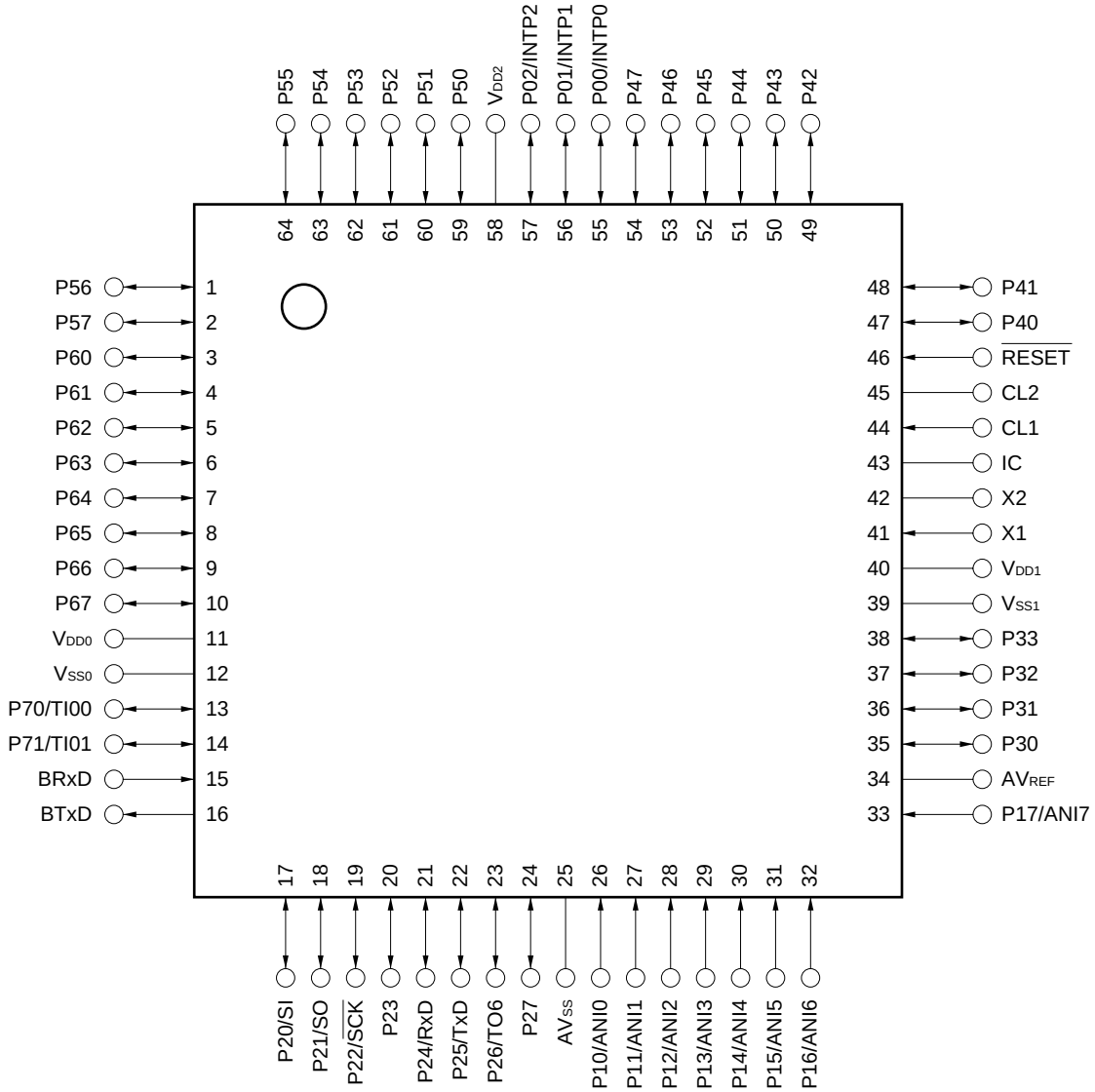
Item		Function
Internal memory	ROM	24 KB
	High-speed RAM	768 bytes
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Minimum instruction execution time		On-chip minimum instruction execution time variable function
	When main system clock is selected	0.24 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (@ 8.38 MHz operation)
	When subsystem clock is selected	100 μs (@ 40 kHz operation)
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjust, etc.
I/O ports (including 16 ports that can be connected directly from the car battery by means of input current limitation)		Total: 49 • CMOS input: 8 • CMOS I/O: 41
A/D converter		• 8-bit resolution × 8 channels
Serial interface		• Automotive multiplex communication: 1 channel • 3-wire serial I/O mode: 1 channel • UART mode: 1 channel
Timer		• 16-bit timer/event counter: 1 channel • 8-bit timer: 3 channels • Watchdog timer: 1 channel
Timer outputs		1 (8-bit PWM output capable: 1)
Vectored interrupt sources	Maskable	Internal: 12, external: 4
	Non-maskable	Internal: 1
	Software	1
Supply voltage		V_{DD} = 4.0 to 5.5 V
Operating ambient temperature		T_A = –40 to +85°C
★ Package		• 64-pin plastic LQFP (12 × 12 mm) • 64-pin plastic TQFP (12 × 12 mm)

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

64-pin plastic LQFP (12 × 12 mm)
μPD780993GK(A)-×××-8A8

★ **64-pin plastic TQFP (12 × 12 mm)**
μPD780993GK(A)-×××-9ET (under development)



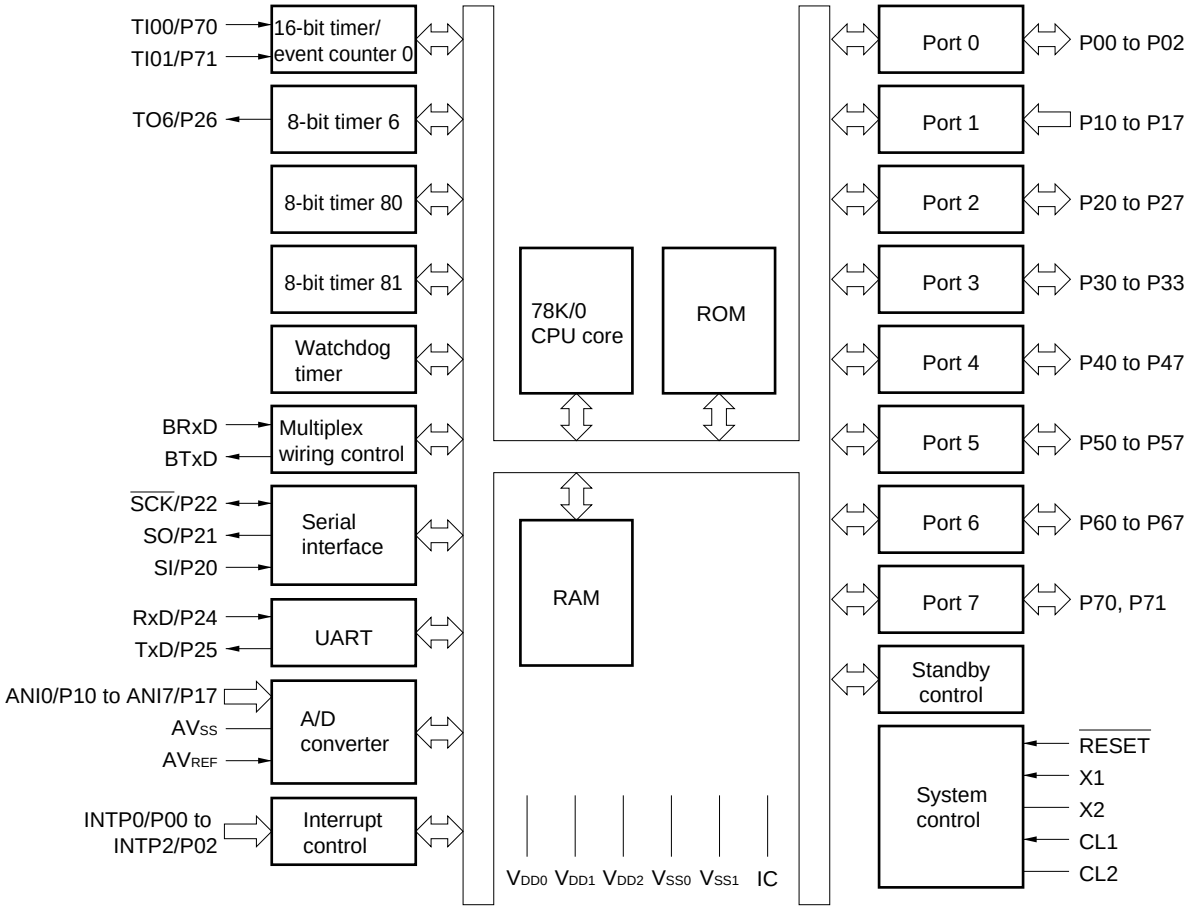
Cautions 1. Connect the IC (Internally Connected) pin directly to V_{SS0} or V_{SS1}.

2. Connect the AV_{SS} pin to V_{SS0}.

Remark When the μPD780993(A) is used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V_{DD0}, V_{DD1} and V_{DD2} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

ANI0 to ANI7:	Analog input
AV_{REF}:	Analog reference voltage
AV_{SS}:	Analog ground
BRxD:	Body control receive data
BTxD:	Body control transmit data
CL1, CL2:	RC (subsystem clock)
IC:	Internally connected
INTP0 to INTP2:	Interrupt from peripherals
P00 to P02:	Port 0
P10 to P17:	Port 1
P20 to P27:	Port 2
P30 to P33:	Port 3
P40 to P47:	Port 4
P50 to P57:	Port 5
P60 to P67:	Port 6
P70, P71:	Port 7
$\overline{\text{RESET}}$:	Reset
RxD:	Receive data
$\overline{\text{SCK}}$:	Serial clock
SI:	Serial input
SO:	Serial output
TI00, TI01:	Timer input
TO6:	Timer output
TxD:	Transmit data
V_{DD0} to V_{DD2}:	Power supply
V_{SS0}, V_{SS1}:	Ground
X1, X2:	Crystal (main system clock)

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P02	I/O	Port 0. 3-bit I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.	Input	INTP0 to INTP2
P10 to P17	Input	Port 1 8-bit input-only port	Input	ANI0 to ANI7
P20	I/O	Port 2 8-bit I/O port. Input/output can be specified in 1-bit units.	Input	SI
P21				SO
P22				$\overline{SCK}$
P23				–
P24				RxD
P25				TxD
P26				TO6
P27				–
P30 to P33	I/O	Port 3 4-bit I/O port. Input/output can be specified in 1-bit units.	Input	–
P40 to P47	I/O	Port 4 8-bit I/O port. Input/output can be specified in 1-bit units.	Input	–
P50 to P57	I/O	Port 5 8-bit I/O port. Capable of direct battery voltage input by means of input current limitation. Input/output can be specified in 1-bit units.	Input	–
P60 to P67	I/O	Port 6 8-bit I/O port. Capable of direct battery voltage input by means of input current limitation. Input/output can be specified in 1-bit units.	Input	–
P70, P71	I/O	Port 7 2-bit I/O port. Input/output can be specified in 1-bit units.	Input	TI00, TI01

3.2 Non-Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0 to INTP2	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P00 to P02
SI	Input	Serial interface serial data input	Input	P20
SO	Output	Serial interface serial data output	Input	P21
$\overline{SCK}$	I/O	Serial interface serial clock input/output	Input	P22
RxD	Input	Serial data input for asynchronous serial interface	Input	P24
TxD	Output	Serial data output for asynchronous serial interface	Input	P25
BRxD	Input	Automotive multiplex communication serial data input. When reception is performed in the standby state, it also functions as a wake-up interrupt request input (INTWAKE).	Input	–
BTxD	Output	Automotive multiplex communication serial data output	Output	–
TI00	Input	Capture trigger signal input to 16-bit timer (TM0)	Input	P70
TI01				P71
TO6	Output	8-bit timer (TM6) output (also used for 8-bit PWM output)	Input	P26
ANI0 to ANI7	Input	A/D converter analog input	Input	P10 to P17
AV_{REF}	Input	A/D converter reference voltage input (also used for analog power supply)	–	–
AV_{SS}	–	A/D converter ground potential. Connect to V_{SS0}.	–	–
$\overline{RESET}$	Input	System reset input	–	–
X1	Input	Connecting crystal resonator for main system clock oscillation	–	–
X2	–		–	–
CL1	Input	Connecting RC for subsystem clock oscillation	–	–
CL2	–		–	–
V_{DD0}	–	Positive power supply of ports	–	–
V_{SS0}	–	Ground potential of ports	–	–
V_{DD1}	–	Positive power supply (except port and analog sections)	–	–
V_{SS1}	–	Ground potential (except port and analog sections)	–	–
V_{DD2}	–	Positive power supply of ports capable of supporting connection directly to the battery (P50 to P57, P60 to P67).	–	–
IC	–	Internally connected. Connect directly to V_{SS0} or V_{SS1}.	–	–

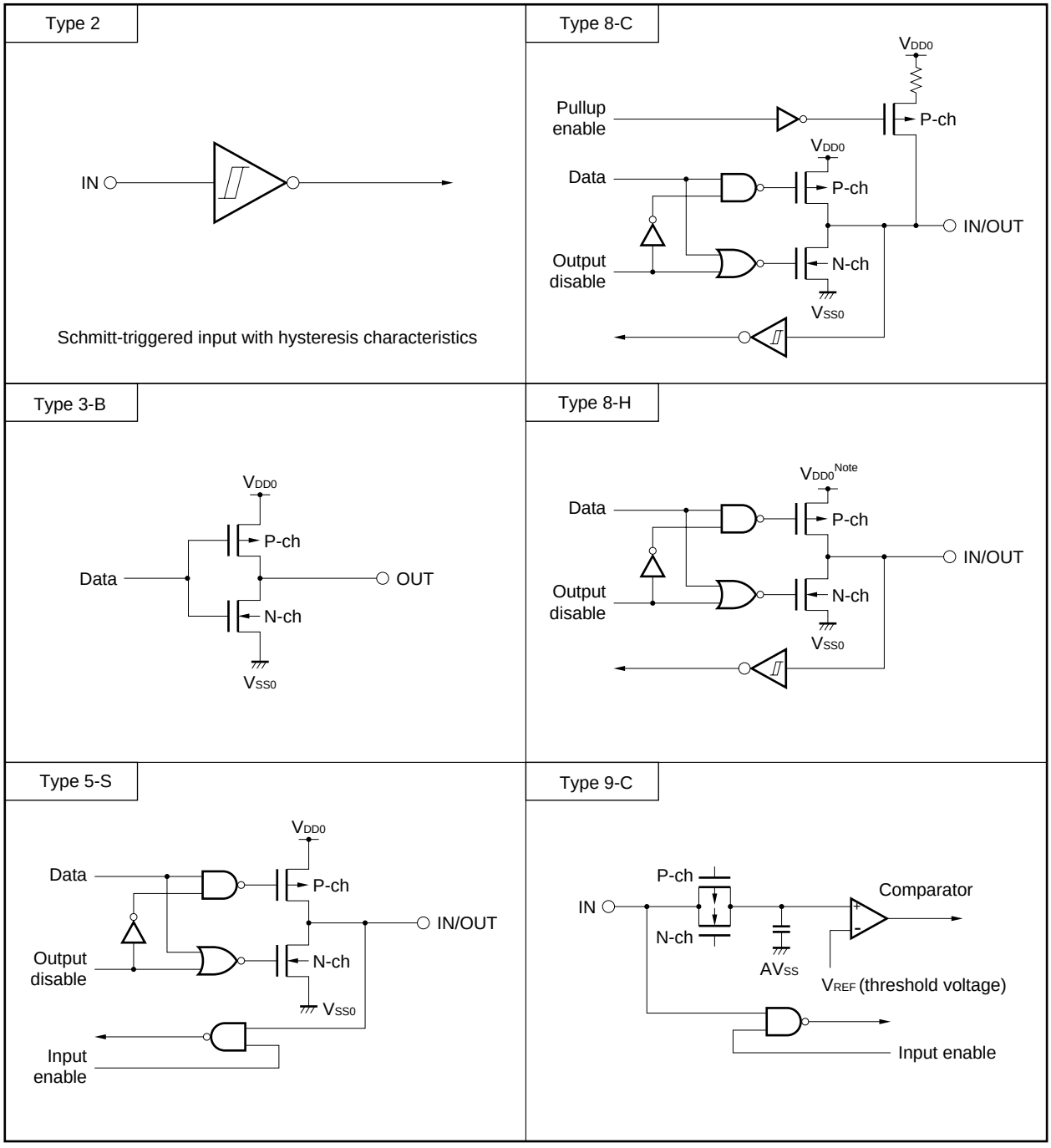
3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, refer to **Figure 3-1**.

Table 3-1. Types of Pin Input/Output Circuits

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0 to P02/INTP2	8-C	I/O	Independently connect to V_{SS0} via a resistor.
P10/ANI0 to P17/ANI7	9-C	Input	Independently connect to V_{DD0} or V_{SS0} via a resistor.
P20/SI	8-H	I/O	
P21/SO	5-S		
P22/$\overline{SCK}$	8-H		
P23	5-S		
P24/RxD	8-H		
P25/TxD	5-S		
P26/TO6			
P27			
P30 to P33			
P40 to P47			
P50 to P57	8-H		
P60 to P67			
P70/TI00, P71/TI01			
BRxD	2	Input	
BTxD	3-B	Output	Leave open.
CL1	–	Input	Independently connect to V_{DD0} or V_{SS0} via a resistor.
CL2	–	–	Leave open.
$\overline{RESET}$	2	Input	–
AV_{REF}	–	–	Connect to V_{SS0}.
AV_{SS}			
IC			Connect directly to V_{SS0} or V_{SS1}.

Figure 3-1. Pin Input/Output Circuits

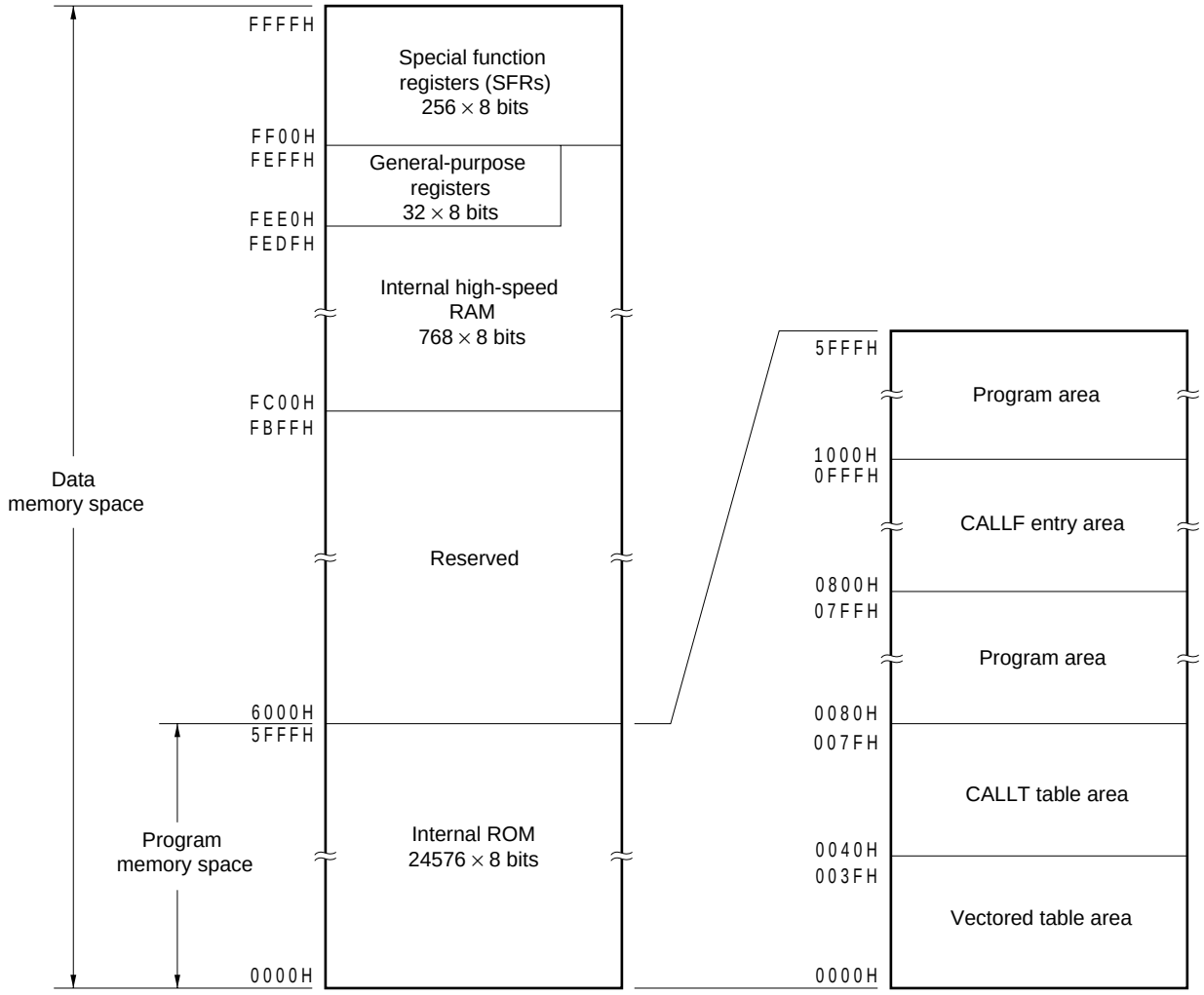


Note Ports 5 and 6 (P50 to P57 and P60 to P67 respectively) become V_{DD2}.

4. MEMORY SPACE

Figure 4-1 shows the memory map of the μPD780993(A).

Figure 4-1. Memory Map



5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

The following two types of I/O ports are available.

- CMOS input (port 1): 8
- CMOS I/O (port 0, ports 2 to 7): 41

Total : 49

Table 5-1. Port Functions

Port Name	Pin Name	Function
Port 0	P00 to P02	I/O port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.
Port 1	P10 to P17	Input-only port.
Port 2	P20 to P27	I/O port. Input/output can be specified in 1-bit units.
Port 3	P30 to P33	I/O port. Input/output can be specified in 1-bit units.
Port 4	P40 to P47	I/O port. Input/output can be specified in 1-bit units.
Port 5	P50 to P57	I/O port. Input/output can be specified in 1-bit units. Can be connected directly from the car battery by means of input current limitation.
Port 6	P60 to P67	I/O port. Input/output can be specified in 1-bit units. Can be connected directly from the car battery by means of input current limitation.
Port 7	P70, P71	I/O port. Input/output can be specified in 1-bit units.

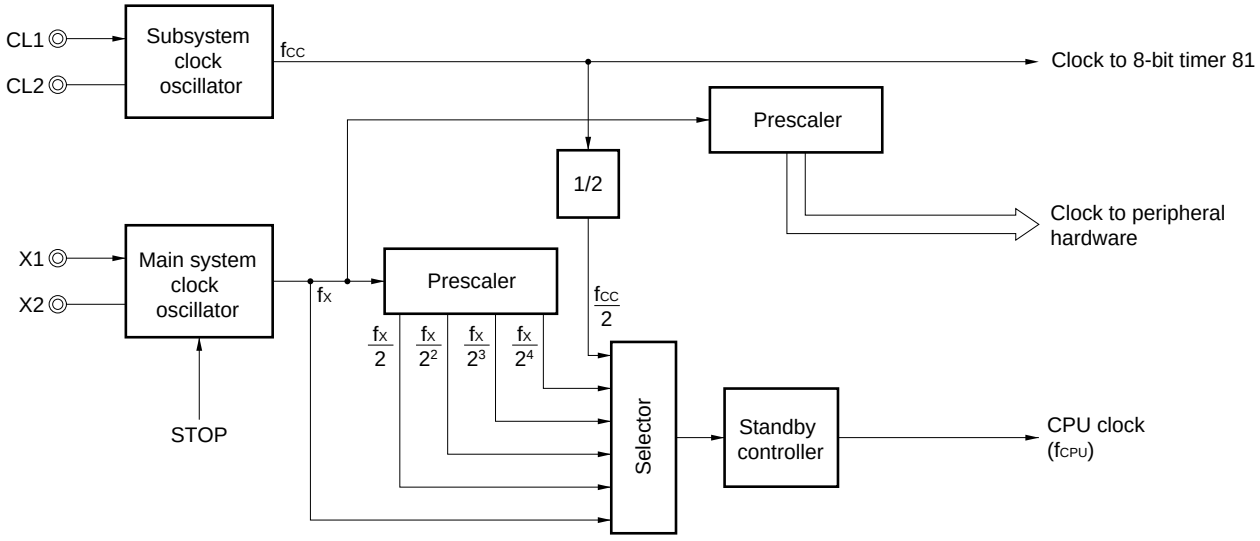
5.2 Clock Generator

A system clock generator is incorporated.

The minimum instruction execution time can be changed.

- 0.24 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (@ 8.38 MHz operation with main system clock)
- 100 μs (@ 40 kHz operation with subsystem clock)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer/Event Counters

Five timer/event counter channels are incorporated.

- 16-bit timer/event counter: 1 channel
- 8-bit timer: 3 channels
- Watchdog timer: 1 channel

Table 5-2. Operation of Timer/Event Counter

		16-Bit Timer/Event Counter	8-Bit Timer 6	8-Bit Timer 80, 81	Watchdog Timer
Operation Mode	Interval timer	2 channels[Note 1]	1 channel	2 channels	1 channel[Note 2]
	External event counter	1 channel	–	–	–
Function	Timer output	–	1 output	–	–
	PWM output	–	1 output	–	–
	Pulse width measurement	2 inputs	–	–	–
	Square wave output	–	1 output	–	–
	Interrupt request	2	1	2	1

Notes 1. When capture/compare registers 00 and 01 (CR00, CR01) are both specified as compare registers.

2. Although the watchdog timer can function as both a watchdog timer and an interval timer, be sure to use it after selecting one of these functions.

Figure 5-2. Block Diagram of 16-Bit Timer/Event Counter 0 (TM0)

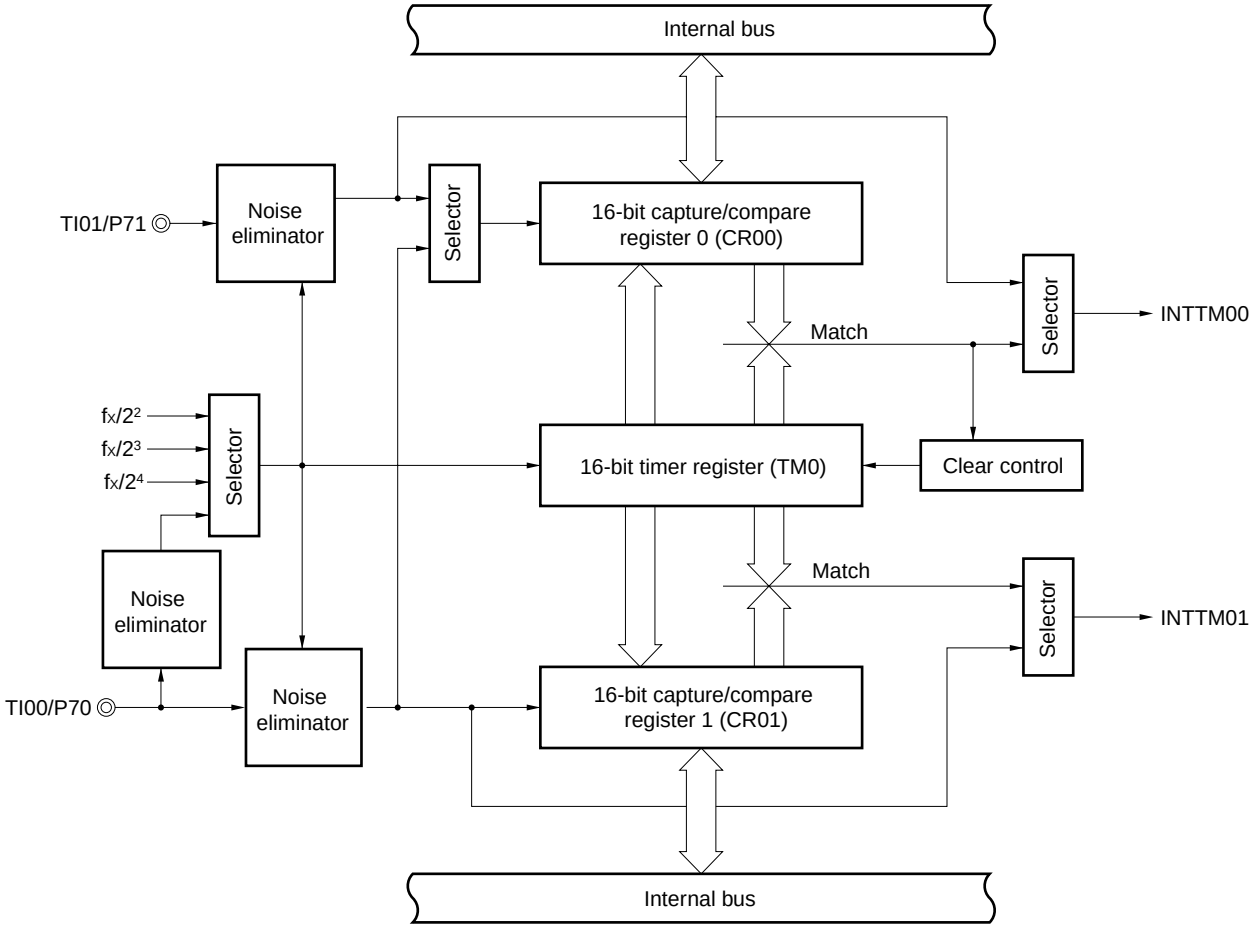


Figure 5-3. Block Diagram of 8-Bit Timer 6 (TM6)

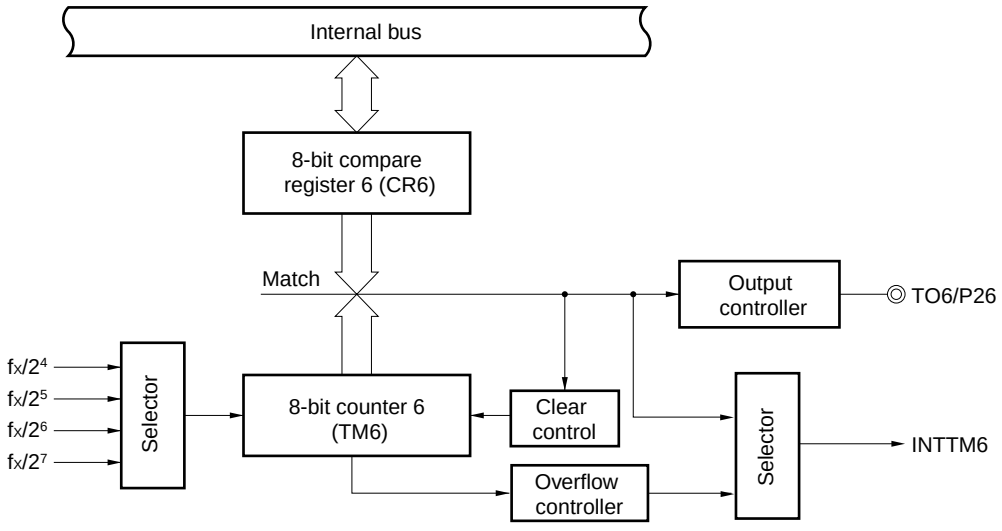


Figure 5-4. Block Diagram of 8-Bit Timer 80 (TM80)

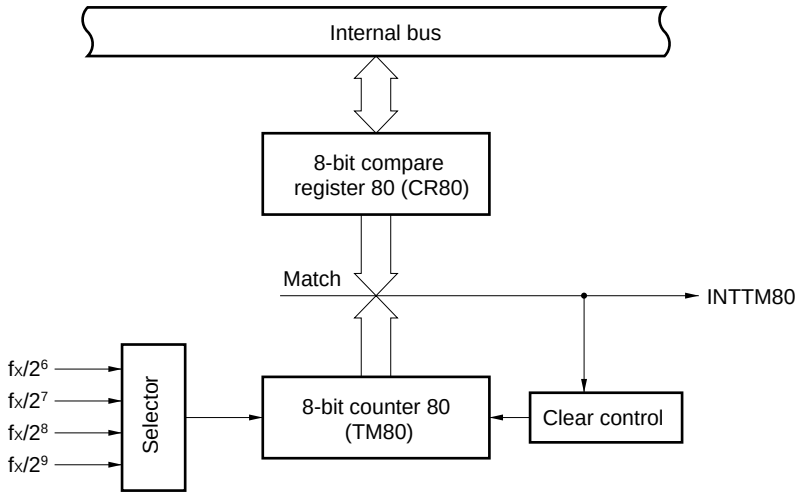


Figure 5-5. Block Diagram of 8-Bit Timer 81 (TM81)

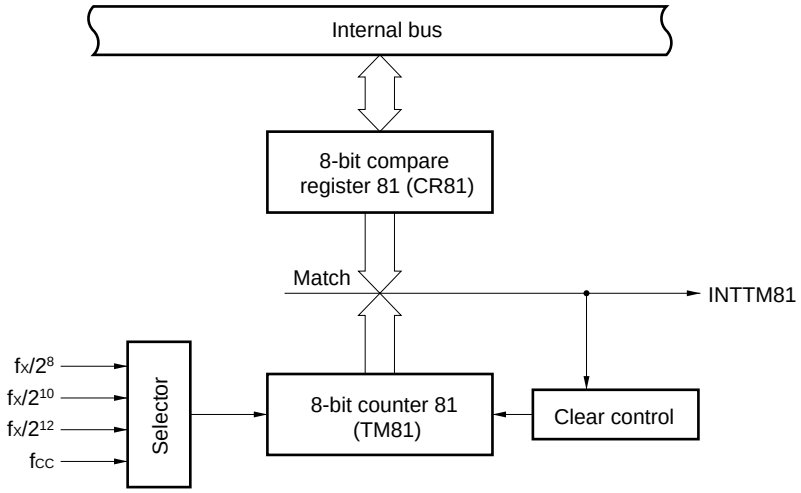
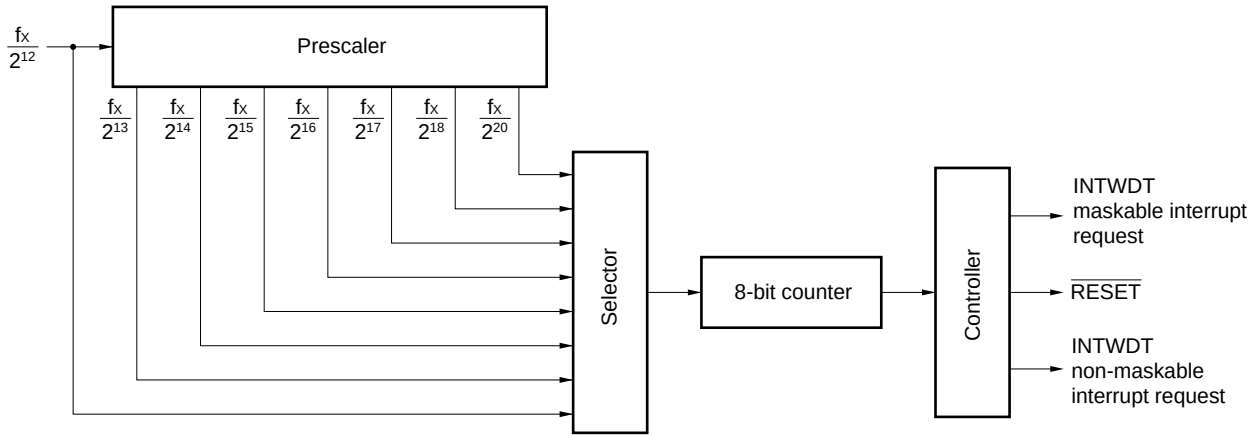


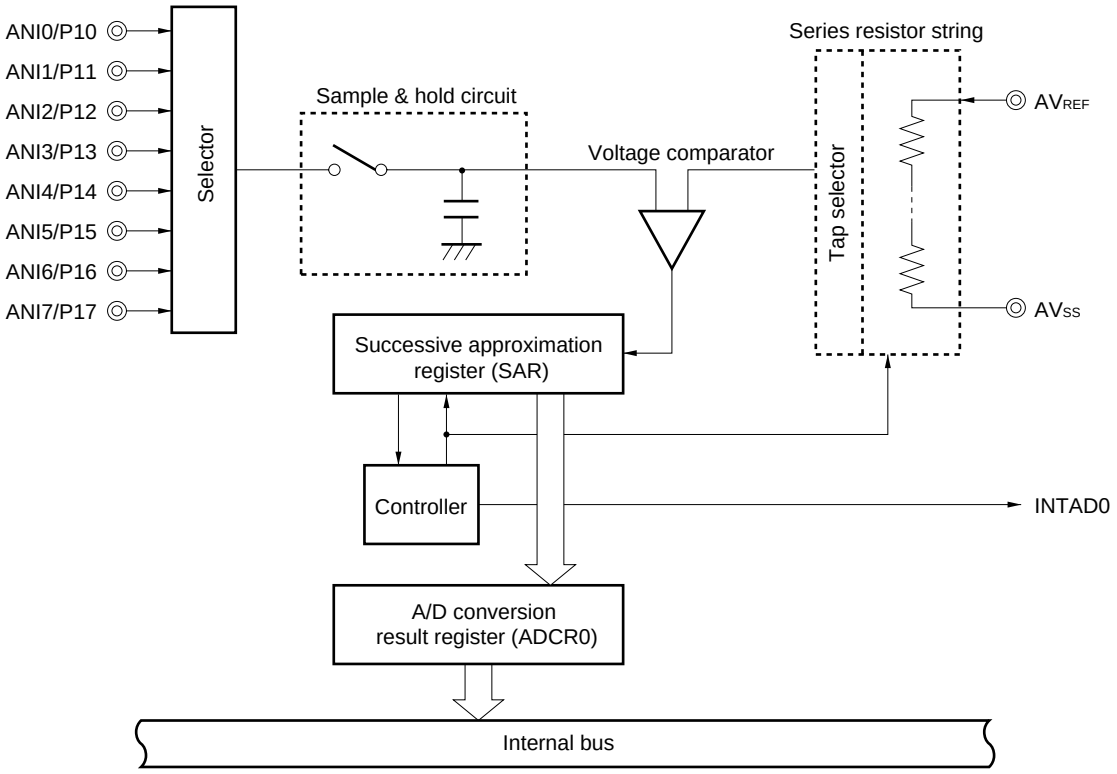
Figure 5-6. Block Diagram of Watchdog Timer



5.4 A/D Converter

An A/D converter consisting of eight 8-bit resolution channels is incorporated.

Figure 5-7. Block Diagram of A/D Converter



5.5 Serial Interface

Three serial interface channels are incorporated.

- Automotive multiplex communication
- Serial interface UART
- Serial interface SIO3

Figure 5-8. Block Diagram of Automotive Multiplex Communication

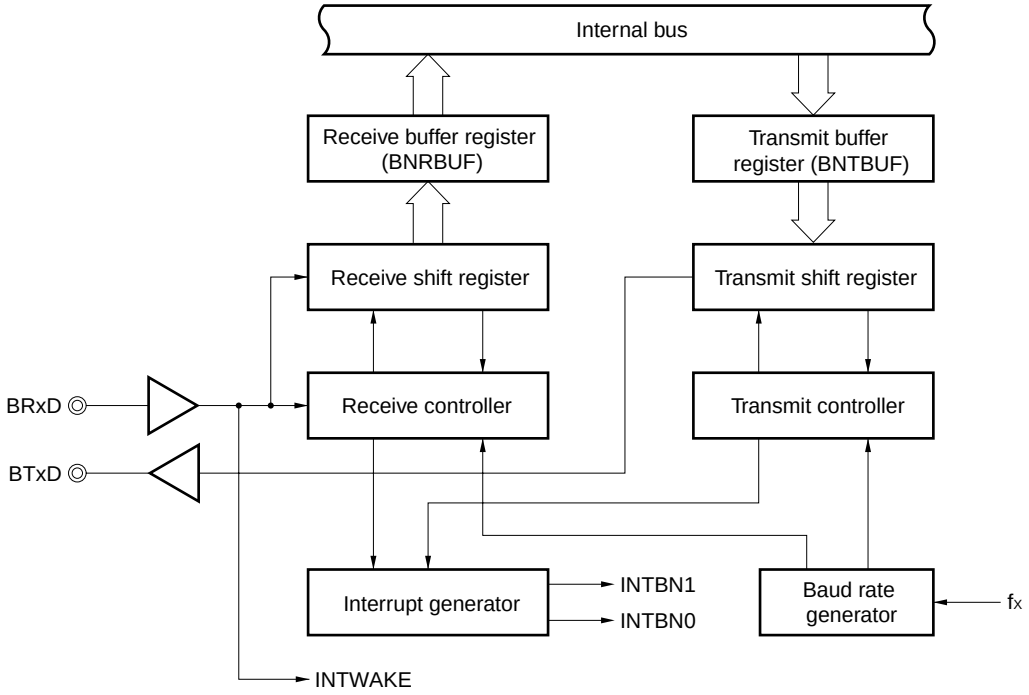


Figure 5-9. Block Diagram of Serial Interface UART

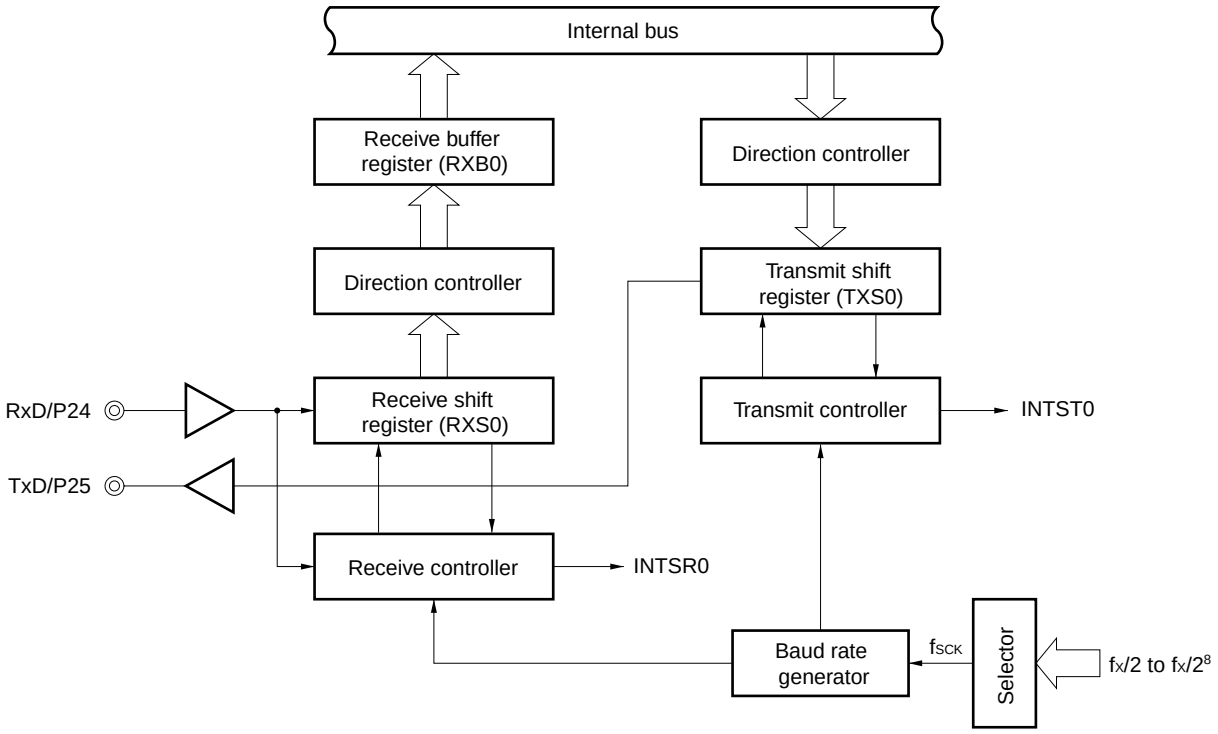
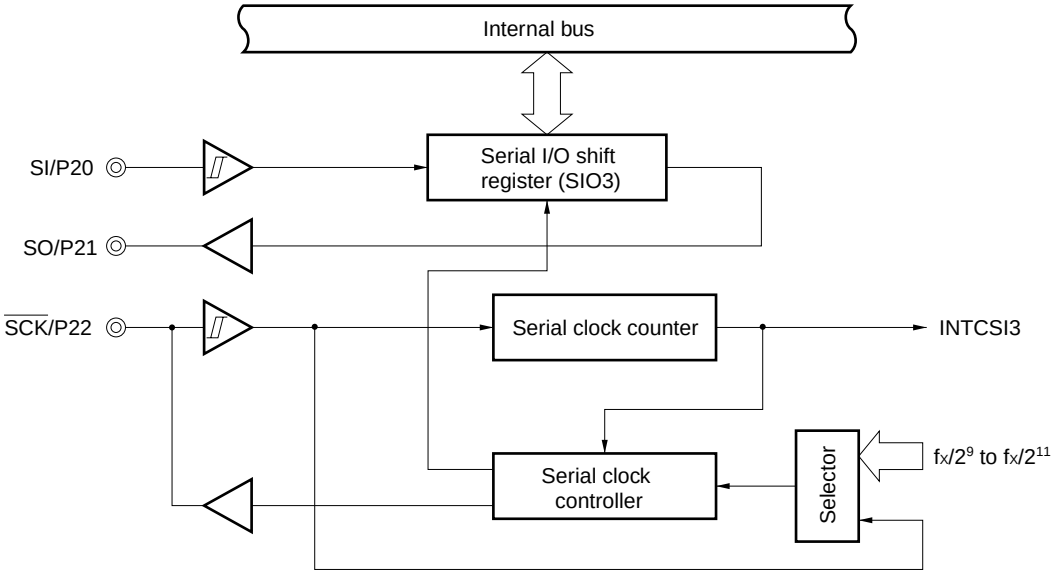


Figure 5-10. Block Diagram of Serial Interface SIO3



6. INTERRUPT FUNCTIONS

Eighteen interrupt sources divided into the following 3 types are provided.

- Non-maskable interrupts: 1
- Maskable interrupts: 16
- Software interrupts: 1

Table 6-1. Interrupt Sources (1/2)

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	–	INTWDT	Watchdog timer overflow (when non-maskable interrupt is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (when interval timer is selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTWAKE	Input edge detection for serial interface automotive multiplex communication wake-up.		000CH	
	5	INTTM00	• When CR00 is specified to the compare register: generates the match signal of the 16-bit timer register (TM0) and capture compare register 0 (CR00) • When CR00 is specified to the capture register: detects the valid edge of TI01	Internal	000EH	(B)
	6	INTTM01	• When CR01 is specified to the compare register: generates the match signal of the 16-bit timer register (TM0) and capture compare register 1 (CR01) • When CR01 is specified to the capture register: detects the valid edge of TI00		0010H	
	7	INTTM6	Generates the match signal of 8-bit counter 6 (TM6) and compare register 6 (CR6)		0012H	
	8	INTTM80	Generates the match signal of 8-bit counter 80 (TM80) and compare register 80 (CR80)		0014H	
	9	INTTM81	Generates the match signal of 8-bit counter 81 (TM81) and compare register 81 (CR81)		0016H	

Notes 1. Default Priority is the priority order when several maskable interrupts are generated at the same time. 0 is the highest priority and 15 is the lowest.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 6-1, respectively.

Table 6-1. Interrupt Sources (2/2)

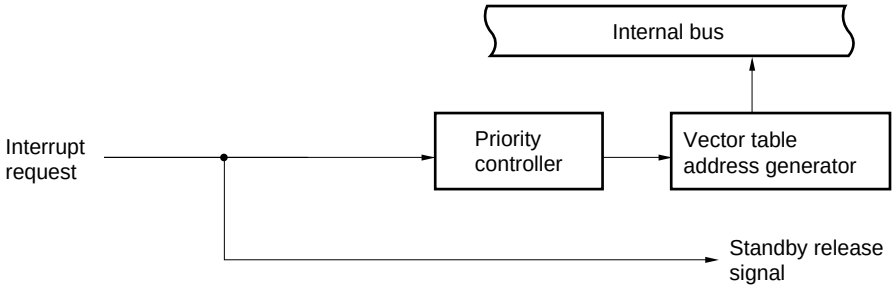
Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Maskable	10	INTBN1	End of automotive multiplex communication transmission/reception	Internal	0018H	(B)
	11	INTBN0	Generation of an automotive multiplex communication reception error		001AH	
	12	INTCSI3	End of serial interface SIO3 transfer		001CH	
	13	INTSR0	End of serial interface UART reception		001EH	
	14	INTST0	End of serial interface UART transmission		0020H	
	15	INTAD0	End of A/D conversion		0022H	
Software	−	BRK	BRK instruction execution	−	003EH	(D)

Notes 1. Default Priority is the priority order when several maskable interrupts are generated at the same time. 0 is the highest priority and 15 is the lowest.

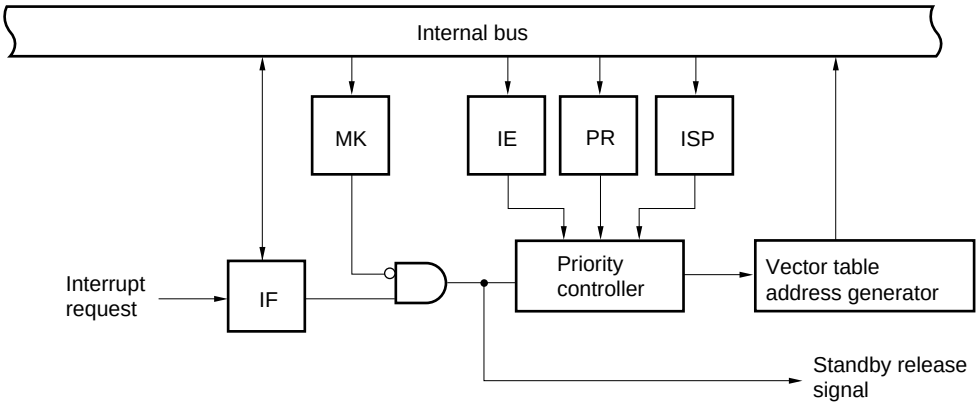
2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 6-1, respectively.

Figure 6-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External Maskable Interrupt

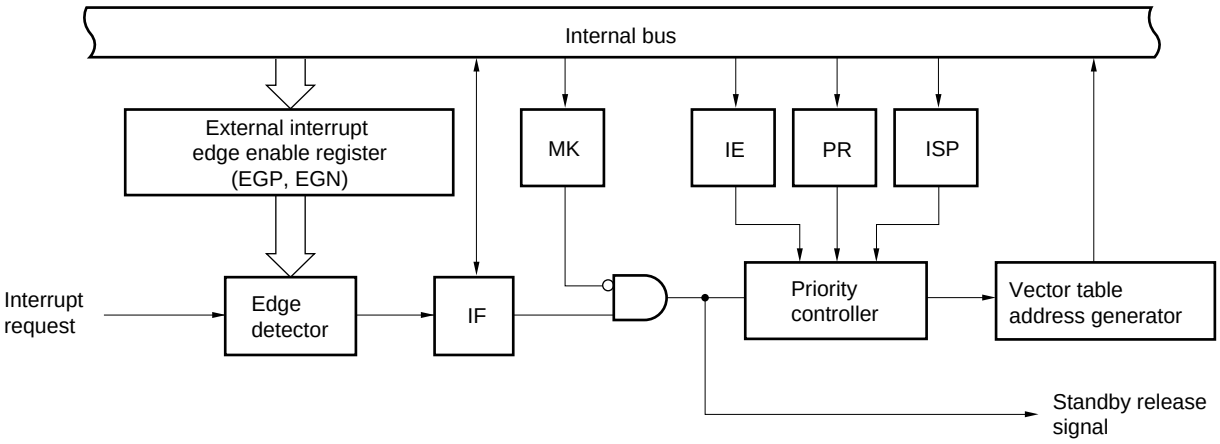
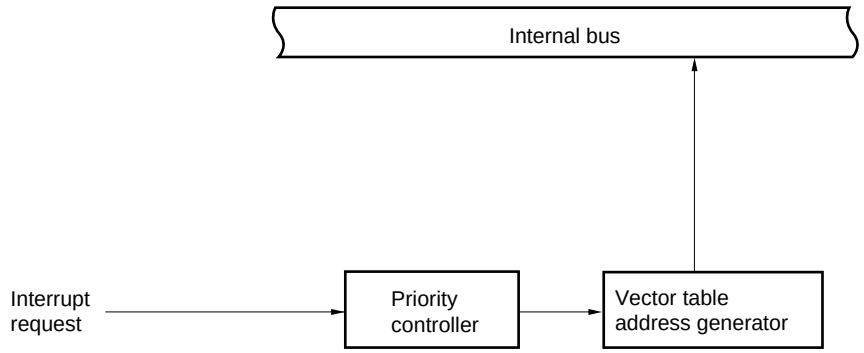


Figure 6-1. Basic Configuration of Interrupt Function (2/2)

(D) Software Interrupt



IF: Interrupt request flag
IE: Interrupt enable flag
ISP: In-service priority flag
MK: Interrupt mask flag
PR: Priority specification flag

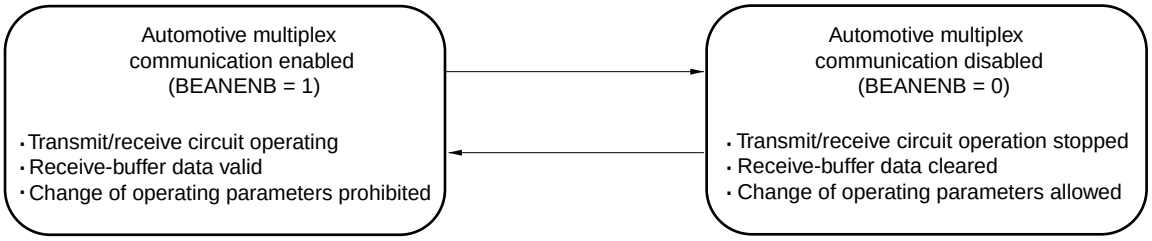
7. AUTOMOTIVE MULTIPLEX COMMUNICATION DISABLE FUNCTION

The automotive multiplex communication disable function sets the automotive multiplex communication function to a state whereby it cannot be used, for cases such as when the automotive multiplex communication operation parameters are changed.

The automotive multiplex communication disable function is controlled by bit 7 (BEANENB) of the automotive multiplex communication control register (BNCNT).

After reset, automotive multiplex communication is in a “not performed” state.

Figure 7-1. Automotive Multiplex Communication Disable Function



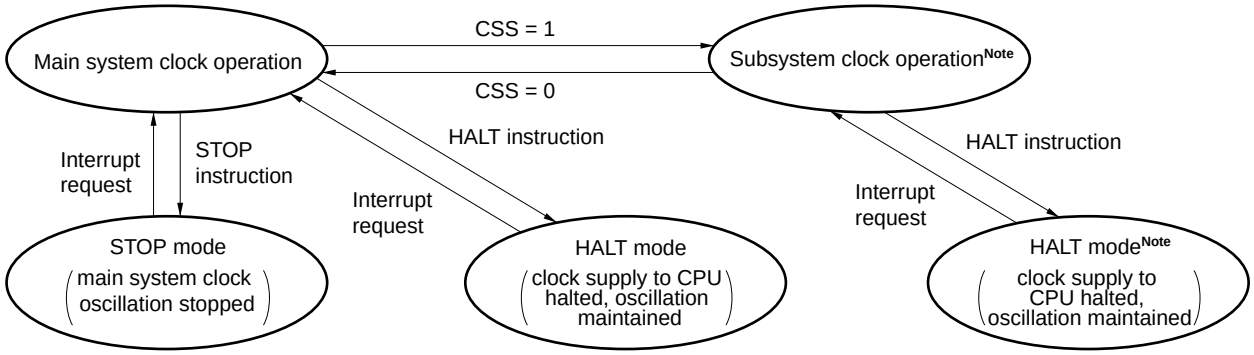
8. STANDBY FUNCTIONS

The following two standby functions are available for further reduction of system current consumption.

- HALT mode: In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation in combination with the normal operation mode.

- STOP mode: In this mode, oscillation of the main system clock is stopped. All operations performed on the main system clock are suspended, and only the subsystem clock is used, resulting in extremely small power consumption.

Figure 8-1. Standby Functions



Note The current consumption can be reduced by stopping the main system clock.
When the CPU is operating on the subsystem clock, set bit 7 (MCC) of the processor clock control register (PCC) to stop the main system clock. The STOP instruction cannot be used.

Caution When the main system clock has been stopped and the system is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Remark CSS: Bit 4 of PCC

9. RESET FUNCTIONS

The following two reset methods are available.

- External reset by $\overline{\text{RESET}}$ signal input.
- Internal reset by watchdog timer program loop time detection

10. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

1st operand \ 2nd operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL+B] [HL+C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL+byte] [HL+B] [HL+C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

2nd operand / 1st operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL.

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

2nd operand / 1st operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instructions/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

2nd operand / 1st operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL, BR	CALLF	CALLT	BR, BC, BNC, BZ, BNZ
Compound instruction					BT, BF, BTCLR, DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	AV_{REF}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_I	P00 to P02, P10 to P17, P20 to P27, P30 to P33, P40 to P47, P70, P71, BRxD, X1, X2, CL1, CL2, $\overline{RESET}$		–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pin	AV_{SS} – 0.3 to AV_{REF} + 0.3	V
★ Input current	I_I	Per pin (P50 to P57, P60 to P67)		15	mA
		Total for P50 to P57, P60 to P67		100	mA
Output current, high	I_{OH}	Per pin		–10	mA
		Total		–15	mA
Output current, low	I_{OL} Note	Per pin	Peak value	20	mA
			rms value	10	mA
		Total	Peak value	50	mA
			rms value	20	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–60 to +150	°C

Note The rms value should be calculated as follows: [rms value] = [Peak value] × $\sqrt{\text{Duty}}$

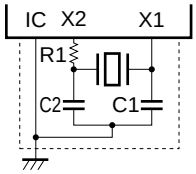
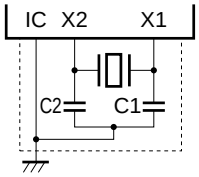
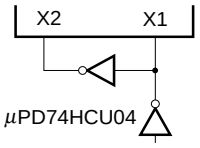
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.	P10 to P17, BRxD			15	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V.	P00 to P02, P20 to P27, P30 to P33, P40 to P47, P50 to P57, P60 to P67, P70, P71			15	pF
Output capacitance	C_O	f = 1 MHz Unmeasured pins returned to 0 V.	BTxD			15	pF

★ **Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)**

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note 1]		4	8	8.38	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} reaches oscillation voltage range MIN.			0.5	ms
Crystal resonator		Oscillation frequency (f_X)[Note 1]		4	8	8.38	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} reaches oscillation voltage range MIN.			1	ms
External clock		X1 input frequency (f_X)[Note 1]		4	8	8.38	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})		55		125	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

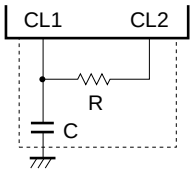
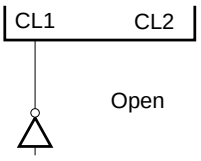
2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
RC oscillation		Oscillation frequency (f_{CC})Note	R = 518 kΩ ± 5% C = 33 pF ± 10%	25	40	55	kHz
External clock		CL1 input frequency (f_{CC})Note		25		55	kHz
		CL1 input high-/low-level width (t_{CCH}, t_{CCL})		9		20	μs

Note Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern in which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

★ **Recommended Oscillator Constant**

Main system clock: Ceramic resonator

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Remarks
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)	
Murata Mfg. Co., Ltd	CSA4.00MGA	4.0	30	30	0	4.0	5.5	
	CSTCC4.00MGA	4.0	15Note	15Note	0	4.0	5.5	On-chip capacitor
	CSA4.19MGA	4.194	30	30	0	4.0	5.5	
	CSTCC4.19MGA	4.194	15Note	15Note	0	4.0	5.5	On-chip capacitor
	CSA8.00MTZA	8.0	30	30	0	4.0	5.5	
	CSTCC8.00MGA	8.0	15Note	15Note	0	4.0	5.5	On-chip capacitor
	CSA8.38MTZA	8.38	30	30	0	4.0	5.5	
	CSTCC8.38MGA	8.38	15Note	15Note	0	4.0	5.5	On-chip capacitor

Note Indicates the capacitance of the on-chip capacitor.

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10 to P17, P21, P23, P25 to P27, P30 to P33, P40 to P47		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P02, P20, P22, P24, P70, P71, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	P50 to P57, P60 to P67, BRxD		0.8V_{DD}		V_{DD}	V
	V_{IH4}	X1, X2, CL1		V_{DD} – 0.5		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P17, P21, P23, P25 to P27, P30 to P33, P40 to P47		0		0.3V_{DD}	V
	V_{IL2}	P00 to P02, P20, P22, P24, P70, P71, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL3}	P50 to P57, P60 to P67, BRxD		0		0.4V_{DD}	V
	V_{IL4}	X1, X2, CL1		0		0.4	V
Output voltage, high	V_{OH1}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD} – 1.0		V_{DD}	V
	V_{OH2}	I_{OH} = –100 μA		V_{DD} – 0.5		V_{DD}	V
Output voltage, low	V_{OL1}	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA				0.4	V
	V_{OL2}	I_{OL} = 400 μA				0.5	V
Input leakage current, high	I_{LIH1}	P00 to P02, P10 to P17, P20 to P27, P30 to P33, P40 to P47, P50 to P57, P60 to P67, P70, P71, BRxD	V_{IN} = V_{DD}			3	μA
★	I_{LIH2}	X1, X2, CL1	V_{IN} = V_{DD}			20	μA
Input leakage current, low	I_{LIL1}	P00 to P02, P10 to P17, P20 to P27, P30 to P33, P40 to P47, P50 to P57, P60 to P67, P70, P71, BRxD	V_{IN} = 0 V			–3	μA
★	I_{LIL2}	X1, X2, CL1	V_{IN} = 0 V			–20	μA
Output leakage current, high	I_{LOH}	V_{OUT} = V_{DD}				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistor	R	V_{IN} = 0 V, P00 to P02		15	30	90	kΩ
Input current (V_{IN} > V_{DD})	I_{I1}	Per pin (P50 to P57, P60 to P67)	Typical value			0.3	mA
	I_{I2}	Total for P50 to P57, P60 to P67	Typical value			4.8	mA
Supply current [Note 1]	I_{DD1}	8.0 MHz crystal oscillation operating mode [Note 2]			7.5	15	mA
	I_{DD2}	8.0 MHz crystal oscillation HALT mode			1.6	3.2	mA
	I_{DD3}	40 kHz RC oscillation operating mode [Note 3]			150	300	μA
	I_{DD4}	40 kHz RC oscillation HALT mode [Note 3]			60	120	μA
	I_{DD5}	STOP mode	CL1 = V_{DD}		1	30	μA

Notes 1. Refers to the current flowing to the V_{DD} pins. The current flowing to the A/D converter, ports, and on-chip pull-up resistors is not included.

2. High-speed mode operation (when processor clock control register (PCC) is set to 00H)

3. When the main system clock is stopped.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

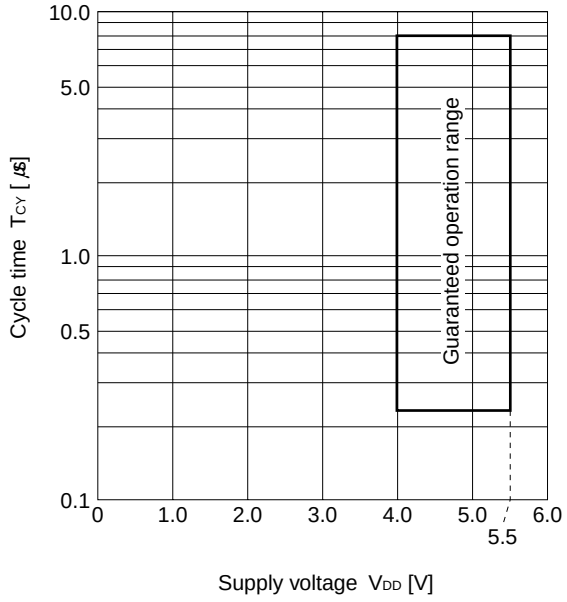
AC Characteristics

(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operating with main system clock	0.238		8	μs
		Operating with subsystem clock	72.7	100	160	μs
TI00 input frequency	f_{TI0}	Operating with external clock	0		f_X/4	MHz
TI00,TI01 input high-/low-level width	t_{CAPH}, t_{CAPL}	At capture trigger	$2/f_{asm} + 0.1$ Note			μs
Interrupt request input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP2	1			μs
$\overline{RESET}$ low-level width	t_{RSL}		10			μs

Note Selection of f_{asm} = f_X/4, f_X/8, f_X/16 is possible with bits 0 and 1 (PRM00, PRM01) of the prescaler mode register (PRM0).

T_{CY} vs V_{DD} (main system clock operation)



(2) Serial interface (T_A = –40 to +85°C, V_{DD} = 4.0 to 5.5 V)

(a) Automotive multiplex communication

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate				10		Kbps

(b) 3-wire serial I/O mode ($\overline{SCK}$: Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}		800			ns
$\overline{SCK}$ high-/low-level width	t_{KH1}, t_{KL1}		$t_{KCY1}/2 - 50$			ns
SI setup time (to $\overline{SCK}\uparrow$)	t_{SIK1}		100			ns
SI hold time (from $\overline{SCK}\uparrow$)	t_{KSI1}		400			ns
Delay time from $\overline{SCK}\downarrow$ to SO output	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the $\overline{SCK}$ and SO output lines.

(c) 3-wire serial I/O mode ($\overline{SCK}$: External clock input)

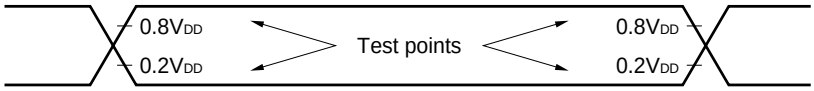
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}		800			ns
$\overline{SCK}$ high-/low-level width	t_{KH2}, t_{KL2}		400			ns
SI setup time (to $\overline{SCK}\uparrow$)	t_{SIK2}		100			ns
SI hold time (from $\overline{SCK}\uparrow$)	t_{KSI2}		400			ns
Delay time from $\overline{SCK}\downarrow$ to SO output	t_{KSO2}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the SO output lines.

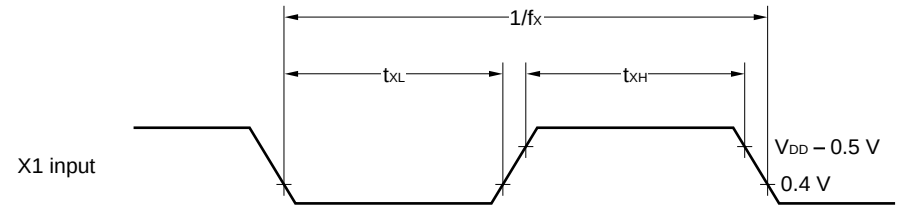
(d) UART mode (dedicated baud rate generator output)

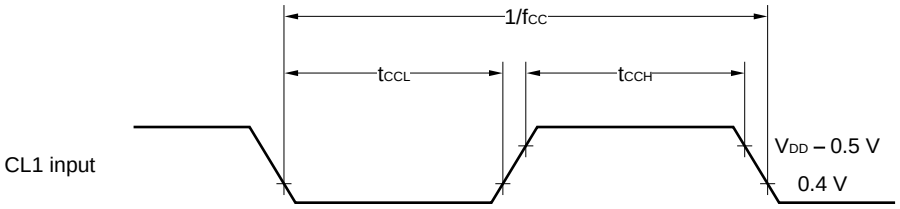
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					125	Kbps

AC Timing Test Points (Excluding X1, CL1 Inputs)

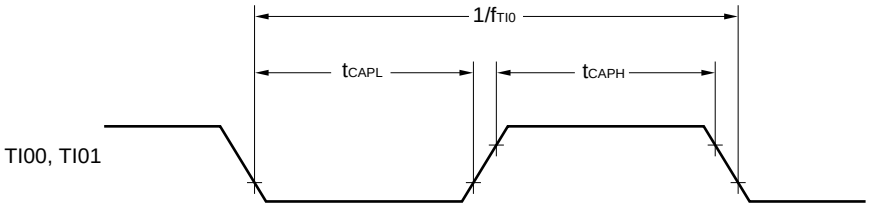


Clock Timing



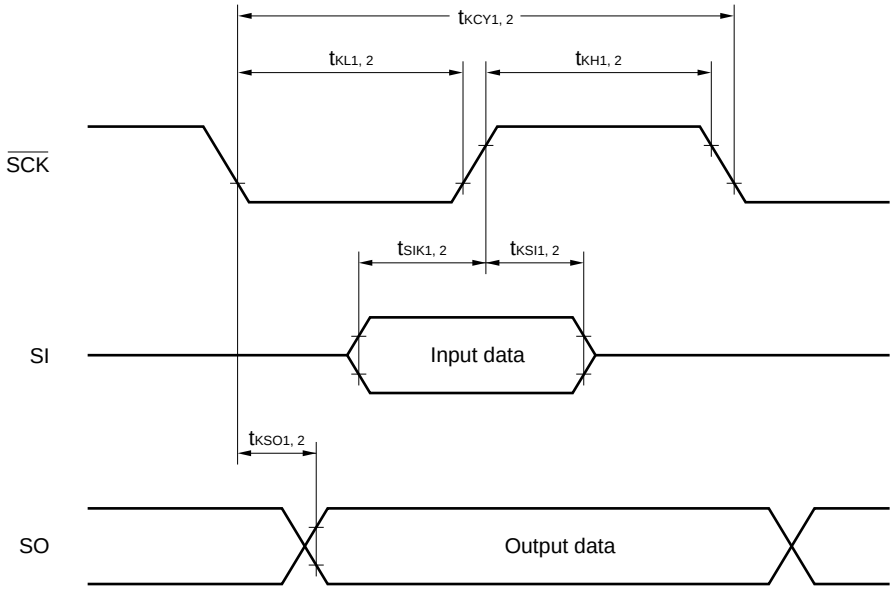


TI Timing



Serial Transfer Timing

3-wire serial I/O mode:



A/D Converter Characteristics (T_A = –40 to +85°C, AV_{REF} = V_{DD} = 4.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V, f_X = 8.38 MHz)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					8	Bits
Overall error[Note]					± 0.6	%FSR
Conversion time	t_{CONV}		14			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF} + 0.3	V
AV_{REF} current	I_{REF}	When A/D converter is operating		1.0	1.4	mA
		When A/D converter is not operating		1.0	1.0	μA

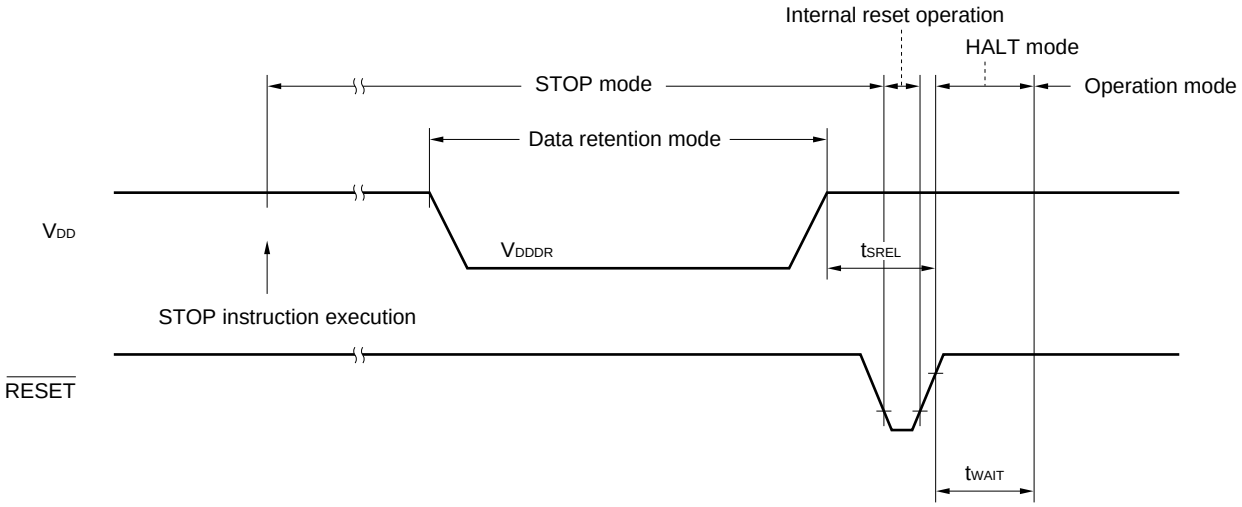
Note Excludes quantization error (±1/2 LSB). This value is indicated as a ratio to the full-scale value.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

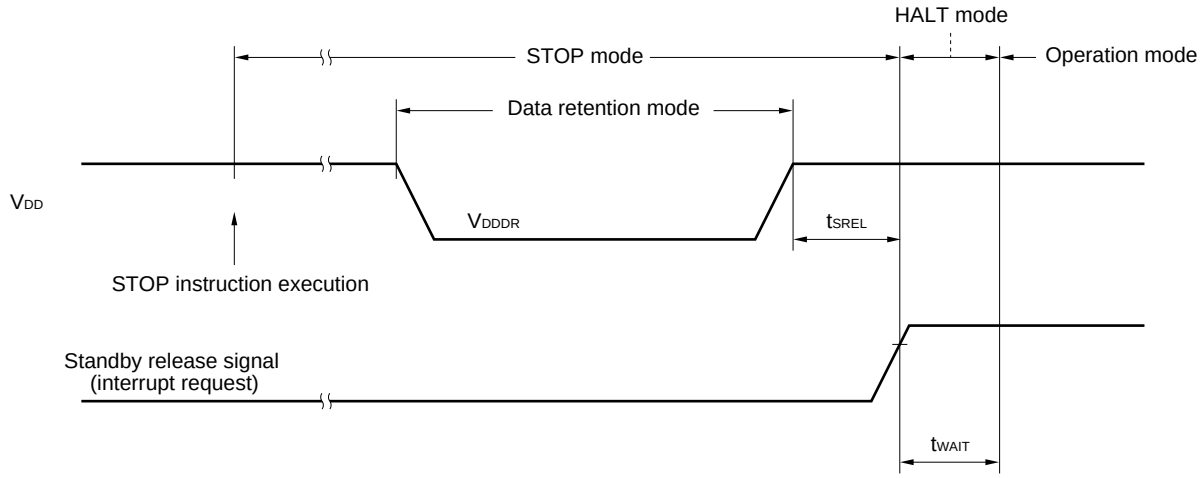
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		2.0		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		s
		Release by interrupt request		**Note**		s

Note Selection of $2^{12}/f_X$ and $2^{14}/f_X$ to $2^{17}/f_X$ is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

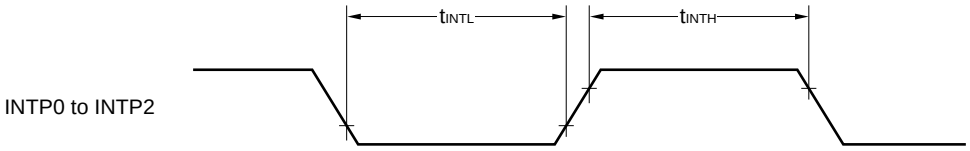
Data Retention Timing (STOP Mode Release by $\overline{RESET}$)



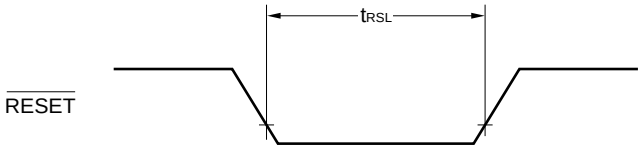
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)



Interrupt Request Input Timing

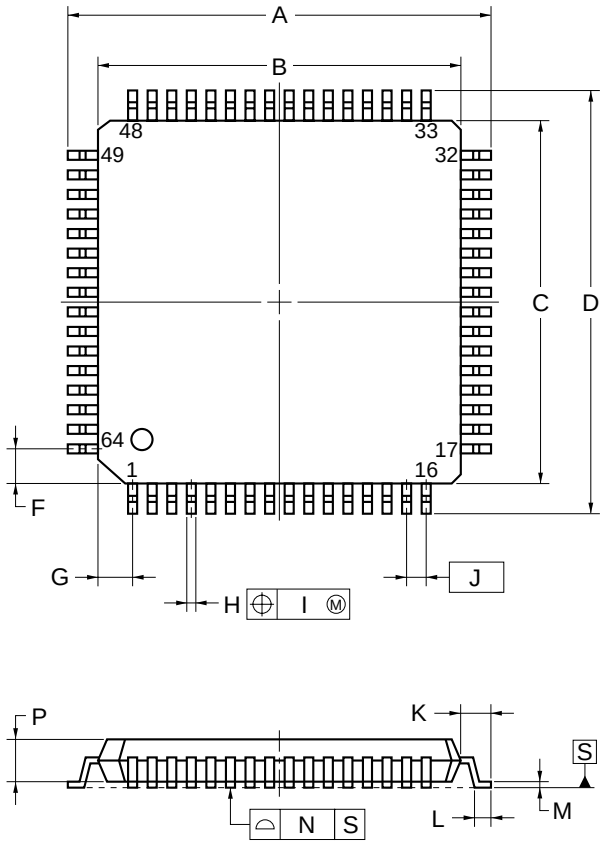


$\overline{\text{RESET}}$ Input Timing

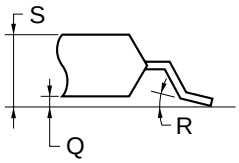


12. PACKAGE DRAWINGS

64-PIN PLASTIC LQFP (12x12)



detail of lead end



NOTE

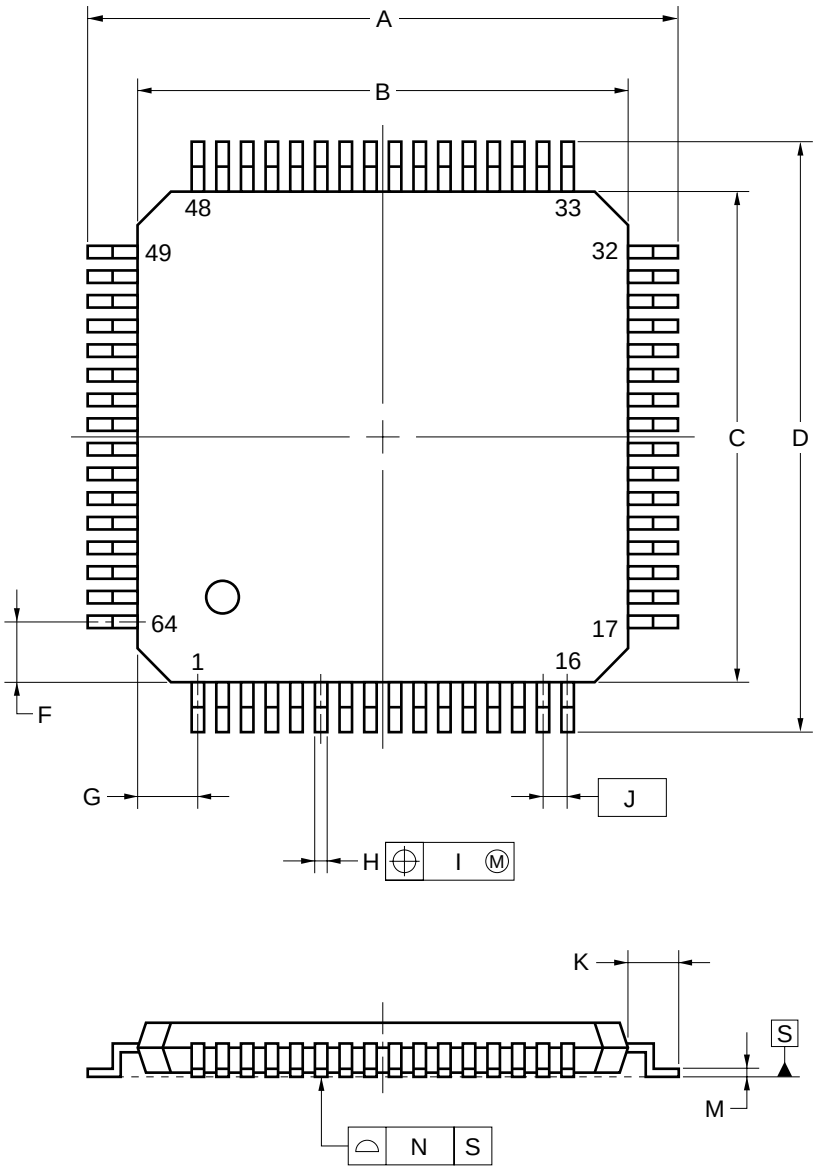
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	14.8±0.4
B	12.0±0.2
C	12.0±0.2
D	14.8±0.4
F	1.125
G	1.125
H	0.32±0.08
I	0.13
J	0.65 (T.P.)
K	1.4±0.2
L	0.6±0.2
M	$0.17^{+0.08}_{-0.07}$
N	0.10
P	1.4±0.1
Q	0.125±0.075
R	5°±5°
S	1.7 MAX.

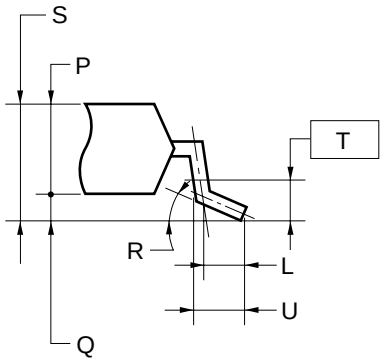
P64GK-65-8A8-3

64-PIN PLASTIC TQFP (12x12)

★



detail of lead end



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	14.0±0.2
B	12.0±0.2
C	12.0±0.2
D	14.0±0.2
F	1.125
G	1.125
H	$0.32^{+0.06}_{-0.10}$
I	0.13
J	0.65 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	1.0
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.1±0.1
T	0.25
U	0.6±0.15

P64GK-65-9ET-3

★ 13. RECOMMENDED SOLDERING CONDITIONS

The μPD780993(A) should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 13-1. Surface-Mount Type Soldering Conditions

μPD780993GK(A)-×××-8A8: 64-pin plastic LQFP (12 × 12 mm)
μPD780993GK(A)-×××-9ET (under development): 64-pin plastic TQFP (12 × 12 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-107-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD780993(A).
Also refer to **(4) Cautions on using development tools**.

(1) Language processing software

RA78K/0	Assembler package common to 78K/0 Series
CC78K/0	C compiler package common to 78K/0 Series
DF780994	Device file for μPD780993 Subseries
CC78K/0-L	C compiler library source file common to 78K/0 Series

(2) Debugging tools

IE-78K0-NS	In-circuit emulator common to 78K/0 Series
IE-70000-MS-PS-B	Power supply unit for IE-78K0-NS
IE-70000-98-IF-C	Interface adapter when using PC-9800 series PC (except notebook type) as host machine (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable when using PC-9800 series notebook PC as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT™ or compatibles as host machine (ISA bus supported)
IE-70000-PCI-IF-A	Interface adapter when using a PC with PCI bus as host machine
IE-780994-NS-EM1	Emulation board to emulate μPD780993 Subseries
NP-64GK	Emulation probe for 64-pin plastic LQFP (GK-8A8 type) and 64-pin plastic TQFP (GK-9ET type)
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
DF780994	Device file for μPD780993 Subseries

(3) Real-time OS

RX78K/0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series

(4) Cautions on using development tools

- The ID78K0-NS and SM78K0 are used in combination with the DF780994.
- The CC78K/0 and RX78K/0 are used in combination with the RA78K/0 and DF780994.
- For third-party development tools, see the **78K/0 Series Selection Guide (U11126E)**.
- The host machine and OS suitable for each software are as follows:

Software \ Host Machine [OS]	PC PC-9800 series [Windows™] IBM PC/AT and compatibles [Japanese/English Windows]	EWS HP9000 Series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K/0	√Note	√
CC78K/0	√Note	√
ID78K0-NS	√	–
SM78K0	√	–
RX78K/0	√Note	√
MX78K0	√Note	√

Note DOS-based software

APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document No.
μPD780993 Subseries User's Manual	Under preparation
μPD780993(A) Data Sheet	This document
μPD78F0994 Preliminary Product Information	U13143E
78K/0 Series User's Manual Instruction	U12326E

Documents Related to Development Tools (User's Manuals)

Document Name		Document No.
RA78K0 Assembler Package	Operation	U11802E
	Language	U11801E
	Structured Assembly Language	U11789E
CC78K0 C Compiler	Operation	U11517E
	Language	U11518E
CC78K/0 C Compiler Application Note	Programming Know-How	U13034E
IE-78K0-NS		U13731E
IE-780994-NS-EM1		To be prepared
SM78K0 System Simulator Windows Based	Reference	U10181E
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092E
ID78K0-NS Integrated Debugger	Reference	U12900E
ID78K0 Integrated Debugger Windows Based	Guide	U11649E
ID78K0 Integrated Debugger PC Based	Reference	U11539E

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No.
78K/0 Series Real-Time OS	Fundamental	U11537E
	Installation	U11536E
78K/0 Series OS MX78K0	Fundamental	U12257E

Other Related Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades in NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

[MEMO]

NOTES FOR BiCMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS

Note:

No connection for device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. Input levels of devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF BiCMOS DEVICES

Note:

Power-on does not necessarily define initial status of device. Production process of BiCMOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset

Regional Information

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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