NEC

MOS INTEGRATED CIRCUIT

μPD78070AY

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78070AY is a limited-function product from which the on-chip ROM of the μPD78078Y Subseries has been removed. Through interchangeable external ROM, program maintenance can be performed easily. Besides a high-speed, high-performance CPU, this microcontroller has on-chip RAM, I/O ports, 8-bit resolution A/D converter, 8-bit resolution D/A converter, timer, serial interface, real-time output port, interrupt control, and various other peripheral hardware.

Detailed information about product features and specifications can be found in the following documents. Be sure to read the following documents before starting design.

μPD78070A, 78070AY User's Manual : U10200E
78K/0 Series User's Manual – Instructions : U12326E

FEATURES

- Internal large-capacity RAM
  - Internal high-speed RAM : 1024 bytes
  - Internal buffer RAM: 32 bytes
- External memory expansion space : 64 Kbytes
- Minimum instruction execution time can be varied from high-speed (0.4 μs) to ultra-low-speed (122 μs)
- I/O ports: 61 (N-ch open-drain : 8)
- 8-bit resolution A/D converter : 8 channels
- 8-bit resolution D/A converter : 2 channels
- Serial interface : 3 channels
  - 3-wire serial I/O/2-wire serial I/O/I^2C bus mode : 1 channel
  - 3-wire serial I/O mode : 1 channel
  - 3-wire serial I/O/UART mode : 1 channel
- Timer : 7 channels
- Power supply voltage : V_{DD} = 2.7 to 5.5 V

APPLICATIONS

Audio visual equipment (VCRs, audio equipment, etc.)

ORDERING INFORMATION

Part Number	Package
μPD78070AYGC-7EA	100-pin plastic QFP (Fine pitch) (14 × 14 mm, Resin thickness 1.45 mm)
★ μPD78070AYGC-8EU[Note]	100-pin plastic LQFP (Fine pitch) (14 × 14 mm, Resin thickness 1.40 mm)
μPD78070AYGF-3BA	100-pin plastic QFP (14 × 20 mm, Resin thickness 2.7 mm)

Note Under planning

Caution Two types of packages are provided for the μPD78070AYGC (Refer to 12. PACKAGE DRAWINGS). Contact an NEC sales representative for available packages.

The information in this document is subject to change without notice.

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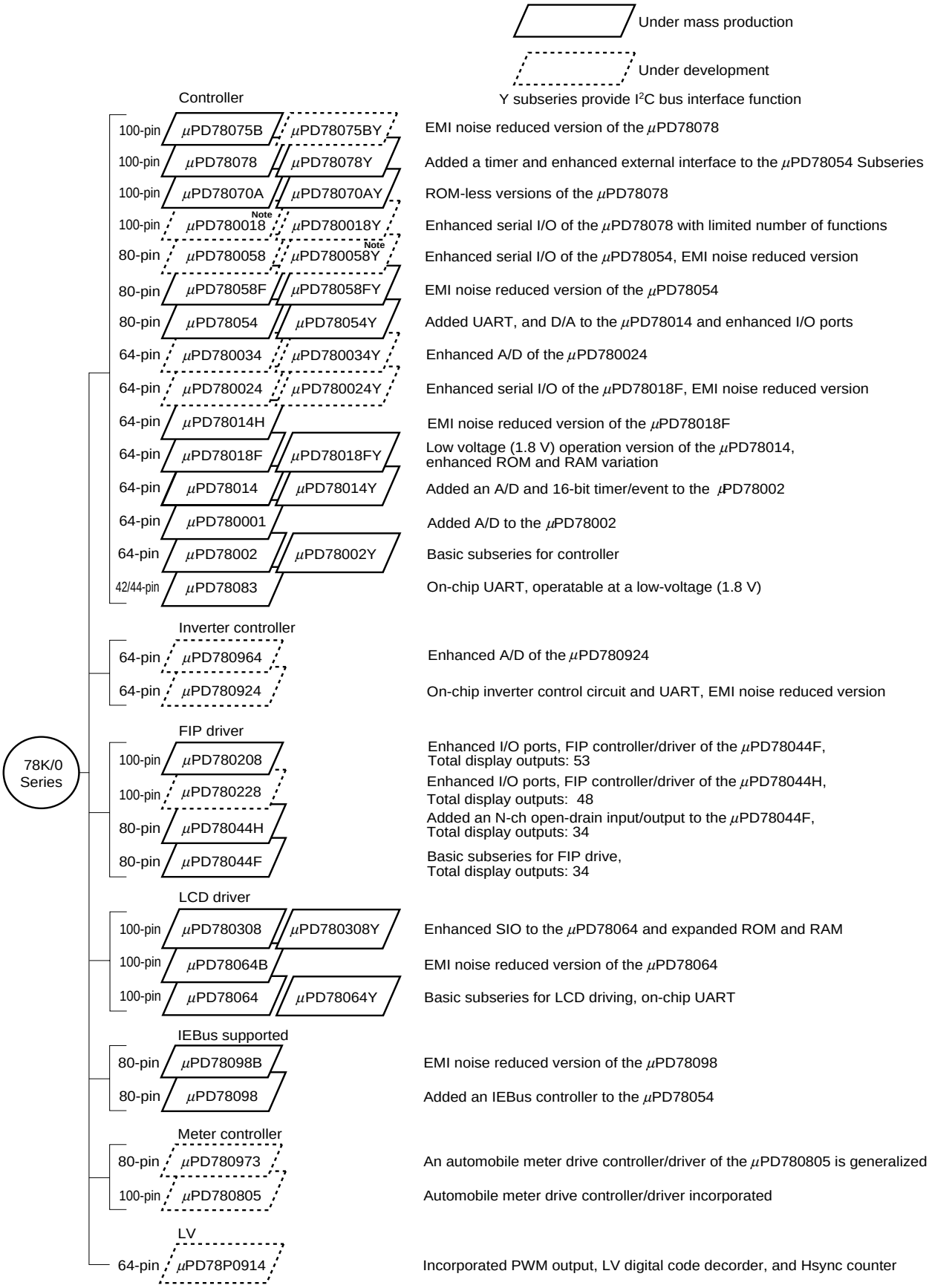
Date Published July 1997 N
Printed in Japan

The mark ★ shows major revised points.

★ 78K/0 Series Development

The following shows the 78K/0 Series products development. Subseries names are shown inside frames.



Note Under planning

The following table shows the differences among subseries functions.

Subseries name \ Function		ROM Capacity	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-bit	16-bit	Watch	WDT							
Controller	μPD78075B	32 K to 40 K	4 ch	1 ch	1 ch	1 ch	8 ch	—	2 ch	3 ch (UART: 1 ch)	88	1.8 V	Available
	μPD78078	48 K to 60 K											
	μPD78070A	—									61	2.7 V	
	μPD780018	48 K to 60 K							—	2 ch (Time division 3-wire: 1 ch)	88		
	μPD780058	24 K to 60 K	2 ch						2 ch	3 ch (Time division UART: 1 ch)	68	1.8 V	
	μPD78058F	48 K to 60 K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16 K to 60 K										2.0 V	
	μPD780034	8 K to 32 K					—	8 ch	—	3 ch (UART: 1 ch, Time division 3-wire: 1 ch)	51	1.8 V	
	μPD780024						8 ch	—					
	μPD78014H									2 ch	53		
	μPD78018F	8 K to 60 K											
	μPD78014	8 K to 32 K										2.7 V	
	μPD780001	8 K		—	—					1 ch	39		—
	μPD78002	8 K to 16 K			1 ch		—				53		Available
	μPD78083				—		8 ch			1 ch (UART: 1 ch)	33	1.8 V	—
Inverter controller	μPD780964	8 K to 32 K	3 ch	**Note**	—	1 ch	—	8 ch	—	2 ch (UART: 2 ch)	47	2.7 V	Available
	μPD780924						8 ch	—					
FIP driver	μPD780208	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	—	—	2 ch	74	2.7 V	—
	μPD780228	48 K to 60 K	3 ch	—	—					1 ch	72	4.5 V	
	μPD78044H	32 K to 48 K	2 ch	1 ch	1 ch						68	2.7 V	
	μPD78044F	16 K to 40 K								2 ch			
LCD driver	μPD780308	48 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	—	—	3 ch (Time division UART: 1 ch)	57	2.0 V	—
	μPD78064B	32 K								2 ch (UART: 1ch)			
	μPD78064	16 K to 32 K											
IEBus supported	μPD78098B	40 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	—	2 ch	3 ch (UART: 1ch)	69	2.7 V	Available
	μPD78098	32 K to 60 K											
Meter controller	μPD780973	24 K to 32 K	3 ch	1 ch	1 ch	1 ch	5 ch	—	—	2 ch (UART: 1ch)	56	4.5 V	—
	μPD780805	40 K to 60 K	2 ch				8 ch				39	2.7 V	
LV	μPD78P0914	32 K	6 ch	—	—	1 ch	8 ch	—	—	2 ch	54	4.5 V	Available

Note 10-bit timer: 1 channel

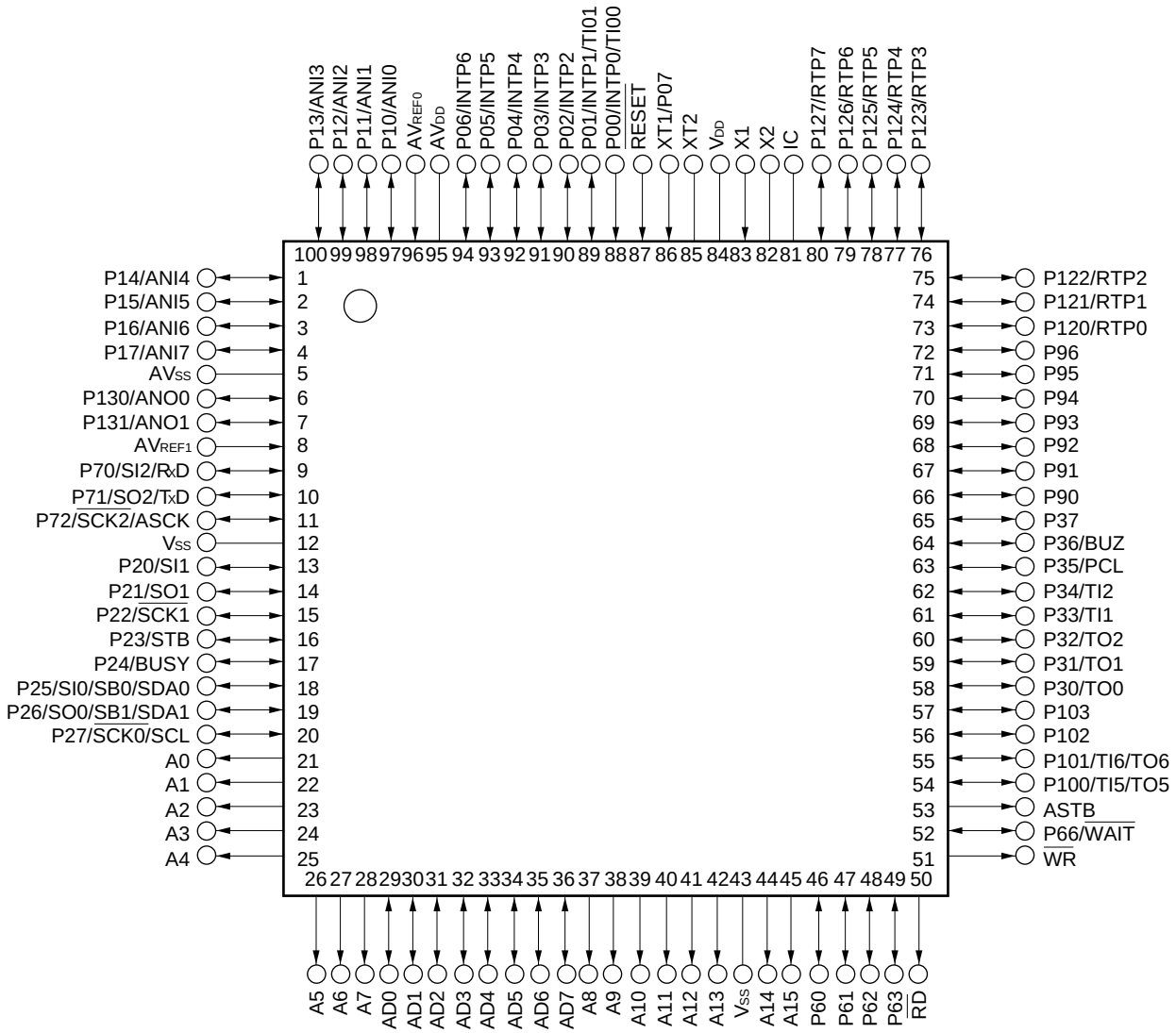
FUNCTION DESCRIPTION

Item		Function
Internal memory	ROM	No
	High-speed RAM	1024 bytes
	Buffer RAM	32 bytes
Memory space		64 Kbytes
General registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Minimum instruction execution time		On-chip minimum instruction execution time variable function
	When main system clock is selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (@ 5.0-MHz operation)
	When subsystem clock is selected	122 μs (@ 32.768-kHz operation)
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits, 16 bits / 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjust, etc.
I/O ports		Total : 61 • CMOS input : 2 • CMOS I/O : 51 • N-ch open-drain I/O : 8
A/D converter		• 8-bit resolution × 8 channels
D/A converter		• 8-bit resolution × 2 channels
Serial interface		• 3-wire serial I/O/2-wire serial I/O/I^2C bus mode selectable: 1 channel • 3-wire serial I/O mode (on-chip max. 32-byte automatic data transmit/receive function): 1 channel • 3-wire serial I/O/UART mode selectable: 1 channel
Timer		• 16-bit timer/event counter: 1 channel • 8-bit timer/event counter: 4 channels • Watch timer: 1 channel • Watchdog timer: 1 channel
Timer output		5 (14-bit PWM output × 1, 8-bit PWM output × 2)
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (main system clock: @ 5.0-MHz operation) 32.768 kHz (subsystem clock: @ 32.768-kHz operation)
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (main system clock: @ 5.0-MHz operation)
Vectored interrupt source	Maskable	Internal : 15, external : 7
	Non-maskable	Internal : 1
	Software	1
Test input		Internal : 1
Power supply voltage		V_{DD} = 2.7 to 5.5 V
Package		★ • 100-pin plastic QFP (Fine pitch) (14 × 14 mm, Resin thickness 1.45 mm) • 100-pin plastic LQFP (Fine pitch) (14 × 14 mm, Resin thickness 1.40 mm, under planning) • 100-pin plastic QFP (14 × 20 mm, Resin thickness 2.7 mm)

CONTENTS

1. PIN CONFIGURATION (Top View)

- 100-pin plastic QFP (Fine pitch) (14 × 14 mm, resin thickness: 1.45 mm)
  μPD78070AYGC-7EA
- ★ 100-pin plastic LQFP (Fine pitch) (14 × 14 mm, resin thickness: 1.40 mm)
  μPD78070AYGC-8EU[Note]



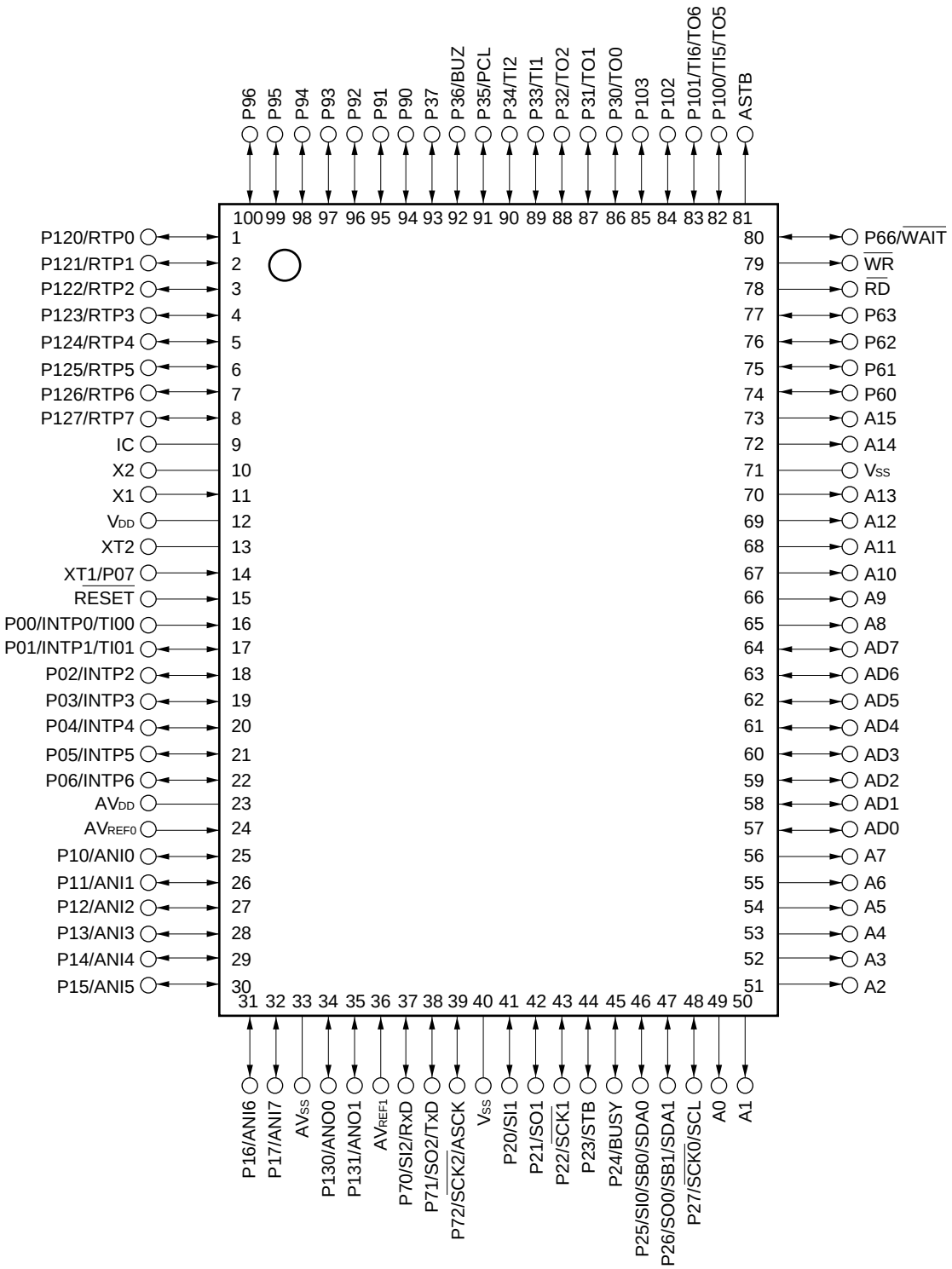
Note Under planning

Cautions 1. Connect IC (Internally Connected) pin directly to V_{SS}.

2. Connect AV_{DD} pin to V_{DD}.

3. Connect AV_{SS} pin to V_{SS}.

- 100-pin plastic QFP (14 × 20 mm)
  μPD78070AYGF-3BA



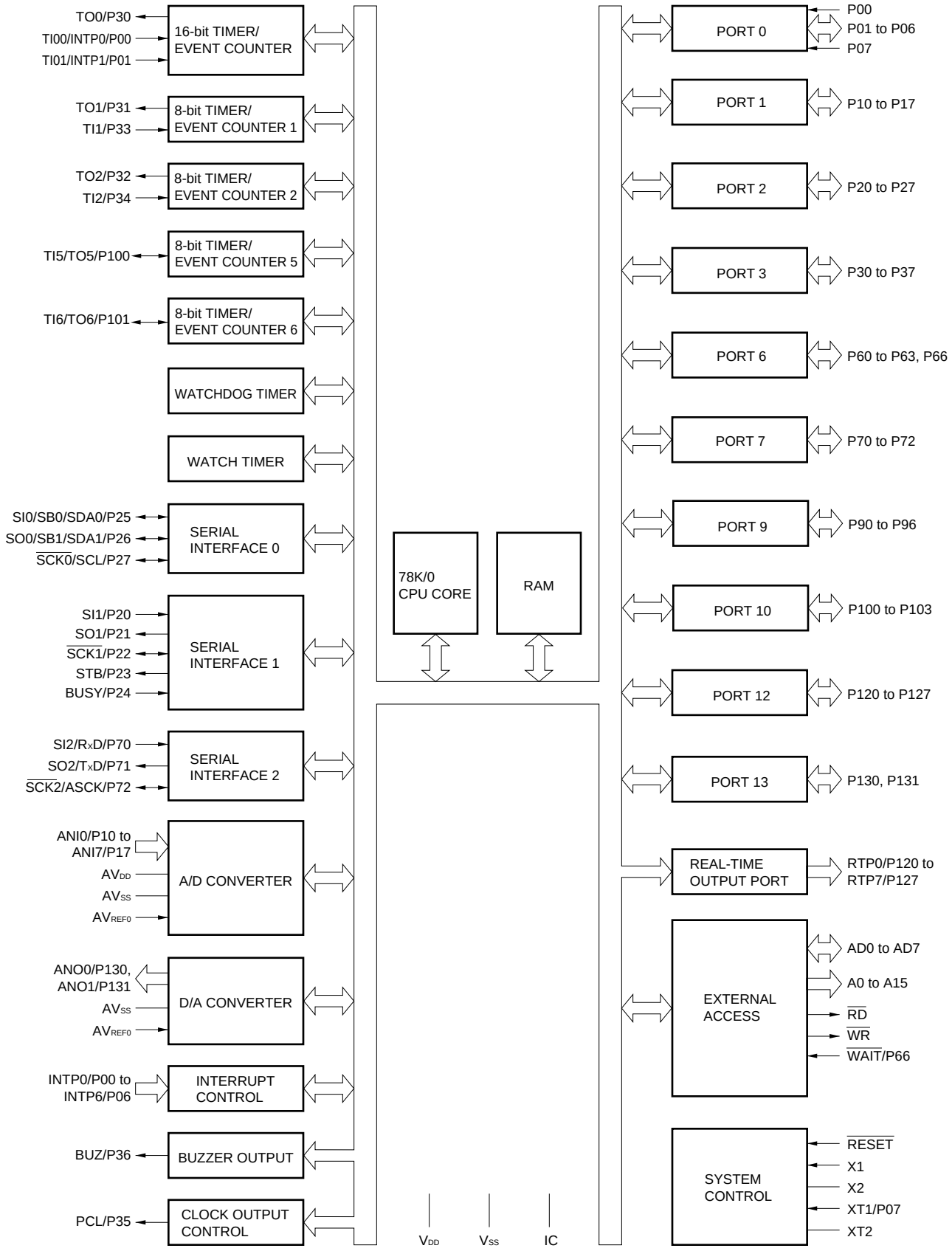
Cautions 1. Connect IC (Internally Connected) pin directly to V_{SS}.

2. Connect AV_{DD} pin to V_{DD}.

3. Connect AV_{SS} pin to V_{SS}.

A0 to A15	:	Address Bus
AD0 to AD7	:	Address/Data Bus
ANI0 to ANI7	:	Analog Input
ANO0, ANO1	:	Analog Output
ASCK	:	Asynchronous Serial Clock
ASTB	:	Address Strobe
AV_{DD}	:	Analog Power Supply
AV_{REF0}, AV_{REF1}	:	Analog Reference Voltage
AV_{SS}	:	Analog Ground
BUSY	:	Busy
BUZ	:	Buzzer Clock
IC	:	Internally Connected
INTP0 to INTP6	:	Interrupt from Peripherals
P00 to P07	:	Port0
P10 to P17	:	Port1
P20 to P27	:	Port2
P30 to P37	:	Port3
P60 to P63, P66	:	Port6
P70 to P72	:	Port7
P90 to P96	:	Port9
P100 to P103	:	Port10
P120 to P127	:	Port12
P130, P131	:	Port13
PCL	:	Programmable Clock
$\overline{RD}$	:	Read Strobe
$\overline{RESET}$	:	Reset
RTP0 to RTP7	:	Real-time Output Port
RxD	:	Receive Data
SB0, SB1	:	Serial Bus
$\overline{SCK0}$ to $\overline{SCK2}$	:	Serial Clock
SCL	:	Serial Clock
SDA0, SDA1	:	Serial Data
SI0 to SI2	:	Serial Input
SO0 to SO2	:	Serial Output
STB	:	Strobe
TI00, TI01	:	Timer Input
TI1, TI2, TI5, TI6	:	Timer Input
TO0 to TO2, TO5, TO6	:	Timer Output
V_{DD}	:	Power Supply
V_{SS}	:	Ground
$\overline{WAIT}$	:	Wait
$\overline{WR}$	:	Write Strobe
X1, X2	:	Crystal (Main System Clock)
XT1, XT2	:	Crystal (Subsystem Clock)

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins (1/2)

Pin Name	Input/Output	Function		After Reset	Alternate Function
P00	Input	Port 0 8-bit input/output port	Input only	Input	INTP0/TI00
P01	Input/output		Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P06					INTP6
P07[Note1]	Input		Input only	Input	XT1
P10 to P17	Input/output	Port 1 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.[Note 2]		Input	ANI0 to ANI7
P20	Input/output	Port 2 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.		Input	SI1
P21					SO1
P22					$\overline{\text{SCK1}}$
P23					STB
P24					BUSY
P25					SI0/SB0/SDA0
P26					SO0/SB1/SDA1
P27					$\overline{\text{SCK0}}$/SCL
P30	Input/output	Port 3 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—

Notes 1. When using the P07/XT1 pin as an input port, set bit 6 (FRC) of the processor clock control register (PCC) to 1. Do not use the on-chip feedback resistor of the subsystem clock oscillator.

2. When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog inputs, their on-chip pull-up resistors are automatically disconnected.

3.1 Port Pins (2/2)

Pin Name	Input/Output	Function		After Reset	Alternate Function
P60	Input/output	Port 6 5-bit input/output port Input/output can be specified bit-wise.	N-ch open-drain input/output port LED can be driven directly.	Input	—
P61					
P62					
P63					
P66			When used as an input port, on-chip pull-up resistor can be used by software.		$\overline{\text{WAIT}}$
P70	Input/output	Port 7 3-bit input/output port Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.		Input	SI2/RxD
P71					SO2/TxD
P72					$\overline{\text{SCK2}}$/ASCK
P90	Input/output	Port 9 7-bit input/output port Input/output can be specified bit-wise.	N-ch open-drain input/output port	Input	—
P91					
P92					
P93					
P94			When used as an input port, on-chip pull-up resistor can be used by software.		
P95					
P96					
P100	Input/output	Port 10 4-bit input/output port Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.		Input	TI5/TO5
P101					TI6/TO6
P102, P103					—
P120 to P127	Input/output	Port 12 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.		Input	RTP0 to RTP7
P130, P131	Input/output	Port 13 2-bit input/output port Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.		Input	ANO0, ANO1

3.2 Non-port Pins (1/2)

Pin Name	Input/Output	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input by which the active edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
INTP6				P06
SI0	Input	Serial interface serial data input	Input	P25/SB0/SDA0
SI1				P20
SI2				P70/RxD
SO0	Output	Serial interface serial data output	Input	P26/SB1/SDA1
SO1				P21
SO2				P71/TxD
SB0	Input/Output	Serial interface serial data input/output	Input	P25/SI0/SDA0
SB1				P26/SO0/SDA1
SDA0				P25/SI0/SB0
SDA1				P26/SO0/SB1
$\overline{SCK0}$	Input/Output	Serial interface serial clock input/output	Input	P27/SCL
$\overline{SCK1}$				P22
$\overline{SCK2}$				P72/ASCK
SCL				P27/$\overline{SCK0}$
STB	Output	Serial interface automatic transmit/receive strobe output	Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input	Input	P24
RxD	Input	Asynchronous serial interface serial data input	Input	P70/SI2
TxD	Output	Asynchronous serial interface serial data output	Input	P71/SO2
ASCK	Input	Asynchronous serial interface serial clock input	Input	P72/$\overline{SCK2}$
TI00	Input	External count clock input to 16-bit timer (TM0)	Input	P00/INTP0
TI01		Capture trigger signal input to capture register (CR00)		P01/INTP1
TI1		External count clock input to 8-bit timer (TM1)		P33
TI2		External count clock input to 8-bit timer (TM2)		P34
TI5		External count clock input to 8-bit timer (TM5)		P100/TO5
TI6		External count clock input to 8-bit timer (TM6)		P101/TO6
TO0	Output	16-bit timer (TM0) output (also used for 14-bit PWM output)	Input	P30
TO1		8-bit timer (TM1) output		P31
TO2		8-bit timer (TM2) output		P32
TO5		8-bit timer (TM5) output (also used for 8-bit PWM output)		P100/TI5
TO6		8-bit timer (TM6) output (also used for 8-bit PWM output)		P101/TI6
PCL	Output	Clock output (for main system clock, subsystem clock trimming)	Input	P35

3.2 Non-port Pins (2/2)

Pin Name	Input/Output	Function	After Reset	Alternate Function
BUZ	Output	Buzzer output	Input	P36
RTP0 to RTP7	Output	Real-time output port by which data is output in synchronization with a trigger	Input	P120 to P127
AD0 to AD7	Input/Output	Data bus for external memory	Input	—
A0 to A15	Output	Address bus for external memory	Input	—
$\overline{RD}$	Output	External memory read operation strobe signal output	Input	—
$\overline{WR}$		External memory write operation strobe signal output		—
$\overline{WAIT}$	Input	Wait insertion at external memory access	Input	P66
ANI0 to ANI7	Input	A/D converter analog input	Input	P10 to P17
ANO0, ANO1	Output	D/A converter analog output	Input	P130, P131
AV_{REF0}	Input	A/D converter reference voltage input	—	—
AV_{REF1}	Input	D/A converter reference voltage input	—	—
AV_{DD}	—	A/D converter analog power supply. Connected to V_{DD}.	—	—
AV_{SS}	—	A/D converter and D/A converter ground potential Connected to V_{SS}.	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection	Input	P07
XT2	—		—	—
V_{DD}	—	Positive power supply	—	—
V_{SS}	—	Ground potential	—	—
IC	—	Internal connection. Connected directly to V_{SS}.	—	—

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, see Figure 3-1.

Table 3-1. Types of Pin Input/Output Circuits (1/2)

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connection for Unused Pins
P00/INTP0/TI00	2	Input	Connect to V_{SS}.
P01/INTP1/TI01	8-A	Input/Output	Independently connect to V_{SS} via a resistor.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P06/INTP6			
P07/XT1	16	Input	Connect to V_{DD}.
P10/ANI0 to P17/ANI7	11	Input/Output	Independently connect to V_{DD} or V_{SS} via a resistor.
P20/SI1	8-A		
P21/SO1	5-A		
P22/$\overline{SCK1}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0/SDA0	10-A		
P26/SO0/SB1/SDA1			
P27/$\overline{SCK0}$/SCL			
P30/TO0	5-A		
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P60 to P63	13-C	Input/Output	Independently connect to V_{DD} via a resistor.
P66/$\overline{WAIT}$	5-A	Input/Output	Independently connect to V_{DD} or V_{SS} via a resistor.

Table 3-1. Types of Pin Input/Output Circuits (2/2)

Pin Name	Input/Output Circuit Type	Input/Output	Recommended Connection for Unused Pins
P70/SI2/RxD	8-A	Input/Output	Independently connect to V_{DD} or V_{SS} via a resistor.
P71/SO2/TxD	5-A		
P72/$\overline{SCK2}$/ASCK	8-A		
P90 to P93	13-C	Input/Output	Independently connect to V_{DD} via a resistor.
P94 to P96	5-A	Input/Output	Independently connect to V_{DD} or V_{SS} via a resistor.
P100/TI5/TO5	8-A		
P101/TI6/TO6			
P102, P103	5-A		
P120/RTP0 to P127/RTP7			
P130/ANO0, P131/ANO1	12-A	Input/Output	Independently connect to V_{SS} via a resistor.
AD0 to AD7	5-E	Input/Output	Independently connect to V_{DD} via a resistor.
A0 to A15	5-A	Output	Leave open.
$\overline{RD}$			
$\overline{WR}$			
ASTB			
$\overline{RESET}$	2	Input	—
XT2	16	—	Leave open.
AV_{REF0}	—		Connect to V_{SS}.
AV_{REF1}			Connect to V_{DD}.
AV_{DD}			
AV_{SS}			Connect to V_{SS}.
IC			Connect directly to V_{SS}.

Figure 3-1. Pin Input/Output Circuits (1/2)

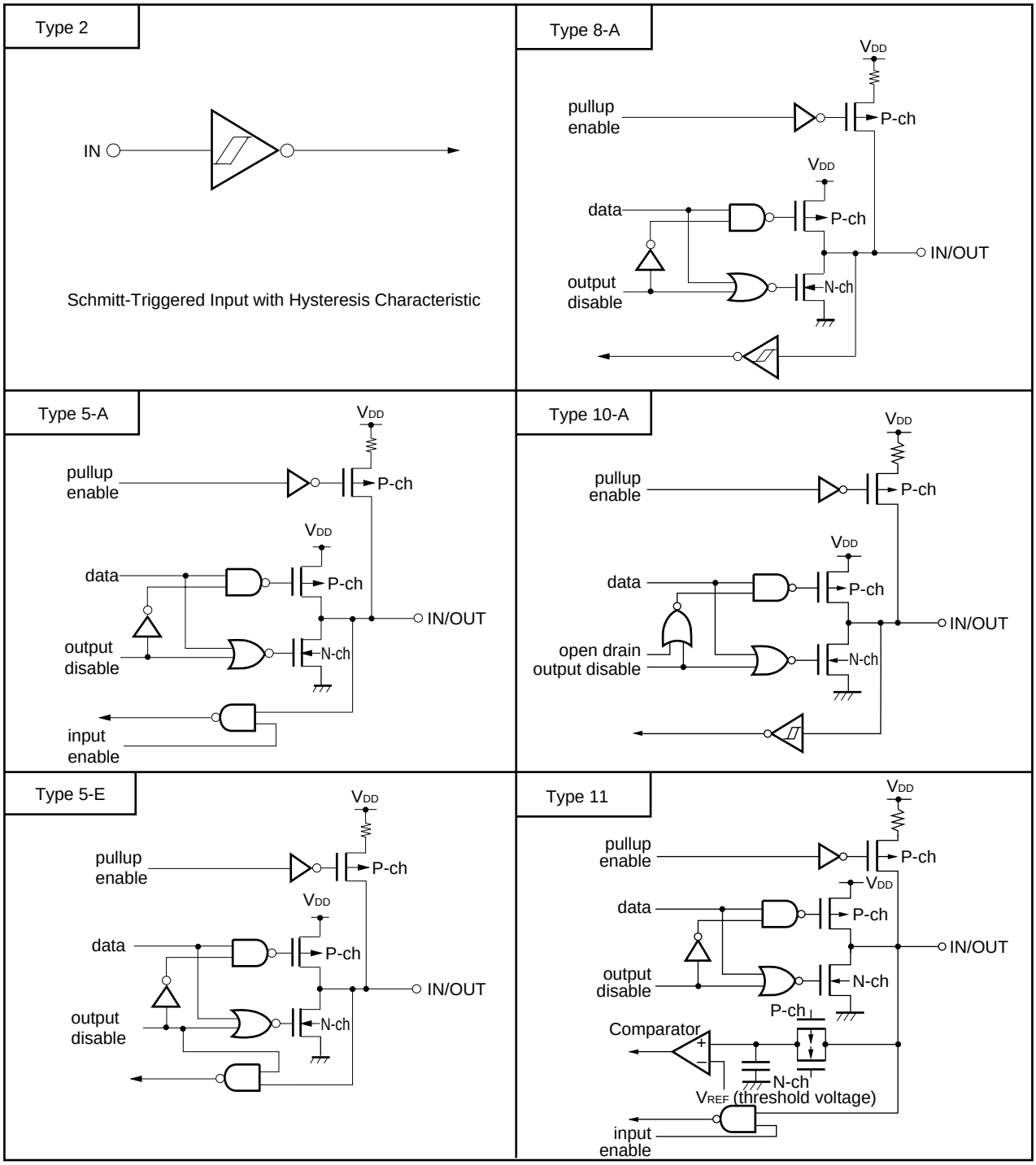
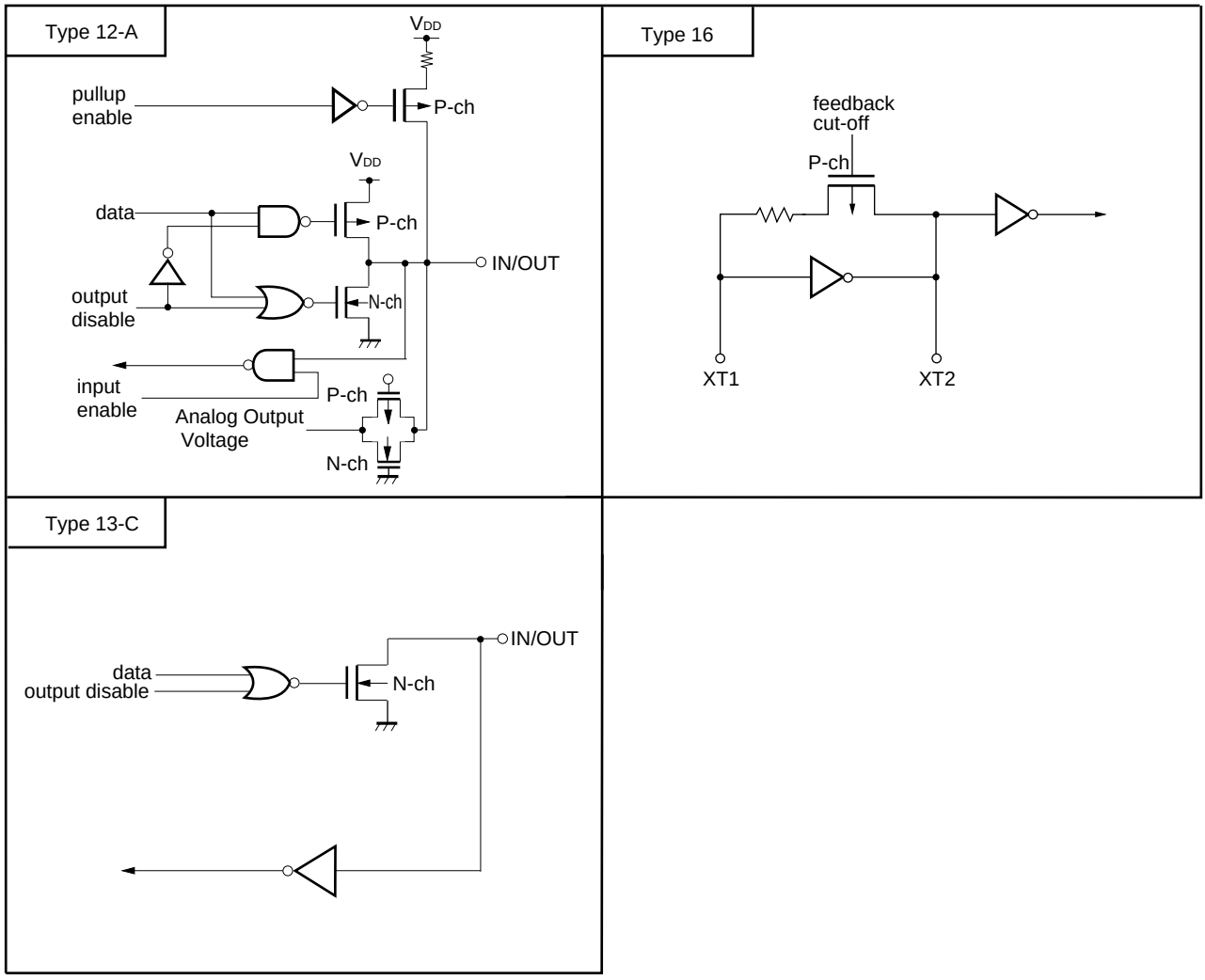


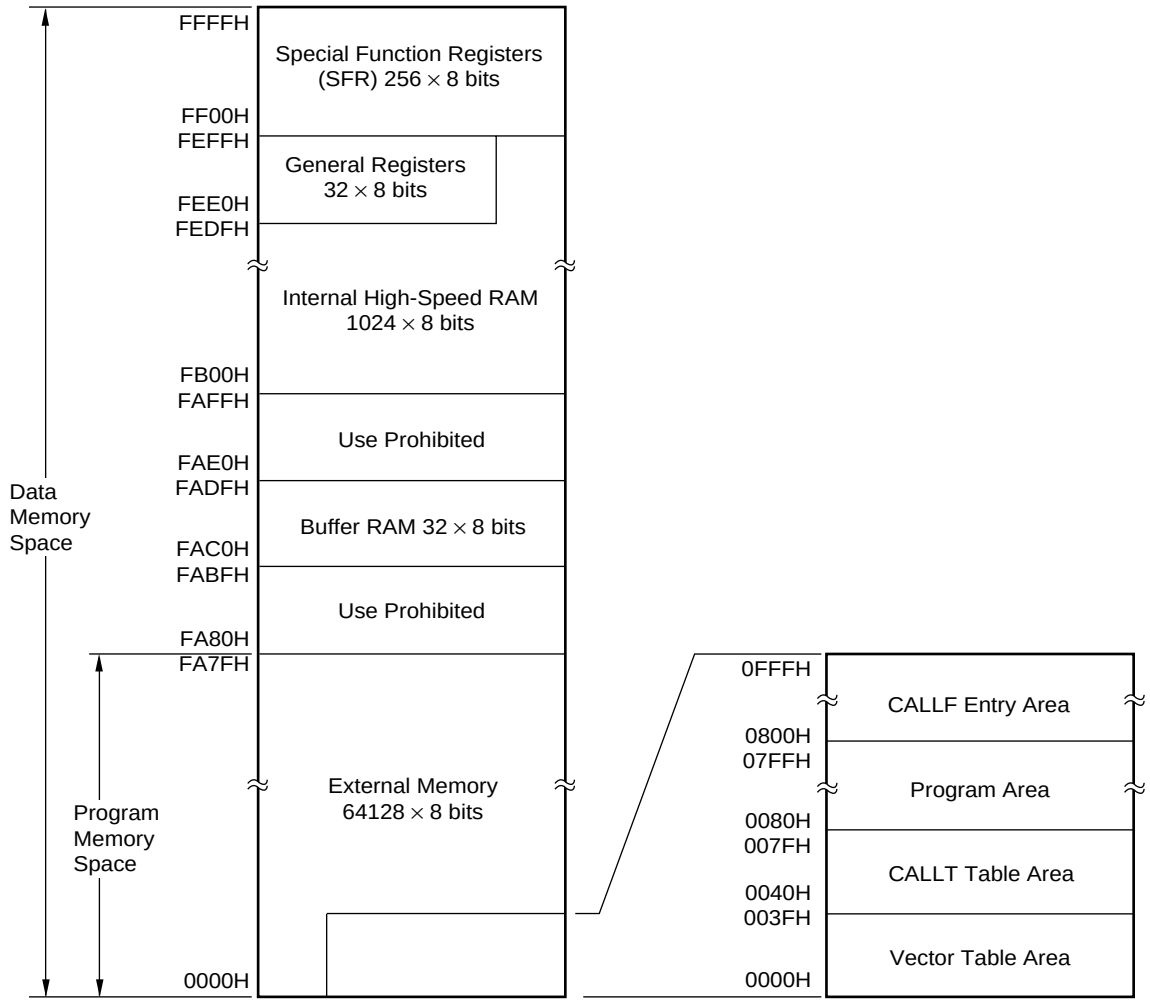
Figure 3-1. Pin Input/Output Circuits (2/2)



4. MEMORY SPACE

The memory map of the μPD78070AY is shown in Figure 4-1.

Figure 4-1. Memory Map



5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

Input/output ports are classified into three types.

- CMOS inputs (P00, P07) : 2
- CMOS input/outputs (P01 to P06, Port 1 to 3, P66, Port 7, P94 to P96, Port 10, Port 12, Port 13) : 51
- N-ch open-drain input/outputs (P60 to P63, P90 to P93) : 8

Total : 61

Table 5-1. Functions of Ports

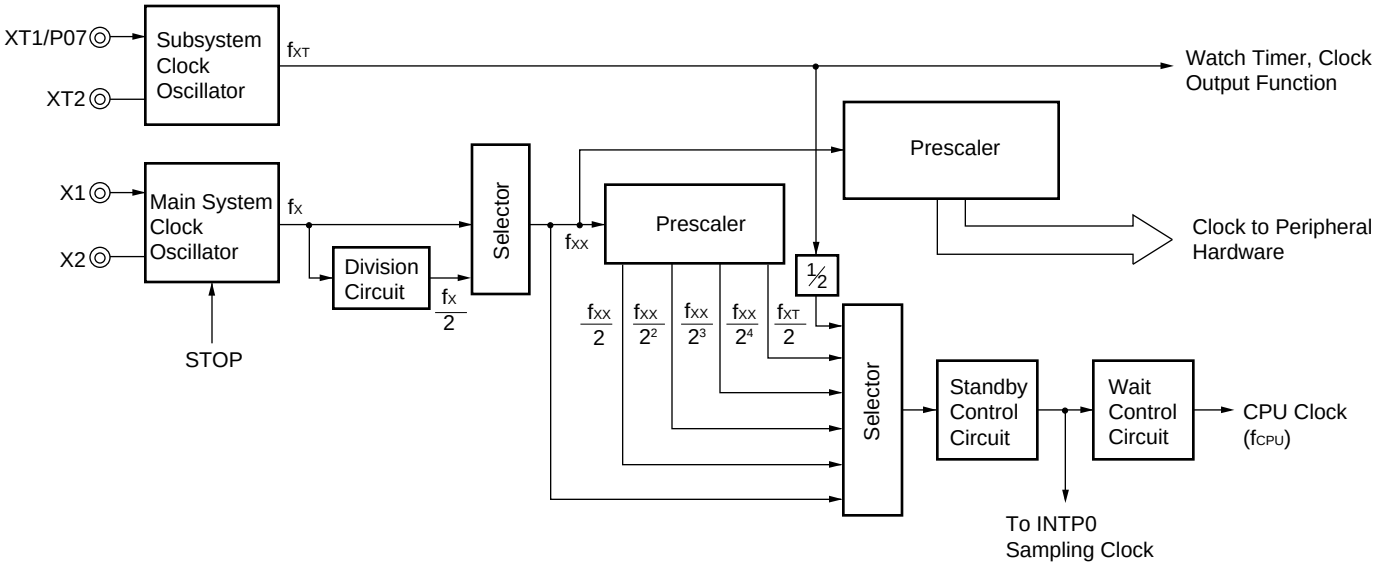
Port Name	Pin Name	Function
Port 0	P00, P07	Input only
	P01 to P06	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 1	P10 to P17	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 2	P20 to P27	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 3	P30 to P37	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 6	P60 to P63	N-ch open-drain input/output port. Input/output can be specified bit-wise. LED can be driven directly.
	P66	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 7	P70 to P72	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 9	P90 to P93	N-ch open-drain input/output port. Input/output can be specified bit-wise.
	P94 to P96	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 10	P100 to P103	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 12	P120 to P127	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.
Port 13	P130, P131	Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be connected by software.

5.2 Clock Generator

There are two kinds of clock generators: main system and subsystem clock generators. It is possible to change the minimum instruction execution time.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (at main system clock frequency of 5.0 MHz)
- 122 μs (at subsystem clock frequency of 32.768 kHz)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer/Event Counter

There are the following seven timer/event counter channels:

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 4 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2. Types and Functions of Timer/Event Counters

		16-bit Timer/ Event Counter	8-bit Timer/ Event Counter 1, 2	8-bit Timer/ Event Counter 5, 6	Watch Timer	Watchdog Timer
Type	Interval timer	1 channel	2 channels	2 channels	1 channel	1 channel
	External event counter	1 channel	2 channels	2 channels	—	—
Function	Timer output	1 output	2 outputs	2 outputs	—	—
	PWM output	1 output	—	2 outputs	—	—
	Pulse width measurement	2 inputs	—	—	—	—
	Square wave output	1 output	2 outputs	2 outputs	—	—
	One-shot pulse output	1 output	—	—	—	—
	Interrupt source	2	2	2	1	1
	Test input	—	—	—	1 input	—

Figure 5-2. 16-Bit Timer/Event Counter Block Diagram

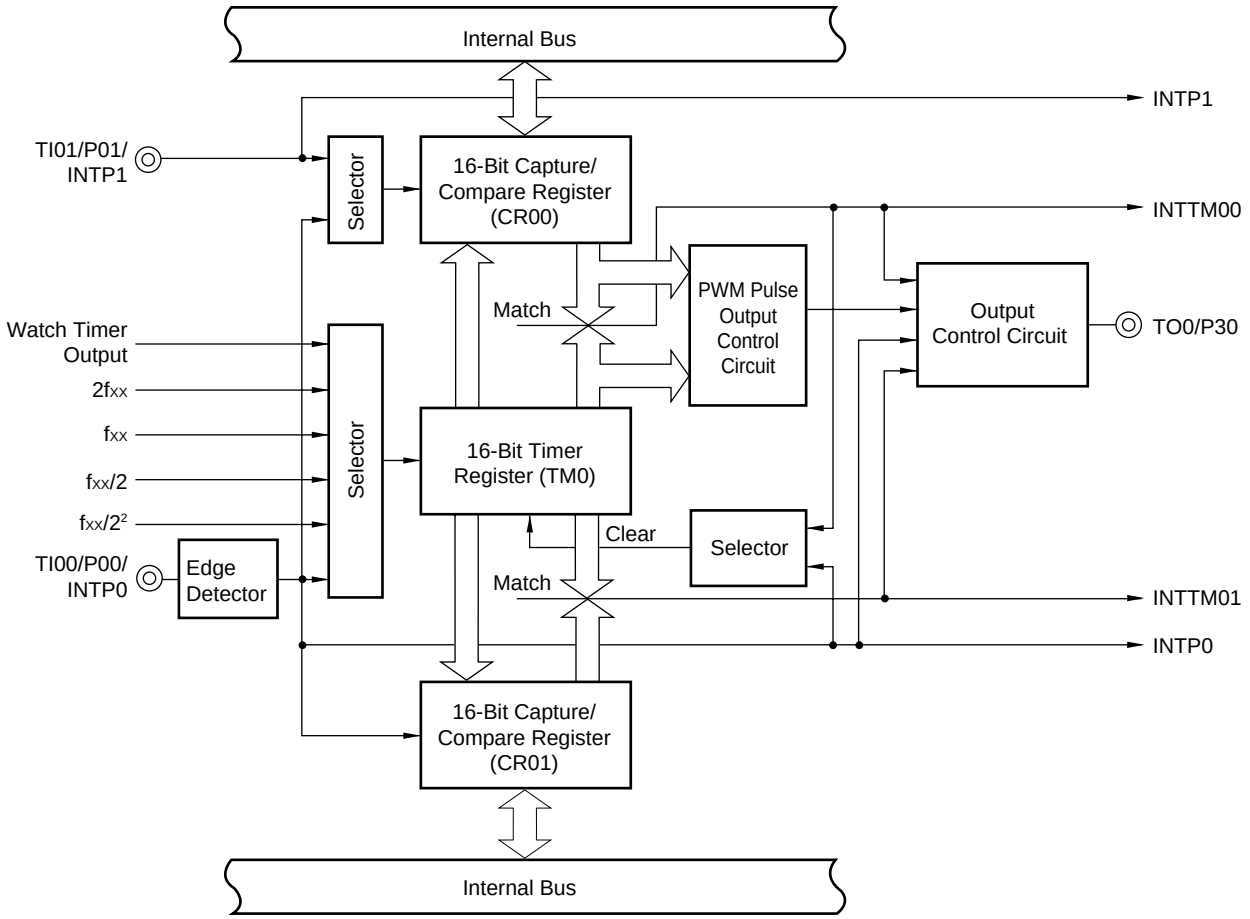


Figure 5-3. 8-Bit Timer/Event Counter 1, 2 Block Diagram

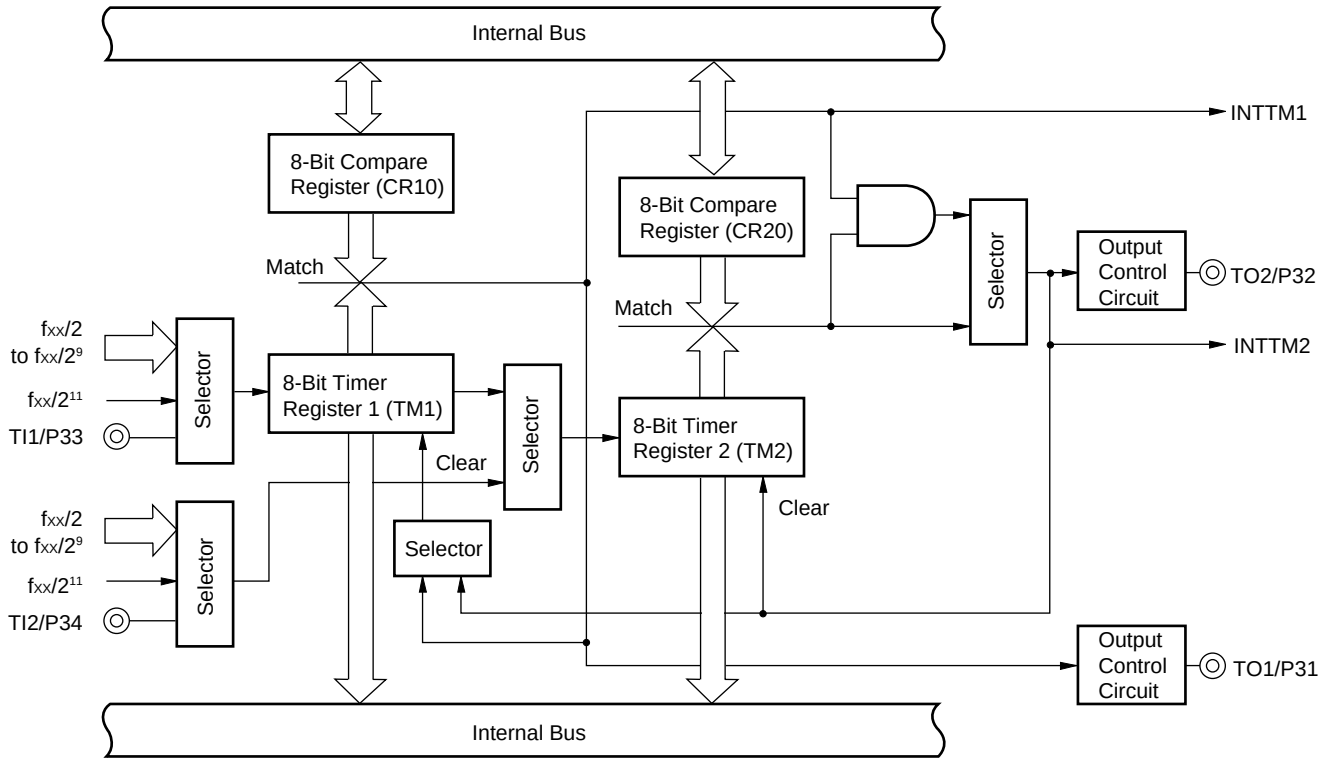
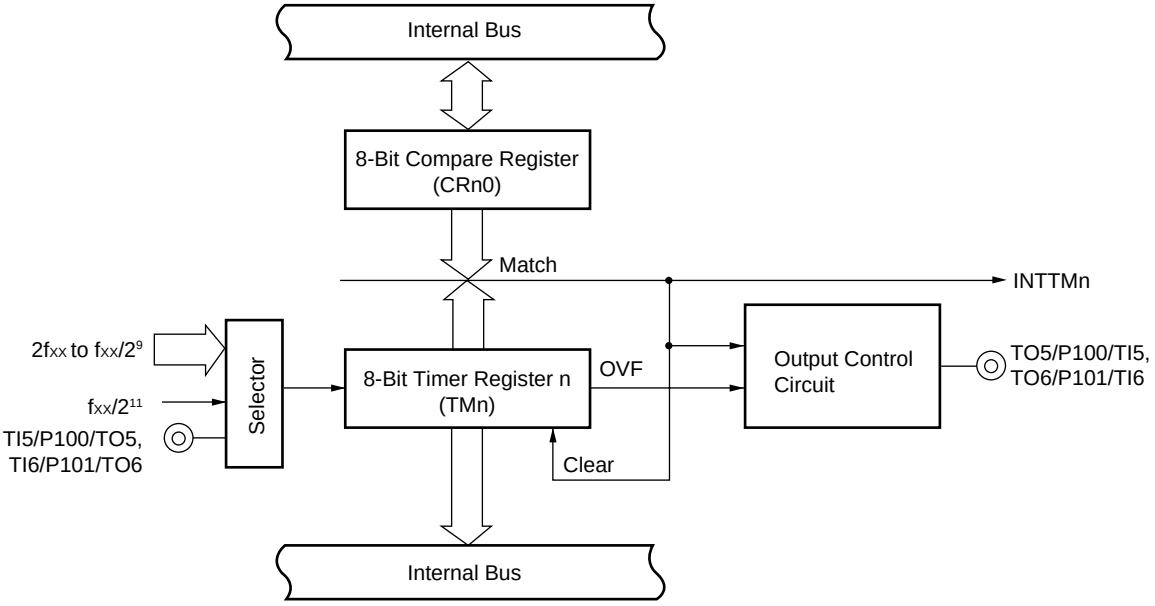


Figure 5-4. 8-Bit Timer/Event Counter 5, 6 Block Diagram



n = 5, 6

Figure 5-5. Watch Timer Block Diagram

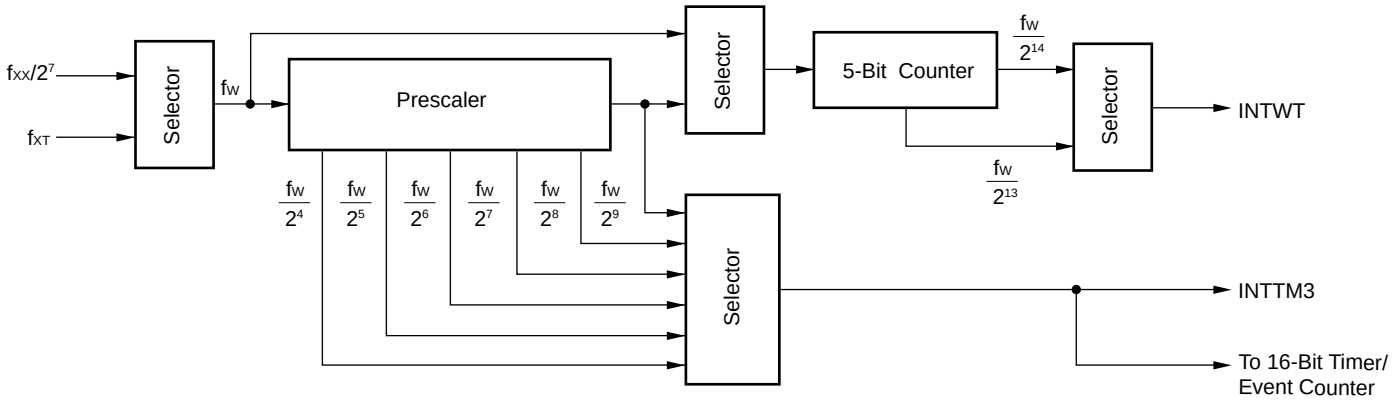
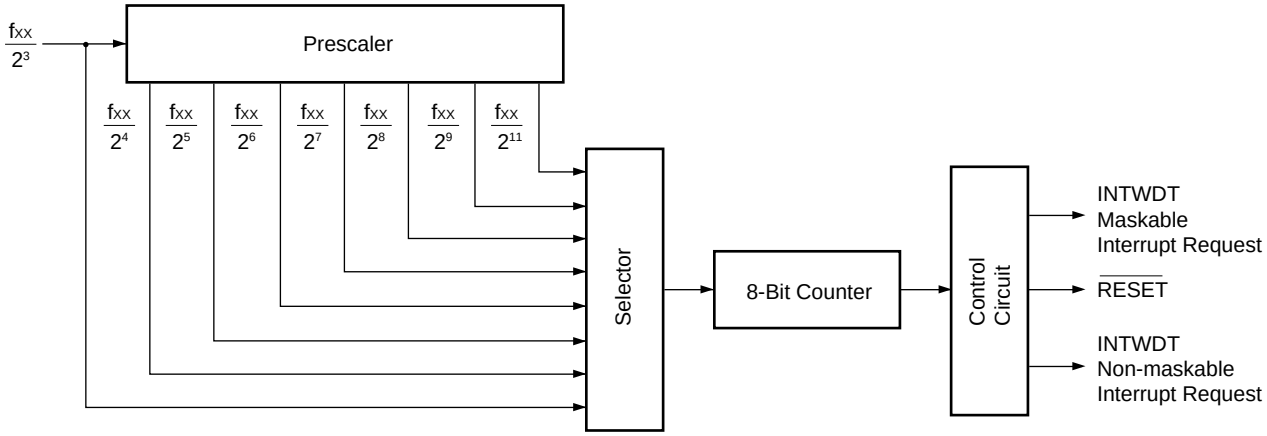


Figure 5-6. Watchdog Timer Block Diagram

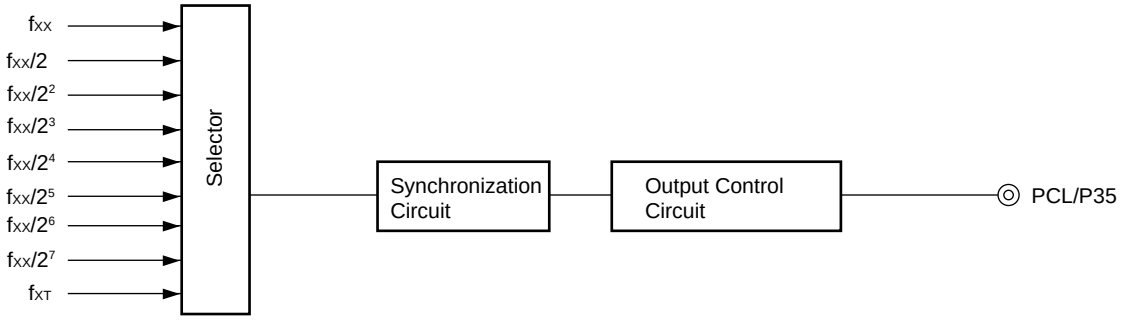


5.4 Clock Output Control Circuit

This circuit can output clocks of the following frequencies:

- 19.5 kHz/39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz/2.5 MHz/5.0 MHz (at main system clock frequency of 5.0 MHz)
- 32.768 kHz (at subsystem clock frequency of 32.768 kHz)

Figure 5-7. Clock Output Control Circuit Block Diagram

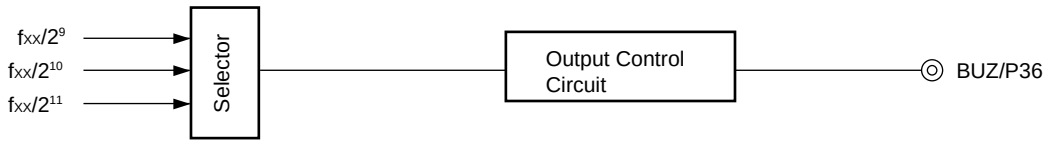


5.5 Buzzer Output Control Circuit

This circuit can output clocks of the following frequencies that can be used for driving buzzers:

- 1.2 kHz/2.4 kHz/4.9 kHz/9.8 kHz (at main system clock frequency of 5.0 MHz)

Figure 5-8. Buzzer Output Control Circuit Block Diagram



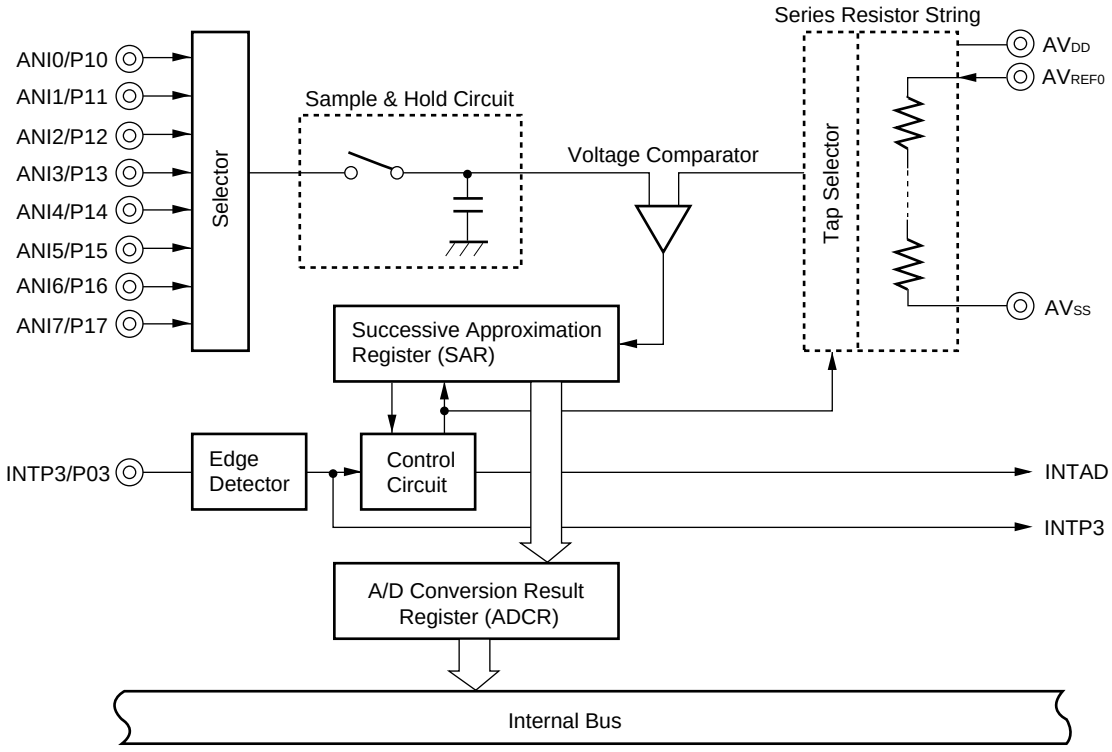
5.6 A/D Converter

The A/D converter consists of eight 8-bit resolution channels.

A/D conversion can be started by the following two methods:

- Hardware starting
- Software starting

Figure 5-9. A/D Converter Block Diagram

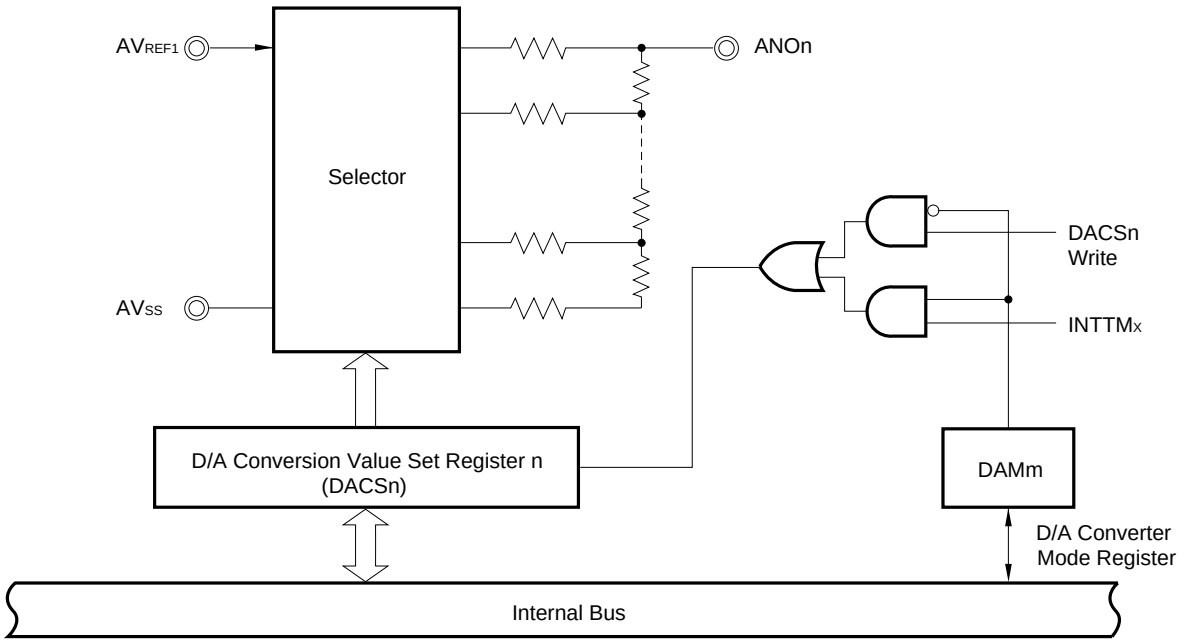


5.7 D/A Converter

The D/A converter consists of two 8-bit resolution channels.

The conversion method is the R-2R resistor ladder method.

Figure 5-10. D/A Converter Block Diagram



n = 0, 1
m = 4, 5
x = 1, 2

5.8 Serial Interfaces

There are the following three on-chip serial interface channels synchronous with the clock:

- Serial interface channel 0
- Serial interface channel 1
- Serial interface channel 2

Table 5-3. Types and Functions of Serial Interfaces

Function	Serial Interface Channel 0	Serial Interface Channel 1	Serial Interface Channel 2
3-wire serial I/O mode	√ (MSB/LSB first bit switching possible)	√ (MSB/LSB first bit switching possible)	√ (MSB/LSB first bit switching possible)
3-wire serial I/O mode with automatic data transmit/receive function	—	√ (MSB/LSB first bit switching possible)	—
2-wire serial I/O mode	√ (MSB first)	—	—
I^2C bus mode	√ (MSB first)	—	—
Asynchronous serial interface (UART) mode	—	—	√ (On-chip dedicated baud rate generator)

Figure 5-11. Serial Interface Channel 0 Block Diagram

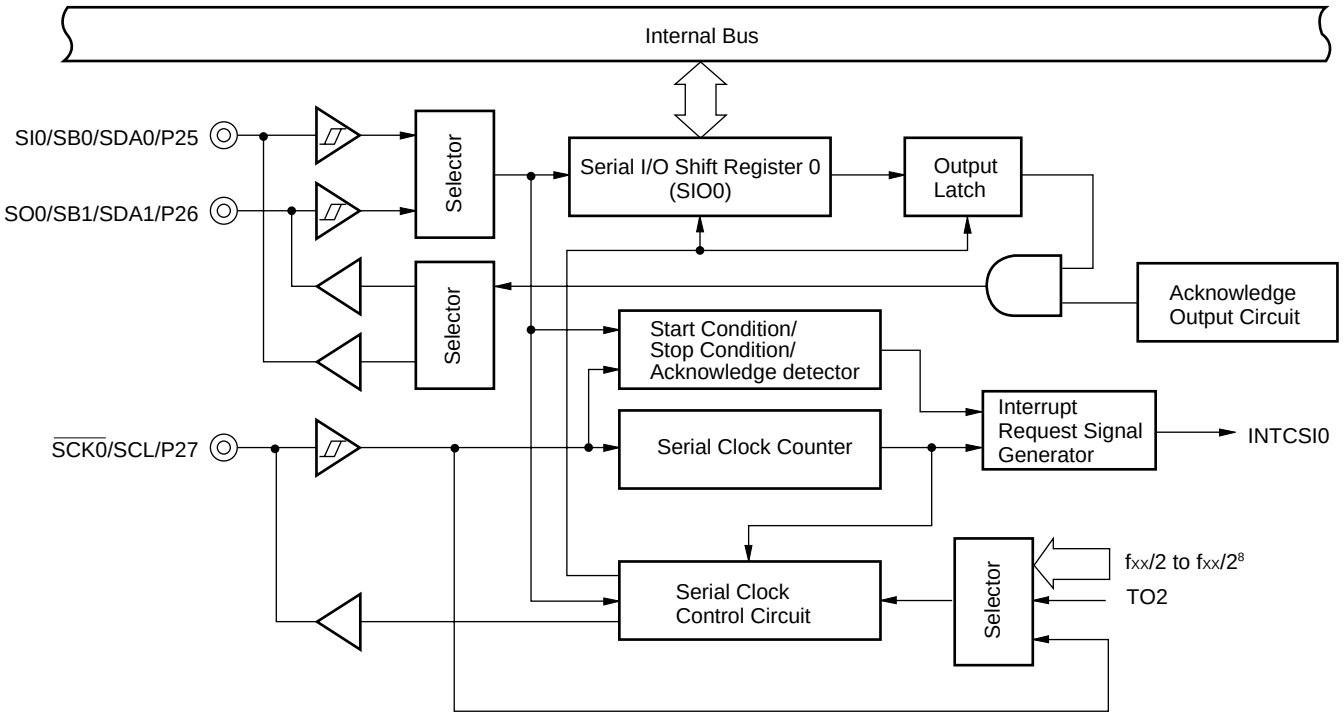


Figure 5-12. Serial Interface Channel 1 Block Diagram

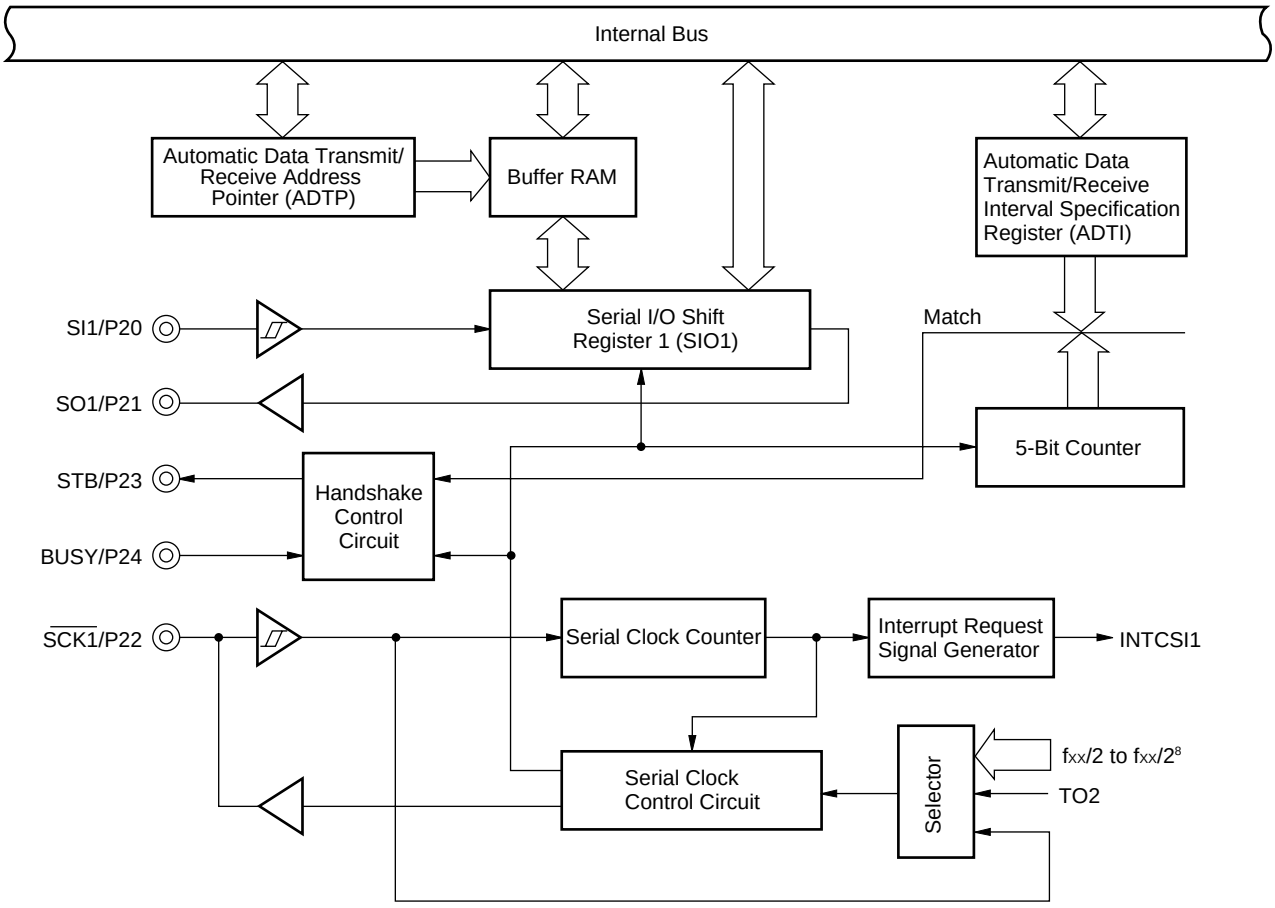
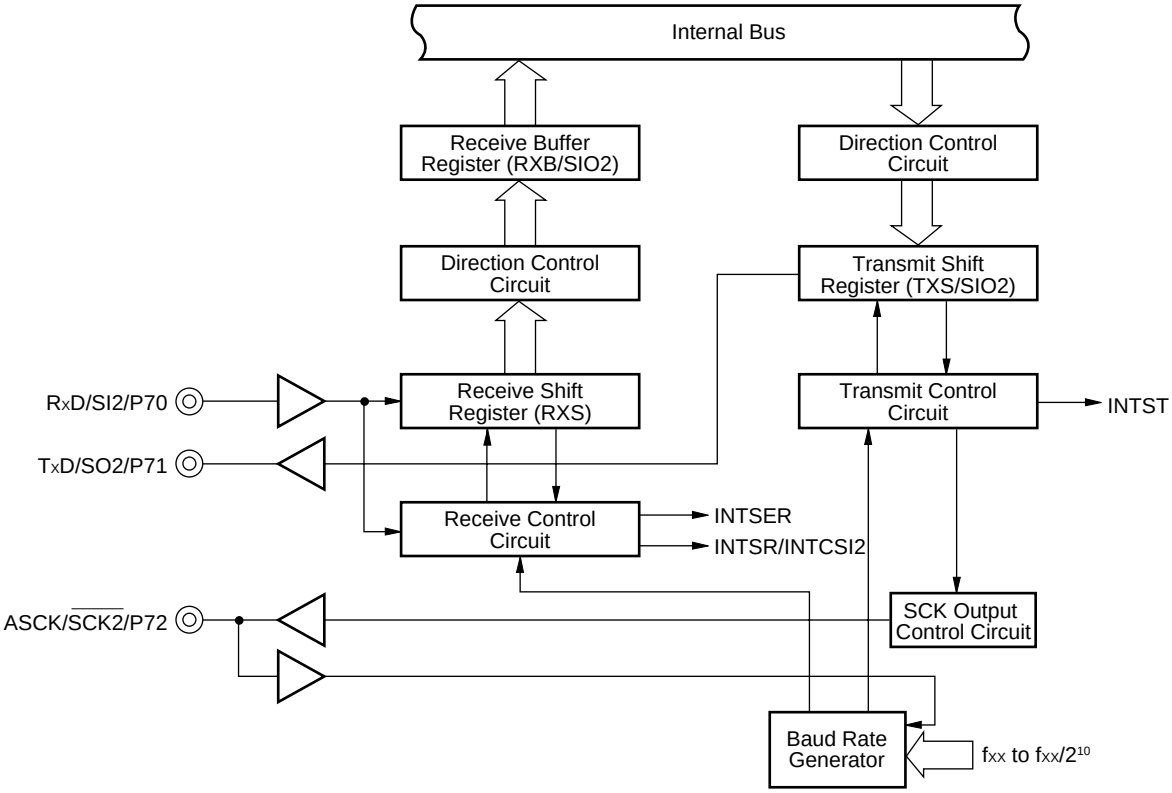


Figure 5-13. Serial Interface Channel 2 Block Diagram

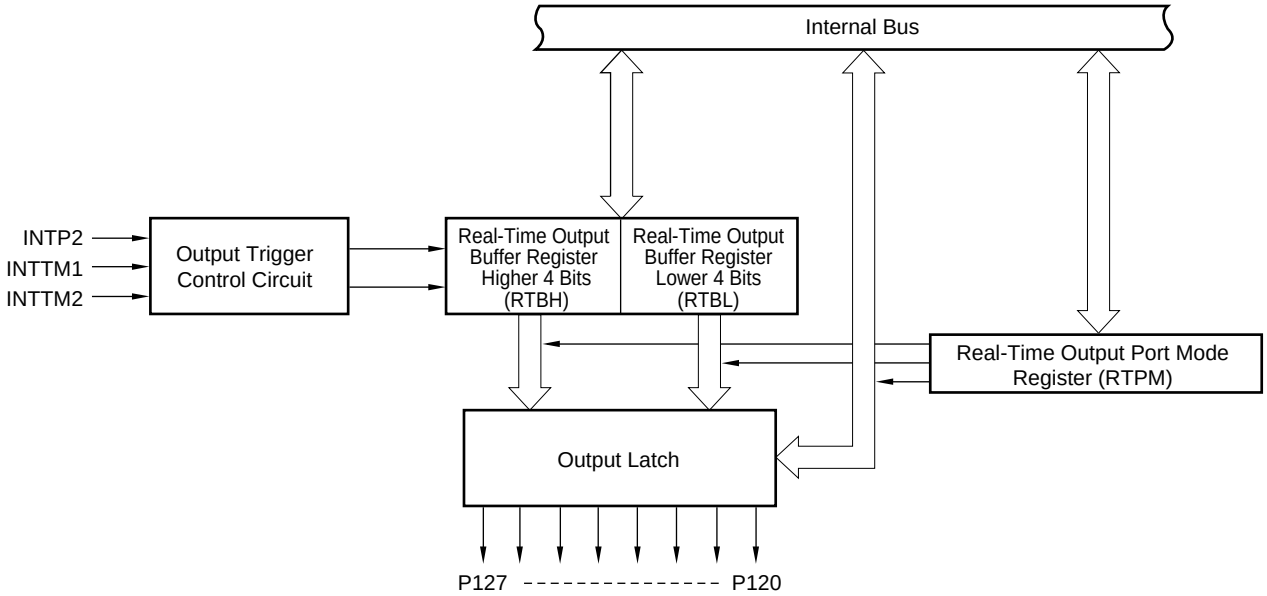


5.9 Real-Time Output Port

Data set previously in the real-time output buffer is transferred to the output latch by hardware concurrently with timer interrupt or external interrupt generation in order to output to off-chip. This is a real-time output function. Pins used to output to off-chip are called real-time output ports.

By using a real-time output port, a signal which has no jitter can be output. This is most applicable to control of stepping motors, etc.

Figure 5-14. Real-Time Output Port Block Diagram



6. INTERRUPT FUNCTIONS AND TEST FUNCTION

6.1 Interrupt Functions

A total of 24 interrupt soources are provided, divided into the following three types.

- Non-maskable : 1
- Maskable : 22
- Software : 1

Table 6-1. List of Interrupt Sources

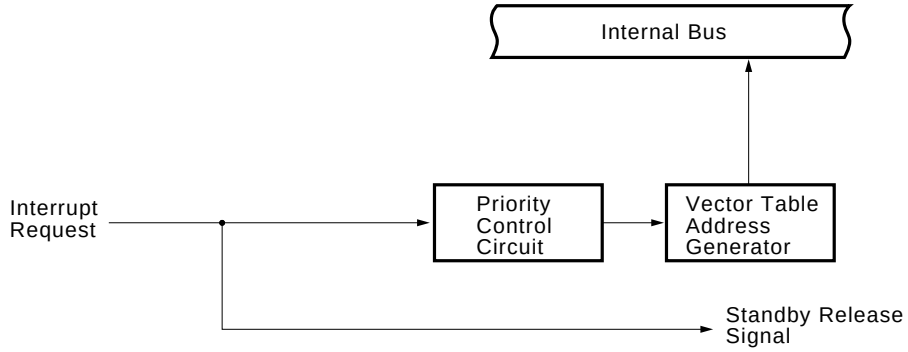
Interrupt Type	Default Priority[Note1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Structure Type[Note2]
		Name	Trigger			
Non-maskable	—	INTWDT	Overflow of watchdog timer (When the watchdog timer mode 1 is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Overflow of watchdog timer (When the interval timer mode is selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	(D)
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTP4			000EH	
	6	INTP5			0010H	
	7	INTP6			0012H	
	8	INTCSI0	Completion of serial interface channel 0 transfer	Internal	0014H	(B)
	9	INTCSI1	Completion of serial interface channel 1 transfer		0016H	
	10	INTSER	Occurrence of serial interface channel 2 UART reception error		0018H	
	11	INTSR	Completion of serial interface channel 2 UART reception		001AH	
		INTCSI2	Completion of serial interface channel 2 3-wire transfer			
	12	INTST	Completion of serial interface channel 2 UART transmission		001CH	
	13	INTTM3	Reference time interval signal from watch timer		001EH	
	14	INTTM00	Generation of matching signal of 16-bit timer register and capture/compare register (CR00)		0020H	
	15	INTTM01	Generation of matching signal of 16-bit timer register and capture/compare register (CR01)		0022H	
	16	INTTM1	Generation of matching signal of 8-bit timer/event counter 1		0024H	
	17	INTTM2	Generation of matching signal of 8-bit timer/event counter 2		0026H	
	18	INTAD	Completion of A/D conversion		0028H	
	19	INTTM5	Generation of matching signal of 8-bit timer/event counter 5		002AH	
	20	INTTM6	Generation of matching signal of 8-bit timer/event counter 6		002CH	
Software	—	BRK	Execution of BRK instruction	—	003EH	(E)

Notes 1. Default priority is the priority order when several maskable interrupt requests are generated at the same time. 0 is the highest priority and 20 is the lowest priority.

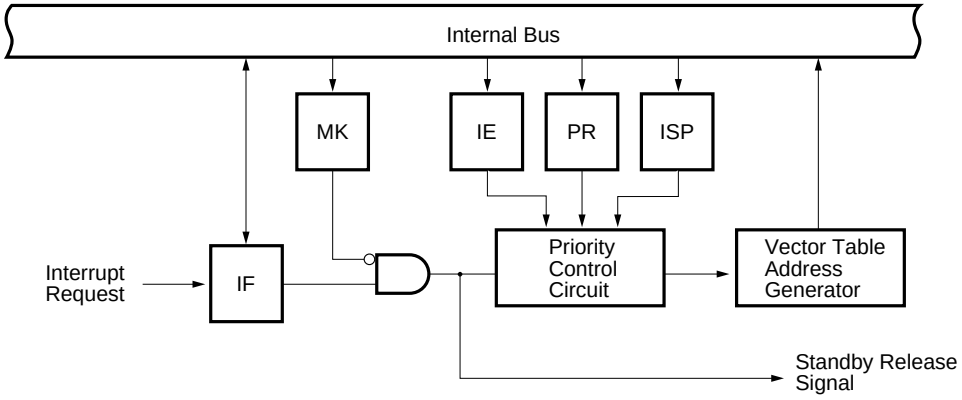
2. Basic structure types (A) to (E) correspond to (A) to (E) in Figure 6-1.

Figure 6-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0)

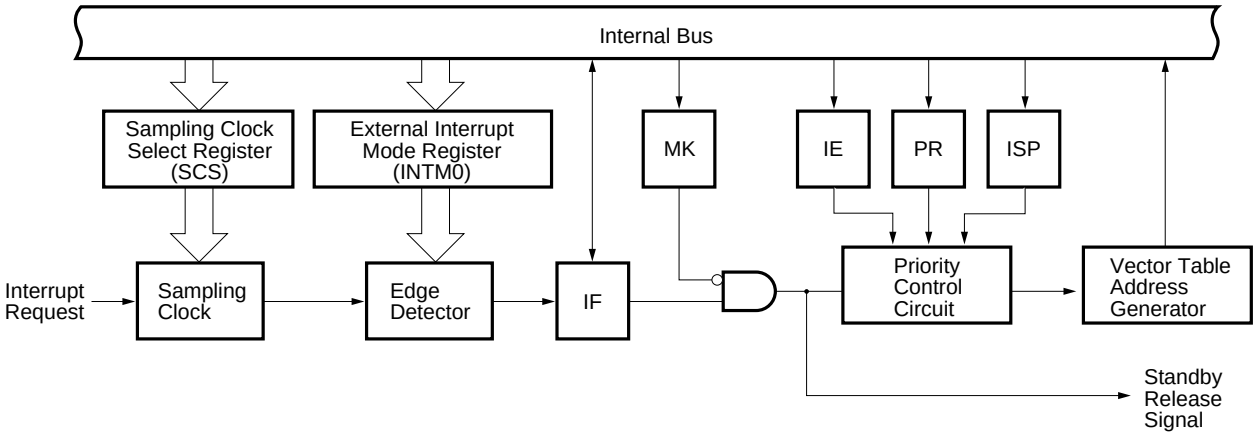
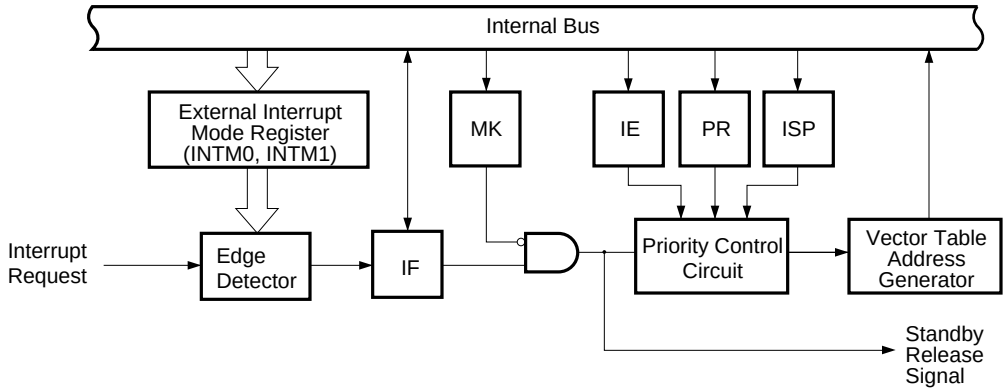
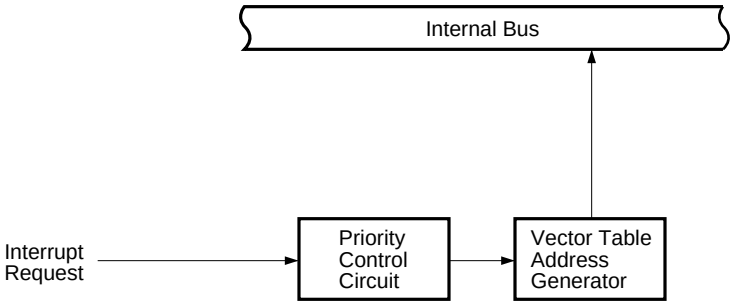


Figure 6-1. Basic Configuration of Interrupt Function (2/2)

(D) External maskable interrupt (except INTP0)



(E) Software interrupt



IF : Interrupt request flag
IE : Interrupt enable flag
ISP : In-service priority flag
MK : Interrupt mask flag
PR : Priority specification flag

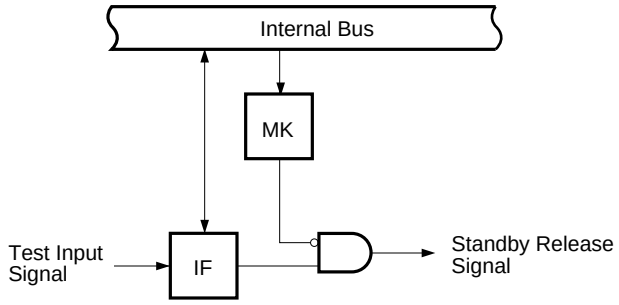
6.2 Test Function

Table 6-2 shows the test function available.

Table 6-2. Test Input Source

Test Input Source		Internal/ External
Name	Trigger	
INTWT	Overflow of watch timer	Internal

Figure 6-2. Basic Configuration of Test Function



IF : Test input flag

MK : Test mask flag

7. EXTERNAL DEVICE EXPANSION FUNCTIONS

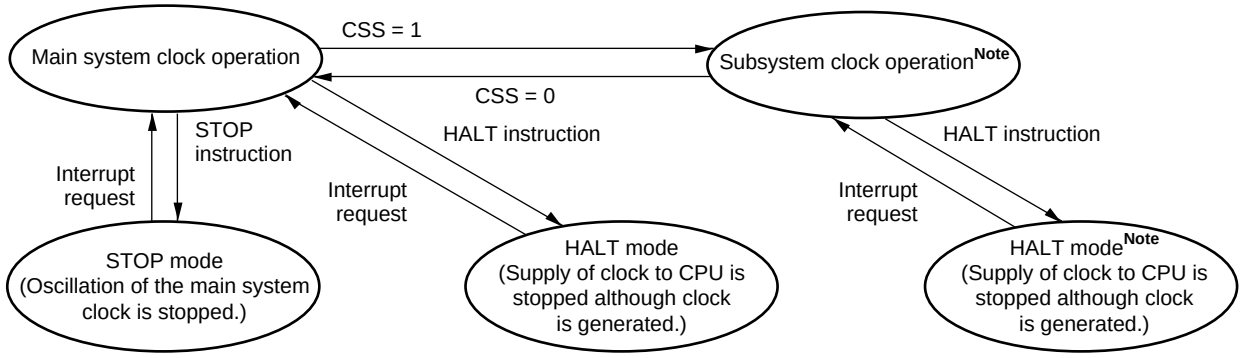
The external device expansion functions connect external devices to areas other than the RAM and SFR. The μPD78070AY is a ROM-less product, and therefore requires the connection of external ROM. Connect external devices using an independent address bus and data bus.

8. STANDBY FUNCTION

The standby function is designed to reduce current consumption.
It has the following two modes:

- HALT mode : In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.
- STOP mode : In this mode, oscillation of the main system clock is stopped. All the operations performed on the main system clock are suspended, and only the subsystem clock is used for extremely small power consumption.

Figure 8-1. Standby Function



Note Current consumption is reduced by shutting off the main system clock. If the CPU is operating on the subsystem clock, shut off the main system clock by setting bit 7 (MCC) of the processor clock control register (PCC). You cannot use a STOP instruction.

Caution When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

9. RESET FUNCTION

There are the following two reset methods.

- External reset input by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer runaway time detection

10. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

2nd Operand / 1st Operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											

Note Except r = A

2nd Operand / 1st Operand	#byte	A	r	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

2nd Operand / 1st Operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

2nd Operand / 1st Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instruction/Branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

2nd Operand / 1st Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL	CALLF BR	CALLT	BR, BC, BNC, BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

11. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Test Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
	AV_{DD}			–0.3 to V_{DD} + 0.3	V
	AV_{REF0}			–0.3 to V_{DD} + 0.3	V
	AV_{REF1}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P66, P70 to P72, P94 to P96, P100 to P103, P120 to P127, P130, P131, AD0 to AD7, X1, X2, XT2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P60 to P63, P90 to P93	N-ch open-drain	–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pins	AV_{SS} – 0.3 to AV_{REF0} + 0.3	V
Output current, high	I_{OH}	Per pin		–10	mA
		Total for P30 to P37, P60 to P63, P66, P90 to P96, P100 to P103, P120 to P127, A14, A15, $\overline{\text{RD}}$, $\overline{\text{WR}}$, ASTB		–15	mA
		Total for P01 to P06, P10 to P17, P20 to P27, P70 to P72, P130, P131, AD0 to AD7, A0 to A13		–15	mA
Output current, low	I_{OL} Note	Per pin	Peak value	30	mA
			r.m.s. value	15	mA
		Total for A8 to A13	Peak value	50	mA
			r.m.s. value	20	mA
		Total for P60 to P63, A14, A15	Peak value	100	mA
			r.m.s. value	70	mA
		Total for P30 to P37, P66, P90 to P96, P100 to P103, P120 to P127, $\overline{\text{RD}}$, $\overline{\text{WR}}$, ASTB	Peak value	50	mA
			r.m.s. value	20	mA
		Total for P20 to P27, AD0 to AD7, A0 to A7	Peak value	50	mA
			r.m.s. value	20	mA
		Total for P01 to P06, P10 to P17, P70 to P72, P130, P131	Peak value	50	mA
			r.m.s. value	20	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note The r.m.s. value should be calculated as follows: [r.m.s. value] = [Peak value] $\times\sqrt{\text{Duty}}$

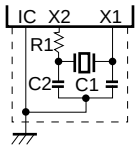
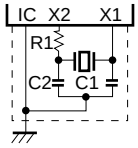
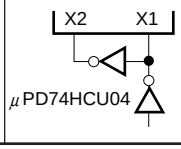
Caution Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.

Remark Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

CAPACITANCE (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz, Unmeasured pins returned to 0 V.			15	pF
Output capacitance	C_{OUT}				15	pF
I/O capacitance	C_{IO}				15	pF

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X) Note 1	V_{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization time Note 2	After V_{DD} came to MIN. of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f_X) Note 1		1.0		5.0	MHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X) Note 1		1.0		5.0	MHz
		X1 input high- and low-level widths (t_{XH}, t_{XL})		85		500	ns

Notes 1. Only the oscillator characteristics are shown. For the instruction execution time, refer to **AC Characteristics**.

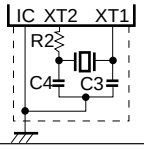
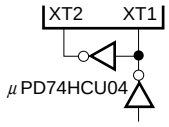
2. Time required for oscillation to stabilize after a reset or the STOP mode has been released.

Cautions 1. When using the oscillation circuit of the main system clock, wire the portion enclosed in dotted lines in the figures as follows to avoid adverse influences on the wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring over other signal lines.**
- **Do not route the wiring in the vicinity of lines through which a high fluctuating current flows.**
- **Always keep the ground point of the capacitor of the oscillation circuit at the same potential as V_{SS}.**
- **Do not connect the power source to a ground pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT}) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT}) Note 1		32		100	kHz
		XT1 input high-, low-level widths (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Only the oscillator characteristics are shown. For the instruction execution time, refer to **AC Characteristics**.

2. Time required for oscillation to stabilize after V_{DD} reaches the minimum value of the oscillation voltage range.

Cautions 1. When using the oscillation circuit of the subsystem clock, wire the portion enclosed in dotted lines in the figures as follows to avoid adverse influences on the wiring capacitance:

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring over other signal lines.**
- **Do not route the wiring in the vicinity of lines through which a high fluctuating current flows.**
- **Always keep the ground point of the capacitor of the oscillation circuit at the same potential as V_{SS}.**
- **Do not connect the power source pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

2. The amplification factor of the subsystem clock oscillator is designed to be low to reduce the current consumption and therefore, the subsystem clock oscillator is influenced by noise more easily than the main system clock oscillator. When using the subsystem clock, therefore, exercise utmost care in wiring the circuit.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P66, P71, P94 to P96, P102, P103, P120 to P127, P130, P131, AD0 to AD7		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, P100, P101, $\overline{RESET}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	P60 to P63, P90 to P93 (N-ch open-drain)		0.7V_{DD}		V_{DD}	V
	V_{IH4}	X1, X2		V_{DD} – 0.5		V_{DD}	V
	V_{IH5}	XT1/P07, XT2	V_{DD} = 4.5 to 5.5 V	0.8V_{DD}		V_{DD}	V
				0.9V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P66, P71, P94 to P96, P102, P103, P120 to P127, P130, P131, AD0 to AD7		0		0.3V_{DD}	V
	V_{IL2}	P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, P100, P101, $\overline{RESET}$		0		0.2V_{DD}	V
	V_{IL3}	P60 to P63, P90 to P93 (N-ch open-drain)	V_{DD} = 4.5 to 5.5 V	0		0.3V_{DD}	V
				0		0.2V_{DD}	V
	V_{IL4}	X1, X2		0		0.4	V
	V_{IL5}	XT1/P07, XT2	V_{DD} = 4.5 to 5.5 V	0		0.2V_{DD}	V
				0		0.1V_{DD}	V
Output voltage, high	V_{OH}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD} – 1.0			V
		I_{OH} = –100 μA		V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P60 to P63	V_{DD} = 4.5 to 5.5 V, I_{OL} = 15 mA		0.4	2.0	V
		P01 to P06, P10 to P17, P20 to P27, P30 to P37, P66, P70 to P72, P90 to P96, P100 to P103, P120 to P127, P130, P131, AD0 to AD7, A0 to A15, $\overline{RD}$, $\overline{WR}$, ASTB	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{SCK0}$	V_{DD} = 4.5 to 5.5 V, Open-drain, pulled up (R = 1 kΩ)			0.2V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V

Remark Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P60 to P63, P66, P70 to P72, P90 to P96, P100 to P103, P120 to P127, P130, P131, AD0 to AD7, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2, XT1/P07, XT2			20	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00 to P06, P10 to P17, P20 to P27, P30 to P37, P60 to P63, P66, P70 to P72, P90 to P96, P100 to P103, P120 to P127, P130, P131, AD0 to AD7, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2, XT1/P07, XT2			–20	μA
Output leakage current, high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA

Remark Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Software pull-up resistor	R	V_{IN} = 0 V, P01 to P06, P10 to P17, P20 to P27, P30 to P37, P66, P70 to P72, P94 to P96, P100 to P103, P120 to P127, P130, P131	V_{DD} = 4.5 to 5.5 V	15	40	90	kΩ
				20		500	kΩ
Supply current[Note 1]	I_{DD1}	5.0-MHz crystal oscillation operating mode (f_{XX} = 2.5 MHz)[Note 2]	V_{DD} = 5.0 V ±10%[Note 5]		4.5	13.5	mA
			V_{DD} = 3.0 V ±10%[Note 6]		0.7	2.1	mA
		5.0-MHz crystal oscillation operating mode (f_{XX} = 5.0 MHz)[Note 3]	V_{DD} = 5.0 V ±10%[Note 5]		8.0	24.0	mA
			V_{DD} = 3.0 V ±10%[Note 6]		0.9	2.7	mA
	I_{DD2}	5.0-MHz crystal oscillation HALT mode (f_{XX} = 2.5 MHz)[Note 2]	V_{DD} = 5.0 V ±10%[Note 5]		1.4	4.2	mA
			V_{DD} = 3.0 V ±10%[Note 6]		0.5	1.5	mA
		5.0-MHz crystal oscillation HALT mode (f_{XX} = 5.0 MHz)[Note 3]	V_{DD} = 5.0 V ±10%[Note 5]		1.6	4.8	mA
			V_{DD} = 3.0 V ±10%[Note 6]		0.65	1.95	mA
	I_{DD3}	32.768-kHz crystal oscillation operating mode[Note 4]	V_{DD} = 5.0 V ±10%		60	120	μA
			V_{DD} = 3.0 V ±10%		32	64	μA
	I_{DD4}	32.768-kHz crystal oscillation operating mode[Note 4]	V_{DD} = 5.0 V ±10%		25	55	μA
			V_{DD} = 3.0 V ±10%		5	15	μA
	I_{DD5}	XT1 = V_{DD} STOP mode Feedback resistor used	V_{DD} = 5.0 V ±10%		1	30	μA
			V_{DD} = 3.0 V ±10%		0.5	10	μA
	I_{DD6}	XT1 = V_{DD} STOP mode Feedback resistor not used	V_{DD} = 5.0 V ±10%		0.1	30	μA
			V_{DD} = 3.0 V ±10%		0.05	10	μA

Notes 1. Current flowing into the V_{DD} pin. Not including the current flowing into an A/D converter, D/A converter, nor on-chip pull-up resistor.

2. f_{XX} = f_X/2 operation (when oscillation mode selection register (OSMS) is set to 00H).

3. f_{XX} = f_X operation (when OSMS is set to 01H).

4. When the main system clock is stopped.

5. High-speed mode operation (when processor clock control register (PCC) is set to 00H).

6. Low-speed mode operation (when PCC is set to 04H).

Remarks 1. Unless otherwise specified, dual-function pin characteristics are the same as port pin characteristics.

2. f_{XX} : Main system clock frequency (f_X or f_X/2)

3. f_X : Main system clock oscillation frequency

AC CHARACTERISTICS

(1) Basic Operation (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions			MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operating on main system clock	$f_{XX} = f_X/2$ Note 1		0.8		64	μs
			$f_{XX} = f_X$ Note 2	V_{DD} = 3.5 to 5.5 V	0.4		32	μs
					0.8		32	μs
		Operating on subsystem clock			40	122	125	μs
TI00 input high-/low-level widths	t_{TIH00}, t_{TIL00}	V_{DD} = 3.5 to 5.5 V			$2/f_{sam}$ + 0.1 Note 3			μs
					$2/f_{sam}$ + 0.2 Note 3			μs
TI01 input high-/low-level widths	t_{TIH01}, t_{TIL01}				10			μs
TI1, TI2, TI5, TI6 input frequency	f_{TI1}	V_{DD} = 4.5 to 5.5 V			0		4	MHz
					0		275	kHz
TI1, TI2, TI5, TI6 input high-/low-level widths	t_{TIH1}, t_{TIL1}	V_{DD} = 4.5 to 5.5 V			100			ns
					1.8			μs
Interrupt request input high-/low-level widths	t_{INTH}, t_{INTL}	INTP0		V_{DD} = 3.5 to 5.5 V	$2/f_{sam}$ + 0.1 Note 3			μs
					$2/f_{sam}$ + 0.2 Note 3			μs
		INTP1 to INTP6			10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			μs

Notes 1. When oscillation mode selection register (OSMS) is set to 00H

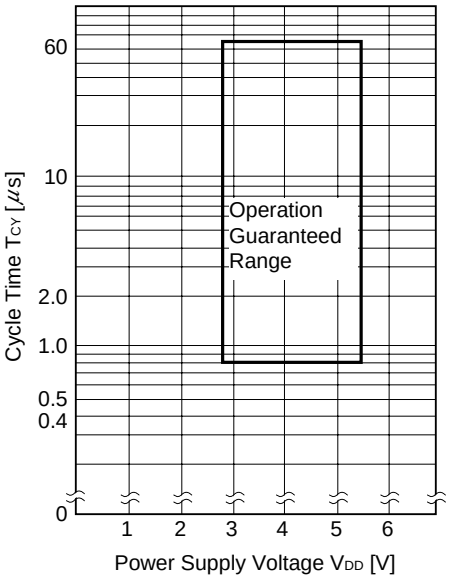
2. When OSMS is set to 01H

3. fsam can be selected as $f_{XX}/2^N$, $f_{XX}/32$, $f_{XX}/64$ or $f_{XX}/128$ (N = 0 to 4) by bits 0 and 1 (SCS0, SCS1) of the sampling clock selection register.

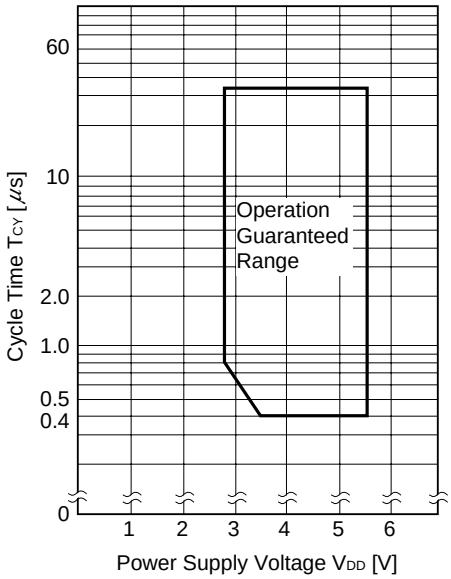
Remark f_{XX} : Main system clock frequency (f_X or $f_X/2$)

f_X : Main system clock oscillation frequency

T_{CY} vs V_{DD}
(Main System Clock $f_{XX} = f_X/2$ Operation)



T_{CY} vs V_{DD}
(Main System Clock $f_{XX} = f_X$ Operation)



(2) Read/Write Operation

(a) When MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.85t_{CY}$ – 50		ns
Address setup time	t_{ADS}		$0.85t_{CY}$ – 50		ns
Address hold time	t_{ADH}		50		ns
Address → Data input time	t_{ADD1}			$(2.85 + 2n)\ t_{CY}$ – 80	ns
	t_{ADD2}			$(4 + 2n)\ t_{CY}$ – 100	ns
$\overline{RD}$ ↓ → Data input time	t_{RDD1}			$(2 + 2n)\ t_{CY}$ – 100	ns
	t_{RDD2}			$(2.85 + 2n)\ t_{CY}$ – 100	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(2 + 2n)\ t_{CY}$ – 60		ns
	t_{RDL2}		$(2.85 + 2n)\ t_{CY}$ – 60		ns
$\overline{RD}$ ↓ → $\overline{WAIT}$ ↓ input time	t_{RDWT1}			$0.85t_{CY}$ – 50	ns
	t_{RDWT2}			$2t_{CY}$ – 60	ns
$\overline{WR}$ ↓ → $\overline{WAIT}$ ↓ input time	t_{WRWT}			$2t_{CY}$ – 60	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(1.15 + 2n)\ t_{CY}$	$(2 + 2n)\ t_{CY}$	ns
Write data setup time	t_{WDS}		$(2.85 + 2n)\ t_{CY}$ – 100		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL}		$(2.85 + 2n)\ t_{CY}$ – 60		ns
ASTB ↓ → $\overline{RD}$ ↓ delay time	t_{ASTRD}		25		ns
ASTB ↓ → $\overline{WR}$ ↓ delay time	t_{ASTWR}		$0.85t_{CY}$ + 20		ns
In external fetch $\overline{RD}$ ↑ → ASTB ↑ delay time	t_{RDAST}		$0.85t_{CY}$ – 10	$1.15t_{CY}$ + 20	ns
In external fetch $\overline{RD}$ ↑ → address hold time	t_{RDADH}		$0.85t_{CY}$ – 50	$1.15t_{CY}$ + 50	ns
$\overline{RD}$ ↑ → write data output time	t_{RDWD}		40		ns
$\overline{WR}$ ↓ → write data output time	t_{WRWD}		0	50	ns
$\overline{WR}$ ↑ → address hold time	t_{WRADH}		$0.85t_{CY}$	$1.15t_{CY}$ + 40	ns
$\overline{WAIT}$↑ → $\overline{RD}$ ↑ delay time	t_{WTRD}		$1.15t_{CY}$ + 40	$3.15t_{CY}$ + 40	ns
$\overline{WAIT}$↑ → $\overline{WR}$ ↑ delay time	t_{WTWR}		$1.15t_{CY}$ + 30	$3.15t_{CY}$ + 30	ns

Remarks 1. MCS: Bit 0 of the oscillation mode selection register (OSMS)

2. PCC2 to PCC0: Bit 2 to bit 0 of the processor clock control register (PCC)

3. $t_{CY} = T_{CY}/4$

4. n indicates the number of waits.

(b) Except When MCS = 1, PCC2 to PCC0 = 000B (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		t_{CY} – 80		ns
Address setup time	t_{ADS}		t_{CY} – 80		ns
Address hold time	t_{ADH}		0.4t_{CY} – 10		ns
Address → Data input time	t_{ADD1}			(3 + 2n) t_{CY} – 160	ns
	t_{ADD2}			(4 + 2n) t_{CY} – 200	ns
$\overline{RD}$ ↓ → Data input time	t_{RDD1}			(1.4 + 2n) t_{CY} – 70	ns
	t_{RDD2}			(2.4 + 2n) t_{CY} – 70	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		(1.4 + 2n) t_{CY} – 20		ns
	t_{RDL2}		(2.4 + 2n) t_{CY} – 20		ns
$\overline{RD}$ ↓ → $\overline{WAIT}$ ↓ input time	t_{RDWT1}			t_{CY} – 100	ns
	t_{RDWT2}			2t_{CY} – 100	ns
$\overline{WR}$ ↓ → $\overline{WAIT}$ ↓ input time	t_{WRWT}			2t_{CY} – 100	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(1 + 2n) t_{CY}	(2 + 2n) t_{CY}	ns
Write data setup time	t_{WDS}		(2.4 + 2n) t_{CY} – 60		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL}		(2.4 + 2n) t_{CY} – 20		ns
ASTB ↓ → $\overline{RD}$ ↓ delay time	t_{ASTRD}		0.4t_{CY} – 30		ns
ASTB ↓ → $\overline{WR}$ ↓ delay time	t_{ASTWR}		1.4t_{CY} – 30		ns
In external fetch $\overline{RD}$ ↑ → ASTB ↑ delay time	t_{RDAST}		t_{CY} – 10	t_{CY} + 20	ns
In external fetch $\overline{RD}$ ↑ → address hold time	t_{RDADH}		t_{CY} – 50	t_{CY} + 50	ns
$\overline{RD}$ ↑ → write data output time	t_{RDWD}		0.4t_{CY} – 20		ns
$\overline{WR}$ ↓ → write data output time	t_{WRWD}		0	60	ns
$\overline{WR}$ ↑ → address hold time	t_{WRADH}		t_{CY}	t_{CY} + 60	ns
$\overline{WAIT}$↑ → $\overline{RD}$ ↑ delay time	t_{WTRD}		0.6t_{CY} + 180	2.6t_{CY} + 180	ns
$\overline{WAIT}$↑ → $\overline{WR}$ ↑ delay time	t_{WTWR}		0.6t_{CY} + 120	2.6t_{CY} + 120	ns

Remarks 1. MCS: Bit 0 of the oscillation mode selection register (OSMS)

2. PCC2-PCC0: Bit 2 to bit 0 of the processor clock control register (PCC)

3. $t_{CY} = T_{CY}/4$

4. n indicates the number of waits.

(3) Serial Interface (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

(a) Serial Interface Channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$ ··· internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK0}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 4.5 to 5.5 V	t_{KCY1}/2 – 50			ns
			t_{KCY1}/2 – 100			ns
SI0 setup time (to $\overline{SCK0}$ ↑)	t_{SIK1}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI0 hold time (from $\overline{SCK0}$ ↑)	t_{KSI1}		400			ns
$\overline{SCK0}$ ↓ → SO0 output delay time	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the $\overline{SCK0}$, SO0 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$ ··· external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK0}$ high-/low-level width	t_{KH2},	V_{DD} = 4.5 to 5.5 V	400			ns
	t_{KL2}		800			ns
SI0 setup time (to $\overline{SCK0}$ ↑)	t_{SIK2}		100			ns
SI0 hold time (from $\overline{SCK0}$ ↑)	t_{KSI2}		400			ns
$\overline{SCK0}$ ↓ → SO0 output delay time	t_{KSO2}	C = 100 pF[Note]			300	ns
$\overline{SCK0}$ rise, fall time	t_{R2}, t_{F2}				160	ns

Note C is the SO0 output line load capacitance.

(iii) 2-wire serial I/O mode ($\overline{SCK0}$ ··· internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	R = 1 kΩ, C = 100 pF[Note]		1600			ns
$\overline{SCK0}$ high-level width	t_{KH3}			$t_{KCY3}/2 - 160$			ns
$\overline{SCK0}$ low-level width	t_{KL3}		V_{DD} = 4.5 to 5.5 V	$t_{KCY3}/2 - 50$			ns
				$t_{KCY3}/2 - 100$			ns
SB0, SB1 setup time (to $\overline{SCK0}$ ↑)	t_{SIK3}		V_{DD} = 4.5 to 5.5 V	300			ns
				350			ns
SB0, SB1 hold time (from $\overline{SCK0}$ ↑)	t_{KSI3}			600			ns
$\overline{SCK0}$ ↓ → SB0, SB1 output delay time	t_{KSO3}			0		300	ns

Note R and C are the $\overline{SCK0}$, SB0, SB1 output line load resistance and load capacitance.

(iv) 2-wire serial I/O mode ($\overline{SCK0}$ ··· external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}			1600			ns
$\overline{SCK0}$ high-level width	t_{KH4}			650			ns
$\overline{SCK0}$ low-level width	t_{KL4}			800			ns
SB0, SB1 setup time (to $\overline{SCK0}$ ↑)	t_{SIK4}			100			ns
SB0, SB1 hold time (from $\overline{SCK0}$ ↑)	t_{KSI4}			$t_{KCY4}/2$			ns
$\overline{SCK0}$ ↓ → SB0, SB1 output delay time	t_{KSO4}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	0		300	ns
				0		500	ns
$\overline{SCK0}$ rise, fall time	t_{R4}, t_{F4}					160	ns

Note R and C are the SB0, SB1 output line load resistance and load capacitance.

(v) I²C bus mode (SCL ⋯ internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF[Note]		10			μs
SCL high-level width	t_{KH5}			$t_{KCY5}/2 - 160$			ns
SCL low-level width	t_{KL5}		V_{DD} = 4.5 to 5.5 V	$t_{KCY5}/2 - 50$			ns
				$t_{KCY5}/2 - 100$			ns
SDA0, SDA1 setup time (to SCL ↑)	t_{SIK5}			200			ns
SDA0, SDA1 hold time (from SCL ↓)	t_{KSI5}			0			ns
SCL ↓ → SDA0, SDA1 output delay time	t_{KSO5}		V_{DD} = 4.5 to 5.5 V	0		300	ns
				0		500	ns
SCL ↑ → SDA0, SDA1 ↓ or SCL ↑ → SDA0, SDA1 ↑	t_{KBS}			200			ns
SDA0, SDA1 ↓ → SCL ↓	t_{SBK}			400			ns
SDA0, SDA1 high-level width	t_{SBH}			500			ns

Note R and C are the SCL, SDA0, SDA1 output line load resistance and load capacitance.

(vi) I²C bus mode (SCL ⋯ external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
SCL cycle time	t_{KCY6}			1000			ns
SCL high-/low-level width	t_{KH6}, t_{KL6}			400			ns
SDA0, SDA1 setup time (to SCL ↑)	t_{SIK6}			200			ns
SDA0, SDA1 hold time (from SCL ↓)	t_{KSI6}			0			ns
SCL ↓ → SDA0, SDA1 output delay time	t_{KSO6}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	0		300	ns
				0		500	ns
SCL ↑ → SDA0, SDA1 ↓ or SCL ↑ → SDA0, SDA1 ↑	t_{KSB}			200			ns
SDA0, SDA1 ↓ → SCL ↓	t_{SBK}			400			ns
SDA0, SDA1 high-level width	t_{SBH}			500			ns
SCL rise, fall time	t_{R6}, t_{F6}					1000	ns

Note R and C are the SDA0, SDA1 output line load resistance and load capacitance.

(b) Serial Interface Channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$ ··· internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY7}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH7},	V_{DD} = 4.5 to 5.5 V	$t_{KCY7}/2 - 50$			ns
	t_{KL7}		$t_{KCY7}/2 - 100$			ns
SI1 setup time (to $\overline{SCK1}$ ↑)	t_{SIK7}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI1 hold time (from $\overline{SCK1}$ ↑)	t_{KSI7}		400			ns
$\overline{SCK1}$ ↓ → SO1 output delay time	t_{KSO7}	C = 100 pF[Note]			300	ns

Note C is the $\overline{SCK1}$, SO1 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$ ··· external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY8}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH8},	V_{DD} = 4.5 to 5.5 V	400			ns
	t_{KL8}		800			ns
SI1 setup time (to $\overline{SCK1}$ ↑)	t_{SIK8}		100			ns
SI1 hold time (from $\overline{SCK1}$ ↑)	t_{KSI8}		400			ns
$\overline{SCK1}$ ↓ → SO1 output delay time	t_{KSO8}	C = 100 pF[Note]			300	ns
$\overline{SCK1}$ rise, fall time	t_{R8}, t_{F8}				160	ns

Note C is the SO1 output line load capacitance.

(iii) 3-wire serial I/O mode with automatic transmission/reception function ($\overline{SCK1}$ ··· internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH9}, t_{KL9}	V_{DD} = 4.5 to 5.5 V	$t_{KCY9}/2 - 50$			ns
			$t_{KCY9}/2 - 100$			ns
SI1 setup time (to $\overline{SCK1}$ ↑)	t_{SIK7}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI1 hold time (from $\overline{SCK1}$ ↑)	t_{KSI7}		400			ns
$\overline{SCK1}$ ↓ → SO1 output delay time	t_{KSO7}	C = 100 pF[Note]			300	ns
$\overline{SCK1}$ ↓ → STB ↑	t_{SBD}		$t_{KCY9}/2 - 100$		$t_{KCY9}/2 + 100$	ns
Strobe signal high-level width	t_{SBW}		$t_{KCY9} - 30$		$t_{KCY9} + 30$	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
Busy inactive → $\overline{SCK1}$ ↓	t_{SPS}				$2t_{KCY9}$	ns

Note C is the $\overline{SCK1}$, SO1 output line load capacitance.

(iv) 3-wire serial I/O mode with automatic transmission/reception function ($\overline{SCK1}$ ··· external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK1}$ high-/low-level width	t_{KH10}, t_{KL10}	V_{DD} = 4.5 to 5.5 V	400			ns
			800			ns
SI1 setup time (to $\overline{SCK1}$ ↑)	t_{SIK10}		100			ns
SI1 hold time (from $\overline{SCK1}$ ↑)	t_{KSI10}		400			ns
$\overline{SCK1}$ ↓ → SO1 output delay time	t_{KSO10}	C = 100 pF[Note]			300	ns
$\overline{SCK1}$ rise, fall time	t_{R10}, t_{F10}				160	ns

Note C is the SO1 output line load capacitance.

(c) Serial Interface Channel 2

(i) 3-wire serial I/O mode ($\overline{SCK2}$ ··· internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY11}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK2}$ high-/low-level width	t_{KH11}, t_{KL11}	V_{DD} = 4.5 to 5.5 V	$t_{KCY11}/2 - 50$			ns
			$t_{KCY11}/2 - 100$			ns
SI2 setup time (to $\overline{SCK2}$ ↑)	t_{SIK11}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI2 hold time (from $\overline{SCK2}$ ↑)	t_{KSI11}		400			ns
$\overline{SCK2}$ ↓ → SO2 output delay time	t_{KSO11}	C = 100 pF[Note]			300	ns

Note C is the $\overline{SCK2}$, SO2 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{SCK2}$ ··· external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY12}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK2}$ high-/low-level width	t_{KH12}, t_{KL12}	V_{DD} = 4.5 to 5.5 V	400			ns
			800			ns
SI2 setup time (to $\overline{SCK2}$ ↑)	t_{SIK12}		100			ns
SI2 hold time (from $\overline{SCK2}$ ↑)	t_{KSI12}		400			ns
$\overline{SCK2}$ ↓ → SO2 output delay time	t_{KSO12}	C = 100 pF[Note]			300	ns
$\overline{SCK2}$ rise, fall time	t_{R12}, t_{F12}				160	ns

Note C is the SO2 output line load capacitance.

(iii) UART mode (Dedicated baud rate generator output)

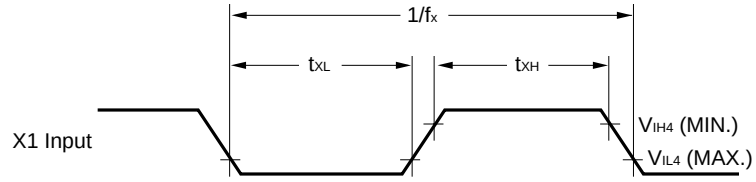
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 4.5 to 5.5 V			78125	bps
					39063	bps

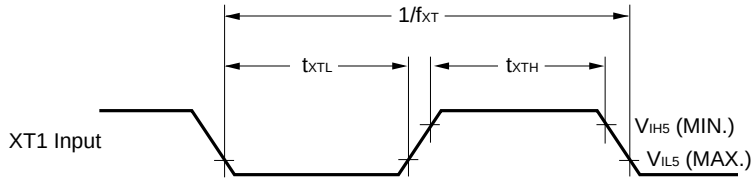
(iv) UART mode (External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY13}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
ASCK high-/low-level width	t_{KH13}, t_{KL13}	V_{DD} = 4.5 to 5.5 V	400			ns
			800			ns
Transfer rate		V_{DD} = 4.5 to 5.5 V			39063	bps
					19531	bps
ASCK rise, fall time	t_{R13}, t_{F13}				160	ns

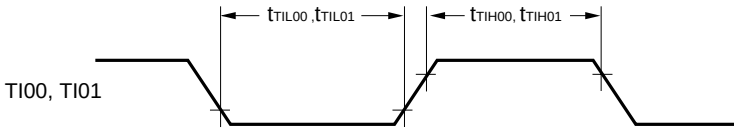
AC Timing Test Point (Excluding X1, XT1 Input)

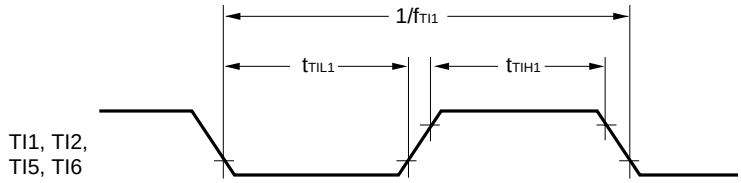
Clock Timing





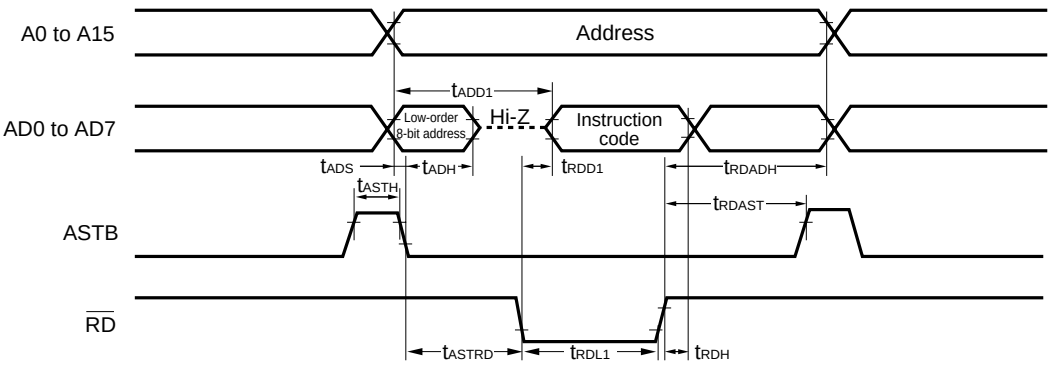
TI Timing



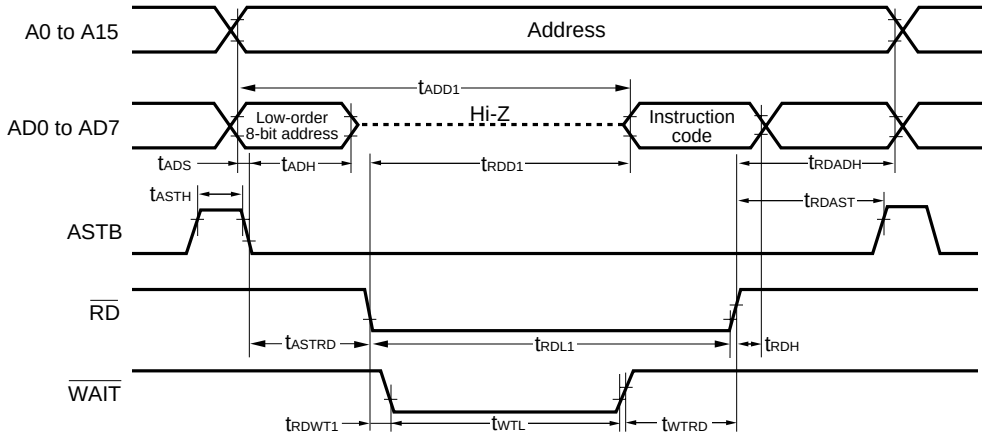


Read/Write Operation

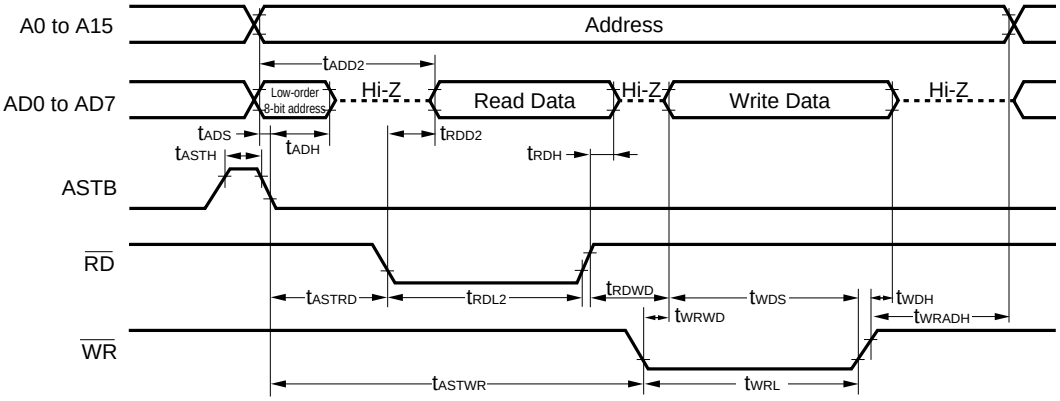
External fetch (no wait):



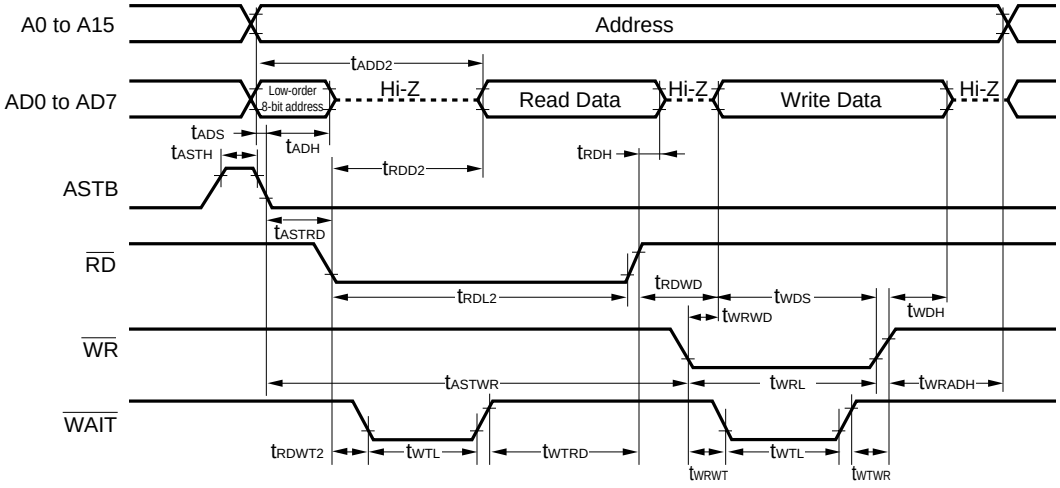
External fetch (wait insertion):



External data access (no wait):

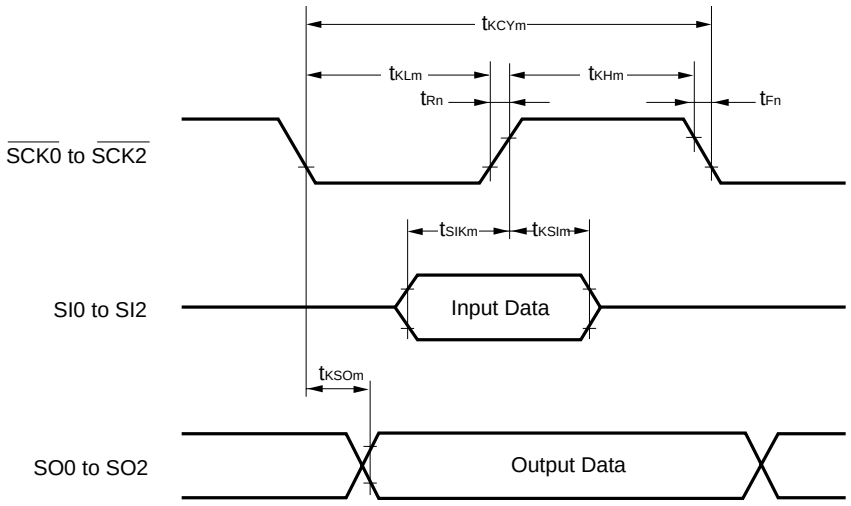


External data access (wait insertion):



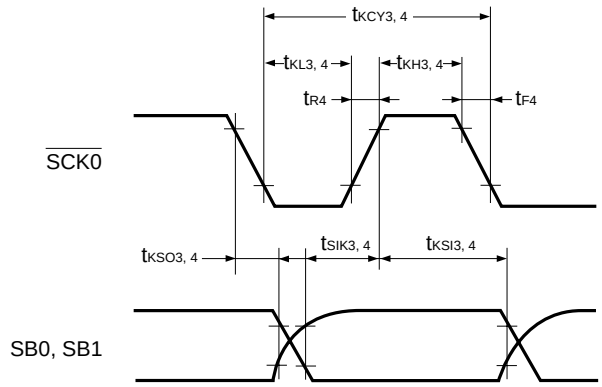
Serial Transfer Timing

3-wire serial I/O mode:

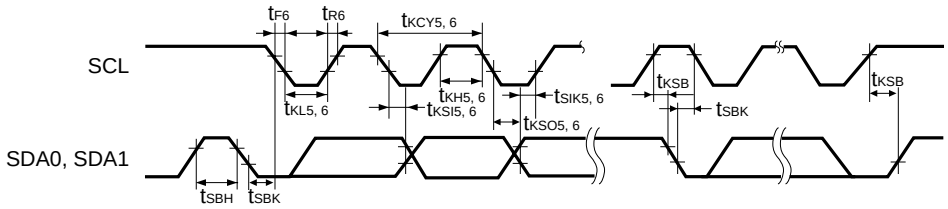


Remark m = 1, 2, 7, 8, 11, 12
n = 2, 8, 12

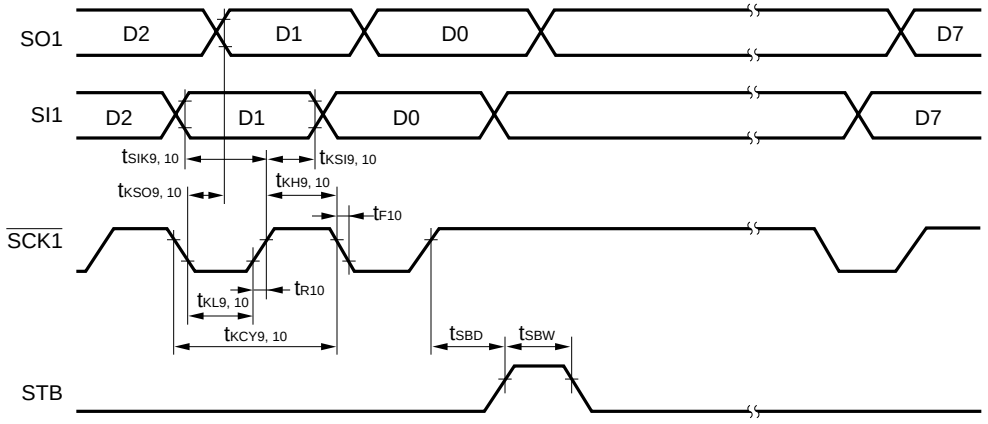
2-wire serial I/O mode:



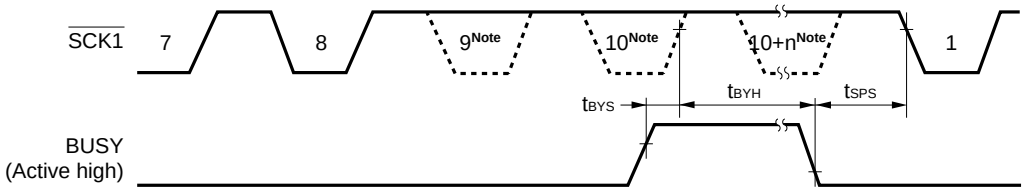
I²C bus mode:



3-wire serial I/O mode with automatic transmission/reception function:

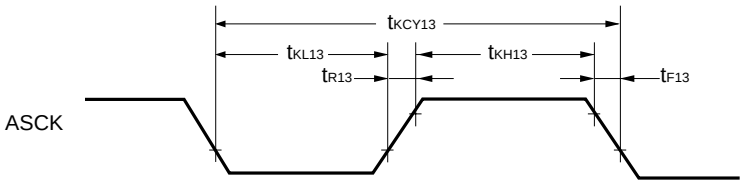


3-wire serial I/O mode with automatic transmission/reception function (busy processing):



Note The signal is not actually low here, but is represented in this way to show the timing.

UART mode (external clock input):



A/D CONVERTER CHARACTERISTICS (T_A = –40 to +85°C, AV_{DD} = V_{DD} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Total error[Note]		2.7 V ≤ AV_{REF0} ≤ AV_{DD}			0.6	%
Conversion time	t_{CONV}		19.1		200	μs
Sampling time	t_{SAMP}		12/f_{XX}			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}		2.7		AV_{DD}	V
AV_{REF0}—AV_{SS} resistance	R_{AIREF0}		4	14		kΩ

Note Excluding quantization error (±1/2 LSB). Shown as a percentage of the full scale value.

Remark f_{XX}: Main system clock frequency (fx or fx/2)
f_X: Main system clock oscillation frequency

D/A CONVERTER CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Resolution						8	bit
Total error		R = 2 MΩ[Note 1]				1.2	%
		R = 4 MΩ[Note 1]				0.8	%
		R = 10 MΩ[Note 1]				0.6	%
Settling time		C = 30 pF[Note 1]	4.5 V ≤ AV_{REF1} ≤ 5.5 V			10	μs
			2.7 V ≤ AV_{REF1} < 4.5 V			15	μs
Output resistor	R_O	**Note 2**			10		kΩ
Analog reference voltage	AV_{REF1}			2.7		V_{DD}	V
AV_{REF0}—AV_{SS} resistance	R_{AIREF1}	DACS0, DACS1 = 55H[Note 2]		4	8		kΩ

Notes 1. R and C are the D/A converter output pin load resistance and load capacitance.
2. Value for one D/A converter channel.

Remark DACS0, DACS1: D/A conversion value setting registers 0, 1.

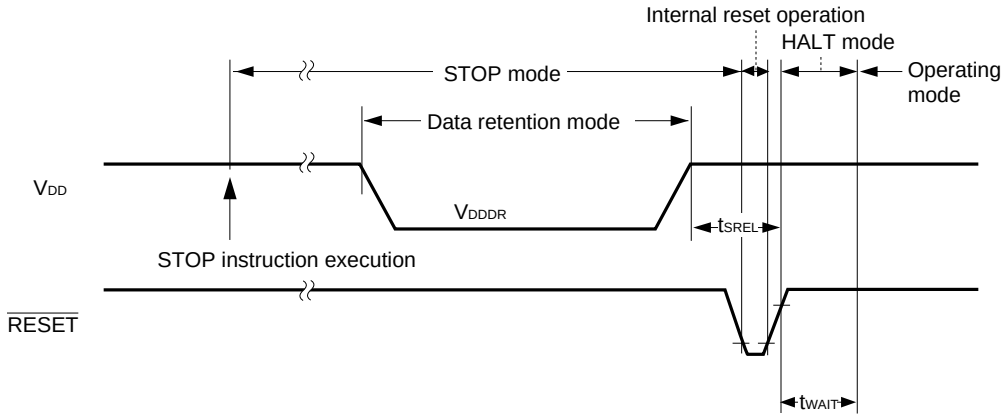
DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (T_A = –40 to +85°C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8 V When subsystem clock stopped and feedback resistor disconnected		0.1	10	μA
Release signal setup time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note**		ms

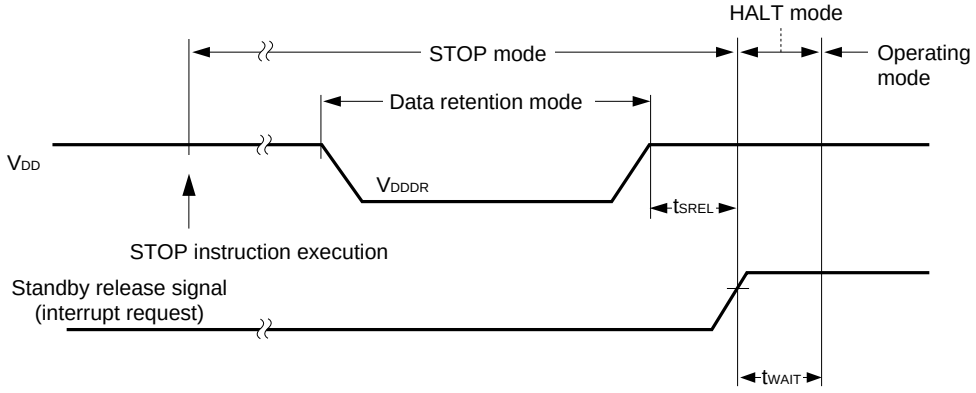
Note $2^{12}/f_{XX}$ or $2^{14}/f_{XX}$ to $2^{17}/f_{XX}$ can be selected by bit 0 to bit 2 (OSTS0 to OSTS2) of oscillation stabilization time selection register (OSTS).

Remark f_{XX}: Main system clock frequency (f_X or $f_X/2$)
f_X: Main system clock oscillation frequency

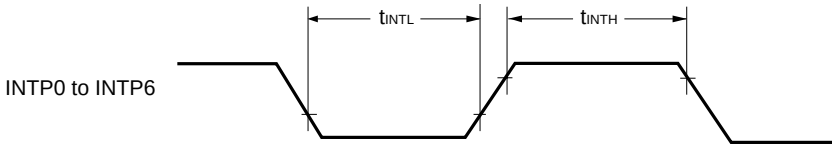
Data Retention Timing (STOP mode released by $\overline{RESET}$)



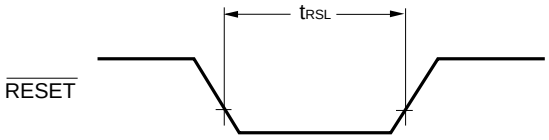
Data Retention Timing (Standby release signal: STOP mode released by interrupt signal)



Interrupt Request Input Timing

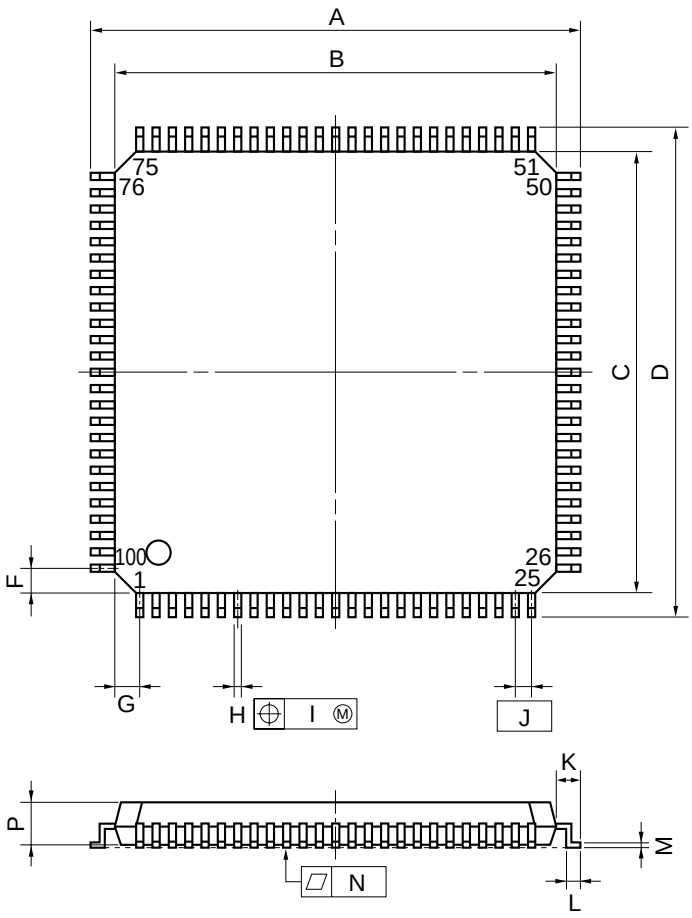


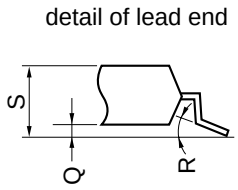
$\overline{\text{RESET}}$ Input Timing



12. PACKAGE DRAWINGS

100 PIN PLASTIC QFP (FINE PITCH) (□14)





NOTE

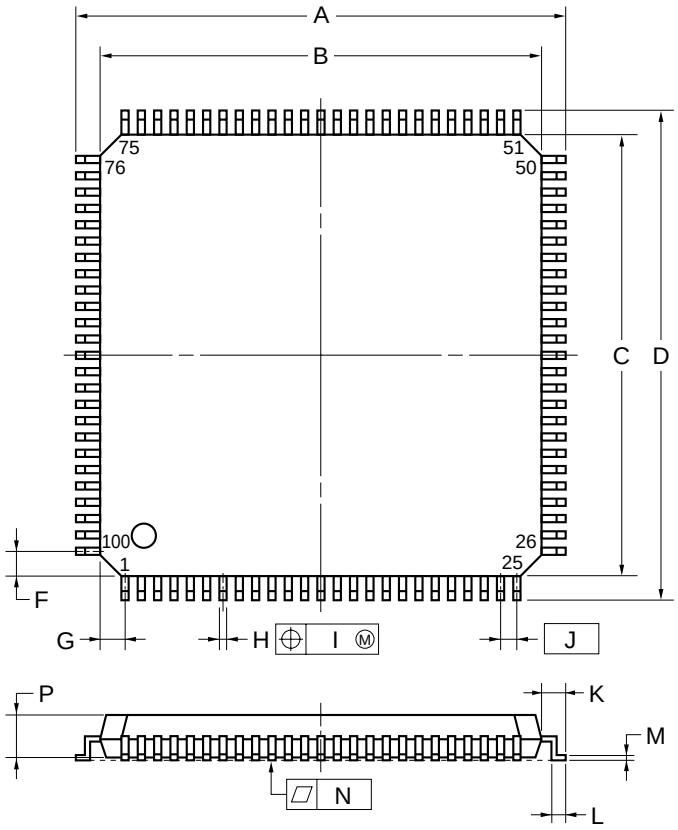
Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

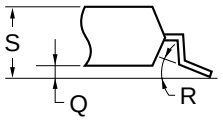
ITEM	MILLIMETERS	INCHES
A	16.0±0.2	0.630±0.008
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	16.0±0.2	0.630±0.008
F	1.0	0.039
G	1.0	0.039
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	1.45	0.057
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

P100GC-50-7EA-2

★ **Remark** The shape and material of ES versions are the same as those mass-produced versions.

★ 100 PIN PLASTIC LQFP (FINE PITCH) (14×14)





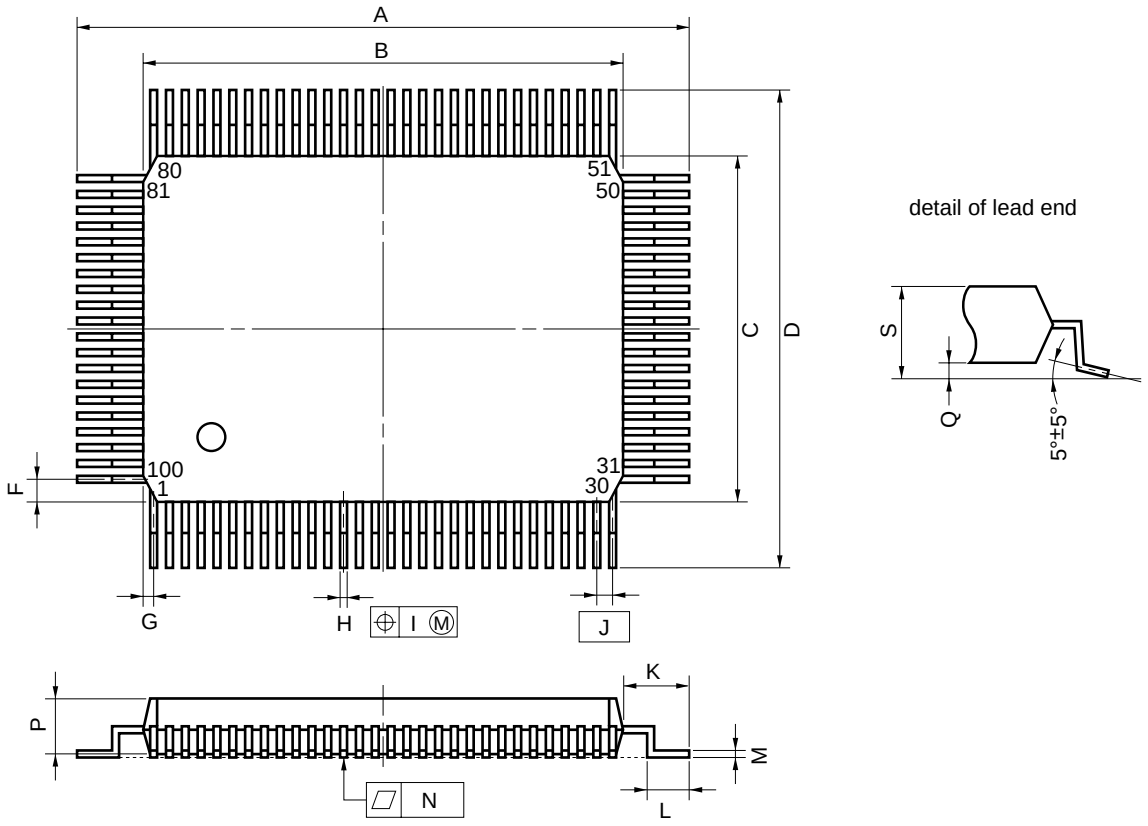
NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.00±0.20	0.630±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	16.00±0.20	0.630±0.008
F	1.00	0.039
G	1.00	0.039
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.08	0.003
J	0.50 (T.P.)	0.020 (T.P.)
K	1.00±0.20	$0.039^{+0.009}_{-0.008}$
L	0.50±0.20	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.08	0.003
P	1.40±0.05	0.055±0.002
Q	0.10±0.05	0.004±0.002
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.60 MAX.	0.063 MAX.

S100GC-50-8EU

100 PIN PLASTIC QFP (14 × 20)



P100GF-65-3BA1-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

★ **Remark** The shape and material of ES versions are the same as those mass-produced versions.

13. RECOMMENDED SOLDERING CONDITIONS

It is recommended that the μPD78070AY be soldered under the following conditions.
For details on the recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

Table 13-1. Soldering Conditions for Surface Mount Devices

(1) μPD78070AYGC-7EA: 100-pin plastic QFP (Fine pitch) (14 × 14 mm, resin thickness 1.45 mm)

Soldering Method	Soldering Conditions	Symbol
Infrared ray reflow	Package peak temperature: 235°C, Reflow time: 30 seconds or less (at 210°C or higher), Number of reflow processes: 2 or less, Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125°C afterwards)	IR35-107-2
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds or less (at 200°C or higher), Number of reflow processes: 2 or less, Exposure limit: 7 days[Note] (10 hours pre-baking is required at 125°C afterwards)	VP15-107-2
Partial heating	Pin temperature: 300°C or below, Flow time: 3 seconds or less (per device side)	—

Note Exposure limit before soldering after the dry pack package is opened. Storage conditions: 25°C and relative humidity at 65% or less.

★ **(2) μPD78070AYGF-3BA: 100-pin plastic QFP (14 × 20 mm, resin thickness 2.7 mm)**

Soldering Method	Soldering Conditions	Symbol
Infrared ray reflow	Package peak temperature: 235°C, Reflow time: 30 seconds or less (at 210°C or higher), Number of reflow processes: 3 or less	IR35-00-3
VPS	Package peak temperature: 215°C, Reflow time: 40 seconds or less (at 200°C or higher), Number of reflow processes: 3 or less	VP15-00-3
Wave soldering	Solder temperature: 260°C or below, Flow time: 10 seconds or less, Number of flow processes: 1, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C or below, Flow time: 3 seconds or less (per device side)	—

Cautions 1. Do not use different soldering methods together (except for partial heating method).
2. Since the μPD78070AYGC-8EU is under planning, soldering conditions are not determined.

★ APPENDIX A. DEVELOPMENT TOOLS

The following dvelopment tools are available to support development of systems using the μPD78070AY.

Language Processing Software

RA78K/0[Notes 1, 2, 3, 4]	Assembler package common to the 78K/0 Series
CC78K/0[Notes 1, 2, 3, 4]	C compiler package common to the 78K/0 Series
DF78078[Notes 1, 2, 3, 4]	Device file common to the μPD78078 Subseries
CC78K/0–L[Notes 1, 2, 3, 4]	C compiler library source file common to the 78K/0 Series

Debugging Tools

IE-78000-R	In-circuit emulator common to the 78K/0 Series
IE-78000-R-A	In-circuit emulator common to the 78K/0 Series (for Integrated debugger)
IE-78000-R-BK	Break board common to the 78K/0 Series
IE-78078-R-EM	Emulation board common to the μPD78078 Subseries
EP-78064GC-R EP-78064GF-R	Emulation probe common to the μPD78064 Subseries
TGC-100SDW	Adapter to be mounted on the target system board prepared for 100-pin plastic QFP (GC-7EA, GC-8EU type) Manufactured by TOKYO ELETECH Corporation Contact an NEC representative to purchase.
EV-9200GF-100	Socket to be mounted on the target system board prepared for 100-pin plastic QFP (GF-3BA type)
SM78K0[Notes 5, 6, 7]	System simulator common to the 78K/0 Series
ID78K0[Notes 4, 5, 6, 7]	Integrated debugger for IE-78000-R-A
SD78K/0[Notes 1, 2]	Screen debugger for the IE-78000-R
DF78078[Notes 1, 2, 4, 5, 6, 7]	Device file common to the μPD78078 Subseries

Real-Time OS

RX78K/0[Notes 1, 2, 3, 4]	Real-time OS used for the 78K/0 Series
MX78K0[Notes 1, 2, 3, 4]	OS used for the 78K/0 Series

Fuzzy Inference Development Support System

FE9000[Note 1]/FE9200[Note 6]	Fuzzy knowledge data creation tool
FT9080[Note 1]/FT9085[Note 2]	Translator
FI78K0[Notes 1, 2]	Fuzzy inference module
FD78K0[Notes 1, 2]	Fuzzy inference debugger

Notes 1. Based on PC-9800 Series (MS-DOS™)
2. Based on IBM PC/AT™ and compatibles (PC DOS™/IBM DOS™/MS-DOS)
3. Based on HP9000 Series 300™ (HP-UX™)
4. Based on HP9000 Series 700™ (HP-UX), SPARCstation™ (SunOS™), and EWS4800 Series (EWS-UX/V)
5. Based on PC-9800 Series (MS-DOS + Windows™)
6. Based on IBM PC/AT and compatibles (PC DOS/IBM DOS/MS-DOS + Windows)
7. Based on NEWS™ (NEWS-OS™)

Remarks 1. Please refer to the **78K/0 Series Selection Guide (U11126E)** for information on the third party development tools.
2. Use the RA78K/0, CC78K/0, SM78K0, ID78K0, SD78K/0, RX78K/0 in combination with the DF78078.

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APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document No.	
	Japanese	English
μPD78070A, 78070AY User's Manual	IEU-907	U10200E
μPD78070AY Data Sheet	U10542J	This document
μPD78P078Y Data Sheet	U10605J	U10605E
78K/0 Series User's Manual—Instructions	U12326J	U12326E
78K/0 Series Instruction Table	U10903J	—
78K/0 Series Instruction Set	U10904J	—
μPD78070AY Special Function Register Table	U10134J	—

Documents Related to Development Tools (1/2)

Document Name		Document No.	
		Japanese	English
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
RA78K0 Assembler Package	Operation	U11802J	U11802E
	Assembly language	U11801J	U11801E
	Structured assembly language	U11789J	U11789E
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K0 C Compiler	Operation	U11517J	U11517E
	Language	U11518J	U11518E
CC78K/0 C Compiler Application Note	Programming know-how	EEA-618	EEA-1208
CC78K Series Library Source File		U12322J	—
IE-78000-R		EEU-810	EEU-1398
IE-78000-R-A		U10057J	U10057E
IE-78000-R-BK		EEU-867	EEU-1427
IE-78078-R-EM		EEU-978	EEU-1504
EP-78064		EEU-934	EEU-1522

Caution The contents of the documents listed above are subject to change without prior notice. Be sure to use the latest edition when starting design.

Documents Related to Development Tools (2/2)

Document Name		Document No.	
		Japanese	English
SM78K0 System Simulator Windows Based	Reference	U10181J	U10181E
SM78K Series System Simulator	External parts user open interface specification	U10092J	U10092E
ID78K0 Integrated Debugger EWS Based	Reference	U11151J	—
ID78K0 Integrated Debugger PC Based	Reference	U11539J	U11539E
ID78K0 Integrated Debugger Windows Based	Guide	U11649J	U11649E
SD78K/0 Screen Debugger PC-9800 Series (MS-DOS) Based	Introduction	EEU-852	U10539E
	Reference	U10952J	—
SD78K/0 Screen Debugger IBM PC/AT (PC DOS) Based	Introduction	EEU-5024	EEU-1414
	Reference	U11279J	U11279E

Documents Related to Embedded Software (User's Manual)

Document Name		Document No.	
		Japanese	English
78K/0 Series Real-time OS	Basic	U11537J	—
	Installation	U11536J	—
78K/0 Series OS MX78K0	Basic	U12257J	—
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K/0, 78K/II, and 87AD Series Fuzzy Inference Development Support System Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-921	EEU-1458

Other Documents

Document Name	Document No.	
	Japanese	English
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
NEC Semiconductor Device Quality Grades	C10531J	C10531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Electrostatic Discharge (ESD) Test	MEM-539	—
Semiconductor Device Quality Assurance Guide	C11893J	MEI-1202
Microcontroller-Related Product Guide – Third Party Products –	U11416J	—

Caution The contents of the documents listed above are subject to change without prior notice. Be sure to use the latest edition when starting design.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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Note: Purchase of NEC I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.