

MOS INTEGRATED CIRCUIT

μ PD78062, 78063, 78064

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

μ PD78062/78063/78064 is a product in the μ PD78064 subseries within the 78K/0 series, which incorporates LCD controller/driver, 8-bit resolution A/D converter, timer, serial interface, interrupt functions and many other peripheral hardwares.

A one-time PROM product capable of operating in the same power supply voltage range as of the mask ROM product, EPROM product and other development tools are also provided.

For the details of functional description, refer to the following user's manual.

μ PD78064 78064Y Subseries User's Manual : U10105E

78K/0 Series User's Manual (Instruction : IEU-1372

FEATURES

- Large on-chip ROM & RAM

Item Product Name	Program Memory (ROM)	Data Memory		Package
		Internal High-Speed RAM	LCD Display RAM	
μ PD78062	16K bytes	512 bytes	40 × 4 bits	100-pin plastic QFP (fine pitch) (14 × 14mm, 0.5 mm pitch)
μ PD78063	24K bytes	1024 bytes		100-pin plastic QFP (14 × 20 mm, 0.65 mm pitch)
★ μ PD78064	32K bytes			100-pin plastic LQFP (fine pitch) (14 × 14 mm, 0.5 mm pitch)

- Instruction execution time can be varied from high speed (0.4 μ s) to ultra-low speed (122 μ s)
- I/O ports: 57 (including segment signal output dual-function pins)
- LCD controller/driver
 - Supply voltage $V_{DD} = 2.0$ to 6.0 V (Static display mode)
 - $V_{DD} = 2.5$ to 6.0 V (1/3 bias)
 - $V_{DD} = 2.7$ to 6.0 V (1/2 bias)
- 8-bit resolution A/D converter : 8 channels
- Serial interface : 2 channels
- Timer: 5 channels
- Supply voltage : $V_{DD} = 2.0$ to 6.0 V

The information in this document is subject to change without notice.

APPLICATIONS

Cellular phone, CD player, cameras, etc.

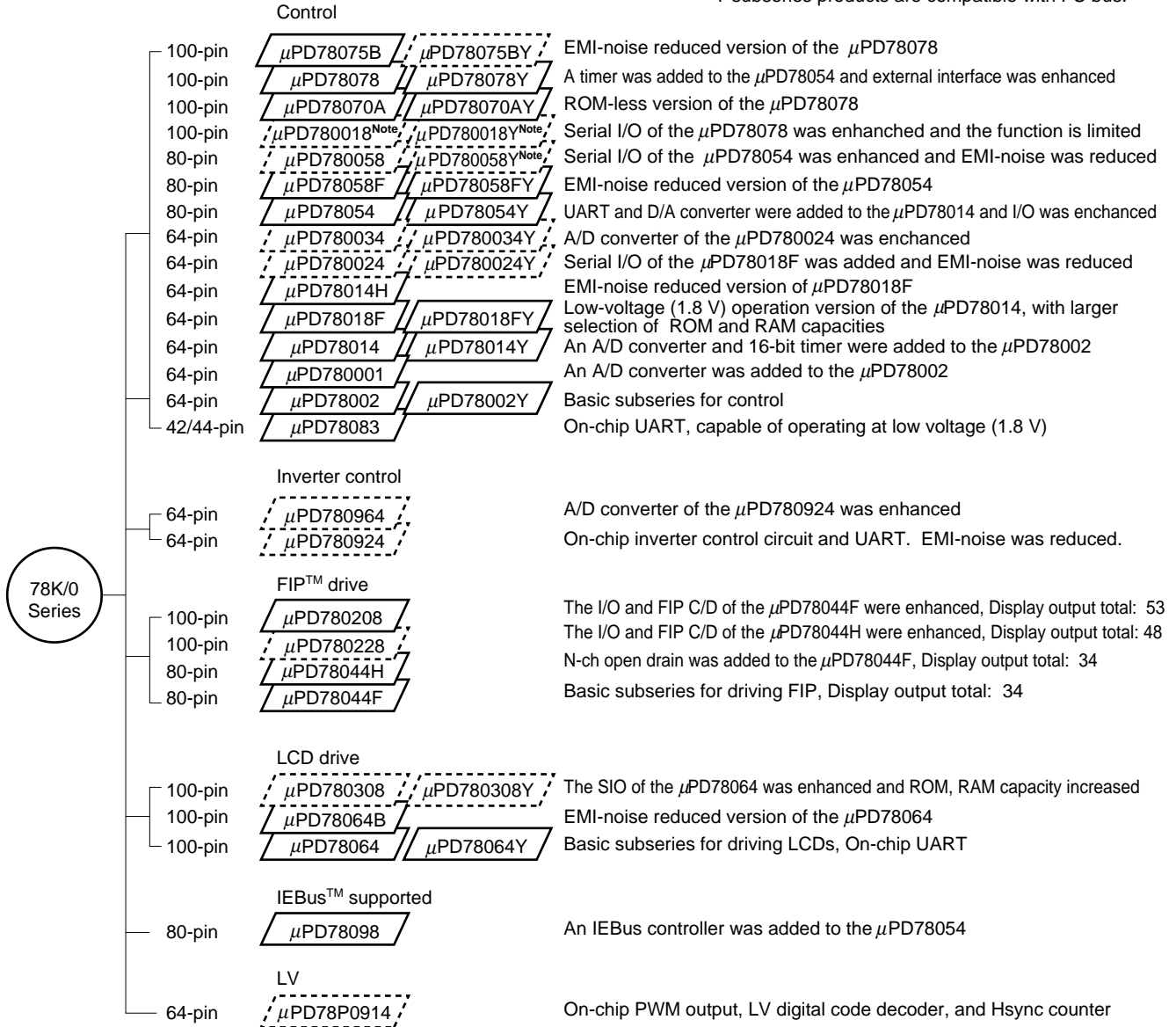
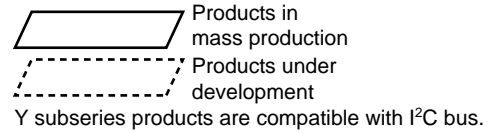
ORDERING INFORMATION

	Part Number	Package
	μPD78062GC-xxx-7EA	100-pin plastic QFP (fine pitch) (14 × 14 mm, resin thickness: 1.45 mm)
★	μPD78062GC-xxx-8EU	100-pin plastic LQFP (fine pitch) (14 × 14 mm, resin thickness: 1.40 mm)
	μPD78062GF-xxx-3BA	100-pin plastic QFP (14 × 20mm)
	μPD78063GC-xxx-7EA	100-pin plastic QFP (fine pitch) (14 × 14 mm, resin thickness: 1.45 mm)
★	μPD78063GC-xxx-8EU	100-pin plastic LQFP (fine pitch) (14 × 14 mm, resin thickness: 1.40 mm)
	μPD78063GF-xxx-3BA	100-pin plastic QFP (14 × 20mm)
	μPD78064GC-xxx-7EA	100-pin plastic QFP (fine pitch) (14 × 14 mm, resin thickness: 1.45 mm)
★	μPD78064GC-xxx-8EU	100-pin plastic LQFP (fine pitch) (14 × 14 mm, resin thickness: 1.40 mm)
	μPD78064GF-xxx-3BA	100-pin plastic QFP (14 × 20mm)
★	Caution The μPD78062GC, 78063GC, and 78064GC are available in two types of packages (refer to 12. PACKAGE DRAWINGS). For the available packages, consult NEC.	

Remark xxx is a ROM code suffix.

★ 78K/0 SERIES PRODUCT DEVELOPMENT

The following shows the 78 K/0 Series products development. Subseries name are shown inside frames.



Note Under planning

The following lists the main functional differences between subseries products.

Function Subseries Name		ROM Capacity	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	V _{DD} MIN. Value	External Expansion									
			8-bit	16-bit	Watch	WDT																
Control	μPD78075B	32 K - 40 K	4 ch	1 ch	1 ch	1 ch	8 ch	-	2 ch	3 ch (UART : 1 ch)	88	1.8 V	○									
	μPD78078	48 K - 60 K									61			2.7 V								
	μPD78070A	-									88											
	μPD780018	48 K - 60 K	2 ch	-	-	-	-	8 ch	-	2 ch (time division 3-wire: 1 ch)	88	1.8 V	-									
	μPD780058	24 K - 60 K								2 ch	3 ch (time division UART: 1 ch)			68	1.8 V							
	μPD78058F	48 K - 60 K								3 ch (UART: 1 ch)	69			2.7 V								
	μPD78054	16 K - 60 K								2.0 V	1.8 V											
	μPD780034	8 K - 32 K								-				8 ch	-	3 ch (UART: 1 ch, time division 3-wire: 1 ch)	51	1.8 V				
	μPD780024									8 ch	-			2 ch	53							
	μPD78014H	8 K - 60 K								-	-			-	-	-	-	-	1 ch	39	2.7 V	-
	μPD78018F																			8 K - 32 K		
	μPD78014	8 K								-	-			-	-	-	-	-	-	39	2.7 V	-
	μPD780001	8 K - 16 K								-	1 ch			-	-	-	-	-	-	53		
	μPD78002	8 K	-	-	-	-	-	-	-	-	39	2.7 V	-									
μPD78083	8 K - 16 K	-	1 ch	-	-	-	-	-	-	53												
μPD78083	8 K	-	-	-	-	8 ch	-	-	1 ch (UART: 1 ch)	33	1.8 V	-										
Inverter control	μPD780964	8 K - 32 K	3 ch	Note	-	1 ch	-	8 ch	-	2 ch (UART: 2 ch)	47	2.7 V	○									
	μPD780924						8 ch	-														
FIP drive	μPD780208	32 K - 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	-	-	2 ch	74	2.7 V	-									
	μPD780228	48 K - 60 K								3 ch	-	-		1 ch	72	4.5 V						
	μPD78044H	32 K - 48 K	2 ch	1 ch	1 ch	-	-	-	-	68	2.7 V											
	μPD78044F	16 K - 40 K								2 ch												
LCD drive	μPD780308	48 K - 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	-	-	3 ch (time division UART: 1 ch)	57	2.0 V	-									
	μPD78064B	32 K								2 ch (UART : 1 ch)												
	μPD78064	16 K - 32 K																				
IEBus supported	μPD78098	32 K - 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	-	2 ch	3 ch (UART : 1 ch)	69	2.7 V	○									
LV	μPD78P0914	32 K	6 ch	-	-	1 ch	8 ch	-	-	2 ch	54	4.5 V	○									

Note 10-bit timer: 1 channel

FUNCTIONAL OUTLINE

Product Name		μPD78062	μPD78063	μPD78064						
Internal memory	ROM	16K bytes	24K bytes	32K bytes						
	High-speed RAM	512 bytes	1024 bytes							
	LCD display RAM	40 × 4 bits								
General registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)								
Instruction cycle		On-chip instruction execution time cycle modification function								
	When main system clock selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (at 5.0 MHz operation)								
	When subsystem clock selected	122 μs (at 32.768 kHz operation)								
Instruction set		<ul style="list-style-type: none"> • 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD correction, etc. 								
I/O ports (including segment signal output pins)		<table> <tr> <td>Total</td> <td>: 57</td> </tr> <tr> <td>• CMOS input</td> <td>: 2</td> </tr> <tr> <td>• CMOS I/O</td> <td>: 55</td> </tr> </table>			Total	: 57	• CMOS input	: 2	• CMOS I/O	: 55
Total	: 57									
• CMOS input	: 2									
• CMOS I/O	: 55									
A/D converter		<ul style="list-style-type: none"> • 8-bit resolution × 8 channels 								
LCD controller/driver		<ul style="list-style-type: none"> • Segment signal output : Maximum 40 • Common signal output : Maximum 4 • Bias : 1/2 or 1/3 switchable 								
Serial interface		<ul style="list-style-type: none"> • 3-wire serial I/O/SBI/2-wire serial I/O mode selectable : 1 channel • 3-wire serial I/O/UART mode selectable : 1 channel 								
Timer		<ul style="list-style-type: none"> • 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel 								
Timer output		3 (14-bit PWM output capability : 1)								
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (at main system clock 5.0 MHz operation) 32.768 kHz (at subsystem clock 32.768 kHz operation)								
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (at main system clock 5.0 MHz operation)								
Vectored interrupt sources	Maskable	Internal : 12, external : 6								
	Non-maskable	Internal : 1								
	Softwar	1								
Test input		Internal: 1, external: 1								
Supply voltage		V _{DD} = 2.0 to 6.0 V								
Package		<ul style="list-style-type: none"> • 100-pin plastic QFP (Fine pitch) (14 × 14 mm, resin thickness: 1.45 mm) • 100-pin plastic QFP (14 × 20 mm) • 100-pin plastic LQFP (Fine pitch) (14 × 14 mm, resin thickness: 1.40 mm) 								

★

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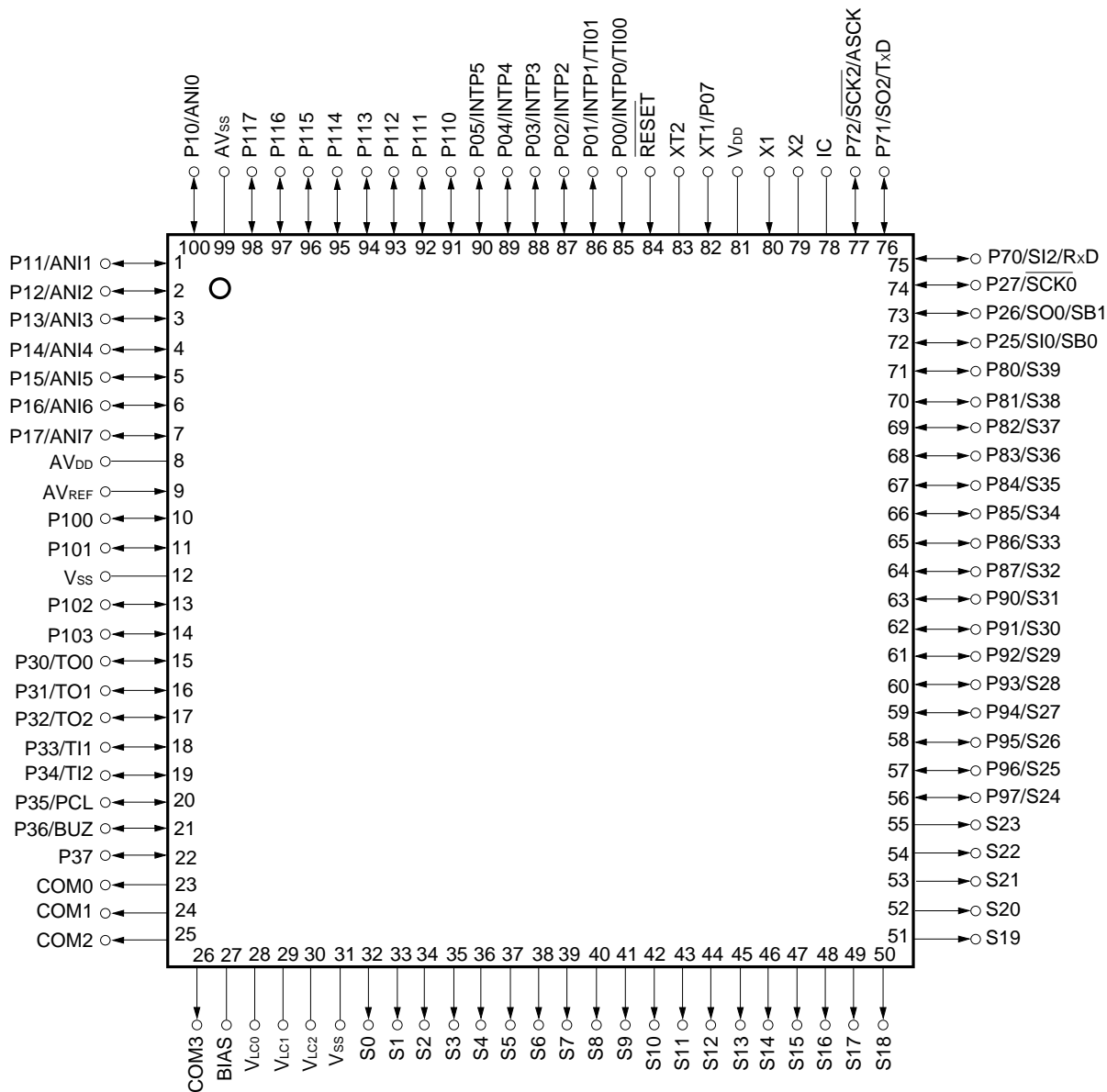
1. PIN CONFIGURATION (Top View)

• 100-pin plastic QFP (fine pitch)(14 × 14 mm, resin thickness: 1.45 mm)

μPD78062GC-xxx-7EA, 78063GC-xxx-7EA, 78064GC-xxx-7EA

★ • 100-pin plastic LQFP (fine pitch)(14 × 14 mm, resin thickness: 1.40 mm)

μPD78062GC-xxx-8EU, 78063GC-xxx-8EU, 78064GC-xxx-8EU



Cautions 1. Connect directly the IC (Internally Connected) pin to V_{SS}.

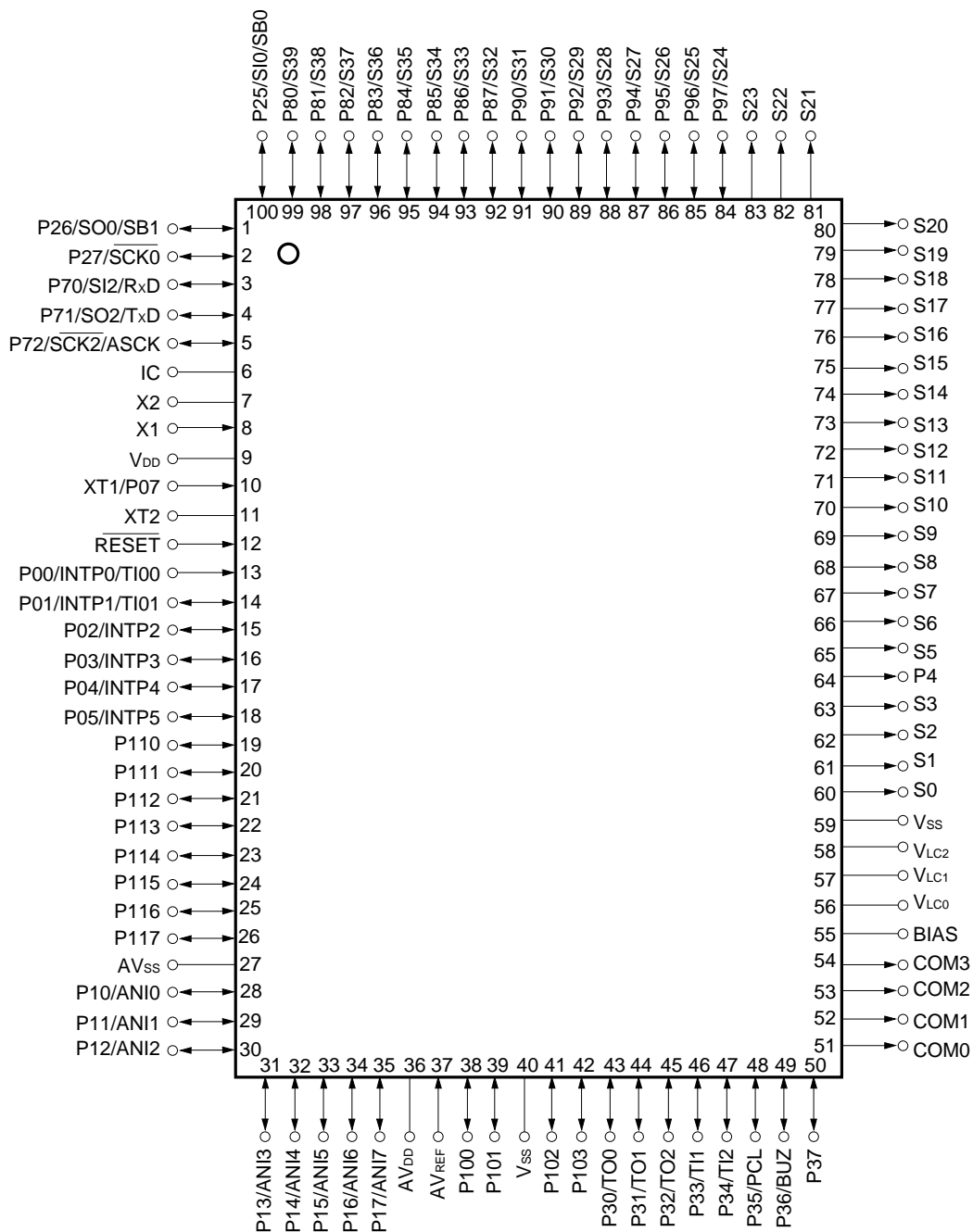
2. Connect the AV_{DD} pin to V_{DD}.

3. Connect the AV_{SS} pin to V_{SS}.

• 100-pin plastic QFP (14 × 20 mm)

μPD78062GF-xxx-3BA, 78063GF-xxx-3BA

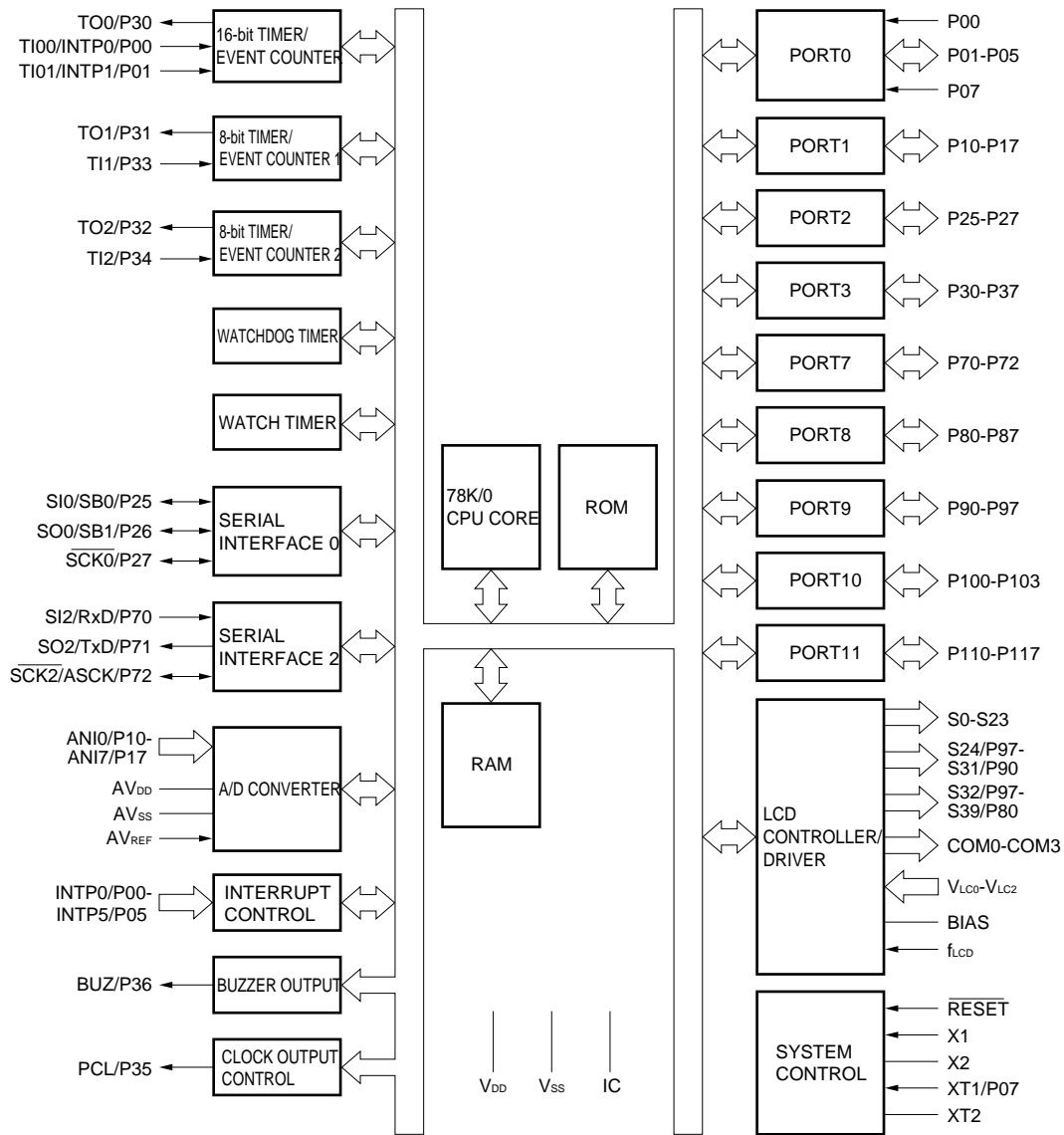
μPD78064GF-xxx-3BA



- Cautions**
1. Connect directly the IC (Internally Connected) pin to V_{SS}.
 2. Connect the AV_{DD} pin to V_{DD}.
 3. Connect the AV_{SS} pin to V_{SS}.

P00 to P05, P07	: Port0	S0 to S39	: Segment Output
P10 to P17	: Port1	COM0 to COM3	: Common Output
P25 to P27	: Port2	VLC0 to VLC2	: LCD Power Supply
P30 to P37	: Port3	BIAS	: LCD Power Supply Bias Control
P70 to P72	: Port7	X1, X2	: Crystal (Main System Clock)
P80 to P87	: Port8	XT1, XT2	: Crystal (Subsystem Clock)
P90 to P97	: Port9	$\overline{\text{RESET}}$: Reset
P100 to P103	: Port10	ANI0 to ANI7	: Analog Input
P110 to P117	: Port11	AV _{DD}	: Analog Power Supply
INTP0 to INTP5	: Interrupt from Peripherals	AV _{SS}	: Analog Ground
TI00, TI01	: Timer Input	AV _{REF}	: Analog Reference Voltage
TI1, TI2	: Timer Input	V _{DD}	: Power Supply
TO0 to TO2	: Timer Output	V _{SS}	: Ground
SB0, SB1	: Serial Bus	IC	: Internally Connected
SI0, SI2	: Serial Input		
SO0, SO2	: Serial Output		
$\overline{\text{SCK0}}, \overline{\text{SCK2}}$: Serial Clock		
RxD	: Receive Data		
TxD	: Transmit Data		
ASCK	: Asynchronous Serial Clock		
PCL	: Programmable Clock		
BUZ	: Buzzer Clock		

2. BLOCK DIAGRAM



Remark The internal ROM and RAM capacities differ depending on the product.

3. PIN FUNCTIONS

3.1 Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Dual-Function Pin
P00	Input	Port 0 7-bit I/O port.	Input only	Input	INTP0/TI00
P01	Input/ output		Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P07 ^{Note1}	Input		Input only	Input	XT1
P10 to P17	Input/ output	Port 1 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. ^{Note2}	Input	Input	ANI0 to ANI7
P25	Input/ output	Port 2 3-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.	Input	SI0/SB0	
P26				SO0/SB1	
P27				$\overline{\text{SCK0}}$	
P30	Input/ output	Port 3 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.	Input	TO0	
P31				TO1	
P32				TO2	
P33				TI1	
P34				TI2	
P35				PCL	
P36				BUZ	
P37				—	
P70	Input/ output	Port 7 3-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software.	Input	SI2/RxD	
P71				SO2/TxD	
P72				$\overline{\text{SCK2}}$ / ASCK	

- Notes**
1. When using the P07/XT1 pins as an input port, set (1) bit 6 (FRC) of the processor clock control register (PCC) (the on-chip feedback resistor of the subsystem clock oscillator should not be used).
 2. When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input, port 1 is set to input mode. However, on-chip pull-up resistor is not automatically used.

3.1 Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Dual-Function Pin
P80 to P87	Input/output	<p>Port 8 8-bit input/output port Input/output can be specified bit-wise. When used as an input port , on-chip pull-up resistor can be used by software. Input/output port/segment signal output function can be specified in 2-bit unit by the LCD control register (LCDC).</p>	Input	S39 to S32
P90 to P97	Input/output	<p>Port 9 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. Input/output port/segment signal output function can be specified in 2-bit unit by the LCD control register (LCDC).</p>	Input	S31 to S24
P100 to P103	Input/output	<p>Port 10 4-bit input/output port Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. LED direct drive capability.</p>	Input	——
P110 to P117	Input/output	<p>Port 11 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. Falling edge detection capability.</p>	Input	——

3.2 Other Pins (1/2)

Pin Name	I/O	Function	After Reset	Dual-Function Pin
INTP0	Input	External interrupt request input by which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
SI0	Input	Serial interface serial data input.	Input	P25/SB0
SI2				P70/RxD
SO0	Output	Serial interface serial data output.	Input	P26/SB1
SO2				P71/TxD
SB0	Input /output	Serial interface serial data input/output.	Input	P25/SI0
SB1				P26/SO0
$\overline{\text{SCK0}}$	Input /output	Serial interface serial clock input/output.	Input	P27
$\overline{\text{SCK2}}$				P72/ $\overline{\text{ASCK}}$
RxD	Input	Asynchronous serial interface serial data input.	Input	P70/SI2
TxD	Output	Asynchronous serial interface serial data output.	Input	P71/SO2
ASCK	Input	Asynchronous serial interface serial clock input.	Input	P72/ $\overline{\text{SCK2}}$
TI00	Input	External count clock input to 16-bit timer (TM0).	Input	P00/INTP0
TI01		Capture trigger signal input to capture register (CR00).		P01/INTP1
TI1		External count clock input to 8-bit timer (TM1).		P33
TI2		External count clock input to 8-bit timer (TM2).		P34
TO0	Output	16-bit timer (TM0) output (shared with 14-bit PWM output).	Input	P30
TO1		8-bit timer (TM1) output.		P31
TO2		8-bit timer (TM2) output.		P32
PCL	Output	Clock output (for main system clock, subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
S0 to S23	Output	LCD controller/driver segment signal output.	Output	—
S24 to S31			Input	P97 to P90
S32 to S39				P87 to P80
COM0 to COM3	Output	LCD controller/driver common signal output.	Output	—
VLC0 to VLC2	—	LCD drive voltage. Split resistors can be incorporated by mask option.	—	—
BIAS	—	LCD drive power supply.	—	—

3.2 Other Pins (2/2)

Pin Name	I/O	Function	After Reset	Dual-Function Pin
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
AV _{REF}	Input	A/D converter reference voltage input.	—	—
AV _{DD}	—	A/D converter analog power supply. Connect to V _{DD} .	—	—
AV _{SS}	—	A/D converter ground potential. Connect to V _{SS} .	—	—
$\overline{\text{RESET}}$	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection.	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection.	Input	P07
XT2	—		—	—
V _{DD}	—	Positive power supply.	—	—
V _{SS}	—	Ground potential.	—	—
IC	—	Internal connection. Connect directly to V _{SS} pin.	—	—

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, refer to **Figure 3-1**.

Table 3-1. Input/Output Circuit Type of Each Pin (1/2)

Pin Name	Input/output Circuit Type	I/O	Recommended Connection when not Used
P00/INTP0/TI00	2	Input	Connected to V _{SS} .
P01/INTP1/TI01	8-A	Input/output	Independently connected to V _{SS} through resistor.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P07/XT1	16	Input	Connected to V _{DD} .
P10/ANI0 to P17/ANI7	11	Input/output	Independently connected to V _{DD} or V _{SS} through resistor.
P25/SI0/SB0	10-A		
P26/SO0/SB1			
P27/ $\overline{\text{SCK0}}$			
P30/TO0	5-A		
P31/TO1			
P32/TO2			

Table 3-1. Input/Output Circuit Type of Each Pin (2/2)

Pin Name	Input/output Circuit Type	I/O	Recommended Connection when not Used
P33/T11	8-A	Input/output	Independently connected to V _{DD} or V _{SS} through resistor.
P34/T12			
P35/PCL	5-A		
P36/BUZ			
P37			
P70/SI2/RxD	8-A		
P71/SO2/TxD	5-A		
P72/SCK2/ASCK	8-A		
P80/S39 to P87/S32	17-A		
P90/S31 to P97/S24			
P100 to P103	5-A		
P110 to P117	5-D		Independently connected to V _{DD} through resistor.
S0 to S23	17		Output
COM0 to COM3	18		
V _{LC0} to V _{LC2}	—	—	
BIAS	—	—	
RESET	2	Input	—
XT2	16	—	Leave open.
AV _{REF}	—		Connected to V _{SS} .
AV _{DD}			Connected to V _{DD} .
AV _{SS}			Connected to V _{SS} .
IC			Connected directly to V _{SS} .

Figure 3-1. Pin Input/Output Circuits (1/2)

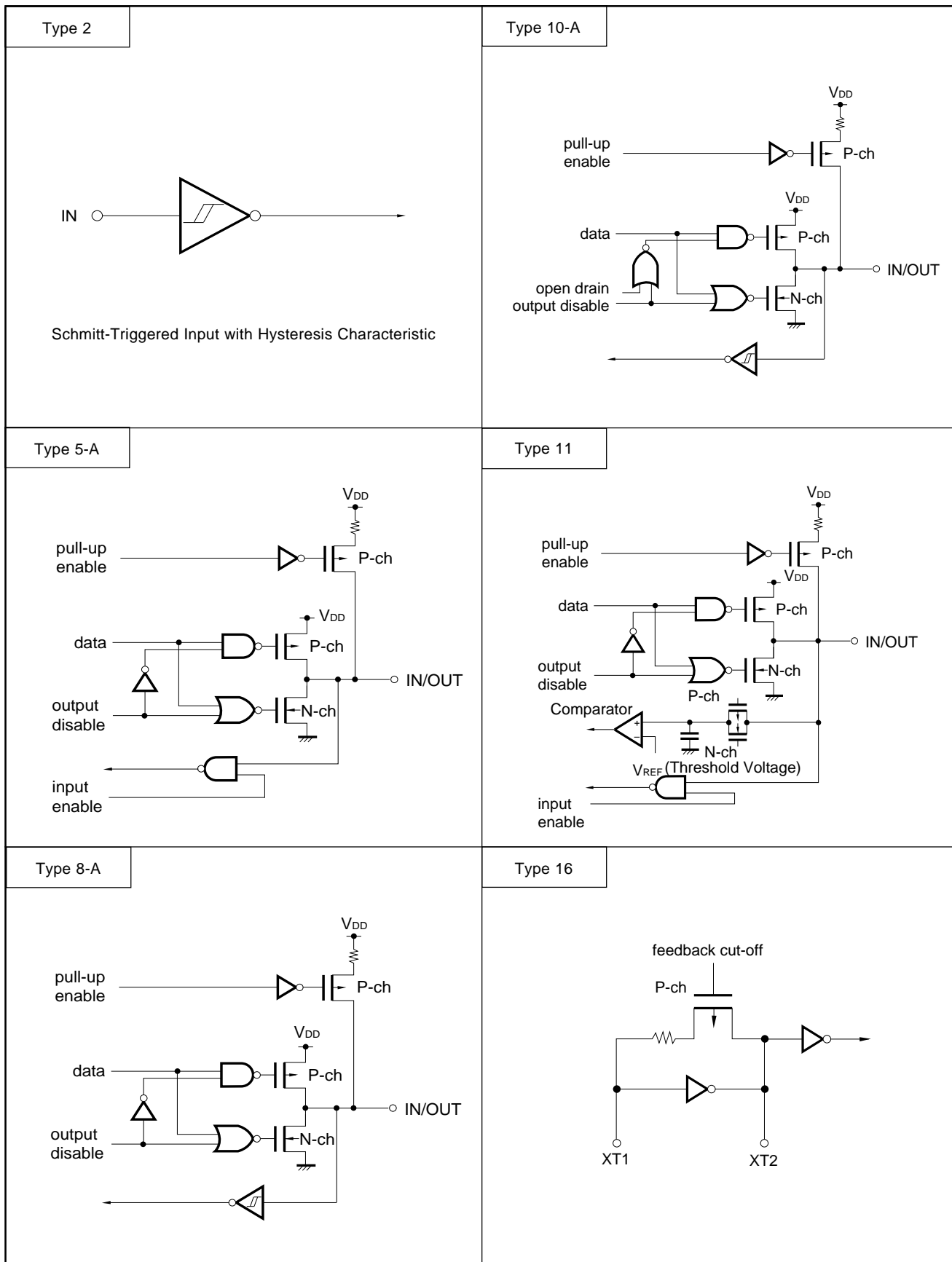
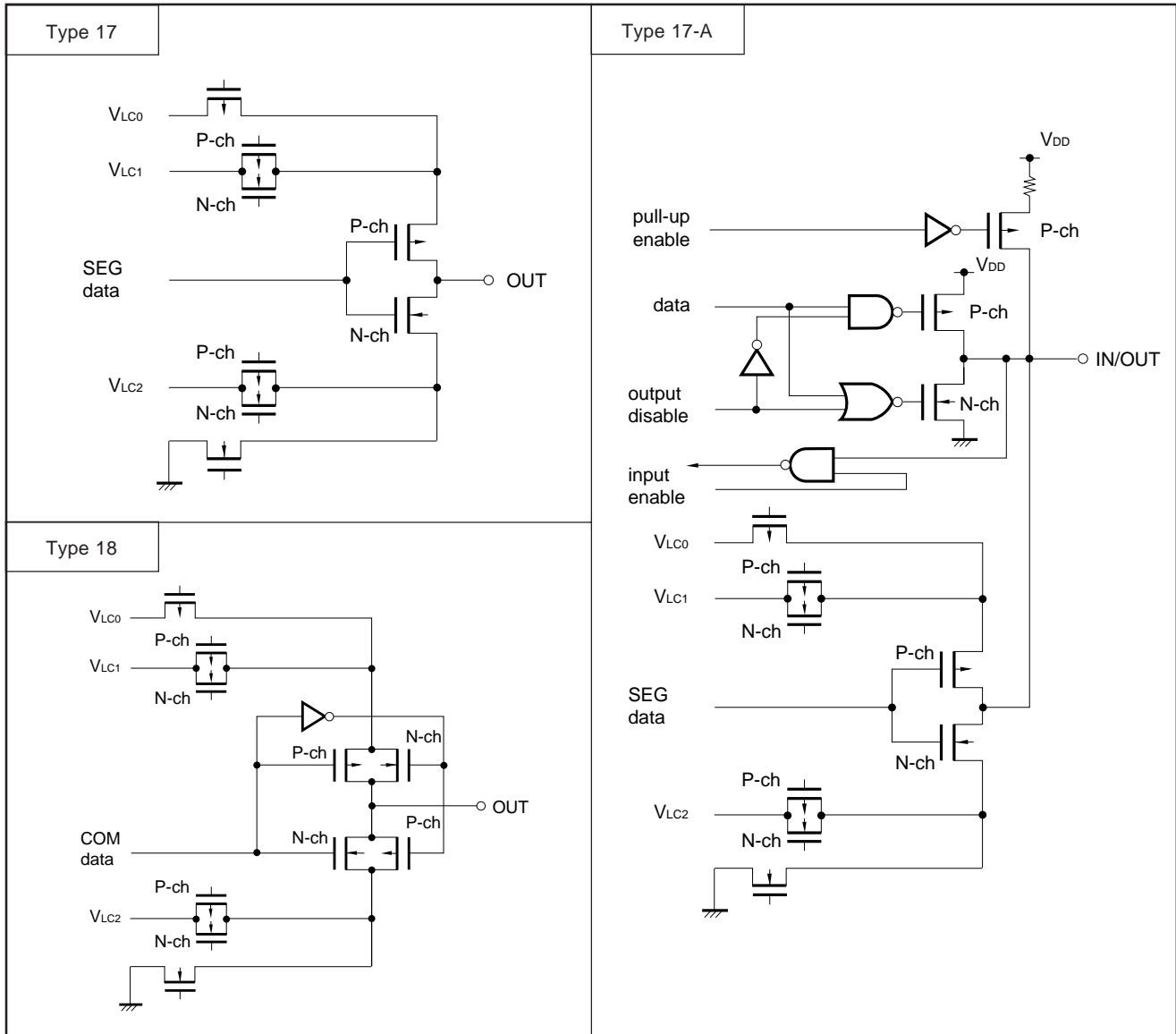


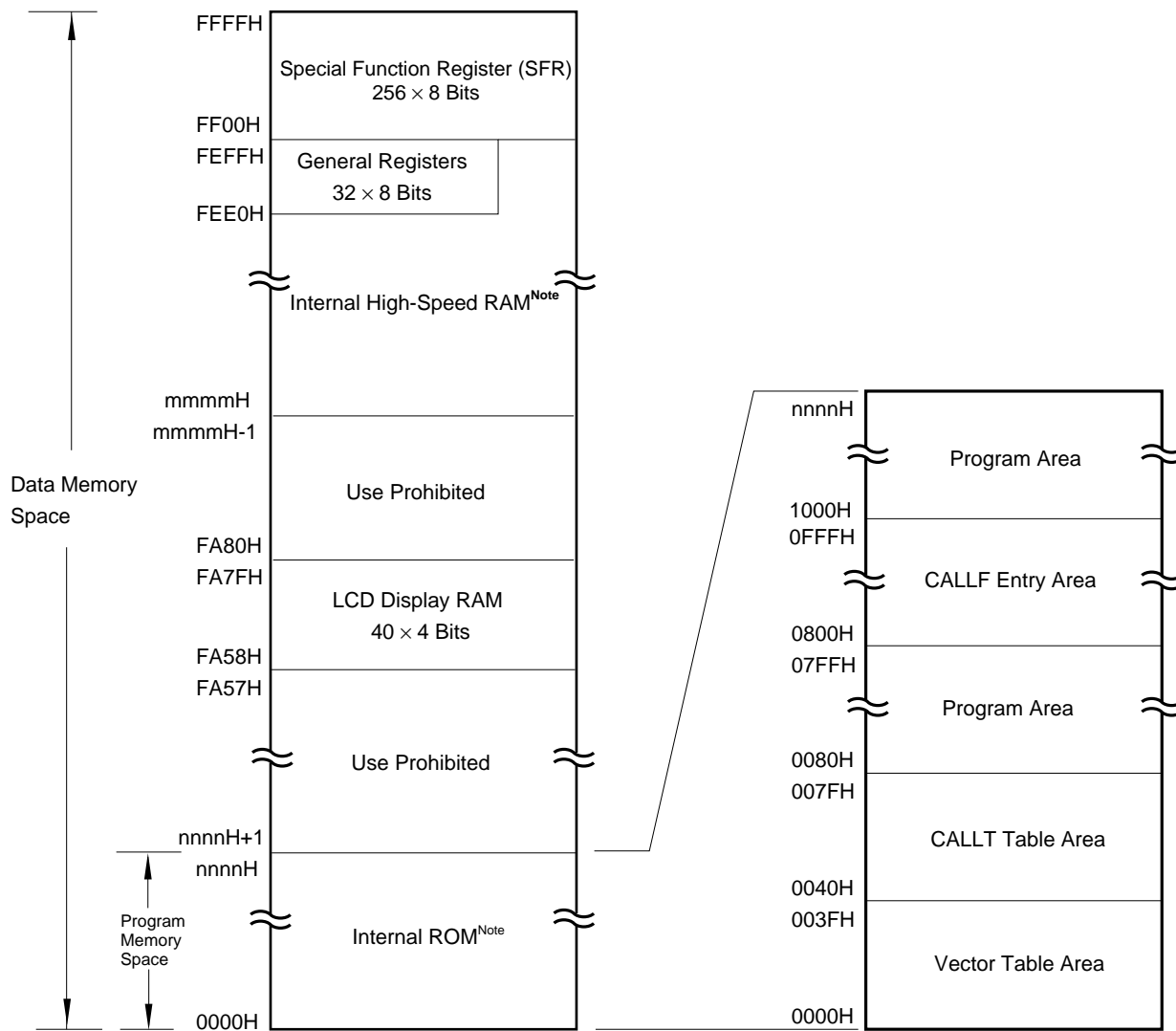
Figure 3-1. Pin Input/Output Circuits (2/2)



4. MEMORY SPACE

The memory map of μPD78062/78063/78064 is shown in Figure 4-1.

Figure 4-1. Memory Map



Note The Internal ROM and Internal High-Speed RAM capacities differ depending on the product. (refer to the following table.)

Product Name	Last Address of Internal ROM n n n n H	Start Address of Internal High-Speed RAM m m m m H
μPD78062	3FFFH	FD00H
μPD78063	5FFFH	FB00H
μPD78064	7FFFH	

5. PERIPHERAL HARDWARE FUNCTION FEATURE

5.1 Port

There are two kinds of I/O port.

• CMOS input (P00, P07)	: 2
• CMOS input/output (P01 to P05, Port 1 to 3, 7 to 11)	: 55
Total	: 57

Table 5-1. Functions of Ports

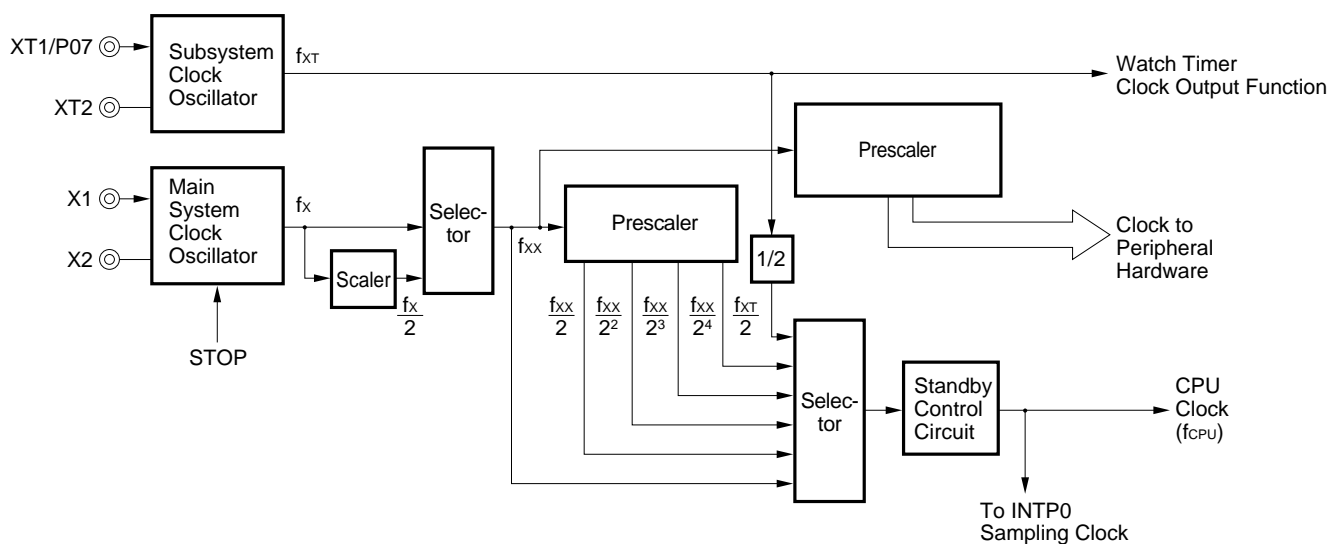
Name	Pin Name	Function
Port 0	P00, P07	Dedicated input port
	P01 to P05	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software .
Port 1	P10 to P17	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software .
Port 2	P25 to P27	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software .
Port 3	P30 to P37	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software.
Port 7	P70 to P72	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software.
Port 8	P80 to P87	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software. Input/output port/segment signal output function specifiable in 2-bit units by LCD control register (LCDC).
Port 9	P90 to P97	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software. Input/output port/segment signal output function specifiable in 2-bit units by LCD control register (LCDC).
Port 10	P100 to P103	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software. Direct LED drive capability.
Port 11	P110 to P117	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software. Test flag (KRIF) is set to 1 by falling edge detection.

5.2 Clock Generator

There are two kinds of clocks, main system clock and subsystem clock.
The instruction execution time can also be changed.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (main system clock: in 5.0 MHz operation)
- 122 μs (subsystem clock: in 32.768 kHz operation)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer/Event Counter

Five timer/event counter channels are incorporated.

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2. Timer/Event Counter Types and Functions

		16-bit Timer/Event Counter	8-bit Timer/Event Counter	Watch Timer	Watchdog Timer
Type	Interval timer	1 channel	2 channels	1 channel	1 channel
	External event counter	1 channel	2 channels	–	–
Function	Timer output	1 output	2 outputs	–	–
	PWM output	1 output	–	–	–
	Pulse width measurement	2 inputs	–	–	–
	Square wave output	1 output	2 outputs	–	–
	One-shot pulse output	1 output	–	–	–
	Interrupt request	2	2	2	1
	Test input	–	–	1 input	–

Figure 5-2. 16-Bit Timer/Event Counter Block Diagram

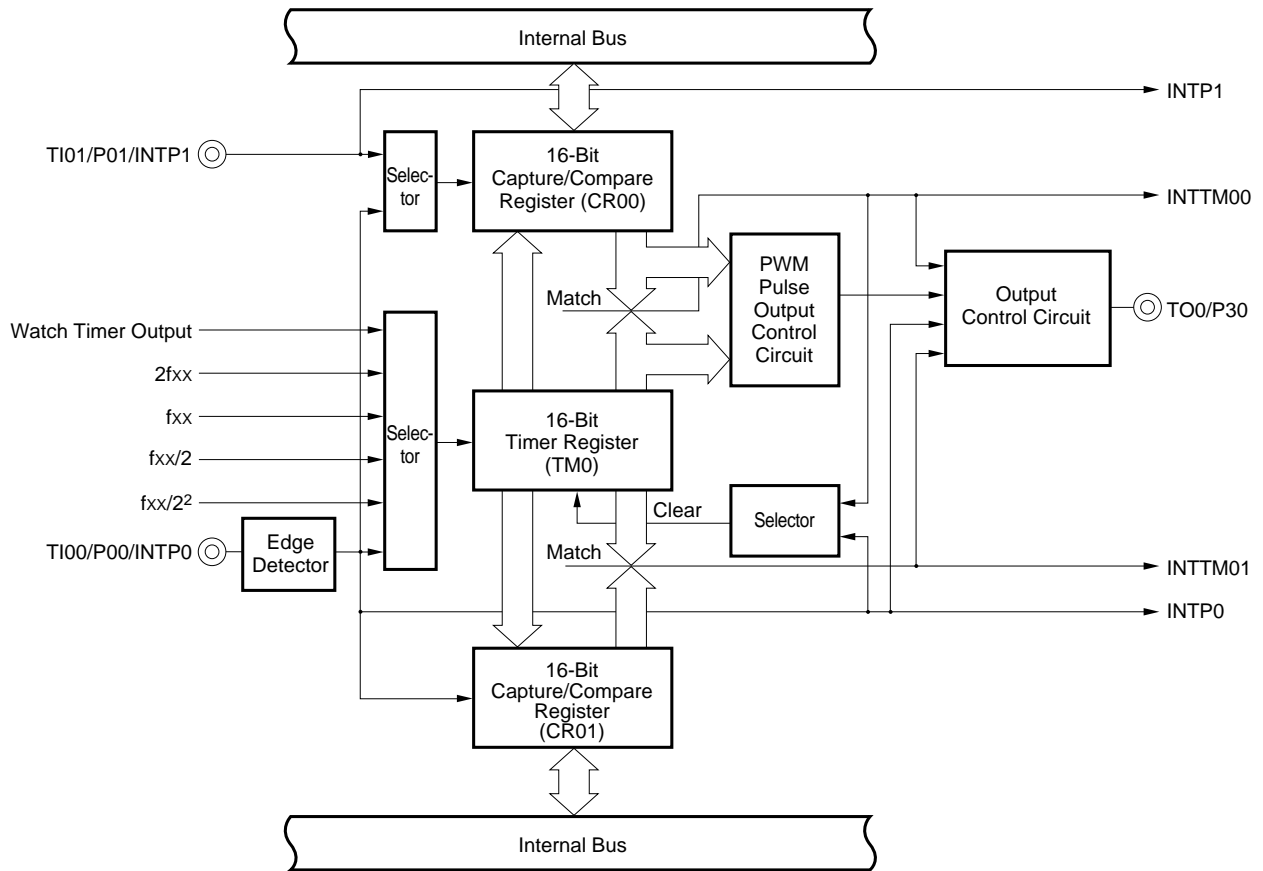


Figure 5-3. 8-Bit Timer/Event Counter Block Diagram

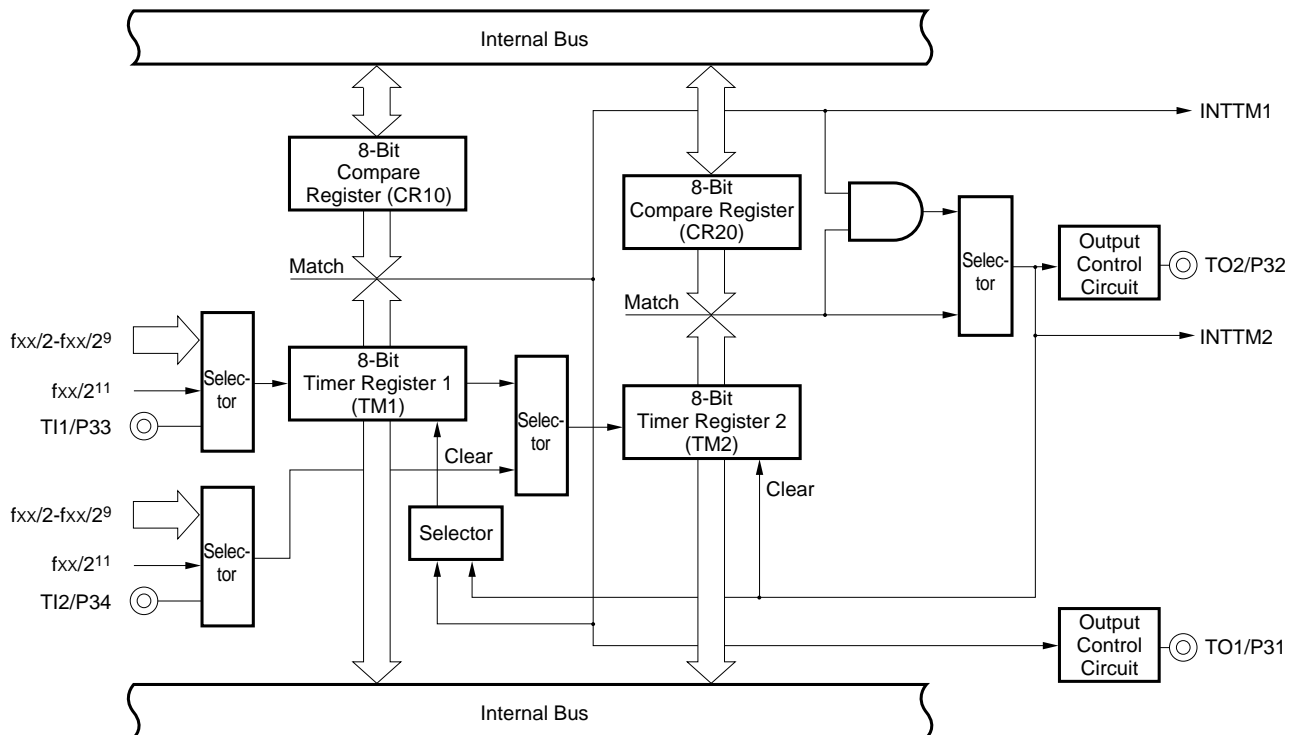


Figure 5-4. Watch Timer Block Diagram

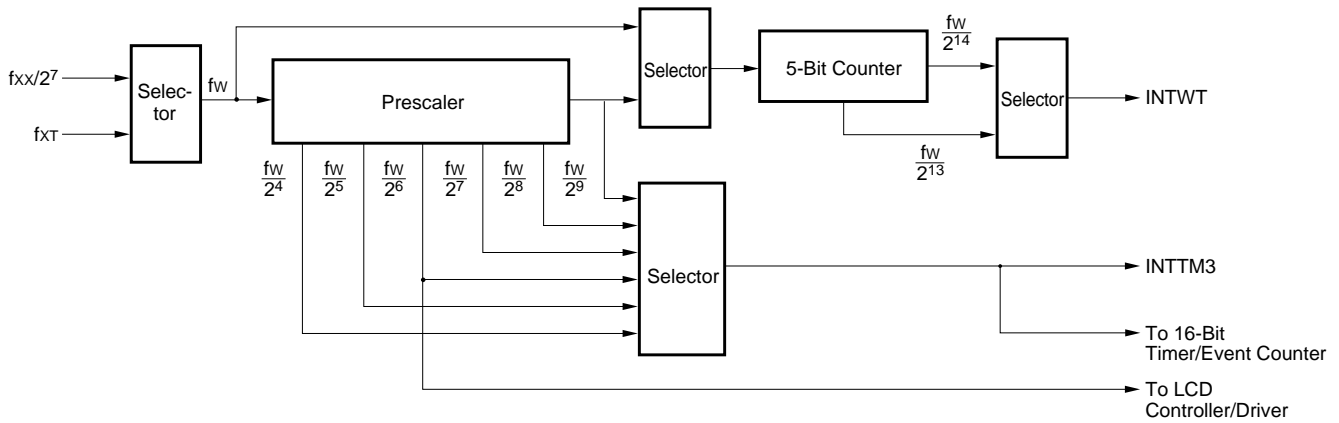
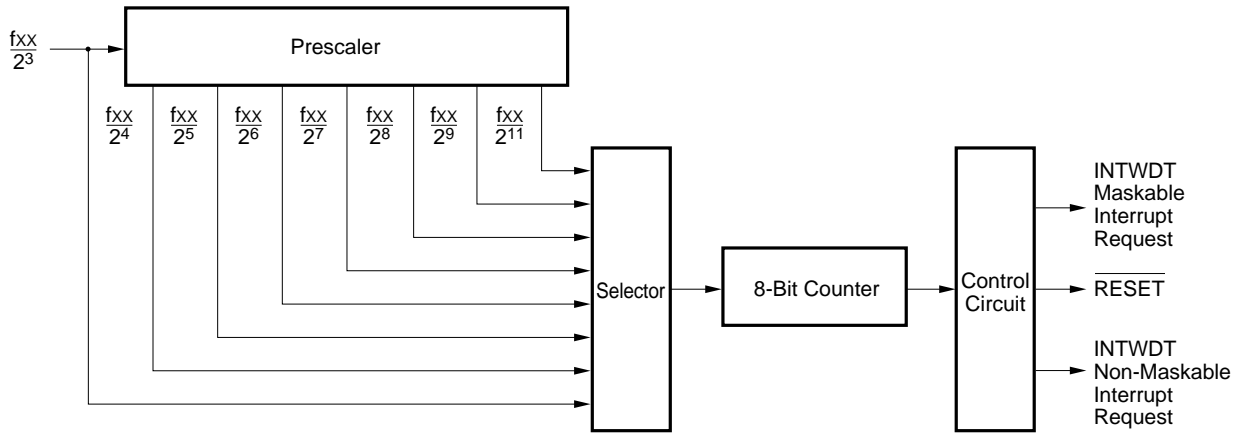


Figure 5-5. Watchdog Timer Block Diagram

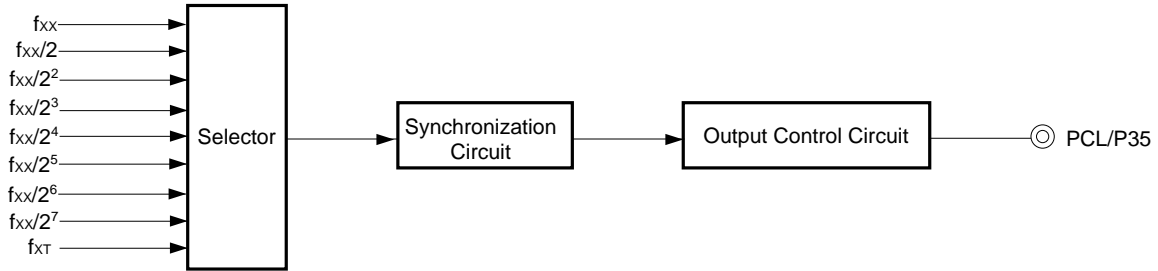


5.4 Clock Output Control Circuit

Clocks of the following frequency can be output as clock outputs.

- 19.5 kHz/39.1kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz/2.5 MHz/5.0 MHz (main system clock: in 5.0 kHz operation)
- 32.768 kHz (subsystem clock: in 32.768 kHz operation)

Figure 5-6. Clock Output Circuit Block Diagram

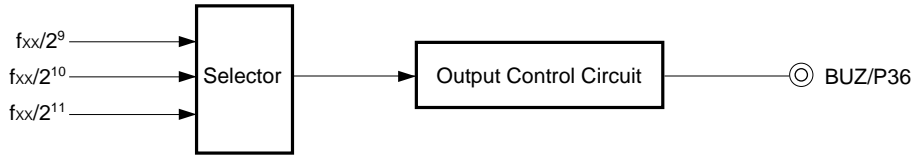


5.5 Buzzer Output Control Circuit

Clocks of the following frequency can be output as buzzer outputs.

- 1.2 kHz/2.4 kHz/4.9 kHz/9.8 kHz (main system clock : in 5.0 MHz operation)

Figure 5-7. Buzzer Output Control Circuit Block Diagram



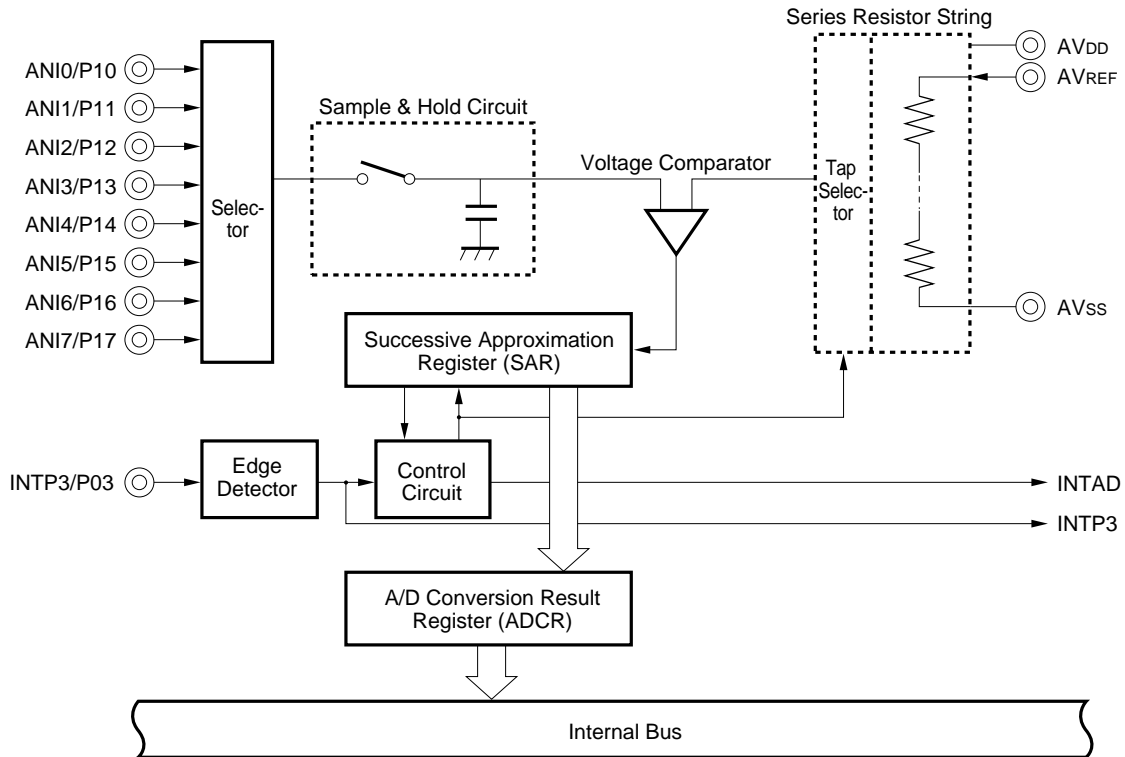
5.6 A/D Converter

Eight 8-bit resolution A/D converter channels are incorporated.

The following two types of start-up method are available.

- Hardware start
- Software start

Figure 5-8. A/D Converter Block Diagram



5.7 Serial Interface

Two clocked serial interface channels are incorporated.

- Serial interface channel 0
- Serial interface channel 2

Table 5-3. Serial Interface Channel Block Diagram

Function	Serial Interface Channel 0	Serial Interface Channel 2
3-wire serial I/O mode	○ (MSB/LSB-first switchable)	○ (MSB/LSB-first switchable)
SBI (serial bus interface) mode	○ (MSB-first)	—
2-wire serial I/O mode	○ (MSB-first)	—
Asynchronous serial interface (UART) mode	—	○ (Dedicated baud rate generator incorporated)

Figure 5-9. Serial Interface Channel 0 Block Diagram

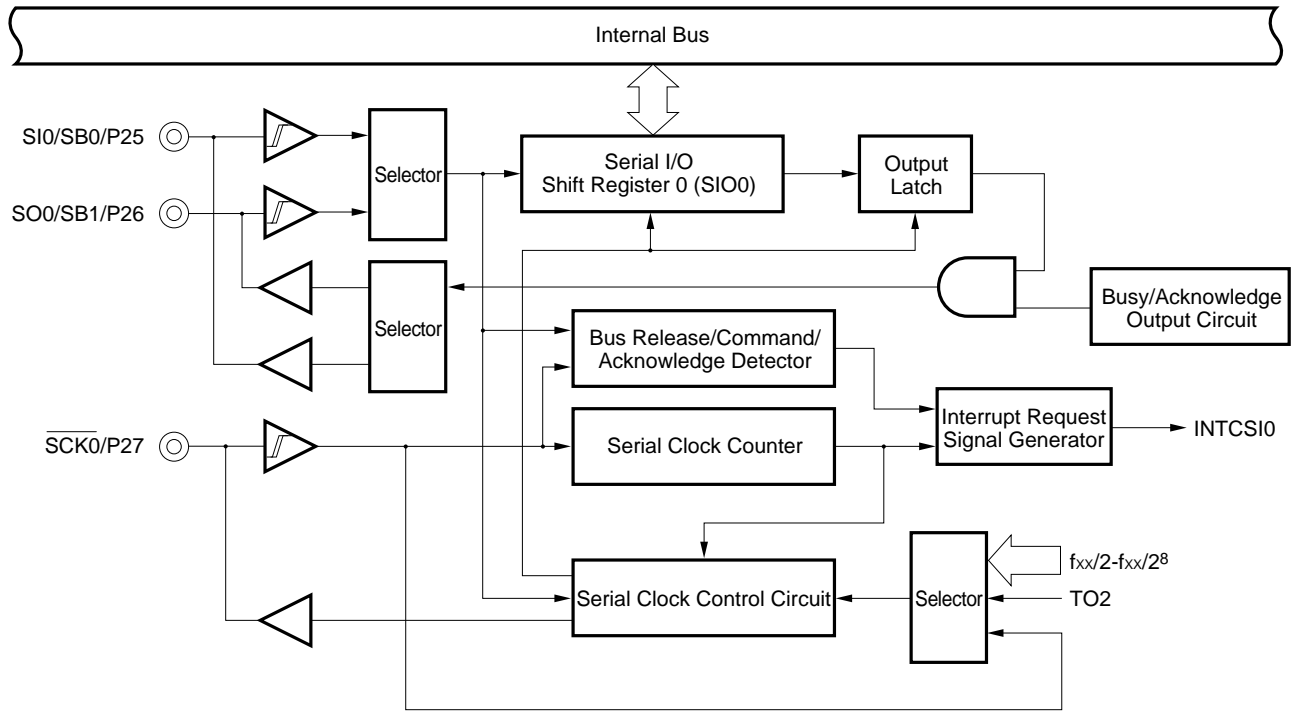
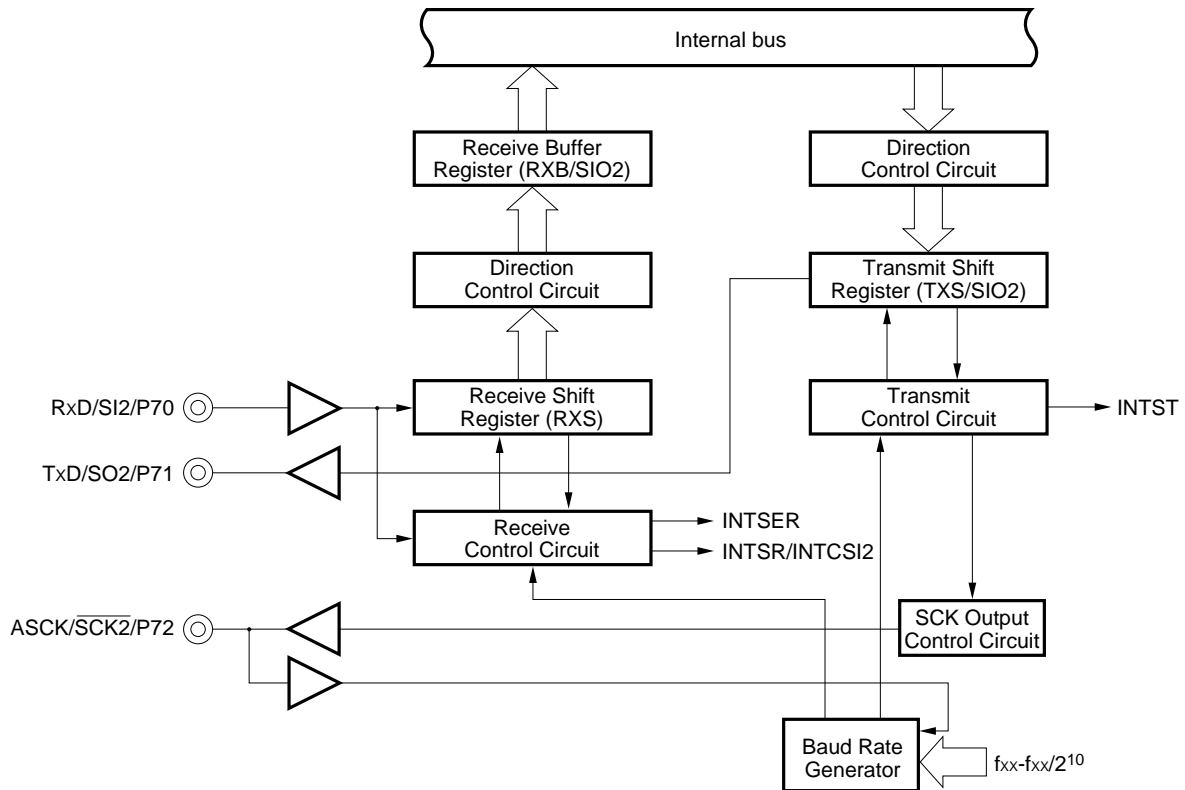


Figure 5-10. Serial Interface Channel 2 Block Diagram



5.8 LCD Controller/Driver

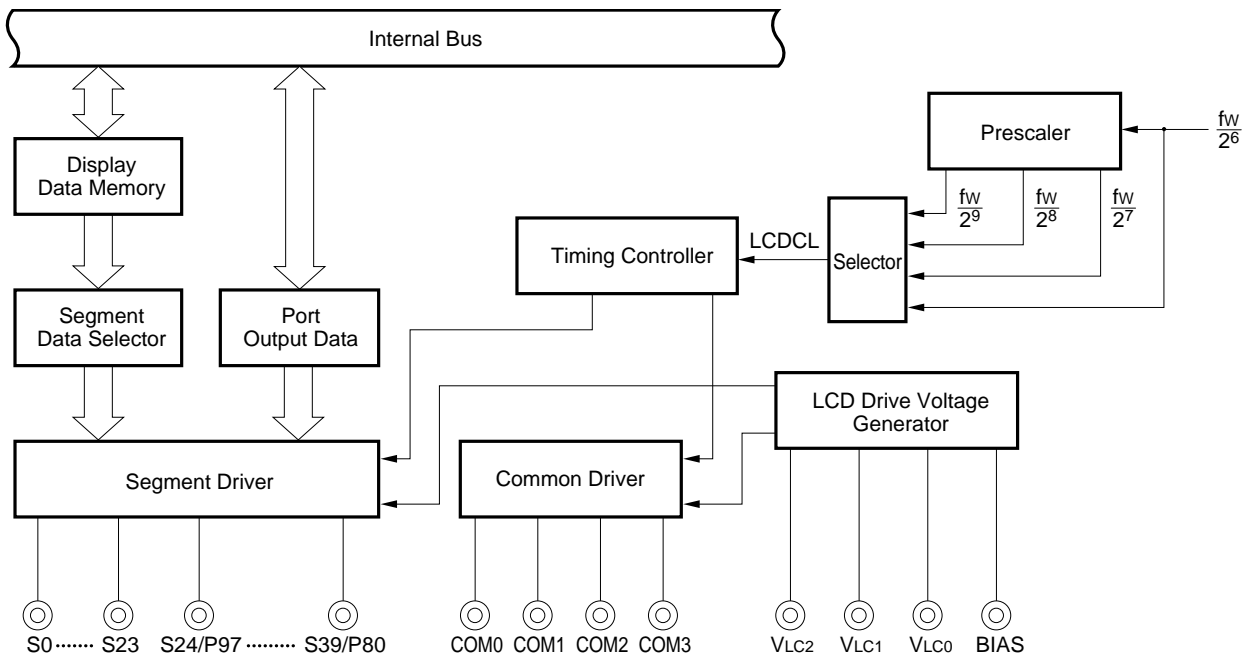
An LCD controller/driver with the following functions is incorporated.

- Selection of 5 types of display mode
- 16 of the segment signal of outputs can be switched to input/output ports in units of 2.
(P80/S39 to P87/S32, P90/S31 to P97/S24)

Table 5-4. Display Mode Types and Maximum Number of Display Pixels

Bias Method	Time Multiplexing	Common Signal Used	Maximum Number of Display Pixels
—	Static	COM0 (COM1 to COM3)	40 (40 segments × 1 common)
1/2	2	COM0, COM1	80 (40 segments × 2 commons)
	3	COM0 to COM2	120 (40 segments × 3 commons)
1/3	3	COM0 to COM2	120 (40 segments × 3 commons)
	4	COM0 to COM3	160 (40 segments × 4 commons)

Figure 5-11. LCD Controller/Driver Block Diagram



6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

6.1 Interrupt Functions

The following three types, 20 sources of interrupt functions are available:

- Non-maskable : 1
- Maskable : 18
- Software : 1

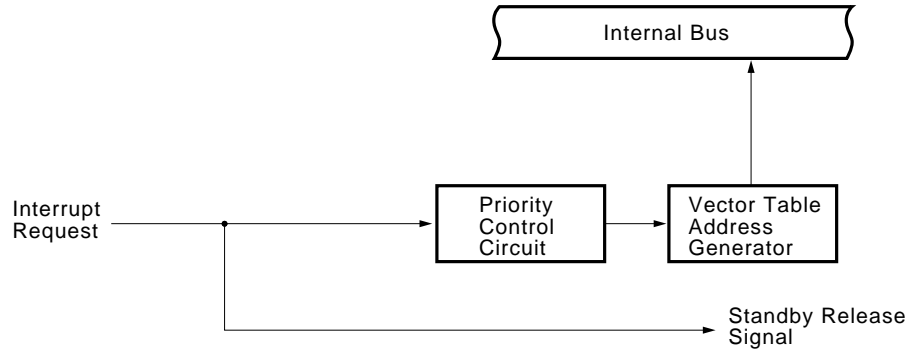
Table 6-1. Interrupt Source List

Interrupt Type	Default Priority ^{Note1}	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type ^{Note2}	
		Name	Trigger				
Non-maskable	—	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)	
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			External	0006H 0008H 000AH 000CH 000EH 0010H
	1	INTP0	Pin input edge detection	(D)	(D)		
	2	INTP1					
	3	INTP2					
	4	INTP3					
	5	INTP4					
	6	INTP5					
	7	INTCSI0	Serial interface channel 0 transfer termination			Internal	0014H
	8	INTSER	Serial interface channel 2 UART reception error generation	0018H			
	9	INTSR	Serial interface channel 2 UART reception termination	001AH			
		INTCSI2	Serial interface channel 2 3-wire transfer termination				
	10	INTST	Serial interface channel 2 UART transmission termination	001CH			
	11	INTTM3	Reference time interval signal from watch timer	001EH			
	12	INTTM00	16-bit timer register and capture/compare register (CR00) match signal generation	0020H			
	13	INTTM01	16-bit timer register and capture/compare register (CR01) match signal generation	0022H			
	14	INTTM1	8-bit timer/event counter 1 match signal generation	0024H			
	15	INTTM2	8-bit timer/event counter 2 match signal generation	0026H			
16	INTAD	A/D converter conversion termination	0028H				
Software	—	BRK	BRK instruction execution	—	003EH	(E)	

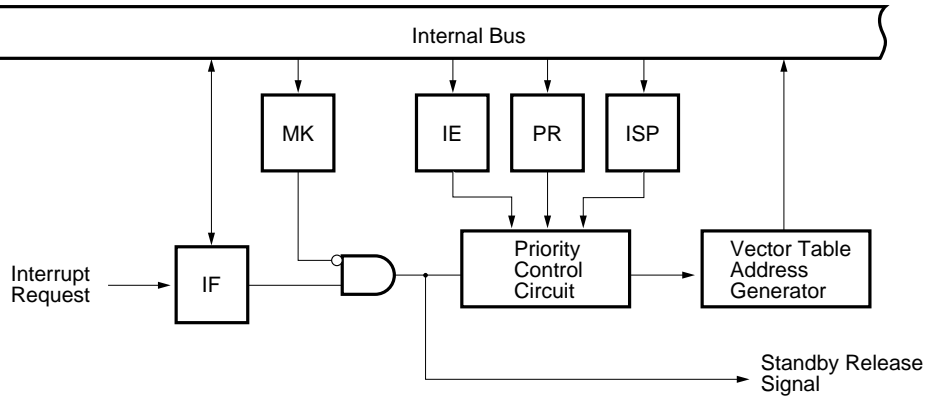
- Notes**
1. Default priority is a priority order when more than one maskable interrupt request is generated simultaneously. 0 is the highest and 16 the lowest.
 2. Basic configuration types (A) to (E) correspond to those shown in Figure 6-1.

Figure 6-1. Basic Configuration of Interrupt Functions (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTPO)

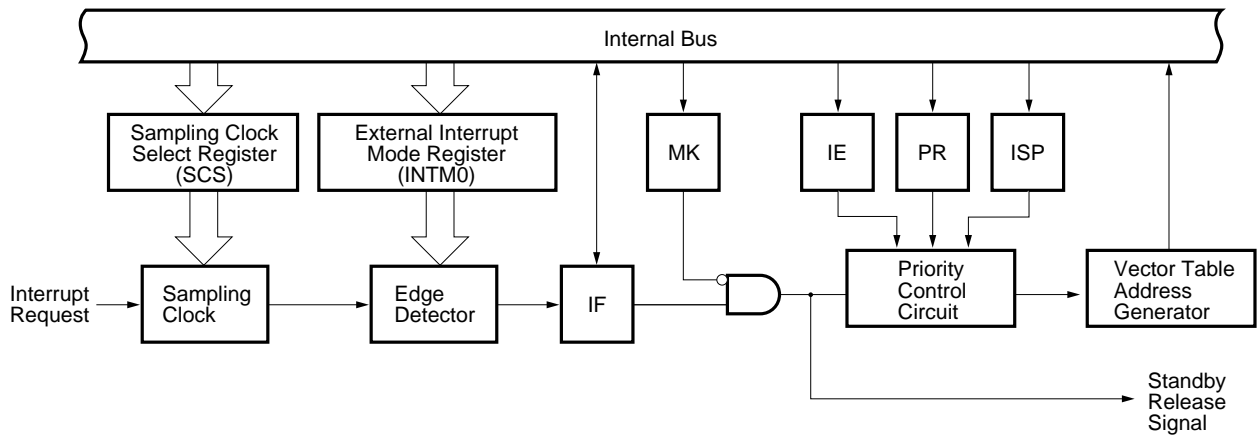
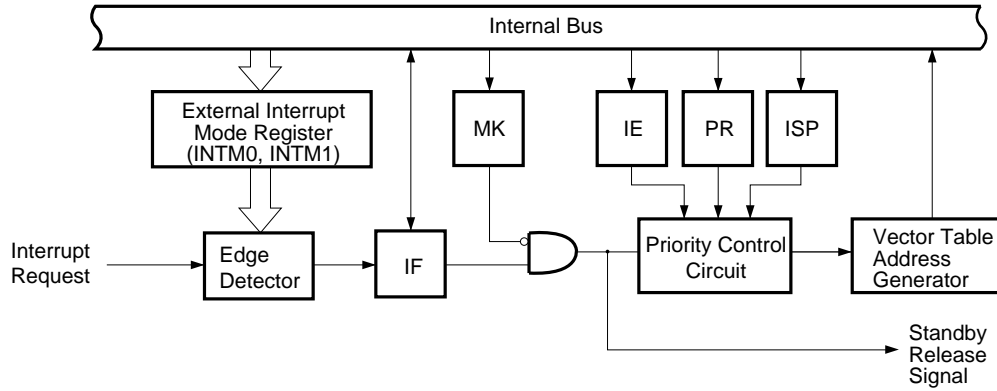
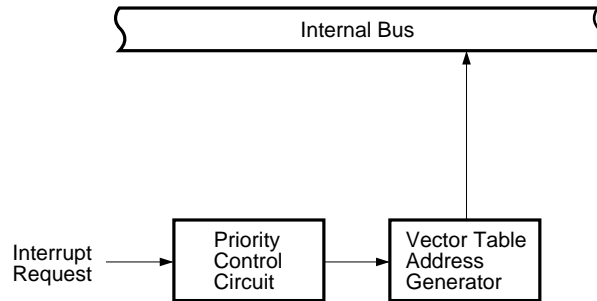


Figure 6-1. Basic Configuration of Interrupt Functions (2/2)

(D) External maskable interrupt (except INTPO)



(E) Software interrupt



- IF : Interrupt request flag
- IE : Interrupt enable flag
- ISP : In-service priority flag
- MK : Interrupt mask flag
- PR : Priority specification flag

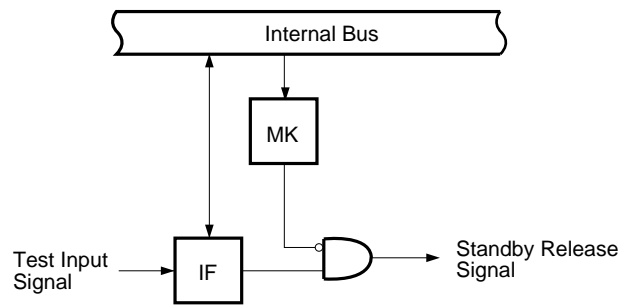
6.2 Test Functions

There are two sources of test functions as shown in Table 6-2.

Table 6-2. Test Input Source List

Test Input Source		Internal/External
Name	Trigger	
INTWT	Watch timer overflow	Internal
INTPT11	Port 11 falling edge detection	External

Figure 6-2. Basic Configuration of Test Function



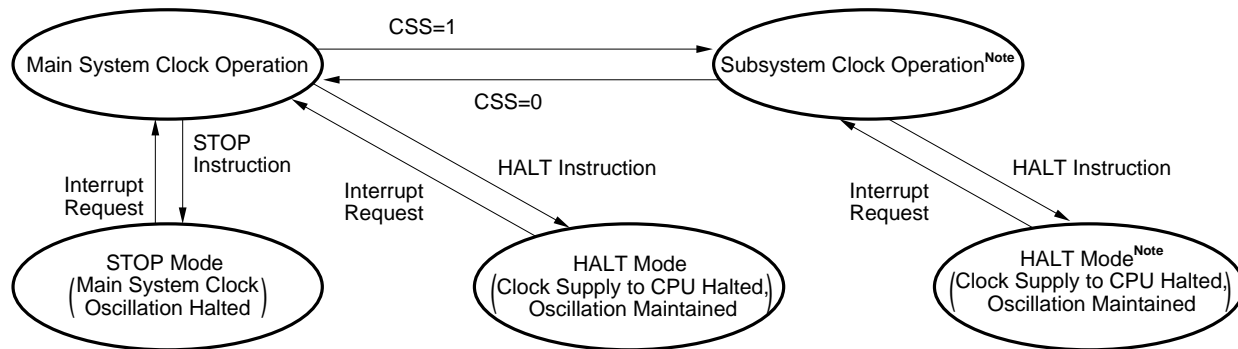
IF : Test input flag
 MK : Test mask flag

7. STANDBY FUNCTION

The standby function is a function to reduce the consumption current and there are the following two kinds of standby functions.

- HALT mode : Halts CPU operating clock and can reduce average consumption current by the intermittent operation along with the normal operation.
- STOP mode : Halts main system clock oscillation. Halts all operations with the main system clock and sets ultra-low consumption current state with subsystem clock only.

Figure 7-1. Standby Function



Note Halting the main system clock enables the consumption current to be reduced.
 When the CPU is operated by the subsystem clock, the main system clock should be halted by setting the bit 7 (MCC) of the processor clock control register (PCC).
 The STOP instruction is not available.

Caution When the main system clock is stopped and the system is operated by the subsystem clock, the main system clock should be returned to after securing the oscillation stabilization time in software.

8. RESET FUNCTION

There are the following two kinds of resetting methods.

- External reset by RESET pin.
- Internal reset by watchdog timer hung-up time detection.

9. INSTRUCTION SET

(1) 8-bit instruction

MOV, XCH, ADD, ADDC, SUB, SUBS, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

2nd operand 1st operand	#byte	A	r ^{Note}	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL+B] [HL+C]	\$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
★ B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL+byte] [HL+B] [HL+C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instruction

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

2nd operand 1st operand	#word	AX	rp ^{Note}	sfrp	saddrp	!addr16	SP	None
A	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW ^{Note}						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp=BC, DE, HL

(3) Bit manipulation instruction

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

2nd operand 1st operand	A.bit	sfr.bit	saddr.bit	PSW.bits	[HL].bit	CY	\$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instruction/branch instruction

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DNZB

2nd Operand 1st Operand	AX	!addr16	!addr11	[addr5]	\$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC, BZ, BNZ
Compound Instruction					BT, BF, BTCLR DNZB

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

10. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Test Conditions		Rating	Unit
Supply voltage	V _{DD}			-0.3 to +7.0	V
	AV _{DD}			-0.3 to V _{DD} +0.3	V
	AV _{REF}			-0.3 to V _{DD} +0.3	V
	AV _{SS}			-0.3 to +0.3	V
Input voltage	V _I			-0.3 to V _{DD} +0.3	V
Output voltage	V _O			-0.3 to V _{DD} +0.3	V
Analog input voltage	V _{AN}	P10 to P17	Analog input pin	AV _{SS} -0.3 to AV _{REF} +0.3	V
Output current high	I _{OH}	1 pin		-10	mA
		Total for P00 to P05, P07, P10 to P17, P100, P101 & P110 to P117		-15	mA
		Total for P25 to P27, P30 to P37, P70 to P72, P80 to P87, P90 to P97, P102 & P103		-15	mA
Output current low	I _{OL} <small>Note</small>	1 pin	Peak value	30	mA
			r.m.s. value	15	mA
		Total for P00 to P05, P10 to P17, P100, P101 & P110 to P117	Peak value	100	mA
			r.m.s. value	70	mA
		Total for P30 to P37, P102 & P103	Peak value	100	mA
			r.m.s. value	70	mA
		Total for P25 to P27, P70 to P72, P80 to P87 & P90 to P97	Peak value	50	mA
			r.m.s. value	20	mA
Operating ambient temperature	T _A			-40 to +85	°C
Storage temperature	T _{stg}			-65 to +150	°C

Note The r.m.s. value should be calculated as follows: [r.m.s. value] = [Peak value] × √Duty

Caution The product quality may be damaged even if a value of only one of the above parameters exceeds the absolute maximum rating or any value exceeds the absolute maximum rating for an instant. That is, the absolute maximum rating is a rating value which may cause a product to be damaged physically. The absolute maximum rating values must therefore be observed in using the product.

Remark Unless otherwise specified, the characteristics of dual-function pins are the same as those of port pins.

Capacitance (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{IN}	f = 1 MHz unmeasured pins returned to 0 V.			15	pF
Output capacitance	C _{OUT}				15	pF
I/O capacitance	C _{IO}				15	pF

Main System Clock Oscillator Characteristics (T_A = -40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Oscillator	Recommended circuit	Parameter	Test conditions	MIN.	TYP.	MAX.	Unit
Ceramic oscillator		Oscillator frequency (f _x) ^{Note1}	V _{DD} = Oscillator voltage range	1		5	MHz
		Oscillation stabilization time ^{Note2}	After V _{DD} reaches oscillator voltage range MIN.			4	ms
Crystal resonator		Oscillator frequency (f _x) ^{Note1}		1		5	MHz
		Oscillation stabilization time ^{Note2}	V _{DD} = 4.5 to 6.0 V			10 30	ms
External clock		X1 input frequency (f _x) ^{Note1}		1.0		5.0	MHz
		X1 input high/low level width (t _{xH} , t _{xL})		85		500	ns

- Notes**
1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.
 2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- Wiring should be as short as possible.
 - Wiring should not cross other signal lines.
 - Wiring should not be placed close to a varying high current.
 - The potential of the oscillator capacitor ground should be the same as V_{SS}.
 - Do not ground it to the ground pattern in which a high current flows.
 - Do not fetch a signal from the oscillator.
2. If the main system clock oscillator is operated by the subsystem clock when the main system clock is stopped, reswitching to the main system clock should be performed after the stable oscillation time has been obtained by the program.

Subsystem Clock Oscillator Characteristics (T_A = -40 to +85°C, V_{DD} = 2.0 to 6.0 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillator frequency (f _{XT}) ^{Note1}		32	32.768	35	kHz
		Oscillation stabilization time ^{Note2}	V _{DD} = 4.5 to 6.0 V		1.2	2	s
External clock		XT1 input frequency (f _{XT}) ^{Note1}		32		100	kHz
		XT1 input high-/low-level width (t _{bXTH} /t _{bXTL})		5		15	μs

- Notes**
- Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.
 - Time required to stabilize oscillation after V_{DD} has reached the minimum oscillation voltage range.

Cautions 1. When using the subsystem clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- Wiring should be as short as possible.
 - Wiring should not cross other signal lines.
 - Wiring should not be placed close to a varying high current.
 - The potential of the oscillator capacitor ground should be the same as V_{SS}.
 - Do not ground it to the ground pattern in which a high current flows.
 - Do not fetch a signal from the oscillator.
2. The subsystem clock oscillator is designed as a low amplification circuit to provide low consumption current, causing misoperation by noise more frequently than the main system clock oscillation circuit. Special care should therefore be taken to wiring method when the subsystem clock is used.

Recommended Oscillator Constant

Main system clock: ceramic oscillator (T_A = -40 to +85 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Circuit Constant		Oscillator Voltage Range		Remarks
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
Murata Mfg. Co., Ltd.	CSA5.00MG	5.00	30	30	2.2	6.0	
	CST5.00MGW	5.00	Built-in	Built-in	2.7	6.0	
Matsushita Electronics Components Co., Ltd.	EF0GC5004A4	5.00	Built-in	Built-in	2.7	6.0	Lead type
	EF0EC5004A4	5.00	Built-in	Built-in	2.0	6.0	Round lead type
	EF0EN5004A4	5.00	33	33	2.7	6.0	Lead type
	EF0S5004B5	5.00	Built-in	Built-in	2.7	6.0	Chip type
Kyocera Corporation	KBR-5.0MSA	5.00	33	33	2.7	6.0	Lead type
	PBRC5.00A	5.00	33	33	2.7	6.0	Chip type
	KBR-5.0MKS	5.00	Built-in	Built-in	2.7	6.0	Lead type
	KBR-5.0MWS	5.00	Built-in	Built-in	2.7	6.0	Chip type

Subsystem clock: crystal resonator (T_A = -40 to +60 °C)

Manufacturer	Product Name	Frequency (kHz)	Recommended Circuit Constant			Oscillator Voltage Range	
			C3 (pF)	C4 (pF)	R2 (kΩ)	MIN. (V)	MAX. (V)
Kyocera Corporation	KF-38G-12P0200 ^{Note} (Load capacitance 12 pF)	32.768	15	22	220	2.0	6.0

★ **Note** KF-38G-12P0200 is a maintenance product.

Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation. However, they do not guarantee accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency in the application circuit. For this, it is necessary to directly contact the manufacturer of the resonator being used.

DC Characteristics ($T_A = -40$ to $+85$ °C, $V_{DD} = 2.0$ to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH1}	P10 to P17, P30 to P32, P35 to P37, P80 to P87, P90 to P97, P100 to P103	$V_{DD} = 2.7$ to 6.0 V	$0.7 V_{DD}$		V_{DD}	V
				$0.8 V_{DD}$		V_{DD}	V
	V_{IH2}	P00 to P05, P25 to P27, P33, P34, P70 to P72, P110 to P117, \overline{RESET}	$V_{DD} = 2.7$ to 6.0 V	$0.8 V_{DD}$		V_{DD}	V
				$0.85 V_{DD}$		V_{DD}	V
	V_{IH3}	X1, X2	$V_{DD} = 2.7$ to 6.0 V	$V_{DD}-0.5$		V_{DD}	V
				$V_{DD}-0.2$		V_{DD}	V
	V_{IH4}	XT1/P07, XT2	$4.5 \text{ V} \leq V_{DD} \leq 6.0 \text{ V}$	$0.8 V_{DD}$		V_{DD}	V
			$2.7 \text{ V} \leq V_{DD} < 4.5 \text{ V}$	$0.9 V_{DD}$		V_{DD}	V
			$2.0 \text{ V} \leq V_{DD} < 2.7 \text{ V}^{\text{Note}}$	$0.9 V_{DD}$		V_{DD}	V
	Input voltage low	V_{IL1}	P10 to P17, P30 to P32, P35 to P37, P80 to P87, P90 to P97, P100 to P103	$V_{DD} = 2.7$ to 6.0 V	0		$0.3 V_{DD}$
				0		$0.2 V_{DD}$	V
V_{IL2}		P00 to P05, P25 to P27, P33, P34, P70 to P72, P110 to P117, \overline{RESET}	$V_{DD} = 2.7$ to 6.0 V	0		$0.2 V_{DD}$	V
				0		$0.15 V_{DD}$	V
V_{IL3}		X1, X2	$V_{DD} = 2.7$ to 6.0 V	0		0.4	V
				0		0.2	V
V_{IL4}		XT1/P07, XT2	$4.5 \text{ V} \leq V_{DD} \leq 6.0 \text{ V}$	0		$0.2 V_{DD}$	V
			$2.7 \text{ V} \leq V_{DD} < 4.5 \text{ V}$	0		$0.1 V_{DD}$	V
			$2.0 \text{ V} \leq V_{DD} < 2.7 \text{ V}^{\text{Note}}$	0		$0.1 V_{DD}$	V
Output voltage high		V_{OH}	$V_{DD} = 4.5$ to 6.0 V, $I_{OH} = -1$ mA		$V_{DD}-1.0$		V_{DD}
	$I_{OH} = -100 \mu\text{A}$		$V_{DD}-0.5$		V_{DD}	V	
Output voltage low	V_{OL1}	P100 to P103	$V_{DD} = 4.5$ to 6.0 V, $I_{OL} = 15$ mA		0.4	2.0	V
		P00 to P05, P10 to P17, P25 to P27, P30 to P37, P70 to P72, P80 to P87, P90 to P97, P110 to P117	$V_{DD} = 4.5$ to 6.0 V, $I_{OL} = 1.6$ mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{SCK0}$	$4.5 \text{ V} \leq V_{DD} \leq 6.0 \text{ V}$, open-drain, pulled high ($R = 1 \text{ k}\Omega$)			$0.2 V_{DD}$	V
	V_{OL3}	$I_{OL} = 400 \mu\text{A}$				0.5	V

Note When P07/XT1 is used as P07, the inverse phase of P07 should be input to XT2.

Remark Unless otherwise specified, the characteristics of dual-function pins are the same as those of port pins.

DC Characteristics (T_A = -40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current high	I _{LH1}	V _I = V _{DD}	P00 to P05, P10 to P17, P25 to P27, P30 to P37, P70 to P72, P80 to P87, P90 to P97, P100 to P103, P110 to P117			3	μA
	I _{LH2}		X1, X2, XT1/P07, XT2			20	μA
Input leakage current low	I _{LIL1}	V _I = 0 V	P00 to P05, P10 to P17, P25 to P27, P30 to P37, P70 to P72, P80 to P87, P90 to P97, P100 to P103, P110 to P117			-3	μA
	I _{LIL2}		X1, X2, XT1/P07, XT2			-20	μA
Output leakage current high	I _{LOH}	V _O = V _{DD}				3	μA
Output leakage current low	I _{LOL}	V _O = 0 V				-3	μA
Software pull-up resistor	R	V _I = 0 V, P01 to P05, P10 to P17, P25 to P27, P30 to P37, P70 to P72, P80 to P87, P90 to P97, P100 to P103, P110 to P117	4.5 V ≤ V _{DD} ≤ 6.0 V	15	40	90	kΩ
			2.7 V ≤ V _{DD} < 4.5 V	20		500	kΩ
Supply current ^{Note1}	I _{DD1}	5.00 MHz, Crystal oscillation (f _{xx} = 2.5 MHz) ^{Note2} operating mode	V _{DD} = 5.0 V ± 10 % ^{Note4}		4	12	mA
			V _{DD} = 3.0 V ± 10 % ^{Note5}		0.6	1.8	mA
			V _{DD} = 2.2 V ± 10 % ^{Note5}		0.35	1.05	mA
	I _{DD2}	5.00 MHz, Crystal oscillation (f _{xx} = 5.0 MHz) ^{Note3} operating mode	V _{DD} = 5.0 V ± 10 % ^{Note4}		6.5	19.5	mA
			V _{DD} = 3.0 V ± 10 % ^{Note5}		0.8	2.4	mA
			V _{DD} = 2.2 V ± 10 %		280	840	μA
	I _{DD2}	5.00 MHz, Crystal oscillation (f _{xx} = 2.5 MHz) ^{Note2} HALT mode	V _{DD} = 5.0 V ± 10 %		1.4	4.2	mA
			V _{DD} = 3.0 V ± 10 %		500	1500	μA
V _{DD} = 2.2 V ± 10 %				280	840	μA	
I _{DD2}	5.00 MHz, Crystal oscillation (f _{xx} = 5.0 MHz) ^{Note3} HALT mode	V _{DD} = 5.0 V ± 10 %		1.6	4.8	mA	
		V _{DD} = 3.0 V ± 10 %		650	1950	μA	

- Notes**
1. Not including currents flowing in on-chip pull-up resistors or LCD split resistors.
 2. Main system clock f_{xx} = f_x/2 operation (when oscillation mode selection register (OSMS) is set to 00H)
 3. Main system clock f_{xx} = f_x operation (when OSMS is set to 01H)
 4. High-speed mode operation (when processor clock control register (PCC) is set to 00H)
 5. Low-speed mode operation (when PCC is set to 04H)

Remark Unless otherwise specified, the characteristics of dual-function pins are the same as those of port pins.

DC Characteristics (T_A = -40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply current ^{Note1}	I _{DD3}	32,768 kHz, Crystal oscillation operating mode ^{Note2}	V _{DD} = 5.0 V ± 10 %	60	120	μA
			V _{DD} = 3.0 V ± 10 %	32	64	μA
			V _{DD} = 2.2 V ± 10 %	24	48	μA
	I _{DD4}	32,768 kHz, Crystal oscillation HALT mode ^{Note2}	V _{DD} = 5.0 V ± 10 %	25	55	μA
			V _{DD} = 3.0 V ± 10 %	5	15	μA
			V _{DD} = 2.2 V ± 10 %	2.5	12.5	μA
	I _{DD5}	XT1 = V _{DD} STOP mode When feedback resistor is connected	V _{DD} = 5.0 V ± 10 %	1	30	μA
			V _{DD} = 3.0 V ± 10 %	0.5	10	μA
			V _{DD} = 2.2 V ± 10 %	0.3	10	μA
	I _{DD6}	XT1 = V _{DD} STOP mode When feedback resistor is disconnected	V _{DD} = 5.0 V ± 10 %	0.1	30	μA
			V _{DD} = 3.0 V ± 10 %	0.05	10	μA
			V _{DD} = 2.2 V ± 10 %	0.05	10	μA

- Notes**
1. Not including currents flowing in on-chip pull-up resistors or LCD split resistors.
 2. When the main system clock is stopped.

DC Characteristics (T_A = -10 to +85 °C)

(1) Static display mode (V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V _{LCD}			2.0		V _{DD}	V
LCD split resistor	R _{LCD}			60	100	150	kΩ
LCD output voltage deviation ^{Note} (common)	V _{ODC}	I _o = ±5 μA	2.0 V ≤ V _{LCD} ≤ V _{DD} V _{LCD0} = V _{LCD}	0		±0.2	V
LCD output voltage deviation ^{Note} (segment)	V _{ODS}	I _o = ±1 μA		0		±0.2	V

Note The voltage deviation is the difference from the output voltage corresponding to the ideal value of the segment and common outputs (V_{LCDn}; n = 0, 1, 2).

(2) 1/3 bias method (V_{DD} = 2.5 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V _{LCD}			2.5		V _{DD}	V
LCD split resistor	R _{LCD}			60	100	150	kΩ
LCD output voltage deviation ^{Note} (common)	V _{ODC}	I _o = ±5 μA	2.5 V ≤ V _{LCD} ≤ V _{DD} V _{LCD0} = V _{LCD}	0		±0.2	V
LCD output voltage deviation ^{Note} (segment)	V _{ODS}	I _o = ±1 μA		V _{LCD1} = V _{LCD} × 2/3 V _{LCD2} = V _{LCD} × 1/3	0		±0.2

Note The voltage deviation is the difference from the output voltage corresponding to the ideal value of the segment and common outputs (V_{LCDn}; n = 0, 1, 2).

(3) 1/2 bias method (V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V _{LCD}			2.7		V _{DD}	V
LCD split resistor	R _{LCD}			60	100	150	kΩ
LCD output voltage deviation ^{Note} (common)	V _{ODC}	I _o = ±5 μA	2.7 V ≤ V _{LCD} ≤ V _{DD} V _{LCD0} = V _{LCD}	0		±0.2	V
LCD output voltage deviation ^{Note} (segment)	V _{ODS}	I _o = ±1 μA		V _{LCD1} = V _{LCD} × 1/2 V _{LCD2} = V _{LCD1}	0		±0.2

Note The voltage deviation is the difference from the output voltage corresponding to the ideal value of the segment and common outputs (V_{LCDn}; n = 0, 1, 2).

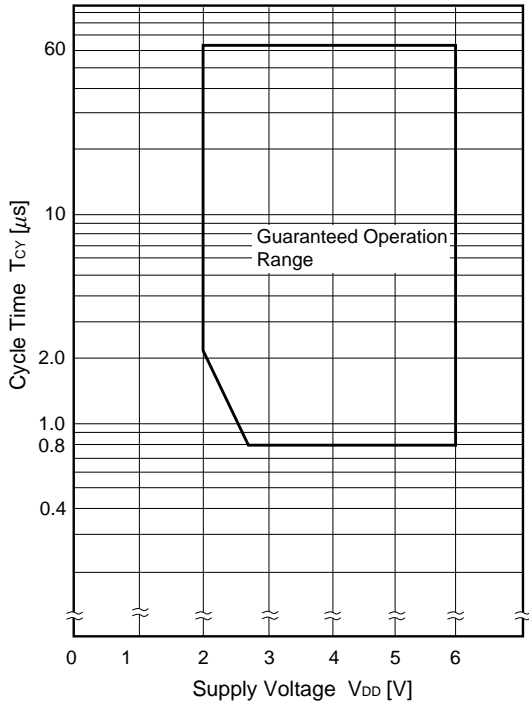
AC Characteristics (T_A = -40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

(1) Basic operation

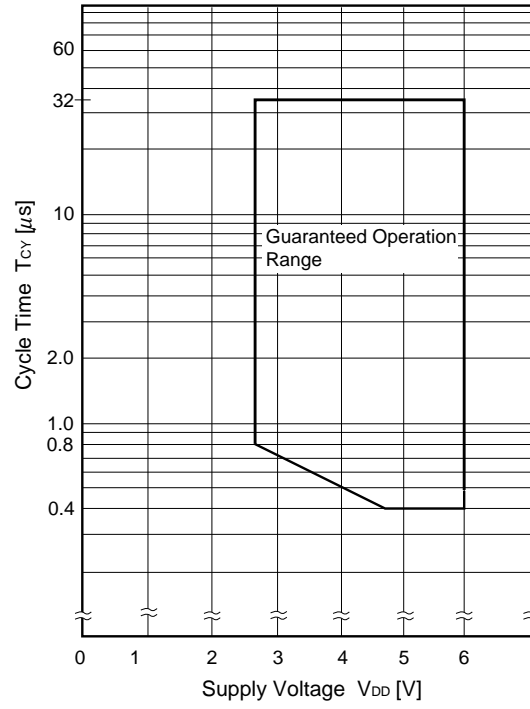
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Cycle time (Minimum instruction execution time)	T _{CY}	Operating on main system clock (f _{XX} = 2.5 MHz) ^{Note1}	V _{DD} = 2.7 to 6.0 V	0.8		64	μs
				2.2		64	μs
		Operating on main system clock (f _{XX} = 5.0 MHz) ^{Note2}	4.5 ≤ V _{DD} ≤ 6.0 V	0.4		32	μs
			2.7 ≤ V _{DD} < 4.5 V	0.8		32	μs
		Operating on subsystem clock	40 ^{Note3}	122	125	μs	
★ TI00 input frequency	f _{TI00}	t _{TI00} = t _{TIH00} + t _{TIL00}	0		1/t _{TI00}	MHz	
★ TI00 input high/ low-level width	f _{TIH00}	4.5 V ≤ V _{DD} ≤ 6.0 V	2/f _{sam} +0.1 ^{Note 4}			μs	
	t _{TIL00}	2.7 V ≤ V _{DD} < 4.5 V	2/f _{sam} +0.2 ^{Note 4}			μs	
		2.0 V ≤ V _{DD} < 2.7 V	2/f _{sam} +0.5 ^{Note 4}			μs	
★ TI01 input high/ low-level width	f _{TIH01}	2.7 V ≤ V _{DD} ≤ 6.0 V	10			μs	
	t _{TIL01}		20			μs	
TI1, T12 input high/ low-level width	f _{TI1}	V _{DD} = 4.5 to 6.0 V	0		4	MHz	
			0		275	kHz	
TI1, T12 input high/ low-level width	t _{TIH1}	V _{DD} = 4.5 to 6.0 V	100			ns	
	t _{TIL1}		1.8			μs	
Interrupt input high/low-level width	t _{INTH} , t _{INTL}	INTP0	8/f _{sam} ^{Note4}			μs	
		INTP1 to INTP5, P110 to P117	V _{DD} = 2.7 to 6.0 V	10			μs
				20			μs
RESET low level width	t _{RSL}	V _{DD} = 2.7 to 6.0 V	10			μs	
			20			μs	

- Notes**
1. Main system clock f_{XX} = f_X/2 operation (when oscillation mode selection register (OSMS) is set to 00H)
 2. Main system clock f_{XX} = f_X operation (when OSMS is set to 01H)
 3. This is the value when the external clock is used. The value is 114 μs (min.) when the crystal resonator is used.
 4. In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register (SCS), selection of f_{sam} is possible between f_{XX}/2^N, f_{XX}/32, f_{XX}/64 and f_{XX}/128 (when N = 0 to 4).

T_{CY} vs V_{DD} (At main system clock $f_{XX} = f_X/2$ operation)



T_{CY} vs V_{DD} (At main system clock $f_{XX} = f_X$ operation)



(2) Serial Interface (T_A = -40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode (SCK0... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
SCK0 cycle time	t _{KCY1}	4.5 V ≤ V _{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V _{DD} < 4.5 V	1600			ns
			3200			ns
SCK0 high/low-level width	t _{KH1} , t _{KL1}	V _{DD} = 4.5 to 6.0 V	t _{KCY1} /2-50			ns
			t _{KCY1} /2-100			ns
SI0 setup time (to SCK0↑)	t _{SIK1}	4.5 V ≤ V _{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V _{DD} < 4.5 V	150			ns
			300			ns
SI0 hold time (from SCK0↑)	t _{KSI1}		400			ns
SO0 output delay time from SCK0↓	t _{KSO1}	C = 100 pF ^{Note}			300	ns

Note C is the load capacitance of SCK0, SO0 output line.

(ii) 3-wire serial I/O mode (SCK0...External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
SCK0 cycle time	t _{KCY2}	4.5 V ≤ V _{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V _{DD} < 4.5 V	1600			ns
			3200			ns
SCK0 high/low-level width	t _{KH2} , t _{KL2}	4.5 V ≤ V _{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V _{DD} < 4.5 V	800			ns
			1600			ns
SI0 setup time (to SCK0↑)	t _{SIK2}		100			ns
SI0 hold time (from SCK0↑)	t _{KSI2}		400			ns
SO0 output delay time from SCK0↓	t _{KSO2}	C = 100 pF ^{Note}			300	ns
SCK0 rise, fall time	t _{R2} , t _{F2}				1000	ns

Note C is the load capacitance of SO0 output line.

(iii) SBI mode ($\overline{\text{SCK0}}$...Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{KCY3}	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$		800			ns
				3200			ns
$\overline{\text{SCK0}}$ high/low-level width	t_{KH3}	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$		$t_{\text{KCY3}}/2-50$			ns
	t_{KL3}			$t_{\text{KCY3}}/2-150$			ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}\uparrow$)	t_{SIK3}	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}\uparrow$)	t_{KSI3}			$t_{\text{KCY3}}/2$			ns
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	t_{KSO3}	R = 1 kΩ , C = 100 pF ^{Note}	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	0		250	ns
				0		1000	ns
SB0, SB1 \downarrow from $\overline{\text{SCK0}}\uparrow$	t_{KSB}			t_{KCY3}			ns
$\overline{\text{SCK0}}\downarrow$ from SB0, SB1 \downarrow	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R and C are the load resistance and load capacitance of the $\overline{\text{SCK0}}$, SB0 and SB1 output line.

(iv) SBI mode ($\overline{\text{SCK0}}$...External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{KCY4}	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$		800			ns
				3200			ns
$\overline{\text{SCK0}}$ high/low-level width	t_{KH4}	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$		400			ns
	t_{KL4}			1600			ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}\uparrow$)	t_{SIK4}	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}\uparrow$)	t_{KSI4}			$t_{\text{KCY4}}/2$			ns
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	t_{KSO4}	R = 1 kΩ , C = 100 pF ^{Note}	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	0		300	ns
				0		1000	ns
SB0, SB1 \downarrow from $\overline{\text{SCK0}}\uparrow$	t_{KSB}			t_{KCY4}			ns
$\overline{\text{SCK0}}\downarrow$ from SB0, SB1 \downarrow	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{\text{SCK0}}$ rise, fall time	t_{R4} , t_{F4}					1000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output line.

(v) 2-wire serial I/O mode ($\overline{\text{SCK0}}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF ^{Note}	V _{DD} = 2.7 to 6.0 V	1600			ns
				3200			ns
$\overline{\text{SCK0}}$ high-level width	t_{KH5}		V _{DD} = 2.7 to 6.0 V	$t_{\text{KCY5}}/2-160$			ns
				$t_{\text{KCY5}}/2-190$			ns
$\overline{\text{SCK0}}$ low-level width	t_{KL5}		V _{DD} = 4.5 to 6.0 V	$t_{\text{KCY5}}/2-50$			ns
				$t_{\text{KCY5}}/2-100$			ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}\uparrow$)	t_{SIK5}		4.5 V ≤ V _{DD} ≤ 6.0 V	300			ns
			2.7 V ≤ V _{DD} < 4.5 V	350			ns
				400			ns
SB0, $\overline{\text{SB1}}$ hold time (from $\overline{\text{SCK0}}\uparrow$)	t_{KSI5}			600			ns
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	t_{KSO5}				300	ns	

Note R and C are the load resistance and load capacitance of the $\overline{\text{SCK0}}$, SB0 and SB1 output line.

(vi) 2-wire serial I/O mode ($\overline{\text{SCK0}}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{KCY6}	V _{DD} = 2.7 to 6.0 V		1600			ns
				3200			ns
$\overline{\text{SCK0}}$ high-level width	t_{KH6}	V _{DD} = 2.7 to 6.0 V		650			ns
				1300			ns
$\overline{\text{SCK0}}$ low-level width	t_{KL6}	V _{DD} = 2.7 to 6.0 V		800			ns
				1600			ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}\uparrow$)	t_{SIK6}			100			ns
SB0, $\overline{\text{SB1}}$ hold time (from $\overline{\text{SCK0}}\uparrow$)	t_{KSI6}			$t_{\text{KCY6}}/2$			ns
SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$	t_{KSO6}	R = 1 kΩ, C = 100 pF ^{Note}	V _{DD} = 4.5 to 6.0 V	0		300	ns
				0		500	ns
$\overline{\text{SCK0}}$ rise, fall time	$t_{\text{R6}},$ t_{F6}					1000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output line.

(b) Serial interface channel 2

(i) 3-wire serial I/O mode ($\overline{\text{SCK2}}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK2}}$ cycle time	t_{KCY7}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$	800			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1600			ns
			3200			ns
$\overline{\text{SCK2}}$ high/low-level width	$t_{\text{KH7}},$ t_{KL7}	$V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$	$t_{\text{KCY1}}/2-50$			ns
			$t_{\text{KCY1}}/2-100$			ns
SI2 setup time (to $\overline{\text{SCK2}}\uparrow$)	t_{SIK7}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$	100			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	150			ns
			300			ns
SI2 hold time (from $\overline{\text{SCK2}}\uparrow$)	t_{KSI7}		400			ns
SO2 output delay time from $\overline{\text{SCK2}}\downarrow$	t_{KSO7}	$C = 100 \text{ pF}^{\text{Note}}$			300	ns

Note C is the load capacitance of $\overline{\text{SCK2}}$, SO2 output line.

(ii) 3-wire serial I/O mode ($\overline{\text{SCK2}}$...External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK2}}$ cycle time	t_{KCY8}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$	800			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	1600			ns
			3200			ns
$\overline{\text{SCK2}}$ high/low-level width	$t_{\text{KH8}},$ t_{KL8}	$4.5 \text{ V} \leq V_{\text{DD}} \leq 6.0 \text{ V}$	400			ns
		$2.7 \text{ V} \leq V_{\text{DD}} < 4.5 \text{ V}$	800			ns
			1600			ns
SI2 setup time (to $\overline{\text{SCK2}}\uparrow$)	t_{SIK8}		100			ns
SI2 hold time (from $\overline{\text{SCK2}}\uparrow$)	t_{KSI8}		400			ns
SO2 output delay time from $\overline{\text{SCK2}}\downarrow$	t_{KSO8}	$C = 100 \text{ pF}^{\text{Note}}$			300	ns
$\overline{\text{SCK2}}$ rise, fall time	$t_{\text{R8}},$ t_{F8}				1000	ns

Note C is the load capacitance of SO2 output line.

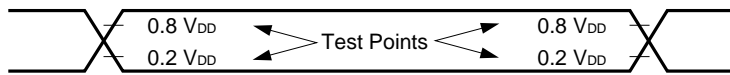
(iii) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		$4.5\text{ V} \leq V_{DD} \leq 6.0\text{ V}$			78125	bps
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$			39063	bps
					19531	bps

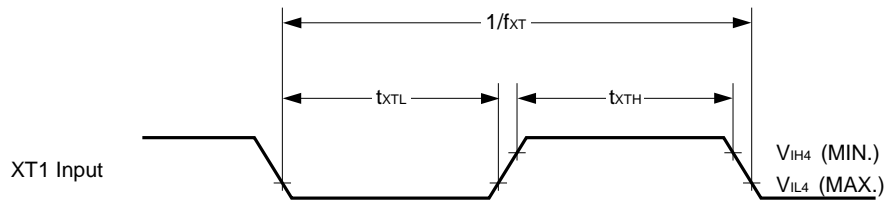
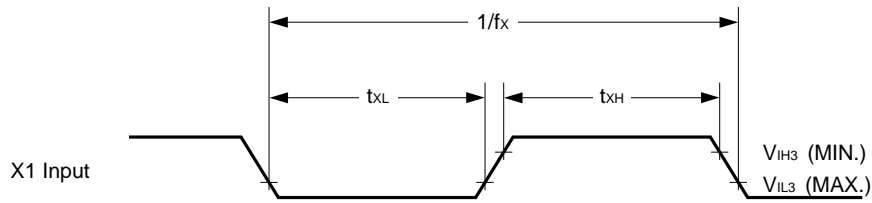
(iv) UART mode (External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY9}	$4.5\text{ V} \leq V_{DD} \leq 6.0\text{ V}$	800			ns
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$	1600			ns
			3200			ns
ASCK high/low-level width	t_{KH9} , t_{KL9}	$4.5\text{ V} \leq V_{DD} \leq 6.0\text{ V}$	400			ns
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$	800			ns
			1600			ns
Transfer rate		$4.5\text{ V} \leq V_{DD} \leq 6.0\text{ V}$			39063	bps
		$2.7\text{ V} \leq V_{DD} < 4.5\text{ V}$			19531	bps
					9766	bps
ASCK rise, fall time	t_{R9} , t_{F9}				1000	ns

AC Timing Test Point (Excluding X1, XT1 Input)

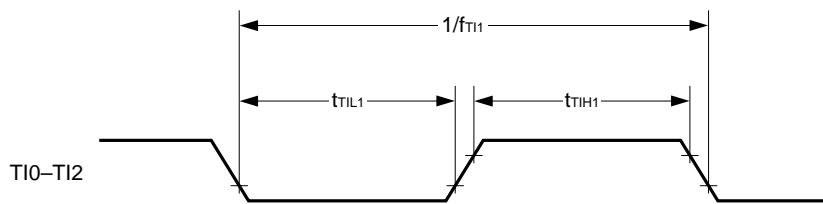
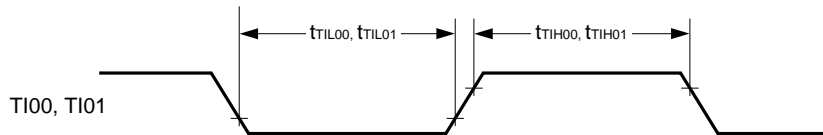


Clock Timing



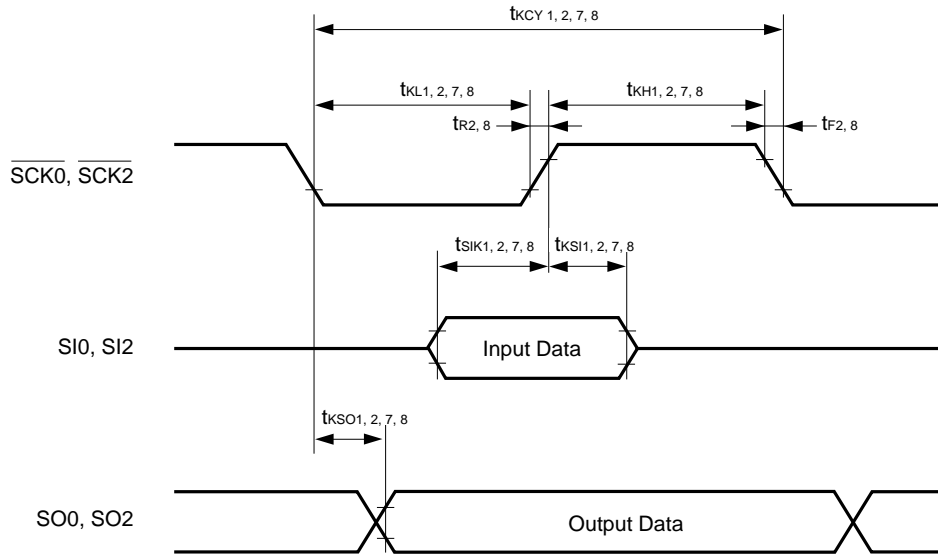
TI Timing

★

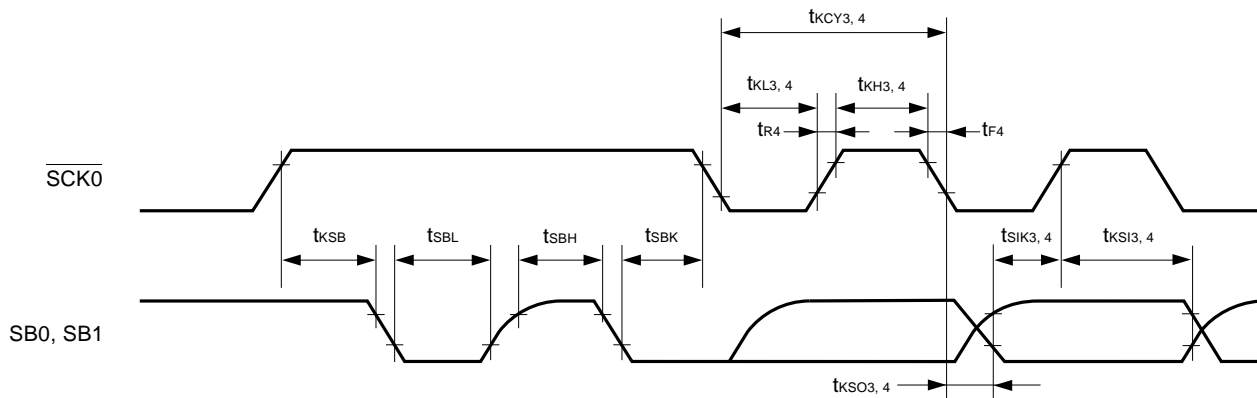


Serial Transfer Timing

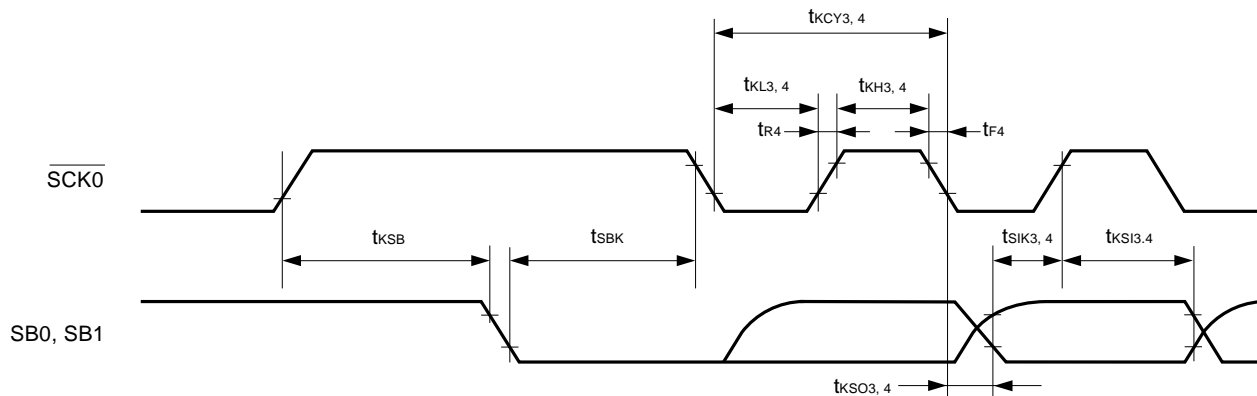
3-wire serial I/O mode:



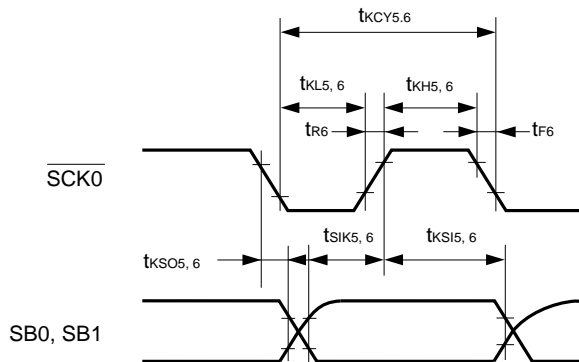
SBI mode (bus release signal transfer):



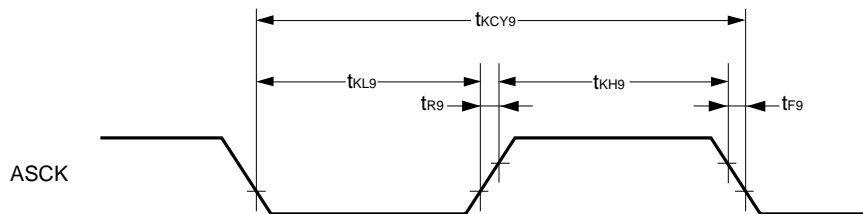
SBI mode (command signal transfer):



2-wire serial I/O mode:



UART mode:



A/D Converter ($T_A = -40$ to $+85$ °C, $AV_{DD} = V_{DD} = 2.0$ to 6.0 V, $AV_{SS} = V_{SS} = 0$ V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error ^{Note}		$2.7\text{ V} \leq AV_{REF} \leq 6.0\text{ V}$			± 0.6	%
					± 1.4	%
Conversion time	t_{CONV}		19.1		200	μs
Sampling time	t_{SAMP}		$12/f_{XX}$			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		2.0		AV_{DD}	V
$AV_{REF}-AV_{SS}$ resistance	R_{AIREF}		4	14		$\text{k}\Omega$

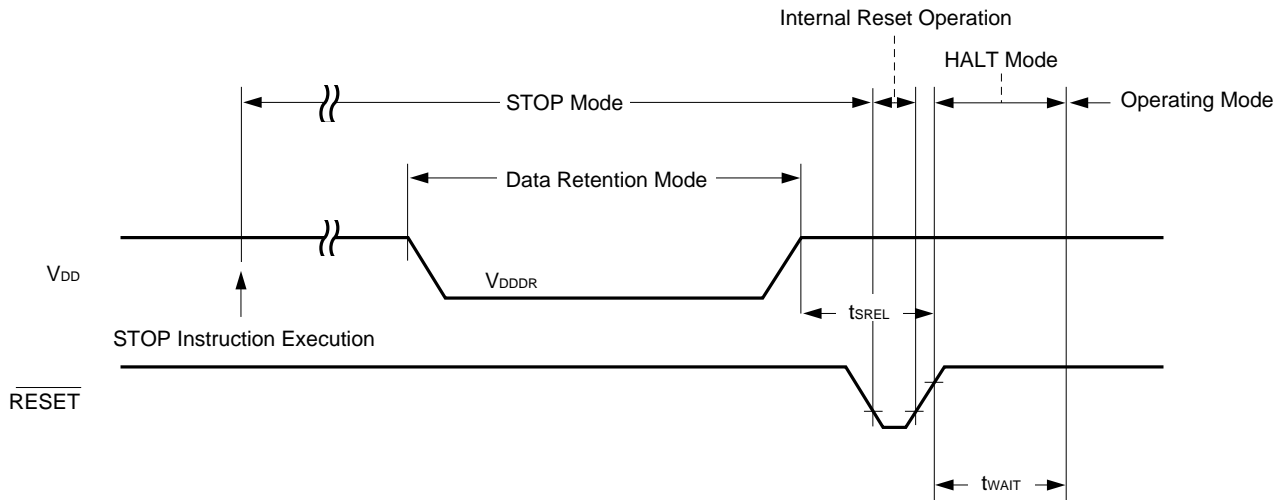
Note Quantization error ($\pm 1/2$ LSB) is not included. This is expressed in proportion to the full-scale value.

Data Memory Stop Mode Low Supply Voltage Data Retention Characteristics (T_A = -40 to +85 °C)

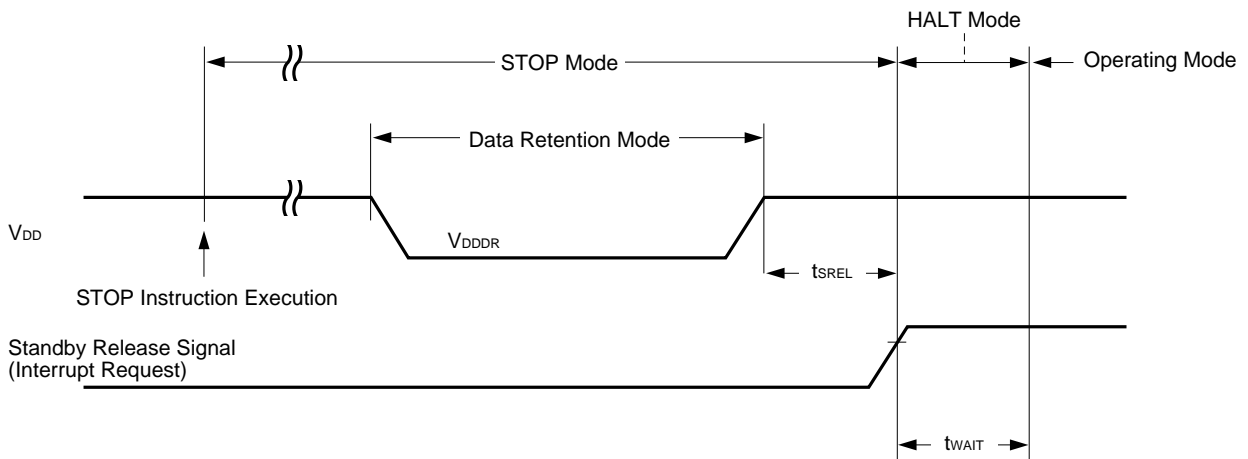
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V _{DDDR}		1.8		6.0	V
Data retention supply current	I _{DDDR}	V _{DDDR} = 1.8 V Subsystem clock stopped and feed-back resistor disconnected		0.1	10	μA
Release signal set time	t _{SREL}		0			μs
Oscillation stabilization wait time	t _{WAIT}	Release by $\overline{\text{RESET}}$		2 ¹⁷ /f _x		ms
		Release by interrupt		Note		ms

Note In combination with bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS), selection of 2¹²/f_{xx} and 2¹⁴/f_{xx} to 2¹⁷/f_{xx} is possible.

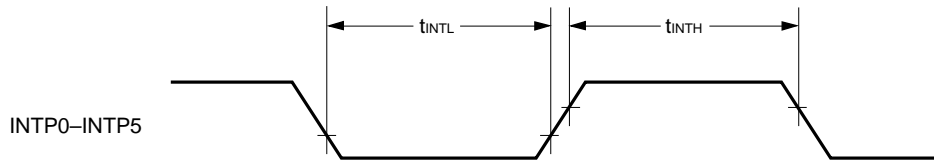
Data retention timing (STOP mode release by $\overline{\text{RESET}}$)



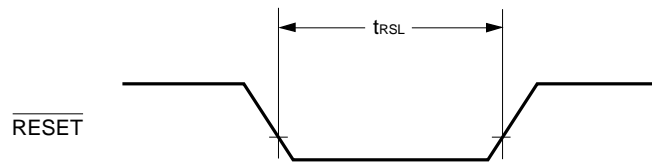
Data retention timing (STOP mode release by standby release signal: Interrupt signal)



Interrupt input timing

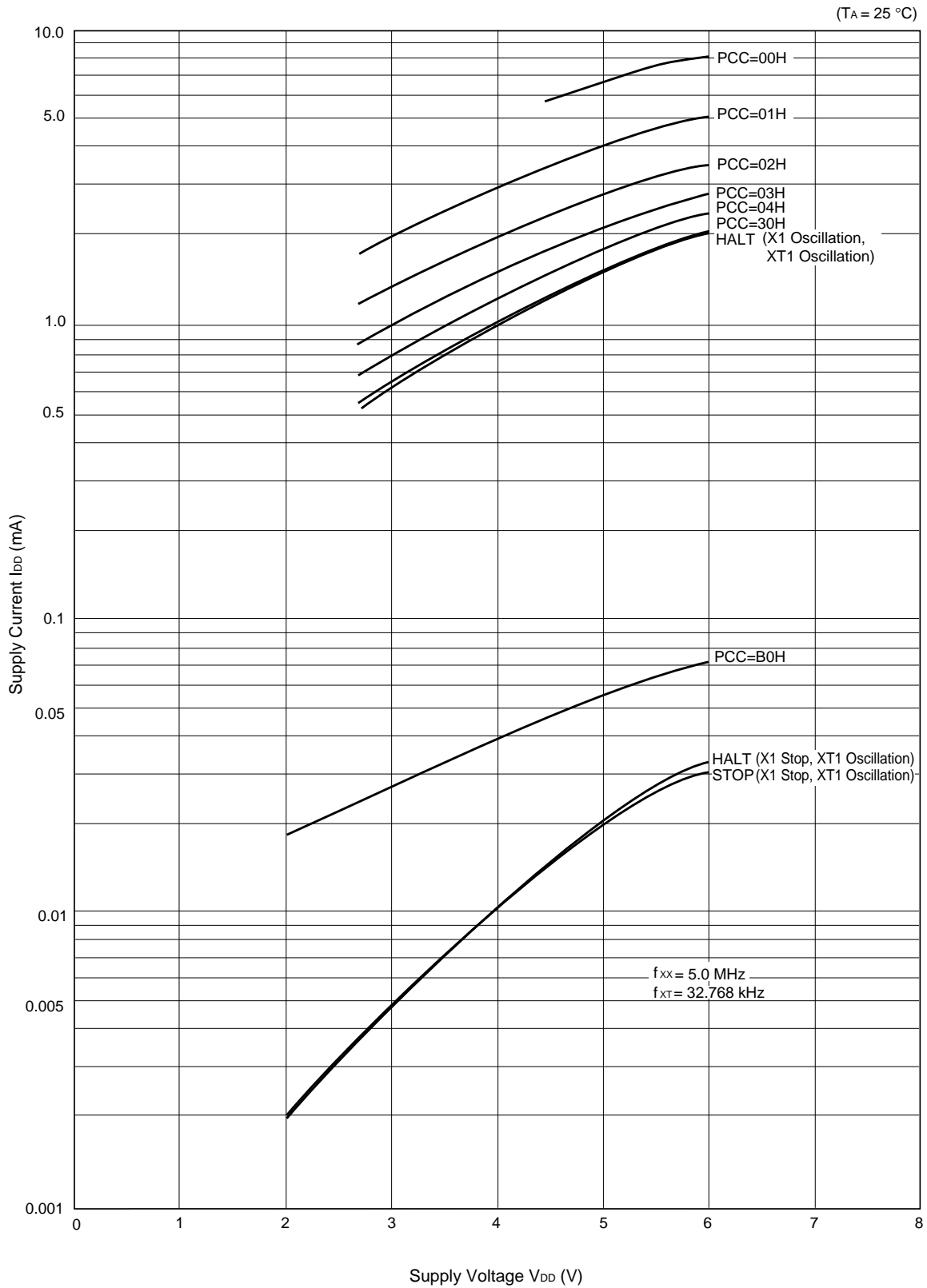


$\overline{\text{RESET}}$ input timing

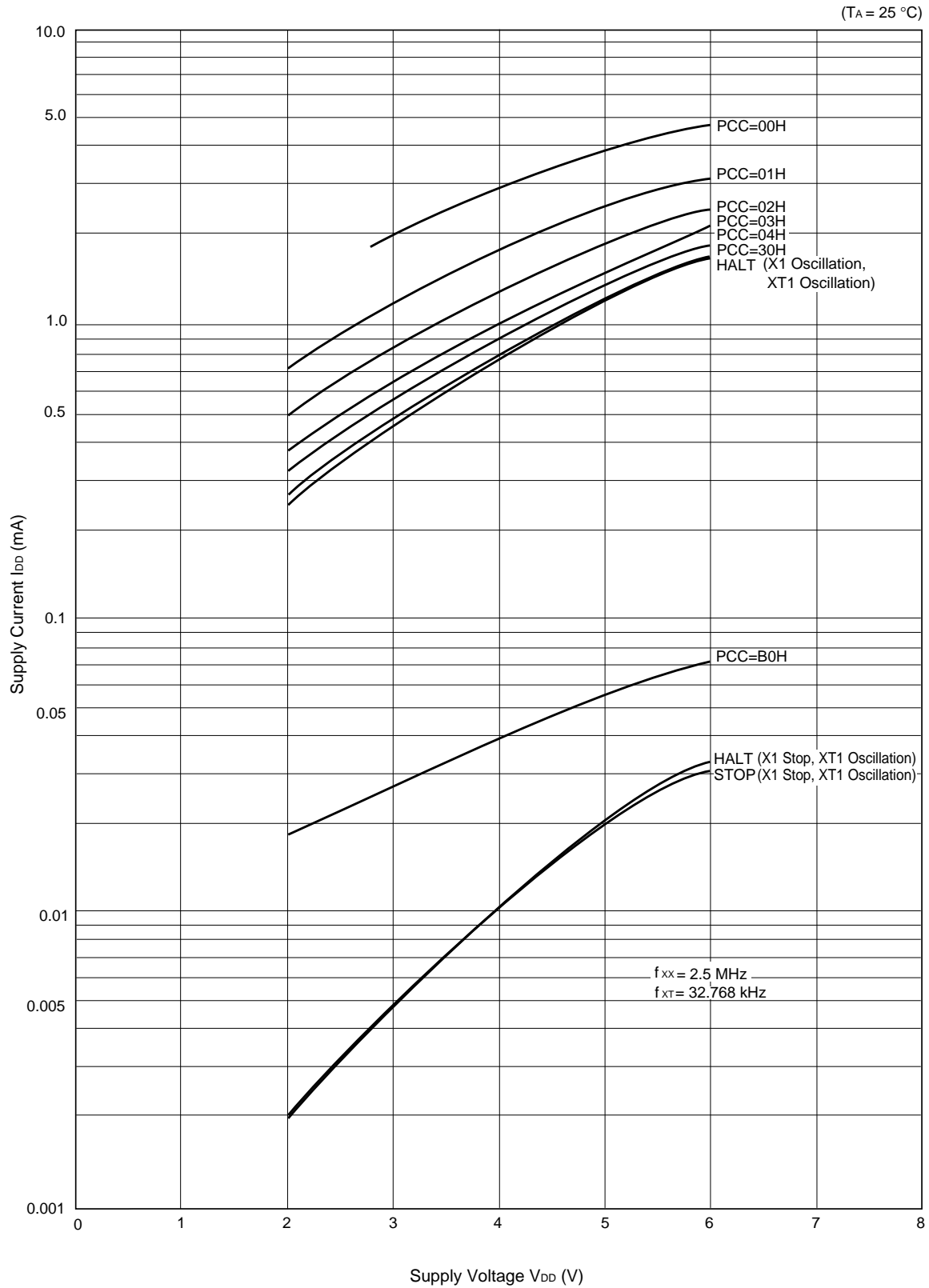


★ 11. CHARACTERISTIC CURVES (REFERENCE VALUES)

I_{DD} vs V_{DD} (Main System Clock: 5.0 MHz)

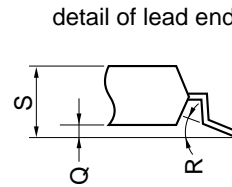
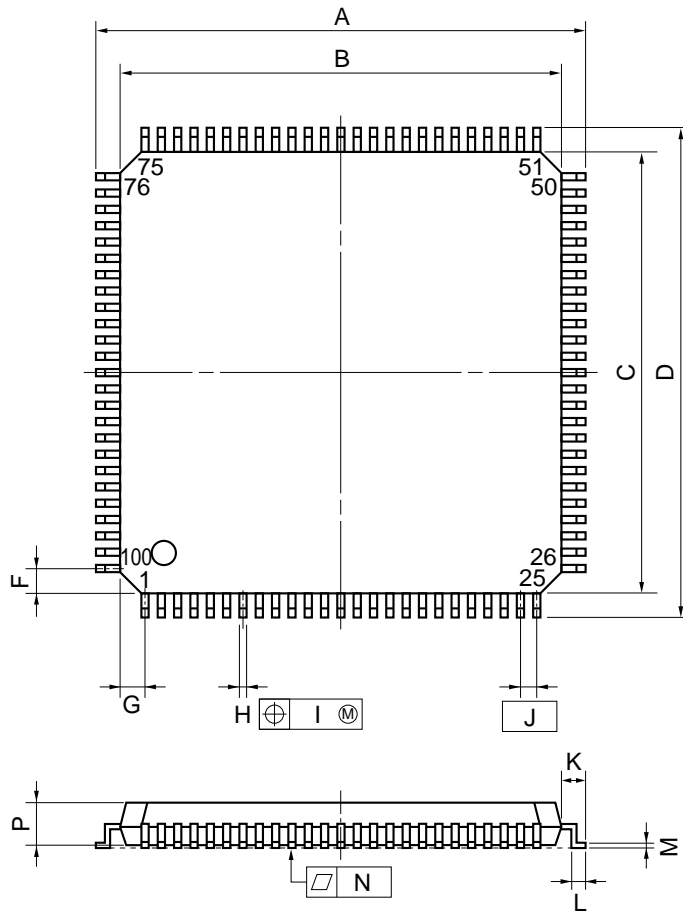


I_{DD} vs V_{DD} (Main System Clock: 2.5 MHz)



12. PACKAGE DRAWINGS

100 PIN PLASTIC QFP (FINE PITCH) (□14)



NOTE

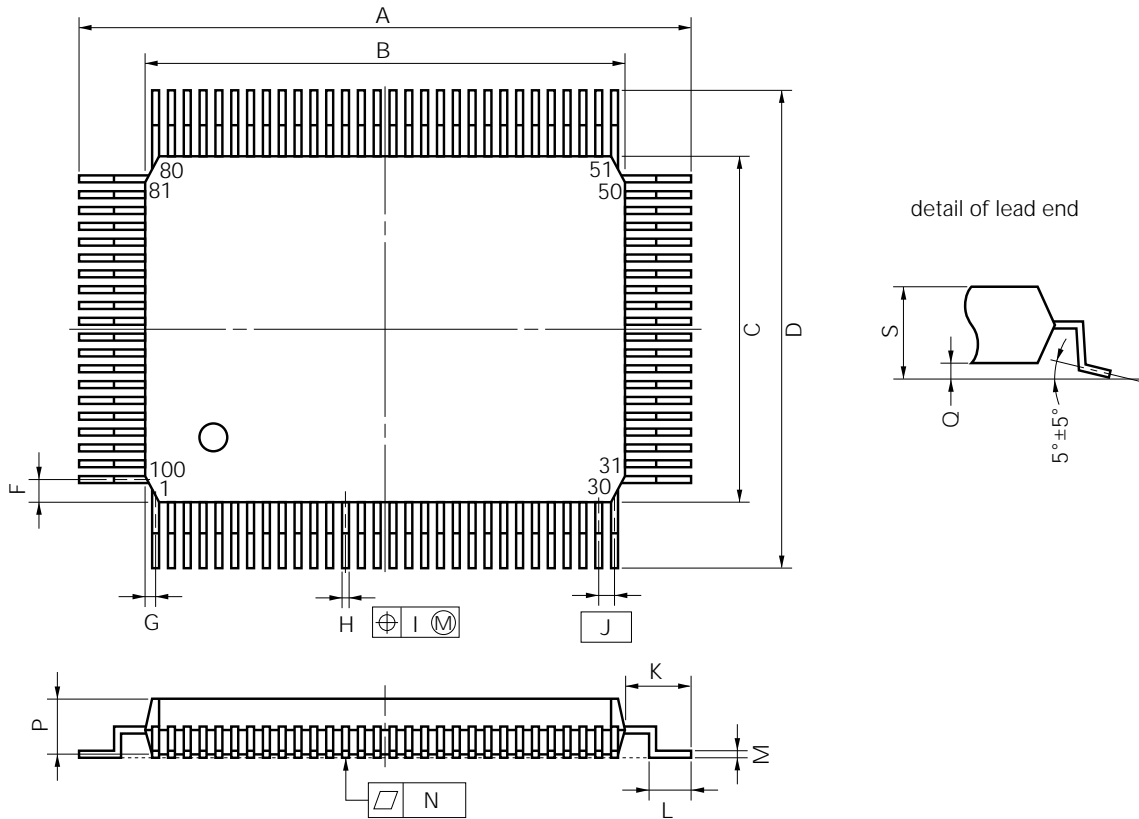
Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

Remark Dimensions and materials of ES products are same as those of mass production product.

ITEM	MILLIMETERS	INCHES
A	16.0±0.2	0.630±0.008
B	14.0±0.2	0.551 ^{+0.009} _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} _{-0.008}
D	16.0±0.2	0.630±0.008
F	1.0	0.039
G	1.0	0.039
H	0.22 ^{+0.05} _{-0.04}	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	0.039 ^{+0.009} _{-0.008}
L	0.5±0.2	0.020 ^{+0.008} _{-0.009}
M	0.17 ^{+0.03} _{-0.07}	0.007 ^{+0.001} _{-0.003}
N	0.10	0.004
P	1.45	0.057
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

P100GC-50-7EA-2

100 PIN PLASTIC QFP (14 × 20)



detail of lead end

NOTE

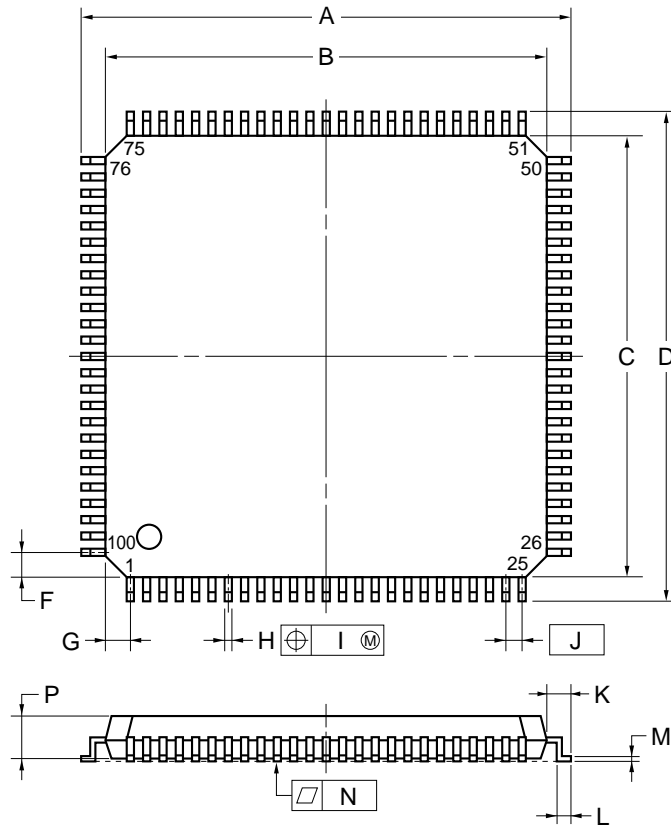
Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

Remark Dimensions and materials of ES products are same as mass production product.

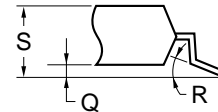
P100GF-65-3BA1-2

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	0.795 ^{+0.009} _{-0.008}
C	14.0±0.2	0.551 ^{+0.009} _{-0.008}
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	0.012 ^{+0.004} _{-0.005}
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	0.071 ^{+0.008} _{-0.009}
L	0.8±0.2	0.031 ^{+0.009} _{-0.008}
M	0.15 ^{+0.10} _{-0.05}	0.006 ^{+0.004} _{-0.003}
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

★ 100 PIN PLASTIC LQFP (FINE PITCH) (14×14)



detail of lead end



NOTE

Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

Remark Dimensions and materials of ES products are same as mass production product.

ITEM	MILLIMETERS	INCHES
A	16.00±0.20	0.630±0.008
B	14.00±0.20	0.551 ^{+0.009} _{-0.008}
C	14.00±0.20	0.551 ^{+0.009} _{-0.008}
D	16.00±0.20	0.630±0.008
F	1.00	0.039
G	1.00	0.039
H	0.22 ^{+0.05} _{-0.04}	0.009±0.002
I	0.08	0.003
J	0.50 (T.P.)	0.020 (T.P.)
K	1.00±0.20	0.039 ^{+0.009} _{-0.008}
L	0.50±0.20	0.020 ^{+0.008} _{-0.009}
M	0.17 ^{+0.03} _{-0.07}	0.007 ^{+0.001} _{-0.003}
N	0.08	0.003
P	1.40±0.05	0.055±0.002
Q	0.10±0.05	0.004±0.002
R	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}
S	1.60 MAX.	0.063 MAX.

S100GC-50-8EU

13. RECOMMENDED SOLDERING CONDITIONS

The μPD78062/78063/78064 should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact our sales personnel.

Table 13-1. Surface Mounting Type Soldering Conditions (1/2)

- (1) μPD78062GC-xxx-7EA : 100-pin plastic QFP (Fine pitch) (14 × 14mm, resin thickness: 1.45 mm)
 ★ μPD78062GC-xxx-8EU : 100-pin plastic LQFP (Fine pitch) (14 × 14mm, resin thickness: 1.40 mm)
 μPD78063GC-xxx-7EA : 100-pin plastic QFP (Fine pitch) (14 × 14mm, resin thickness: 1.45 mm)
 ★ μPD78063GC-xxx-8EU : 100-pin plastic LQFP (Fine pitch) (14 × 14mm, resin thickness: 1.40 mm)
 μPD78064GC-xxx-7EA : 100-pin plastic QFP (Fine pitch) (14 × 14mm, resin thickness: 1.45 mm)
 ★ μPD78064GC-xxx-8EU : 100-pin plastic LQFP (Fine pitch) (14 × 14mm, resin thickness: 1.40 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
★ Infrared reflow	Package peak temperature: 235°C, Duration: 30 sec. max. (at 210°C or above), Number of times: Twice max., Time limit: 7 days ^{Note} (thereafter 10 hours prebaking required at 125°C) <precaution> Baking cannot be applied to other than heat-resistant trays (magazine, taping, non-heat-resistant trays) when the product is wrapped.	IR35-107-2
★ VPS	Package peak temperature: 215°C, Duration: 40 sec. (at 200°C or above), Number of times: Twice max., Time limit: 7 days ^{Note} (thereafter 10 hours prebaking required at 125°C) <precaution> Baking cannot be applied to other than heat-resistant trays (magazine, taping, non-heat-resistant trays) when the product is wrapped.	VP15-107-2
Partial heating	Pin temperature: 300°C max. Duration: 3 sec. max. (per device side)	—

Note For the storage period after dry-pack decapsulation, storage conditions are max. 25°C, 65% RH.

(2) μPD78062GF-xxx-3BA : 100-pin plastic QFP (14 × 20 mm)

μPD78063GF-xxx-3BA : 100-pin plastic QFP (14 × 20 mm)

μPD78064GF-xxx-3BA : 100-pin plastic QFP (14 × 20 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
★ Infrared reflow	Package peak temperature: 235°C, Duration: 30 sec. max. (at 210°C or above), Number of times: Thrice max.	IR35-00-3
★ VPS	Package peak temperature: 215°C, Duration: 40 sec. (at 200°C or above), Number of times: Thrice max.	VP15-00-3
Wave soldering	Solder bath temperature: 260°C max., Duration: 10 sec. max., Number of times: Once, Preliminary heat temperature: 120°C max. (Package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max. Duration: 3 sec. max. (per device side)	—

Caution Use of more than one soldering method should be avoided (except in the case of partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using μPD78062/78063/78064.

Language Processing Software

RA78K/0 <small>Note 1, 2, 3, 4</small>	78K/0 series common assembler package
CC78K/0 <small>Note 1, 2, 3, 4</small>	78K/0 series common C compiler package
DF78064 <small>Note 1, 2, 3, 4</small>	μPD78064 subseries device file
CC78K/0-L <small>Note 1, 2, 3, 4</small>	78K/0 series common C compiler library source file

PROM Writing Tools

PG-1500	PROM programmer
PA-78P0308GC PA-78P0308GF PA-78P0308KL-T	Programmer adapters connected to PG-1500
PG-1500 controller <small>Note 1, 2</small>	PG-1500 control program

Debugging Tools

	IE-78000-R	78K/0 series common in-circuit emulator
★	IE-78000-R-A	78K/0 series common in-circuit emulator (for integrated debugger)
	IE-78000-R-BK	78K/0 series common break board
	IE-78064-R-EM <small>Note 8</small>	μPD78064 subseries evaluation emulation board
★	IE-780308-R-EM	μPD780308 subseries common emulation board
	EP-78064GC-R EP-78064GF-R	μPD78064 subseries common emulation probes
★	TGC-100SDW	Adapter to be mounted on a target system board made for 100-pin plastic QFP (GC-7EA, GC-8EU type) TGC-100SDW is a product from Tokyo Eletech Corp. (TEL (03) 5295-1661) When purchasing this product, please consult with our sales offices.
	EV-9200GF-100	Socket to be mounted on a target system board made for 100-pin plastic QFP (GF-3BA type)
	EV-9900	Tool used when removing μPD78P064KL-T from EV-9200GF-100
	SM78K0 <small>Note 5, 6, 7</small>	78K/0 series common system simulator
★	ID78K0 <small>Note 4, 5, 6, 7</small>	IE-78000-R-A integrated debugger
	SD78K/0 <small>Note 1, 2</small>	IE-78000-R screen debugger
	DF78064 <small>Note 1, 2, 4, 5, 6, 7</small>	μPD78064 subseries device file

Real-Time OS

RX78K/0 <small>Note 1, 2, 3, 4</small>	78K/0 series real-time OS
MX78K0 <small>Note 1, 2, 3, 4</small>	78K/0 series OS

Fuzzy Inference Development Support System

FE9000 <small>Note 1</small> , FE9200 <small>Note 6</small>	Fuzzy knowledge data creation tool
FT9080 <small>Note 1</small> , FT9085 <small>Note 2</small>	Translator
FI78K/0 <small>Note 1, 2</small>	Fuzzy inference module
FD78K/0 <small>Note 1, 2</small>	Fussy inference debugger

Notes 1. PC-9800 series (MS-DOS™) based

2. IBM PC/AT™ and compatible (PC DOS™/IBM DOS™/MS-DOS) based

3. HP9000 series 300™ (HP-UX™) based

4. HP9000 series 700™ (HP-UX) based, SPARCstation™ (SunOS™) based, EWS-4800 series (EWS-UX/V) based

5. PC-9800 series (MS-DOS + Windows™) based.

6. IBM PC/AT and compatible (PC DOS/IBM DOS/MS-DOS + Windows) based

★ 7. NEWS™ (NEWS-OS™) based

8. IE-78064-R-EM is a maintenance product.

Remarks 1. For third party development tools, refer to the **78K/0 Series Selection Guide (U11126E)**.

2. RA78K/0, CC78K/0, SM78K0, ID78K0, SD78K/0, and RX78K/0 are used in combination with DF78064.

APPENDIX B. RELATED DOCUMENTS

Device Related Documents

Document Name		Document No.	
		Japanese	English
μPD78062, 78063, 78064 Data Sheet		U12338J	This document
μPD78062(A), 78063(A) 78064(A) Data Sheet		ID-9133	U10335E
μPD78P064 Data Sheet		IC-8636	IC-3224
μPD78064, 78064Y Subseries User's Manual		U10105J	U10105E
78K/0 Series User's Manual - Instruction		U12326J	IEU-1372
78K/0 Series Instruction List		U10903J	—
78K/0 Series Instruction Set		U10904J	—
μPD78018F Subseries Special Function Register Table		IEM-5568	—
78K/0 Series Application Note	Fundamental (III)	IEA-767	U10182E
	Floating-Point Arithmetic Program	IEA-718	IEA-1289

Development Tools Related Documents (User's Manual) (1/2)

Document Name		Document No.	
		Japanese	English
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
★ RA78K0 Assembler Package	Operation	U11802J	U11802E
	Assembly Language	U11801J	U11801E
	Structured Assembly Language	U11789J	U11789E
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
★ CC78K/0 C Compiler	Operation	U11517J	U11517E
	Language	U11518J	U11518E
★ CC78K/0 C Compiler Application Note	Programming Know-how	EEA-618	EEA-1208
CC78K Series Library Source File		U12322J	—
PG-1500 PROM Programmer		U11940J	EEU-1335
PG-1500 Controller PC-9800 Series (MS-DOS) Based		EEU-704	EEU-1291
PG-1500 Controller IBM PC Series (PC DOS) Based		EEU-5008	U10540E
IE-78000-R		EEU-810	U11376E
★	IE-78000-R-A	U10057J	U10057E
IE-78000-R-BK		EEU-867	EEU-1427
IE-78064-R-EM		EEU-905	EEU-1443
★	IE-780308-R-EM	U11362J	U11362E
EP-78064		EEU-934	EEU-1469

Caution The contents of the above related documents are subject to change without notice. The latest documents should be used for design, etc.

Development Tools Documents (User's Manual) (2/2)

Document Name		Document No.	
		Japanese	English
★ SM78K Series System Simulator	External Components User Open Interface	U10092J	U10092E
	SM78K0 System Simulator Windows Based	U10181J	U10181E
★ ID78K0 Integrated Debugger EWS Based	Reference	U11515J	—
★ ID78K0 Integrated Debugger PC Based	Reference	U11539J	U11539E
★ ID78K0 Integrated Debugger Windows Based	Guide	U11649J	U11649E
	SD78K/0 Screen Debugger	EEU-852	U10539E
	PC-9800 Series (MS-DOS) Based	U10952J	—
	SD78K/0 Screen Debugger	EEU-5024	EEU-1414
	IBM PC/AT (PC DOS) Based	U11279J	U11279E

Embedded Software Documents (User's Manual)

Document Name		Document No.	
		Japanese	English
78K/0 Series Real-Time OS	Fundamental	U11537J	—
	Installation	U11536J	—
78K/0 Series OS MX78K0	Fundamental	U12257J	—
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System - Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System - Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System - Fuzzy Inference Debugger		EEU-921	EEU-1458

Other Documents

Document Name		Document No.	
		Japanese	English
IC Package Manual		C10943X	
Semiconductor Device Mounting Technology Manual		C10535J	C10535E
Quality Grades on NEC Semiconductor Device		C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System		C10983J	C10983E
Electrostatic Discharge (ESD) Test		MEM-539	—
Guide to Quality Assurance for Semiconductor Device		C11893J	C11893E
Guide for Products Related to Micro-Computer: Other Companies		U11416J	—

Caution The contents of the above related documents are subject to change without notice. The latest documents should be used for design, etc.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Fax: 800-729-9288

NEC Electronics (Germany) GmbH

Duesseldorf, Germany
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Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.

Milton Keynes, UK
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Fax: 01908-670-290

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Fax: 02-66 75 42 99

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NEC Electronics Singapore Pte. Ltd.

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Fax: 02-719-5951

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NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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