

MOS INTEGRATED CIRCUIT

μ PD78056FY,78058FY

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μ PD78056FY,78058FY reduce the electromagnetic interference (EMI) noise in comparison with the conventional μ PD78056Y,78058Y. The μ PD78056FY,78058FY belong to the μ PD78058FY Subseries products of the 78K/0 Series. These microcontrollers include a variety of peripheral hardware, such as an 8-bit resolution A/D converter, 8-bit resolution D/A converter, timer, serial interface (supports I²C bus mode), real-time output ports, and interrupt functions.

The μ PD78P058FY, a one-time PROM which can be operated in the same supply voltage range as for the mask ROM version, and various development tools are also available.

Detailed function descriptions are provided in the following user's manual. Be sure to read them before designing.

μ PD78058F, 78058FY Subseries User's Manual: U12068E
78K/0 Series User's Manual-Instruction: U12326E

FEATURES

- EMI noise reduction version (The overall peak level is reduced by 5 to 10 dB.)
- Large on-chip ROM & RAM

| Products | Items | Program Memory (ROM) | Data Memory | | | Packages |
|-----------------|-------|----------------------|-------------------------|------------|------------------------|---|
| | | | Internal High-Speed RAM | Buffer RAM | Internal Expansion RAM | |
| μ PD78056FY | | 48 Kbytes | 1024 bytes | 32 bytes | None | 80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm) 80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm) 80-pin plastic TQFP (fine pitch) (12 × 12 mm) ^{Note} |
| μ PD78058FY | | 60 Kbytes | | | 1024 bytes | |

Note This package is available only for the μ PD78058FY.

- External memory expansion space: 64 Kbytes
- Minimum instruction execution time can be varied from high-speed (0.4 μ s) to ultra-low-speed (122 μ s)
- I/O ports: 69 (N-ch open-drain: 4)
- 8-bit resolution A/D converter: 8 channels
- 8-bit resolution D/A converter: 2 channels
- Serial interface: 3 channels (supports I²C bus mode: 1 channel)
- Timer: 5 channels
- Supply voltage: V_{DD} = 2.7 to 6.0 V

APPLICATIONS

Cellular phones, pagers, printers, AV equipment, air conditioners, cameras, PPC, fuzzy home appliances, vending machines, etc.

The information in this document is subject to change without notice.

ORDERING INFORMATION

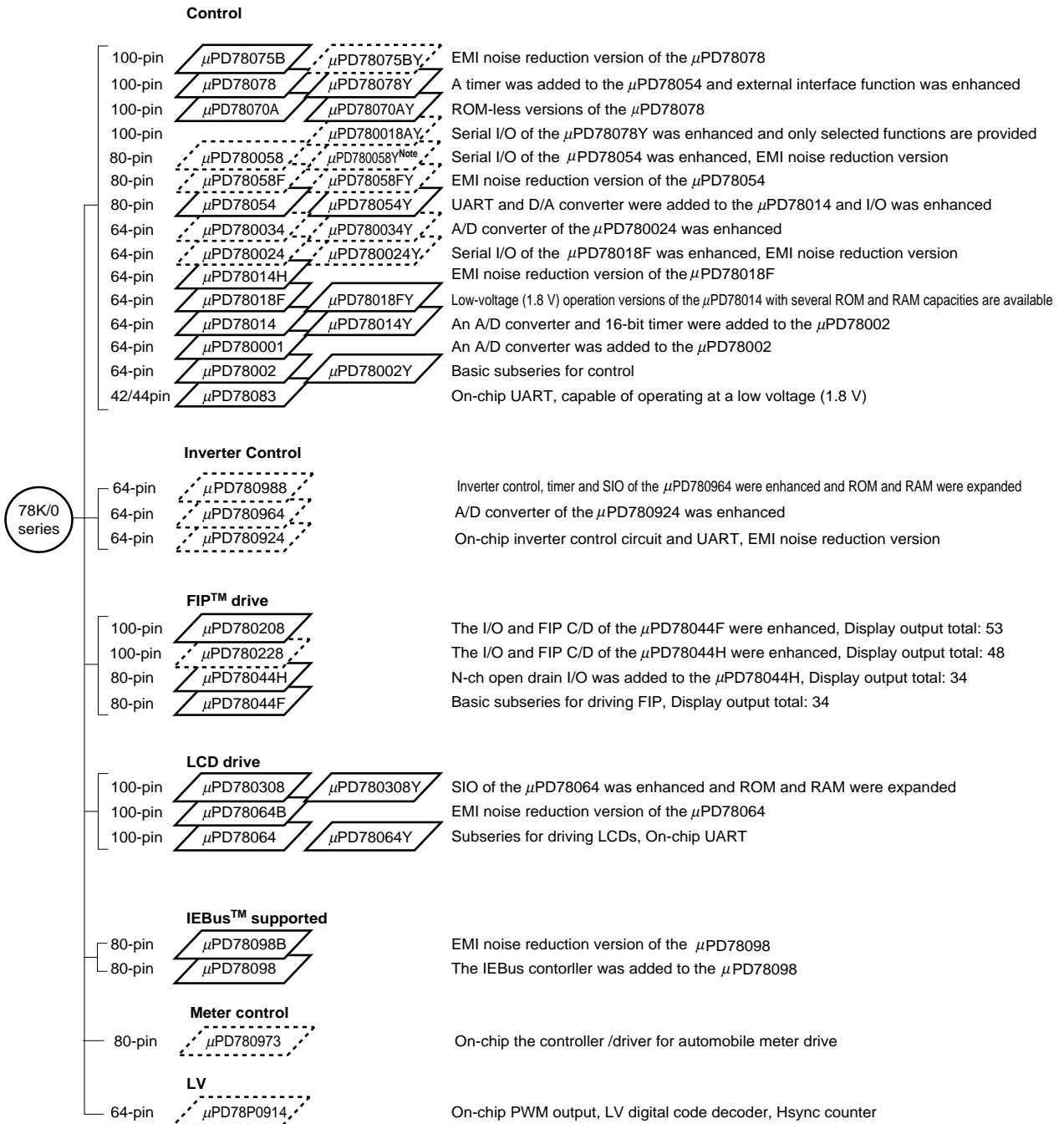
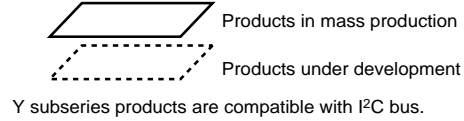
| | Part Number | Package |
|---|---------------------------|---|
| | μ PD78056FYGC-xxx-3B9 | 80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm) |
| ★ | μ PD78056FYGC-xxx-8BT | 80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm) |
| | μ PD78058FYGC-xxx-3B9 | 80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm) |
| ★ | μ PD78058FYGC-xxx-8BT | 80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm) |
| | μ PD78058FYGK-xxx-BE9 | 80-pin plastic TQFP (fine pitch) (12 × 12 mm) |

Caution The μ PD78056FYGC, μ PD78058FYGC come in two types of packages (see 12 Package Drawings).
For the packages that can be supplied, consult your local NEC sales representative.

Remark xxx denotes the ROM code number.

★ 78K/0 SERIES PRODUCT DEVELOPMENT

These products are a further development in the 78K/0 Series. The designations appearing inside the boxes are subseries names.



Note Under planning

The major functional differences among the Y subseries are shown below.

| Subseries | Function | ROM Capacity | Serial Interface | I/O | V _{DD} MIN. Value |
|-------------|-------------|--------------|---|-----|----------------------------|
| Control | μPD78075BY | 32 K to 40 K | 3-wire/2-wire/I ² C : 1 ch | 88 | 1.8 V |
| | μPD78078Y | 48 K to 60 K | 3-wire with automatic send/receive function : 1 ch | | |
| | μPD78070AY | — | 3-wire/UART : 1 ch | 61 | 2.7 V |
| | μPD780018AY | 48 K to 60 K | 3-wire with automatic send/receive function : 1 ch Time division 3-wire : 1 ch I ² C bus (supports multimaster) : 1 ch | 88 | |
| | μPD780058Y | 24 K to 60 K | 3-wire/2-wire/I ² C : 1 ch 3-wire with automatic send/receive function : 1 ch 3-wire/time division UART : 1 ch | 68 | 1.8 V |
| | μPD78058FY | 48 K to 60 K | 3-wire/2-wire/I ² C : 1 ch | 69 | 2.7 V |
| | μPD78054Y | 16 K to 60 K | 3-wire with automatic send/receive function : 1 ch 3-wire/UART : 1 ch | | 2.0 V |
| | μPD780034Y | 8 K to 32 K | UART : 1 ch | 51 | 1.8 V |
| | μPD780024Y | | 3-wire : 1 ch I ² C bus (supports multimaster) : 1 ch | | |
| | μPD78018FY | 8 K to 60 K | 3-wire/2-wire/I ² C : 1 ch 3-wire with automatic send/receive function : 1 ch | | |
| | μPD78014Y | 8 K to 32 K | 3-wire/2-wire/SBI/I ² C : 1 ch 3-wire with automatic send/receive function : 1 ch | | |
| | μPD78002Y | 8 K to 16 K | 3-wire/2-wire/SBI/I ² C : 1 ch | | |
| LCD driving | μPD780308Y | 48 K to 60 K | 3-wire/2-wire/I ² C : 1 ch | 57 | 2.0 V |
| | | | 3-wire/time-division UART : 1 ch 3-wire : 1 ch | | |
| | μPD78064Y | 16 K to 32 K | 3-wire/2-wire/I ² C : 1 ch 3-wire/UART : 1 ch | | |

Remark The functions, except for the serial interface, are the same as those of subseries without Y.

OVERVIEW OF FUNCTION

| Item | | Product Name | μPD78056FY | μPD78058FY | | | | | | | | |
|------------------------------------|---------------------------------|--------------|--|-------------|-------|------|--------------|-----|------------|------|-----------------------|-----|
| Internal memory | ROM | | 48 Kbytes | 60 Kbytes | | | | | | | | |
| | High-speed RAM | | 1024 bytes | | | | | | | | | |
| | Buffer RAM | | 32 bytes | | | | | | | | | |
| | Expanded RAM | | None | 1024 Kbytes | | | | | | | | |
| Memory space | | | 64 Kbytes | | | | | | | | | |
| General registers | | | 8 bits × 32 registers (8 bits × 8 registers × 4 banks) | | | | | | | | | |
| Minimum instruction execution time | | | On-chip instruction execution time cycle modification function | | | | | | | | | |
| | When main system clock selected | | 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (at 5.0-MHz operation) | | | | | | | | | |
| | When subsystem clock selected | | 122 μs (at 32.768-kHz operation) | | | | | | | | | |
| Instruction set | | | <ul style="list-style-type: none"> • 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD correction, etc. | | | | | | | | | |
| I/O ports | | | <table> <tr> <td>Total</td> <td>: 69</td> </tr> <tr> <td>• CMOS input</td> <td>: 2</td> </tr> <tr> <td>• CMOS I/O</td> <td>: 63</td> </tr> <tr> <td>• N-ch open-drain I/O</td> <td>: 4</td> </tr> </table> | | Total | : 69 | • CMOS input | : 2 | • CMOS I/O | : 63 | • N-ch open-drain I/O | : 4 |
| Total | : 69 | | | | | | | | | | | |
| • CMOS input | : 2 | | | | | | | | | | | |
| • CMOS I/O | : 63 | | | | | | | | | | | |
| • N-ch open-drain I/O | : 4 | | | | | | | | | | | |
| A/D converter | | | • 8-bit resolution × 8 channels | | | | | | | | | |
| D/A converter | | | • 8-bit resolution × 2 channels | | | | | | | | | |
| Serial interface | | | <ul style="list-style-type: none"> • 3-wire serial I/O/2-wire serial I/O/I²C bus mode selectable: 1 channel • 3-wire serial I/O mode (on-chip max. 32 bytes automatic data transmit/receive function): 1 channel • 3-wire serial I/O/UART mode selectable: 1 channel | | | | | | | | | |
| Timer | | | <ul style="list-style-type: none"> • 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel | | | | | | | | | |
| Timer output | | | 3 (14-bit PWM output × 1) | | | | | | | | | |
| Clock output | | | 19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (at main system clock 5.0-MHz operation) 32.768 kHz (at subsystem clock 32.768-kHz operation) | | | | | | | | | |
| Buzzer output | | | 1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (at main system clock 5.0-MHz operation) | | | | | | | | | |
| Vectored-interrupt source | Maskable | | Internal : 13, external : 7 | | | | | | | | | |
| | Non-maskable | | Internal : 1 | | | | | | | | | |
| | Software | | 1 | | | | | | | | | |
| Test input | | | Internal : 1, external : 1 | | | | | | | | | |
| Supply voltage | | | V _{DD} = 2.7 to 6.0 V | | | | | | | | | |
| Operating ambient temperature | | | T _A = - 40 to + 85°C | | | | | | | | | |
| Package | | | <ul style="list-style-type: none"> • 80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm) • 80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm) • 80-pin plastic TQFP (fine pitch) (12 × 12 mm) Note | | | | | | | | | |

Note μPD78058FY only

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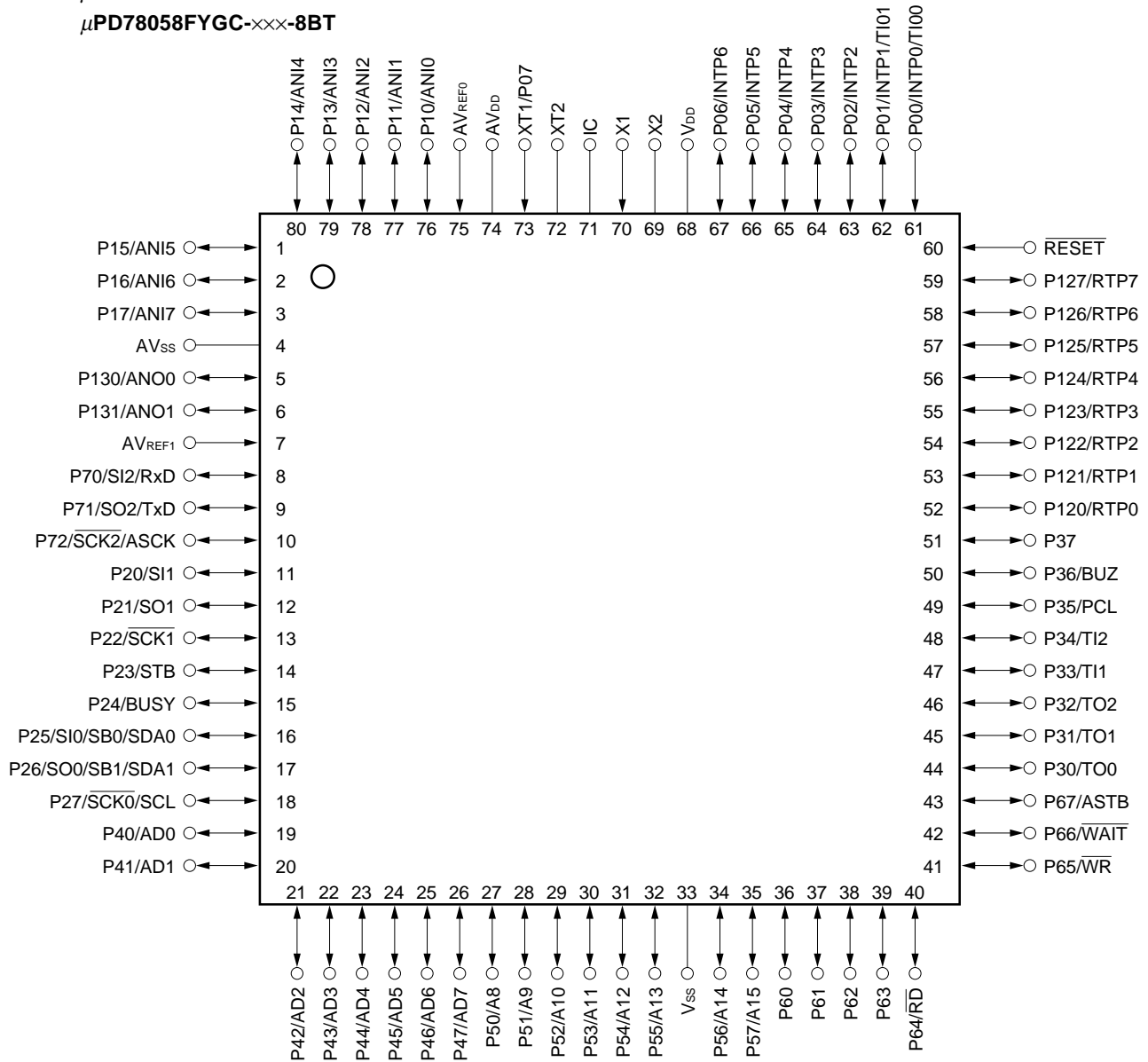
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1. PIN CONFIGURATION (TOP VIEW)

- 80-pin plastic QFP (14 × 14, resin thickness 2.7 mm)
μPD78056FYGC-xxx-3B9
μPD78058FYGC-xxx-3B9

- 80-pin plastic TQFP (fine pitch) (12 × 12 mm)
μPD78058FYGK-xxx-BE9

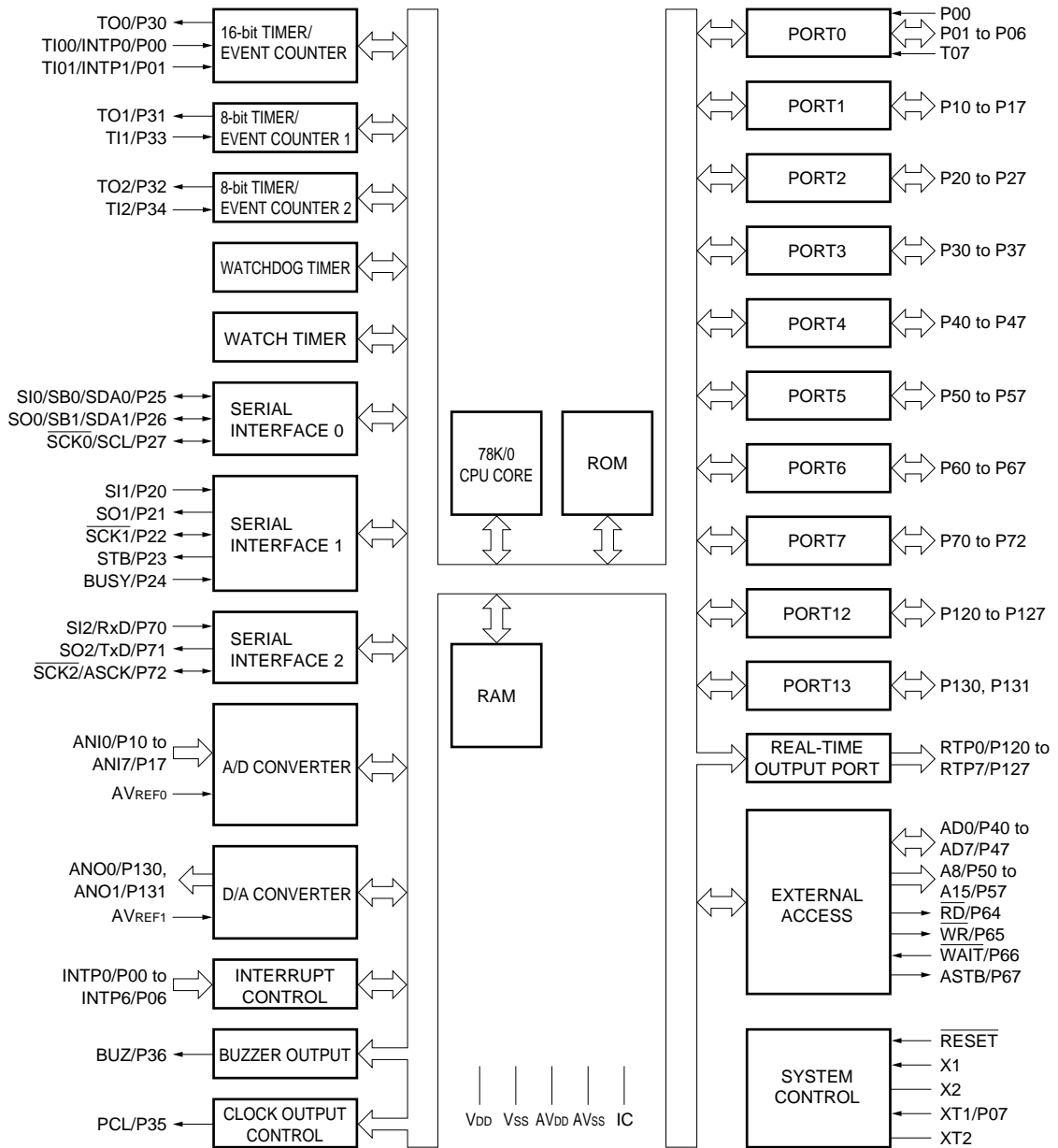
- 80-pin plastic QFP (14 × 14, resin thickness 1.4 mm)
μPD78056FYGC-xxx-8BT
μPD78058FYGC-xxx-8BT



- Cautions**
1. Connect directly the Internally Connected (IC) pin to V_{ss}.
 2. The AV_{DD} pin functions as both an A/D converter power supply and a port power supply. When the μPD78056FY and 78058FY are used in applications where the noise generated inside the microcontroller needs to be reduced, connect the AV_{DD} pin to another power supply which has the same potential as V_{DD}.
 3. The AV_{ss} pin functions as both an A/D and D/A converter ground and as a port ground. When the μPD78056FY and 78058FY are used in applications where the noise generated inside the microcontroller needs to be reduced, connect the AV_{ss} pin to a ground line other than V_{ss}.

| | | | |
|----------------|------------------------------|--|-------------------------------|
| A8 to A15 | : Address Bus | PCL | : Programmable Clock |
| AD0 to AD7 | : Address/Data Bus | \overline{RD} | : Read Strobe |
| ANI0 to ANI7 | : Analog Input | \overline{RESET} | : Reset |
| ANO0, ANO1 | : Analog Output | RTP0 to RTP7 | : Real-Time Output Port |
| ASCK | : Asynchronous Serial Clock | RxD | : Receive Data |
| ASTB | : Address Strobe | SB0, SB1 | : Serial Bus |
| AVDD | : Analog Power Supply | $\overline{SCK0}$ to $\overline{SCK2}$ | : Serial Clock |
| AVREF0, AVREF1 | : Analog Reference Voltage | SCL | : Serial Clock |
| AVSS | : Analog Ground | SDA0, SDA1 | : Serial Data |
| BUSY | : Busy | SI0 to SI2 | : Serial Input |
| BUZ | : Buzzer Clock | SO0 to SO2 | : Serial Output |
| IC | : Internally Connected | STB | : Strobe |
| INTP0 to INTP6 | : Interrupt from Peripherals | TI00, TI01 | : Timer Input |
| P00 to P07 | : Port0 | TI1, TI2, | : Timer Input |
| P10 to P17 | : Port1 | TO0 to TO2 | : Timer Output |
| P20 to P27 | : Port2 | TxD | : Transmit Data |
| P30 to P37 | : Port3 | VDD | : Power Supply |
| P40 to P47 | : Port4 | VSS | : Ground |
| P50 to P57 | : Port5 | \overline{WAIT} | : Wait |
| P60 to P67 | : Port6 | \overline{WR} | : Write Strobe |
| P70 to P72 | : Port7 | X1, X2 | : Crystal (Main System Clock) |
| P120 to P127 | : Port12 | XT1, XT2 | : Crystal (Subsystem Clock) |
| P130, P131 | : Port13 | | |

2. BLOCK DIAGRAM



Remark The internal ROM and RAM capacity depends on the product.

3. PIN FUNCTIONS

3.1 Port Pins (1/2)

| Pin Name | I/O | Function | | After Reset | Alternate Function |
|-------------------|------------------|---|--|-------------------------------------|--------------------|
| P00 | Input | Port 0 8-bit I/O port | Input only | Input | INTP0/TI00 |
| P01 | Input/ output | | Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. | Input | INTP1/TI01 |
| P02 | | | | | INTP2 |
| P03 | | | | | INTP3 |
| P04 | | | | | INTP4 |
| P05 | | | | | INTP5 |
| P06 | | | | | INTP6 |
| P07 Note 1 | Input | | Input only | Input | XT1 |
| P10 to P17 | Input/ output | Port 1 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. Note 2 | Input | ANI0 to ANI7 | |
| P20 | Input/ output | Port 2 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. | Input | SI1 | |
| P21 | | | | SO1 | |
| P22 | | | | $\overline{\text{SCK}}1$ | |
| P23 | | | | STB | |
| P24 | | | | BUSY | |
| P25 | | | | SI0/SB0/SDA0 | |
| P26 | | | | SO0/SB1/SDA1 | |
| P27 | | | | $\overline{\text{SCK}}0/\text{SCL}$ | |
| P30 | Input/ output | Port 3 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. | Input | TO0 | |
| P31 | | | | TO1 | |
| P32 | | | | TO2 | |
| P33 | | | | TI1 | |
| P34 | | | | TI2 | |
| P35 | | | | PCL | |
| P36 | | | | BUZ | |
| P37 | | | | — | |
| P40 to P47 | Input/ output | Port 4 8-bit input/output port. Input/output can be specified in 8-bit unit. When used as an input port, on-chip pull-up resistor can be used by software. Test input flag (KRIF) is set to 1 by falling edge detection. | Input | AD0 to AD7 | |

Notes 1. When using the P07/XT1 pins as an input port, set 1 in bit 6 (FRC) of the processor clock control register. On-chip feedback resistor of the subsystem clock oscillator should not be used.

2. When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input pins, use of the on-chip pull-up resistor is cancelled automatically.

3.1 Port Pins (2/2)

| Pin Name | I/O | Function | | After Reset | Alternate Function |
|--------------|--------------|---|--|------------------------|--------------------|
| P50 to P57 | Input/output | Port 5 8-bit input/output port. LED can be driven directly. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. | | Input | A8 to A15 |
| P60 | Input/output | Port 6 8-bit input/output port. Input/output can be specified bit-wise. | N-ch open-drain input/output port. On-chip pull-up resistor can be specified by mask option. LED can be driven directly. | Input | — |
| P61 | | | | | |
| P62 | | | | | |
| P63 | | | | | |
| P64 | | | When used as an input port, on-chip pull-up resistor can be used by software. | Input | \overline{RD} |
| P65 | | | | | \overline{WR} |
| P66 | | | | | \overline{WAIT} |
| P67 | | | | | ASTB |
| P70 | Input/output | Port 7 3-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. | Input | $\overline{SI2/RxD}$ | |
| P71 | | | | $\overline{SO2/TxD}$ | |
| P72 | | | | $\overline{SCK2/ASCK}$ | |
| P120 to P127 | Input/output | Port 12 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. | | Input | RTP0 to RTP7 |
| P130, P131 | Input/output | Port 13 2-bit input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. | | Input | ANO0, ANO1 |

Caution For pins which also function as port pins, do not perform the following operations during A/D conversion. If these operations are performed, the total error ratings cannot be kept (except for LCD segment output alternate-function pin).

- (1) Rewrite the output latch which the pin is used as a port pin.
- (2) Change the output level of the pin used as an output pin, even if it is not used as a port pin.

3.2 Non-port Pins (1/2)

| Pin Name | I/O | Function | After Reset | Alternate Function |
|--------------------------|---------------|--|-------------|-------------------------------|
| INTP0 | Input | External interrupt request input by which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified. | Input | P00/TI00 |
| INTP1 | | | | P01/TI01 |
| INTP2 | | | | P02 |
| INTP3 | | | | P03 |
| INTP4 | | | | P04 |
| INTP5 | | | | P05 |
| INTP6 | | | | P06 |
| SI0 | Input | Serial interface serial data input. | Input | P25/SB0/SDA0 |
| SI1 | | | | P20 |
| SI2 | | | | P70/RxD |
| SO0 | Output | Serial interface serial data output. | Input | P26/SB1/SDA1 |
| SO1 | | | | P21 |
| SO2 | | | | P71/TxD |
| SB0 | Input /output | Serial interface serial data input/output. | Input | P25/SI0/SDA0 |
| SB1 | | | | P26/SO0/SDA1 |
| SDA0 | | | | P25/SI0/SB0 |
| SDA1 | | | | P26/SO0/SBI |
| $\overline{\text{SCK0}}$ | Input /output | Serial interface serial clock input/ output | Input | P27/SCL |
| $\overline{\text{SCK1}}$ | | | | P22 |
| $\overline{\text{SCK2}}$ | | | | P72/ASCK |
| SCL | | | | P27/ $\overline{\text{SCK0}}$ |
| STB | Output | Serial interface automatic transmit/receive strobe output. | Input | P23 |
| BUSY | Input | Serial interface automatic transmit/receive busy input. | Input | P24 |
| RxD | Input | Asynchronous serial interface serial data input. | Input | P70/SI2 |
| TxD | Output | Asynchronous serial interface serial data output. | Input | P71/SO2 |
| ASCK | Input | Asynchronous serial interface serial clock input. | Input | P72/ $\overline{\text{SCK2}}$ |
| TI00 | Input | External count clock input to the 16-bit timer (TM0) | Input | P00/INTP0 |
| TI01 | | Capture trigger signal input to the capture register (CR00) | | P01/INTP1 |
| TI1 | | External count clock input to the 8-bit timer (TM1) | | P33 |
| TI2 | | External count clock input to the 8-bit timer (TM2) | | P34 |
| TO0 | Output | 16-bit timer (TM0) output (alternate function as 14-bit PWM output) | Input | P30 |
| TO1 | | 8-bit timer (TM1) output | | P31 |
| TO2 | | 8-bit timer (TM2) | | P32 |
| PCL | Output | Clock output (for main system clock, subsystem clock trimming). | Input | P35 |
| BUZ | Output | Buzzer output. | Input | P36 |
| RTP0 to RTP7 | Output | Real-time output port by which data is output in synchronization with a trigger. | Input | P120 to P127 |
| AD0 to AD7 | Input /output | Low-order address/data bus at external memory expansion. | Input | P40 to P47 |

3.2 Non-port Pins (2/2)

| Pin Name | I/O | Function | After Reset | Alternate Function |
|--------------------|--------|---|-------------|--------------------|
| A8 to A15 | Output | High-order address bus at external memory expansion. | Input | P50 to P57 |
| \overline{RD} | Output | External memory read operation strobe signal output. | Input | P64 |
| \overline{WR} | | External memory write operation strobe signal output. | | P65 |
| \overline{WAIT} | Input | Wait insertion at external memory access. | Input | P66 |
| ASTB | Output | Strobe output which latches the address information output at port 4 to access external memory. | Input | P67 |
| ANI0 to ANI7 | Input | A/D converter analog input. | Input | P10 to P17 |
| ANO0, ANO1 | Output | D/A converter analog output. | Input | P130, P131 |
| AVREF0 | Input | A/D converter reference voltage input. | — | — |
| AVREF1 | Input | D/A converter reference voltage input. | — | — |
| AVDD | — | A/D converter analog power supply (shared with the port power supply) | — | — |
| AVSS | — | A/D and D/A converter ground potential (shared with the port ground potential) | — | — |
| \overline{RESET} | Input | System reset input. | — | — |
| X1 | Input | Main system clock oscillation crystal connection. | — | — |
| X2 | — | | — | — |
| XT1 | Input | Subsystem clock oscillation crystal connection. | Input | P07 |
| XT2 | — | | — | — |
| VDD | — | Positive power supply (except for port). | — | — |
| VSS | — | Ground potential (except for port). | — | — |
| IC | — | Internally connected. Connect directly to VSS. | — | — |

- Cautions**
1. The AVDD pin functions as both an A/D converter power supply and a port power supply. When the μPD78056FY and 78058FY are used in applications where the noise generated inside the microcontroller needs to be reduced, connect the AVDD pin to another power supply which has the same potential as VDD.
 2. The AVSS pin functions as both an A/D converter and D/A converter ground and as a port ground. When the μPD78056FY and 78058FY are used in applications where the noise generated inside the microcontroller needs to be reduced, connect the AVSS pin to a ground line other than VSS.

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, see Figure 3-1.

Table 3-1. Input/Output Circuit Type of Each Pin (1/2)

| Pin Name | Input/output Circuit Type | I/O | Recommended Connection when not Used | |
|------------------------------------|---------------------------|--------------|---|---|
| P00/INTP0/TI00 | 2 | Input | Connected to V _{SS} . | |
| P01/INTP1/TI01 | 8-D | Input/output | Independently connect to V _{SS} through resistor. | |
| P02/INTP2 | | | | |
| P03/INTP3 | | | | |
| P04/INTP4 | | | | |
| P05/INTP5 | | | | |
| P06/INTP6 | | | | |
| P07/XT1 | 16 | Input | Connect to V _{DD} . | |
| P10/ANI0 to P17/ANI7 | 11-C | Input/output | Independently connect to V _{DD} or V _{SS} through resistor. | |
| P20/SI1 | 8-D | | | |
| P21/SO1 | 5-J | | | |
| P22/ $\overline{\text{SCK1}}$ | 8-D | | | |
| P23/STB | 5-J | | | |
| P24/BUSY | 8-D | | | |
| P25/SI0/SB0/SDA0 | 10-C | | | |
| P26/SO0/SB1/SDA1 | | | | |
| P27/ $\overline{\text{SCK0}}$ /SCL | | | | |
| P30/TO0 | 5-J | | | |
| P31/TO1 | | | | |
| P32/TO2 | | | | |
| P33/TI1 | 8-D | | | |
| P34/TI2 | | | | |
| P35/PCL | 5-J | | | |
| P36/BUZ | | | | |
| P37 | | | | |
| P40/AD0 to P47/AD7 | 5-O | | | Independently connect to V _{DD} through resistor. |
| P50/A8 to P57/A15 | 5-J | | | Independently connect to V _{DD} or V _{SS} through resistor. |
| P60 to P63 | 13-I | | | Independently connect to V _{DD} through resistor. |
| P64/ $\overline{\text{RD}}$ | 5-J | | | Independently connect to V _{DD} or V _{SS} through resistor. |
| P65/ $\overline{\text{WR}}$ | | | | |
| P66/ $\overline{\text{WAIT}}$ | | | | |
| P67/ASTB | | | | |

Table 3-1. Input/Output Circuit Type of Each Pin (2/2)

| Pin Name | Input/output Circuit Type | I/O | Recommended Connection when not Used |
|---------------------------|---------------------------|------------------|---|
| P70/SI2/RxD | 8-D | Input/ output | Independently connect to V _{DD} or V _{SS} through resistor. |
| P71/SO2/TxD | 5-J | | |
| P72/SCK2/ASCK | 8-D | | |
| P120/RTP0 to P127/RTP7 | 5-J | | |
| P130/ANO0 , P131/ANO1 | 12-B | Input/ output | Independently connect to V _{SS} through resistor. |
| RESET | 2 | Input | — |
| XT2 | 16 | — | Leave open. |
| AV _{REF0} | — | | Connect to V _{SS} . |
| AV _{REF1} | | | Connect to V _{DD} . |
| AV _{DD} | | | Connect to another power supply which has the same potential as V _{DD} . |
| AV _{SS} | | | Connect to another ground line which has the same potential as V _{SS} . |
| IC | | | Connect directly to V _{SS} . |
| | | | |

Figure 3-1. Pin Input/Output Circuits (1/2)

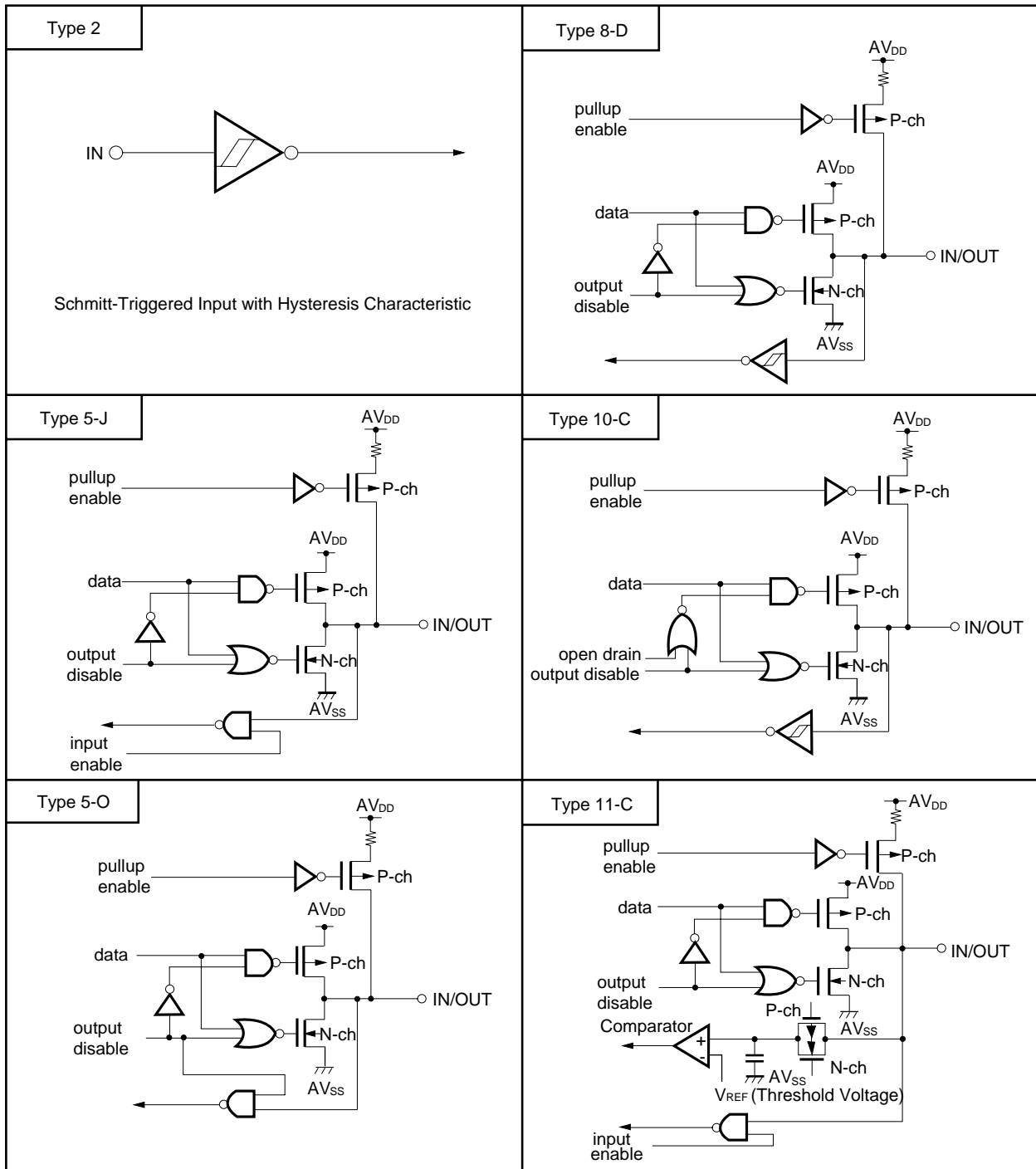
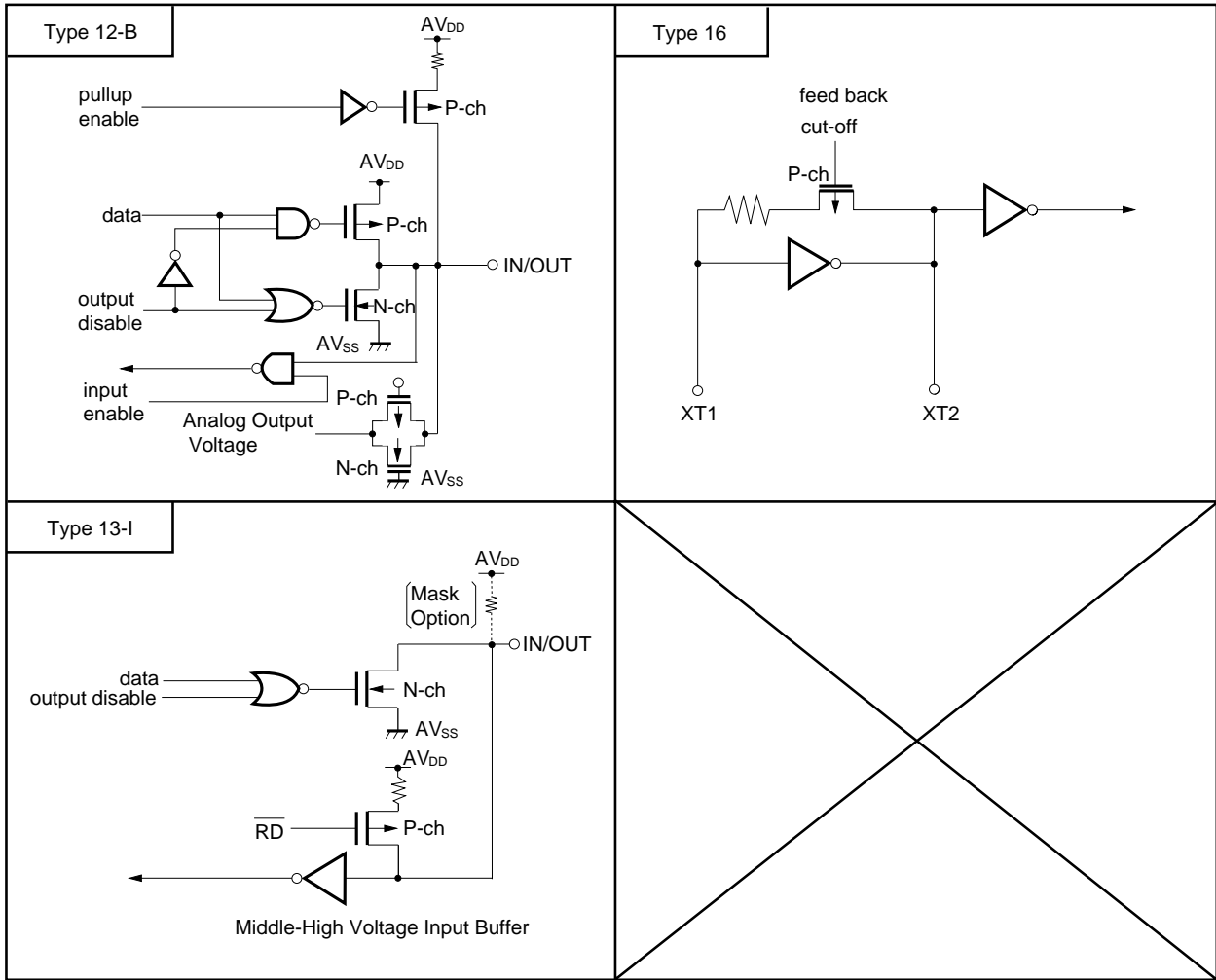


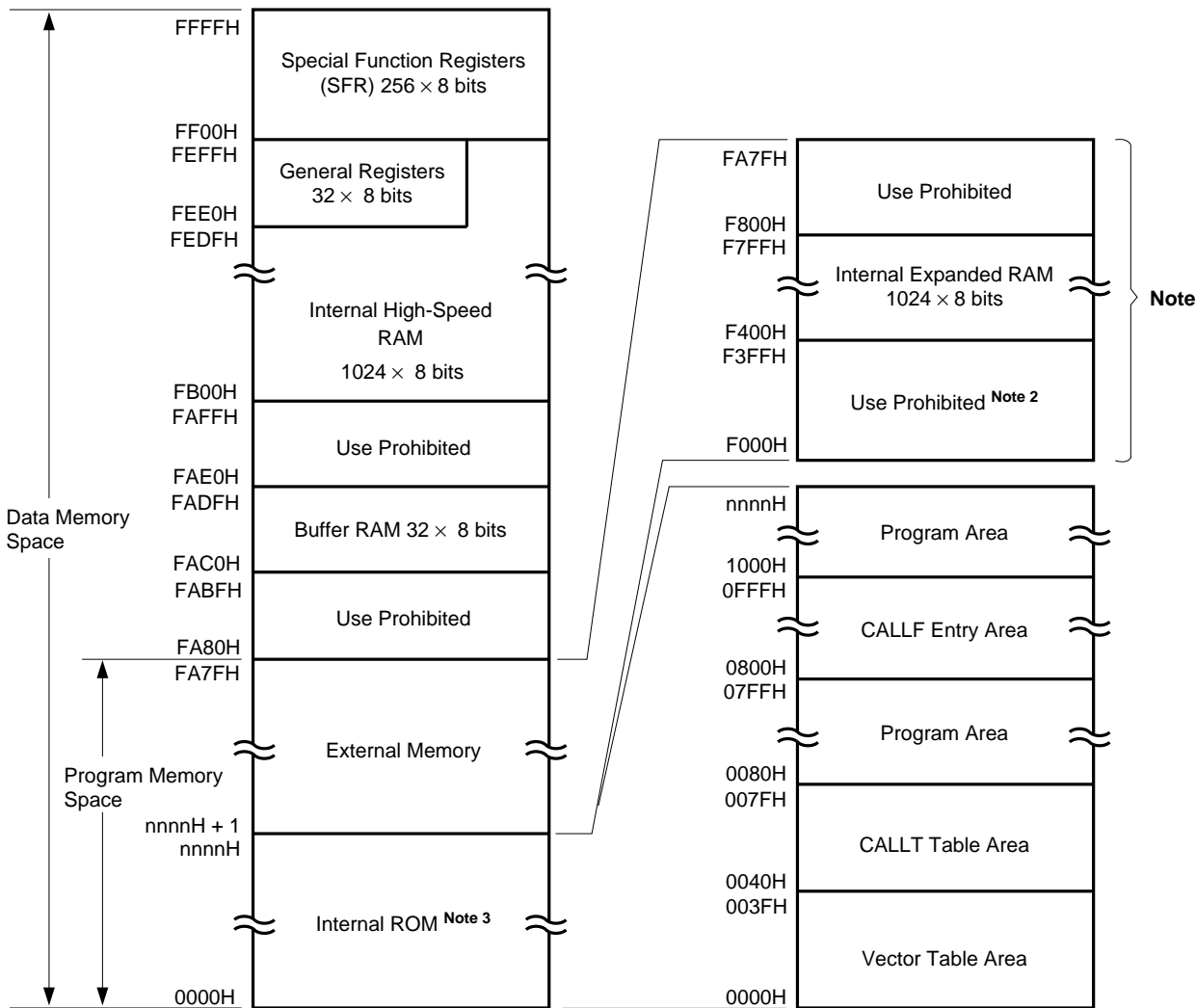
Figure 3-1. Pin Input/Output Circuits (2/2)



4. MEMORY SPACE

Figure 4-1 shows the memory map of the μPD78056FY,78058FY.

Figure 4-1. Memory Map



Notes 1. μPD78058FY only

2. When the external device expansion function is used with the μPD78058FY, set the internal ROM capacity to 56 Kbytes or less using the memory size switching register (IMS).
3. The internal ROM capacity and internal high-speed RAM capacity depend on the products (see the table below).

| Target Product | Internal ROM Last Address nnnnH |
|----------------|------------------------------------|
| μPD78056FY | BFFFH |
| μPD78058FY | EFFFH |

5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 Ports

The following 3 types of I/O ports are available.

| | |
|--|-------------|
| • CMOS input (P00, P07) | : 2 |
| • CMOS input/output (P01 to P06, port 1 to port 5, P64 to P67, port 7, port 12, port 13) | : 63 |
| • N-channel open-drain input/output (P60 to P63) | : 4 |
| Total | : 69 |

Table 5-1. Port Functions

| Name | Pin Name | Function |
|---------|--------------|--|
| Port 0 | P00, P07 | Dedicated input port pins |
| | P01 to P06 | Input/output port pins. Input/output specifiable bit-wise. When used as input/output port pins, on-chip pull-up resistor can be used by software. |
| Port 1 | P10 to P17 | Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software. |
| Port 2 | P20 to P27 | Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software. |
| Port 3 | P30 to P37 | Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software. |
| Port 4 | P40 to P47 | Input/output port pins. Input/output specifiable in 8-bit units. When used as input port pins, on-chip pull-up resistor can be used by software. Test input flag (KRIF) is set to 1 by falling edge detection. |
| Port 5 | P50 to P57 | Input/output port pins. Input/output specifiable bit-wise. When used as input port pins, on-chip pull-up resistor can be used by software. LED direct drive capability. |
| Port 6 | P60 to P63 | N-channel open-drain input/output port pins. Input/output specifiable bit-wise. On-chip pull-up resistor can be used by mask option. LED direct drive capability. |
| | P64 to P67 | Input/output port pins. Input/output specifiable bit-wise. When used as input/output port pins, on-chip pull-up resistor can be used by software. |
| Port 7 | P70 to P72 | Input/output port pins. Input/output specifiable bit-wise. When used as input/output port pins, on-chip pull-up resistor can be used by software. |
| Port 12 | P120 to P127 | Input/output port pins. Input/output specifiable bit-wise. When used as input/output port pins, on-chip pull-up resistor can be used by software. |
| Port 13 | P130, P131 | Input/output port pins. Input/output specifiable bit-wise. When used as input/output port pins, on-chip pull-up resistor can be used by software. |

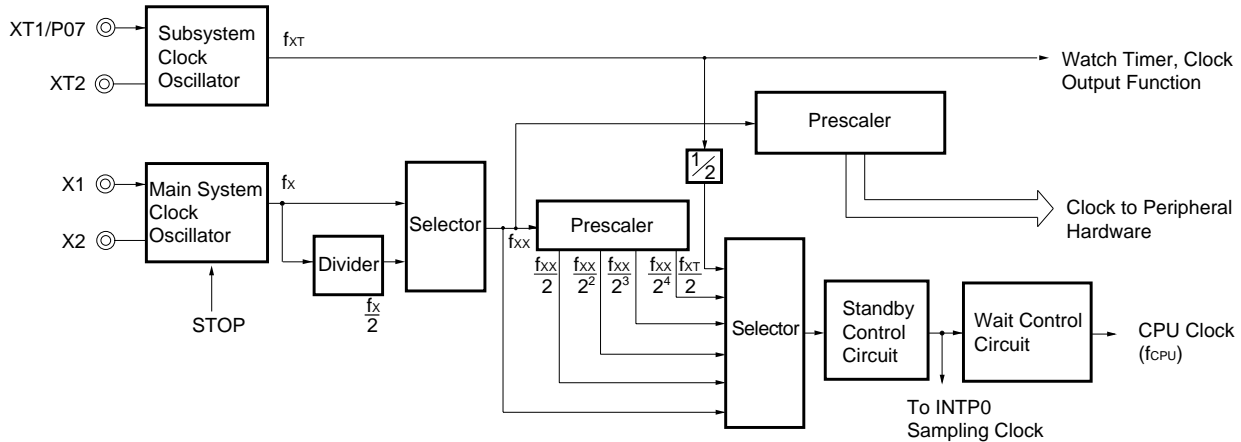
5.2 Clock Generator

Two types of generators, a main system clock generator and a subsystem clock generator, are available.

The minimum instruction execution time can also be changed.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (main system clock: at 5.0-MHz operation)
- 122 μs (subsystem clock: at 32.768-kHz operation)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer/Event Counter

5 timer/event counter channels are incorporated.

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2. Operation of Timer/Event Counter

| | 16-Bit Timer/Event Counter | 8-Bit Timer/Event Counter | Watch Timer | Watchdog Timer |
|-------------------------|----------------------------|---------------------------|-------------|----------------|
| Operation mode | | | | |
| Interval timer | 1 channel | 2 channels | 1 channel | 1 channel |
| External event counter | 1 channel | 2 channels | — | — |
| Function | | | | |
| Timer output | 1 output | 2 outputs | — | — |
| PWM output | 1 output | — | — | — |
| Pulse width measurement | 2 input | — | — | — |
| Square wave output | 1 output | 2 outputs | — | — |
| One-shot pulse output | 1 output | — | — | — |
| Interrupt request | 2 | 2 | 1 | 1 |
| Test input | — | — | 1 input | — |

Figure 5-2. 16-Bit Timer/Event Counter Block Diagram

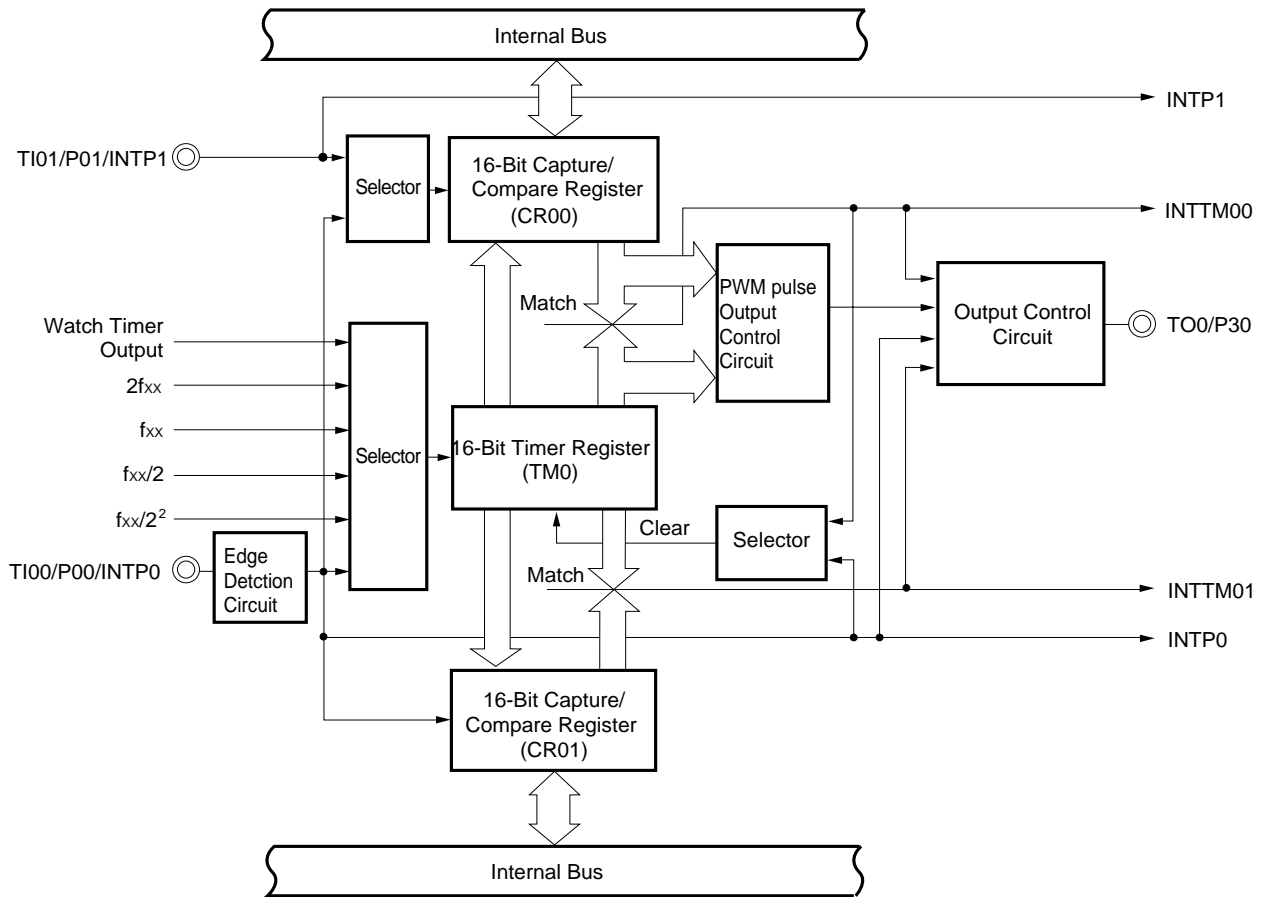


Figure 5-3. 8-Bit Timer/Event Counter Block Diagram

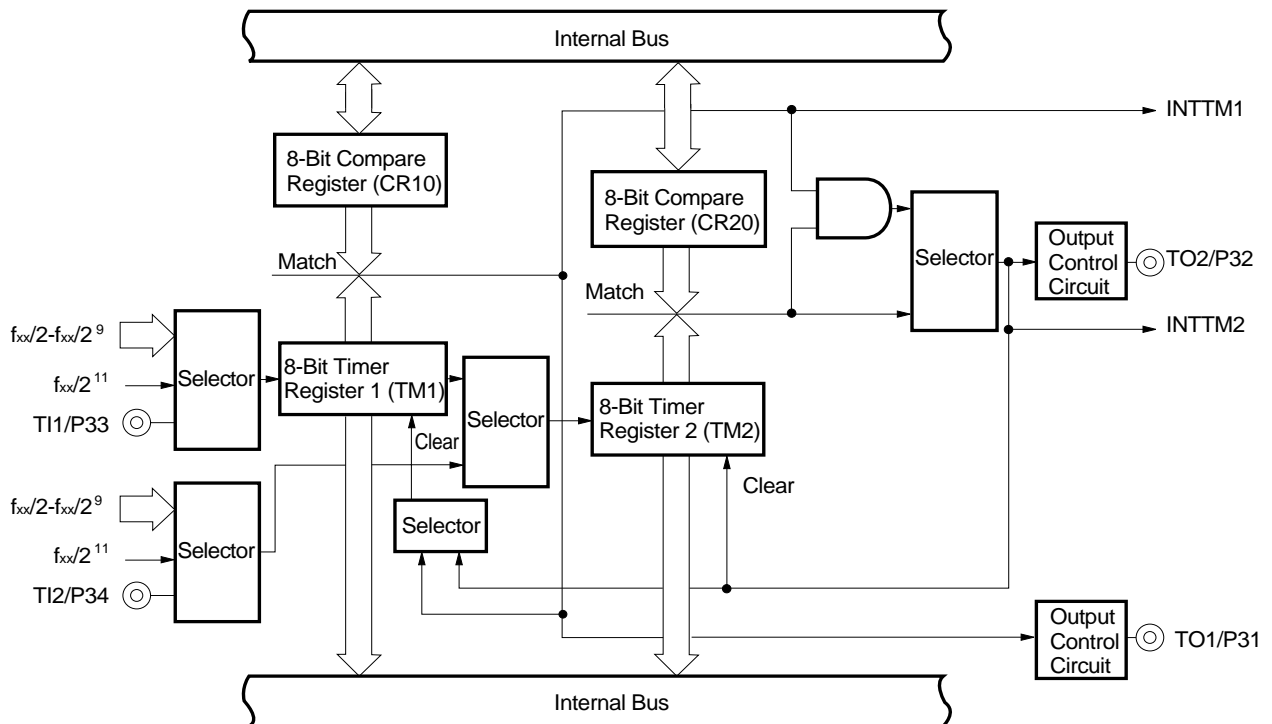


Figure 5-4. Watch Timer Block Diagram

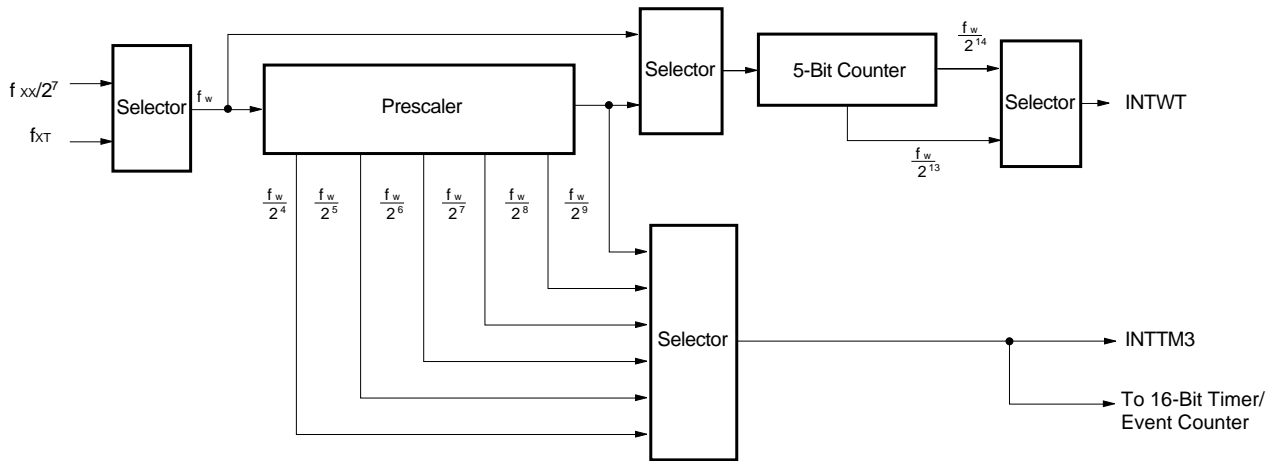
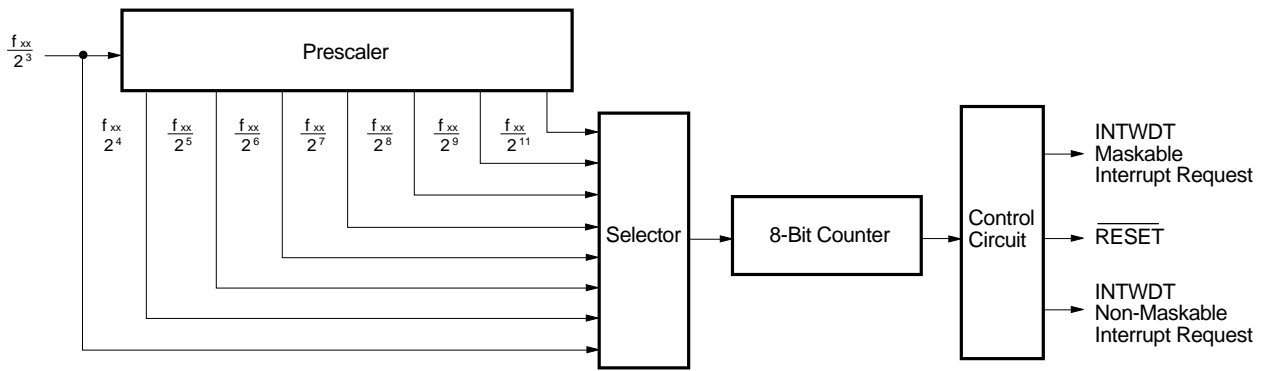


Figure 5-5. Watchdog Timer Block Diagram

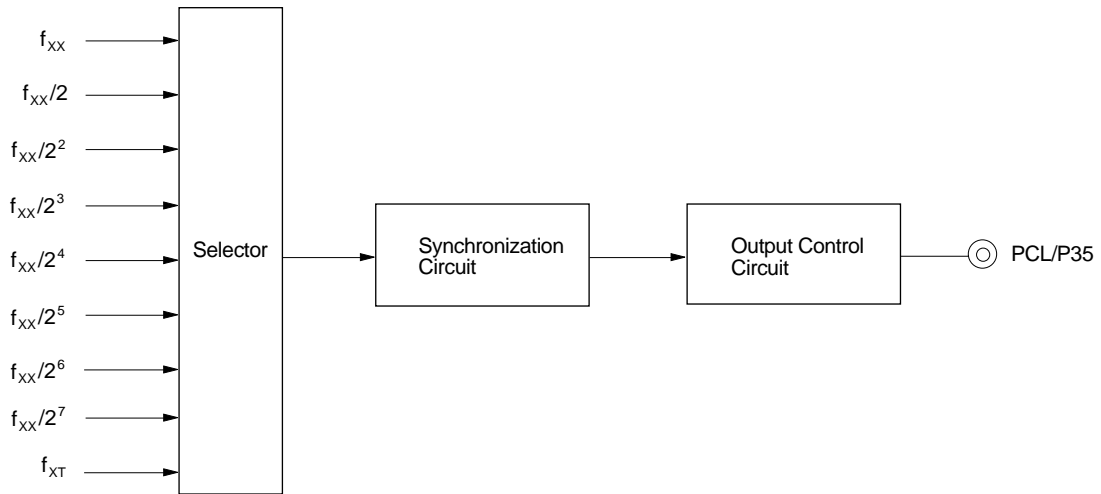


5.4 Clock Output Control Circuit

Clock with the following frequencies can be output as clock output.

- 19.5 kHz/39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz/2.5 MHz/5.0 MHz (main system clock: at 5.0-MHz operation)
- 32.768 kHz (subsystem clock: at 32.768-kHz operation)

Figure 5-6. Clock Output Control Block Diagram

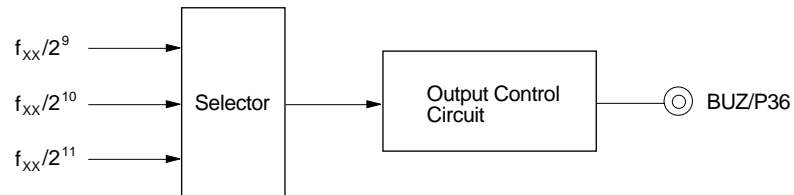


5.5 Buzzer Output Control Circuit

Clock with the following frequencies can be output as buzzer output.

- 1.2 kHz/2.4 kHz/4.9 kHz/9.8 kHz (main system clock: at 5.0-MHz operation)

Figure 5-7. Buzzer Output Control Circuit Block Diagram



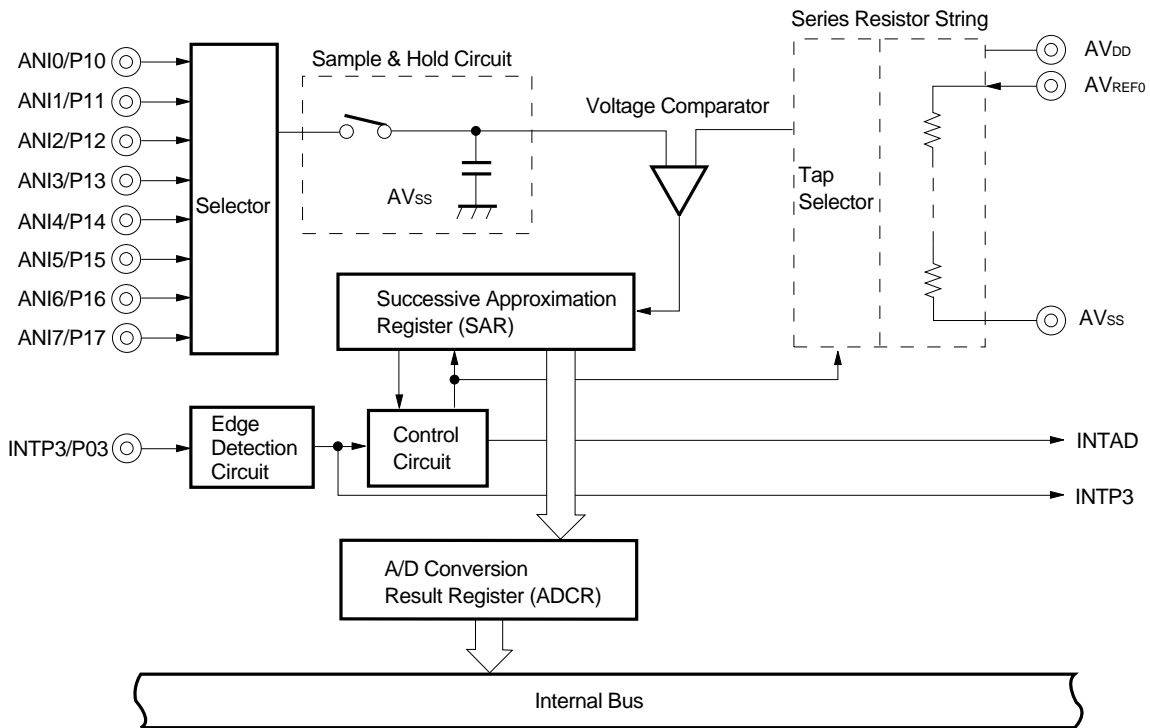
5.6 A/D Converter

An A/D converter of 8-bit resolution × 8 channels is incorporated.

The following two types of A/D conversion operation start-up methods are available.

- Hardware start
- Software start

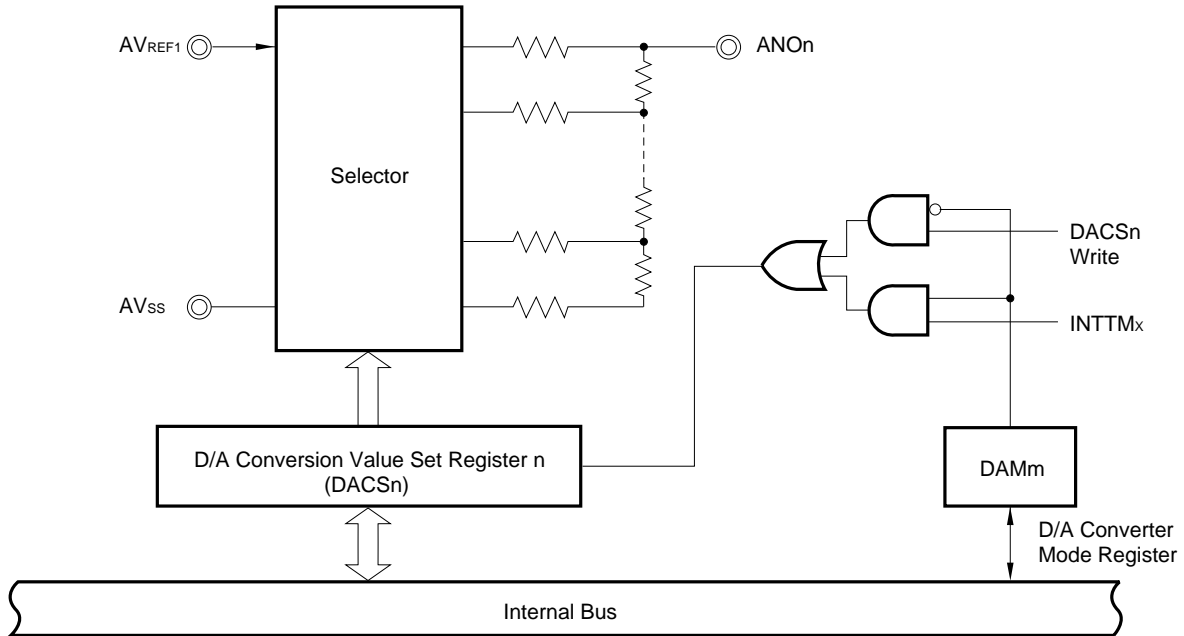
Figure 5-8. A/D Converter Block Diagram



5.7 D/A Converter

A D/A converter of 8-bit resolution × 2 channels is available.
The conversion method is the R-2R resistor ladder method.

Figure 5-9. D/A Converter Block Diagram



n = 0, 1
m = 4, 5
x = 1, 2

5.8 Serial Interfaces

3 channels of the clocked serial interface are incorporated.

- Serial interface channel 0
- Serial interface channel 1
- Serial interface channel 2

Table 5-3. Types and Functions of Serial Interface

| Function | Serial Interface Channel 0 | Serial Interface Channel 1 | Serial Interface Channel 2 |
|--|------------------------------|------------------------------|--|
| 3-wire serial I/O mode | ○ (MSB/LSB first switchable) | ○ (MSB/LSB first switchable) | ○ (MSB/LSB first switchable) |
| 3-wire serial I/O mode with auto-matic transmission/reception function | — | ○ (MSB/LSB first switchable) | — |
| 2-wire serial I/O mode | ○ (MSB first) | — | — |
| I ² C bus mode | ○ (MSB first) | — | — |
| Asynchronous serial interface (UART) mode | — | — | ○ (Dedicated baud rate generator incorporated) |

Figure 5-10. Serial Interface Channel 0 Block Diagram

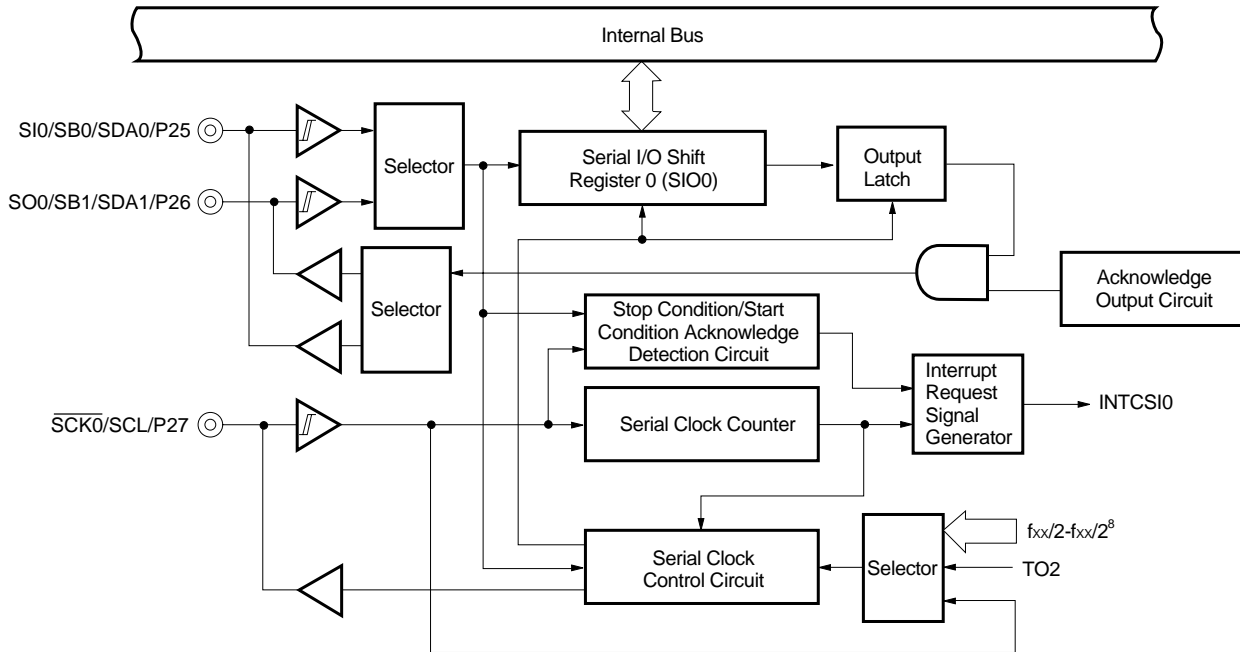


Figure 5-11. Serial Interface Channel 1 Block Diagram

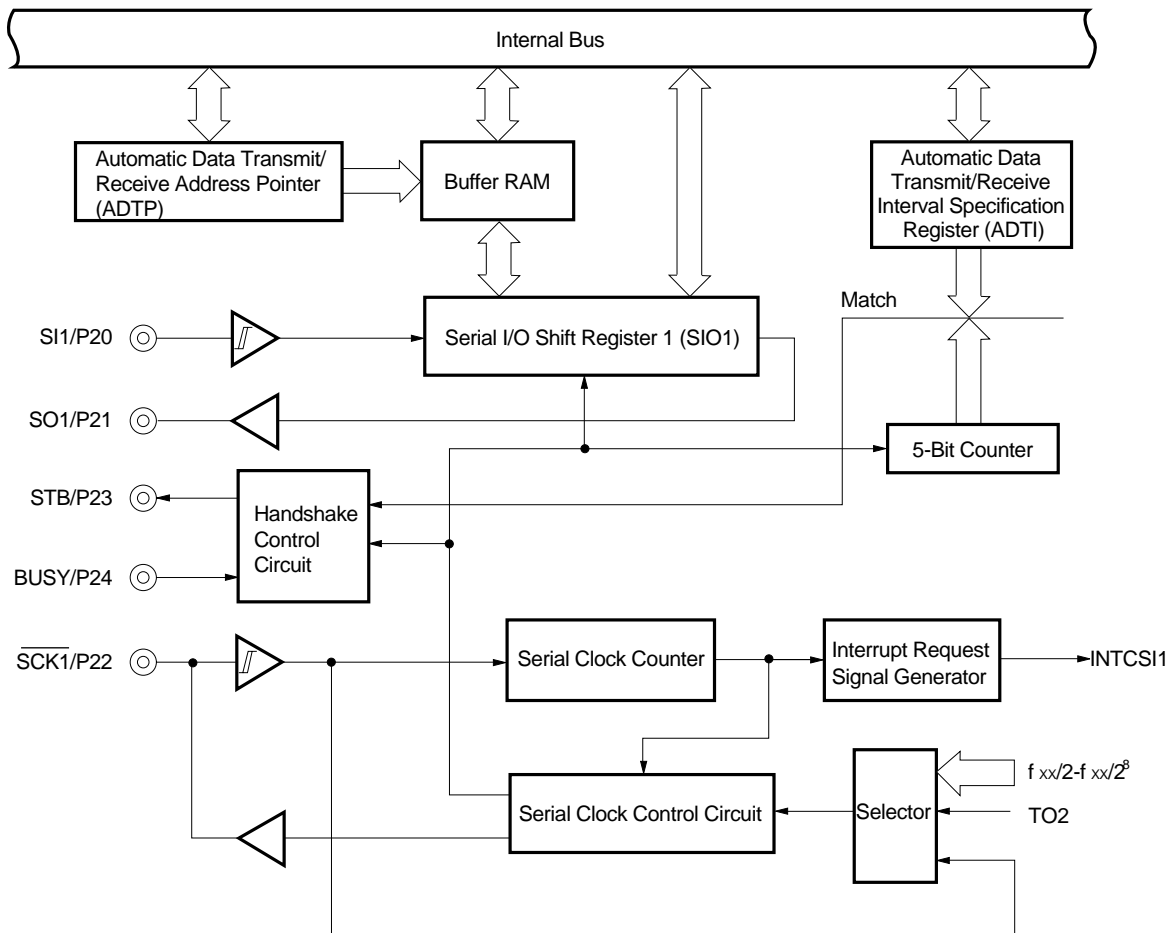
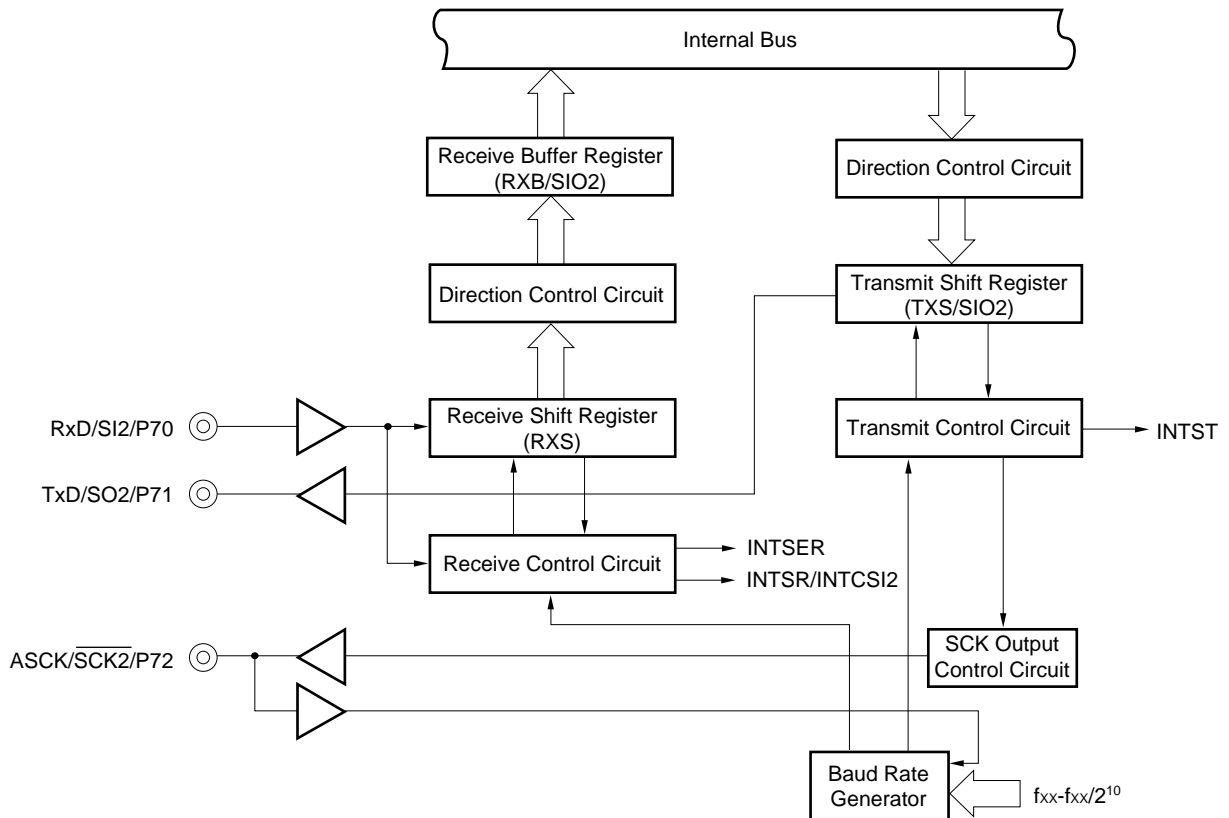


Figure 5-12. Serial Interface Channel 2 Block Diagram

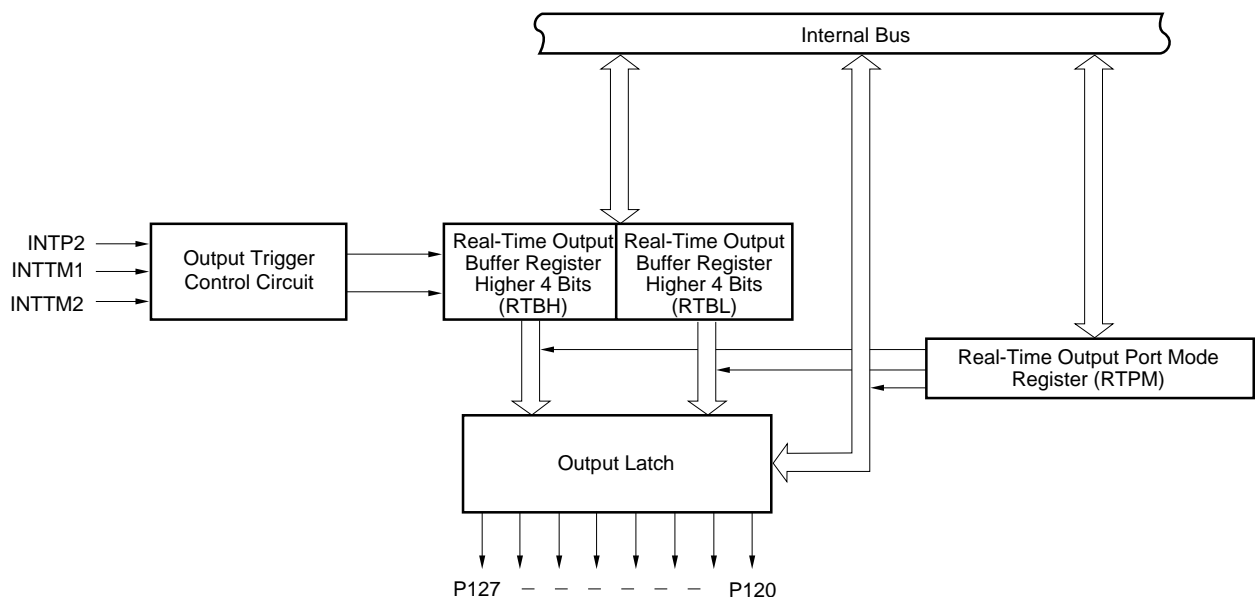


5.9 Real-Time Output Port Functions

Data set previously in the real-time output buffer register is transferred to the output latch by hardware concurrently with timer interrupt request and external interrupt request generation in order to output to off-chip. This is a real-time output function. Pins to output to off-chip are called real-time output ports.

By using a real-time output port, a signal which has no jitter can be output. This is most applicable to control of stepping motors, etc.

Figure 5-13. Real-Time Output Port Block Diagram



6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

6.1 Interrupt Functions

There are 22 interrupt functions of 3 different kinds, as shown below.

- Non-maskable : 1
- Maskable : 20
- Software : 1

Table 6-1. Interrupt Source List (1/2)

| Interrupt Type | Note 1 Default Priority | Interrupt Source | | Internal/ External | Vector Table Address | Basic Configuration Type Note 2 |
|----------------|-------------------------------|------------------|---|-----------------------|--|---------------------------------------|
| | | Name | Trigger | | | |
| Non-maskable | — | INTWDT | Watchdog timer overflow (watchdog timer mode 1 selected) | Internal | 0004H | (A) |
| Maskable | 0 | INTWDT | Watchdog timer overflow (interval timer mode selected) | | | (B) |
| | 1 | INTP0 | Pin input edge detection | External | 0006H | (C) |
| | 2 | INTP1 | | | 0008H | |
| | 3 | INTP2 | | | 000AH | |
| | 4 | INTP3 | | | 000CH | |
| | 5 | INTP4 | | | 000EH | |
| | 6 | INTP5 | | | 0010H | |
| | 7 | INTP6 | | | 0012H | |
| | 8 | INTCSI0 | | | End of serial interface channel 0 transfer | |
| | 9 | INTCSI1 | End of serial interface channel 1 transfer | 0016H | | |
| | 10 | INTSER | Generation of serial interface channel 2 UART receive error | 0018H | | |
| | 11 | INTSR | End of serial interface channel 2 UART reception | 001AH | | |
| | | INTCSI2 | End of serial interface channel 2 3-wire transfer | | | |
| | 12 | INTST | End of serial interface channel 2 UART transmission | | 001CH | |

Notes 1. The default priority is a priority order when two or more maskable interrupt requests are generated simultaneously. 0 is the highest order and 18, the lowest.

2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 6-1, respectively.

Table 6-1. Interrupt Source List (2/2)

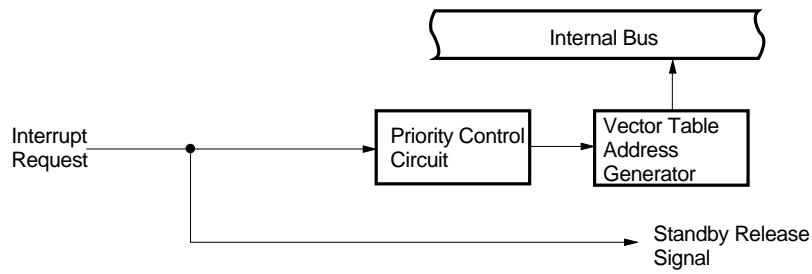
| Interrupt Type | Note 1 Default Priority | Interrupt Source | | Internal/ External | Vector Table Address | Basic Configuration Type Note 2 |
|----------------|-------------------------------|------------------|---|-----------------------|-------------------------|---------------------------------------|
| | | Name | Trigger | | | |
| Maskable | 13 | INTTM3 | Referencetime interval signal from watch timer | Internal | 001EH | (B) |
| | 14 | INTTM00 | Generation of match signal of 16-bit timer register and capture/compare register (CR00) | | 0020H | |
| | 15 | INTTM01 | Generation of match signal of 16-bit timer register and capture/compare register (CR01) | | 0022H | |
| | 16 | INTTM1 | Generation of match signal of 8-bit timer/event counter 1 | | 0024H | |
| | 17 | INTTM2 | Generation of match signal of 8-bit timer/ event counter 2 | | 0026H | |
| | 18 | INTAD | End of conversion by A/D converter | | 0028H | |
| Software | — | BRK | BRK instruction execution | — | 003EH | (E) |

Notes 1. The default priority is a priority order when two or more maskable interrupt requests are generated simultaneously. 0 is the highest order and 18, the lowest.

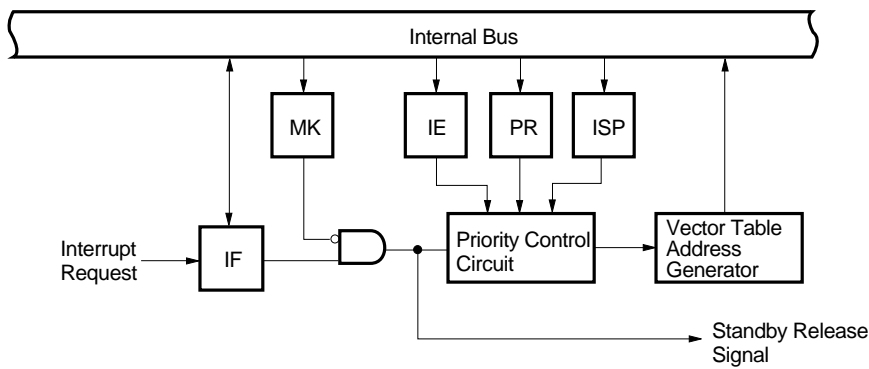
2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 6-1, respectively.

Figure 6-1. Interrupt Function Basic Configuration (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0)

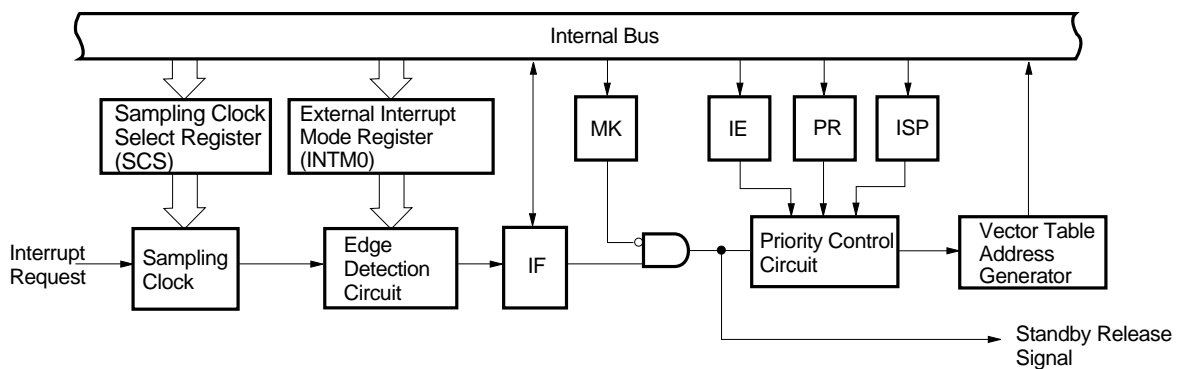
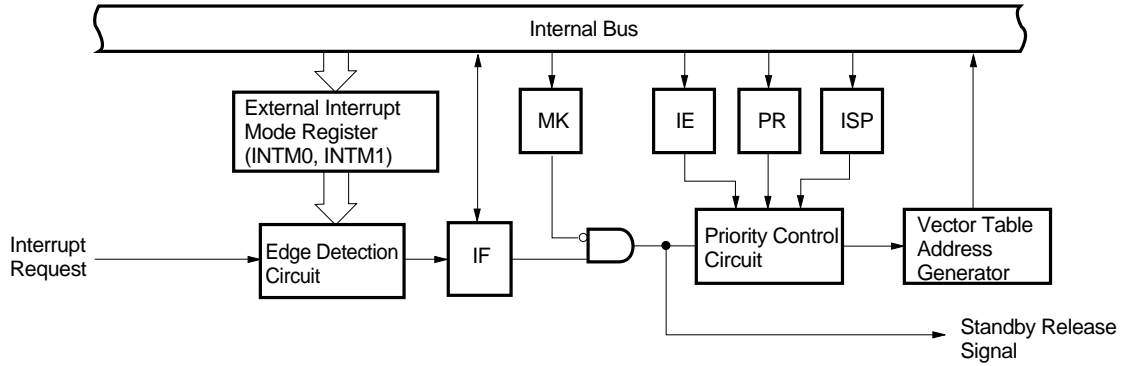
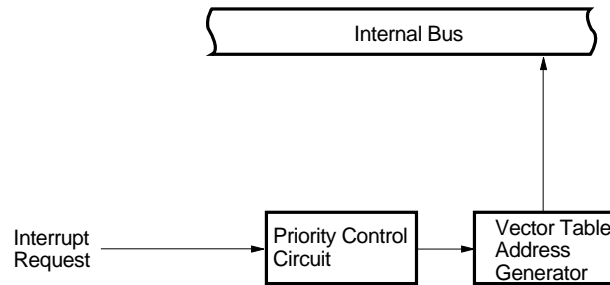


Figure 6-1. Interrupt Function Basic Configuration (2/2)

(D) External maskable interrupt (except INTP0)



(E) Software interrupt



- IF** : Interrupt request flag
- IE** : Interrupt enable flag
- ISP** : In-service priority flag
- MK** : Interrupt mask flag
- PR** : Priority specification flag

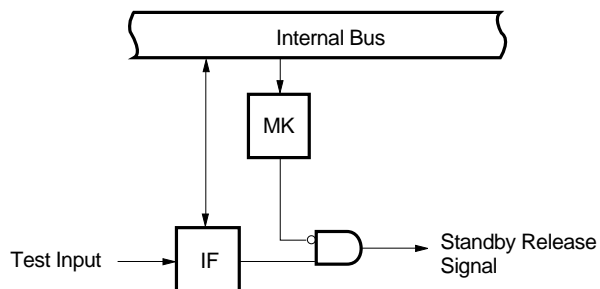
6.2 Test Functions

There are two test functions as shown in Table 6-2.

Table 6-2. Test Input Source List

| Test Input Source | | Internal/External |
|-------------------|-------------------------------|-------------------|
| Name | Trigger | |
| INTWT | Watch timer overflow | Internal |
| INTPT4 | Port 4 falling edge detection | External |

Figure 6-2. Test Function Basic Configuration



IF : Test input flag
 MK : Test mask flag

7. EXTERNAL DEVICE EXPANSION FUNCTIONS

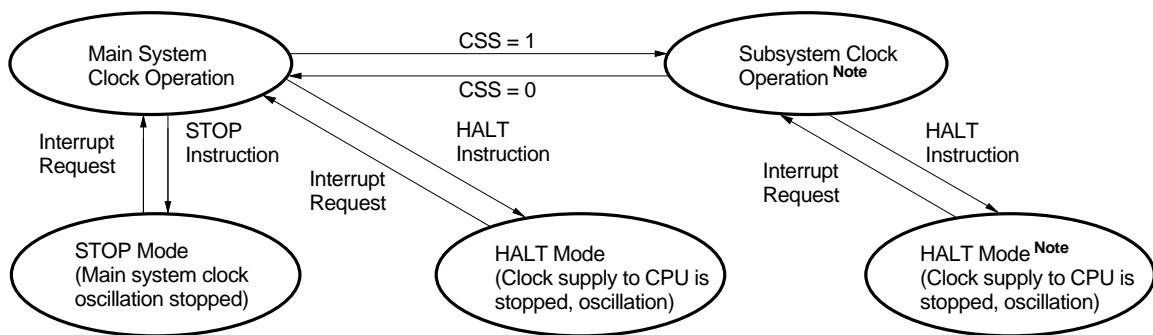
The external device expansion functions connect external devices to areas other than the internal ROM, RAM and SFR. Ports 4 to 6 are used for external device connection.

8. STANDBY FUNCTION

There are the following two standby functions to reduce the system power consumption.

- HALT mode : The CPU operating clock is stopped.
The average consumption current can be reduced by intermittent operation in combination with the normal operating mode.
- STOP mode : The main system clock oscillation is stopped. The whole operation by the main system clock is stopped, so that the system operates with ultra-low power consumption using only the subsystem clock.

Figure 8-1. Stand-by Function



Note The power consumption can be reduced by stopping the main system clock. When the CPU is operating on the subsystem clock, set bit 7 (MCC) in the processor clock control register (PCC) to stop the main system clock. The STOP instruction cannot be used.

Caution When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

Remark CSS : bit 4 in the PCC

9. RESET FUNCTION

There are the following two reset methods.

- External reset input by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog time runaway time detection

10. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

| Second Operand First Operand | #byte | A | r Note | sfr | saddr | !addr16 | PSW | [DE] | [HL] | [HL + Byte] [HL + B] [HL + C] | \$saddr16 | 1 | None |
|-------------------------------------|--|--|---|------------|---|---|-----|------------|---|---|-----------|----------------------------|--------------|
| A | ADD ADDC SUB SUBC AND OR XOR CMP | | MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP | MOV XCH | MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP | MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP | MOV | MOV XCH | MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP | MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP | | ROR ROL RORC ROLC | |
| r | MOV | MOV ADD ADDC SUB SUBC AND OR XOR CMP | | | | | | | | | | | INC DEC |
| B, C | | | | | | | | | | | DBNZ | | |
| sfr | MOV | MOV | | | | | | | | | | | |
| saddr | MOV ADD ADDC SUB SUBC AND OR XOR CMP | MOV | | | | | | | | | DBNZ | | INC DEC |
| !addr16 | | MOV | | | | | | | | | | | |
| PSW | MOV | MOV | | | | | | | | | | | PUSH POP |
| [DE] | | MOV | | | | | | | | | | | |
| [HL] | | MOV | | | | | | | | | | | ROR4 ROL4 |
| [HL + Byte] [HL + B] [HL + C] | | MOV | | | | | | | | | | | |
| X | | | | | | | | | | | | | MULU |
| C | | | | | | | | | | | | | DIVUW |

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

| Second Operand First Operand | #word | AX | rp ^{Note} | sfrp | saddrp | !addr16 | SP | None |
|---------------------------------|----------------------|----------------------|--------------------|------|--------|---------|------|-------------------------|
| AX | ADDW SUBW CMPW | | MOVW XCHW | MOVW | MOVW | MOVW | MOVW | |
| rp | MOVW | MOVW ^{Note} | | | | | | INCW, DECW PUSH, POP |
| sfrp | MOVW | MOVW | | | | | | |
| saddrp | MOVW | MOVW | | | | | | |
| !addr16 | | MOVW | | | | | | |
| SP | MOVW | MOVW | | | | | | |

Note Only when rp = BC, DE or HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

| Second Operand First Operand | A.bit | sfr.bit | saddr.bit | PSW.bit | [HL].bit | CY | \$addr16 | None |
|---------------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|------|-------------------|----------------------|
| A.bit | | | | | | MOV1 | BT BF BTCLR | SET1 CLR1 |
| sfr.bit | | | | | | MOV1 | BT BF BTCLR | SET1 CLR1 |
| saddr.bit | | | | | | MOV1 | BT BF BTCLR | SET1 CLR1 |
| PSW.bit | | | | | | MOV1 | BT BF BTCLR | SET1 CLR1 |
| [HL].bit | | | | | | MOV1 | BT BF BTCLR | SET1 CLR1 |
| CY | MOV1 AND1 OR1 XOR1 | MOV1 AND1 OR1 XOR1 | MOV1 AND1 OR1 XOR1 | MOV1 AND1 OR1 XOR1 | MOV1 AND1 OR1 XOR1 | | | SET1 CLR1 NOT1 |

(4) Call instruction/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

| Second Operand First Operand | AX | !addr16 | !addr11 | [addr5] | \$addr16 |
|---------------------------------|----|------------|---------|---------|-------------------------|
| Basic instruction | BR | CALL BR | CALLF | CALLT | BR, BC, BNC BZ, BNZ |
| Compound instruction | | | | | BT, BF BTCLR DBNZ |

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

| Parameter | Symbol | Test Conditions | | Rating | Unit | | |
|---------------------------|-----------------------------|---|------------------|---|------|-------------|----|
| Supply voltage | V _{DD} | | | -0.3 to + 7.0 | V | | |
| | AV _{DD} | | | -0.3 to V _{DD} + 0.3 | V | | |
| | AV _{REF0} | | | -0.3 to V _{DD} + 0.3 | V | | |
| | AV _{REF1} | | | -0.3 to V _{DD} + 0.3 | V | | |
| | AV _{SS} | | | -0.3 to + 0.3 | V | | |
| Input voltage | V _{I1} | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131, X1, X2, XT2 RESET | | -0.3 to V _{DD} + 0.3 | V | | |
| | V _{I2} | P60 to P63 | N-ch Open-drain | -0.3 to +16 | V | | |
| Output voltage | V _O | | | -0.3 to V _{DD} + 0.3 | V | | |
| Analog input voltage | V _{AN} | P10 to P17 | Analog input pin | AV _{SS} -0.3 to AV _{REF0} + 0.3 | V | | |
| High level output current | I _{OH} | 1 pin | | -10 | mA | | |
| | | P01 to P06, P30-P37, P56, P57, P60 to P67, P120 to P127 total | | -15 | mA | | |
| | | P10 to P17, P20 to P27, P40 to P47, P50 to P55, P70 to P72, P130, P131 total | | -15 | mA | | |
| Low level output current | I _{OL} Note | 1 pin | Peak value | 30 | mA | | |
| | | | Effective value | 15 | mA | | |
| | | P50 to P55 total | Peak value | 100 | mA | | |
| | | | Effective value | 70 | mA | | |
| | | P56, P57, P60 to P63 total | Peak value | 100 | mA | | |
| | | | Effective value | 70 | mA | | |
| | | P10 to P17, P20 to P27, P40 to P47, P70 to P72, P130, P131 total | Peak value | 50 | mA | | |
| | | | Effective value | 20 | mA | | |
| | | P01 to P06, P30 to P37, P64 to P67, P120 to P127 total | Peak value | 50 | mA | | |
| | | | Effective value | 20 | mA | | |
| | | Operating ambient temperature | T _A | | | -40 to +85 | °C |
| | | Storage temperature | T _{stg} | | | -65 to +150 | °C |

Note The effective value should be calculated as follows: [Effective value] = [Peak value] × √duty

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, alternate-function pin characteristics are the same as port pin characteristics.

Main System Clock Oscillation Circuit Characteristics (T_A = -40 to 85°C, V_{DD} = 2.7 to 6.0 V)

| Resonator | Recommended Circuit | Parameter | Test Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------|---------------------|--|---|------|------|----------|------|
| Ceramic resonator | | Oscillator frequency (f _x) Note 1 | V _{DD} = Oscillator voltage range | 1.0 | | 5.0 | MHz |
| | | Oscillation stabilization time Note 2 | After V _{DD} reaches oscillator voltage range MIN. | | | 4 | ms |
| Crystal resonator | | Oscillator frequency (f _x) Note 1 | | 1.0 | | 5.0 | MHz |
| | | Oscillation stabilization time Note 2 | V _{DD} = 4.5 to 6.0 V | | | 10 30 | ms |
| External clock | | X1 input frequency (f _x) Note 1 | | 1.0 | | 5.0 | MHz |
| | | X1 input high/low level width (t _{xH} , t _{xL}) | | 85 | | 500 | ns |

- Notes**
1. Indicates only oscillation circuit characteristics. Refer to “AC Characteristics” for instruction execution time.
 2. Time required to stabilize oscillation after reset or STOP mode release.

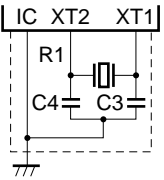
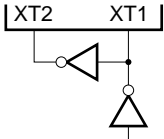
Cautions

1. When using the main system clock oscillator, wiring in the area enclosed with the broken line in the above figures should be carried out as follows to avoid an adverse effect from wiring capacitance.

- Wiring should be as short as possible.
- Wiring should not cross other signal lines.
- Wiring should not be placed close to a varying high current.
- The potential of the oscillator capacitor ground should be the same as V_{SS}.
- Do not ground wiring to a ground pattern in which a high current flows.
- Do not fetch a signal from the oscillator.

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

Subsystem Clock Oscillation Circuit Characteristics (T_A = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

| Resonator | Recommended Circuit | Parameter | Test Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------|---|--|--------------------------------|------|--------|------|------|
| Crystal resonator |  | Oscillator frequency (f _{XT}) Note 1 | | 32 | 32.768 | 35 | kHz |
| | | Oscillation stabilization time Note 2 | V _{DD} = 4.5 to 6.0 V | | 1.2 | 2 | s |
| External clock |  | XT1 input frequency (f _{XT}) Note 1 | | 32 | | 100 | kHz |
| | | XT1 input high-/low-level width (t _{XTH} , t _{XTL}) | | 5 | | 15 | μs |

- Notes**
1. Indicates only oscillation circuit characteristics. Refer to “AC Characteristics” for instruction execution time.
 2. Time required to stabilize oscillation after V_{DD} reaches oscillator voltage MIN.

Cautions

1. When using the subsystem clock oscillator, wiring in the area enclosed with the broken line in the above figures should be carried out as follows to avoid an adverse effect from wiring capacitance.

- Wiring should be as short as possible.
- Wiring should not cross other signal lines.
- Wiring should not be placed close to a varying high current.
- The potential of the oscillator capacitor ground should be the same as V_{SS}.
- Do not ground wiring to a ground pattern in which a high current flows.
- Do not fetch a signal from the oscillator.

2. The subsystem clock oscillator is a low-amplitude circuit in order to achieve a low consumption current, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit |
|-------------------|-----------------|---|--|------|------|------|------|
| Input capacitance | C _{IN} | f = 1 MHz Measured pins returned to 0 V. | | | | 15 | pF |
| I/O capacitance | C _{IO} | f = 1 MHz Measured pins returned to 0 V. | P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131 | | | 15 | pF |
| | | | P60 to P63 | | | 20 | pF |

Remark The characteristics of the alternate-function pins are the same as those of the port pins unless otherwise specified.

DC Characteristics (T_A = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit |
|-----------------------------|-------------------|---|--|----------------------|---------------------|---------------------|------|
| Input voltage, high | V _{IH1} | P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131 | | 0.7 V _{DD} | | V _{DD} | V |
| | V _{IH2} | P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, $\overline{\text{RESET}}$ | | 0.8 V _{DD} | | V _{DD} | V |
| | V _{IH3} | P60 to P63 (N-ch Open-drain) | | 0.7 V _{DD} | | 15 | V |
| | V _{IH4} | X1, X2 | | V _{DD} -0.5 | | V _{DD} | V |
| | V _{IH5} | XT1/P07, XT2 | V _{DD} = 4.5 to 6.0 V | 0.8 V _{DD} | | V _{DD} | V |
| 0.9 V _{DD} | | | | | V _{DD} | V | |
| Input voltage, low | V _{IL1} | P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67, P71, P120 to P127, P130, P131 | | 0 | | 0.3 V _{DD} | V |
| | V _{IL2} | P00 to P06, P20, P22, P24 to P27, P33, P34, P70, P72, $\overline{\text{RESET}}$ | | 0 | | 0.2 V _{DD} | V |
| | V _{IL3} | P60 to P63 | V _{DD} = 4.5 to 6.0 V | 0 | | 0.3 V _{DD} | V |
| | | | | 0 | | 0.2 V _{DD} | V |
| | V _{IL4} | X1, X2 | | 0 | | 0.4 | V |
| V _{IL5} | XT1/P07, XT2 | V _{DD} = 4.5 to 6.0 V | 0 | | 0.2 V _{DD} | V | |
| | | | 0 | | 0.1 V _{DD} | V | |
| Output voltage, high | V _{OH} | V _{DD} = 4.5 to 6.0 V, I _{OH} = -1mA | | V _{DD} -1.0 | | | V |
| | | I _{OH} = -100 μA | | V _{DD} -0.5 | | | V |
| Output voltage, low | V _{OL1} | P50 to P57, P60 to P63 | V _{DD} = 4.5 to 6.0 V, I _{OL} = 15 mA | | 0.4 | 2.0 | V |
| | | P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P70 to P72, P120 to P127, P130, P131 | V _{DD} = 4.5 to 6.0 V, I _{OL} = 1.6 mA | | | 0.4 | V |
| | V _{OL2} | SB0, SB1, $\overline{\text{SCK0}}$ | V _{DD} = 4.5 to 6.0 V, N-ch open-drain at pull-up time(R = 1 kΩ) | | | 0.2 V _{DD} | V |
| | V _{OL3} | I _{OL} = 400 μA | | | | 0.5 | V |
| Input leakage current, high | I _{LIH1} | V _{IN} = V _{DD} | P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P72, P120 to P127, P130, P131 $\overline{\text{RESET}}$ | | | 3 | μA |
| | I _{LIH2} | | | X1, X2, XT1/P07, XT2 | | | 20 |
| | I _{LIH3} | V _{IN} = 15 V | P60 to P63 | | | 80 | μA |

Remark The characteristics of alternate-function pins and a port pin are the same unless specified otherwise.

DC Characteristics (T_A = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit |
|------------------------------|-------------------|---|---|------|------|--------------------|------|
| Input leakage current, low | I _{LIL1} | V _{IN} = 0 V | P00 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131, RESET | | | -3 | μA |
| | I _{LIL2} | | X1, X2, XT1/P07, XT2 | | | -20 | μA |
| | I _{LIL3} | | P60 to P63 | | | -3 ^{Note} | μA |
| Output leakage current, high | I _{LOH} | V _{OUT} = V _{DD} | | | | 3 | μA |
| Output leakage current, low | I _{LOL} | V _{OUT} = 0 V | | | | -3 | μA |
| Mask option pull-up resistor | R ₁ | V _{IN} = 0 V, P60 to P63 | | 20 | 40 | 90 | kΩ |
| Software pull-up resistor | R ₂ | V _{IN} = 0 V, P01 to P06, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P72, P120 to P127, P130, P131 | V _{DD} = 4.5 V to 6.0 V | 15 | 40 | 90 | kΩ |
| | | | | 20 | | 500 | kΩ |

Note When the pull-up resistor is not included in P60 to P63 (specified by a mask option), a -200 μA (MAX.) low-level input leakage current flows only at the 1.5 clock interval (no wait) when the read instruction to port 6 (PM6) and port mode register (PM6) is executed. At times other than this 1.5 interval, a -3 μA (MAX.) current flows.

Remark The characteristics of alternate-function pins and port pins are the same unless specified otherwise.

DC Characteristics (T_A = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit | |
|------------------------------------|---|--|---|------|------|------|----|
| Power supply current Note 1 | I _{DD1} | 5.0-MHz crystal oscillation operating mode (f _{xx} = 2.5 MHz) Note 2 | V _{DD} = 5.0 V ± 10% Note 5 | | 4 | 12 | mA |
| | | | V _{DD} = 3.0 V ± 10% Note 6 | | 0.6 | 1.8 | mA |
| | | 5.0-MHz crystal oscillation operating mode (f _{xx} = 5.0 MHz) Note 3 | V _{DD} = 5.0 V ± 10% Note 5 | | 6.5 | 19.5 | mA |
| | | | V _{DD} = 3.0 V ± 10% Note 6 | | 0.8 | 2.4 | mA |
| | I _{DD2} | 5.0-MHz crystal oscillation HALT mode (f _{xx} = 2.5 MHz) Note 2 | V _{DD} = 5.0 V ± 10% | | 1.4 | 4.2 | mA |
| | | | V _{DD} = 3.0 V ± 10% | | 0.5 | 1.5 | mA |
| | | 5.0-MHz crystal oscillation HALT mode (f _{xx} = 5.0 MHz) Note 3 | V _{DD} = 5.0 V ± 10% | | 1.6 | 4.8 | mA |
| | | | V _{DD} = 3.0 V ± 10% | | 0.65 | 1.95 | mA |
| | I _{DD3} | 32.768-kHz crystal oscillation operating mode Note 4 | V _{DD} = 5.0 V ± 10% | | 60 | 120 | μA |
| | | | V _{DD} = 3.0 V ± 10% | | 32 | 64 | μA |
| | I _{DD4} | 32.768-kHz crystal oscillation HALT mode Note 4 | V _{DD} = 5.0 V ± 10% | | 25 | 55 | μA |
| | | | V _{DD} = 3.0 V ± 10% | | 5 | 15 | μA |
| I _{DD5} | XT1 = V _{DD} STOP mode When feedback resistor is used | V _{DD} = 5.0 V ± 10% | | 1 | 30 | μA | |
| | | V _{DD} = 3.0 V ± 10% | | 0.5 | 10 | μA | |
| I _{DD6} | XT1 = V _{DD} STOP mode When feedback resistor is not used | V _{DD} = 5.0 V ± 10% | | 0.1 | 30 | μA | |
| | | V _{DD} = 3.0 V ± 10% | | 0.05 | 10 | μA | |

- Notes**
1. Flows through the V_{DD} and AV_{DD} pins. Does not include the current which flows through the A/D converter, D/A converter, and on-chip pull-up resistor.
 2. f_{xx} = f_x/2 operation (when oscillation mode selection register (OSMS) is set to 00H)
 3. f_{xx} = f_x operation (when the OSMS is set to 01H)
 4. When the main system clock is stopped
 5. High-speed mode operation (when a processor clock control register (PCC) is set to 00H)
 6. Low-speed mode operation (when the PCC is set to 04H)

- Remarks**
1. f_{xx}: Main system clock frequency (f_x or f_x/2)
 2. f_x: Main system clock oscillator frequency

AC CHARACTERISTICS

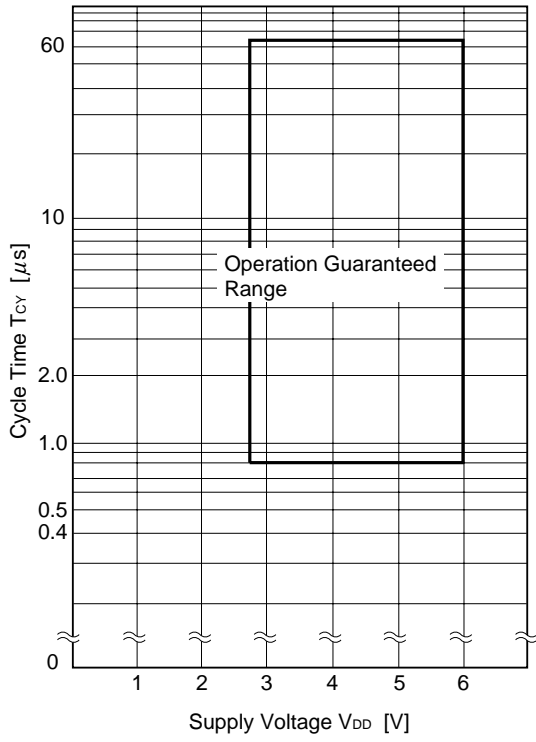
(1) Basic Operation (T_A = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit | |
|--|---|-----------------------------------|---|--------------------------------------|------|------|----|
| Cycle time (Min. instruction execution time) | T _{CY} | Operating on main system clock | f _{XX} = f _X /2 Note 1 | 0.8 | | 64 | μs |
| | | | f _{XX} = f _X Note 2 | V _{DD} = 4.5 to 6.0 V | 0.4 | | 32 |
| | | | | 0.8 | | 32 | μs |
| | | Operating on subsystem clock | | 40 | 122 | 125 | μs |
| T100 input high-/ low-level width | t _{TIH00} , t _{TIL00} | V _{DD} = 4.5 to 6.0 V | | 2f _{sam} +0.1 Note 3 | | μs | |
| | | | | 2f _{sam} +0.2 Note 3 | | μs | |
| T101 input high-/ low-level width | t _{TIH01} , t _{TIL01} | | 10 | | | μs | |
| T11, T12 input frequency | f _{TI1} | V _{DD} = 4.5 to 6.0 V | 0 | | 4 | MHz | |
| | | | 0 | | 275 | kHz | |
| T11, T12 input high-/low-level width | t _{TIH1} , t _{TIL1} | V _{DD} = 4.5 to 6.0 V | | 100 | | ns | |
| | | | | 1.8 | | μs | |
| Interrupt request input high-/low -level width | t _{INTH} , t _{INTL} | INTP0 | V _{DD} = 4.5 to 6.0 V | 2f _{sam} +0.1 Note 3 | | μs | |
| | | | | 2f _{sam} +0.2 Note 3 | | μs | |
| | | INTP1 to INTP6, KR0 to KR7 | | 10 | | μs | |
| RESET low-level width | t _{RSL} | | 10 | | | μs | |

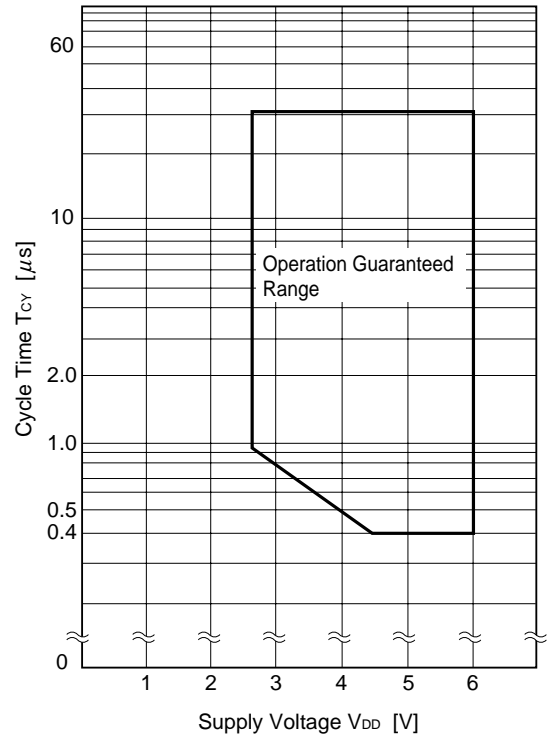
- Notes**
1. When oscillation mode selection register is set to 00H
 2. When oscillation mode selection register is set to 01H
 3. In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register (SCS), selection of f_{sam} is possible between f_{XX}/2^N, f_{XX}/32, f_{XX}/64 and f_{XX}/128 (when N= 0 to 4).

- Remarks**
1. f_{XX}: Main system clock frequency (f_X or f_X/2)
 2. f_X: Main system clock oscillation frequency

T_{CY} vs V_{DD} (at f_{XX} = f_X/2 main system clock operation)



T_{CY} vs V_{DD} (at f_{XX} = f_X main system clock operation)



(2) Read/Write Operation

(a) When MCS = 1, PCC2 to PCC0 = 000B (T_A = -40 to + 85°C, V_{DD} = 4.5 to 6.0 V)

| Parameter | Symbol | Test Conditions | MIN. | MAX. | Unit |
|---|--------------------|-----------------|-------------------------------|-------------------------------|------|
| ASTB high-level width | t _{ASTH} | | 0.85t _{cy} - 50 | | ns |
| Address setup time | t _{ADS} | | 0.85t _{cy} - 50 | | ns |
| Address hold time | t _{ADH} | | 50 | | ns |
| Data input time from address | t _{ADD1} | | | (2.85+2n)t _{cy} -80 | ns |
| | t _{ADD2} | | | (4+2n)t _{cy} -100 | ns |
| Data input time from $\overline{RD}\downarrow$ | t _{RDD1} | | | (2+2n)t _{cy} -100 | ns |
| | t _{RDD2} | | | (2.85+2n)t _{cy} -100 | ns |
| Read data hold time | t _{RDH} | | 0 | | ns |
| \overline{RD} low-level width | t _{RDL1} | | (2+2n)t _{cy} -60 | | ns |
| | t _{RDL2} | | (2.85+2n)t _{cy} -60 | | ns |
| $\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$ | t _{RDWT1} | | | 0.85t _{cy} -50 | ns |
| | t _{RDWT2} | | | 2t _{cy} -60 | ns |
| $\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$ | t _{WRWT} | | | 2t _{cy} -60 | ns |
| \overline{WAIT} low-level width | t _{WTL} | | (1.15+2n)t _{cy} | (2+2n)t _{cy} | ns |
| Write data setup time | t _{WDS} | | (2.85+2n)t _{cy} -100 | | ns |
| Write data hold time | t _{WDH} | | 20 | | ns |
| \overline{WR} low-level width | t _{WRL} | | (2.85+2n)t _{cy} -60 | | ns |
| $\overline{RD}\downarrow$ delay time from ASTB \downarrow | t _{ASTRD} | | 25 | | ns |
| $\overline{WR}\downarrow$ delay time from ASTB \downarrow | t _{ASTWR} | | 0.85t _{cy} + 20 | | ns |
| ASTB \uparrow delay time from $\overline{RD}\uparrow$ in external fetch | t _{RDAST} | | 0.85t _{cy} - 10 | 1.15t _{cy} + 20 | ns |
| Address hold time from $\overline{RD}\uparrow$ in external fetch | t _{RDADH} | | 0.85t _{cy} - 50 | 1.15t _{cy} + 50 | ns |
| Write data output time from $\overline{RD}\uparrow$ | t _{RDWD} | | 40 | | ns |
| Write data output time from $\overline{WR}\downarrow$ | t _{RDWD} | | 0 | 50 | ns |
| Address hold time from $\overline{WR}\uparrow$ | t _{WRADH} | | 0.85t _{cy} | 1.15t _{cy} + 40 | ns |
| $\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$ | t _{WTRD} | | 1.15t _{cy} + 40 | 3.15t _{cy} + 40 | ns |
| $\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$ | t _{WTWR} | | 1.15t _{cy} + 30 | 3.15t _{cy} + 30 | ns |

- Remarks**
1. MCS: Oscillation mode selection register (OSMS) bit 0
 2. PCC2 to PCC0: Processor clock control register (PCC) bit 2 to bit 0
 3. t_{cy} = T_{cy}/4
 4. n indicates the number of waits.

(b) Except when MCS = 1, PCC2 to PCC0 = 000B (T_A = -40 to + 85°C, V_{DD} = 2.7 to 6.0 V)

| Parameter | Symbol | Test Conditions | MIN. | MAX. | Unit |
|---|--------------------|-----------------|-----------------------------|-----------------------------|------|
| ASTB high-level width | t _{ASTH} | | t _{cy} - 80 | | ns |
| Address setup time | t _{ADS} | | t _{cy} - 80 | | ns |
| Address hold time | t _{ADH} | | 0.4t _{cy} - 10 | | ns |
| Data input time from address | t _{ADD1} | | | (3+2n)t _{cy} -160 | ns |
| | t _{ADD2} | | | (4+2n)t _{cy} -200 | ns |
| Data input time from $\overline{RD}\downarrow$ | t _{RDD1} | | | (1.4+2n)t _{cy} -70 | ns |
| | t _{RDD2} | | | (2.4+2n)t _{cy} -70 | ns |
| Read data hold time | t _{RDH} | | 0 | | ns |
| \overline{RD} low-level width | t _{RDL1} | | (1.4+2n)t _{cy} -20 | | ns |
| | t _{RDL2} | | (2.4+2n)t _{cy} -20 | | ns |
| $\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$ | t _{RDWT1} | | | t _{cy} -100 | ns |
| | t _{RDWT2} | | | 2t _{cy} -100 | ns |
| $\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$ | t _{WRWT} | | | 2t _{cy} -100 | ns |
| \overline{WAIT} low-level width | t _{WTL} | | (1+2n)t _{cy} | (2+2n)t _{cy} | ns |
| Write data setup time | t _{WDS} | | (2.4+2n)t _{cy} -60 | | ns |
| Write data hold time | t _{WDH} | | 20 | | ns |
| \overline{WR} low-level width | t _{WRL} | | (2.4+2n)t _{cy} -20 | | ns |
| $\overline{RD}\downarrow$ delay time from $\overline{ASTB}\downarrow$ | t _{ASTRD} | | 0.4t _{cy} -30 | | ns |
| $\overline{WR}\downarrow$ delay time from $\overline{ASTB}\downarrow$ | t _{ASTWR} | | 1.4t _{cy} -30 | | ns |
| ASTB \uparrow delay time from $\overline{RD}\uparrow$ in external fetch | t _{RDAST} | | t _{cy} -10 | t _{cy} + 20 | ns |
| Address hold time from $\overline{RD}\uparrow$ in external fetch | t _{RDADH} | | t _{cy} - 50 | t _{cy} + 50 | ns |
| Write data output time from $\overline{RD}\uparrow$ | t _{RDWD} | | 0.4t _{cy} - 20 | | ns |
| Write data output time from $\overline{WR}\downarrow$ | t _{WRWD} | | 0 | 60 | ns |
| Address hold time from $\overline{WR}\uparrow$ | t _{WRADH} | | t _{cy} | t _{cy} + 60 | ns |
| $\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$ | t _{WTRD} | | 0.6t _{cy} + 180 | 2.6t _{cy} + 180 | ns |
| $\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$ | t _{WTWR} | | 0.6t _{cy} + 120 | 2.6t _{cy} + 120 | ns |

- Remarks**
1. MCS: Oscillation mode selection register (OSMS) bit 0
 2. PCC2 to PCC0: Processor clock control register (PCC) bit 2 to bit 0
 3. t_{cy} = T_{cy}/4
 4. n indicates the number of waits.

(3) Serial Interface (T_A = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode ($\overline{\text{SCK0}}$... Internal clock output)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|-------------------------------------|--------------------------------|--------------------------|------|------|------|
| $\overline{\text{SCK0}}$ cycle time | t _{KCY1} | V _{DD} = 4.5 to 6.0 V | 800 | | | ns |
| | | | 1600 | | | ns |
| $\overline{\text{SCK0}}$ high-/low-level width | t _{KH1} , t _{KL1} | V _{DD} = 4.5 to 6.0 V | t _{KCY1} /2-50 | | | ns |
| | | | t _{KCY1} /2-100 | | | ns |
| SI0 setup time (to $\overline{\text{SCK0}}$ ↑) | t _{SIK1} | V _{DD} = 4.5 to 6.0 V | 100 | | | ns |
| | | | 150 | | | ns |
| SI0 hold time (to $\overline{\text{SCK0}}$ ↑) | t _{KSI1} | | 400 | | | ns |
| SO0 output delay time from $\overline{\text{SCK0}}$ ↓ | t _{KSO1} | C = 100 pF Note | | | 300 | ns |

Note C is the load capacitance of the $\overline{\text{SCK0}}$ and SO0 output lines.

(ii) 3-wire serial I/O mode ($\overline{\text{SCK0}}$... External clock input)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|--------------------------------------|---|------|------|------|------|
| $\overline{\text{SCK0}}$ cycle time | t _{KCY2} | V _{DD} = 4.5 to 6.0 V | 800 | | | ns |
| | | | 1600 | | | ns |
| $\overline{\text{SCK0}}$ high-/low-level width | t _{KH2} , t _{KL2} | V _{DD} = 4.5 to 6.0 V | 400 | | | ns |
| | | | 800 | | | ns |
| SI0 setup time (to $\overline{\text{SCK0}}$ ↑) | t _{SIK2} | | 100 | | | ns |
| SI0 hold time (to $\overline{\text{SCK0}}$ ↑) | t _{KSI2} | | 400 | | | ns |
| SO0 output delay time from $\overline{\text{SCK0}}$ ↓ | t _{KSO2} | C = 100 pF Note | | | 300 | ns |
| $\overline{\text{SCK0}}$ rise, fall time | t _{R2} , t _{F2} | When using external device expansion function | | | 160 | ns |
| | | When not using external device expansion function | | | 1000 | ns |

Note C is the load capacitance of the SO0 output line.

(iii) 2-wire serial I/O mode ($\overline{\text{SCK0}}$... Internal clock output)

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit | |
|---|-------------------|-------------------------------------|---|-------------------------|------|------|------|----|
| $\overline{\text{SCK0}}$ cycle time | t_{KCY3} | R = 1 kΩ, C = 100 pF Note | | 1600 | | | ns | |
| $\overline{\text{SCK0}}$ high-level width | t_{KH3} | | | $t_{\text{KCY3}}/2-160$ | | | ns | |
| $\overline{\text{SCK0}}$ low-level width | t_{KL3} | | $V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$ | $t_{\text{KCY3}}/2-50$ | | | ns | |
| | | | | $t_{\text{KCY3}}/2-100$ | | | ns | |
| SB0, SB1 setup time (to $\overline{\text{SCK0}}\uparrow$) | t_{SIK3} | | $V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$ | | 300 | | | ns |
| | | | | | 350 | | | ns |
| SB0, SB1 hold time (to $\overline{\text{SCK0}}\uparrow$) | t_{KS13} | | | | 600 | | | ns |
| SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$ | t_{KSO3} | | | 0 | | 300 | ns | |

Note R and C are the load resistance and load capacitance of the $\overline{\text{SCK0}}$, SB0, and SB1 output lines.

(iv) 2-wire serial I/O mode ($\overline{\text{SCK0}}$... External clock input)

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit |
|---|-------------------------------------|--|---|---------------------|------|------|------|
| $\overline{\text{SCK0}}$ cycle time | t_{KCY4} | | | 1600 | | | ns |
| $\overline{\text{SCK0}}$ high-level width | t_{KH4} | | | 650 | | | ns |
| $\overline{\text{SCK0}}$ low-level width | t_{KL4} | | | 800 | | | ns |
| SB0, SB1 setup time (to $\overline{\text{SCK0}}\uparrow$) | t_{SIK4} | | | 100 | | | ns |
| SB0, SB1 hold time (to $\overline{\text{SCK0}}\uparrow$) | t_{KS14} | | | $t_{\text{KCY4}}/2$ | | | ns |
| SB0, SB1 output delay time from $\overline{\text{SCK0}}\downarrow$ | t_{KSO4} | R = 1 kΩ, C = 100 pF Note | $V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$ | 0 | | 300 | ns |
| | | | | 0 | | 500 | ns |
| $\overline{\text{SCK0}}$ rise, fall time | $t_{\text{R4}},$ t_{F4} | When using external device expansion function | | | | 160 | ns |
| | | When not using external device expansion function | | | | 1000 | ns |

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output lines.

(v) I²C bus mode (SCL... Internal clock output)

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit |
|--|-------------------|---|--------------------------------|------------------------|------|------|------|
| SCL cycle time | t _{KCY5} | R = 1 kΩ, C = 100 pF ^{Note} | V _{DD} = 2.7 to 6.0 V | 10 | | | μs |
| | | | | 20 | | | μs |
| SCL high-level width | t _{KH5} | | V _{DD} = 2.7 to 6.0 V | t _{KCY5} —160 | | | ns |
| | | | | t _{KCY5} —190 | | | ns |
| SCL low-level width | t _{KL5} | | V _{DD} = 4.5 to 6.0 V | t _{KCY5} —50 | | | ns |
| | | | | t _{KCY5} —100 | | | ns |
| SDA0, SDA1 setup time (to SCL↑) | t _{SIK5} | | V _{DD} = 2.7 to 6.0 V | 200 | | | ns |
| | | | | 300 | | | ns |
| SDA0, SDA1 hold time (to SCL↓) | t _{KSI5} | | | 0 | | | ns |
| SDA0, SDA1 output delay time from SCL↓ | t _{KSO5} | | V _{DD} = 4.5 to 6.0 V | 0 | | 300 | ns |
| | | 0 | | | 500 | ns | |
| SCL↑ → SDA0, SDA1↓ or SCL↑ → SDA0, SDA1↑ | t _{KSB} | | 200 | | | ns | |
| SDA0, SDA1↓ → SCL↓ | t _{SBK} | | 400 | | | ns | |
| SDA0, SDA1 high-level width | t _{SBH} | | 500 | | | ns | |

Note R and C are the load resistance and load capacitance of the SCL, SDA0, and SDA1 output lines.

(vi) I²C bus mode (SCL... External clock input)

| Parameter | Symbol | Test Conditions | | MIN. | TYP. | MAX. | Unit |
|--|--------------------|---|--------------------------------|------|------|------|------|
| SCL cycle time | t _{KCY6} | | | 1000 | | | ns |
| SCL high-/low-level width | t _{KH6} , | | | 400 | | | ns |
| | t _{KL6} | | | | | | |
| SDA0, SDA1 setup time (to SCL↑) | t _{SIK6} | | | 200 | | | ns |
| SDA0, SDA1 hold time (to SCL↓) | t _{KSI6} | | | 0 | | | ns |
| SDA0, SDA1 output delay time from SCL↓ | t _{KSO6} | R = 1 kΩ C = 100 pF ^{Note} | V _{DD} = 4.5 to 6.0 V | 0 | | 300 | ns |
| | | | | 0 | | 500 | ns |
| SCL↑ → SDA0, SDA1↓ or SCL↑ → SDA0, SDA1↑ | t _{KSB} | | | 200 | | | ns |
| SDA0, SDA1↓ → SCL↓ | t _{SBK} | | | 400 | | | ns |
| SDA0, SDA1 high-level width | t _{SBH} | | | 500 | | | ns |
| SCL rise, fall time | t _{RE6} , | When using external device expansion function | | | | 160 | ns |
| | t _{FE6} | When not using external device expansion function | | | | 1000 | ns |

Note R and C are the load resistance and load capacitance of the SDA0 and SDA1 output lines.

(b) Serial interface channel 1

(i) 3-wire serial I/O mode ($\overline{\text{SCK1}}$...Internal clock output)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|-------------------|---|-------------------------|------|------|------|
| $\overline{\text{SCK1}}$ cycle time | t_{KCY7} | $V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$ | 800 | | | ns |
| | | | 1600 | | | ns |
| $\overline{\text{SCK1}}$ high-/low-level width | t_{KH7} | $V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$ | $t_{\text{KCY7}}/2-50$ | | | ns |
| | t_{KL7} | | $t_{\text{KCY7}}/2-100$ | | | ns |
| SI1 setup time (to $\overline{\text{SCK1}}\uparrow$) | t_{SIK7} | $V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$ | 100 | | | ns |
| | | | 150 | | | ns |
| SI1 hold time (to $\overline{\text{SCK1}}\uparrow$) | t_{KSI7} | | 400 | | | ns |
| SO1 output delay time from $\overline{\text{SCK1}}\downarrow$ | t_{KSO7} | $C = 100 \text{ pF}$ Note | | | 300 | ns |

Note C is the load capacitance of the $\overline{\text{SCK1}}$ and SO1 output lines.

(ii) 3-wire serial I/O mode ($\overline{\text{SCK1}}$...External clock input)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|-------------------------------------|---|------|------|------|------|
| $\overline{\text{SCK1}}$ cycle time | t_{KCY8} | $V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$ | 800 | | | ns |
| | | | 1600 | | | ns |
| $\overline{\text{SCK1}}$ high-/low-level width | t_{KH8} | $V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$ | 400 | | | ns |
| | t_{KL8} | | 800 | | | ns |
| SI1 setup time (to $\overline{\text{SCK1}}\uparrow$) | t_{SIK8} | | 100 | | | ns |
| SI1 hold time (to $\overline{\text{SCK1}}\uparrow$) | t_{KSI8} | | 400 | | | ns |
| SO1 output delay time from $\overline{\text{SCK1}}\downarrow$ | t_{KSO8} | $C = 100 \text{ pF}$ Note | | | 300 | ns |
| $\overline{\text{SCK1}}$ rise, fall time | $t_{\text{R8}},$ t_{F8} | When using external device expansion function | | | 160 | ns |
| | | When not using external device expansion function | | | 1000 | ns |

Note C is the load capacitance of the SO1 output line.

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{\text{SCK1}}$... Internal clock output)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|-------------------|---|-------------------------|------|-------------------------|------|
| $\overline{\text{SCK1}}$ cycle time | t_{KCY9} | $V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$ | 800 | | | ns |
| | | | 1600 | | | ns |
| $\overline{\text{SCK1}}$ high-/low-level width | t_{KH9} | $V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$ | $t_{\text{KCY9}}/2-50$ | | | ns |
| | t_{KL9} | | $t_{\text{KCY9}}/2-100$ | | | ns |
| SI1 setup time (to $\overline{\text{SCK1}}\uparrow$) | t_{SIK9} | $V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$ | 100 | | | ns |
| | | | 150 | | | ns |
| SI1 hold time (to $\overline{\text{SCK1}}\uparrow$) | t_{KSI9} | | 400 | | | ns |
| SO1 output delay time from $\overline{\text{SCK1}}\downarrow$ | t_{KSO9} | $C = 100 \text{ pF}$ Note | | | 300 | ns |
| STB \uparrow from $\overline{\text{SCK1}}\uparrow$ | t_{SBD} | | $t_{\text{KCY9}}/2-100$ | | $t_{\text{KCY9}}/2+100$ | ns |
| Strobe signal high-level width | t_{SBW} | | $t_{\text{KCY9}}-30$ | | $t_{\text{KCY9}}+30$ | ns |
| Busy signal setup time (to busy signal detection timing) | t_{BYS} | | 100 | | | ns |
| Busy signal hold time (to busy signal detection timing) | t_{BYH} | $V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$ | 100 | | | ns |
| | | | 150 | | | ns |
| $\overline{\text{SCK1}}\downarrow$ from busy inactive | t_{SPS} | | | | $2t_{\text{KCY9}}$ | ns |

Note C is the load capacitance of the $\overline{\text{SCK1}}$ and SO1 output lines.

(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{\text{SCK1}}$... External clock input)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---|--|---|------|------|------|------|
| $\overline{\text{SCK1}}$ cycle time | t_{KCY10} | $V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$ | 800 | | | ns |
| | | | 1600 | | | ns |
| $\overline{\text{SCK1}}$ high-/low-level width | t_{KH10} | $V_{\text{DD}} = 4.5 \text{ to } 6.0 \text{ V}$ | 400 | | | ns |
| | t_{KL10} | | 800 | | | ns |
| SI1 setup time (to $\overline{\text{SCK1}}\uparrow$) | t_{SIK10} | | 100 | | | ns |
| SI1 hold time (from $\overline{\text{SCK1}}\uparrow$) | t_{KSI10} | | 400 | | | ns |
| SO1 output delay time from $\overline{\text{SCK1}}\downarrow$ | t_{KSO10} | $C = 100 \text{ pF}$ Note | | | 300 | ns |
| $\overline{\text{SCK1}}$ rise, fall time | t_{R10} , t_{F10} | When using external device expansion function | | | 160 | ns |
| | | When not using external device expansion function | | | 1000 | ns |

Note C is the load capacitance of the SO1 output line.

(c) Serial interface channel 2

(i) 3-wire serial I/O mode (SCK2...Internal clock output)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|----------------------------------|--|--------------------------------|---------------------------|------|------|------|
| SCK2 cycle time | t _{KCY11} | V _{DD} = 4.5 to 6.0 V | 800 | | | ns |
| | | | 1600 | | | ns |
| SCK2 high-/low-level width | t _{KH11} , t _{KL11} | V _{DD} = 4.5 to 6.0 V | t _{KCY11} /2-50 | | | ns |
| | | | t _{KCY11} /2-100 | | | ns |
| SI2 setup time (to SCK2↑) | t _{SIK11} | V _{DD} = 4.5 to 6.0 V | 100 | | | ns |
| | | | 150 | | | ns |
| SI2 hold time (to SCK2↑) | t _{KSI11} | | 400 | | | ns |
| SO2 output delay time from SCK2↓ | t _{KSO11} | C = 100 pF Note | | | 300 | ns |

Note C is the load capacitance of the SCK2 and SO2 output lines.

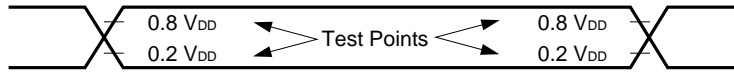
(ii) UART mode (Dedicated baud rate generator output)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|---------------|--------|--------------------------------|------|------|-------|------|
| Transfer rate | | V _{DD} = 4.5 to 6.0 V | | | 78125 | bps |
| | | | | | 39063 | bps |

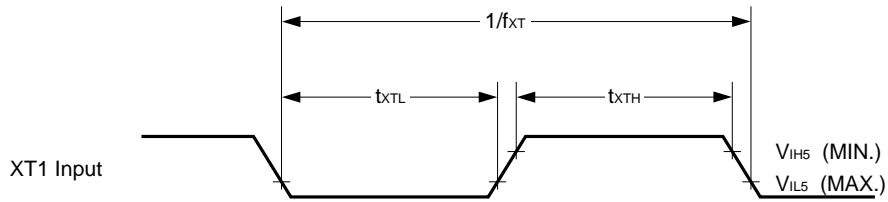
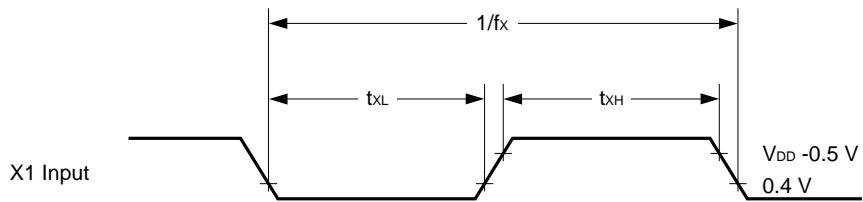
(iii) UART mode (External clock input)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|----------------------------|--|--|------|------|-------|------|
| ASCK cycle time | t _{KCY12} | V _{DD} = 4.5 to 6.0 V | 800 | | | ns |
| | | | 1600 | | | ns |
| ASCK high-/low-level width | t _{KH12} , t _{KL12} | V _{DD} = 4.5 to 6.0 V | 400 | | | ns |
| | | | 800 | | | ns |
| Transfer rate | | V _{DD} = 4.5 to 6.0 V | | | 39063 | bps |
| | | | | | 19531 | bps |
| ASCK rise, fall time | t _{R12} , t _{F12} | V _{DD} = 4.5 to 6.0 V, when not using external device expansion function. | | | 1000 | ns |
| | | | | | 160 | ns |

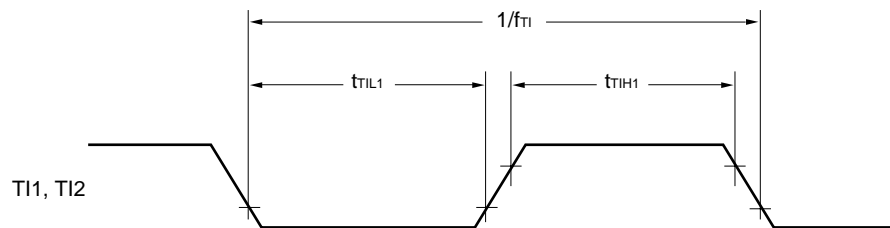
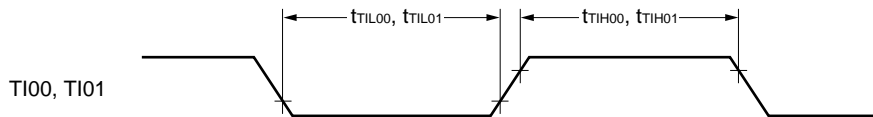
AC Timing Test Point (Excluding X1, XT1 Input)



Clock Timing

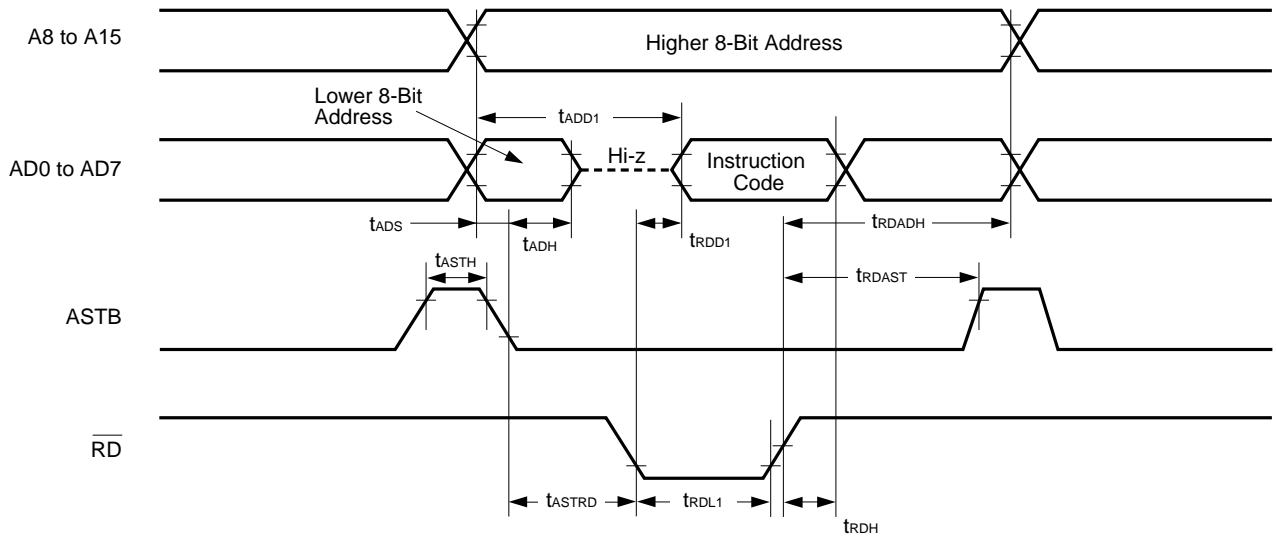


TI Timing

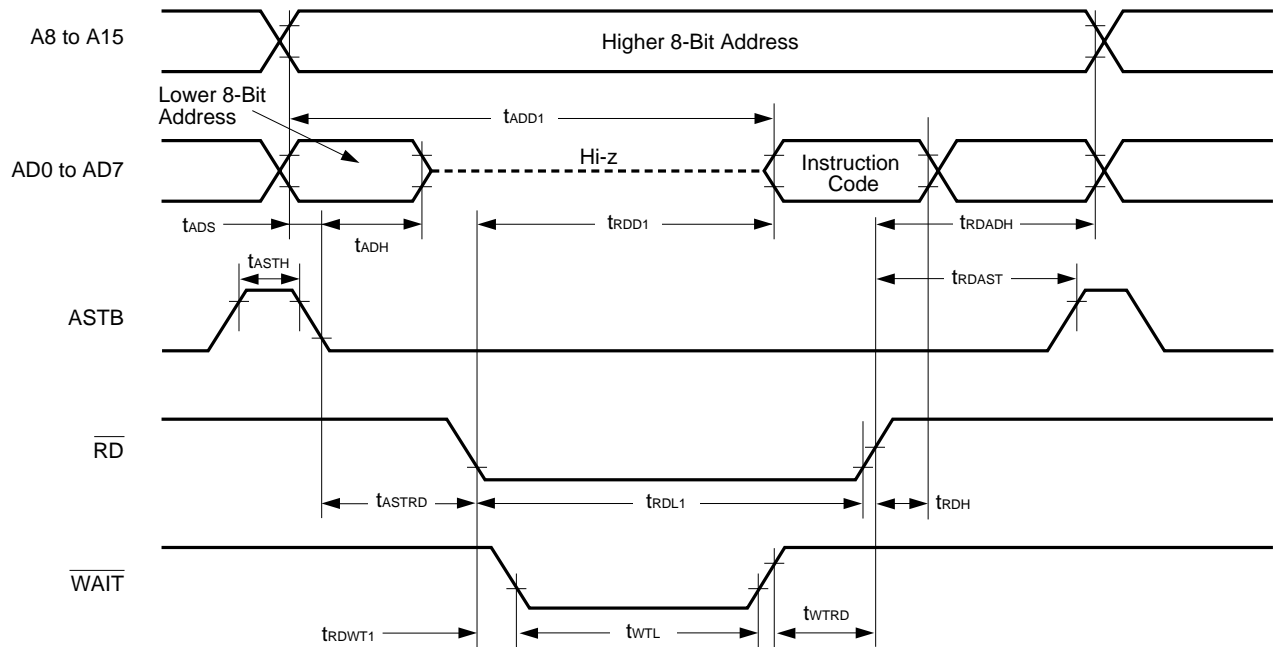


Read/Write Operation

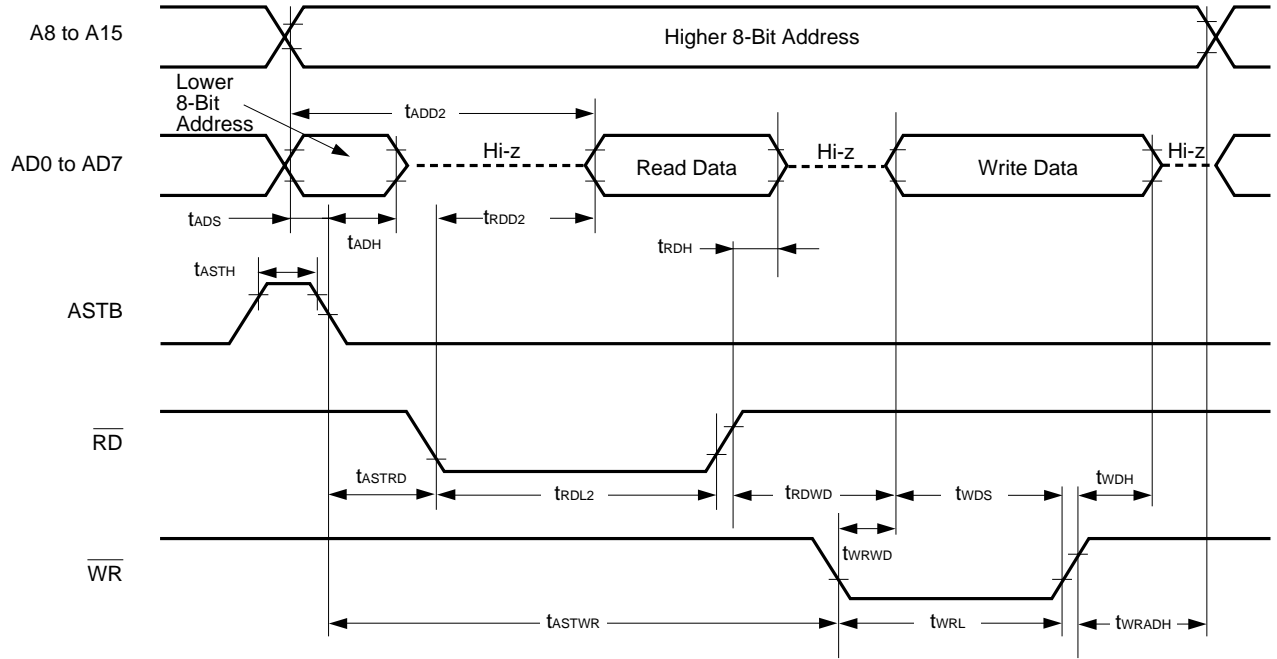
External Fetch (No Wait) :



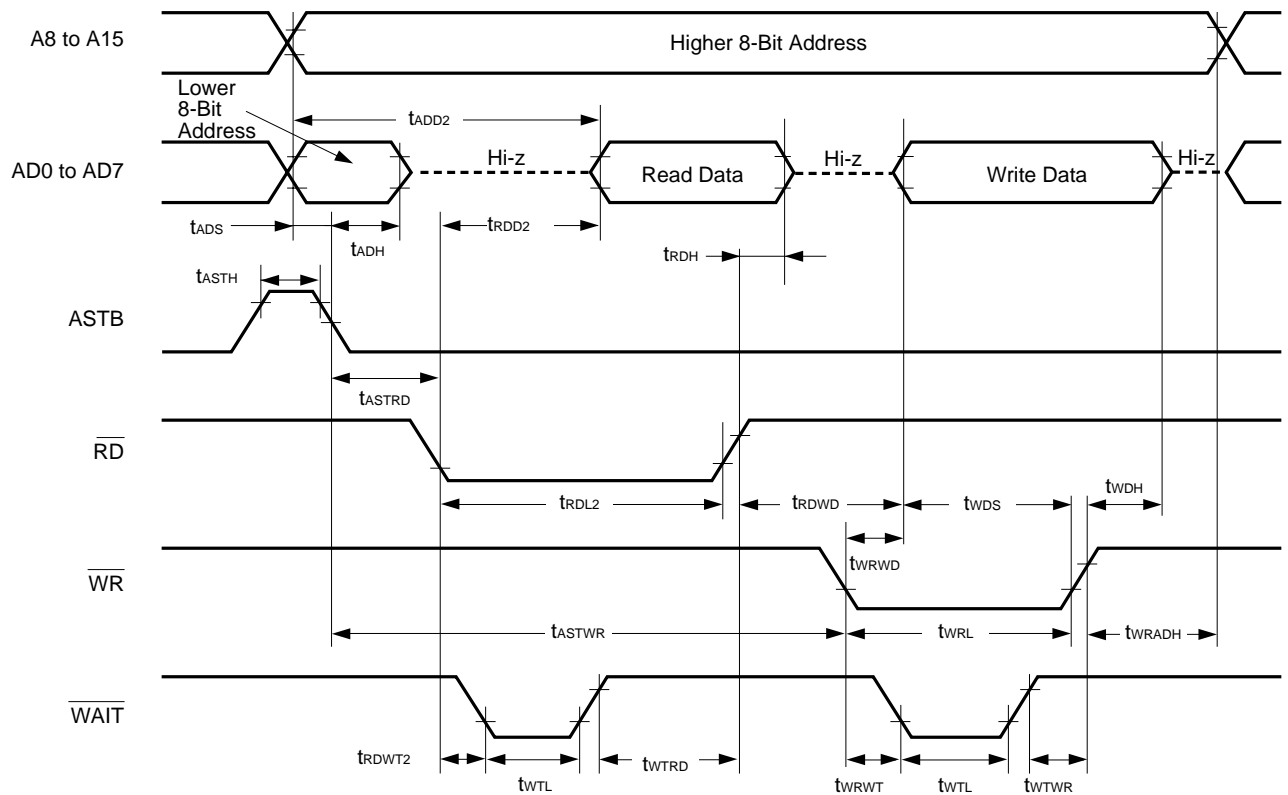
External Fetch (Wait Insertion) :



External Data Access (No Wait) :

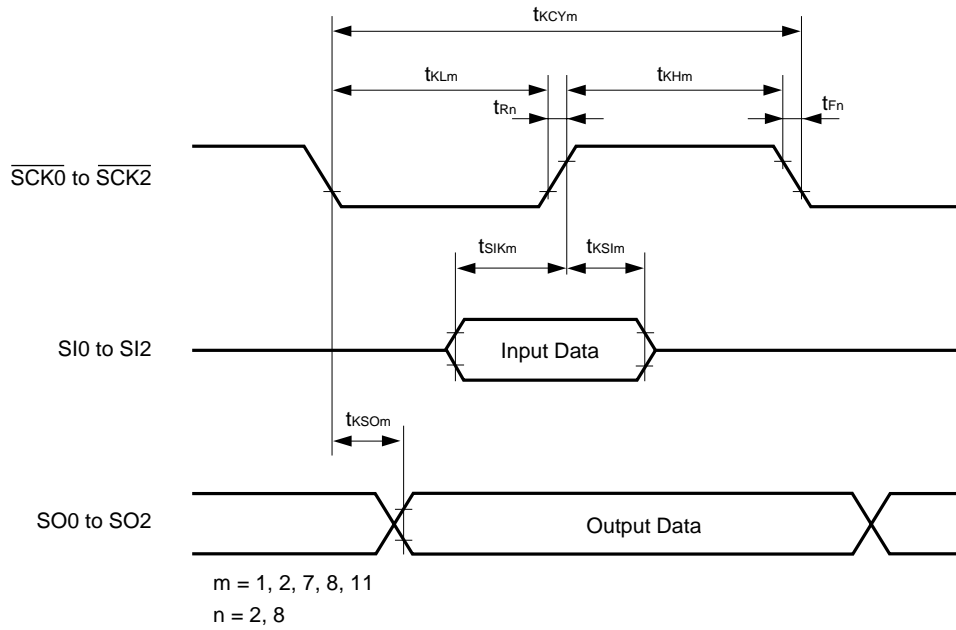


External Data Access (Wait Insertion) :

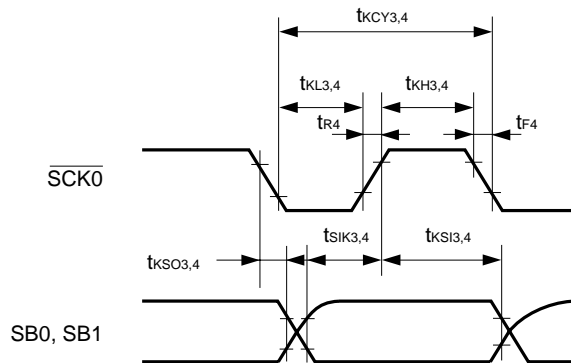


Serial Transfer Timing

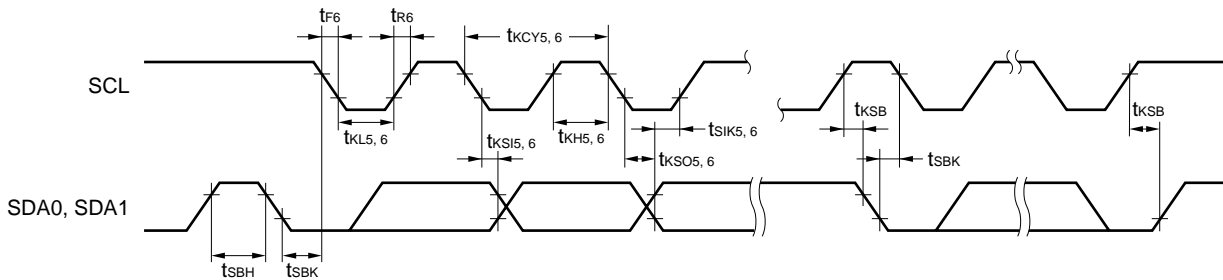
3-wire Serial I/O Mode :



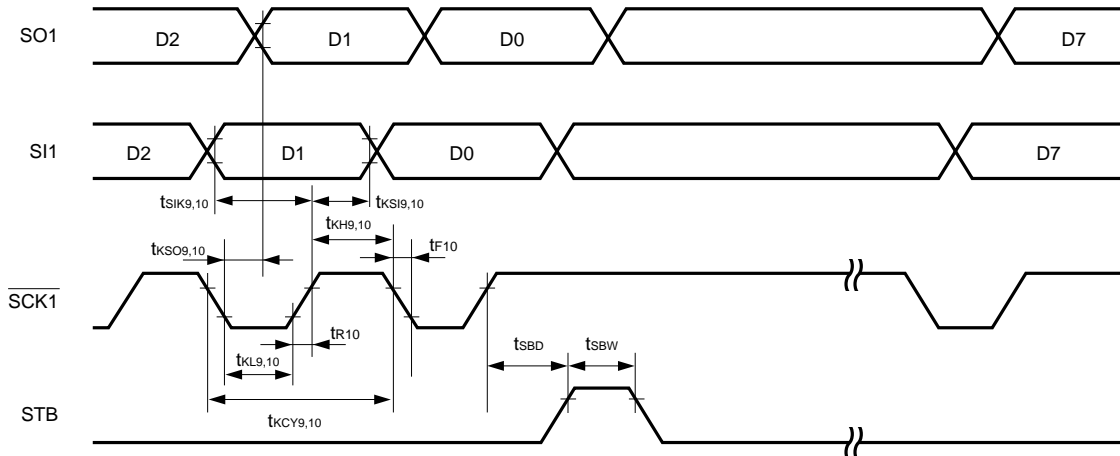
2-wire Serial I/O Mode :



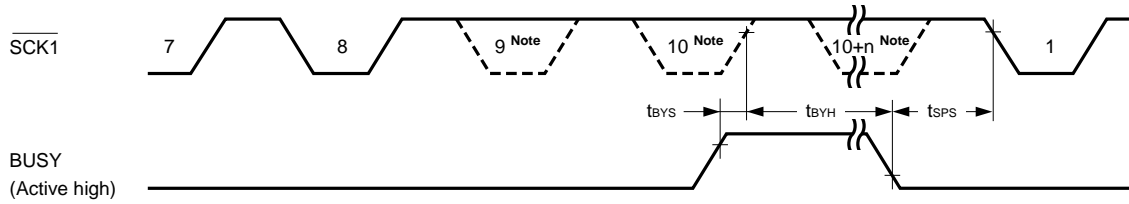
I²C Bus Mode



3-wire Serial I/O Mode with Automatic Transmit/Receive Function :

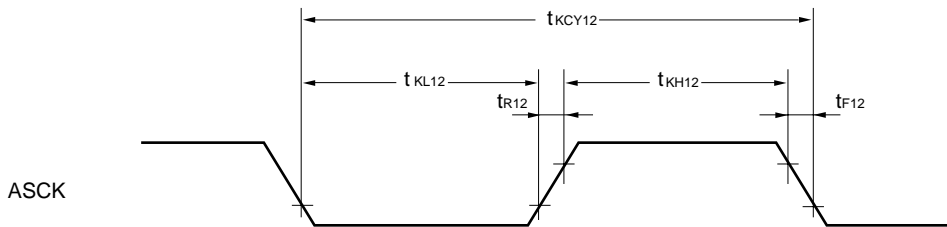


3-wire Serial I/O Mode with Automatic Transmit/Receive Function (Busy Processing) :



Note The signal is not actually driven low here; it is shown as such to indicate the timing.

UART Mode (External Clock Input) :



A/D CONVERTER CHARACTERISTICS (T_A = -40 to +85°C, AV_{DD} = V_{DD} = 2.7 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|--|---------------------|---|--------------------|------|--------------------|------|
| Resolution | | | 8 | 8 | 8 | bit |
| Overall error ^{Note} | | 2.7 V ≤ AV _{REF0} ≤ AV _{DD} | | | 0.6 | % |
| Conversion time | t _{CONV} | | 19.1 | | 200 | μs |
| Sampling time | t _{SAMP} | | 12/f _{xx} | | | μs |
| Analog input voltage | V _{IAN} | | AV _{SS} | | AV _{REF0} | V |
| Reference voltage | AV _{REF0} | | 2.7 | | AV _{DD} | V |
| Resistance between AV _{REF0} and AV _{SS} | R _{AIREF0} | | 4 | 14 | | kΩ |

Note Overall error excluding quantization error (±1/2 LSB). It is indicated as a ratio to the full-scale value.

Caution For pins which also function as port pins, do not perform the following operations during A/D conversion. If these operations are performed, the total error ratings cannot be kept (except for LCD segment output alternate-function pin).

- (1) Rewrite the output latch while the pin is used as a port pin.
- (2) Change the output level of the pin used as an output pin, even if it is not used as a port pin.

- Remarks**
1. f_{xx}: Main system clock frequency (f_x or f_x/2)
 2. f_x: Main system clock oscillation frequency

D/A CONVERTER CHARACTERISTICS (T_A = -40 to +85°C, V_{DD} = 2.7 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|--|---------------------|--------------------------------------|------------------------------------|------|-----------------|------|
| Resolution | | | | | 8 | bit |
| Overall error | | R = 2MΩ ^{Note 1} | | | 1.2 | % |
| | | R = 4MΩ ^{Note 1} | | | 0.8 | % |
| | | R = 10MΩ ^{Note 1} | | | 0.6 | % |
| Settling time | | ^{Note 1} C=30pF | 4.5 V ≤ AV _{REF1} ≤ 6.0 V | | 10 | μs |
| | | | 2.7 V ≤ AV _{REF1} < 4.5 V | | 15 | μs |
| Output resistance | R _O | Note 2 | | 10 | | kΩ |
| Analog reference voltage | AV _{REF1} | | 2.0 | | V _{DD} | V |
| Resistance between AV _{REF1} and AV _{SS} | R _{AIREF1} | DACS0, DACS1 = 55H ^{Note 2} | 4 | 8 | | kΩ |

- Notes**
1. R and C are the load resistance and load capacitance of the D/A converter output pins.
 2. Value for D/A converter 1 channel

Remark DACS0, DACS1: D/A conversion value setting register 0, 1

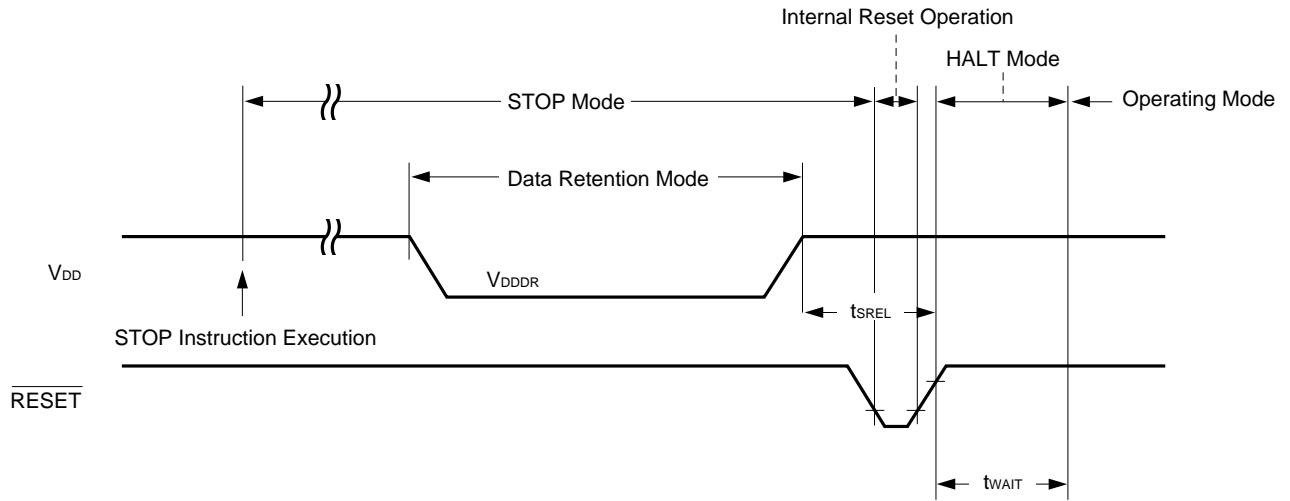
Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (TA = -40 to + 85°C)

| Parameter | Symbol | Test Conditions | MIN. | TYP. | MAX. | Unit |
|-------------------------------------|-------------------|---|------|---------------------------------|------|------|
| Data retention power supply voltage | V _{DDDR} | | 1.8 | | 6.0 | V |
| Data retention power supply current | I _{DDDR} | V _{DDDR} = 1.8 V Subsystem clock stop and feed-back resistor disconnected | | 0.1 | 10 | μA |
| Release signal set time | t _{SREL} | | 0 | | | μs |
| Oscillation stabilization wait time | t _{WAIT} | Release by $\overline{\text{RESET}}$ | | 2 ¹⁷ /f _x | | ms |
| | | Release by interrupt request | | Note | | ms |

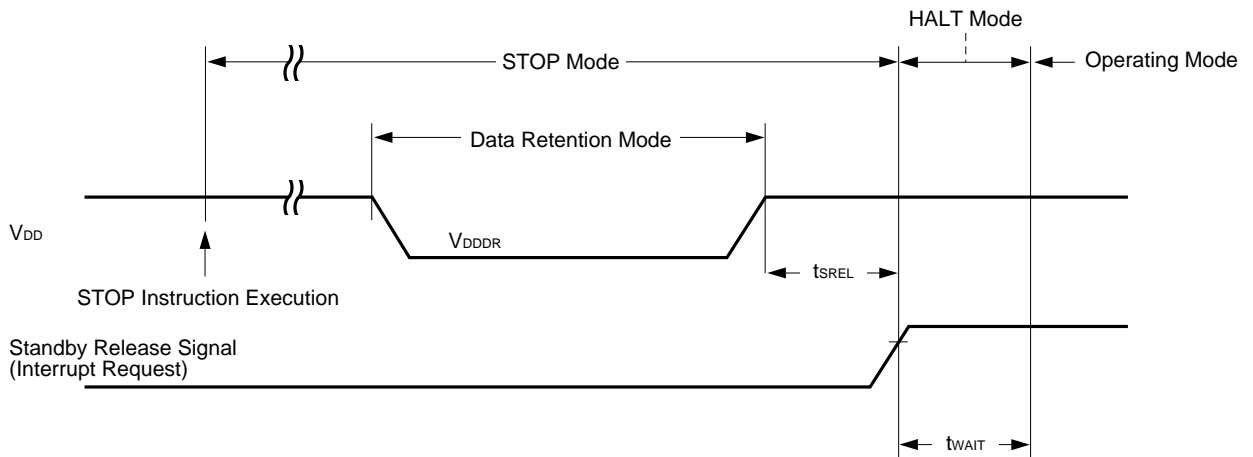
Note In combination with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register, selection of 2¹²/f_{xx} and 2¹⁴/f_{xx} to 2¹⁷/f_{xx} is possible.

Remark f_{xx}: Main system clock frequency (f_x or f_x/2)
f_x: Main system clock oscillation frequency

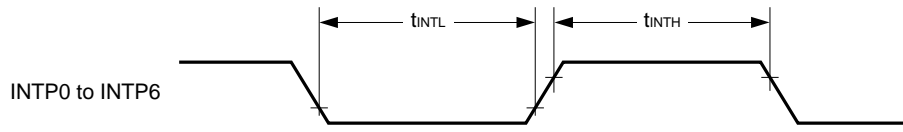
Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



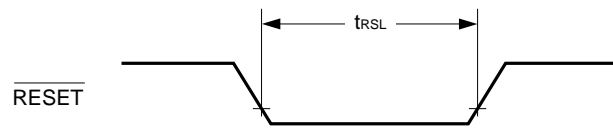
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)



Interrupt Request Input Timing



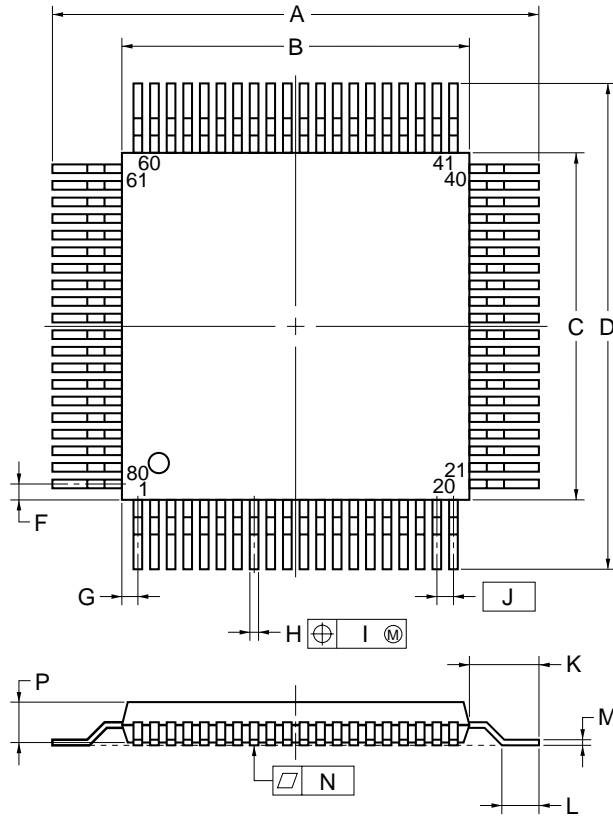
$\overline{\text{RESET}}$ Input Timing



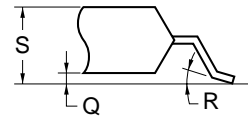
12. PACKAGE DRAWINGS

μPD78056FYGC-xxx-3B9, 78058FYGC-xxx-3B9

80 PIN PLASTIC QFP (14×14)



detail of lead end



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

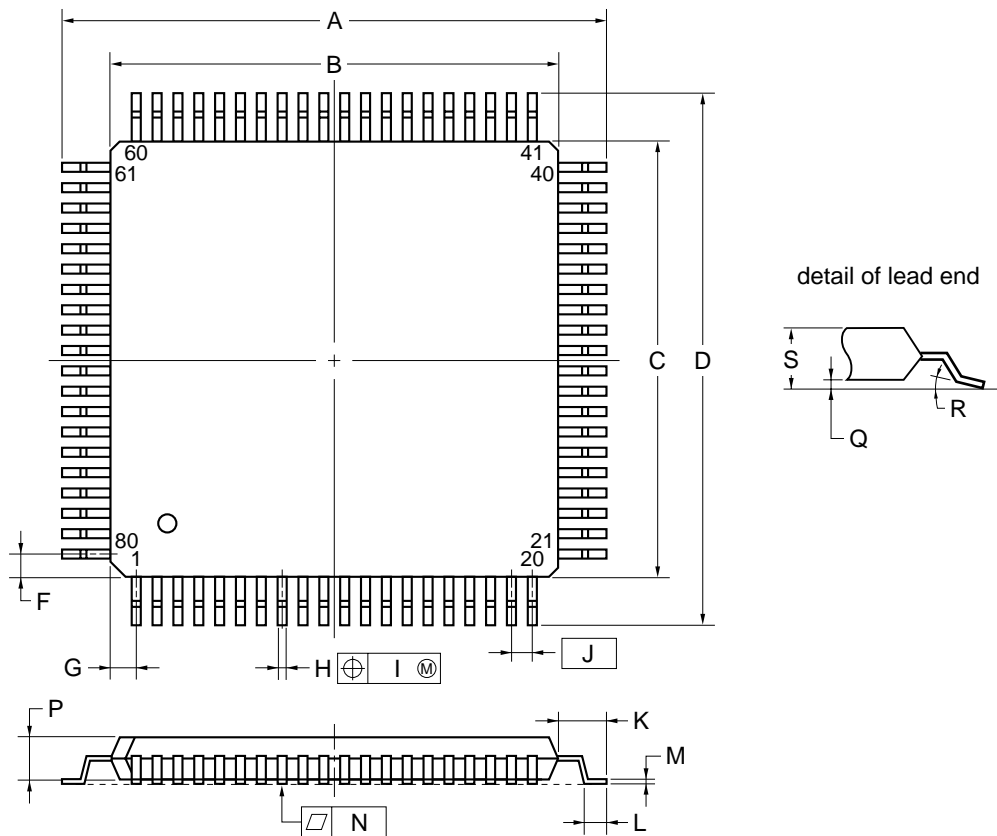
| ITEM | MILLIMETERS | INCHES |
|------|--|---|
| A | 17.2±0.4 | 0.677±0.016 |
| B | 14.0±0.2 | 0.551 ^{+0.009} _{-0.008} |
| C | 14.0±0.2 | 0.551 ^{+0.009} _{-0.008} |
| D | 17.2±0.4 | 0.677±0.016 |
| F | 0.825 | 0.032 |
| G | 0.825 | 0.032 |
| H | 0.30±0.10 | 0.012 ^{+0.004} _{-0.005} |
| I | 0.13 | 0.005 |
| J | 0.65 (T.P.) | 0.026 (T.P.) |
| K | 1.6±0.2 | 0.063±0.008 |
| L | 0.8±0.2 | 0.031 ^{+0.009} _{-0.008} |
| M | 0.15 ^{+0.10} _{-0.05} | 0.006 ^{+0.004} _{-0.003} |
| N | 0.10 | 0.004 |
| P | 2.7 | 0.106 |
| Q | 0.1±0.1 | 0.004±0.004 |
| R | 5°±5° | 5°±5° |
| S | 3.0 MAX. | 0.119 MAX. |

S80GC-65-3B9-4

Remark Dimensions and materials of ES product are the same as those of mass-production products.

μPD78056FYGC-xxx-8BT, 78058FYGC-xxx-8BT

80 PIN PLASTIC QFP (14×14)



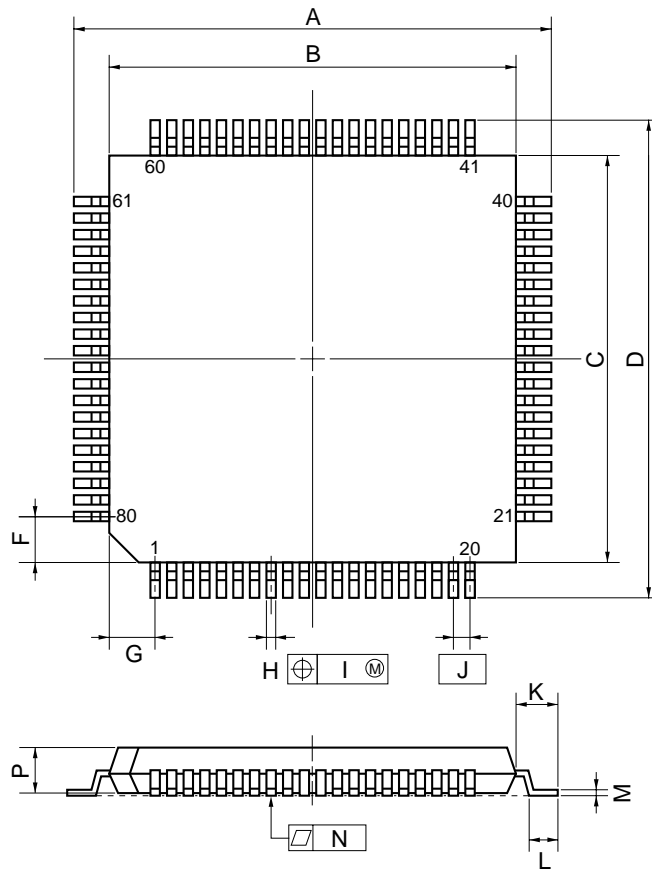
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|------|--|---|
| A | 17.20±0.20 | 0.677±0.008 |
| B | 14.00±0.20 | 0.551 ^{+0.009} _{-0.008} |
| C | 14.00±0.20 | 0.551 ^{+0.009} _{-0.008} |
| D | 17.20±0.20 | 0.677±0.008 |
| F | 0.825 | 0.032 |
| G | 0.825 | 0.032 |
| H | 0.32±0.06 | 0.013 ^{+0.002} _{-0.003} |
| I | 0.13 | 0.005 |
| J | 0.65 (T.P.) | 0.026 (T.P.) |
| K | 1.60±0.20 | 0.063±0.008 |
| L | 0.80±0.20 | 0.031 ^{+0.009} _{-0.008} |
| M | 0.17 ^{+0.03} _{-0.07} | 0.007 ^{+0.001} _{-0.003} |
| N | 0.10 | 0.004 |
| P | 1.40±0.10 | 0.055±0.004 |
| Q | 0.125±0.075 | 0.005±0.003 |
| R | 3° ^{+7°} _{-3°} | 3° ^{+7°} _{-3°} |
| S | 1.70 MAX. | 0.067 MAX. |

P80GC-65-8BT

80 PIN PLASTIC TQFP (FINE PITCH) (12 × 12)



NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|------|---|---|
| A | 14.0±0.2 | 0.551 ^{+0.009} _{-0.008} |
| B | 12.0±0.2 | 0.472 ^{+0.009} _{-0.008} |
| C | 12.0±0.2 | 0.472 ^{+0.009} _{-0.008} |
| D | 14.0±0.2 | 0.551 ^{+0.009} _{-0.008} |
| F | 1.25 | 0.049 |
| G | 1.25 | 0.049 |
| H | 0.22 ^{+0.05} _{-0.04} | 0.009±0.002 |
| I | 0.10 | 0.004 |
| J | 0.5 (T.P.) | 0.020 (T.P.) |
| K | 1.0±0.2 | 0.039 ^{+0.009} _{-0.008} |
| L | 0.5±0.2 | 0.020 ^{+0.008} _{-0.009} |
| M | 0.145 ^{+0.055} _{-0.045} | 0.006±0.002 |
| N | 0.10 | 0.004 |
| P | 1.05 | 0.041 |
| Q | 0.05±0.05 | 0.002±0.002 |
| R | 5°±5° | 5°±5° |
| S | 1.27 MAX. | 0.050 MAX. |

P80GK-50-BE9-4

Remark Dimensions and materials of ES product are the same as those of mass-production products.

13. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 13-1. Surface Mounting Type Soldering Conditions (1/2)

- (1) μPD78056FYGC-xxx-3B9 : 80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm)
- μPD78058FYGC-xxx-3B9 : 80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm)

| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
|------------------|--|------------------------------|
| Infrared reflow | Package peak temperature: 235°C, Duration: 30 sec. max. (at 210°C or above), Number of times: Three times max. | IR35-00-3 |
| VPS | Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above), Number of times: Three times max. | VP15-00-3 |
| Wave soldering | Solder bath temperature : 260°C max., Duration : 10 sec. max., Number of times: once, Preheating temperature : 120°C max. (package surface temperature) | WS60-00-1 |
| Partial heating | Pin temperature: 300°C max. Duration: 3 sec. max. (per pin row) | — |

Caution Use of more than one soldering method should be avoided (except in the case of partial heating).

- ★ (2) μPD78056FYGC-xxx-8BT : 80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm)
- μPD78058FYGC-xxx-8BT : 80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm)

| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
|------------------|--|------------------------------|
| Infrared reflow | Package peak temperature: 235°C, Duration: 30 sec. max. (at 210°C or above), Number of times: Twice max. | IR35-00-2 |
| VPS | Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above), Number of times: Twice max. | VP15-00-2 |
| Wave soldering | Solder bath temperature : 260°C max., Duration : 10 sec. max., Number of times: once, Preheating temperature : 120°C max. (package surface temperature) | WS60-00-1 |
| Partial heating | Pin temperature: 300°C max. Duration: 3 sec. max. (per pin row) | — |

Caution Use of more than one soldering method should be avoided (except in the case of partial heating).

Table 13-1. Surface Mounting Type Soldering Conditions (2/2)

(3) μPD78058FYGK-xxx-BE9: 80-pin plastic QFP (fine pitch) (12 × 12 mm)

| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
|------------------|--|------------------------------|
| Infrared reflow | Package peak temperature: 235°C, Duration: 30 sec. max. (at 210°C or above), Number of times: Three times max., Time limit: 7 days Note (thereafter 10 hours 125°C prebaking required) | IR35-107-3 |
| VPS | Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above), Number of times: Three times max., Time limit: 7 days Note (thereafter 10 hours 125°C prebaking required) | VP15-107-3 |
| Wave Soldering | Solder bath temperature: 260°C max., Duration: 10 sec. max., Number of times: once, Preheating temperature: 120°C max. (package surface temperature). Time limit: 7 days Note (therefore 10 hours 125°C prebaking required) | WS60-107-1 |
| Partial Heating | Pin temperature: 300°C max. Duration: 3 sec. max. (per pin row) | — |

Note For the storage period after dry-pack decompression storage conditions are max. 25°C, 65 % RH.

Caution Use of more than one soldering method should be avoided (except in the case of partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78058FY Subseries.

Language Processing Software

| | |
|-----------------------------------|---|
| RA78K/0 Notes 1, 2, 3, 4 | Assembler package common to 78K/0 Series |
| CC78K/0 Notes 1, 2, 3, 4 | C compiler package common to 78K/0 Series |
| DF78054 Notes 1, 2, 3, 4 | Device file common to μPD78054 Subseries |
| CC78K/0-L Notes 1, 2, 3, 4 | C compiler library source file common to 78K/0 Series |

PROM Writing Tools

| | |
|--------------------------------------|--|
| PG-1500 | PROM programmer |
| PA-78P054GC | Programmer adapters connected to PG-1500 |
| PG-1500 controller Notes 1, 2 | PG-1500 control program |

Debugging Tools

| | | |
|---|---------------------------------------|--|
| | IE-78000-R | In-circuit emulator common to 78K/0 Series |
| | IE-78000-R-A | 78K/0 Series common to in-circuit emulator (for integrated debugger) |
| | IE-78000-R-BK | Break board common to 78K/0 Series |
| | IE-78064-R-EM Note 8 | Emulation board common to μPD78064 Subseries |
| | IE-780308-R-EM | Emulation board common to μPD780308 Subseries |
| ★ | IE-78000-R-SV3 | Interface adapter and cable when EWS is used as host machine (for IE-78000-R-A) |
| ★ | IE-70000-98-IF-B | Interface adapter when PC-9800 series (except notebook type) is used as host machine. |
| ★ | IE-70000-98N-IF | Interface adapter and cable when notebook type PC-9800 series is used as host machine. |
| ★ | IE-70000-PC-IF-B | Interface adapter when IBM PC/AT™ and compatibles are used as host machine. |
| | EP-78230GC-R | Emulation probe common to μPD78234 Subseries |
| | EP-78054GK-R | Emulation probe common to μPD78054 Subseries |
| | EV-9200GC-80 | Socket to be mounted on the target system board manufactured for 80-pin plastic QFP (GC-3B9, GC-8BT type) |
| | TGK-080SDW | Adapter to be mounted in the target system board manufactured for 80-pin plastic TQFP (GK-BE9 type) Product made by TOKYO ELETECH Corporation ((03) 5295-1661). Contact an NEC dealer regarding the purchase of this product. |
| | SM78K0 Notes 5, 6, 7 | System simulator common to 78K/0 Series |
| | ID78K0 Notes 4, 5, 6, 7 | Integrated debugger for IE-78000-R |
| | SD78K/0 Notes 1, 2 | IE-78000-R screen debugger |
| | DF78054 Notes 1, 2, 4, 5, 6, 7 | μPD78054 Subseries device file |

Real-Time OS

| | |
|---------------------------------|-------------------------------|
| RX78K/0 Notes 1, 2, 3, 4 | Real-time OS for 78K/0 Series |
| MX78K0 Notes 1, 2, 3, 4 | Real-time OS for 78K/0 Series |

Fuzzy Inference Development Support System

| | |
|---|------------------------------------|
| FE9000 Note 1 / FE9200 Note 6 | Fuzzy knowledge data creation tool |
| FT9080 Note 1 / FT9085 Note 2 | Translator |
| FI78K0 Notes 1, 2 | Fuzzy inference module |
| FD78K0 Notes 1, 2 | Fussy inference debugger |

Notes 1. PC-9800 series (MS-DOS™) based

2. IBM PC/AT and compatibles (PC DOS™/IBM DOS™/MS-DOS) based

3. HP9000 series 300™ (HP-UX™) based

4. HP9000 series 700™ (HP-UX) based, SPARCstation™ (SunOS™) based, EWS4800 series (EWS-UX/V) based

5. PC-9800 series (MS-DOS + Windows™) based

6. IBM PC/AT and compatibles (PC DOS/IBM DOS/MS-DOS + Windows) based

7. NEWS™ (NEWS-OS™) based

8. Maintenance product

Remarks 1. For third party development tools, see **78K/0 Series Selection Guide (U11126E)**.

2. The RA78K/0, CC78K/0, SM78K0, ID78K0, SD78K/0, RX78K/0 are used in combination with the DF78054.

APPENDIX B. RELATED DOCUMENTS

Device Related Documents

| Document Name | Document No. (English) | Document No. (Japanese) |
|--|---------------------------|----------------------------|
| μPD78058F, 78058FY Subseries User's Manual | U12068E | U12068J |
| μPD78056FY, 78058FY Data Sheet | This document | U10121J |
| μPD78P058FY Data Sheet | U12076E | U12076J |
| 78K/0 Series User's Manual-Instruction | U12326E | U12326J |
| 78K/0 Series Instruction Set | – | U10904J |
| 78K/0 Series Instruction Table | – | U10903J |

Caution The above related documents are subject to change without notice. Be sure to read the latest documents before designing.

Development Tool Related Documents (User's Manual)

| Document Name | | Document No. (English) | Document No. (Japanese) |
|--|--|---------------------------|----------------------------|
| RA78K Series Assembler Package | Operation | EEU-1399 | EEU-809 |
| | Language | EEU-1404 | EEU-815 |
| RA78K Series Structured Assembler Preprocessor | | EEU-1402 | U12323J |
| RA78K0 Assembler Package | Operation | U11802E | U11802J |
| | Assembly Language | U11801E | U11801J |
| | Structured Assembly Language | U11789E | U11789J |
| CC78K Series C Compiler | Operation | EEU-1280 | EEU-656 |
| | Language | EEU-1284 | EEU-655 |
| CC78K0 C Compiler | Operation | U11517E | U11517J |
| | Language | U11518E | U11518J |
| CC78K/0 C Compiler Application Note | Programming know-how | EEA-1208 | EEA-618 |
| CC78K Series Library Source File | | – | U12322J |
| PG-1500 PROM Programmer | | EEU-1335 | U11940J |
| PG-1500 Controller PC-9800 Series (MS-DOS) based | | EEU-1291 | EEU-704 |
| PG-1500 Controller IBM PC Series (PC DOS) based | | U10540E | EEU-5008 |
| IE-78000-R | | U11376E | U11376J |
| IE-78000-R-A | | U10057E | U10057J |
| IE-78000-R-BK | | EEU-1427 | EEU-867 |
| IE-78064-R-EM | | EEU-1443 | EEU-905 |
| IE-780308-R-EM | | U11362E | U11362J |
| EP-78230 | | EEU-1515 | EEU-985 |
| EP-78054GK-R | | EEU-1468 | EEU-932 |
| SM78K0 System Simulator, Windows based | Reference | U10181E | U10181J |
| SM78K Series System Simulator | External parts user open interface specification | U10092E | U10092J |
| ID78K0 Integrated Debugger, EWS based | Reference | – | U11151J |
| ID78K0 Integrated Debugger, PC based | Reference | U11539E | U11539J |
| ID78K0 Integrated Debugger, Windows based | Guide | U11649E | U11649J |
| SD78K/0 Screen Debugger PC-9800 Series (MS-DOS) based | Introduction | – | EEU-852 |
| | Reference | – | U10952J |
| SD78K/0 Screen Debugger IBM PC/AT (PC DOS) based | Introduction | U10539E | EEU-5024 |
| | Reference | U11279E | U11279J |

Caution The above related documents are subject to change without notice. Be sure to read the latest documents before designing.

Embedded Software Documents (User's Manual)

| Document Name | | Document No. (English) | Document No. (Japanese) |
|---|--------------|---------------------------|----------------------------|
| 78K/0 Series Real-time OS | Fundamental | U11537E | U11537J |
| | Installation | U11536E | U11536J |
| 78K/0 Series OS MX78K0 | Fundamental | U12257E | U12257J |
| Fuzzy Knowledge Data Creation Tool | | EEU-1438 | EEU-829 |
| 78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System Translator | | EEU-1444 | EEU-862 |
| 78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module | | EEU-1441 | EEU-858 |
| 78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger | | EEU-1458 | EEU-921 |

Other Documents

| Document Name | Document No. (English) | Document No. (Japanese) |
|---|---------------------------|----------------------------|
| IC Package Manual | C10943X | |
| Semiconductor Device Mounting Technology Manual | C10535E | C10535J |
| Quality Grades on NEC Semiconductor Devices | C11531E | C11531J |
| NEC Semiconductor Device Reliability/Quality Control System | C10983E | C10983J |
| Electrostatic Discharge (ESD) Test | – | MEM-539 |
| Guide to Quality Assurance for Semiconductor Devices | MEI-1202 | C11893J |
| Microcomputer Product Series Guide | – | U11416J |

Caution The above related documents are subject to change without notice. Be sure to read the latest documents before designing.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Fax: 800-729-9288

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