NEC

MOS INTEGRATED CIRCUIT

μPD780306, 780308

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

μPD780306 and 780308 are products in the μPD780308 subseries within the 78K/0 series, which incorporates LCD controller/driver, 8-bit resolution A/D converter, timer, serial interface, interrupt functions and many other peripheral hardwares.

A one-time PROM product capable of operating in the same power supply voltage range as of the mask ROM product, EPROM product, μPD78P0308, and other development tools are available.

For the details of functional description, refer to the following user's manual.

μPD780308, 780308Y Subseries User's Manual : U11377E

78K/0 Series User's Manual (Instruction) : U12326E

FEATURES

- Large on-chip ROM & RAM

Item / Product Name	Program Memory (ROM)	Data Memory		
		Internal High-Speed RAM	Internal Extended RAM	LCD Display RAM
μPD780306	48K bytes	1024 bytes	1024 bytes	40 × 4 bits
μPD780308	60K bytes			

- Minimum instruction execution time can be varied from high speed (0.4 μs) to ultra-low speed (122 μs)
- I/O ports: 57 (including segment signal output alternate-function pins)
- LCD controller/driver
  Supply voltage V_{DD} = 2.0 to 5.5 V (Operable in any mode)
- 8-bit resolution A/D converter : 8 channels
- Serial interface : 3 channels
- Timer: 5 channels
- Supply voltage : V_{DD} = 2.0 to 5.5 V

APPLICATIONS

Celullar phones, compact disk players, cameras, meters, etc.

Document No. U11105EJ3V1DS00 (3rd edition)
Date Published June 2001 N CP(K)
Printed in Japan

The mark ★ shows major revised points.

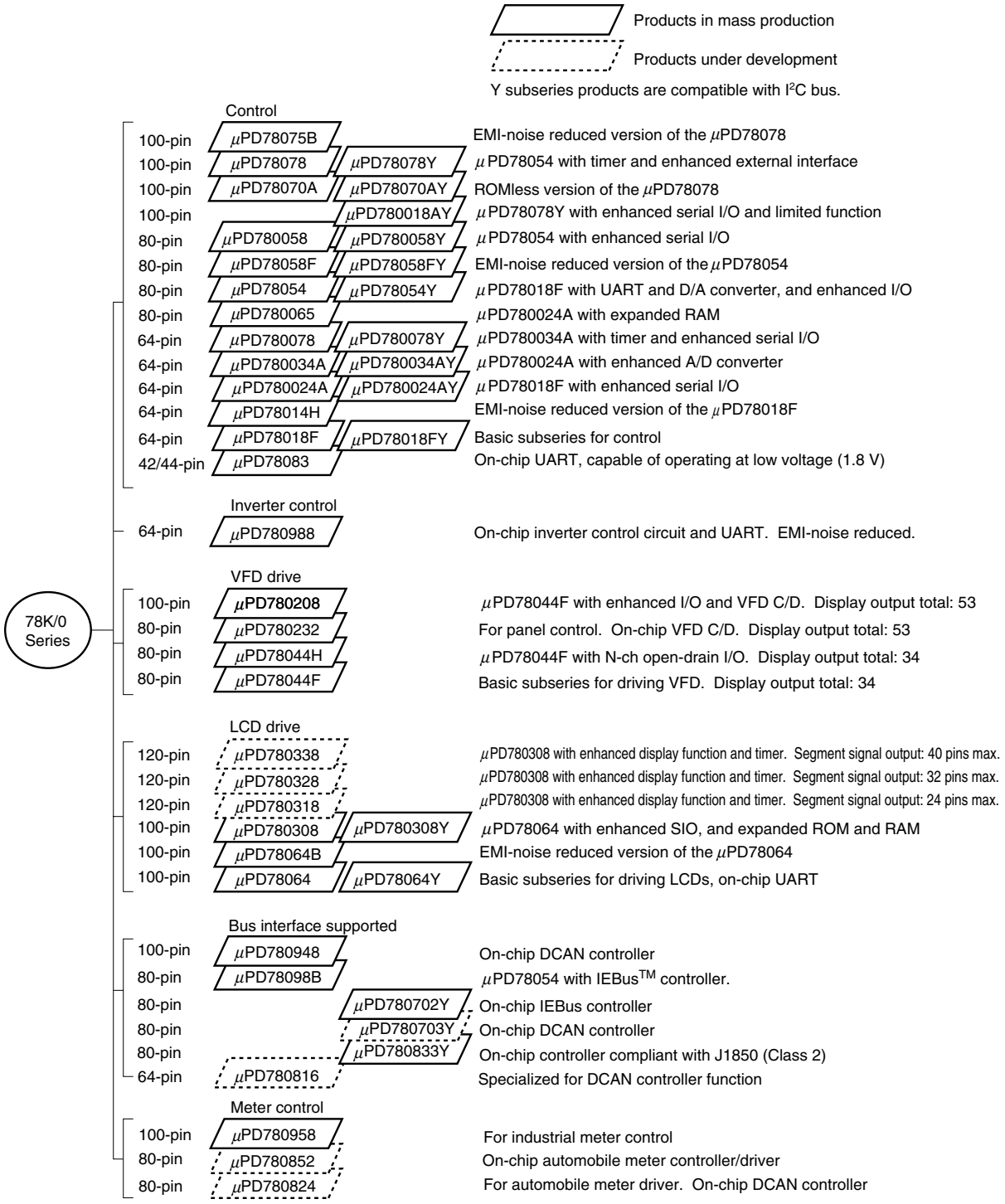
ORDERING INFORMATION

	Part Number	Package
★	μPD780306GC-×××-8EU	100-pin plastic LQFP (Fine pitch) (14 × 14 mm)
	μPD780306GF-×××-3BA	100-pin plastic QFP (14 × 20 mm)
★	μPD780308GC-×××-8EU	100-pin plastic LQFP (Fine pitch) (14 × 14 mm)
	μPD780308GF-×××-3BA	100-pin plastic QFP (14 × 20 mm)

Remark ××× indicates ROM code suffix.

★ 78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.



Remark VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major functional differences among the subseries are shown below.

Subseries Name \ Function		ROM Capacity	Timer 8-bit	Timer 16-bit	Timer Watch	Timer WDT	8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
Control	μPD78075B	32 K to 40 K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	88	1.8 V	Yes
	μPD78078	48 K to 60 K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24 K to 60 K	2 ch							3 ch (time-division UART: 1 ch)	68	1.8 V	
	μPD78058F	48 K to 60 K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16 K to 60 K										2.0 V	
	μPD780065	40 K to 48 K							–	4 ch (UART: 1 ch)	60	2.7 V	
	μPD780078	48 K to 60 K		2 ch			–	8 ch		3 ch (UART: 2 ch)	52	1.8 V	
	μPD780034A	8 K to 32 K		1 ch						3 ch (UART: 1 ch)	51		
	μPD780024A						8 ch	–					
	μPD78014H									2 ch	53		
	μPD78018F	8 K to 60 K											
	μPD78083	8 K to 16 K		–	–					1 ch (UART: 1 ch)	33		–
Inverter control	μPD780988	16 K to 60 K	3 ch	**Note**	–	1 ch	–	8 ch	–	3 ch (UART: 2 ch)	47	4.0 V	Yes
VFD drive	μPD780208	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	2 ch	74	2.7 V	–
	μPD780232	16 K to 24 K	3 ch	–	–		4 ch				40	4.5 V	
	μPD78044H	32 K to 48 K	2 ch	1 ch	1 ch		8 ch			1 ch	68	2.7 V	
	μPD78044F	16 K to 40 K								2 ch			
LCD drive	μPD780338	48 K to 60 K	3 ch	2 ch	1 ch	1 ch	–	10 ch	1 ch	2 ch (UART: 1 ch)	54	1.8 V	–
	μPD780328										62		
	μPD780318										70		
	μPD780308	48 K to 60 K	2 ch	1 ch			8 ch	–	–	3 ch (time-division UART: 1 ch)	57	2.0 V	
	μPD78064B	32 K								2 ch (UART: 1 ch)			
	μPD78064	16 K to 32 K											
Bus interface supported	μPD780948	60 K	2 ch	2 ch	1 ch	1 ch	8 ch	–	–	3 ch (UART: 1 ch)	79	4.0 V	Yes
	μPD78098B	40 K to 60 K		1 ch					2 ch		69	2.7 V	–
	μPD780816	32 K to 60 K		2 ch			12 ch		–	2 ch (UART: 1 ch)	46	4.0 V	
Meter control	μPD780958	48 K to 60 K	4 ch	2 ch	–	1 ch	–	–	–	2 ch (UART: 1 ch)	69	2.2 V	–
Dash board control	μPD780852	32 K to 40 K	3 ch	1 ch	1 ch	1 ch	5 ch	–	–	3 ch (UART: 1 ch)	56	4.0 V	–
	μPD780824	32 K to 60 K								2 ch (UART: 1 ch)	59		

Note 16-bit timer: 2 channels
10-bit timer: 1 channel

OVERVIEW OF FUNCTION

Item \ Product Name		μPD780306	μPD780308
Internal memory	ROM	48K bytes	60K bytes
	High-speed RAM	1024 bytes	
	Extended RAM	1024 bytes	
	LCD display RAM	40 × 4 bits	
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		On-chip minimum instruction execution time cycle modification function	
	When main system clock selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (at 5.0 MHz operation)	
	When subsystem clock selected	122 μs (at 32.768 kHz operation)	
Instruction set		• 16-bit operation • Multiplication/division (8 bits × 8 bits,16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD correction, etc.	
I/O ports (including segment signal output pins)		Total : 57 • CMOS input : 2 • CMOS I/O : 55	
A/D converter		• 8-bit resolution × 8 channels	
LCD controller/driver		• Segment signal output : Maximum 40 • Common signal output : Maximum 4 • Bias : 1/2 or 1/3 switchable	
Serial interface		• 3-wire serial I/O/SBI/2-wire serial I/O mode selectable : 1 channel • 3-wire serial I/O/UART mode selectable : 1 channel • 3-wire serial I/O mode : 1 channel	
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel	
Timer output		3 (14-bit PWM output capability : 1)	
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (at main system clock: 5.0 MHz operation) 32.768 kHz (at subsystem clock: 32.768 kHz operation)	
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz, 9.8 kHz (at main system clock 5.0 MHz operation)	
Vectored interrupt sources	Maskable	Internal : 13, external : 6	
	Non-maskable	Internal : 1	
	Software	1	
Test input		Internal : 1, external: 1	
Supply voltage		V_{DD} = 2.0 to 5.5 V	
Package		• 100-pin plastic LQFP (Fine pitch) (14 × 14 mm) • 100-pin plastic QFP (14 × 20 mm)	

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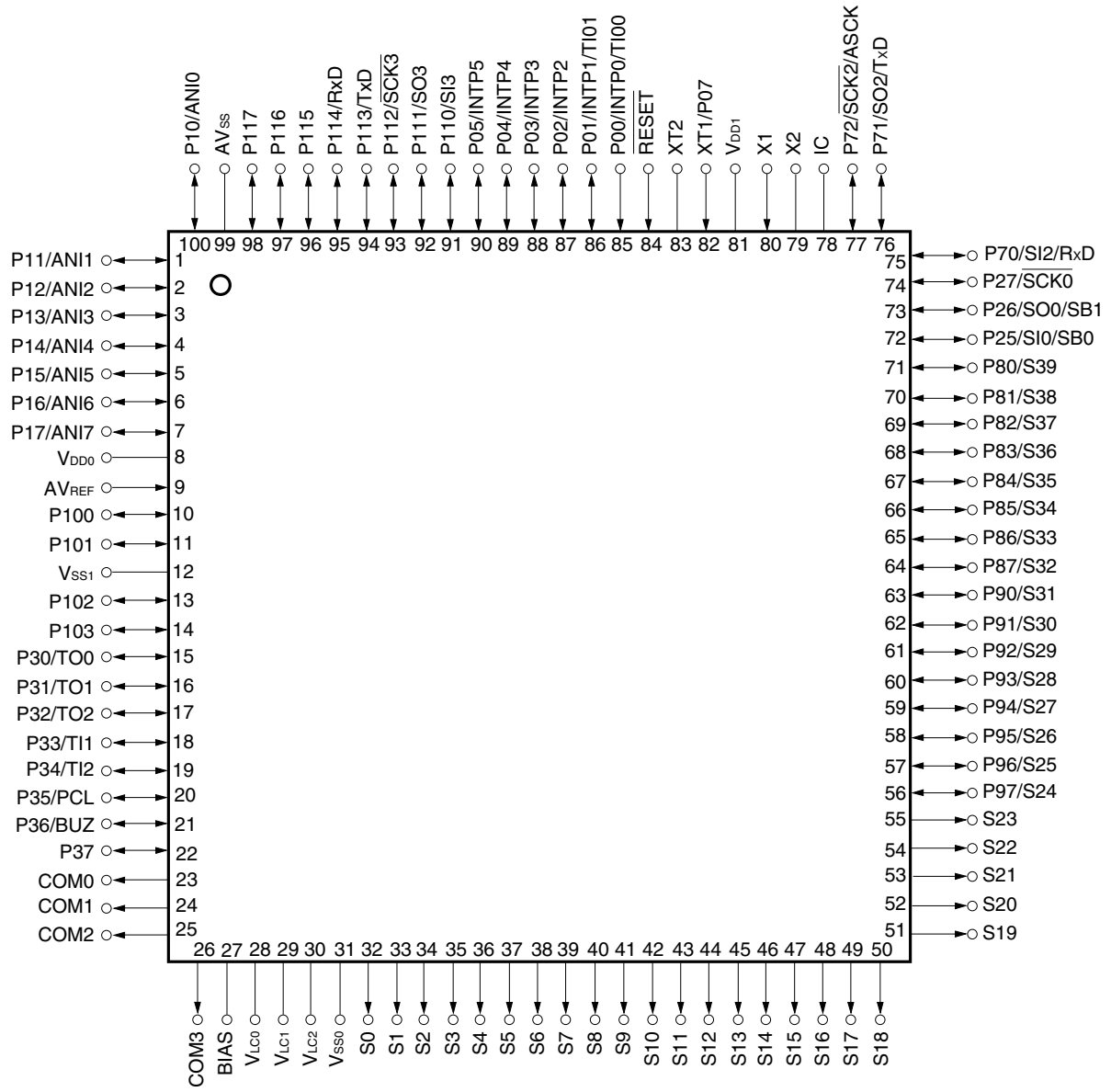
1. PIN CONFIGURATION (TOP VIEW)

• 100-pin plastic LQFP (Fine pitch) (14 × 14 mm)
μPD780306GC-×××-8EU, 780308GC-×××-8EU



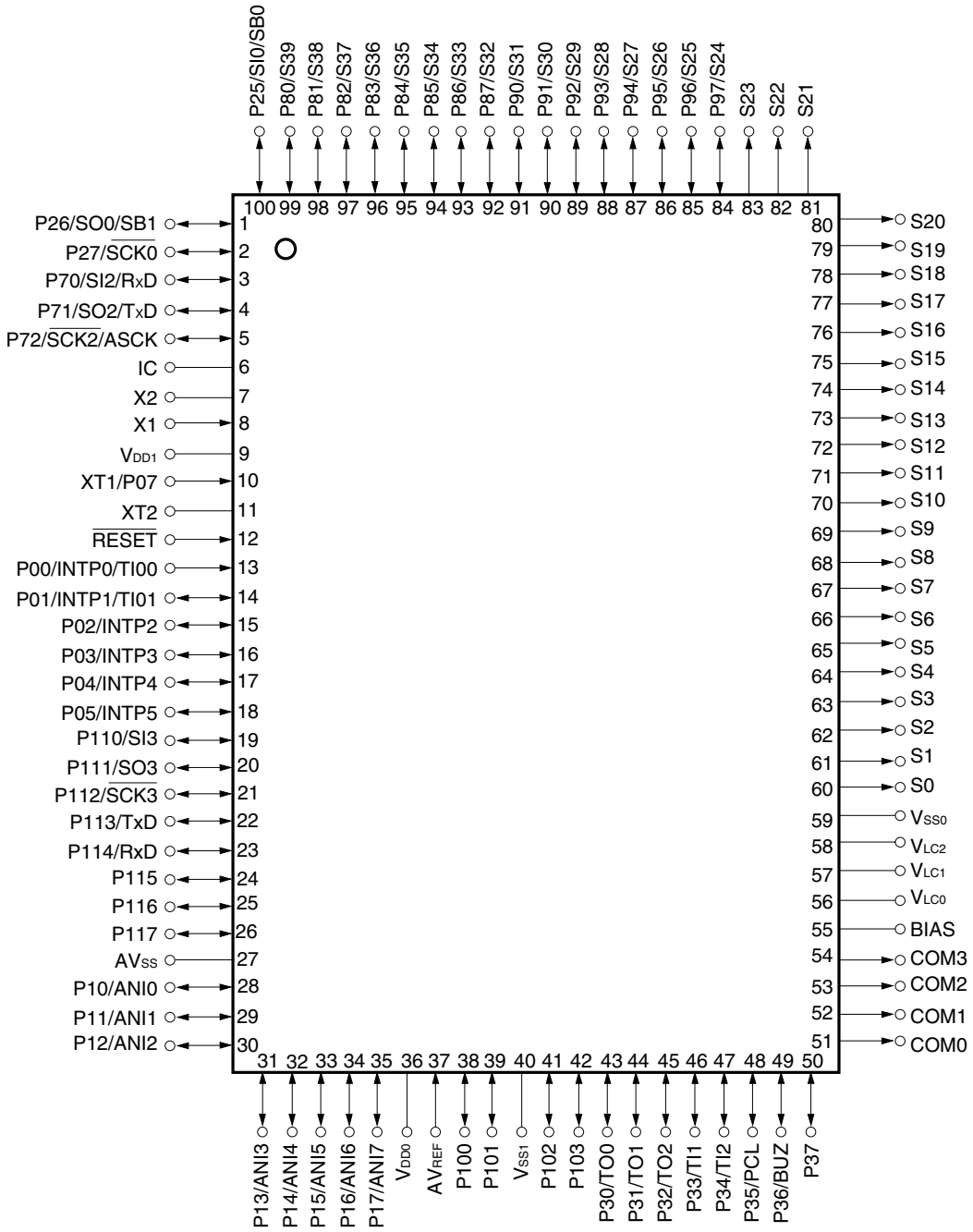
Cautions 1. Connect directly the IC (Internally Connected) pin to V_{SS0} or V_{SS1}.

2. Connect the AV_{SS} pin to V_{SS0}.

Remark When using in applications where noise from inside the microcontroller has to be reduced, it is recommended that countermeasures against the noise are taken, such as supplying power separately to V_{DD0} and V_{DD1}, and connecting V_{DD0} and V_{DD1} to ground lines separately.

• **100-pin plastic QFP (14 × 20 mm)**

μPD780306GF-×××-3BA, 780308GF-×××-3BA



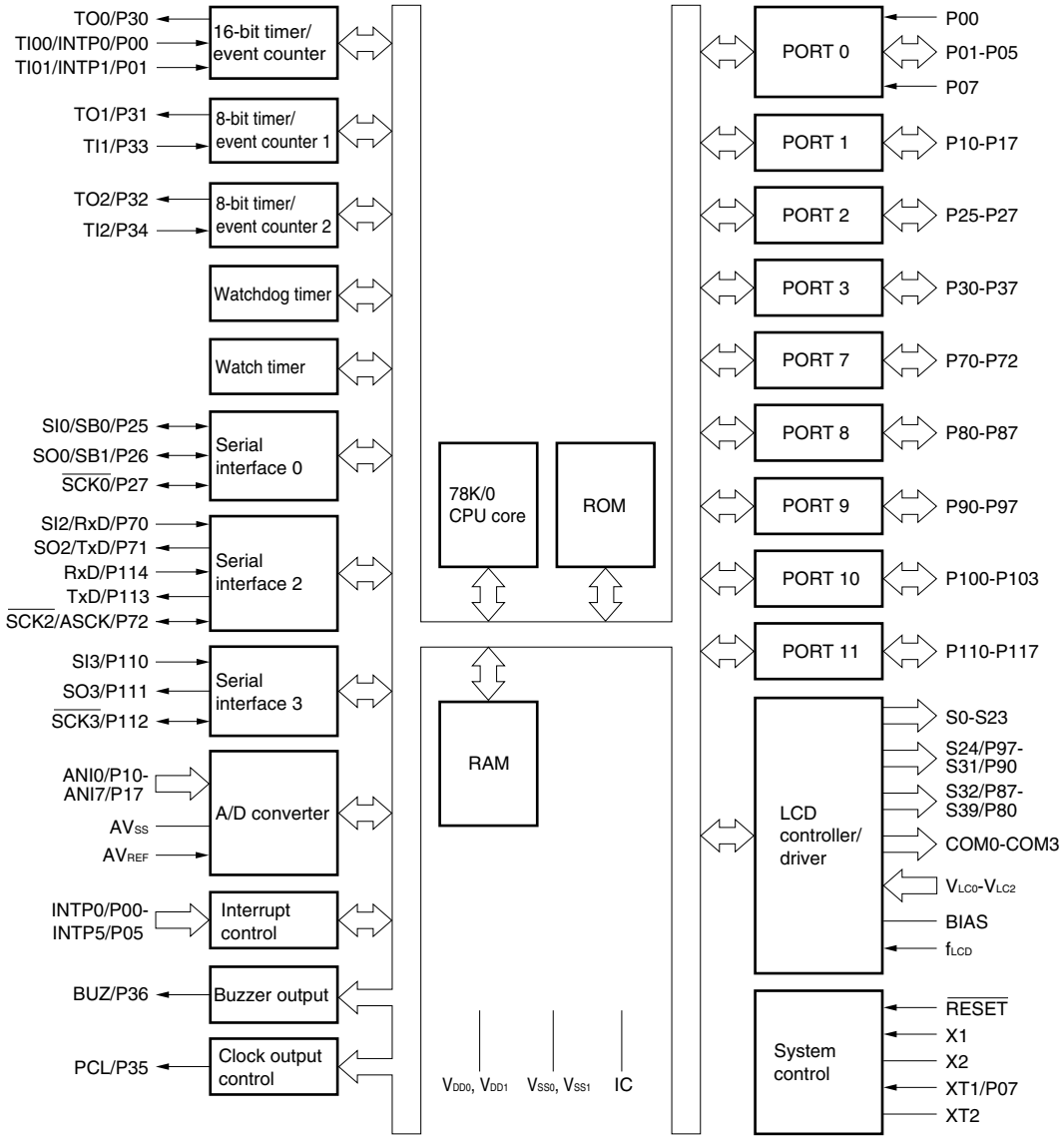
Cautions 1. Connect directly the IC (Internally Connected) pin to V_{SS0} or V_{SS1}.

2. Connect the AV_{SS} pin to V_{SS0}.

Remark When using in applications where noise from inside the microcontroller has to be reduced, it is recommended that countermeasures against the noise are taken, such as supplying power separately to V_{DD0} and V_{DD1}, and connecting V_{DD0} and V_{DD1} to ground lines separately.

ANI0-ANI7	:	Analog Input
ASCK	:	Asynchronous Serial Clock
AV_{REF}	:	Analog Reference Voltage
AV_{SS}	:	Analog Ground
BIAS	:	LCD Power Supply Bias Control
BUZ	:	Buzzer Clock
COM0-COM3	:	Common Output
IC	:	Internally Connected
INTP0-INTP5	:	Interrupt from Peripherals
P00-P05, P07	:	Port0
P10-P17	:	Port1
P25-P27	:	Port2
P30-P37	:	Port3
P70-P72	:	Port7
P80-P87	:	Port8
P90-P97	:	Port9
P100-P103	:	Port10
P110-P117	:	Port11
PCL	:	Programmable Clock
$\overline{\text{RESET}}$	:	Reset
RxD	:	Receive Data
S0-S39	:	Segment Output
SB0, SB1	:	Serial Bus
$\overline{\text{SCK0}}$, $\overline{\text{SCK2}}$, $\overline{\text{SCK3}}$	:	Serial Clock
SI0, SI2, SI3	:	Serial Input
SO0, SO2, SO3	:	Serial Output
TI00, TI01, TI1, TI2	:	Timer Input
TO0-TO2	:	Timer Output
TxD	:	Transmit Data
V_{DD0}, V_{DD1}	:	Power Supply
V_{LC0}-V_{LC2}	:	LCD Power Supply
V_{SS0}, V_{SS1}	:	Ground
X1, X2	:	Crystal (Main System Clock)
XT1, XT2	:	Crystal (Subsystem Clock)

2. BLOCK DIAGRAM



Remark The internal ROM capacity varies depending on the product.

3. PIN FUNCTIONS

3.1 PORT PINS (1/2)

Pin Name	I/O	Function		On Reset	Alternate Function
P00	Input	Port 0 7-bit Input/output port.	Input only	Input	INTP0/TI00
P01	Input/ output		Input/output can be specified bit-wise. When used as an input port, internal pull-up resistor can be used by software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P07[Note 1]	Input		Input only	Input	XT1
P10-P17	Input/ output	Port 1 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, internal pull-up resistor can be used by software.[Note 2]		Input	ANI0-ANI7
P25	Input/ output	Port 2 3-bit input/output port. Input/output can be specified bit-wise. When used as an input port, internal pull-up resistor can be used by software.		Input	SI0/SB0
P26					SO0/SB1
P27					$\overline{\text{SCK0}}$
P30	Input/ output	Port 3 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, internal pull-up resistor can be used by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—
P70	Input/ output	Port 7 3-bit input/output port. Input/output can be specified bit-wise. When used as an input port, internal pull-up resistor can be used by software.		Input	SI2/RxD
P71					SO2/TxD
P72					$\overline{\text{SCK2}}$/ASCK

Notes 1. When using the P07/XT1 pins as an input port, set (1) bit 6 (FRC) of the processor clock control register (PCC) (the on-chip feedback resistor of the subsystem clock oscillator should not be used).

2. When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input, port 1 is set to input mode. However, internal pull-up resistor is not automatically used.

3.1 NON-PORT PINS (2/2)

Pin Name	I/O	Function	On Reset	Alternate Function
P80-P87	Input/ output	Port 8 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, internal pull-up resistor can be used by software. Input/output port/segment signal output function can be specified in 2-bit unit by the LCD display control register (LCDC).	Input	S39-S32
P90-P97	Input/ output	Port 9 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, internal pull-up resistor can be used by software. Input/output port/segment signal output function can be specified in 2-bit unit by the LCD display control register (LCDC).	Input	S31-S24
P100-P103	Input/ output	Port 10 4-bit input/output port Input/output can be specified bit-wise. When used as an input port, internal pull-up resistor can be used by software. LED direct drive capability.	Input	—
P110	Input/ output	Port 11 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, internal pull-up resistor can be used by software. Falling edge detection capability.	Input	SI3
P111				SO3
P112				$\overline{\text{SCK3}}$
P113				TxD
P114				RxD
P115-P117				—

3.2 NON-PORT PINS (1/2)

Pin Name	I/O	Function	On Reset	Alternate Function
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
SI0	Input	Serial interface serial data input.	Input	P25/SB0
SI2				P70/RxD
SI3				P110
SO0	Output	Serial interface serial data output.	Input	P26/SB1
SO2				P71/TxD
SO3				P111
SB0	Input/output	Serial interface serial data input/output.	Input	P25/SI0
SB1				P26/SO0
$\overline{SCK0}$	Input/output	Serial interface serial clock input/output.	Input	P27
$\overline{SCK2}$				P72/ASCK
$\overline{SCK3}$				P112
RxD	Input	Asynchronous serial interface serial data input.	Input	P70/SI2, P114
TxD	Output	Asynchronous serial interface serial data output.	Input	P71/SO2, P113
ASCK	Input	Asynchronous serial interface serial clock input.	Input	P72/$\overline{SCK2}$
TI00	Input	External count clock input to 16-bit timer (TM0).	Input	P00/INTP0
TI01		Capture trigger signal input to capture register (CR00).		P01/INTP1
TI1		External count clock input to 8-bit timer (TM1).		P33
TI2		External count clock input to 8-bit timer (TM2).		P34
TO0	Output	16-bit timer (TM0) output (shared with 14-bit PWM output).	Input	P30
TO1		8-bit timer (TM1) output.		P31
TO2		8-bit timer (TM2) output.		P32
PCL	Output	Clock output (for main system clock, subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
S0-S23	Output	LCD controller/driver segment signal output.	Output	—
S24-S31			Input	P97-P90
S32-S39				P87-P80
COM0-COM3	Output	LCD controller/driver common signal output.	Output	—
V_{LC0}-V_{LC2}	—	LCD drive voltage. Split resistors can be incorporated by mask option.	—	—
BIAS	—	LCD drive power supply.	—	—

3.2 NON-PORT PINS (2/2)

Pin Name	I/O	Function	On Reset	Alternate Function
ANI0-ANI7	Input	A/D converter analog input.	Input	P10-P17
AV_{REF}	Input	Reference voltage input of A/D converter (shared with analog power supply).	—	—
AV_{SS}	—	Ground potential of A/D converter. Set the same potential as V_{SS0}.	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection.	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection.	Input	P07
XT2	—		—	—
V_{DD0}	—	Positive power supply for port block.	—	—
V_{SS0}	—	Ground potential for port block.	—	—
V_{DD1}	—	Positive power supply (except port and analog block).	—	—
V_{SS1}	—	Ground potential (except port and analog block).	—	—
IC	—	Internally connected. Connect directly to V_{SS0} or V_{SS1} pin.	—	—

3.3 PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, refer to **Figure 3-1**.

Table 3-1. Input/Output Circuit Type of Each Pin (1/2)

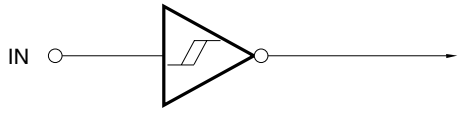
Pin Name	Input/output Circuit Type	I/O	Recommended Connection When Not Used
P00/INTP0/TI00	2	Input	Connect to V_{SS0}.
P01/INTP1/TI01	8-C	Input/output	Independently connect to V_{SS0} through resistor.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P07/XT1	16	Input	Connect to V_{DD0}.
P10/ANI0-P17/ANI7	11-B	Input/output	Independently connect to V_{DD0} or V_{SS0} through resistor.
P25/SI0/SB0	10-B		
P26/SO0/SB1			
P27/$\overline{SCK0}$			
P30/TO0	5-H		
P31/TO1			
P32/TO2			
P33/TI1	8-C		
P34/TI2			

Table 3-1. Input/Output Circuit Type of Each Pin (2/2)

Pin Name	Input/output Circuit Type	I/O	Recommended Connection When Not Used
P35/PCL	5-H	Input/output	Independently connect to V_{DD0} or V_{SS0} through resistor.
P36/BUZ			
P37			
P70/SI2/RxD	8-C		
P71/SO2/TxD	5-H		
P72/$\overline{SCK2}$/ASCK	8-C		
P80/S39 to P87/S32	17-C		
P90/S31 to P97/S24			
P100 to P103	5-H		
P110/SI3	8-C		Independently connect to V_{DD0} through resistor.
P111/SO3			
P112/$\overline{SCK3}$			
P113/TxD			
P114/RxD			
P115 to P117			
S0 to S23	17-B	Output	Leave unconnected.
COM0 to C0M3	18-A		
V_{LC0} to V_{LC2}	—	—	
BIAS			
$\overline{RESET}$	2	Input	—
XT2	16	—	Leave unconnected.
AV_{REF}	—		Connect to V_{SS0}.
AV_{SS}			Connect to V_{SS0}.
IC			Connect directly to V_{SS0} or V_{SS1}.

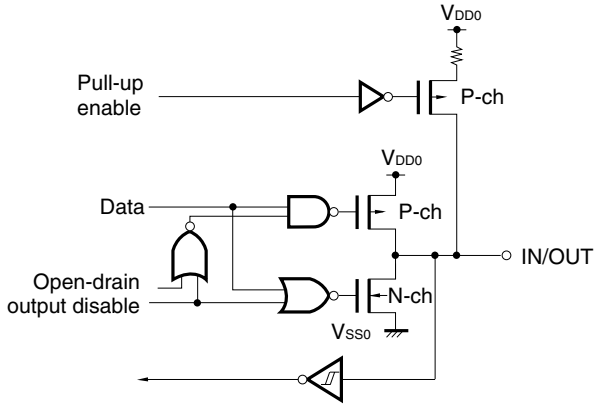
Figure 3-1. Pin Input/Output Circuits (1/2)

Type 2

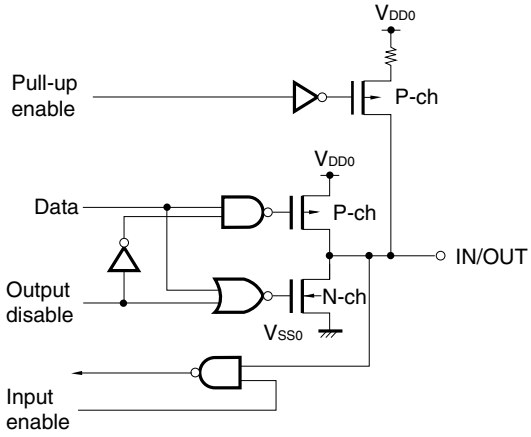


Schmitt-triggered input with hysteresis characteristic

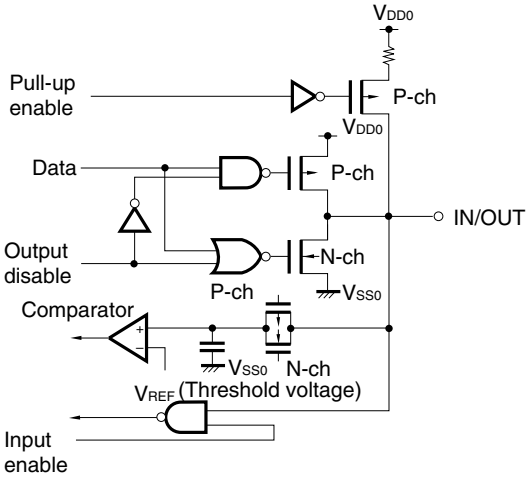
Type 10-B



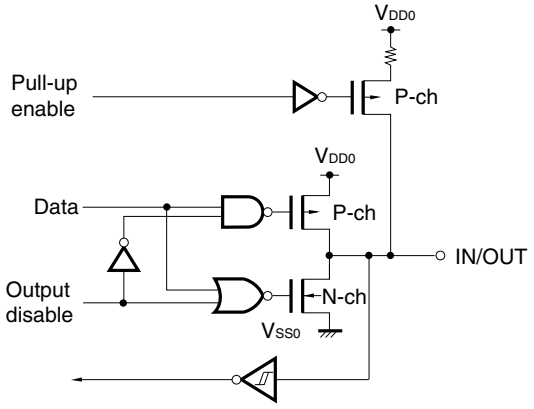
Type 5-H



Type 11-B



Type 8-C



Type 16

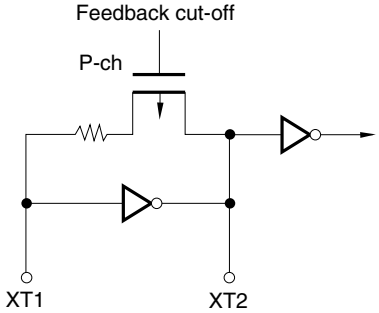
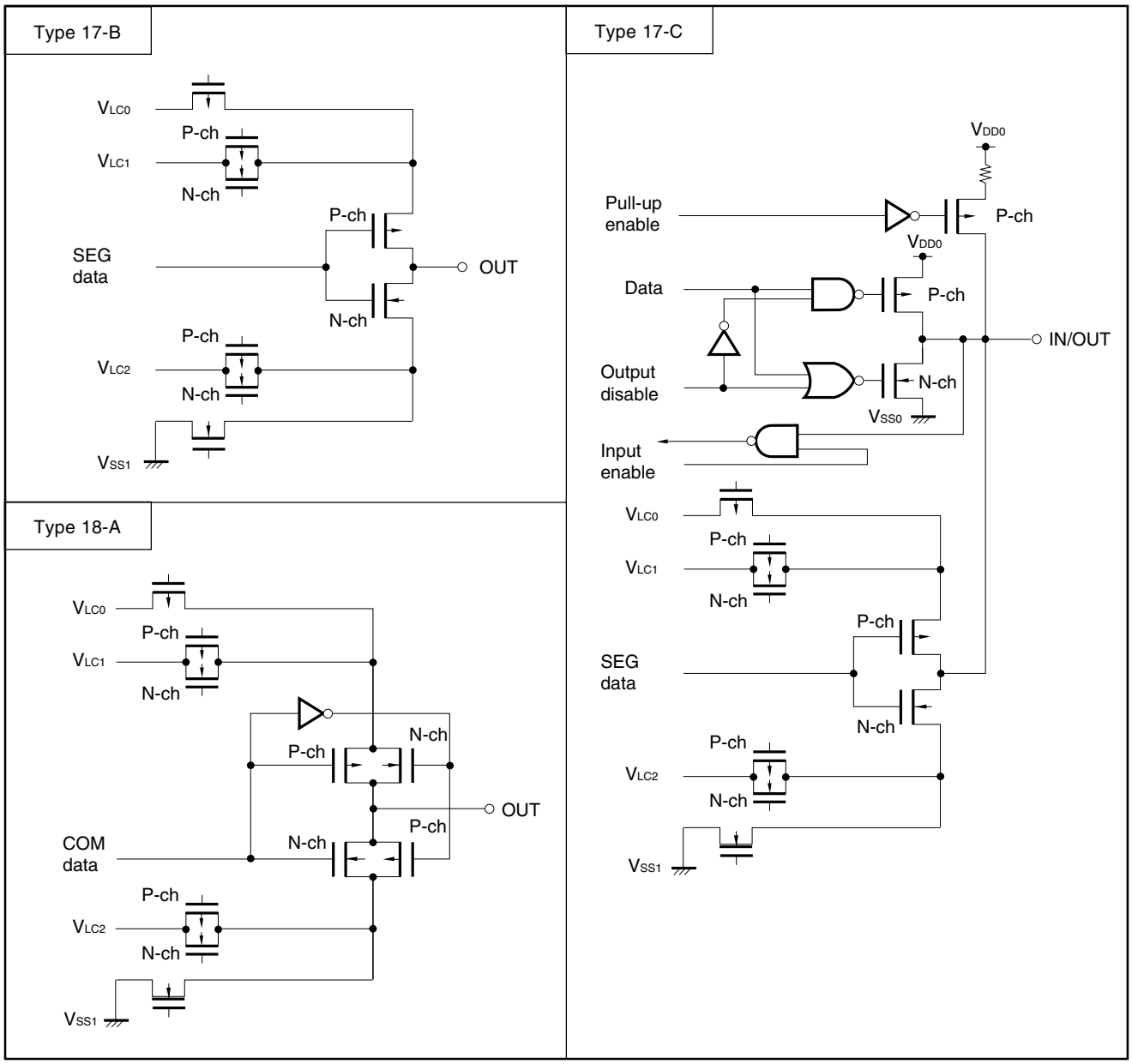


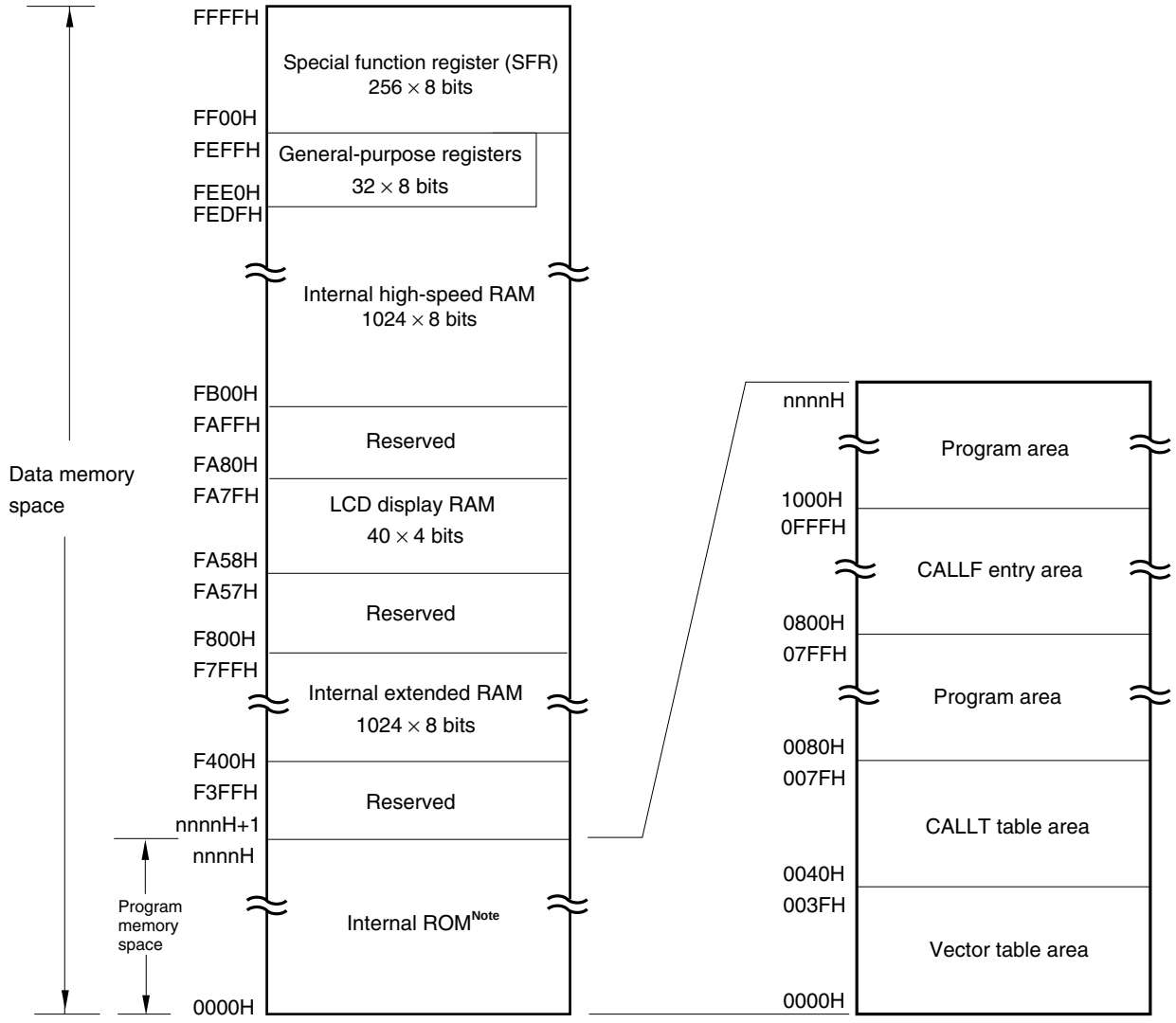
Figure 3-1. Pin Input/Output Circuits (2/2)



4. MEMORY SPACE

The memory map of μPD780306 and 780308 is shown in Figure 4-1.

Figure 4-1. Memory Map



Note The capacity of Internal ROM differs according to product. (refer to the following table.)

Product Name	Last Address of Internal ROM nnnnH
μPD780306	BFFFH
μPD780308	EFFFH

5. PERIPHERAL HARDWARE FUNCTION FEATURE

5.1 PORT

There are two kinds of I/O port.

- CMOS input (P00, P07) : 2
- CMOS input/output (P01 to P05, Port 1 to 3, 7 to 11) : 55

Total : 57

Table 5-1. Functions of Ports

Name	Pin Name	Function
Port 0	P00, P07	Dedicated input port
	P01 to P05	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software.
Port 1	P10 to P17	Input/output port. Input/output specifialbe bit-wise. When used as input port, on-chip pull-up resistor can be used by software.
Port 2	P25 to P27	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software.
Port 3	P30 to P37	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software.
Port 7	P70 to P72	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software.
Port 8	P80 to P87	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software. Input/output port/segment signal output function specifiable in 2-bit units by LCD display control register (LCDC).
Port 9	P90 to P97	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software. Input/output port/segment signal output function specifiable in 2-bit units by LCD display control register (LCDC).
Port 10	P100 to P103	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software. Direct LED drive capability.
Port 11	P110 to P117	Input/output port. Input/output specifiable bit-wise. When used as input port, on-chip pull-up resistor can be used by software. Test input flag (KRIF) is set to 1 by falling edge detection.

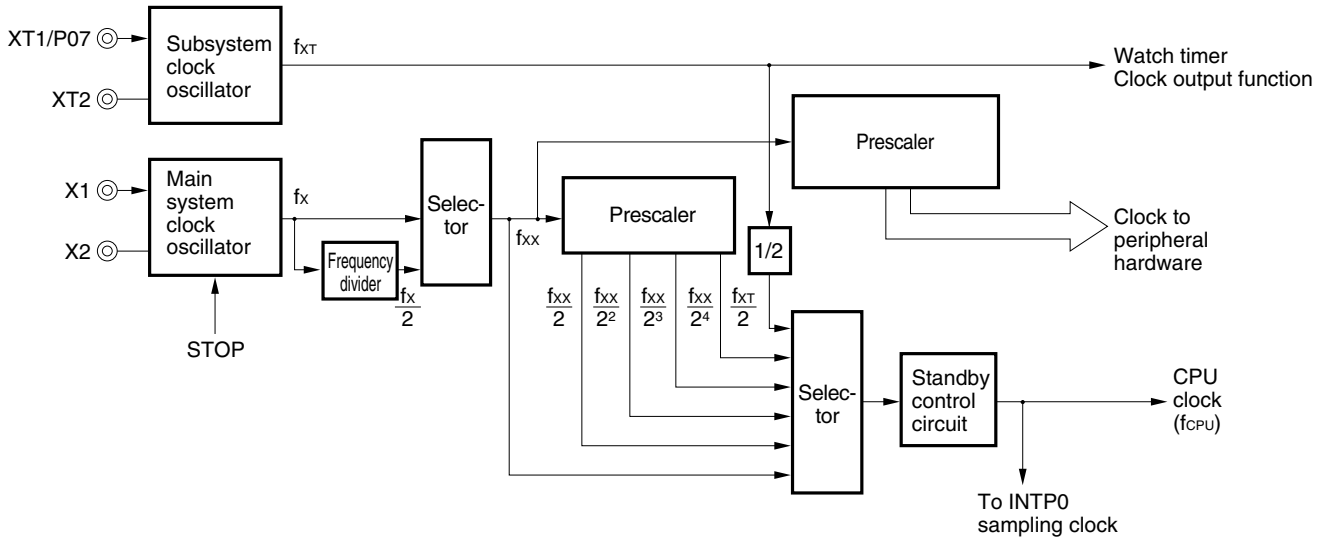
5.2 CLOCK GENERATOR

There are two kinds of clocks, main system clock and subsystem clock.

The minimum instruction execution time can also be changed.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (main system clock: in 5.0 MHz operation)
- 122 μs (subsystem clock: in 32.768 kHz operation)

Figure 5-1. Clock Generator Block Diagram



5.3 TIMER/EVENT COUNTER

Five timer/event counter channels are incorporated.

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2. Operation of Timer/Event Counter

		16-bit Timer/ Event Counter	8-bit Timer/ Event Counter	Watch Timer	Watchdog Timer
Operating mode	Interval timer	1 channel	2 channels	1 channel	1 channel
	External event counter	1 channel	2 channels	–	–
Function	Timer output	1 output	2 outputs	–	–
	PWM output	1 output	–	–	–
	Pulse width measurement	2 inputs	–	–	–
	Square wave output	1 output	2 outputs	–	–
	One-shot pulse output	1 output	–	–	–
	Interrupt request	2	2	1	1
	Test input	–	–	1 input	–

Figure 5-2. 16-Bit Timer/Event Counter Block Diagram

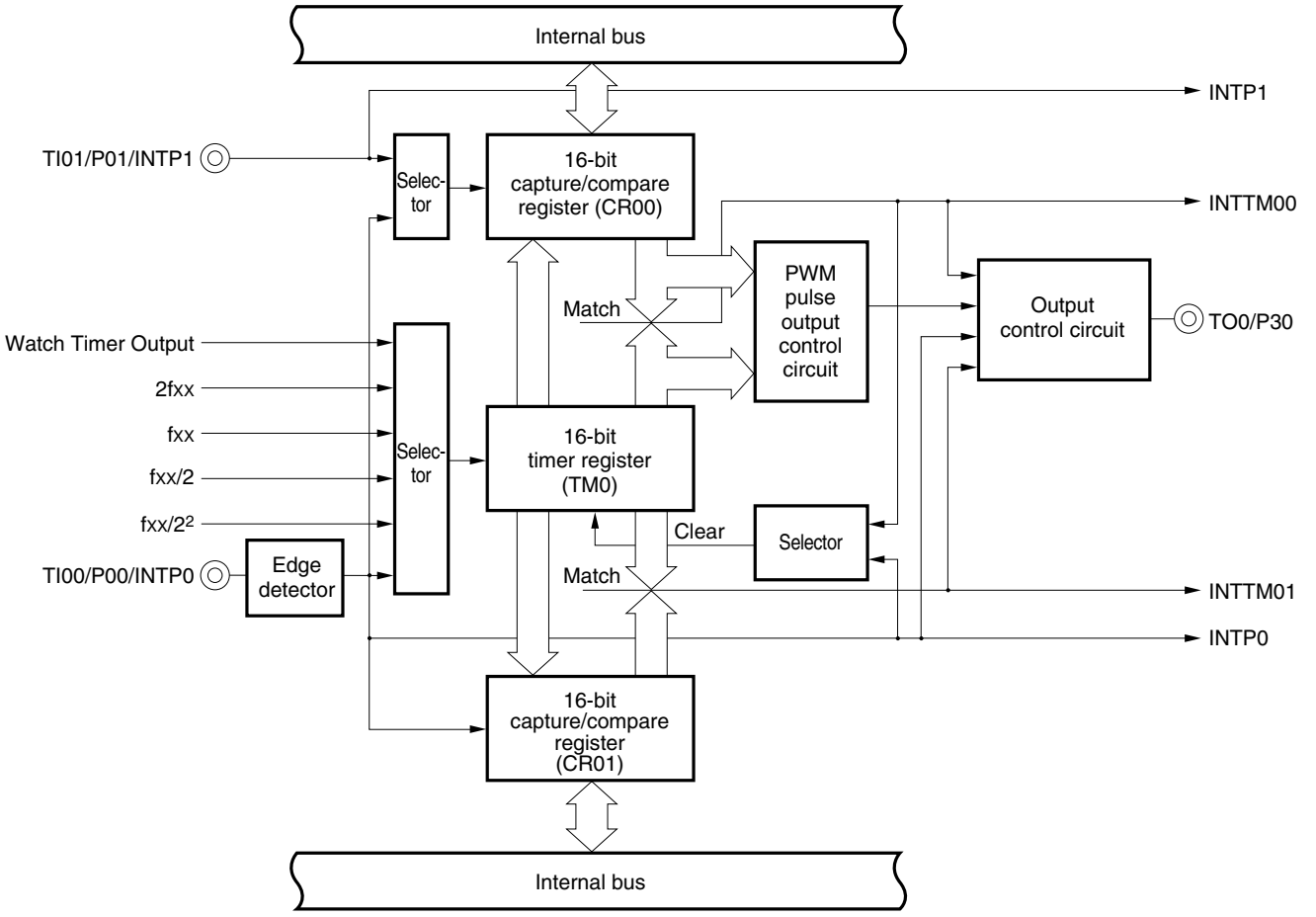


Figure 5-3. 8-Bit Timer/Event Counter Block Diagram

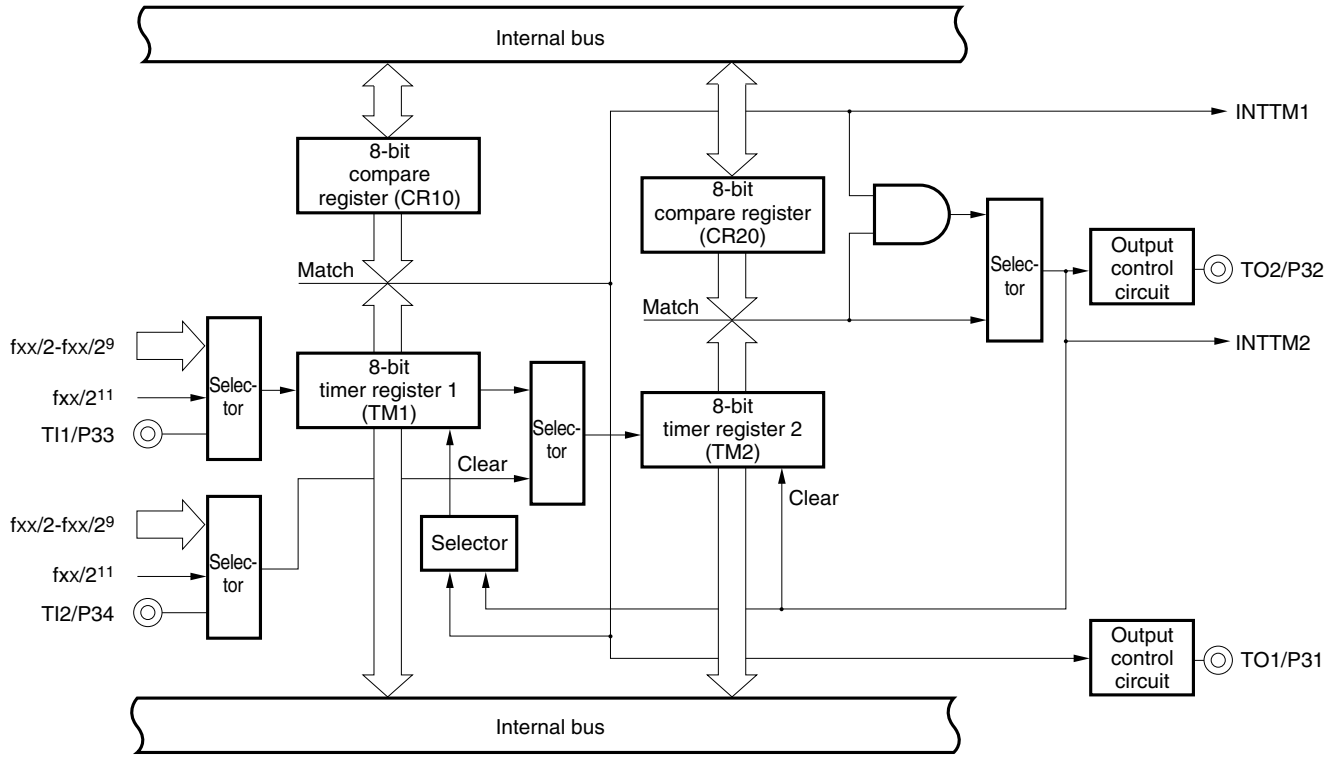


Figure 5-4. Watch Timer Block Diagram

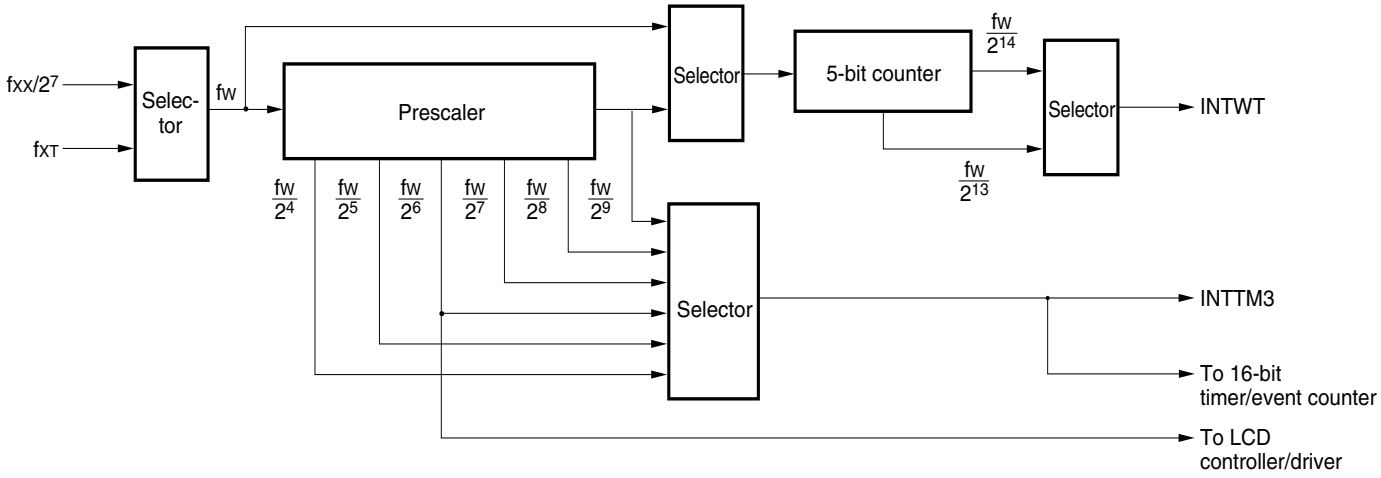
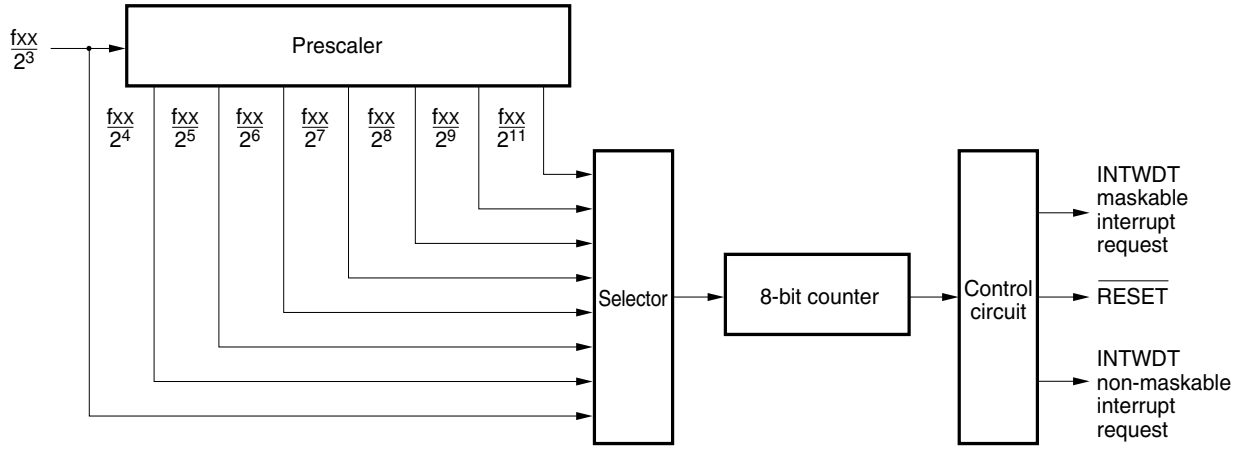


Figure 5-5. Watchdog Timer Block Diagram

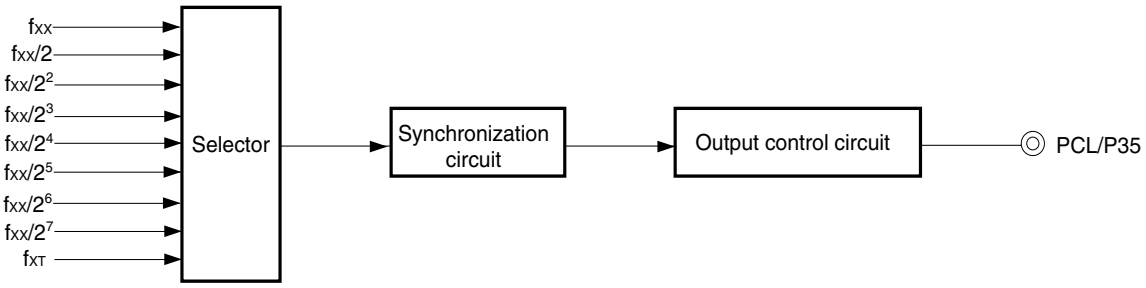


5.4 CLOCK OUTPUT CONTROL CIRCUIT

Clocks of the following frequency can be output as clock outputs.

- 19.5 kHz/39.1kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz/2.5 MHz/5.0 MHz (main system clock: in 5.0 MHz operation)
- 32.768 kHz (subsystem clock: in 32.768 kHz operation)

Figure 5-6. Clock Output Control Circuit Block Diagram

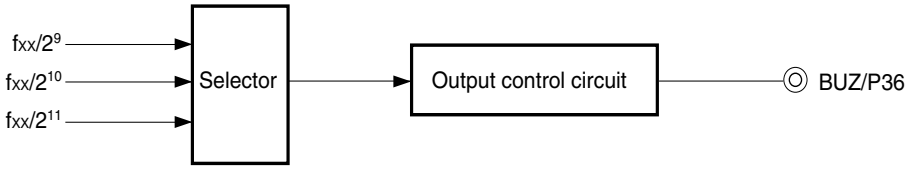


5.5 BUZZER OUTPUT CONTROL CIRCUIT

Clocks of the following frequency can be output as buzzer outputs.

- 1.2 kHz/2.4 kHz/4.9 kHz/9.8 kHz (main system clock : in 5.0 MHz operation)

Figure 5-7. Buzzer Output Control Circuit Block Diagram



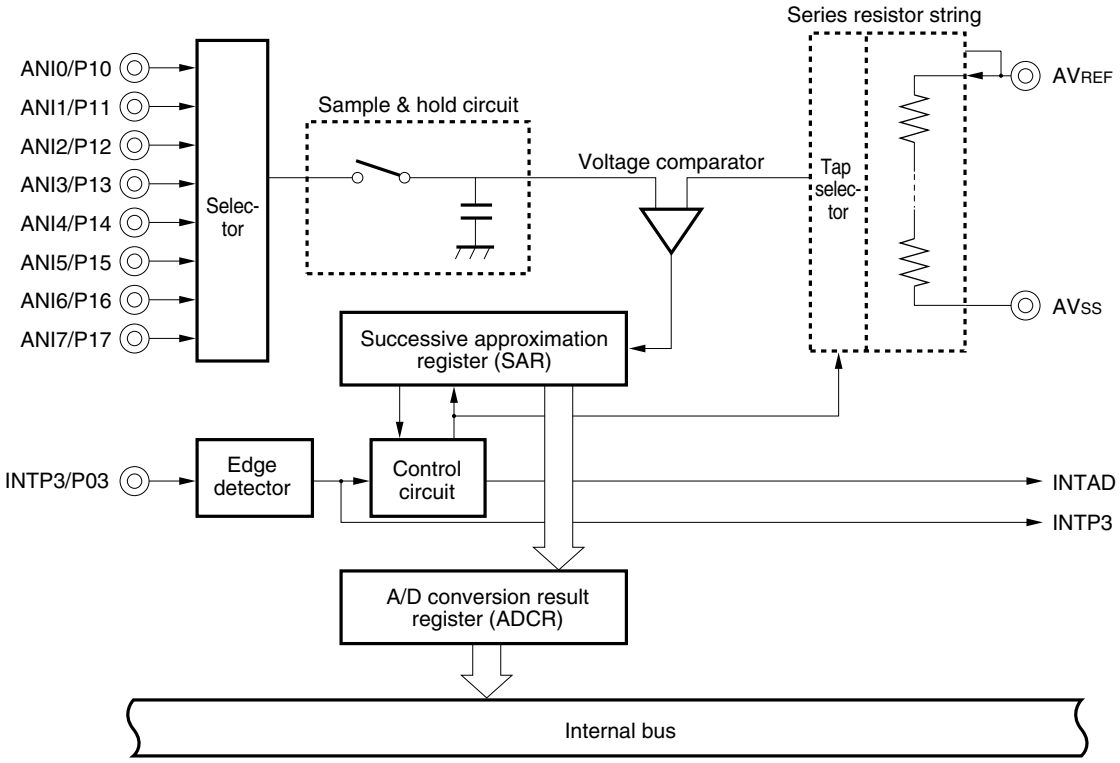
5.6 A/D CONVERTER

Eight 8-bit resolution A/D converter channels are incorporated.

The following two types of start-up method are available.

- Hardware start
- Software start

Figure 5-8. A/D Converter Block Diagram



5.7 SERIAL INTERFACE

Three clocked serial interface channels are incorporated.

- Serial interface channel 0
- Serial interface channel 2
- Serial interface channel 3

Table 5-3. Serial Interface Channel Block Diagram

Function	Serial Interface Channel 0	Serial Interface Channel 2	Serial Interface Channel 3
3-wire serial I/O mode	○ (MSB/LSB-first switchable)	○ (MSB/LSB-first switchable)	○ (MSB/LSB-first switchable)
SBI (serial bus interface) mode	○ (MSB-first)	—	—
2-wire serial I/O mode	○ (MSB-first)	—	—
Asynchronous serial interface (UART) mode	—	○ (With dedicated baud rate generator, data I/O pin switch function)	—

Figure 5-9. Serial Interface Channel 0 Block Diagram

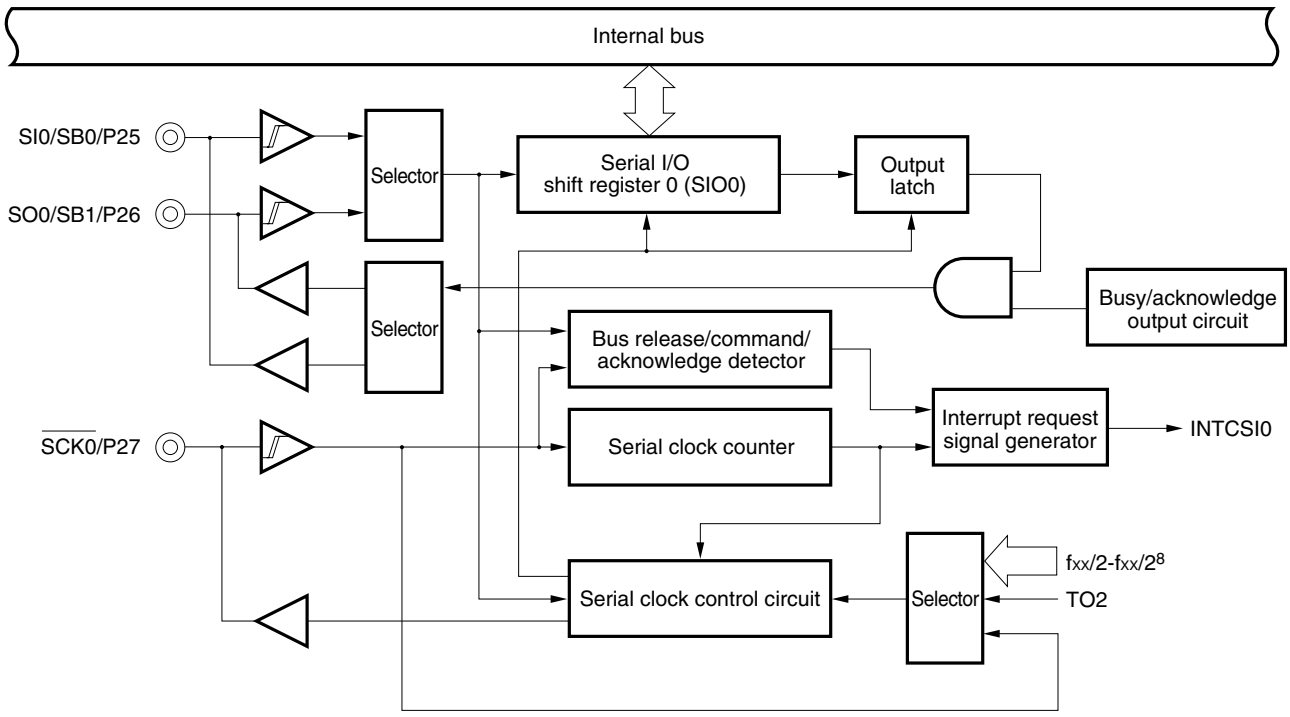


Figure 5-10. Serial Interface Channel 2 Block Diagram

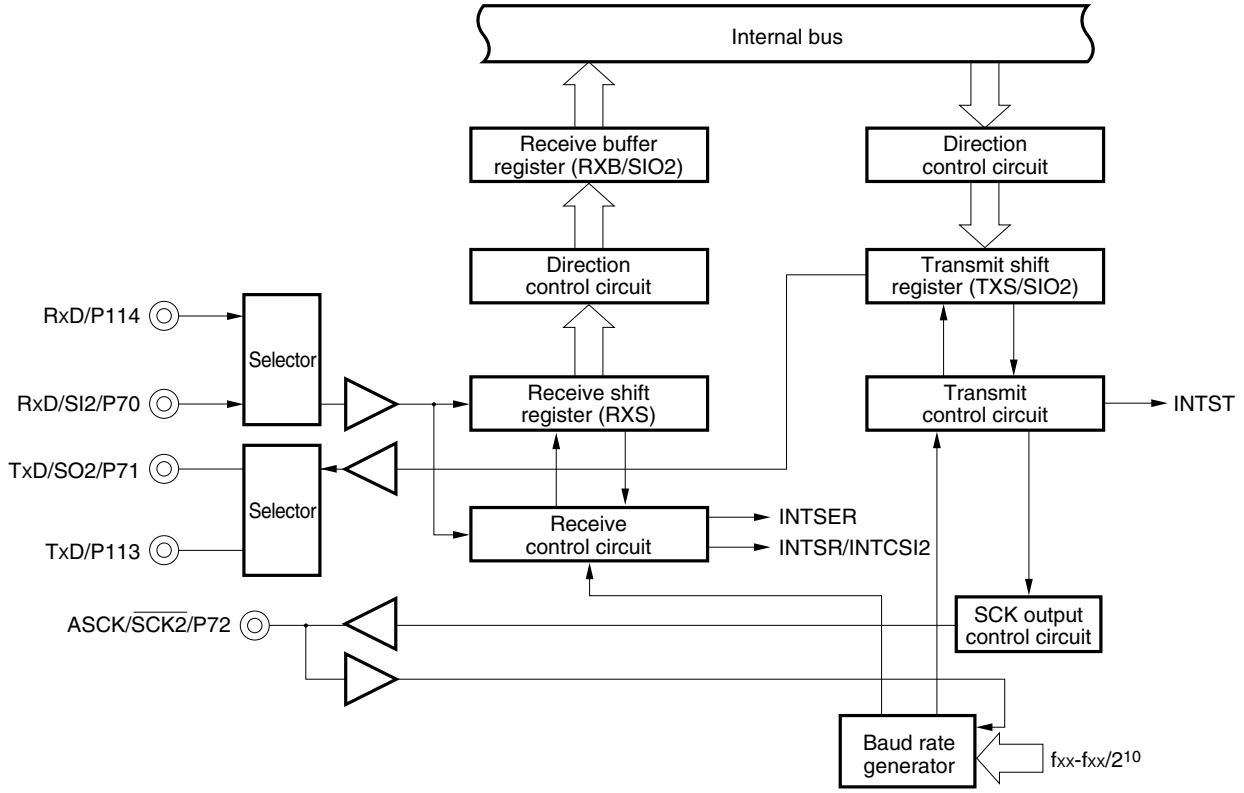
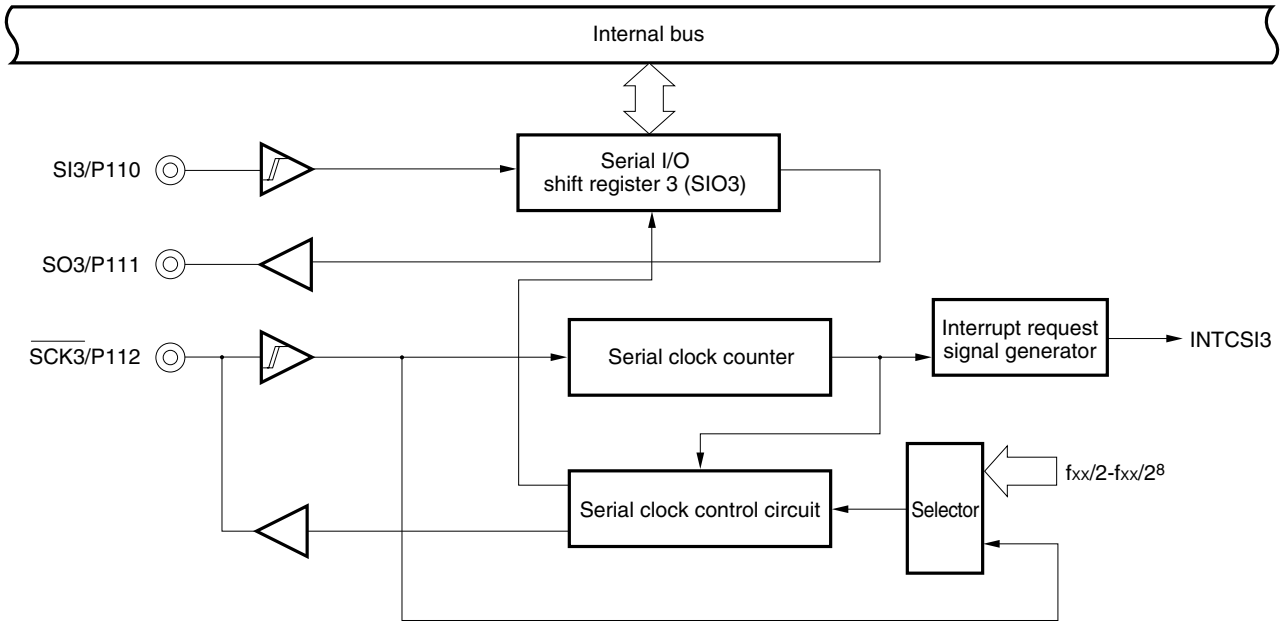


Figure 5-11. Serial Interface Channel 3 Block Diagram



5.8 LCD CONTROLLER/DRIVER

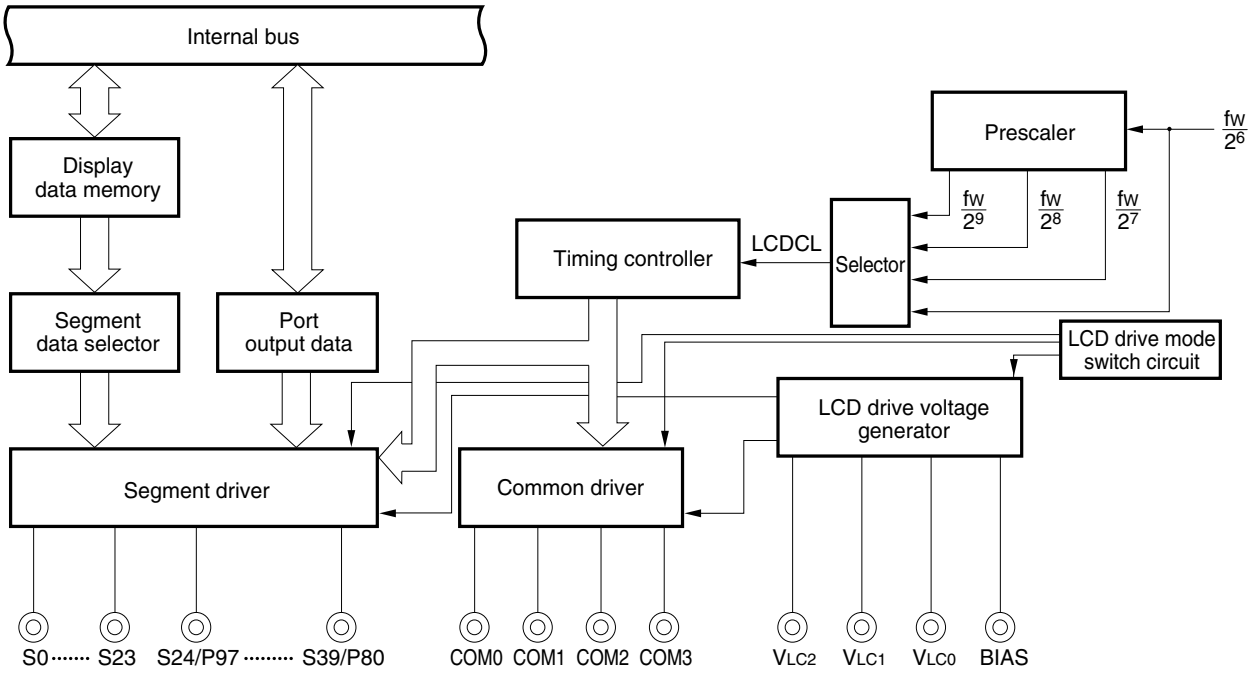
An LCD controller/driver with the following functions is incorporated.

- Selection of 5 types of display mode
- 16 of the segment signal of outputs can be switched to input/output ports in units of 2. (P80/S39 to P87/S32, P90/S31 to P97/S24)

Table 5-4. Display Mode Types and Maximum Number of Display Pixels

Bias Method	Time Division	Common Signal Used	Maximum Number of Display Pixels
——	Static	COM0 (COM1 to COM3)	40 (40 segments × 1 common)
1/2	2	COM0, COM1	80 (40 segments × 2 commons)
	3	COM0 to COM2	120 (40 segments × 3 commons)
1/3	3	COM0 to COM2	
	4	COM0 to COM3	160 (40 segments × 4 commons)

Figure 5-12. LCD Controller/Driver Block Diagram



6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

6.1 INTERRUPT FUNCTIONS

There are twenty-one of interrupt sources of three different kinds, as shown below.

- Non-maskable : 1
- Maskable : 19
- Software : 1

Table 6-1. Interrupt Source List

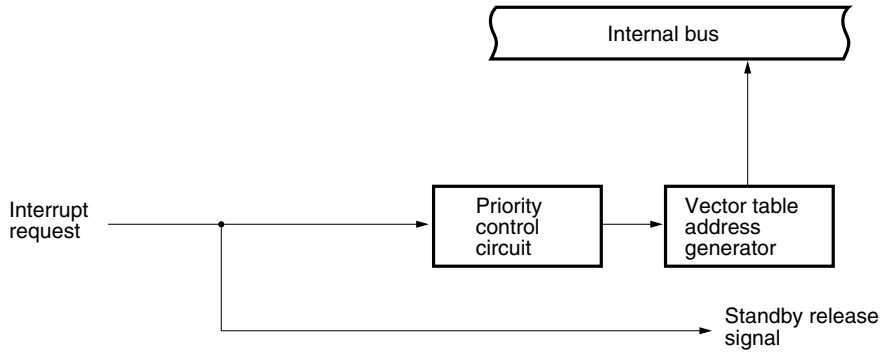
Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2
		Name	Trigger			
Non-maskable	——	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	(D)
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTP4			000EH	
	6	INTP5			0010H	
	7	INTCSI0	Serial interface channel 0 transfer termination	Internal	0014H	(B)
	8	INTSER	Serial interface channel 2 UART reception error generation		0018H	
	9	INTSR	Serial interface channel 2 UART reception termination		001AH	
		INTCSI2	Serial interface channel 2 3-wire transfer termination			
	10	INTST	Serial interface channel 2 UART transmission termination		001CH	
	11	INTTM3	Reference time interval signal from watch timer		001EH	
	12	INTTM00	16-bit timer register and capture/compare register (CR00) match signal generation		0020H	
	13	INTTM01	16-bit timer register and capture/compare register (CR01) match signal generation		0022H	
	14	INTTM1	8-bit timer/event counter 1 match signal generation		0024H	
	15	INTTM2	8-bit timer/event counter 2 match signal generation		0026H	
	16	INTAD	A/D converter conversion termination		0028H	
	17	INTCSI3	Serial interface channel 3 transfer termination		002AH	
Software	——	BRK	BRK instruction execution	——	003EH	(E)

Notes 1. Default priority is a priority order when more than one maskable interrupt request is generated simultaneously. 0 is the highest and 17 the lowest.

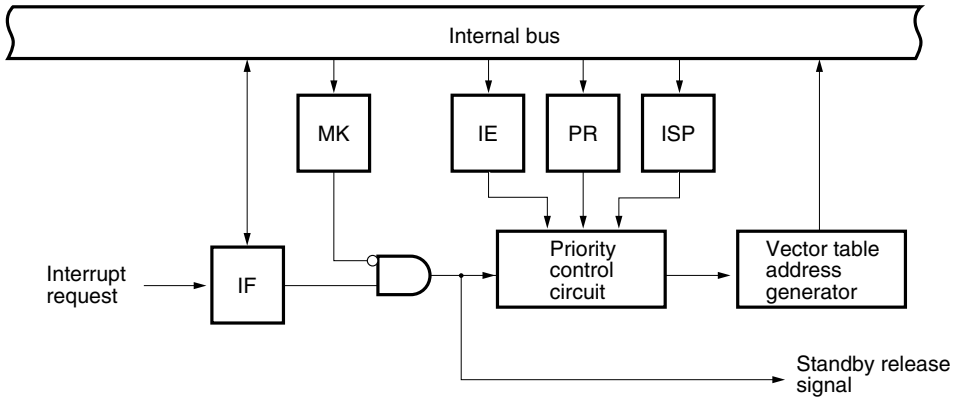
2. Basic configuration types (A) to (E) correspond to those shown on the next page.

Figure 6-1. Basic Configuration of Interrupt Functions (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0)

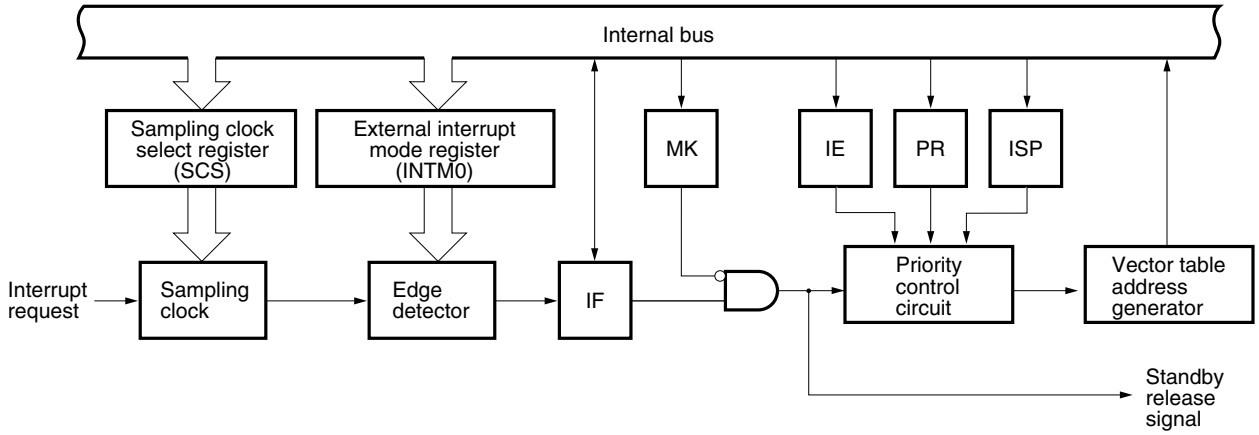
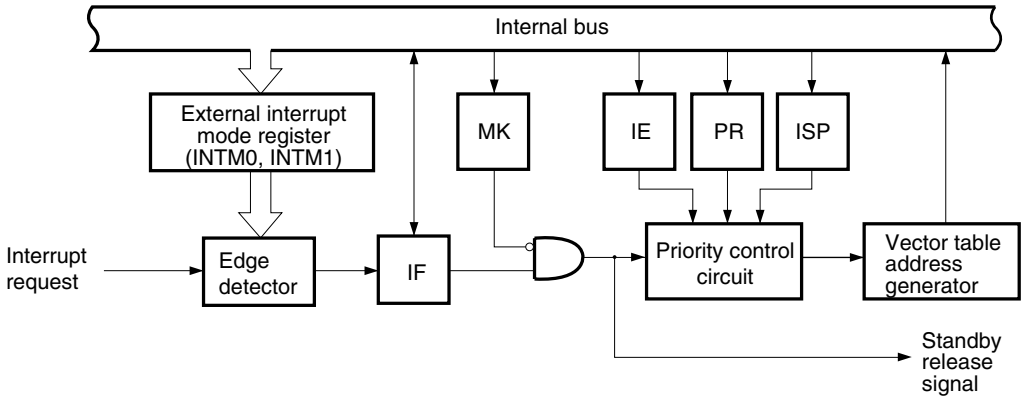
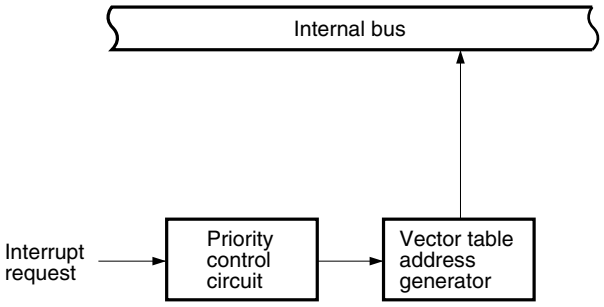


Figure 6-1. Basic Configuration of Interrupt Functions (2/2)

(D) External maskable interrupt (except INTP0)



(E) Software interrupt



IF : Interrupt request flag
IE : Interrupt enable flag
ISP : In-service priority flag
MK : Interrupt mask flag
PR : Priority specification flag

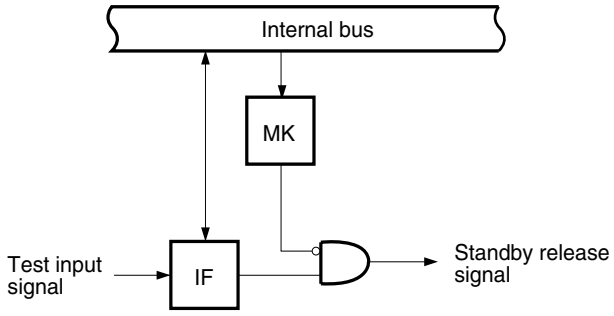
6.2 TEST FUNCTIONS

There are two test functions as shown in Table 6-2.

Table 6-2. Test Input Source List

Test Input Source		Internal/External
Name	Trigger	
INTWT	Watch timer overflow	Internal
INTPT11	Port 11 falling edge detection	External

Figure 6-2. Basic Configuration of Test Function



IF : Test input flag

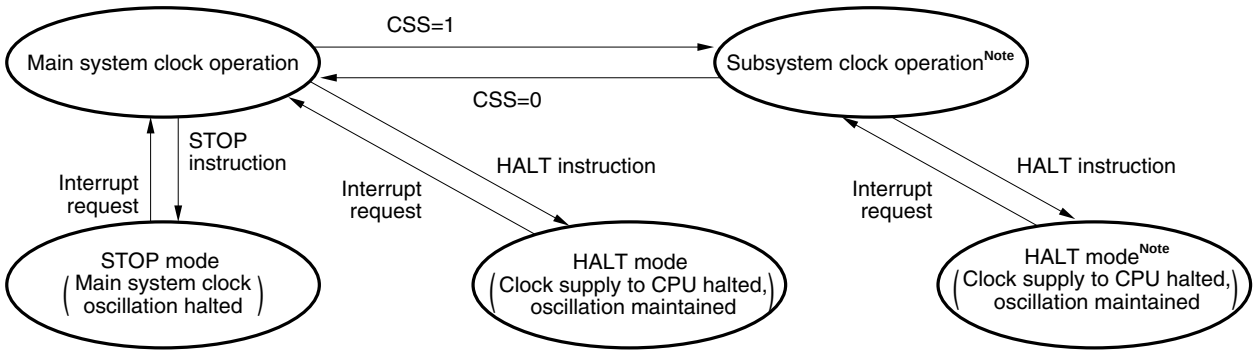
MK : Test mask flag

7. STANDBY FUNCTION

The standby function is a function to reduce the current consumption and there are the following two kinds of standby functions.

- HALT mode : Halts CPU operating clock and can reduce average current consumption by the intermittent operation along with the normal operation.
- STOP mode : Halts main system clock oscillation. Halts all operations with the main system clock and sets ultra-low current consumption state with subsystem clock only.

Figure 7-1. Standby Function



Note Halting the main system clock enables the current consumption to be reduced.
When the CPU is operated by the subsystem clock, the main system clock should be halted by setting the bit 7 (MCC) of the processor clock control register (PCC). The STOP instruction is not available.

Caution When the main system clock is stopped and the system is operated by the subsystem clock, the main system clock should be returned to after securing the oscillation stabilization time by a program.

8. RESET FUNCTION

There are the following two kinds of resetting methods.

- External reset by $\overline{\text{RESET}}$ pin.
- Internal reset by watchdog timer hung-up time detection.

9. INSTRUCTION SET

(1) 8-bit instruction

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

2nd Operand / 1st Operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL+B] [HL+C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL+byte] [HL+B] [HL+C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instruction

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

1st Operand \ 2nd Operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL

(3) Bit manipulation instruction

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

1st Operand \ 2nd Operand	A.bit	sfr.bit	saddr.bit	PSW.bits	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instruction/branch instruction

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

2nd Operand / 1st Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC, BZ, BNZ
Compound Instruction					BT, BF, BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

10. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter	Symbol	Test Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
	AV_{REF}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_I			–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10-P17	Analog input pin	AV_{SS} – 0.3 to AV_{REF} + 0.3	V
Output current, high	I_{OH}	1 pin		–10	V
		Total for P01-P05, P10-P17, P25-P27, P70-P72, P110-P117		–15	mA
		Total for P30-P37, P80-P87, P90-P97, P100-P103		–15	mA
Output current, low	I_{OL}	1 pin	Peak value	30	mA
			r.m.s. value	15[Note]	mA
		Total for P01-P05, P10-P17, P110-P117	Peak value	60	mA
			r.m.s. value	40[Note]	mA
		Total for P30-P37, P100-P103	Peak value	140	mA
			r.m.s. value	100[Note]	mA
		Total for P25-P27, P70-P72, P80-P87, P90-P97	Peak value	50	mA
			r.m.s. value	20[Note]	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note The r.m.s. value should be calculated as follows: [r.m.s. value] = [Peak value] × $\sqrt{\text{Duty}}$

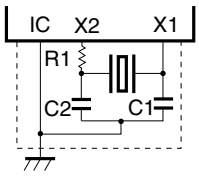
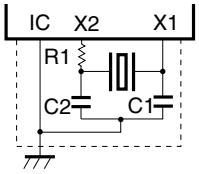
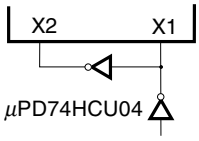
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

CAPACITANCE (T_A= 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz unmeasured pins returned to 0 V.			15	pF
Output capacitance	C_{OUT}				15	pF
I/O capacitance	C_{IO}				15	pF

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.0[Note 4] to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (f_X)[Note 1]	V_{DD} = Oscillator voltage range	1		5	MHz
		Oscillation stabilization time[Note 2]	After V_{DD} reaches oscillator voltage range MIN.			4	ms
Crystal resonator		Oscillator frequency (f_X)[Note 1]	V_{DD} = Oscillator voltage range	1		5	MHz
		Oscillation stabilization time[Note 2]	V_{DD} = 4.5 to 5.5 V[Note 3]			10	ms
			Note 3			30	
External clock		X1 input frequency (f_X)[Note 1]		1.0		5.0	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		85		500	ns

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after reset or STOP mode release.

3. After V_{DD} reaches the minimum oscillator voltage range.

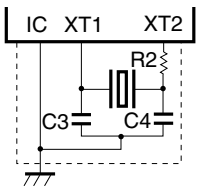
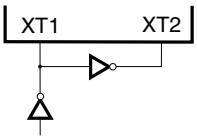
4. Actually, oscillation start voltage or over, and V_{DD} = 2.0 or over (For an external clock, V_{DD} = 2.0 or over is OK).

Cautions 1. When using the main system clock oscillator, wiring in the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS1}.**
- **Do not ground it to the ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. If the main system clock oscillator is operated by the subsystem clock when the main system clock is stopped, reswitching to the main system clock should be performed after the stable oscillation time has been obtained by the program.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.0[Note 4] to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillator frequency (f_{XT})[Note 1]	V_{DD} = Oscillator voltage range	32	32.768	35	kHz
		Oscillation stabilization time[Note 2]	V_{DD} = 4.5 to 5.5 V[Note 3]		1.2	2	s
			Note 3			10	
External clock		XT1 input frequency (f_{XT})[Note 1]		32		100	kHz
		XT1 input high-/low-level width (t_{XTH}/t_{XTL})		5		15	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} has reached the minimum oscillation voltage range.

3. After V_{DD} reaches the minimum oscillator voltage range.

4. Actually, oscillation start voltage or over, and V_{DD} = 2.0 or over (For an external clock, V_{DD} = 2.0 or over is OK).

Cautions 1. When using the subsystem clock oscillator, wiring in the area enclosed with the broken line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS1}.**
- **Do not ground it to the ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. The subsystem clock oscillator is designed as a low amplification circuit to provide low consumption current, causing misoperation to noise more frequently than the main system clock oscillator. Special care should therefore be taken to wiring method when the subsystem clock is used.

RECOMMENDED OSCILLATOR CONSTANT

MAIN SYSTEM CLOCK: CERAMIC RESONATOR (T_A = –40 to +85 °C)

Manufacturer	Product Name	Frequency (MHz)	Recommended Circuit Constant			Oscillator Voltage Range	
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)
Matsushita Electronics Components Co., Ltd.	EFOEC2004A5	2.00	Built-in	Built-in	4.7	2.0	5.5
	EFOEC3584A4	3.58	Built-in	Built-in	0	2.0	5.5
	EFOEC4194A4	4.19	Built-in	Built-in	0	2.0	5.5
	EFOEC4914A4	4.91	Built-in	Built-in	0	2.0	5.5
	EFOEC5004A4	5.00	Built-in	Built-in	0	2.0	5.5
TDK Corp.	CCR1000K2	1.00	150	150	0	2.0	5.5
	CCR3.58MC3	3.58	Built-in	Built-in	0	2.0	5.5
	CCR4.19MC3	4.19	Built-in	Built-in	0	2.0	5.5
	CCR4.91MC3	4.91	Built-in	Built-in	0	2.0	5.5
	CCR5.0MC3	5.00	Built-in	Built-in	0	2.0	5.5
Murata Mfg. Co., Ltd.	CSB1000J	1.00	100	100	2.2	2.0	5.5
	CSA2.00MG040	2.00	100	100	0	2.0	5.5
	CST2.00MG040	2.00	Built-in	Built-in	0	2.0	5.5
	CSA3.58MG	3.58	30	30	0	2.0	5.5
	CST3.58MGW	3.58	Built-in	Built-in	0	2.0	5.5
	CSA4.19MG	4.19	30	30	0	2.0	5.5
	CST4.19MGW	4.19	Built-in	Built-in	0	2.0	5.5
	CSA4.91MG	4.91	30	30	0	2.0	5.5
	CST4.91MGW	4.91	Built-in	Built-in	0	2.0	5.5
	CSA5.00MG	5.00	30	30	0	2.0	5.5
	CST5.00MGW	5.00	Built-in	Built-in	0	2.0	5.5

Caution The oscillator constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency in the application circuit. For this, it is necessary to directly contact the manufacturer of the resonator being used.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 2.0 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10-P17, P30-P32, P35-P37, P80-P87, P90-P97, P100-P103	V_{DD} = 2.7 to 5.5 V	0.7 V_{DD}		V_{DD}	V
				0.8 V_{DD}		V_{DD}	V
	V_{IH2}	P00-P05, P25-P27, P33, P34, P70-P72, P110-P117, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0.8 V_{DD}		V_{DD}	V
				0.85 V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2	V_{DD} = 2.7 to 5.5 V	V_{DD}–0.5		V_{DD}	V
				V_{DD}–0.2		V_{DD}	V
	V_{IH4}	XT1/P07, XT2	4.5 ≤ V_{DD} ≤ 5.5 V	0.8 V_{DD}		V_{DD}	V
			2.7 ≤ V_{DD} < 4.5 V	0.9 V_{DD}		V_{DD}	V
			2.0 ≤ V_{DD} < 2.7 V[Note]	0.9 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10-P17, P30-P32, P35-P37, P80-P87, P90-P97, P100-P103	V_{DD} = 2.7 to 5.5 V	0		0.3 V_{DD}	V
				0		0.2 V_{DD}	V
	V_{IL2}	P00-P05, P25-P27, P33, P34, P70-P72, P110-P117, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0		0.2 V_{DD}	V
				0		0.15 V_{DD}	V
	V_{IL3}	X1, X2	V_{DD} = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
	V_{IL4}	XT1/P07, XT2	4.5 ≤ V_{DD} ≤ 5.5 V	0		0.2 V_{DD}	V
			2.7 ≤ V_{DD} < 4.5 V	0		0.1 V_{DD}	V
			2.0 ≤ V_{DD} < 2.7 V[Note]	0		0.1 V_{DD}	V
Output voltage, high	V_{OH}	V_{DD} = 4.5 to 5.5 V I_{OH} = –1 mA		V_{DD}–1.0		V_{DD}	V
		I_{OH} = –100 μA		V_{DD}–0.5		V_{DD}	V
Output voltage, low	V_{OL1}	P100-P103	V_{DD} = 4.5 to 5.5 V, I_{OL} = 15 mA		0.6	2.0	V
		P01-P05, P10-P17, P25-P27, P30-P37, P70-P72, P80-P87, P90-P97, P110-P117	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V_{DD} = 4.5 to 5.5 V, open-drain, pulled up (R = 1 kΩ)			0.2 V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V

Note When used as P07, the inverse phase of P07 should be input to XT2 using an inverter.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as the those of port pins.

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.0 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00-P05, P10-P17, P25-P27, P30-P37, P70-P72, P80-P87, P90-P97, P100-P103, P110-P117			3	μA
	I_{LIH2}		X1, X2, XT1/P07, XT2			20	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00-P05, P10-P17, P25-P27, P30-P37, P70-P72, P80-P87, P90-P97, P100-P103, P110-P117			–3	μA
	I_{LIH2}		X1, X2, XT1/P07, XT2			–20	μA
Output leakage current, high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistor	R	V_{IN} = 0 V	P01-P05, P10-P17, P25-P27, P30-P37, P70-P72, P80-P87, P90-P97, P100-P103, P110-P117	15	45	90	kΩ
Supply current[Note 1]	I_{DD1}	5.00 MHz, Crystal oscillation (f_{XX} = 2.5 MHz)[Note 2] operating mode	V_{DD} = 5.0 V ± 10%[Note 5]		4	12	mA
			V_{DD} = 3.0 V ± 10%[Note 6]		0.6	1.8	mA
			V_{DD} = 2.2 V ± 10%[Note 6]		0.35	1.05	mA
		5.00 MHz, Crystal oscillation (f_{XX} = 5.0 MHz)[Note 3] operating mode	V_{DD} = 5.0 V ± 10%[Note 5]		6.5	19.5	mA
			V_{DD} = 3.0 V ± 10%[Note 6]		0.8	2.4	mA
	I_{DD2}	5.00 MHz, Crystal oscillation (f_{XX} = 2.5 MHz)[Note 2] HALT mode	V_{DD} = 5.0 V ± 10%		1.4	4.2	mA
			V_{DD} = 3.0 V ± 10%		500	1500	μA
			V_{DD} = 2.2 V ± 10%		280	840	μA
		5.00 MHz, Crystal oscillation (f_{XX} = 5.0 MHz)[Note 3] HALT mode	V_{DD} = 5.0 V ± 10%		1.6	4.8	mA
			V_{DD} = 3.0 V ± 10%		650	1950	μA
	I_{DD3}	32.768 kHz, Crystal oscillation operating mode[Note 4]	V_{DD} = 5.0 V ± 10%		60	120	μA
			V_{DD} = 3.0 V ± 10%		32	64	μA
			V_{DD} = 2.2 V ± 10%		24	48	μA
	I_{DD4}	32.768 kHz, Crystal oscillation HALT mode[Note 4]	V_{DD} = 5.0 V ± 10%		25	55	μA
			V_{DD} = 3.0 V ± 10%		5	15	μA
			V_{DD} = 2.2 V ± 10%		2.5	12.5	μA
	I_{DD5}	XT1 = V_{DD} STOP mode When feedback resistor is connected	V_{DD} = 5.0 V ± 10%		1	30	μA
			V_{DD} = 3.0 V ± 10%		0.5	10	μA
			V_{DD} = 2.2 V ± 10%		0.3	10	μA
	I_{DD6}	XT1 = V_{DD} STOP mode When feedback resistor is disconnected	V_{DD} = 5.0 V ± 10%		0.1	30	μA
			V_{DD} = 3.0 V ± 10%		0.05	10	μA
			V_{DD} = 2.2 V ± 10%		0.05	10	μA

Notes 1. Current flowing V_{DD} pin. Not including A/D converter, ports, on-chip pull-up resistors or LCD dividing resistors.

2. Main system clock $f_{XX} = f_X/2$ operation (when oscillation mode selection register (OSMS) is set to 00H)

3. Main system clock $f_{XX} = f_X$ operation (when OSMS is set to 01H)

4. When the main system clock is stopped.

5. High-speed mode operation (when processor clock control register (PCC) is set to 00H)

6. Low-speed mode operation (when PCC is set to 04H)

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as the those of port pins.

LCD CONTROLLER/DRIVER CHARACTERISTICS (AT NORMAL OPERATION)

(1) Static Display Mode (T_A = –10 to +85 °C, V_{DD} = 2.0 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}			2.0		V_{DD}	V
LCD dividing resistor	R_{LCD}			60	100	150	kΩ
LCD output voltage deviation[Note] (common)	V_{ODC}	I_O = ±5 μA	$V_{LCD0} = V_{LCD}$	0		±0.2	V
LCD output voltage deviation[Note] (segment)	V_{ODS}	I_O = ±1 μA		0		±0.2	V

Note The voltage deviation is the difference from the output voltage corresponding to the ideal value of the segment and common outputs (V_{LCDn}; n = 0, 1, 2).

(2) 1/3 Bias Method (T_A = –10 to +85 °C, V_{DD} = 2.5 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}			2.5		V_{DD}	V
LCD dividing resistor	R_{LCD}			60	100	150	kΩ
LCD output voltage deviation[Note] (common)	V_{ODC}	I_O = ±5 μA	$V_{LCD0} = V_{LCD}$ $V_{LCD1} = V_{LCD} \times 2/3$ $V_{LCD2} = V_{LCD} \times 1/3$	0		±0.2	V
LCD output voltage deviation[Note] (segment)	V_{ODS}	I_O = ±1 μA		0		±0.2	V

Note The voltage deviation is the difference from the output voltage corresponding to the ideal value of the segment and common outputs (V_{LCDn}; n = 0, 1, 2).

(3) 1/2 Bias Method (T_A = –10 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}			2.7		V_{DD}	V
LCD dividing resistor	R_{LCD}			60	100	150	kΩ
LCD output voltage deviation[Note] (common)	V_{ODC}	I_O = ±5 μA	$V_{LCD0} = V_{LCD}$ $V_{LCD1} = V_{LCD} \times 1/2$ $V_{LCD2} = V_{LCD1}$	0		±0.2	V
LCD output voltage deviation[Note](segment)	V_{ODS}	I_O = ±1 μA		0		±0.2	V

Note The voltage deviation is the difference from the output voltage corresponding to the ideal value of the segment and common outputs (V_{LCDn}; n = 0, 1, 2).

LCD CONTROLLER/DRIVER CHARACTERISTICS (AT LOW-VOLTAGE OPERATION)

(1) Static Display Mode (T_A = –10 to +85 °C, 2.0 V ≤ V_{DD} < 3.4 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}			2.0		V_{DD}	V
LCD dividing resistor	R_{LCD}			60	100	150	kΩ
LCD output voltage deviation[Note] (common)	V_{ODC}	I_O = ±5 μA	V_{LCD0} = V_{LCD}	0		±0.2	V
LCD output voltage deviation[Note] (segment)	V_{ODS}	I_O = ±1 μA		0		±0.2	V

Note The voltage deviation is the difference from the output voltage corresponding to the ideal value of the segment and common outputs (V_{LCDn}; n = 0, 1, 2).

(2) 1/3 Bias Method (T_A = –10 to +85 °C, 2.0 V ≤ V_{DD} < 3.4 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}			2.0		V_{DD}	V
LCD dividing resistor	R_{LCD}			60	100	150	kΩ
LCD output voltage deviation[Note] (common)	V_{ODC}	I_O = ±5 μA	V_{LCD0} = V_{LCD} V_{LCD1} = V_{LCD} × 2/3 V_{LCD2} = V_{LCD} × 1/3	0		±0.2	V
LCD output voltage deviation[Note] (segment)	V_{ODS}	I_O = ±1 μA		0		±0.2	V

Note The voltage deviation is the difference from the output voltage corresponding to the ideal value of the segment and common outputs (V_{LCDn}; n = 0, 1, 2).

(3) 1/2 Bias Method (T_A = –10 to +85 °C, 2.0 V ≤ V_{DD} < 3.4 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}			2.0		V_{DD}	V
LCD dividing resistor	R_{LCD}			60	100	150	kΩ
LCD output voltage deviation[Note] (common)	V_{ODC}	I_O = ±5 μA	V_{LCD0} = V_{LCD} V_{LCD1} = V_{LCD} × 1/2 V_{LCD2} = V_{LCD1}	0		±0.2	V
LCD output voltage deviation[Note] (segment)	V_{ODS}	I_O = ±1 μA		0		±0.2	V

Note The voltage deviation is the difference from the output voltage corresponding to the ideal value of the segment and common outputs (V_{LCDn}; n = 0, 1, 2).

AC CHARACTERISTICS

(1) Basic Operation (T_A = –40 to +85 °C, V_{DD} = 2.0 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating on main system clock (f_{XX} = 2.5 MHz)Note 1	V_{DD} = 2.7 to 5.5 V	0.8		64	μs
				2.0		64	μs
		Operating on main system clock (f_{XX} = 5.0 MHz)Note 2	3.5 ≤ V_{DD} ≤ 5.5 V	0.4		32	μs
			2.7 ≤ V_{DD} < 3.5 V	0.8		32	μs
		Operating on subsystem clock		40Note 3	122	125	μs
TI00 input frequency	f_{TI00}	$f_{TI00} = t_{TIH00} + t_{TIL00}$		0		$1/t_{TI00}$	MHz
TI00 input high/low-level width	t_{TIH00}, t_{TIL00}	3.5 V ≤ V_{DD} ≤ 5.5 V		$2/f_{sam}$+0.1Note 4			μs
		2.7 V ≤ V_{DD} < 3.5 V		$2/f_{sam}$+0.2Note 4			μs
		2.0 V ≤ V_{DD} < 2.7 V		$2/f_{sam}$+0.5Note 4			μs
TI01 input frequency	f_{TI01}	V_{DD} = 2.7 to 5.5 V		0		100	kHz
				0		50	kHz
TI01 input high/low-level width	t_{TIH01}, t_{TIL01}	V_{DD} = 2.7 to 5.5 V		10			μs
				20			μs
TI1, TI2 input frequency	f_{TI1}	V_{DD} = 4.5 to 5.5 V		0		4	MHz
				0		275	kHz
TI1, TI2 input high/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 5.5 V		100			ns
				1.8			μs
Interrupt request input high/low-level width	t_{INTH}, t_{INTH}, t_{INTH}, t_{INTL}	INTP0	3.5 V ≤ V_{DD} ≤ 5.5 V	$2/f_{sam}$+0.1Note 4			μs
			2.7 V ≤ V_{DD} < 3.5 V	$2/f_{sam}$+0.2Note 4			μs
			2.0 V ≤ V_{DD} < 2.7 V	$2/f_{sam}$+0.5Note 4			μs
		INTP1-INTP5, P110-P117	V_{DD} = 2.7 to 5.5 V	10			μs
				20			μs
$\overline{\text{RESET}}$ low level width	t_{RST}	V_{DD} = 2.7 to 5.5 V		10			μs
				20			μs

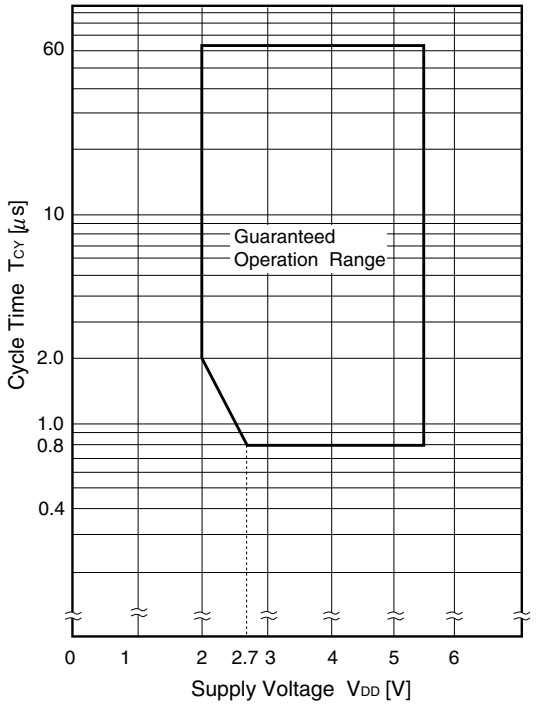
Notes 1. Main system clock f_{XX} = f_X/2 operation (when oscillation mode selection register (OSMS) is set to 00H)

2. Main system clock f_{XX} = f_X operation (when OSMS is set to 01H)

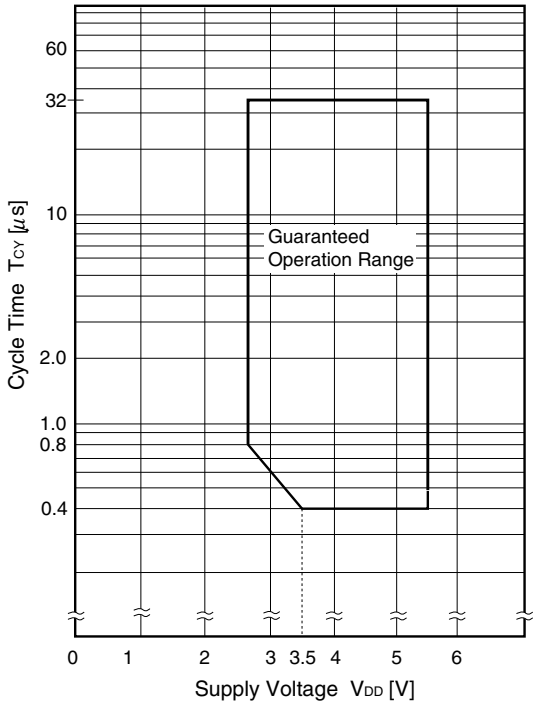
3. This is the value when the external clock is used. The value is 114 μs (min.) when the crystal resonator is used.

4. In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register (SCS), selection of f_{sam} is possible between $f_{XX}/2^N$, f_{XX}/32, f_{XX}/64 and f_{XX}/128 (when N = 0 to 4).

T_{CY} vs V_{DD} (At main system clock $f_{XX} = f_X/2$ operation)



★ **T_{CY} vs V_{DD} (At main system clock $f_{XX} = f_X$ operation)**



(2) Serial Interface (T_A = –40 to +85 °C, V_{DD} = 2.0 to 5.5 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK0}$ high/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 4.5 to 5.5 V	t_{KCY1}/2–50			ns
			t_{KCY1}/2–100			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI1}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of $\overline{SCK0}$, SO0 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$...External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK0}$ high/low-level width	t_{KH2}, t_{KL2}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK2}		100			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI2}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO2}	C = 100 pF[Note]			300	ns
$\overline{SCK0}$ rise, fall time	t_{R2}, t_{F2}				1000	ns

Note C is the load capacitance of SO0 output line.

(iii) SBI mode ($\overline{SCK0}$...Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 4.5 to 5.5 V		t_{KCY3}/2–50			ns
				t_{KCY3}/2–150			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK3}	V_{DD} = 4.5 to 5.5 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI3}			t_{KCY3}/2			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO3}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	0		250	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R and C are the load resistance and load capacitance of the $\overline{SCK0}$, SB0 and SB1 output line.

(iv) SBI mode ($\overline{SCK0}$...External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high/low-level width	t_{KH4}, t_{KL4}	V_{DD} = 4.5 to 5.5 V		400			ns
				1600			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK4}	V_{DD} = 4.5 to 5.5 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI4}			t_{KCY4}/2			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO4}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	0		300	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{SCK0}$ rise, fall time	t_{R4}, t_{F4}					1000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output line.

(v) 2-wire serial I/O mode ($\overline{\text{SCK0}}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 2.7 to 5.5 V	1600			ns
				3200			ns
$\overline{\text{SCK0}}$ high-level width	t_{KH5}		V_{DD} = 2.7 to 5.5 V	$t_{KCY5}/2-160$			ns
				$t_{KCY5}/2-190$			ns
$\overline{\text{SCK0}}$ low-level width	t_{KL5}		V_{DD} = 4.5 to 5.5 V	$t_{KCY5}/2-50$			ns
				$t_{KCY5}/2-100$			ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}$↑)	t_{SIK5}		4.5 V ≤ V_{DD} ≤ 5.5 V	300			ns
			2.7 V ≤ V_{DD} < 4.5 V	350			ns
				400			ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}$↑)	t_{KSI5}			600			ns
SB0, SB1 output delay time from $\overline{\text{SCK0}}$↓	t_{KSO5}					300	ns

Note R and C are the load resistance and load capacitance of the $\overline{\text{SCK0}}$, SB0 and SB1 output line.

(vi) 2-wire serial I/O mode ($\overline{\text{SCK0}}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{KCY6}	V_{DD} = 2.7 to 5.5 V		1600			ns
				3200			ns
$\overline{\text{SCK0}}$ high-level width	t_{KH6}	V_{DD} = 2.7 to 5.5 V		650			ns
				1300			ns
$\overline{\text{SCK0}}$ low-level width	t_{KL6}	V_{DD} = 2.7 to 5.5 V		800			ns
				1600			ns
SB0, SB1 setup time (to $\overline{\text{SCK0}}$↑)	t_{SIK6}			100			ns
SB0, SB1 hold time (from $\overline{\text{SCK0}}$↑)	t_{KSI6}			$t_{KCY6}/2$			ns
SB0, SB1 output delay time from $\overline{\text{SCK0}}$↓	t_{KSO6}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	0		300	ns
				0		500	ns
$\overline{\text{SCK0}}$ rise, fall time	t_{R6}, t_{F6}					1000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output line.

(b) Serial interface channel 2

(i) 3-wire serial I/O mode ($\overline{SCK2}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY7}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK2}$ high/low-level width	t_{KH7}, t_{KL7}	V_{DD} = 4.5 to 5.5 V	t_{KCY7}/2–50			ns
			t_{KCY7}/2–100			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK7}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI7}		400			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of $\overline{SCK2}$, SO2 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK2}$...External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY8}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK2}$ high/low-level width	t_{KH8}, t_{KL8}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK8}		100			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI8}		400			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO8}	C = 100 pF[Note]			300	ns
$\overline{SCK2}$ rise, fall time	t_{R8}, t_{F8}				1000	ns

Note C is the load capacitance of SO2 output line.

(iii) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.5 V ≤ V_{DD} ≤ 5.5 V			78125	bps
		2.7 V ≤ V_{DD} < 4.5 V			39063	bps
					19531	bps

(iv) UART mode (External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY9}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
ASCK high/low-level width	t_{KH9}, t_{KL9}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
Transfer rate		4.5 V ≤ V_{DD} ≤ 5.5 V			39063	bps
		2.7 V ≤ V_{DD} < 4.5 V			19531	bps
					9766	bps
ASCK rise, fall time	t_{R9}, t_{F9}				1000	ns

(c) Serial interface channel 3

(i) 3-wire serial I/O mode ($\overline{SCK3}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY10}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK3}$ high/low-level width	t_{KH10}, t_{KL10}	V_{DD} = 4.5 to 5.5 V	t_{KCY10}/2–50			ns
			t_{KCY10}/2–100			ns
SI3 setup time (to $\overline{SCK3}$↑)	t_{SIK10}	4.5 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI3 hold time (from $\overline{SCK3}$↑)	t_{KSI10}		400			ns
SO3 output delay time from $\overline{SCK3}$↓	t_{KSO10}	C = 100 pF[Note]			300	ns

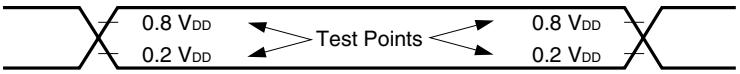
Note C is the load capacitance of $\overline{SCK3}$, SO3 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK3}$...External clock input)

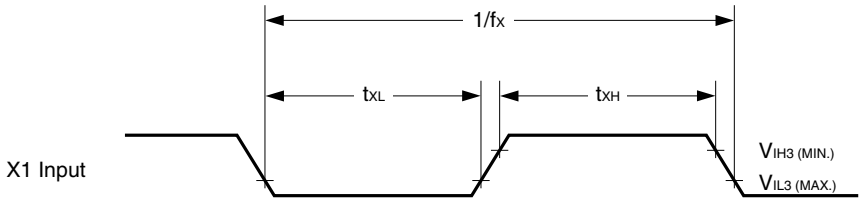
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY11}	4.5 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK3}$ high/low-level width	t_{KH11}, t_{KL11}	4.5 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
SI3 setup time (to $\overline{SCK3}$↑)	t_{SIK11}		100			ns
SI3 hold time (from $\overline{SCK3}$↑)	t_{KSI11}		400			ns
SO3 output delay time from $\overline{SCK3}$↓	t_{KSO11}	C = 100 pF[Note]			300	ns
$\overline{SCK3}$ rise, fall time	t_{R11}, t_{F11}				1000	ns

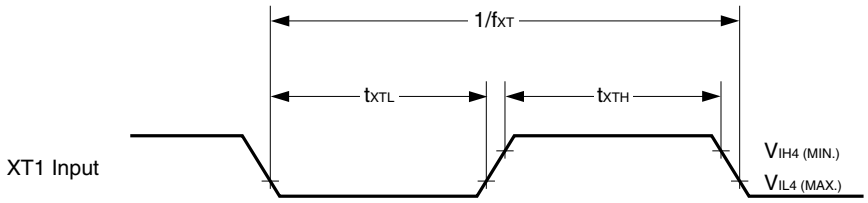
Note C is the load capacitance of SO3 output line.

AC Timing Test Point (Excluding X1, XT1 Input)

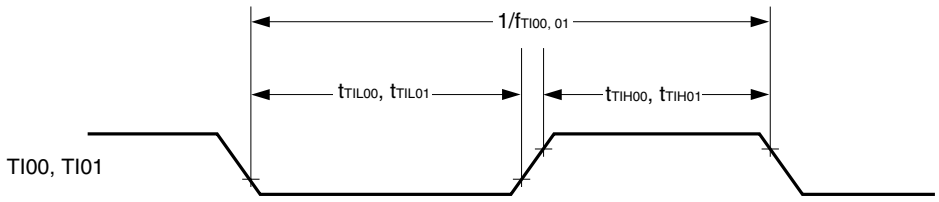


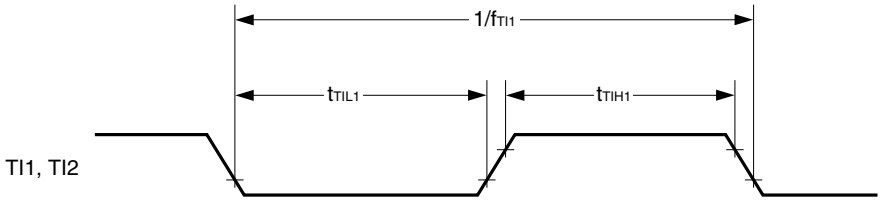
Clock Timing





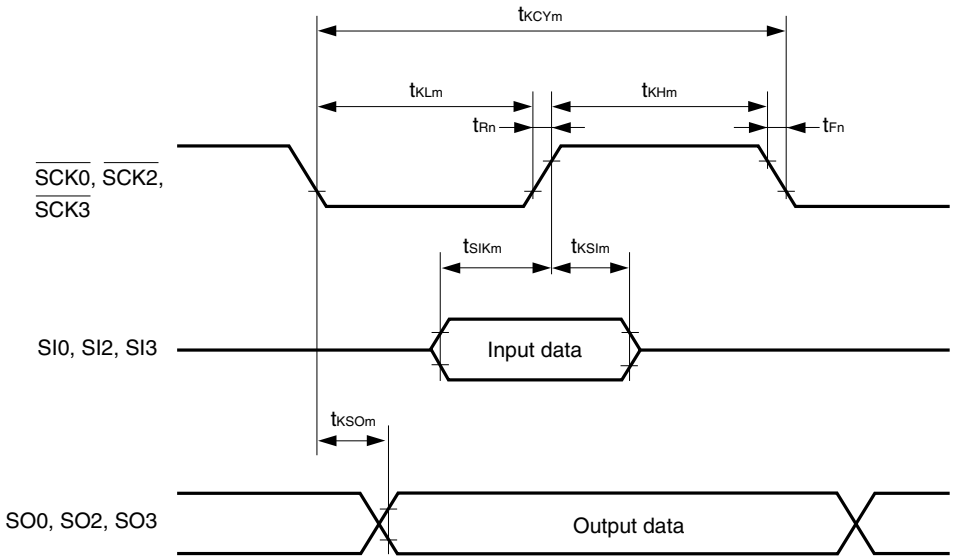
TI Timing





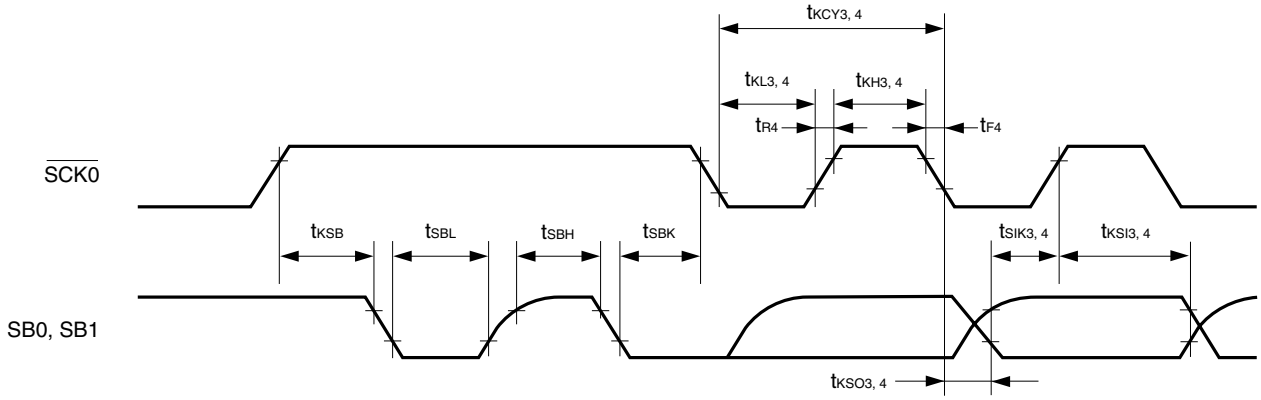
Serial Transfer Timing

3-wire serial I/O mode:

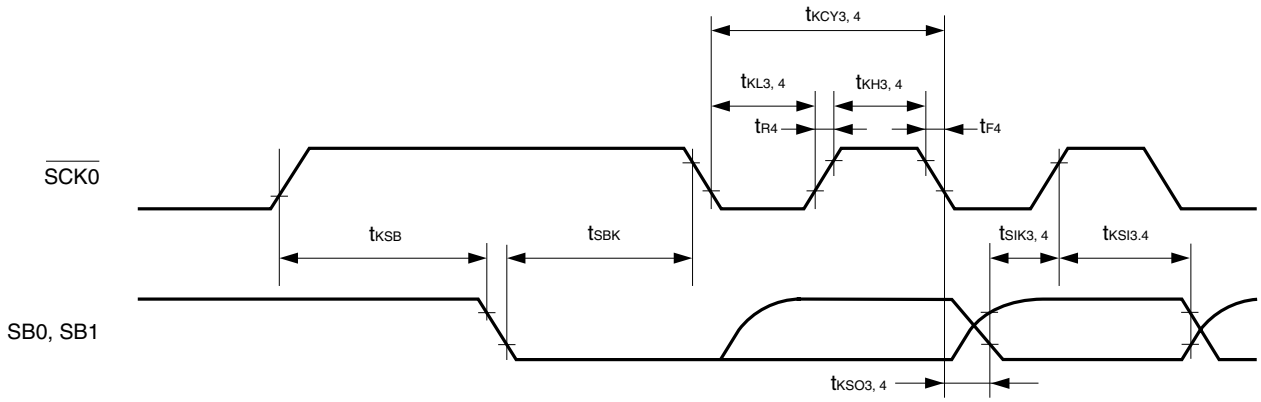


m = 1, 2, 7, 8, 10, 11
n = 2, 8, 11

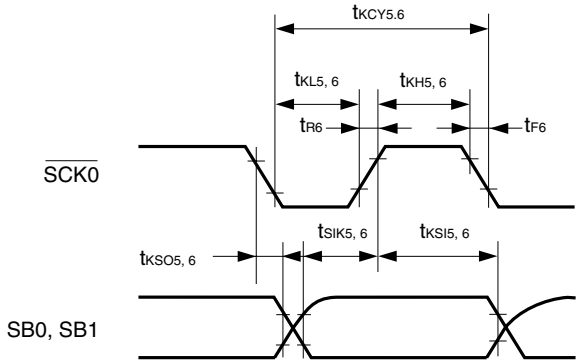
SBI mode (bus release signal transfer):



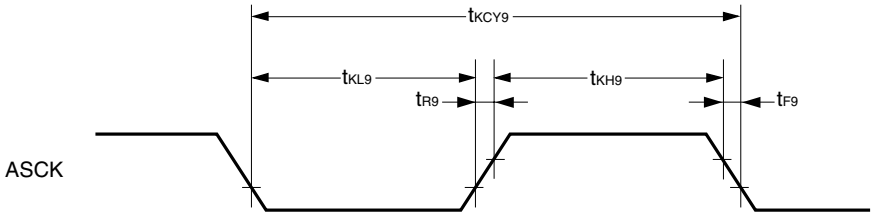
SBI mode (command signal transfer):



2-wire serial I/O mode:



UART mode:



A/D CONVERTER CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note 1]		2.7 V ≤ AV_{REF} ≤ 5.5			±0.6	%
		2.0 V ≤ AV_{REF} < 2.7 V			±1.4	%
Conversion time	t_{CONV}		19.1		200	μs
Sampling time	t_{SAMP}		12/f_{XX}			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		2.0		AV_{DD}	V
AV_{REF}-AV_{SS} resistance	R_{REF}	When not operating A/D conversion	4	14		kΩ
AV_{REF} current	AI_{REF}	When operating A/D conversion[Note 2]		2.5	5.0	mA
		When not operating A/D conversion[Note 3]		0.5	1.5	mA

Notes 1. Quantization error (±1/2 LSB) is not included. This is expressed in proportion to the full-scale value.

2. Indicates current flowing to AV_{REF} pin when the CS bit of the A/D converter mode register (ADM) is 1.

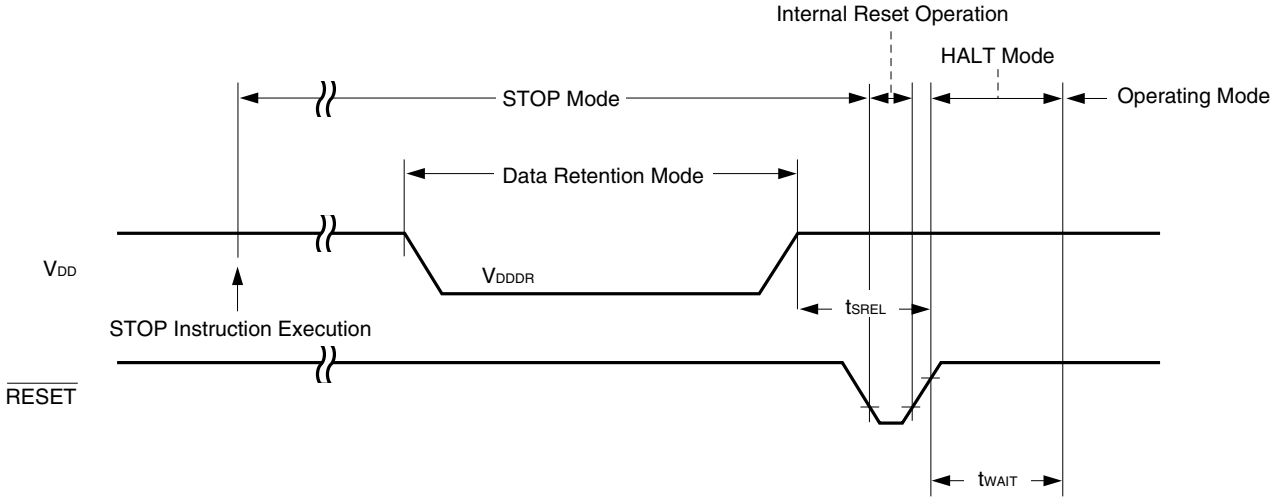
3. Indicates current flowing to AV_{REF} pin when the CS bit of the ADM is 0.

DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (T_A = –40 to +85 °C)

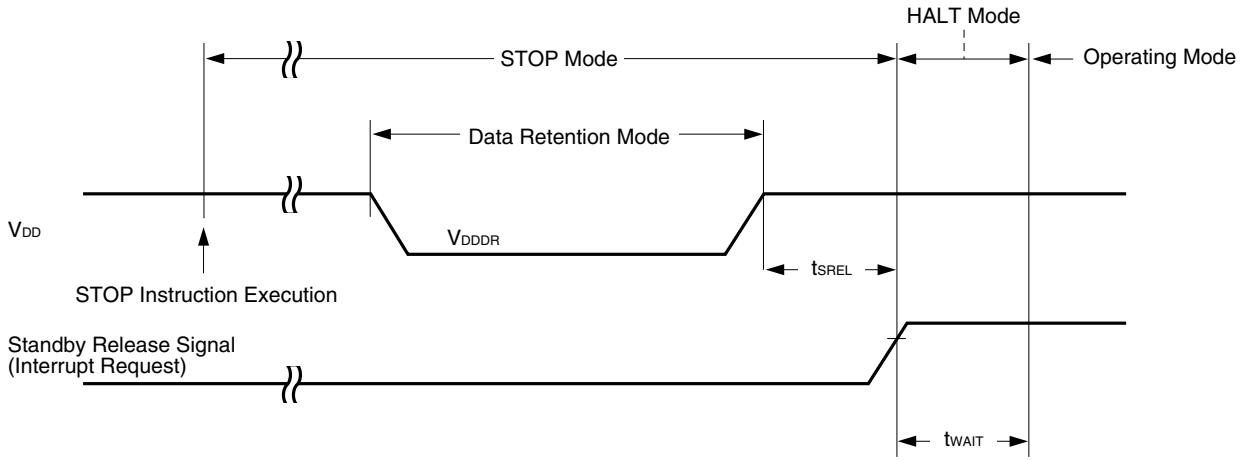
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.6		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 1.6 V Subsystem clock stop and feed-back resistor disconnected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{17}/f_X$		ms
		Release by interrupt		**Note**		ms

Note In combination with bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS), selection of $2^{12}/f_{XX}$ and $2^{14}/f_{XX}$ to $2^{17}/f_{XX}$ is possible.

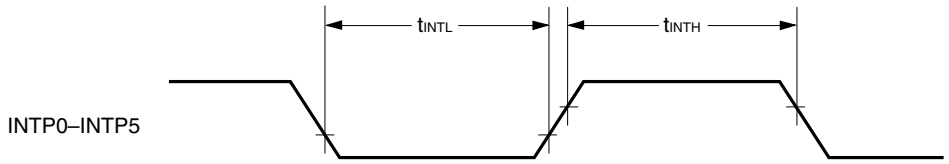
Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



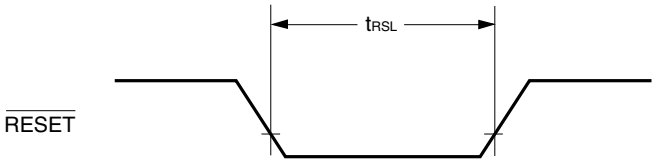
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



Interrupt Request Input Timing

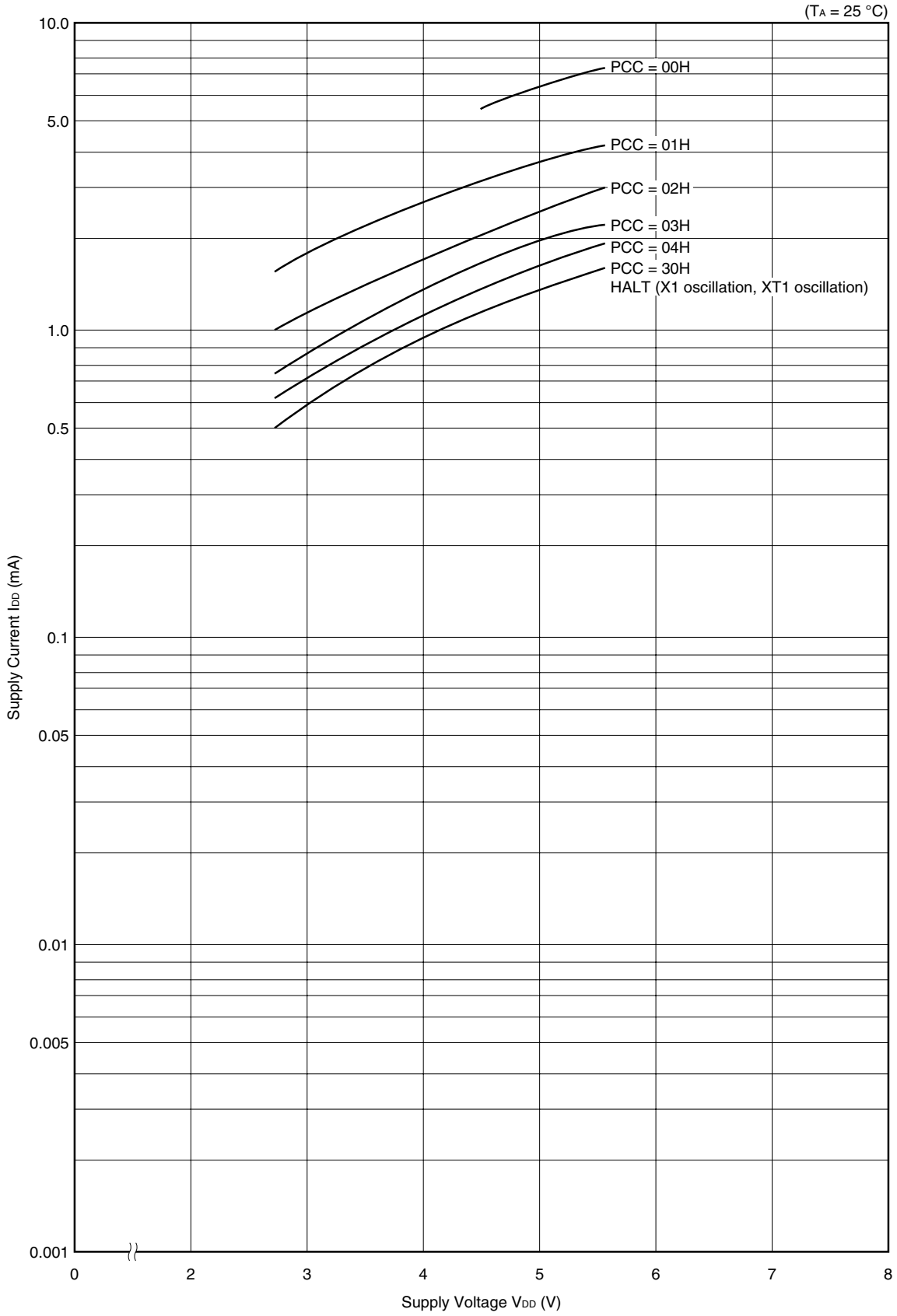


$\overline{\text{RESET}}$ Input Timing

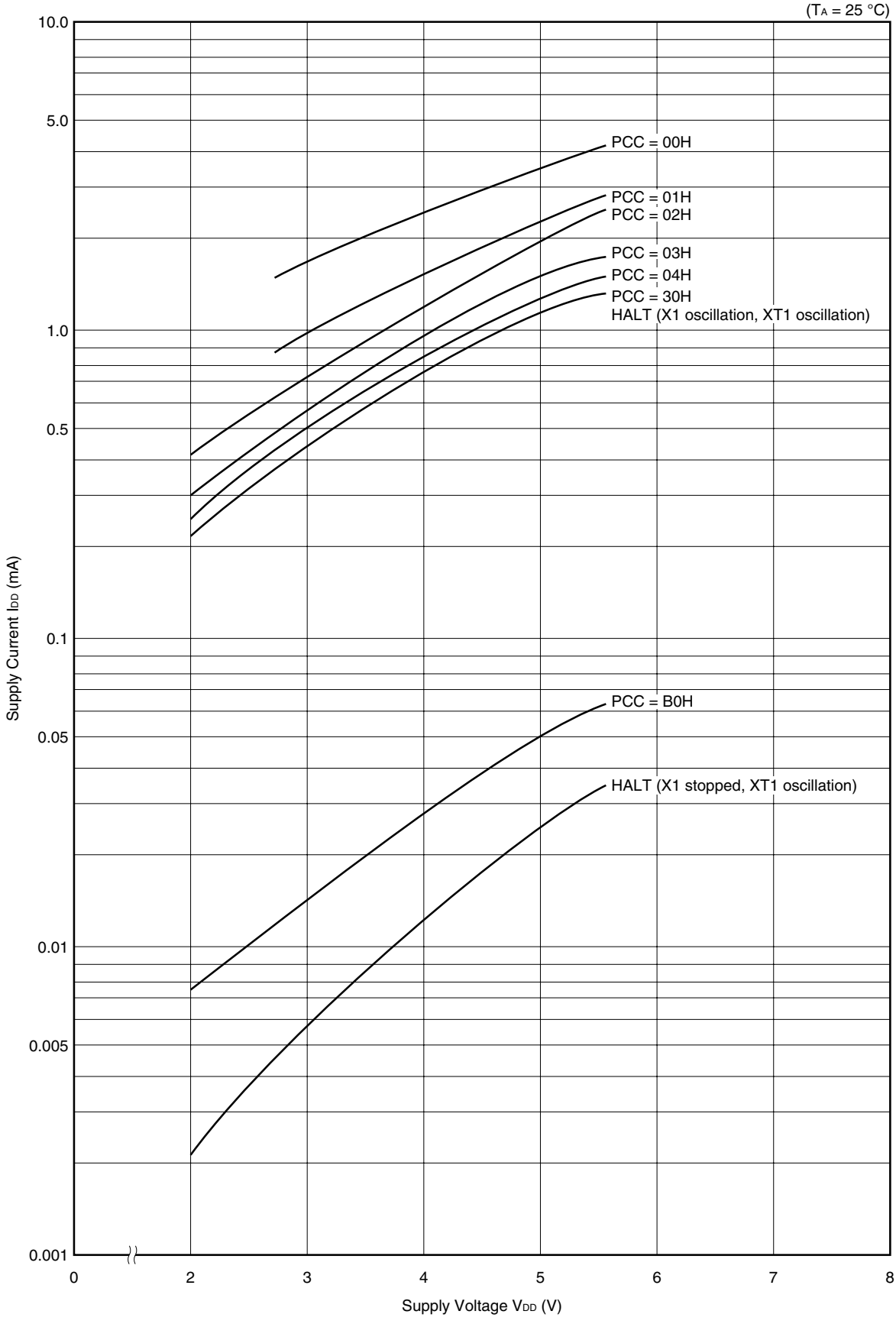


11. CHARACTERISTIC CURVES (REFERENCE VALUE)

I_{DD} vs V_{DD} (f_X = f_{XX} = 5.0 MHz)

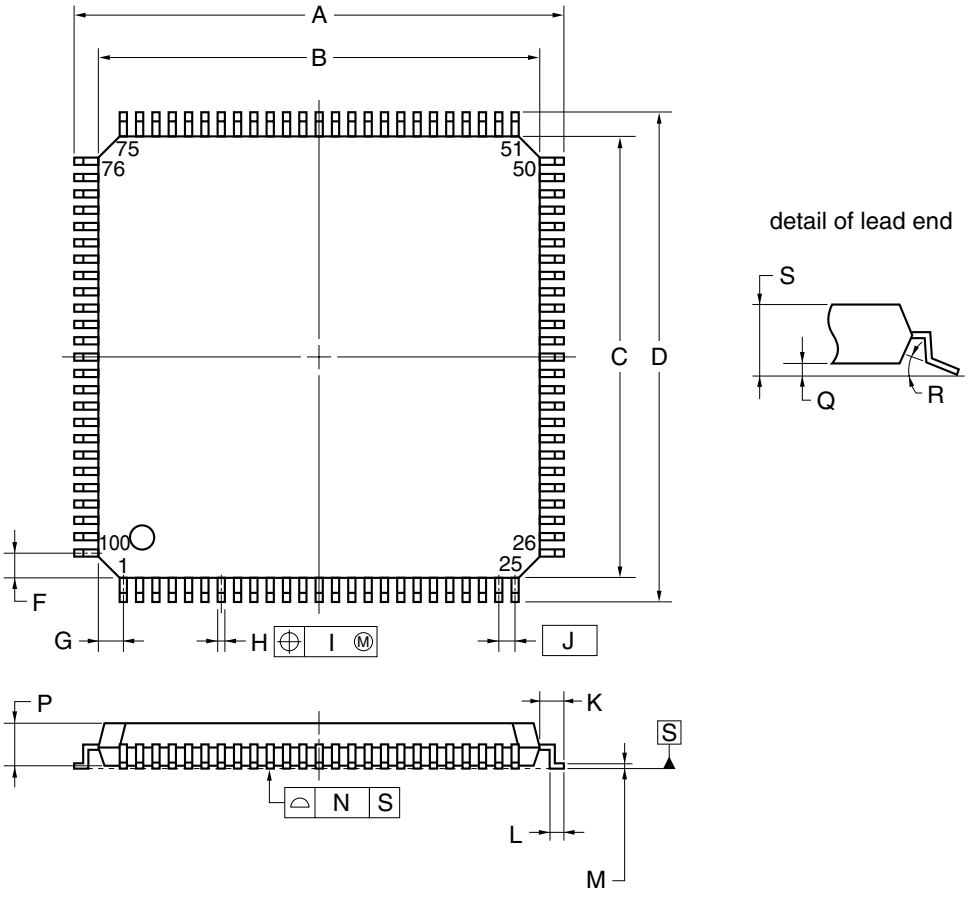


I_{DD} vs V_{DD} (f_X = 5.0 MHz, f_{XX} = 2.5 MHz)



★ 12. PACKAGE DRAWINGS

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



NOTE

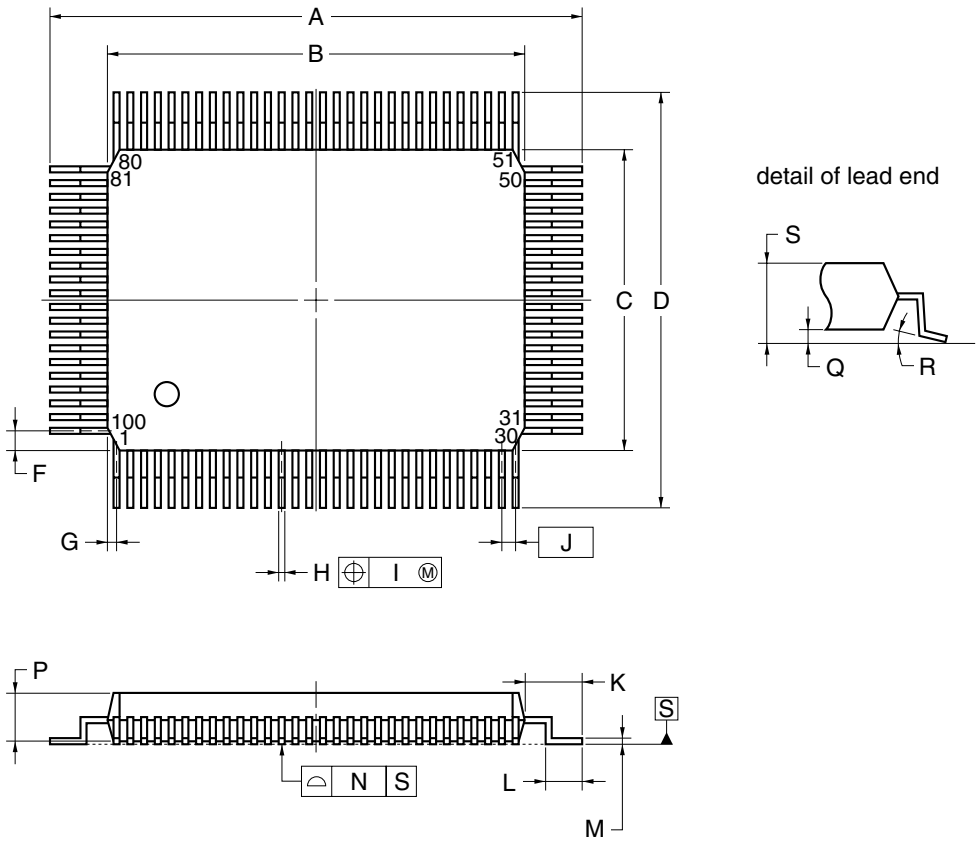
Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	$0.22^{+0.05}_{-0.04}$
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.60 MAX.

S100GC-50-8EU, 8EA-2

Remark Dimensions and materials of ES products are the same as those of the mass production product.

100-PIN PLASTIC QFP (14x20)



NOTE

Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	23.6±0.4
B	20.0±0.2
C	14.0±0.2
D	17.6±0.4
F	0.8
G	0.6
H	0.30±0.10
I	0.15
J	0.65 (T.P.)
K	1.8±0.2
L	0.8±0.2
M	$0.15^{+0.10}_{-0.05}$
N	0.10
P	2.7±0.1
Q	0.1±0.1
R	5°±5°
S	3.0 MAX.

P100GF-65-3BA1-4

Remark Dimensions and materials of ES products are the same as those of the mass production product.

13. RECOMMENDED SOLDERING CONDITIONS

The μPD780306 and 780308 should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact our sales personnel.

Table 13-1. Surface Mounting Type Soldering Conditions

(1) μPD780306GF-×××-3BA: 100-pin plastic QFP (14 × 20 mm)
μPD780308GF-×××-3BA: 100-pin plastic QFP (14 × 20 mm)

Soldering Method	Soldering Conditions	Recommended Soldering Symbols
Infrared reflow	Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C or above), Number of times: Three times max.	IR35-00-3
VPS	Package peak temperature: 215 °C, Duration: 40 sec. (at 200 °C or above), Number of times: Three times max.	VP15-00-3
Wave soldering	Solder bath temperature: 260 °C max., Duration: 10 sec. max., Number of times: Once, Preheating temperature: 120 °C max. (Package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300 °C max., Duration: 3 sec. max. (per device side)	—

★ **(2) μPD780306GC-×××-8EU: 100-pin plastic LQFP (fine pitch)(14 × 14 mm)**
μPD780308GC-×××-8EU: 100-pin plastic LQFP (fine pitch)(14 × 14 mm)

Soldering Method	Soldering Conditions	Recommended Soldering Symbols
Infrared reflow	Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C or above), Number of times: Twice max.	IR35-00-2
VPS	Package peak temperature: 215 °C, Duration: 40 sec. (at 200 °C or above), Number of times: Twice max.	VP15-00-2
Partial heating	Pin temperature: 300 °C max., Duration: 3 sec. max. (per device side)	—

Caution Use of more than one soldering method should be avoided (except in the case of partial heating).

★ APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using μPD780306/780308.
Also refer to **(5) Notes on using development tools**.

(1) Language Processing Software

RA78K0	78K/0 series common assembler package
CC78K0	78K/0 series common C compiler package
DF780308	μPD780308 subseries device file (Part number : μS××××DF78064)
CC78K0-L	78K/0 series common C compiler library source file

(2) PROM Writing Tools

PG-1500	PROM programmer
PA-78P0308GC-8EU PA-78P0308GF PA-78P0308KL-T	Programmer adapters connected to PG-1500
PG-1500 controller	PG-1500 control program

(3) Debugging Tools

- **When in-circuit emulator IE-78K0-NS is used**

IE-78K0-NS	In-circuit emulator common to 78K/0 series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-78K0-NS-PA	Performance board to enhance/expand functions of IE-78K0-NS
IE-70000-98-IF-C	Adapter when using PC-9800 series as host machine (excluding notebook type PCs) (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable when using notebook type PC as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Adapter when using IBM PC/AT™ compatible as host machine (ISA bus supported)
IE-70000-PCI-IF-A	Interface adapter required when using PC with on-chip PCI bus as host machine
IE-780308-NS-EM1	Emulation board to emulate μPD780308 subseries
NP-100GC	Emulation probe for 100-pin plastic LQFP (GC-3EU type)
NP-100GF	Emulation probe for 100-pin plastic QFP (GF-3BA type)
TGC-100SDW	Conversion adapter to connect NP-100GC and a target system board made to be mounted on 100-pin plastic LQFP (GC-8EU type)
EV-9200GF-100	Socket to be mounted on a target system board made for 100-pin plastic QFP (GF-3BA type)
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	78K/0 series common system simulator
DF780308	μPD780308 subseries device file (Part number: μS××××DF78064)

- **When in-circuit emulator IE-78001-R-A is used**

IE-78001-R-A	In-circuit emulator common to 78K/0 series
IE-70000-98-IF-C	Adapter required when PC-9800 series (except notebook type) is used as host machine (C bus supported)
IE-70000-PC-IF-C	Adapter required when IBM PC/AT compatible machine is used as host machine (ISA bus supported)
IE-70000-PCI-IF-A	Interface adapter required when using PC with on-chip PCI bus as host machine
IE-78000-R-SV3	Interface adapter and cable required when EWS is used as host machine
IE-780308-NS-EM1 IE-780308-R-EM	Emulation board to emulate μPD780308 subseries
IE-78K0-R-EX1	Emulation probe conversion board necessary when using IE-780308-NS-EM1 on IE-78001-R-A
NP-100GC	Emulation probe for 100-pin plastic LQFP (GC-8EU type)
NP-100GF	Emulation probe for 100-pin plastic QFP (GF-3BA type)
TGC-100SDW	Conversion adapter to connect NP-100GC and a target system board made to be mounted on 100-pin plastic LQFP (GC-8EU type)
EV-9200GF-100	Socket mounted on board of target system created for 100-pin plastic QFP (GF-3BA type)
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 series
DF780308	Device file for μPD780308 subseries (Part number: μS××××DF78064)

(4) Real-Time OS

RX78K0	78K/0 series real-time OS
MX78K0	78K/0 series OS

(5) Notes on using development tools

- The package name of DF780308 is the DF78064.
- Use ID78K0-NS, ID78K0, and SM78K0 in combination with DF780308.
- Use CC78K0 and RX78K0 in combination with RA78K0 and DF780308.
- NP-100GC and NP-100GF are products of Naito Densei Machida Mfg. Co., Ltd. (TEL (044) 822-3813).
- TGC-100SDW is a product of TOKYO ELETECH CORPORATION.
  Contact: Daimaru Kogyo Ltd.
  Tokyo Electronics Department (TEL: +81-3-3820-7112)
  Osaka Electronics Department (TEL: +81-6-6244-6672)
- For third party development tools, see the **Single-Chip Microcontroller Development Tool Selection Guide (U11069E)**.
- The host machines and OS suitable for each each software are as follows.

Software \ Host Machine [OS]	PC PC-9800 series [Japanese Windows™] IBM PC/AT Compatible Machines [Japanese/English Windows]	EWS HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™]
RA78K0	√Note	√
CC78K0	√Note	√
PG-1500 controller	√Note	—
ID78K0-NS	√	—
ID78K0	√	√
SM78K0	√	—
RX78K0	√Note	√
MX78K0	√Note	√

Note This software is based on DOS.

★ APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are nor marked as such.

Documents Related to Devices

Document Name		Document No.
μPD780308, 780308Y Subseries User's Manual		U11377E
μPD780306, 780308 Data Sheet		This document
μPD780306Y, 780308Y Data Sheet		U12251E
μPD78P0308 Data Sheet		U11776E
μPD78P0308Y Data Sheet		U11832E
78K/0 Series User's Manual (Instruction)		U12326E
78K/0 Series Application Note	Basic (III)	U10182E

Documents Related to Development Tools (User's Manual)

Document Name		Document No.
RA78K0 Assembler Package	Operation	U14445E
	Language	U14446E
	Structured assembly language	U11789E
CC78K0 C Compiler	Operation	U14297E
	Language	U14298E
PG-1500 PROM Programmer		U11940E
PG-1500 Controller PC-9800 Series (MS-DOS™) Based		EEU-1291
PG-1500 Controller IBM PC Series (PC DOS™) Based		U10540E
IE-78K0-NS		U13731E
IE-78K0-NS-A		U14889E
IE-78001-R-A		Planned
IE-780308-NS-EM1		U13304E
IE-780308-R-EM		U11362E
EP-78064		EEU-1469
SM78K0S, SM78K0 System Simulator Ver.2.10 or Later Windows Based	Operation	U14611E
SM78K Series System Simulator Ver. 2.10 or Later	External Part User Open Interface Specifications	U15006E
ID78K0-NS Integrated Debugger Ver 2.00 or Later Windows Based	Operation	U14379E
ID78K0 Integrated Debugger Windows Based	Reference	U11539E
	Guide	U11649E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No.
78K/0 Series Real-Time OS	Fundamentals	U11537E
	Installation	U11536E
78K/0 Series OS MX78K0	Fundamental	U12257E

Other Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE-Products & Packages- (CD-ROM)	X13769E
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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