NEC

MOS INTEGRATED CIRCUIT

μPD780204, 780205, 780206, 780208

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD780204, 780205, 780206, and 780208 microcontrollers are the products of μPD780208 subseries in 78K/0 series, and incorporate many hardware peripherals such as an FIP™ controller/driver, 8-bit resolution A/D converter, timer, serial interface, and interrupt controller.

In addition to these standard mask ROM models, one-time PROM models that can operate in the same voltage range, EPROM models μPD78P0208, and various development tools are available.

The functions of these microcontrollers are described in detail in the following User's Manual. Be sure to read this manual when you design a system using any of these microcontrollers.

μPD780208 Subseries User's Manual: U11302E

78K/0 Series User's Manual - Instruction: IEU-1372

FEATURES

- High-capacity ROM and RAM

Item / Product Name	Program Memory (ROM)	Data Memory				Package
		Internal high-speed RAM	Buffer RAM	FIP display RAM	Internal expansion RAM	
μPD780204	32 K bytes	1024 bytes	64 bytes	80 bytes	Not provided	100-pin plastic QFP (14 × 20 mm)
μPD780205	40 K bytes					
μPD780206	48 K bytes				1024 bytes	
μPD780208	60 K bytes					

- Wide range of instruction execution time
  - from high-speed (0.4 μs) to ultra low-speed (122 μs)
- I/O ports: 74
- FIP controller/driver: total display outputs: 53
- 8-bit resolution A/D converter: 8 channels
- Serial interface: 2 channels
- Timer: 5 channels
- Power supply voltage: V_{DD} = 2.7 to 5.5 V

APPLICATIONS

Minicomponent stereo, cassette deck, tuner, CD player, VCR.

ORDERING INFORMATION

Part Number	Package
μPD780204GF-×××-3BA	100-pin plastic QFP (14 × 20 mm)
μPD780205GF-×××-3BA	100-pin plastic QFP (14 × 20 mm)
★ μPD780206GF-×××-3BA	100-pin plastic QFP (14 × 20 mm)
★ μPD780208GF-×××-3BA	100-pin plastic QFP (14 × 20 mm)

Remark "×××" indicates ROM code number.

The information in this document is subject to change without notice.

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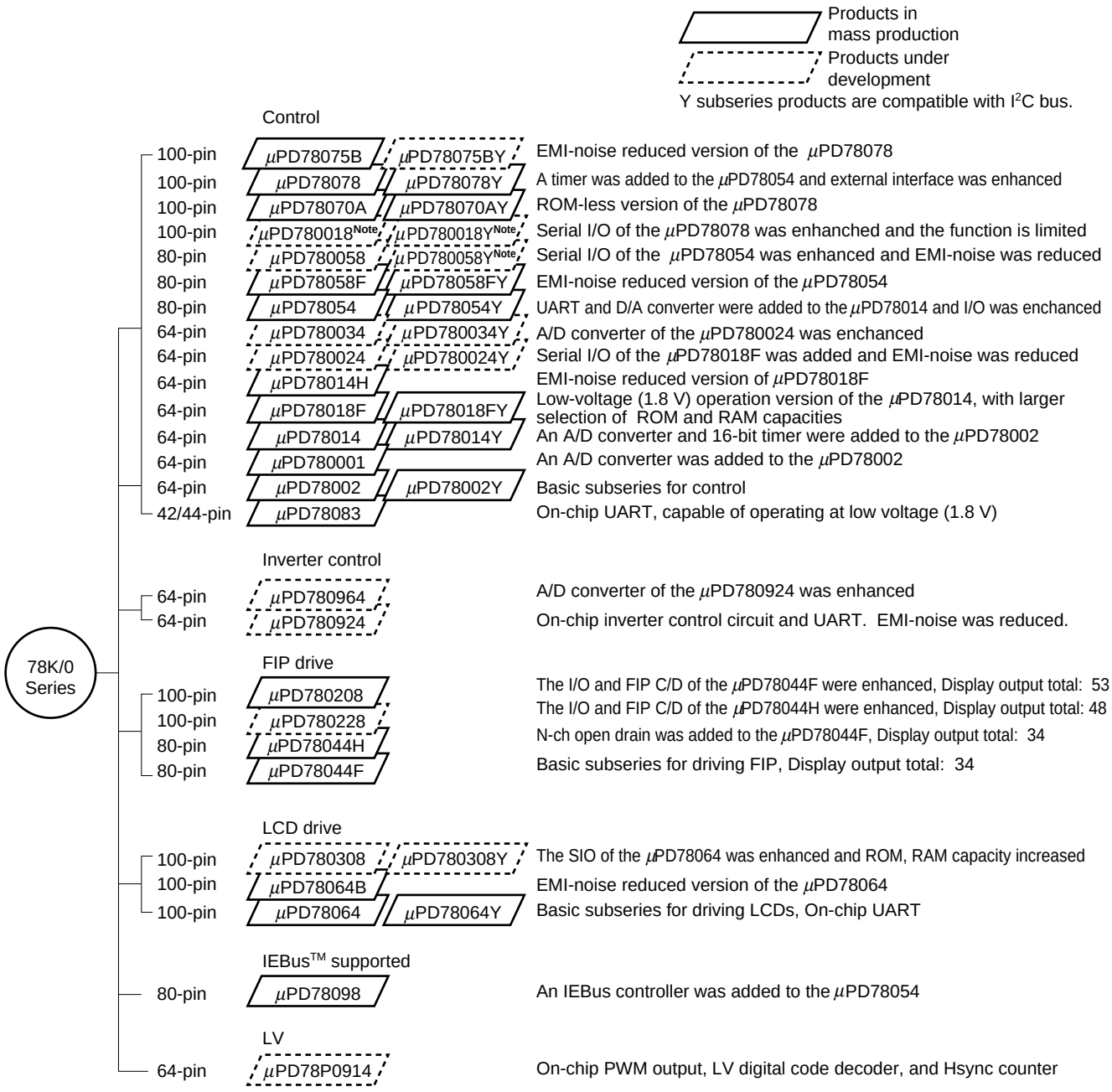
The mark ★ shows major revised point.

★ **78K/0 SERIES PRODUCT DEVELOPMENT**

The following shows the 78K/0 Series products development. Subseries name are shown inside frames.



Note Under planning

The following lists the main functional differences between subseries products.

Subseries Name \ Function		ROM Capacity	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-bit	16-bit	Watch	WDT							
Control	μPD78075B	32 K - 40K	4ch	1ch	1ch	1ch	8ch	–	2ch	3ch (UART : 1ch)	88	1.8 V	○
	μPD78078	48 K - 60K											
	μPD78070A	–									61	2.7 V	
	μPD780018	48 K - 60K							–	2ch (time division 3-wire: 1ch)	88		
	μPD780058	24 K - 60 K	2ch						2ch	3ch (time division UART: 1ch)	68	1.8 V	
	μPD78058F	48 K - 60 K								3ch (UART: 1ch)	69	2.7 V	
	μPD78054	16 K - 60 K										2.0 V	
	μPD780034	8 K - 32 K					–	8ch	–	3ch (UART: 1ch, time division 3-wire: 1ch)	51	1.8 V	
	μPD780024						8 ch	–					
	μPD78014H									2ch	53		
	μPD78018F	8 K - 60 K											
	μPD78014	8 K - 32 K										2.7 V	
	μPD780001	8 K		–	–					1ch	39		–
	μPD78002	8 K - 16 K			1ch		–				53		○
	μPD78083				–		8ch			1ch (UART: 1ch)	33	1.8 V	–
Inverter control	μPD780964	8 K - 32 K	3ch	**Note**	–	1ch	–	8ch	–	2c (UART: 2ch)	47	2.7 V	○
	μPD780924						8ch	–					
FIP drive	μPD780208	32 K - 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	2 ch	74	2.7 V	–
	μPD780228	48 K - 60 K	3ch	–	–					1ch	72	4.5 V	
	μPD78044H	32 K - 48 K	2ch	1ch	1ch						68	2.7 V	
	μPD78044F	16 K - 40 K								2ch			
LCD drive	μPD780308	48 K - 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	3 ch (time division UART: 1ch)	57	1.8 V	–
	μPD78064B	32 K								2 ch (UART : 1 ch)		2.0 V	
	μPD78064	16 K - 32 K											
IEBus supported	μPD78098	32 K - 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART : 1 ch)	69	2.7 V	○
LV	μPD78P0914	32 K	6 ch	–	–	1 ch	8 ch	–	–	2 ch	54	4.5 V	○

Note 10-bit timer: 1 channel

FUNCTIONAL OUTLINE

Item \ Product Name		μPD780204	μPD780205	μPD780206	μPD780208
Internal memory	ROM	32 K bytes	40 K bytes	48 K bytes	60 K bytes
	High-speed RAM	1024 bytes			
	Buffer RAM	64 bytes			
	FIP display RAM	80 bytes			
	Expansion RAM	Not provided		1024 bytes	
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Instruction cycle		Variable instruction execution time			
	w/main system clock	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (at 5.0 MHz)			
	w/subsystem clock	122 μs (at 32.768 kHz)			
Instruction set		• Multiplecation/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit operation (set, reset, test, Boolean algebra)			
I/O ports (including those multiplexed with FIP pins)		Total : 74 lines • CMOS input : 2 lines • CMOS I/O : 27 lines • N-ch open-drain I/O : 5 lines • P-ch open-drain I/O : 24 lines • P-ch open-drain output : 16 lines			
FIP controller/driver		Total : 53 lines • Segment : 9 to 40 lines • Digit : 2 to 16 lines			
A/D converter		• 8-bit resolution × 8 channels • Supply voltage : AV_{DD} = 4.0 to 5.5 V			
Serial interface		• 3-wire serial I/O/SBI/2-wire serial I/O mode selectable : 1 channel • 3-wire serial I/O mode (w/automatic transfer/receive function of up to 64 bytes): 1 channel			
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel			
Timer output		3 lines (one for 14-bit PWM output)			
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz (main system clock: at 5.0 MHz) 32.768 kHz (subsystem clock: at 32.768 kHz)			
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz : (main system clock: at 5.0 MHz)			

Item \ Product Name		μPD780204	μPD780205	μPD780206	μPD780208
Vectored interrupt sources	Maskable	Internal: 9, external: 4			
	Non-maskable	Internal: 1			
	Software	1			
Test input		Internal: 1 line			
Supply voltage		V_{DD} = 2.7 to 5.5 V			
Package		100-pin plastic QFP (14 × 20 mm)			

CONTENTS

1. PIN CONFIGURATION (Top View)

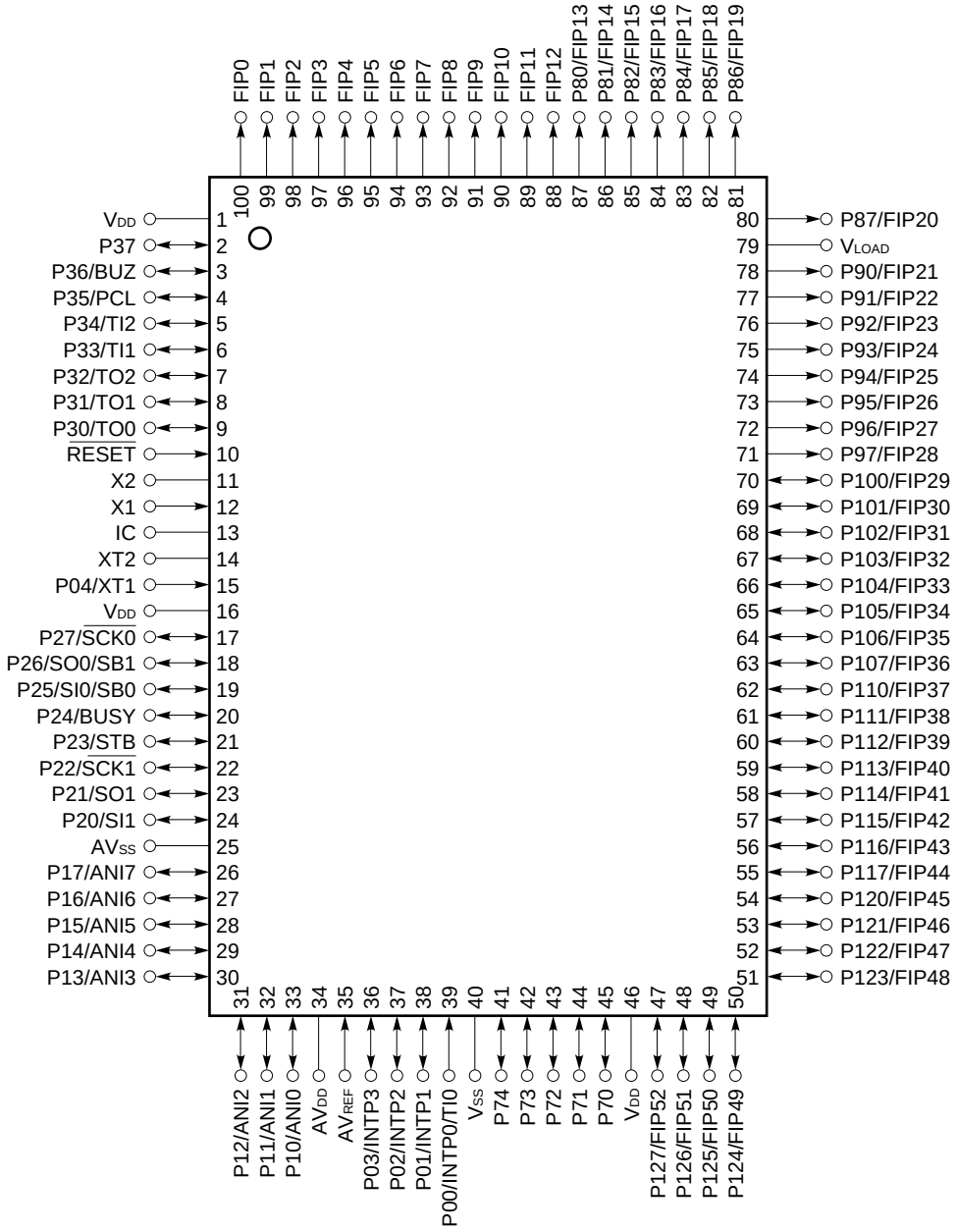
100-Pin Plastic QFP (14 × 20 mm)

μPD780204GF - ××× - 3BA

μPD780205GF - ××× - 3BA

★ μPD780206GF - ××× - 3BA

★ μPD780208GF - ××× - 3BA



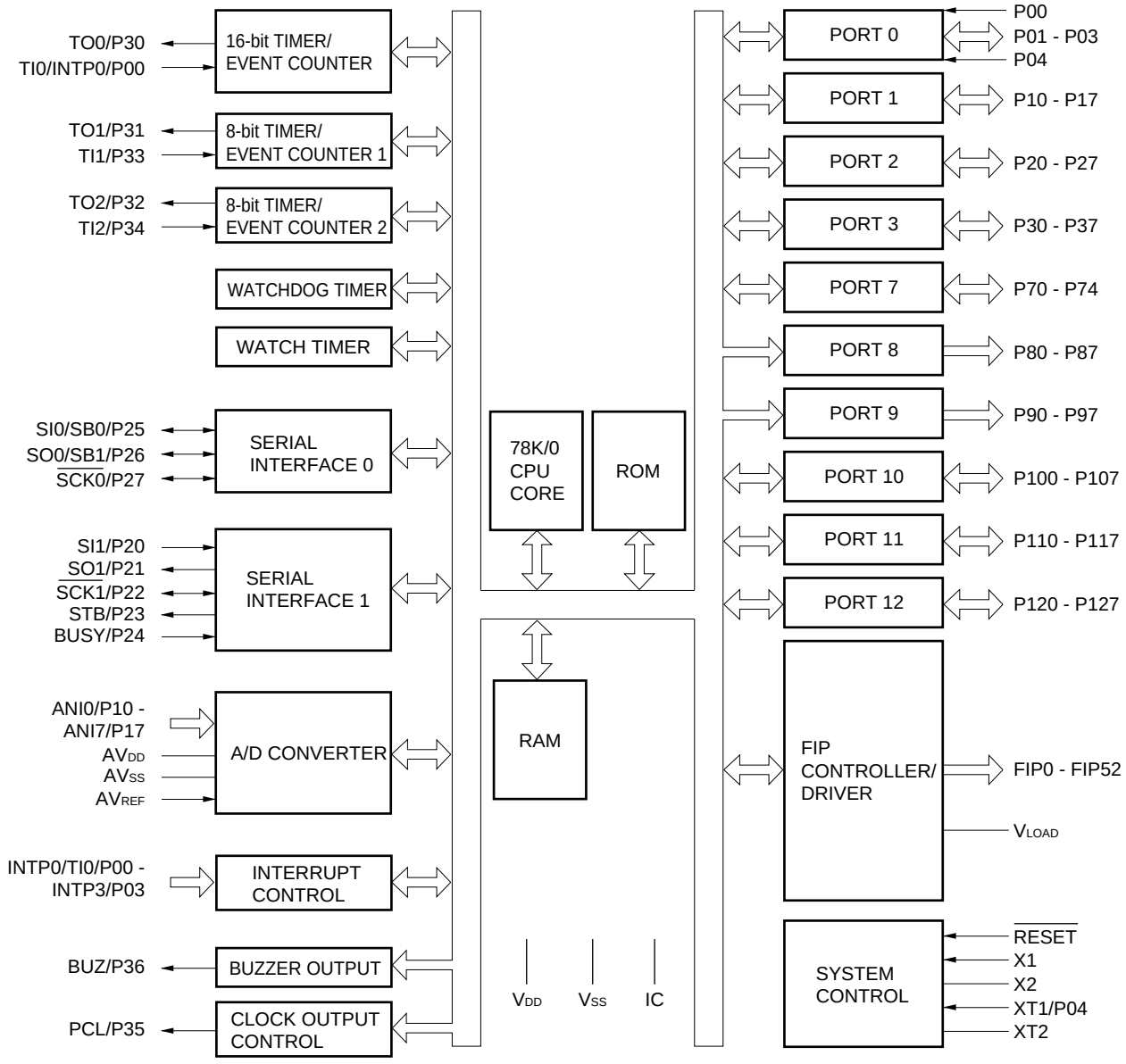
Cautions 1. Connect the IC (Internally Connected) pins directly to the V_{SS}.

2. Connect the AV_{DD} pin to the V_{DD} pin.

3. Connect the AV_{SS} pin to the V_{SS} pin.

P00-P04	:	Port0
P10-P17	:	Port1
P20-P27	:	Port2
P30-P37	:	Port3
P70-P74	:	Port7
P80-P87	:	Port8
P90-P97	:	Port9
P100-P107	:	Port10
P110-P117	:	Port11
P120-P127	:	Port12
INTP0-INTP3	:	Interrupt from Peripherals
TI0-TI2	:	Timer Input
TO0-TO2	:	Timer Output
SB0, SB1	:	Serial Bus
SI0, SI1	:	Serial Input
SO0, SO1	:	Serial Output
$\overline{SCK0}$, $\overline{SCK1}$	:	Serial Clock
PCL	:	Programmable Clock
BUZ	:	Buzzer Clock
STB	:	Strobe
BUSY	:	Busy
FIP0-FIP52	:	Fluorescent Indicator Panel
V_{LOAD}	:	Negative Power Supply
X1, X2	:	Crystal (Main System Clock)
XT1, XT2	:	Crystal (Subsystem Clock)
$\overline{RESET}$	:	Reset
ANI0-ANI7	:	Analog Input
AV_{DD}	:	Analog Power Supply
AV_{SS}	:	Analog Ground
AV_{REF}	:	Analog Reference Voltage
V_{DD}	:	Power Supply
V_{SS}	:	Ground
IC	:	Internally Connected

2. BLOCK DIAGRAM



Remark The capacities of the internal ROM and RAM differ depending on the product.

3. PIN FUNCTIONS

3.1 PORT PINS (1/2)

Pin Name	I/O	Function		On Reset	Sharde by:
P00	Input	Port 0 5-bit I/O port	Input only	Input	INTP0/TI0
P01	I/O		Can be specified for input or output in 1-bit units. When used as an input port pin, an on-chip pull-up resistor can be used through software.	Input	INTP1
P02					INTP2
P03					INTP3
P04[Note 1]	Input		Input only	Input	XT1
P10-P17	I/O	Port 1 8-bit I/O port Can be specified for input or output in 1-bit units. When used as an input port pin, an on-chip pull-up resistor can be used through software.[Note 2]		Input	ANI0-ANI7
P20	I/O	Port 2 8-bit I/O port Can be specified for input or output in 1-bit units. When used as an input port pin, an on-chip pull-up resistor can be used through software.		Input	SI1
P21					SO1
P22					$\overline{SCK1}$
P23					STB
P24					BUSY
P25					SI0/SB0
P26					SO0/SB1
P27					$\overline{SCK0}$
P30	I/O	Port 3 8-bit I/O port Can be specified for input or output in 1-bit units. Can directly drive LEDs. When used as an input port pin, an on-chip pull-up resistor can be used through software. A pull-down resistor can be connected in 1-bit units by mask option.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—

Notes 1. When the P04/XT1 pins is used as an input port pin, bit 6 (FRC) of the porcessor clock control register (PCC) must be set to 1. (At this time, do not use the feedback resistor of the subsystem clock oscillator circuit.)

2. When the P10/ANI0 through P17/ANI7 pins are used as the analog input lines of the A/D converter, be sure to place the port 1 in the input mode. In this case, the on-chip pull-up resistors are automaticaly unused.

3.1 PORT PINS (2/2)

Pin Name	I/O	Function	On Reset	Shared by:
P70-P74	I/O	Port 7 5-bit N-ch open-drain I/O port Can be specified for input or output in 1-bit units. Can directly drive LEDs. A pull-up resistor can be connected in 1-bit units by mask option.	Input	—
P80-P87	Output	Port 8 8-bit P-ch open-drain high-voltage output port Can directly drive LEDs. A pull-down resistor can be connected in 1-bit units by mask option (whether V_{LOAD} or V_{SS} is connected can be specified in 4-bit units).	Output	FIP13-FIP20
P90-P97	Output	Port 9 8-bit P-ch open-drain high-voltage output port Can directly drive LEDs. A pull-down resistor can be connected in 1-bit units by mask option (whether V_{LOAD} or V_{SS} is connected can be specified in 4-bit units).	Output	FIP21-FIP28
P100-P107	I/O	Port 10 8-bit P-ch open-drain high-voltage output port Can be specified for input or output in bit units. Can directly drive LEDs. A pull-down resistor can be connected in 1-bit units by mask option (whether V_{LOAD} or V_{SS} is connected can be specified in 4-bit units).	Input	FIP29-FIP36
P110-P117	I/O	Port 11 8-bit P-ch open-drain high-voltage I/O port Can be specified for input or output in 1-bit units. Can directly drive LEDs. A pull-down resistor can be conneced in 1-bit units by mask option (whether V_{LOAD} or V_{SS} is connected can be specified in 4-bit units).	Input	FIP37-FIP44
P120-P127	I/O	Port12 8-bit P-ch open-drain high-voltage I/O port. Can be specified for input or output in 1-bit units. Can directly drive LEDs. A pul-down resistor can be connected in 1-bit units by mask option (whether V_{LOAD} or V_{SS} is connected can be specified in 4-bit units).	Input	FIP45-FIP52

3.2 PINS OTHER THAN PORT PINS (1/2)

Pin Name	I/O	Function	On Reset	Shared by:
INTP0	Input	Valid edge (rising, falling, or both rising and falling edges) can be specified. External interrupt request input	Input	P00/TI0
INTP1				P01
INTP2				P02
INTP3		Falling edge-active external interrupt input	Input	P03
SI0	Input	Serial data input lines of serial interface	Input	P25/SB0
SI1				P20
SO0	Output	Serial data output lines of serial interface	Input	P26/SB1
SO1				P21
SB0	I/O	Serial data I/O lines of serial interface	Input	P25/SI0
SB1				P26/SO0
$\overline{SCK0}$	I/O	Serial clock I/O lines of serial interface	Input	P27
$\overline{SCK1}$				P22
STB	Output	Automatic transfer/receive strobe output line of serial interface	Input	P23
BUSY	Input	Automatic transfer/receive busy input line of serial interface	Input	P24
TI0	Input	External count clock input to 16-bit timer (TM0)	Input	P00/INTP0
TI1		External count clock input to 8-bit timer (TM1)		P33
TI2		External count clock input to 8-bit timer (TM2)		P34
TO0	Output	16-bit timer (TM0) output (multiplexed with 14-bit PWM output)	Input	P30
TO1		8-bit timer (TM1) output		P31
TO2		8-bit timer (TM2) output		P32
PCL	Output	Clock output (for trimming main system clock and subsystem clock)	Input	P35
BUZ	Output	Buzzer output	Input	P36
FIP0-FIP12	Output	High-voltage, high-current output for FIP controller/driver display output A pull down register can be connected by mask option.	Output	–
FIP13-FIP20	Output	High-voltage, high-current output for FIP controller/driver display output	Output	P80-P87
FIP21-FIP28				P90-P97
FIP29-FIP36			Input	P100-P107
FIP37-FIP44				P110-P117
FIP45-FIP52				P120-P127
V_{LOAD}	–	Connects pull-down resistor to FIP controller/driver	–	–

3.2 PINS OTHER THAN PORT PINS (2/2)

Pin Name	I/O	Function	On Reset	Shared by:
ANI0-ANI7	Input	A/D converter analog input lines	Input	P10-P17
AV_{REF}	Input	A/D converter reference voltage input line	—	—
AV_{DD}	—	Analog power supply to A/D converter. Connected to V_{DD} pin.	—	—
AV_{SS}	—	A/D converter ground line. Connected to V_{SS} pin.	—	—
$\overline{\text{RESET}}$	Input	System reset input	—	—
X1	Input	Connect crystal for main system clock oscillation.	—	—
X2	—		—	—
XT1	Input	Connect crystal for subsystem clock oscillation.	Input	P04
XT2	—		—	—
V_{DD}	—	Positive power supply	—	—
V_{SS}	—	Ground potential	—	—
IC	—	Internal connection. Connected directly to V_{SS} pin.	—	—

3.3 PIN I/O CIRCUITS AND PROCESSING OF UNUSED PINS

Table 3-1 shows the I/O circuit type of each pin and the processing of unused pins.

For the configuration of the I/O circuit of each type, refer to Figure 3-1.

Table 3-1. I/O Circuit Type

	Pin Name	I/O Circuit Type	I/O	Recommended Connections When Unused
	P00/INTP0/TI0	2	Input	Connect to V_{SS}
	P01/INTP1	8-A	I/O	Independently connect to Vss through resistor
	P02/INTP2			
	P03/INTP3			
	P04/XT1	16	Input	Connect to V_{DD} or V_{SS}
	P10/ANI0-P17/ANI7	11	I/O	Independently connect to V_{DD} or V_{SS} through resistor
	P20/SI1	8-A		
	P21/SO1	5-A		
	P22/$\overline{SCK1}$	8-A		
	P23/STB	5-A		
	P24/BUSY	8-A		
	P25/SI0/SB0	10-A		
	P26/SO0/SB1			
	P27/$\overline{SCK0}$			
	P30/TO0	5-C		
	P31/TO1			
	P32/TO2			
	P33/TI1	8-B		
	P34/TI2			
	P35/PCL	5-C		
	P36/BUZ			
	P37			
★	P70-P74	13-B		
	FIP0-FIP12	14-A	Output	Open
	P80/FIP13-P87/FIP20			
	P90/FIP21-P97/FIP28			
★	P100/FIP29-P107/FIP36	15-C	I/O	Independently connect to V_{DD} or V_{SS} through resistor
	P110/FIP37-P117/FIP44			
	P120/FIP45-P127/FIP52			
	$\overline{RESET}$	2	Input	—
	XT2	16	—	Open
	AV_{REF}	—		Connect to V_{SS}
	AV_{DD}			Connect to V_{DD}
	AV_{SS}			Connect to V_{SS}
	V_{LOAD}			
	IC			Connect directly to V_{SS}

Figure 3-1. Pin I/O Circuits (1/2)

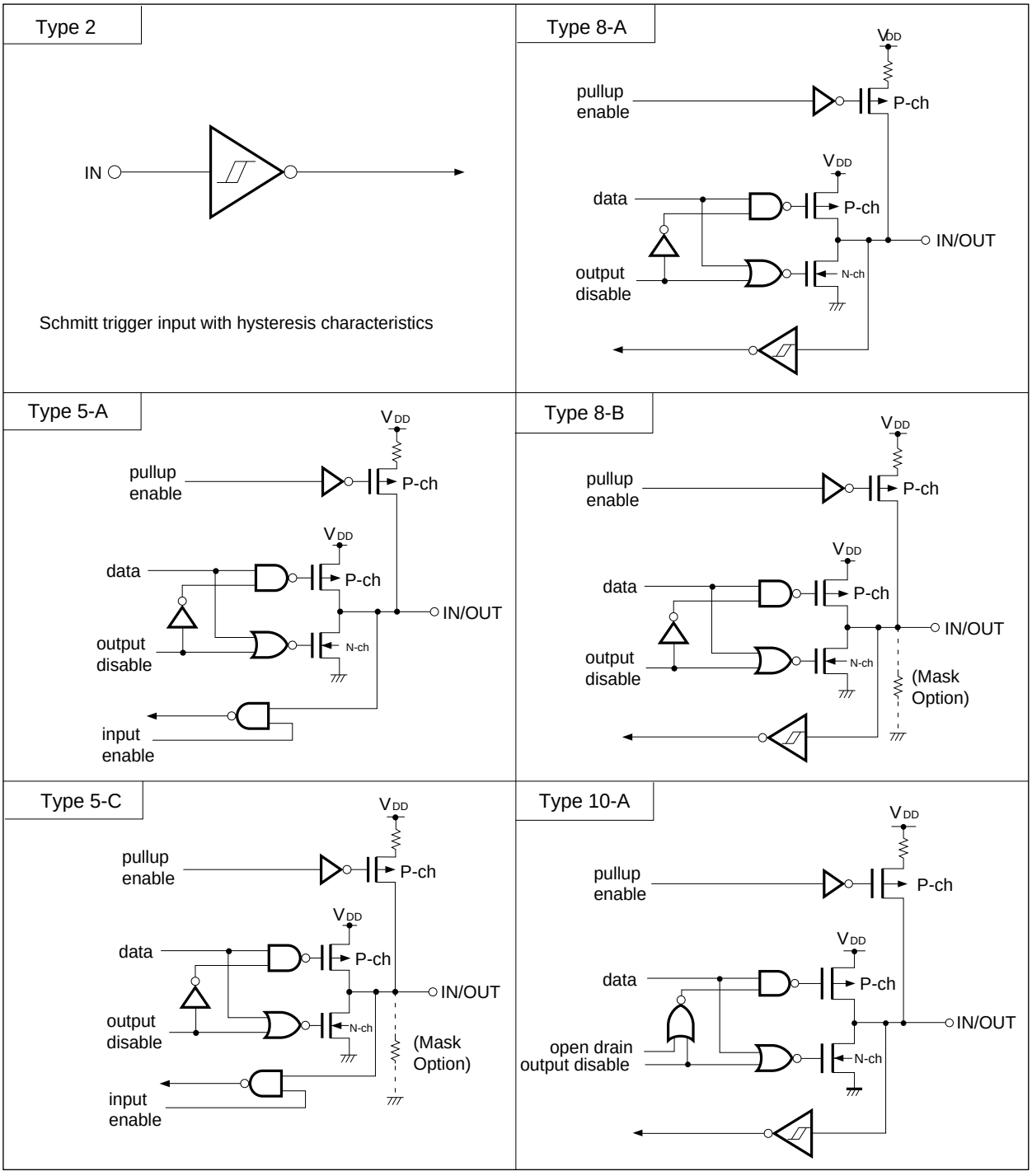
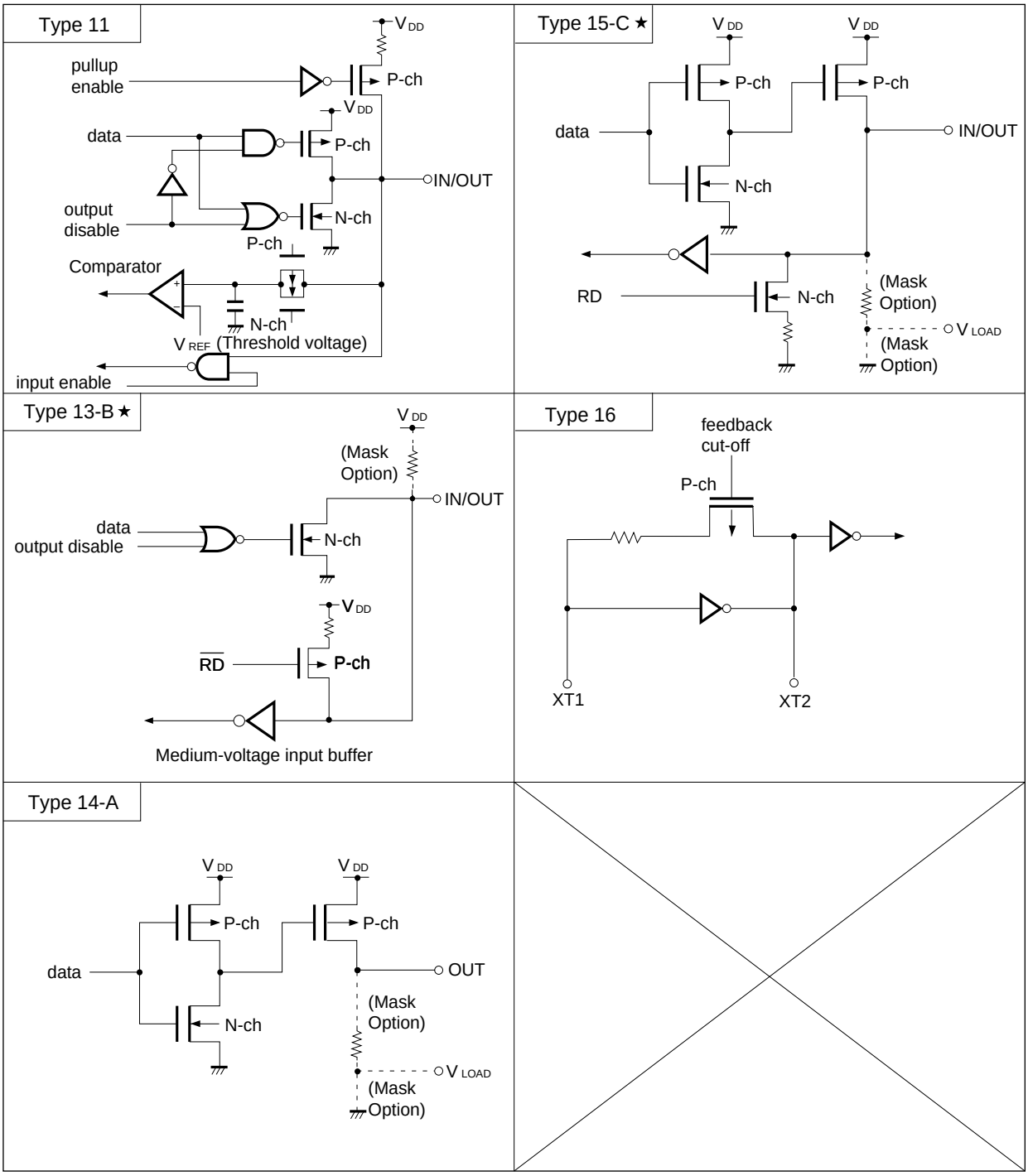


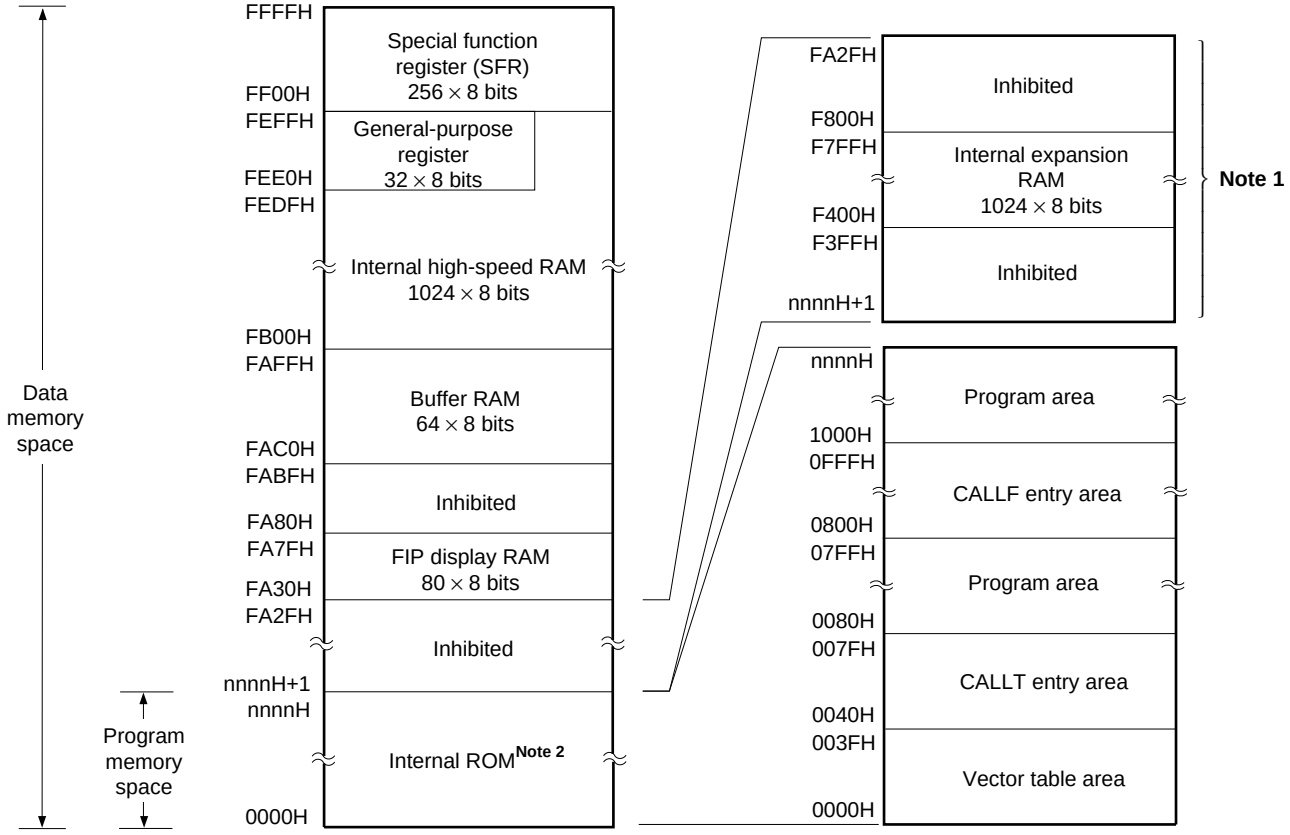
Figure 3-1. Pin I/O Circuits (2/2)



4. MEMORY SPACE

Figure 4-1 shows the memory maps for μPD780204, 780205, 780206, and 780208.

Figure 4-1. Memory Map



Notes 1. μPD780206 and 780208 only.

2. The internal ROM capacities vary depending on the product. (Refer to the table below.)

Product Name	Internal ROM Last Address nnnnH
μPD780204	7FFFH
μPD780205	9FFFH
μPD780206	BFFFH
μPD780208	EFFFH

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 PORTS

I/O ports are classified into the following 5 kinds:

- CMOS input (P00, P04) : 2
- CMOS input/output (P01 - P03, ports 1-3) : 27
- N-ch open-drain input/output (port 7) : 5
- P-ch open-drain output (ports 8, 9) : 16
- P-ch open-drain input/output (ports 10 - 12) : 24

Total : 74

Table 5-1. Port Function

Name	Pin Name	Function
Port 0	P00, P04	Input port
	P01-P03	I/O port. Can be specified for input or output in 1-bit units. When used as input port, internal pull-up resistor can be connected through software.
Port 1	P10-P17	I/O port. Can be specified for input or output in 1-bit units. When used as input port, internal pull-up resistor can be connected through software.
Port 2	P20-P27	I/O port. Can be specified for input or output in 1-bit units. When used as input port, internal pull-up resistor can be connected through software.
Port 3	P30-P37	I/O port. Can be specified for input or output in 1-bit units. When used as input port, internal pull-up resistor can be connected through software. Pull-down resistor can be connected in 1-bit units by mask option. Can directly drive LED.
Port 7	P70-P74	N-ch open-drain I/O port. Can be specified for input or output in 1-bit units. Pull-up resistor can be connected in 1-bit units by mask option. Can directly drive LED.
Port 8	P80-P87	P-ch open-drain high-voltage output port. Pull-down resistor can be connected in 1-bit units by mask option (connection to V_{LOAD} or V_{SS} can be specified in 4-bit units). Can directly drive LEDs.
Port 9	P90-P97	P-ch open-drain high-voltage output port. Pull-down resistor can be connected in 1-bit units by mask option (connection to V_{LOAD} or V_{SS} can be specified in 4-bit units). Can directly drive LEDs.
Port 10	P100-P107	P-ch open-drain high-voltage I/O port. Can be specified for input or output in 1-bit units. Pull-down resistor can be connected in 1-bit units by mask option (connection to V_{LOAD} or V_{SS} can be specified in 4-bit units). Can directly drive LEDs.
Port 11	P110-P117	P-ch open-drain high-voltage I/O port. Can be specified for input or output in 1-bit units. Pull-down resistor can be connected in 1-bit units by mask option (connection to V_{LOAD} or V_{SS} can be specified in 4-bit units). Can directly drive LEDs.
Port 12	P120-P127	P-ch open-drain high-voltage I/O port. Can be specified for input or output in 1-bit units. Pull-down resistor can be connected in 1-bit units by mask option (connection to V_{LOAD} or V_{SS} can be specified in 4-bit units). Can directly drive LEDs.

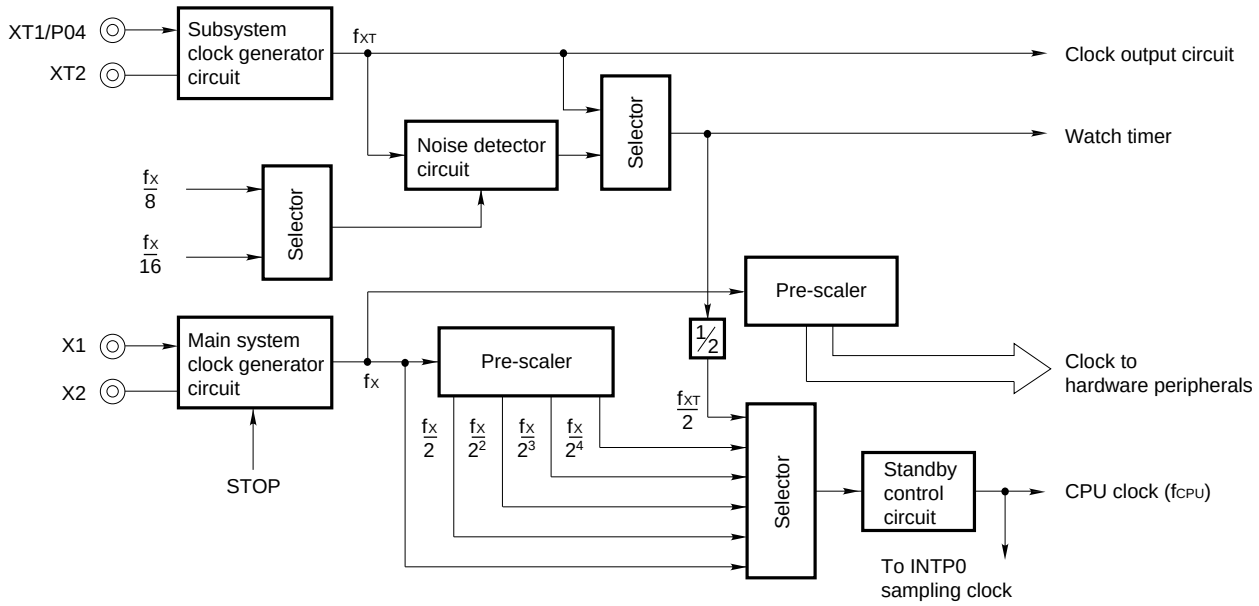
5.2 CLOCK GENERATOR CIRCUIT

The clock generator circuit has two kinds of generator circuits: the main system clock and subsystem clock.

The instruction time can be changed.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (with main system clock: 5.0 MHz)
- 122 μs (with subsystem clock: 32.768 kHz)

Figure 5-1. Clock Generator Circuit Block Diagram



5.3 TIMER/EVENT COUNTER

Five channels of timer/event counters are provided.

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2. Timer/Event Counter Groups and Configurations

		16-bit Timer/ Event Counter	8-bit Timer/ Event Counter	Watch Timer	Watchdog Timer
Group	Interval timer	1 channel	2 channels	1 channel	1 channel
	External event counter	1 channel	2 channels	–	–
Function	Timer output	1 output	2 outputs	–	–
	PWM output	1 output	–	–	–
	Pulse width measurement	1 input	–	–	–
	Square wave output	1 output	2 outputs	–	–
	Interrupt Request	1	2	1	1
	Test input	–	–	1 input	–

Figure 5-2. 16-Bit Timer/Event Counter Block Diagram

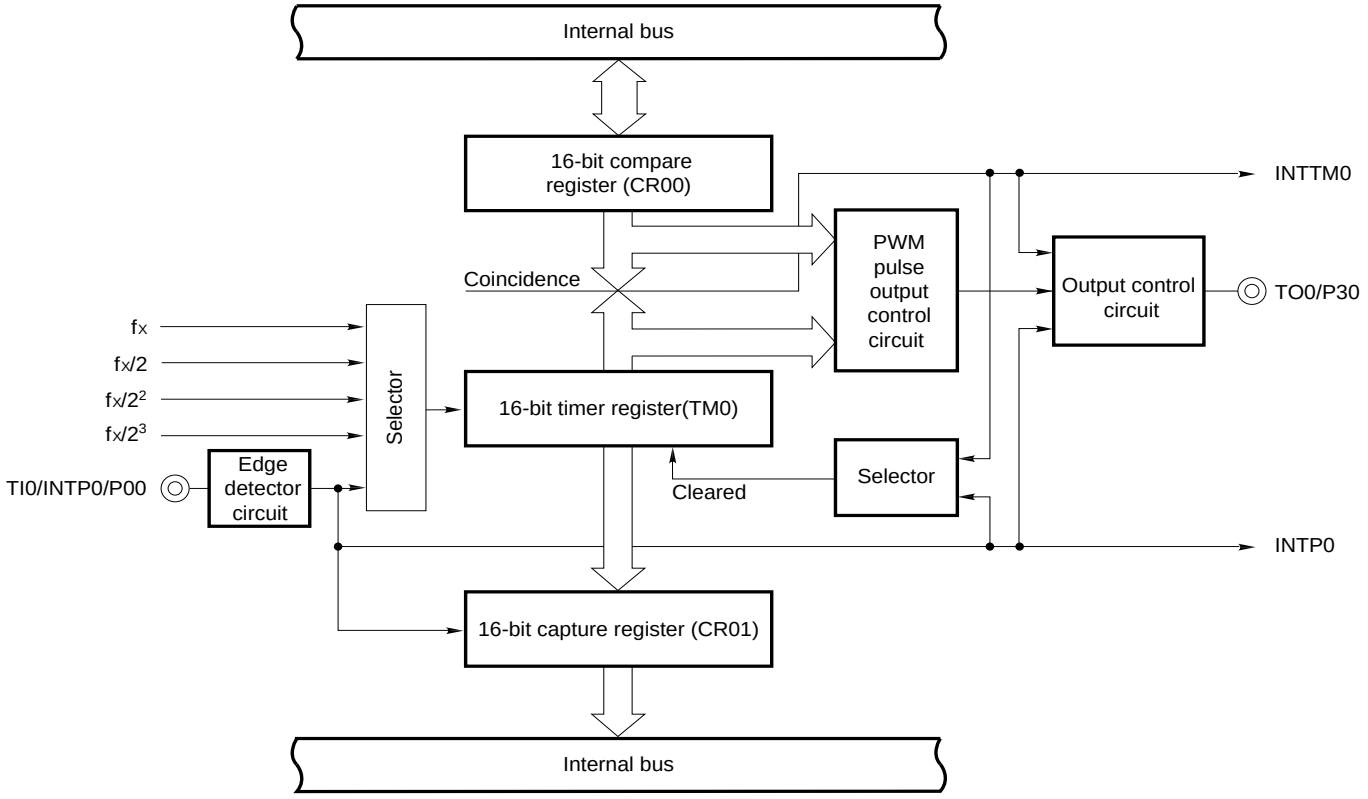


Figure 5-3. 8-Bit Timer/Event Counter Block Diagram

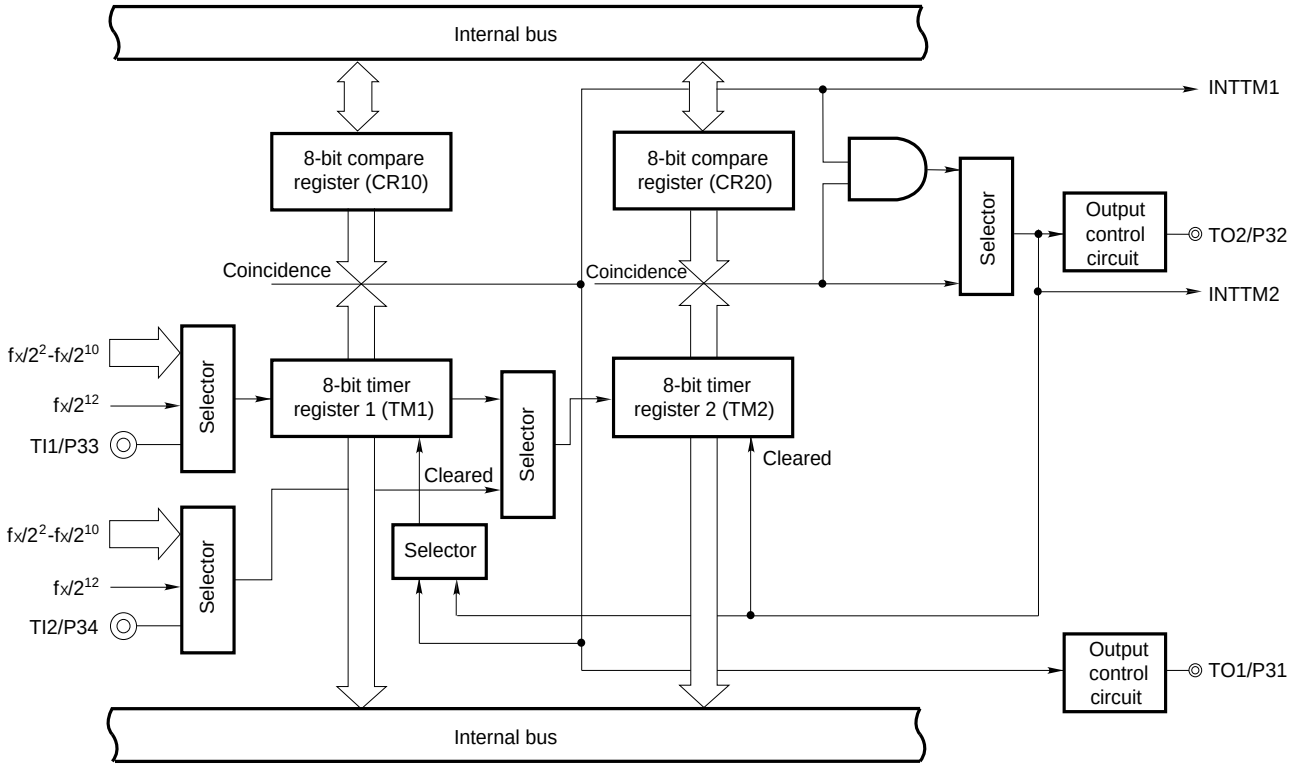


Figure 5-4. Watch Timer Block Diagram

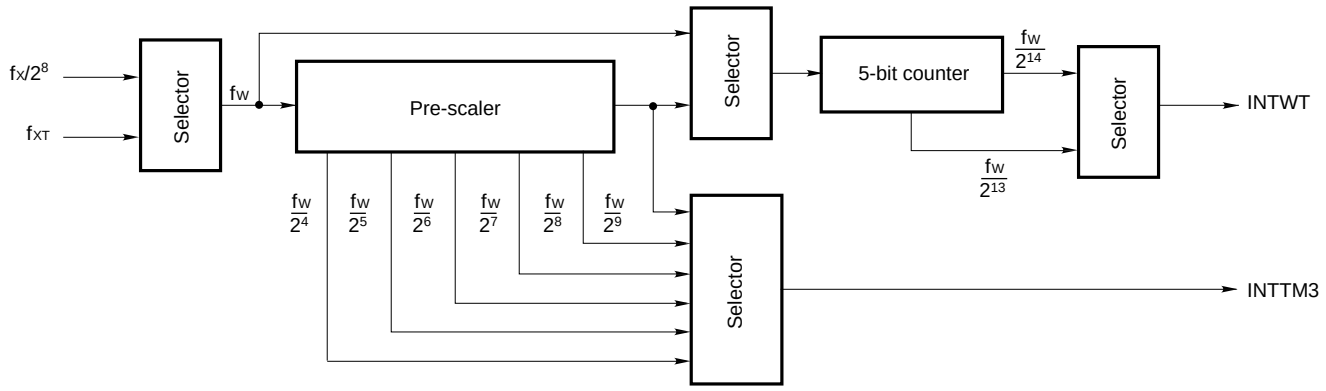
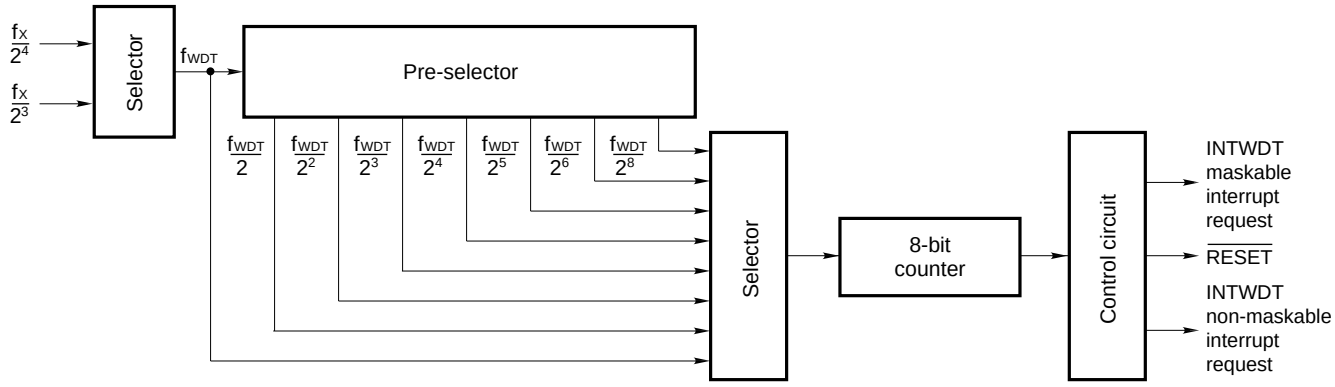


Figure 5-5. Watchdog Timer Block Diagram

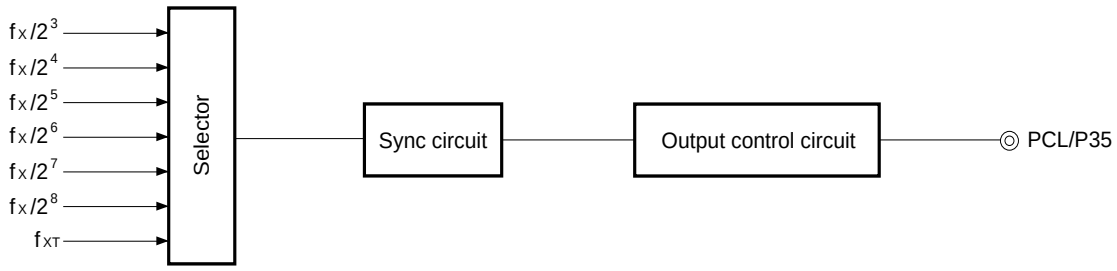


5.4 CLOCK OUTPUT CONTROL CIRCUIT

Clocks of the following frequencies can be output to the clock :

- 19.5 kHz/39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz (with main system clock: 5.0 MHz)
- 32.768 kHz (with subsystem clock: 32.768 kHz)

Figure 5-6. Clock Output Control Circuit Block Diagram

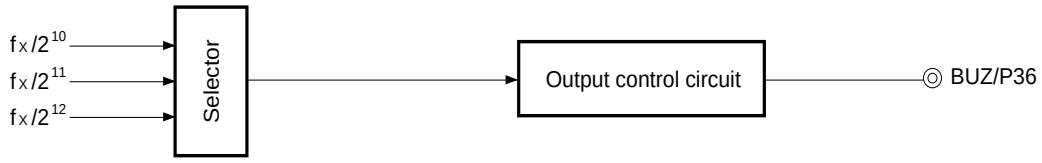


5.5 BUZZER OUTPUT CONTROL CIRCUIT

Clocks of the following frequencies can be output to the buzzer:

- 1.2 kHz/2.4 kHz/4.9 kHz (with main system clock: 5.0 MHz)

Figure 5-7. Buzzer Output Control Circuit Block Diagram



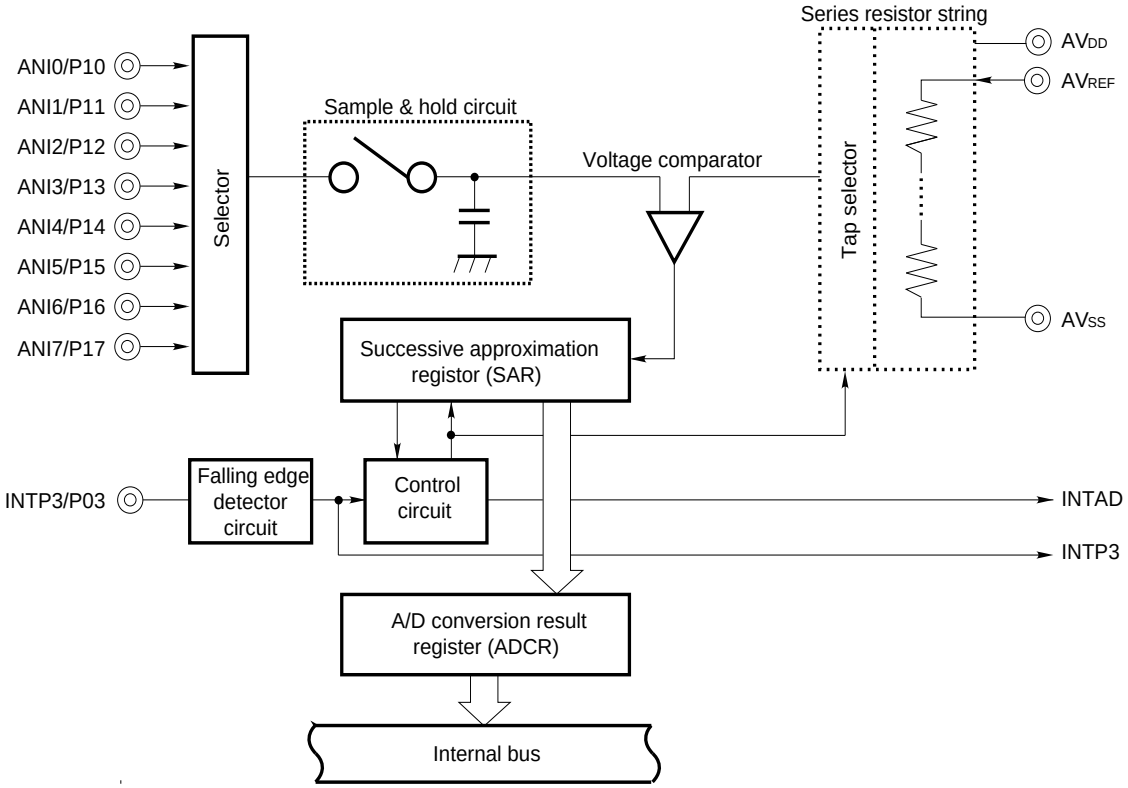
5.6 A/D CONVERTER

An 8-bit resolution 8-channel A/D converter is provided.

This A/D converter can be started in the following two modes:

- Hardware start
- Software start

Figure 5-8. A/D Converter Block Diagram



5.7 SERIAL INTERFACE

Two channels of clocked serial interfaces are provided.

- Serial interface channel 0
- Serial interface channel 1

Table 5-3. Serial Interface Groups and Functions

Function	Serial Interface Channel 0	Serial Interface Channel 1
3-line serial I/O mode	○ (MSB/LSB first selectable)	○ (MSB/LSB first selectable)
SBI (serial bus interface) mode	○ (MSB first)	–
2-line serial I/O mode	○ (MSB first)	–
3-line serial I/O mode w/automatic transfer/reception function	–	○ (MSB/LSB first selectable)

Figure 5-9. Serial Interface Channel 0 Block Diagram

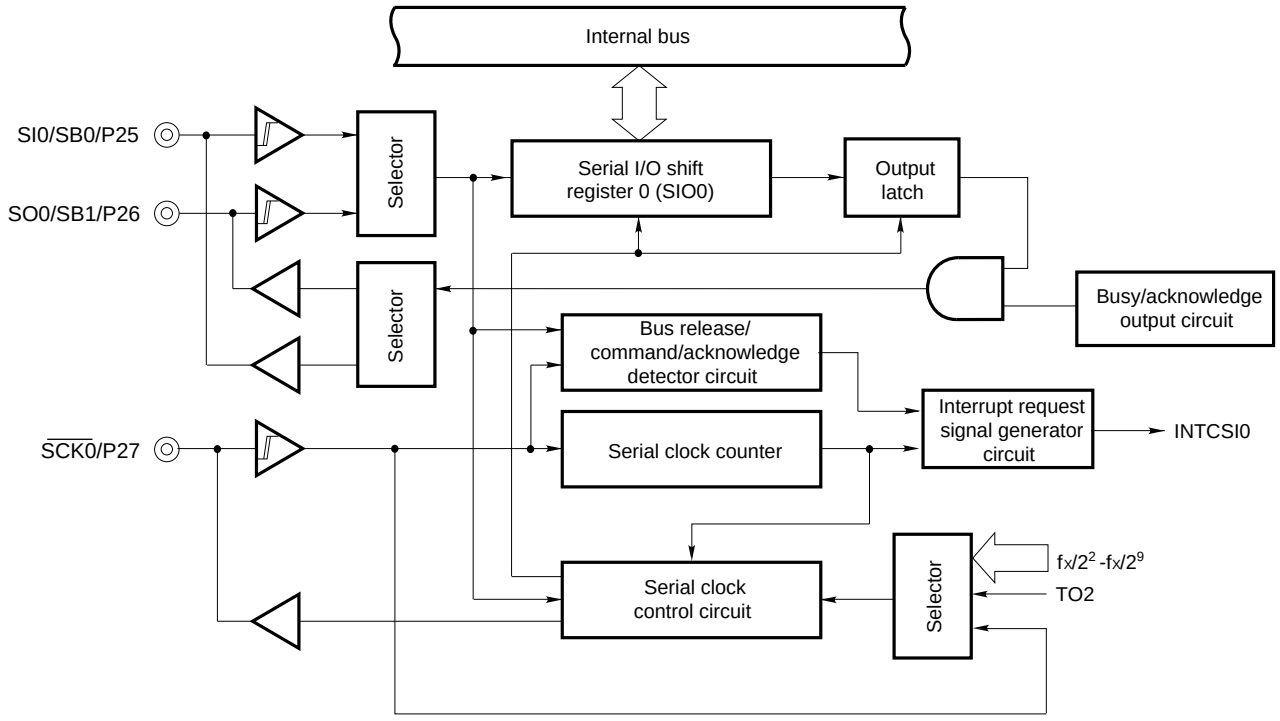
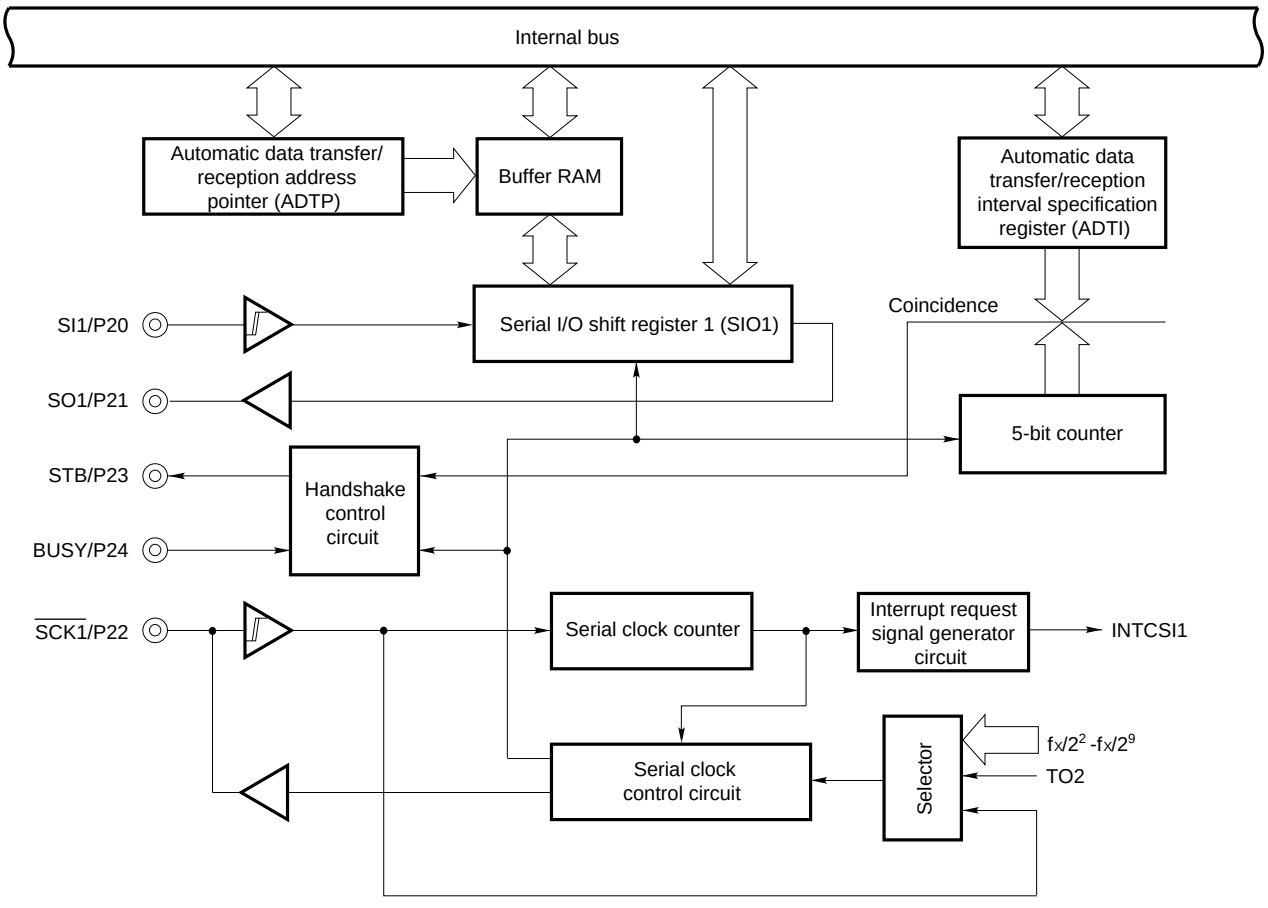


Figure 5-10. Serial Interface Channel 1 Block Diagram

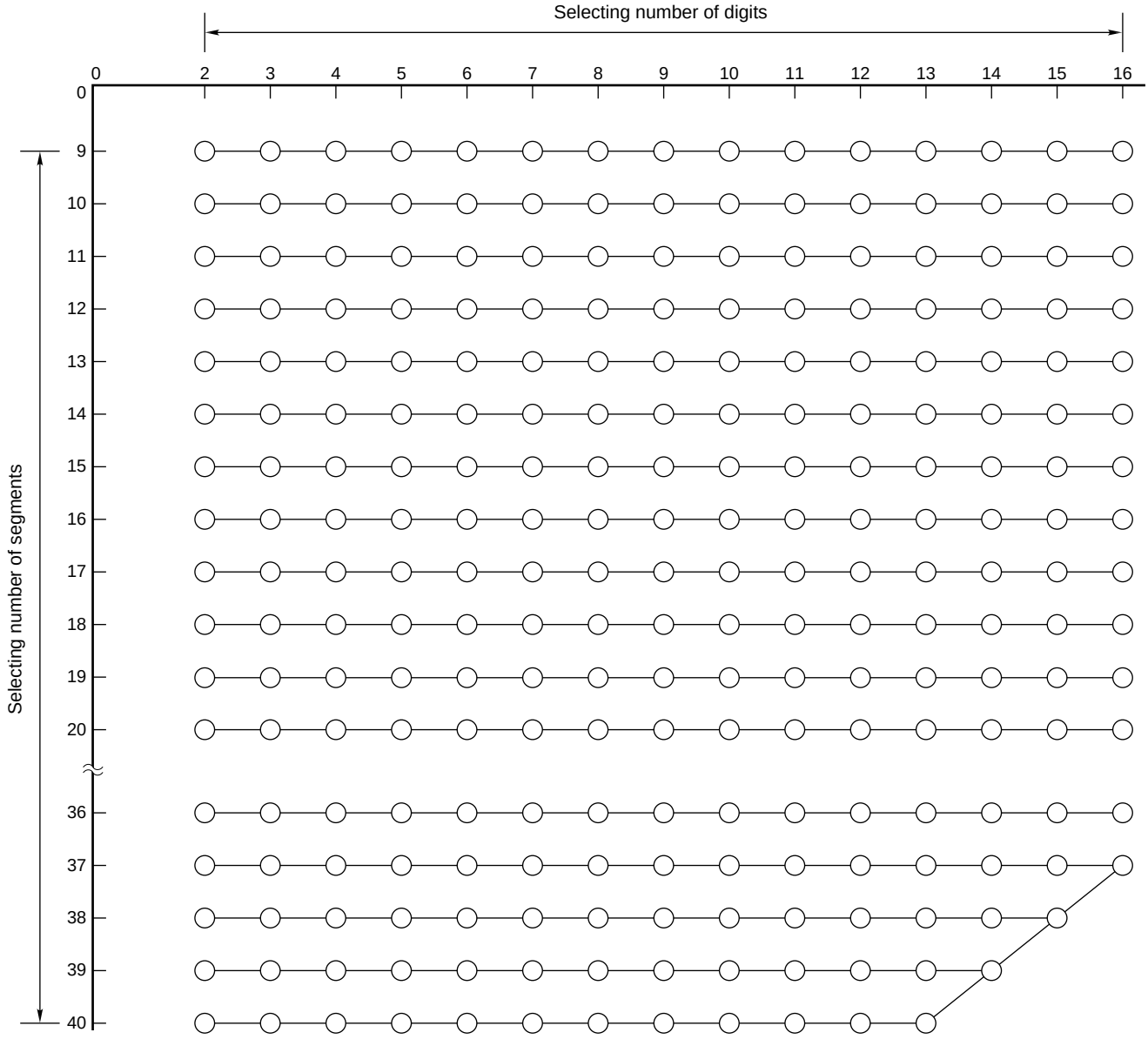


5.8 FIP CONTROLLER/DRIVER

An FIP controller/driver having the following features is provided:

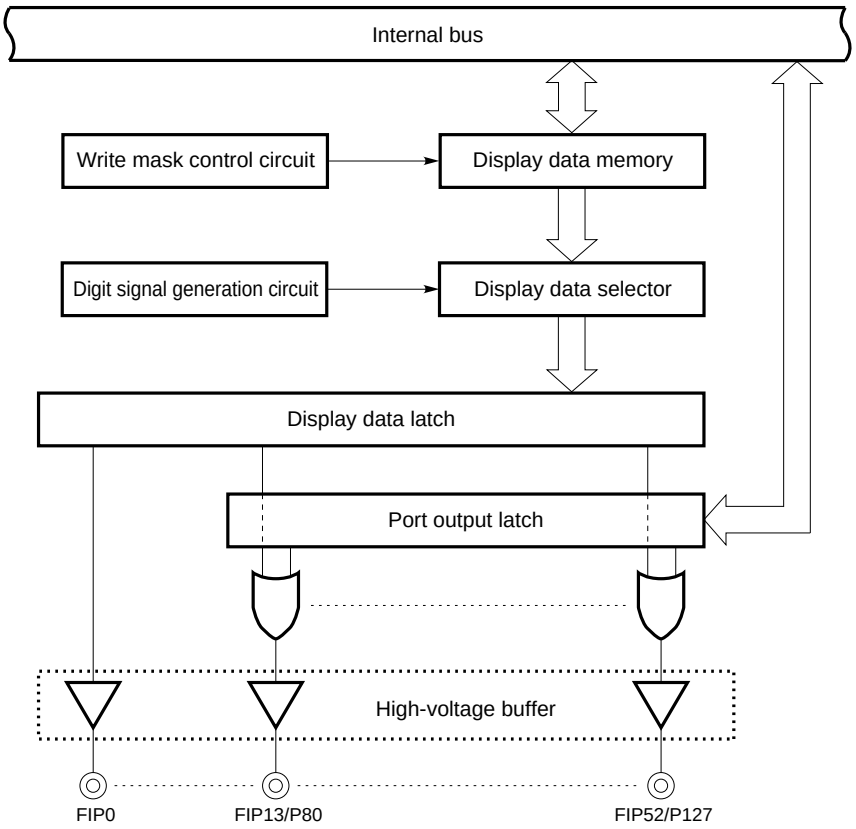
(a) Automatic output of segment signals (DMA operation) and digit signals by automatically reading display data
(b) Display mode register 0-2 (DSPM0-DSPM2) that can control an FIP of 9 to 40 segments and 2 to 16 digits
(c) The output timing of the digit signal can be freely set by selecting the display mode 2 by using the display mode register 0 (DSPM0).
(d) Port pins not used for FIP display can be used as output port or I/O port pins (however, FIP0-FIP12 are display output pins).
(e) Display mode register 1 (DSPM1) can adjust luminance in eight steps.
(f) Hardware suitable for key scan application using segment pins
(g) High-voltage output buffer (FIP driver) that can directly drive an FIP
(h) Display output pins can be connected to a pull-down resistor by mask option.

Figure 5-11. Selecting Display Modes



Caution If the total number of digits and segments exceeds 53, the specified number of digits takes precedence.

Figure 5-12. FIP Controller/Driver Block Diagram



6. INTERRUPT FUNCTION AND TEST FUNCTION

6.1 INTERRUPT FUNCTION

The following three types, 15 sources of interrupt functions are available:

- Non-maskable : 1
- Maskable : 13
- Software : 1

Table 6-1. Interrupt Sources

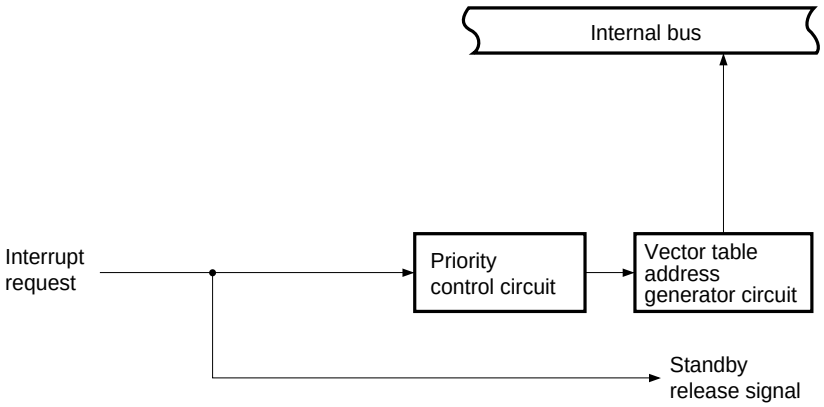
Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	—	INTWDT	Overflow of watchdog timer (when watchdog timer mode 1 is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Overflow of watchdog timer (when interval timer mode is selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	(D)
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTCSI0	End of transfer by serial interface channel 0	Internal	000EH	(B)
	6	INTCSI1	End of transfer by serial interface channel 1		0010H	
	7	INTTM3	Reference time interval signal from watch timer		0012H	
	8	INTTM0	Coincidence signal generation of 16-bit timer/event counter		0014H	
	9	INTTM1	Coincidence signal generation of 8-bit timer/event counter 1		0016H	
	10	INTTM2	Coincidence signal generation of 8-bit timer/event counter 2		0018H	
	11	INTAD	End of conversion by A/D converter		001AH	
	12	INTKS	Key scan timing from FIP controller/ driver		001CH	
Software	—	BRK	Execution of BRK instruction		003EH	(E)

Notes 1. The default priority is assumed when two or more maskable interrupts are generated at the same time, and 0 is the highest and 12 is the lowest.

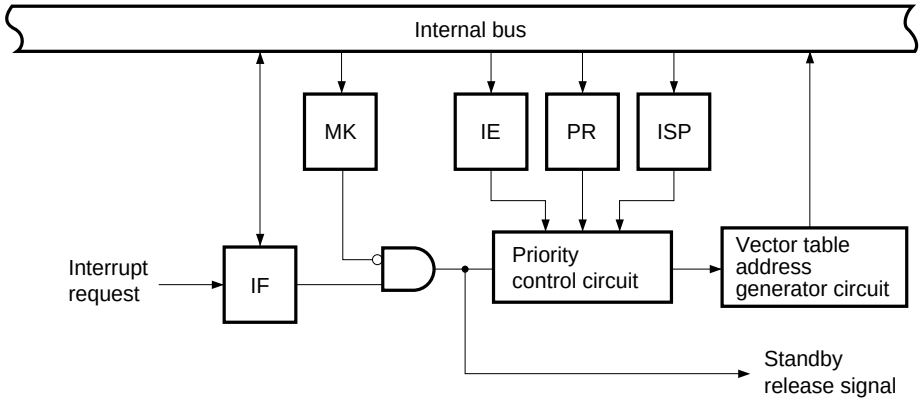
2. Basic configuration types (A)-(E) respectively correspond to (A) to (E) in Figure 6-1.

Figure 6-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0)

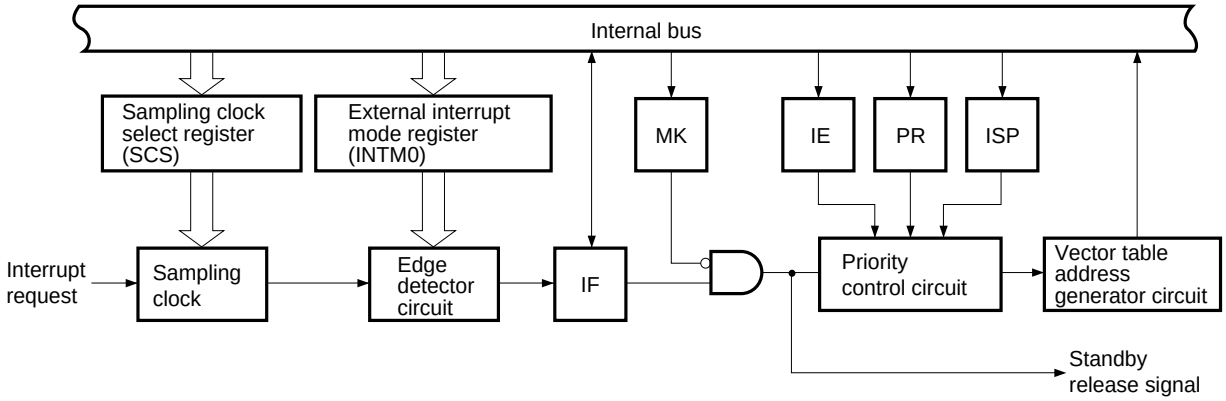
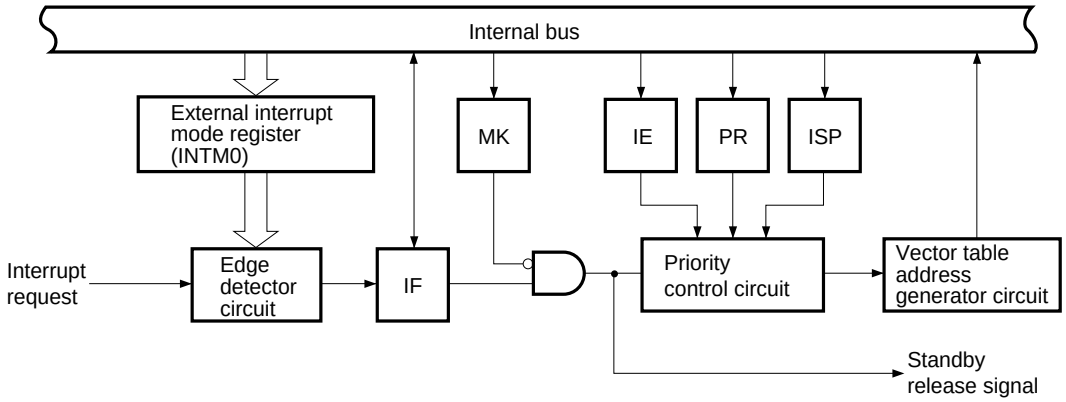
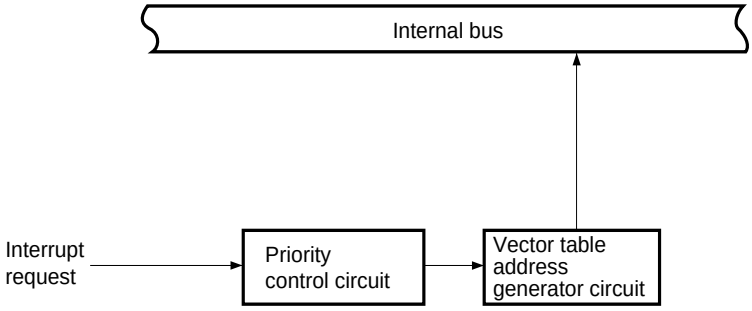


Figure 6-1. Basic Configuration of Interrupt Function (2/2)

(D) External maskable interrupt (except INTP0)



(E) Software interrupt



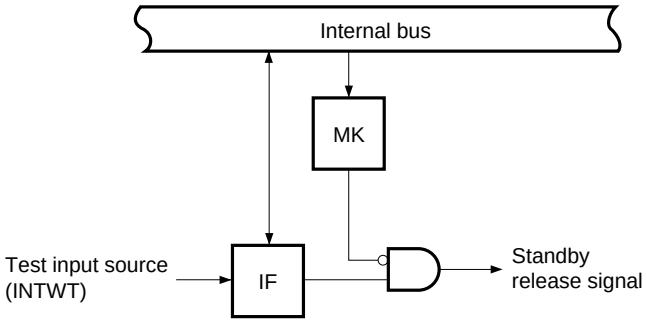
IF : Interrupt request flag
IE : Interrupt enable flag
ISP : In-service priority flag
MK : Interrupt mask flag
PR : Priority specification flag

6.2 TEST FUNCTION

The following trigger is available for test function.

Test Input Source		Internal/ External
Name	Trigger	
INTWT	Overflow of watch timer	Internal

Figure 6-2. Basic Configuration of Test Function



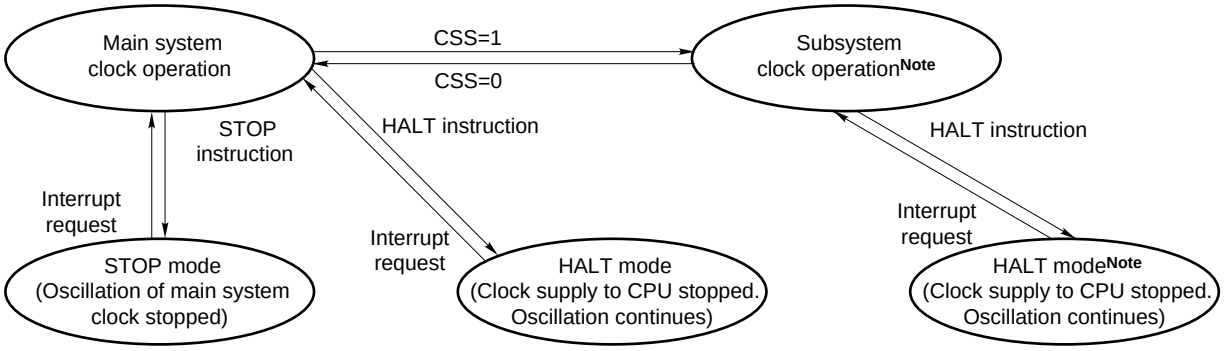
IF : Test request flag
MK : Test mask flag

7. STANDBY FUNCTION

The standby function is to reduce the current dissipation of the system and can be effected in the following two modes:

- HALT mode: In this mode, the operating clock of the CPU is stopped. By using this mode in combination with the normal operation mode, the system can be operated intermittently, so that the average current dissipation can be reduced.
- STOP mode: Oscillation of the main system clock is stopped. All the operations on the main system clock are stopped, and therefore, the current dissipation of the system can be minimized with only the subsystem clock oscillating.

Figure 7-1. Standby Function



Note By stopping the main system clock, the current dissipation can be reduced. When the CPU operates on the subsystem clock, stop the main system clock by setting the MCC. The STOP instruction cannot be used.

Caution To select the main system clock again after the main system clock has been stopped once while the subsystem clock is in use, make sure through the program that the oscillation stabilization time elapses, and then that the main system clock is selected.

8. RESET FUNCTION

The system can be reset in the following two modes:

- External reset by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer that detects hang up

9. INSTRUCTION SET

(1) 8-bit instruction

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

Second Operand / First Operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B,C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except for r=A

(2) 16-bit instruction

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

First Operand \ Second Operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW DECW PUSH POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp=BC, DE, HL

(3) Bit manipulation instruction

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

First Operand \ Second Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call/Branch instruction

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

First Operand \ Second Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic operation	BR	CALL BR	CALLF	CALLT	BR BC BNC BZ BNZ
Compound operation					BT BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

10. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
	V_{LOAD}			V_{DD} –45 to V_{DD} +0.3	V
	AV_{DD}			–0.3 to V_{DD} +0.3	V
	AV_{REF}			–0.3 to V_{DD} +0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P04, P10 to P17 (except analog input pin), P20 to P27, P30 to P37, X1, X2, XT2, $\overline{RESET}$		–0.3 to V_{DD} +0.3	V
	V_{I2}	P70 to P74	N-ch open drain	–0.3 to +16 **Note 1**	V
	V_{I3}	P100 to P107, P110 to P117, P120 to P127	P-ch open drain	V_{DD} –45 to V_{DD} +0.3	V
Output voltage	V_{O1}	P01 to P03, P10 to P17, P20 to P27, P30 to P37		–0.3 to V_{DD} +0.3	V
	V_{O2}	P70 to P74		–0.3 to +16 **Note 1**	V
	V_{OD}	P80 to P87, P90 to P97, P100 to P107, P110 to P117, P120 to P127, FIP0 to FIP12		V_{DD} –45 to V_{DD} +0.3	V
Analog input voltage	V_{AN}	ANI0 to ANI7	Analog input pins	AV_{SS} –0.3 to AV_{REF} +0.3	V
High-level output current	I_{OH}	1 pin of P01 to P03, P10 to P17, P20 to P27, P30 to P37		–10	mA
		Total for P01 to P03, P10 to P17, P20 to P27, P30 to P37		–30	mA
		1 pin of P80 to P87, P90 to P97, P100 to P107, P110 to P117, P120 to P127, FIP0 to FIP12		–30	mA
		Total for P80 to P87, FIP0 to FIP12	Peak value	–240	mA
			RMS	–120 **Note 2**	mA
		Total for P90 to P97, P100 to P107, P110 to 117, P120 to P127	Peak value	–100	mA
			RMS	–60 **Note 2**	mA
Low-level output current	I_{OL}	1 pin of P01 to P03, P10 to P17, P20 to P27, P30 to P37, P70 to P74	Peak value	30	mA
			RMS	15 **Note 2**	mA
		Total for P70 to P74	Peak value	100	mA
			RMS	60 **Note 2**	mA
		Total for P01 to P03, P10 to17, P20 to 27, P30 to P37	Peak value	50	mA
			RMS	20 **Note 2**	mA
Total power dissipation	P_T **Note 3**	T_A = –40 to +60 °C		800	mW
				600	mW
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

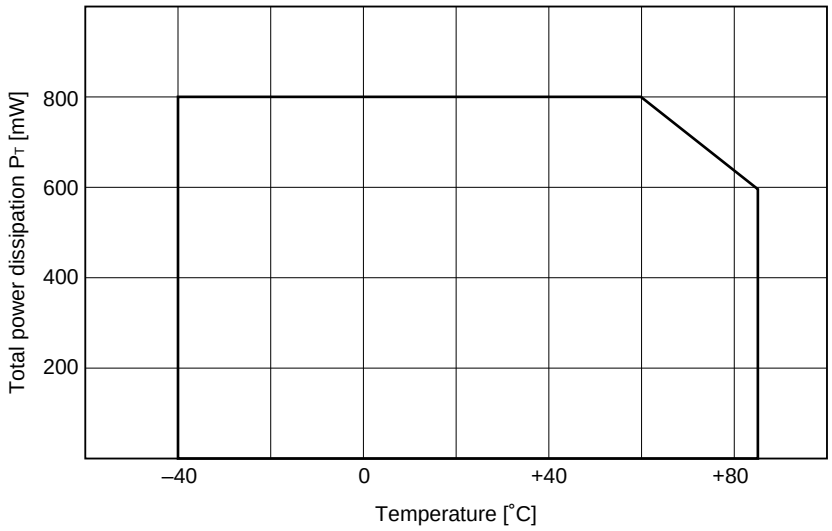
Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter, or even momentarily. In other words, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, dual-function pin characteristics are the same as port pin characteristics.

Notes 1. With the mask option, the range of the internal pull-up resistor pin is 0.3 to V_{DD} +0.3.

2. The RMS should be calculated as follows: [RMS] = [Peak value] × $\sqrt{\text{Duty}}$

Notes 3. Total power dissipation differs depending on the temperature (see the following figure).



★ **How to calculate total power dissipation**

The following three power dissipation are available for the μPD780204, 780205, 780206, and 780208. The sum of the three power dissipation should be less than the total power dissipation P_T (80 % or less of ratings is recommended).

<1> CPU power dissipation: calculate V_{DD} (MAX.) × I_{DD1} (MAX.).

<2> Output pin power dissipation: Normal output and display output are available. Power dissipation when maximum current flows into each output.

<3> Pull-down resistor power dissipation: Power dissipation by pull-down resistor incorporated in display output pin by mask option.

The following is how to calculate total power dissipation for the example in the next page.

Example Assume the following conditions:

V_{DD} = 5 V ± 10 %, 5.0 MHz oscillator

Supply current (I_{DD}) = 21.6 mA

Display output: 11 grids × 10 segments (Cut width = 1/16)
Maximum current at the grid pin is 15 mA.
Maximum current at the segment pin is 3 mA.
At the key scan timing, display output pin is OFF.

Display output voltage: grid $V_{OD} = V_{DD}$ – 2 V (voltage drop of 2 V)
segments $V_{OD} = V_{DD}$ – 0.4 V (voltage drop of 0.4 V)

Fluorescent display control voltage (V_{LOAD}) = –35 V

Mask option pull-down resistor = 25 kΩ

By placing the above conditions in calculation <1> to <3>, the total dissipation can be worked out.

<1> CPU power dissipation: $5.5\ V \times 21.6\ mA = 118.8\ mW$

<2> Output pin power dissipation:

Grid $(V_{DD} - V_{OD}) \times \dfrac{\text{Total current value of each grid}}{\text{The number of grids} + 1} \times \text{Digit width}\ (1 - \text{Cut width})$

$$= 2\ V \times \frac{15\ mA \times 11\ Grids}{11\ Grids + 1} \times \left(1 - \frac{1}{16}\right) = 25.8\ mW$$

Segment $(V_{DD} - V_{OD}) \times \dfrac{\text{Total segment current value of illuminated dots}}{\text{The number of grids} + 1}$

$$= 0.4\ V \times \frac{3\ mA \times 31\ Dots}{11\ Grids + 1} = 3.1\ mW$$

<3> Pull-down resistor power dissipation:

Grid $\dfrac{(V_{OD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \dfrac{\text{The number of grids}}{\text{The number of grids} + 1} \times \text{Digit width}$

$$= \frac{(5.5\ V - 2\ V - (-35\ V))^2}{25\ k\Omega} \times \frac{11\ Grids}{11\ Grids + 1} \times \left(1 - \frac{1}{16}\right) = 50.9\ mW$$

Segment $\dfrac{(V_{OD} - V_{LOAD})^2}{\text{Pull-down resistor value}} \times \dfrac{\text{The number of illuminated dots}}{\text{The number of grids} + 1}$

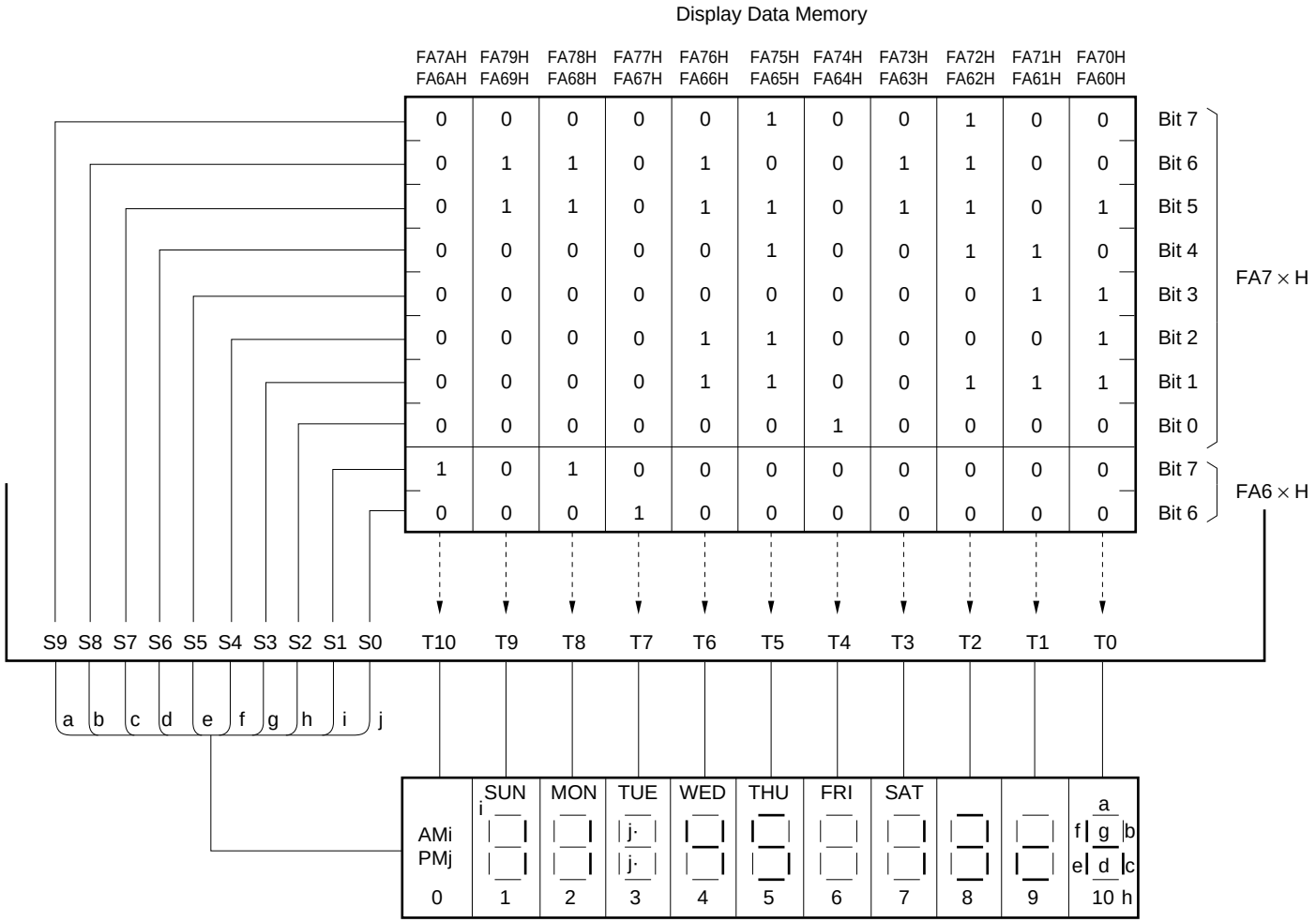
$$= \frac{(5.5\ V - 0.4\ V - (-35\ V))^2}{25\ k\Omega} \times \frac{31\ dots}{11\ Grids + 1} = 166.1\ mW$$

Total power dissipation = <1> + <2> + <3> = 118.8 + 25.8 + 3.1 + 50.9 + 166.1 = 364.7 mW

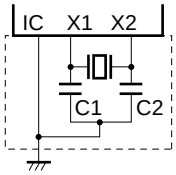
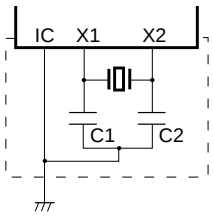
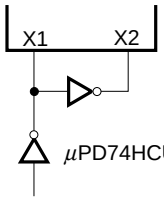
In this example, the total power dissipation do not exceed the rating of the total power dissipation, so there is no problem in power dissipation.

However, when the total power dissipation exceeds the rating of the total power dissipation, it is necessary to lower the power dissipation. To reduce power dissipation, reduce the number of pull-down resistor.

Figure 10-1 Display Example of 10 segments-11 digits



MAIN SYSTEM CLOCK OSCILLATION CIRCUIT CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (f_X)**Note 1**		1		5	MHz
		Oscillator stabilization time**Note 2**				4	ms
Crystal resonator		Oscillator frequency (f_X)**Note 1**		1	4.19	5	MHz
		Oscillator stabilization time**Note 2**	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X)**Note 1**		1		5	MHz
		X1 input high-/low-level width (t_{XH}/t_{XL})		85		500	ns

Notes 1. Only the oscillator characteristics are shown. See **AC CHARACTERISTICS** for instruction execution times.

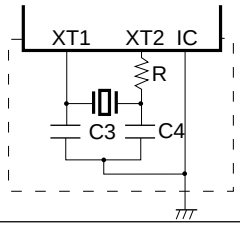
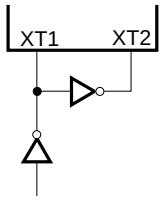
2. This is the time required for oscillation to stabilize after reset, or STOP mode release.

Cautions 1. When the main system clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a broken line to prevent the influence of wiring capacitance, etc.

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as V_{SS}.**
- **Do not connect to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillator frequency (f_{XT})**Note 1**		32	32.768	35	kHz
		Oscillator stabilization time**Note 2**	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	
★ External clock		XT1 input frequency (f_{XT})**Note 1**		32		100	kHz
		XT1 input high-/low-level width (t_{XTH}/t_{XTL})		5		15	μs

Notes 1. Only the oscillator characteristics are shown. See **AC CHARACTERISTICS** for instruction execution times.

2. This is the time required for oscillation to stabilize after V_{DD} reaches MIN. in the range of oscillation voltage.

Cautions 1. When the subsystem clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a broken line to prevent the influence of wiring capacitance, etc.

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as V_{SS}.**
- **Do not connect to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

2. The subsystem clock oscillator is a low-amplitude circuit in order to achieve a low consumption current, and is more prone to misoperation due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

★ RECOMMENDED OSCILLATOR CONSTANT

(1) μPD780204, 780205

Main System Clock: Ceramic Resonator (T_A = –40 to +85 °C)

Manufacturer	Product Name	Frequency (MHz)	Circuit Constant		Oscillator Voltage Range		Remark
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
Murata Mfg. Co., Ltd.	CSB1000J	1.0	100	100	3.00	5.50	
Toyama	CSA2.00MG040	2.0	100	100	2.80	5.50	
	CST2.00MG040	2.0	—	—	2.80	5.50	Built-in capacitor
	CSA4.00MG	4.0	30	30	2.70	5.50	
	CST4.00MGW	4.0	—	—	2.70	5.50	Built-in capacitor
	CSA5.00MG	5.0	30	30	2.90	5.50	
	CST5.00MGW	5.0	—	—	2.90	5.50	Built-in capacitor
TDK Corp.	CCR1000K2	1.0	150	150	2.70	5.50	
	FCR4.00MC5	4.0	—	—	2.70	5.50	Built-in capacitor
	CCR4.00MC3	4.0	—	—	2.70	5.50	Built-in capacitor
	FCR5.00MC5	5.0	—	—	2.80	5.50	Built-in capacitor
	CCR5.00MC3	5.0	—	—	2.70	5.50	Built-in capacitor
Matsushita Electronics	EFOEC5004A4	5.0	—	—	2.70	5.50	Built-in capacitor
Components Co., Ltd.	EFOEN5004A4	5.0	33	33	2.70	5.50	
	EFOS5004B5	5.0	—	—	2.70	5.50	Built-in capacitor

Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation. However, they do not guarantee accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency in the application circuit. For this, it is necessary to directly contact the manufacturer of the resonator being used.

(2) μPD780206, 780208

Main System Clock: Ceramic Resonator (T_A = –40 to +85 °C)

Manufacturer	Product Name	Frequency (MHz)	Circuit Constant		Oscillator Voltage Range		Remark
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
Murata Mfg. Co., Ltd.	CSB1000J	1.0	100	100	2.80	5.50	
Toyama	CSA2.00MG040	2.0	100	100	2.70	5.50	
	CST2.00MG040	2.0	—	—	2.70	5.50	Built-in capacitor
	CSA4.00MG	4.0	30	30	2.70	5.50	
	CST4.00MGW	4.0	—	—	2.70	5.50	Built-in capacitor
	CSA5.00MG	5.0	30	30	2.70	5.50	
	CST5.00MGW	5.0	—	—	2.70	5.50	Built-in capacitor
TDK Corp.	CCR1000K2	1.0	220	220	2.70	5.50	
	CCR2.0MC33	2.0	—	—	2.70	5.50	Built-in capacitor
	CCR4.0MC3	4.0	—	—	2.70	5.50	Built-in capacitor
	FCR4.0MC5	4.0	—	—	2.70	5.50	Built-in capacitor
	CCR4.19MC3	4.19	—	—	2.70	5.50	Built-in capacitor
	FCR4.19MC5	4.19	—	—	2.70	5.50	Built-in capacitor
	CCR5.0MC3	5.0	—	—	2.70	5.50	Built-in capacitor
	FCR5.0MC5	5.0	—	—	2.70	5.50	Built-in capacitor
Matsushita Electronics	EFOEC2004A5	2.0	33	33	2.70	5.50	
Components Co., Ltd.	EFOEC4004A4	4.0	33	33	2.85	5.50	
	EFOEC4194A4	4.19	33	33	2.70	5.50	
	EFOEC5004A4	5.0	33	33	2.70	5.50	

Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation. However, they do not guarantee accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency in the application circuit. For this, it is necessary to directly contact the manufacturer of the resonator being used.

CAPACITANCE (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V				15	pF
Output capacitance	C_{OUT}	f = 1 MHz Unmeasured pins returned to 0 V				35	pF
Input/output capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V	P01 to P03, P10 to P17, P20 to P27, P30 to P37			15	pF
			P70 to P74			20	pF
			P100 to P107, P110 to P117, P120 to P127			35	pF

Remark Unless otherwise specified, the characteristics of the shared pin are the same as the characteristics of the port pin.

POWER SUPPLY VOLTAGE (T_A = –40 to +85 °C)

Parameter	Conditions	MIN.	TYP.	MAX.	Unit
CPU[Note 1]		2.7[Note 2]		5.5	V
Display controller/driver		4.5		5.5	V
PWM mode of 16-bit time/event counter (TM0)		4.5		5.5	V
A/D converter		4.0		5.5	V
Other hardware		2.7		5.5	V

Notes 1. Except for system clock oscillator, display controller/driver, and PWM.

2. Operating power supply voltage range differs depending on the cycle time. See **AC CHARACTERISTICS**.

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level input voltage	V_{IH1}	P21, P23		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P03, P20, P22, P24 to P27, P33, P34, $\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	P70 to P74	N-ch open-drain	0.7 V_{DD}		15	V
	V_{IH4}	X1, X2		V_{DD} – 0.5		V_{DD}	V
	V_{IH5}	XT1/P04, XT2	V_{DD} = 4.5 to 5.5 V	0.8 V_{DD}		V_{DD}	V
				0.9 V_{DD}		V_{DD}	V
	V_{IH6}	P10 to P17, P30 to P32,	V_{DD} = 4.5 to 5.5 V	0.65 V_{DD}		V_{DD}	V
		P35 to P37		0.7 V_{DD}		V_{DD}	V
	V_{IH7}	P100 to P107, P110 to P117,	V_{DD} = 4.5 to 5.5 V	0.7 V_{DD}		V_{DD}	V
		P120 to P127		V_{DD} – 0.5		V_{DD}	V
Low-level input voltage	V_{IL1}	P21, P23		0		0.3 V_{DD}	V
	V_{IL2}	P00 to P03, P20, P22, P24 to P27, P33, P34, $\overline{\text{RESET}}$		0		0.2 V_{DD}	V
	V_{IL3}	P70 to P74	V_{DD} = 4.5 to 5.5 V	0		0.3 V_{DD}	V
				0		0.2 V_{DD}	V
	V_{IL4}	X1, X2		0		0.4	V
	V_{IL5}	XT1/P04, XT2	V_{DD} = 4.5 to 5.5 V	0		0.2 V_{DD}	V
				0		0.1 V_{DD}	V
	V_{IL6}	P10 to P17, P30 to P32, P35 to P37		0		0.3 V_{DD}	V
	V_{IL7}	P100 to P107, P110 to P117, P120 to P127		V_{DD} – 40		0.3 V_{DD}	V
High-level output voltage	V_{OH}	P01 to P03, P10 to P17, P20 to P27, P30 to P37, P80 to P87, P90 to P97, P100 to P107, P110 to P117, P120 to P127, FIP0 to FIP12	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA	V_{DD} – 1.0			V
			I_{OH} = –100 μA	V_{DD} – 0.5			V
Low-level output voltage	V_{OL1}	P30 to P37, P70 to P74	V_{DD} = 4.5 to 5.5 V I_{OL} = 15 mA		0.4	2.0	V
		P01 to P03, P10 to P17, P20 to P27	V_{DD} = 4.5 to 5.5 V I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V_{DD} = 4.5 to 5.5 V With open-drain and pull-up (R = 1 kΩ)			0.2 V_{DD}	V
	V_{OL3}		I_{OL} = 400 μA			0.5	V

Remark Unless otherwise specified, the characteristics of a shared pin are the same as those of a port pin.

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-level input leakage current	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P03, P10 to P17, P20 to P27, P30 to P37, P70 to P74, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2, XT1/P04, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P70 to P74			80	μA
	I_{LIH4}	P100 to P107, P110 to P117,	V_{DD} = 4.5 to 5.5 V			3 Note 1	μA
		P120 to P127 $V_{IN} = V_{DD}$				3 Note 2	μA
Low-level input leakage current	I_{LIL1}	V_{IN} = 0 V	P00 to P03, P10 to P17, P20 to P27, P30 to P37, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2, XT1/P04 XT2			–20	μA
	I_{LIL3}		P70 to P74			–3 Note 3	μA
	I_{LIL4}		P100 to P107, P110 to P117, P120 to P127			–10	μA
High-level output leakage current Note 4	I_{LOH1}	$V_{OUT} = V_{DD}$	P01 to P03, P10 to P17, P20 to P27, P30 to P37, P80 to P87, P90 to P97, P100 to P107, P110 to P117, P120 to P127, FIP0 to FIP12			3	μA
	I_{LOH2}	V_{OUT} = 15 V	P70 to P74, N-ch open-drain			80	μA
Low-level output leakage current Note 4	I_{LOL1}	V_{OUT} = 0 V	P01 to P03, P10 to P17, P20 to P27, P30 to P37, P70 to P74			–3	μA
	I_{LOL2}	$V_{OUT} = V_{LOAD} = V_{DD}$ – 40 V	P80 to P87, P90 to P97, P100 to 107, P110 to P117, P120 to P127, FIP0 to FIP12			–10	μA
Display output current	I_{OD}	V_{DD} = 4.5 to 5.5 V, $V_{OD} = V_{DD}$ – 2 V		–15	–18		mA
Mask option pull-up resistor	R_1	V_{IN} = 0 V, P70 to P74		20	40	90	kΩ
Software pull-up resistor	R_2	V_{IN} = 0 V, P01 to P03, P10 to P17, P20 to P27, P30 to P37	V_{DD} = 4.5 to 5.5 V	15	40	90	kΩ
				20		500	kΩ

Notes 1. For P110 to P117 and P120 to P127 without on-chip pull-down resistor (specifiable by mask option), a high-level input leak current of 50 μA (MAX.) flows only during the 1.5 clocks after an instruction has been executed to read out ports 11, 12 (P11, P12) or port mode registers 11, 12 (PM11, PM12). Outside the period of 1.5 clocks following executing a read-out instruction, the current is 3 μA (MAX.).

2. For P110 to P117 and P120 to P127 without on-chip pull-down resistor (specifiable by mask option), a high-level input leak current of 30 μA (MAX.) flows only during the 1.5 clocks after an instruction has been executed to read out P11, P12, PM11, and PM12. Outside the period of 1.5 clocks following executing a read-out instruction, the current is 3 μA (MAX.).

3. For P70 to P74 without on-chip pull-up resistor (specifiable by mask option), a low-level input leak current of –200 μA (MAX.) flows only during the 1.5 clocks after an instruction has been executed to read out port 7 (P7) or port mode register 7 (PM7). Outside the period of 1.5 clocks following executing a read-out instruction, the current is –3 μA (MAX.).

4. This current excludes the current which flows in the on-chip pull-up/pull-down resistor.

Remark Unless otherwise specified, the characteritics of a shared pin are the same as those of a port pin.

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Mask option pull-down resistor	R_3	P80 to P87, P90 to P97, P100 to P107, P110 to P117, P120 to P127	$V_{OD} - V_{LOAD}$ = 40 V	25	70	135	kΩ
			$V_{OD} - V_{SS}$ = 5 V	20	55	100	kΩ
	R_4	P30 to P37, $V_{IN} = V_{DD}$		40	80	150	KΩ
Power supply current Note 1	I_{DD1}	5.0 MHz crystal oscillation operating mode	V_{DD} = 5.0 V ± 10 % Note 2		7.2	21.6	mA
			V_{DD} = 3.0 V ± 10 % Note 3		0.9	2.7	mA
	I_{DD2}	5.0 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ± 10 %		1.6	4.8	mA
			V_{DD} = 3.0 V ± 10 %		650	1950	μA
	I_{DD3}	32.768 kHz crystal oscillation operating mode Note 4	V_{DD} = 5.0 V ± 10 %		60	120	μA
			V_{DD} = 3.0 V ± 10 %		32	64	μA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode Note 4	V_{DD} = 5.0 V ± 10 %		25	55	μA
			V_{DD} = 3.0 V ± 10 %		5	15	μA
	I_{DD5}	XT1 = 0 V in STOP mode when connecting to feedback resistor	V_{DD} = 5.0 V ± 10 %		1	30	μA
			V_{DD} = 3.0 V ± 10 %		0.5	10	μA
	I_{DD6}	XT1 = 0 V in STOP mode when not connecting to feedback resistor	V_{DD} = 5.0 V ± 10 %		0.1	30	μA
			V_{DD} = 3.0 V ± 10 %		0.05	10	μA

Notes 1. This current excludes the AV_{REF} current, port current, and current which flows in the on-chip pull-down resistor (mask option).

2. When operating at high-speed mode (when the processor clock control register (PCC) is set to 00H)

3. When operating at low-speed mode (when the PCC is set to 04H)

4. When main system clock stopped.

AC CHARACTERISTICS

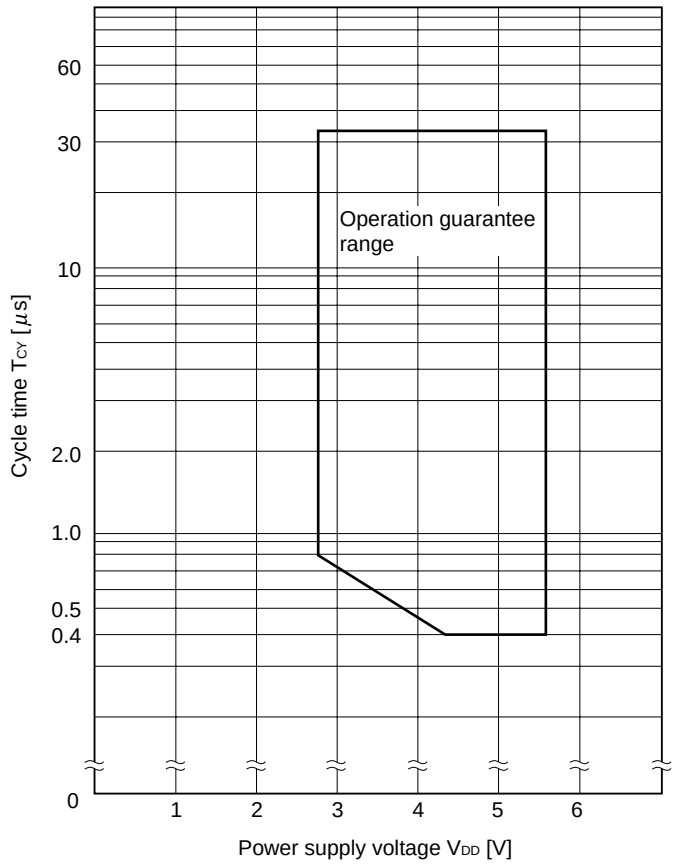
(1) Basic Operation (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operated with main system clock	V_{DD} = 4.5 to 5.5 V	0.4		32	μs
				0.8		32	μs
★		Operated with subsystem clock		40 Note 1	122	125	μs
TI1, TI2 input frequency	f_{TI}	V_{DD} = 4.5 to 5.5 V		0		2	MHz
				0		138	kHz
TI1, TI2 input high, low-level width	f_{TIH}	V_{DD} = 4.5 to 5.5 V		250			ns
	f_{TIL}			3.6			μs
Interrupt input high, low-level width	f_{INTH}	INTP0		$8/f_{sam}$ Note 2			μs
	f_{INTL}	INTP1 to INTP3		10			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

Notes 1. Value when external clock input is used as subsystem clock. When crystal is used, the value becomes 114 μs.

2. Selection of $f_{sam} = fx/2^{N+1}$, fx/64, fx/128 is available (N = 0 to 4) by bits 0 and 1 (SCS0, SCS1) of sampling clock select register (SCS).

T_{CY} vs. V_{DD} (with main system clock operated)



(2) Serial Interface (T_A = –40 to +85 °C, V_{DD} = 2.7 to 5.5 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$: Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK0}$ high, low-level width	t_{KH1}	V_{DD} = 4.5 to 5.5 V	$t_{KCY1}/2 - 50$			ns
	t_{KL1}		$t_{KCY1}/2 - 100$			ns
SI0 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK1}	V_{DD} = 4.5 to 5.5	100			ns
			150			ns
SI0 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI1}		400			ns
$\overline{SCK0}\downarrow\rightarrow$ SO0 output delay time	t_{KSO1}	C = 100 pF**Note**			300	ns

Note C is a load capacitance of the $\overline{SCK0}$ or SO0 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$: External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK0}$ high, low-level width	t_{KH2}	V_{DD} = 4.5 to 5.5 V	$t_{KCY2}/2 - 50$			ns
	t_{KL2}		$t_{KCY2}/2 - 100$			ns
SI0 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK2}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI0 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI2}		400			ns
$\overline{SCK0}\downarrow\rightarrow$ SO0 output delay time	t_{KSO2}	C = 100 pF**Note**			300	ns
$\overline{SCK0}$ rise, fall time	t_{R2} t_{F2}				160	ns

Note C is a load capacitance of the SO0 output line.

(iii) SBI mode ($\overline{SCK0}$: Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high, low-level width	t_{KH3}	V_{DD} = 4.5 to 5.5 V		$t_{KCY3}/2 - 50$			ns
	t_{KL3}			$t_{KCY3}/2 - 150$			ns
SB0, SB1 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK3}	V_{DD} = 4.5 to 5.5 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI3}			$t_{KCY3}/2$			ns
$\overline{SCK0}\downarrow\rightarrow$ SB0, SB1 output delay time	t_{KSO3}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	0		250	ns
				0		1000	ns
$\overline{SCK0}\uparrow\rightarrow$SB0, SB1$\downarrow$	t_{KSB}			t_{KCY3}			ns
SB0, SB1$\downarrow\rightarrow\overline{SCK0}\downarrow$	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R is a load resistance and C is a load capacitance of the $\overline{SCK0}$, SB0, or SB1 output line.

(iv) SBI mode ($\overline{SCK0}$: External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 5.5 V		800			ns
				3200			ns
$\overline{SCK0}$ high, low-level width	t_{KH4}	V_{DD} = 4.5 to 5.5 V		400			ns
	t_{KL4}			1600			ns
SB0, SB1 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK4}	V_{DD} = 4.5 to 5.5 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI4}			$t_{KCY4}/2$			ns
$\overline{SCK0}\downarrow\rightarrow$ SB0, SB1 output delay time	t_{KSO4}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	0		250	ns
				0		1000	ns
$\overline{SCK0}\uparrow\rightarrow$SB0, SB1$\downarrow$	t_{KSB}			t_{KCY4}			ns
SB0, SB1$\downarrow\rightarrow\overline{SCK0}\downarrow$	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{SCK0}$ rise, fall time	t_{R4} t_{F4}					160	ns

Note R is a load resistance and C is a load capacitance of the SB0 or SB1 output line.

(v) 2-wire serial I/O mode ($\overline{SCK0}$: Internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF[Note]		1600			ns
$\overline{SCK0}$ high-level width	t_{KH5}			$t_{KCY5}/2 - 160$			ns
$\overline{SCK0}$ low-level width	t_{KL5}		V_{DD} = 4.5 to 5.5 V	$t_{KCY5}/2 - 50$			ns
				$t_{KCY5}/2 - 100$			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK5}		V_{DD} = 4.5 to 5.5 V	300			ns
				350			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI5}			600			ns
$\overline{SCK0}$↓→SB0, SB1 output delay time	t_{KSO5}			0		300	ns

Note R is a load resistance and C is a load capacitance of the $\overline{SCK0}$, SB0, or SB1 output line.

(vi) 2-wire serial I/O mode ($\overline{SCK0}$: External clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}			1600			ns
$\overline{SCK0}$ high-level width	t_{KH6}			650			ns
$\overline{SCK0}$ low-level width	t_{KL6}			800			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK6}			100			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI6}			$t_{KCY6}/2$			ns
$\overline{SCK0}$↓→SB0, SB1 output delay time	t_{KSO6}	R = 1 kΩ, C = 100 pF[Note]	V_{DD} = 4.5 to 5.5 V	0		300	ns
				0		500	ns
$\overline{SCK0}$ rise, fall time	t_{R6} t_{F6}					160	ns

Note R is a load resistance and C is a load capacitance of the SB0 or SB1 output line.

(b) Serial interface channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$: Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY7}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK1}$ high, low-level width	t_{KH7}	V_{DD} = 4.5 to 5.5 V	$t_{KCY7}/2 - 50$			ns
	t_{KL7}		$t_{KCY7}/2 - 100$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK7}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI7}		400			ns
$\overline{SCK1}\downarrow\rightarrow$ SO1 output delay time	t_{KSO7}	C = 100 pF[Note]			300	ns

Note C is a load capacitance of the $\overline{SCK1}$ or SO1 output line.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$: External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY8}	V_{DD} = 4.5 to 5.5 V	800			ns
★			1600			ns
★ $\overline{SCK1}$ high, low-level width	t_{KH8}	V_{DD} = 4.5 to 5.5 V	$t_{KCY8}/2-50$			ns
★	t_{KL8}		$t_{KCY8}/2-100$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK8}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI8}		400			ns
$\overline{SCK1}\downarrow\rightarrow$ SO1 output delay time	t_{KSO8}	C = 100 pF[Note]			300	ns
$\overline{SCK1}$ rise, fall time	t_{R8}				160	ns
	t_{F8}					

Note C is a load capacitance of the SO1 output line.

(iii) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$: Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY9}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
★ $\overline{SCK1}$ high, low-level width	t_{KH9}	V_{DD} = 4.5 to 5.5 V	$t_{KCY9}/2 - 50$			ns
	t_{KL9}		$t_{KCY9}/2 - 100$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK9}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI9}		400			ns
$\overline{SCK1}\downarrow \rightarrow$ SO1 output delay time	t_{KSO9}	C = 100 pF[Note]			300	ns
$\overline{SCK1}\downarrow \rightarrow$ STB$\uparrow$	t_{SBD}		$t_{KCY9}/2 - 100$		$t_{KCY9}/2 + 100$	ns
Strobe signal high-level width	t_{SBW}		$t_{KCY9} - 30$		$t_{KCY9} + 30$	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing	t_{BYH}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
Busy inactibe $\rightarrow$ $\overline{SCK1}\downarrow$	t_{SPS}				$2t_{KCY9}$	ns

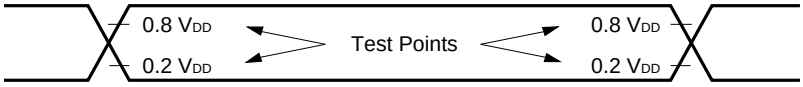
Note C is a load capacitance of the $\overline{SCK1}$ or SO1 output line.

(iv) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK1}$: External clock input)

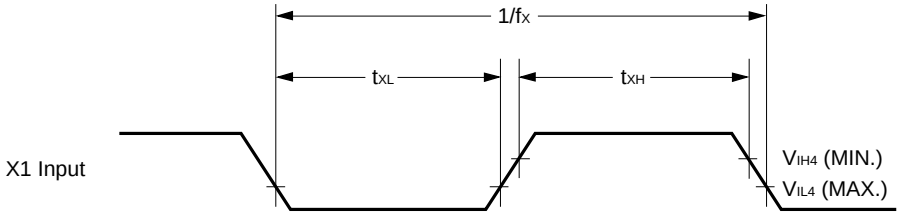
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY10}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK1}$ high, low-level width	t_{KH10}	V_{DD} = 4.5 to 5.5 V	400			ns
	t_{KL10}		800			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK10}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI10}		400			ns
$\overline{SCK1}\downarrow \rightarrow$ SO1 output delay time	t_{KSO10}	C = 100 pF[Note]			300	ns
$\overline{SCK1}$ rise, fall time	t_{R10} t_{F10}				160	ns

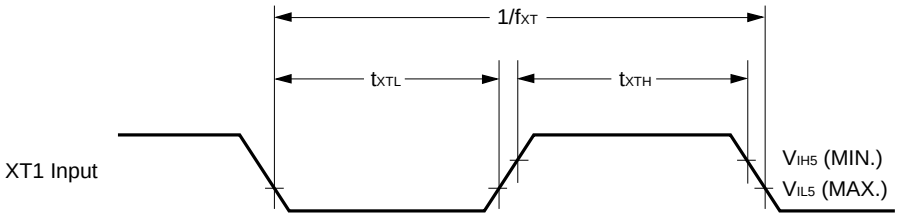
Note C is a load capacitance of the SO1 output line.

AC TIMING TEST POINT (EXCLUDING X1, XT1 INPUT)

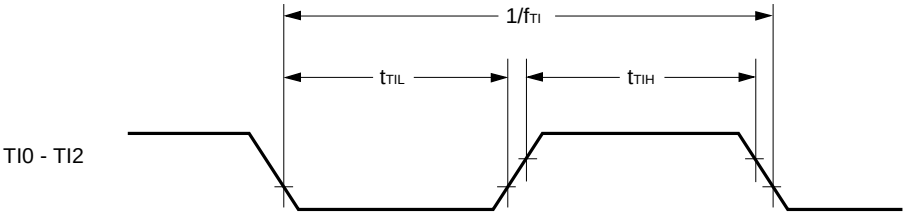


CLOCK TIMING



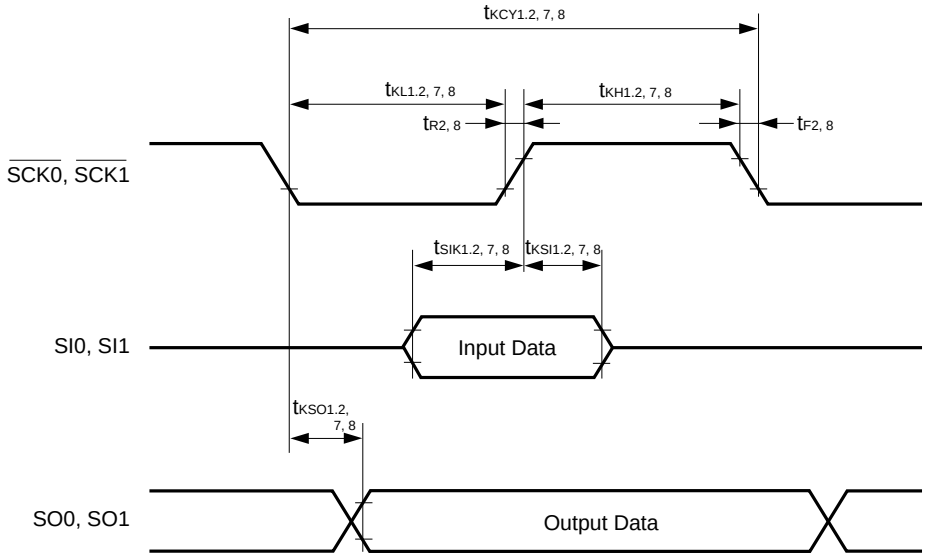


TI TIMING

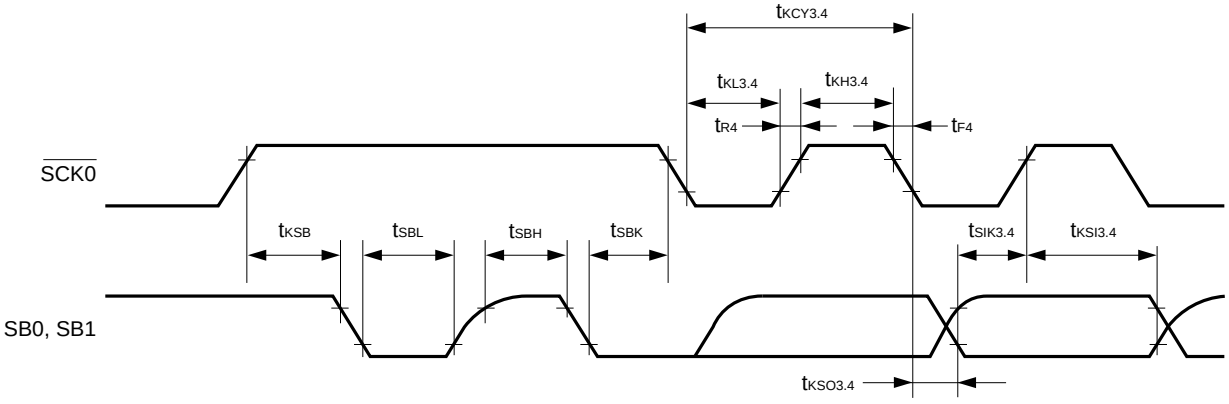


SERIAL TRANSFER TIMING

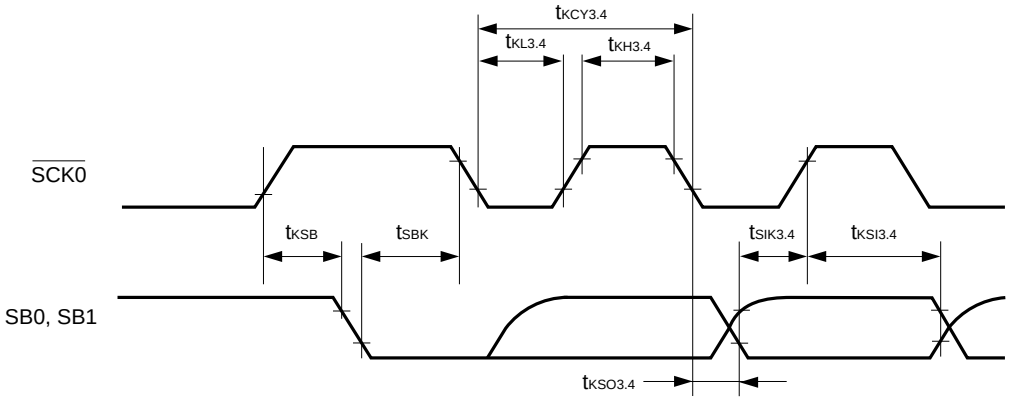
3-wire serial I/O mode:



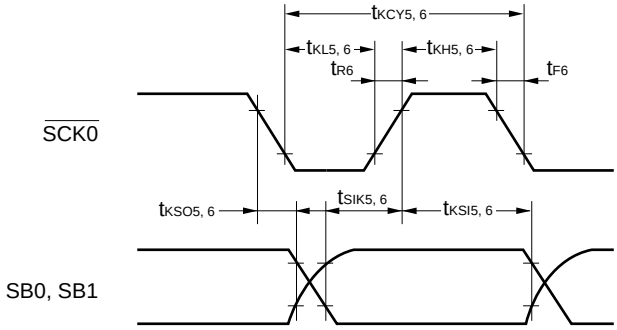
SBI mode (bus release signal transfer):



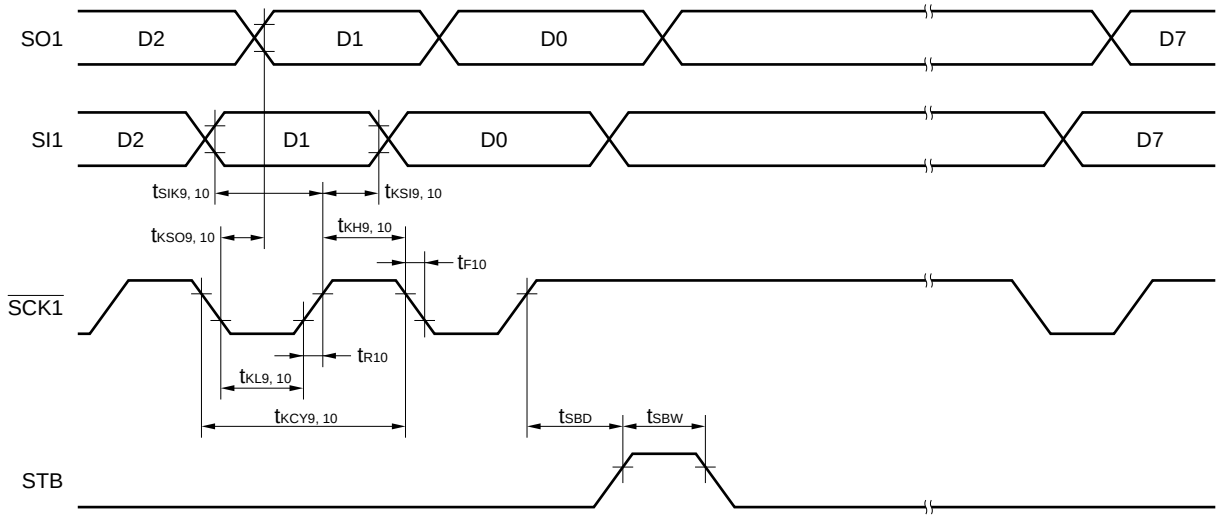
SBI mode (command signal transfer):



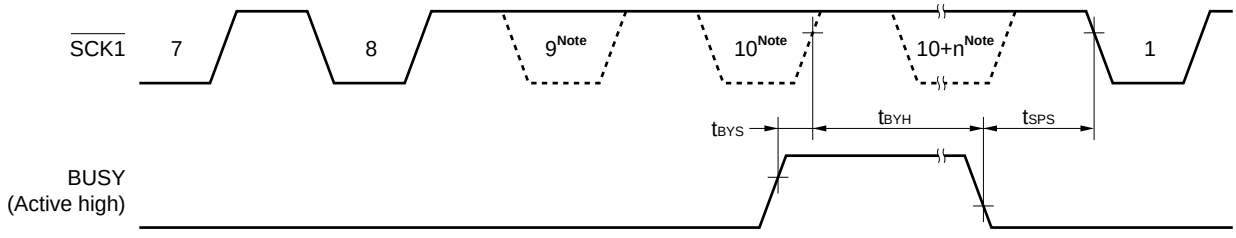
2-wire serial I/O mode:



3-wire serial I/O mode with automatic transmit/receive function:



3-wire serial I/O mode with automatic transmit/receive function (Busy processing):



Note Though it does not become low level actually, here it is described as it does due to the timing rule.

A/D CONVERTER CHARACTERISTICS (T_A = –40 to +85 °C, AV_{DD} = V_{DD} = 4.0 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	Resolution			8	8	8	bit
	Total error **Note 1**					0.6	%
	Conversion time **Note 2**	t_{CONV}	1 MHz ≤ f_X ≤ 5.0 MHz	19.1		200	μs
★	Sampling time **Note 3**	t_{SAMP}		12/f_X			μs
	Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
★	Reference voltage	AV_{REF}		4.0		AV_{DD}	V
	AV_{REF} resistor	R_{AVREF}		4	14		kΩ

Notes 1. Quantization error (±1/2LSB) is not included. This parameter is indicated as the ratio to the full-scale value.

2. Set the A/D conversion time to 19.1 μs or more.

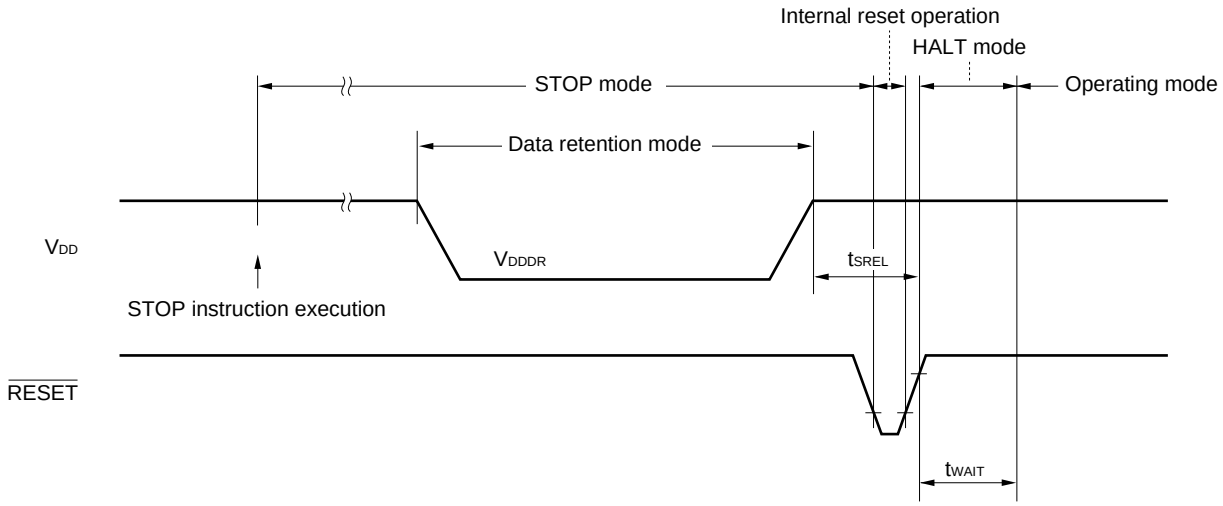
3. Sampling time depends on the conversion time.

DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (T_A = –40 to +85 °C)

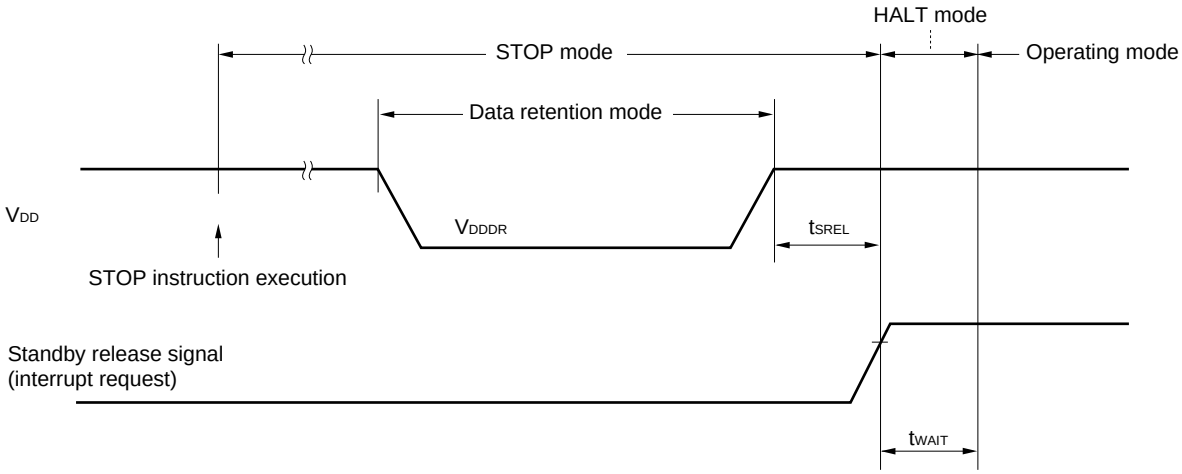
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.0 V Subsystem clock stopped, Feedback resistor not connected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{17}/f_X$		ms
		Release by interrupt		**Note**		ms

Note Selection of $2^{12}/f_X$, $2^{14}/f_X$ to $2^{17}/f_X$ is available by bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS).

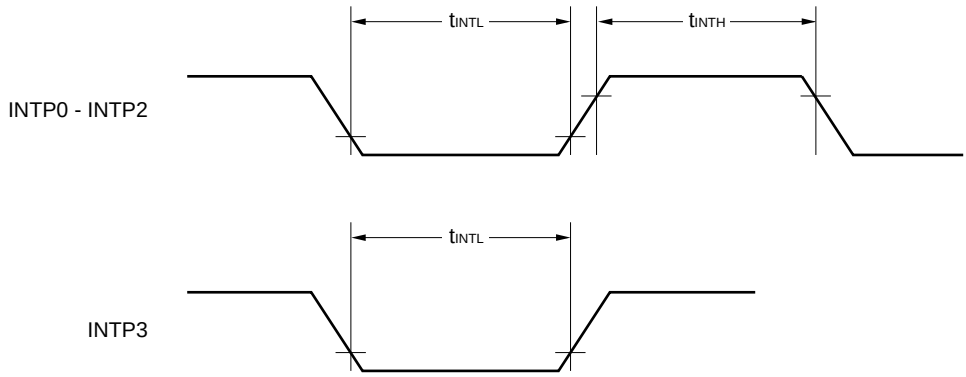
Data retention timing (STOP mode release by $\overline{\text{RESET}}$)



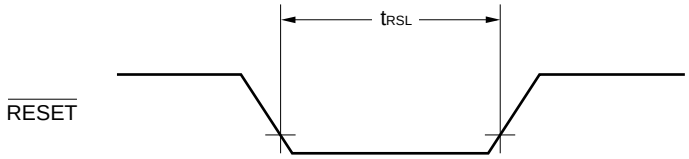
Data retention timing (standby release signal: STOP mode release by interrupt signal)



Interrupt input timing

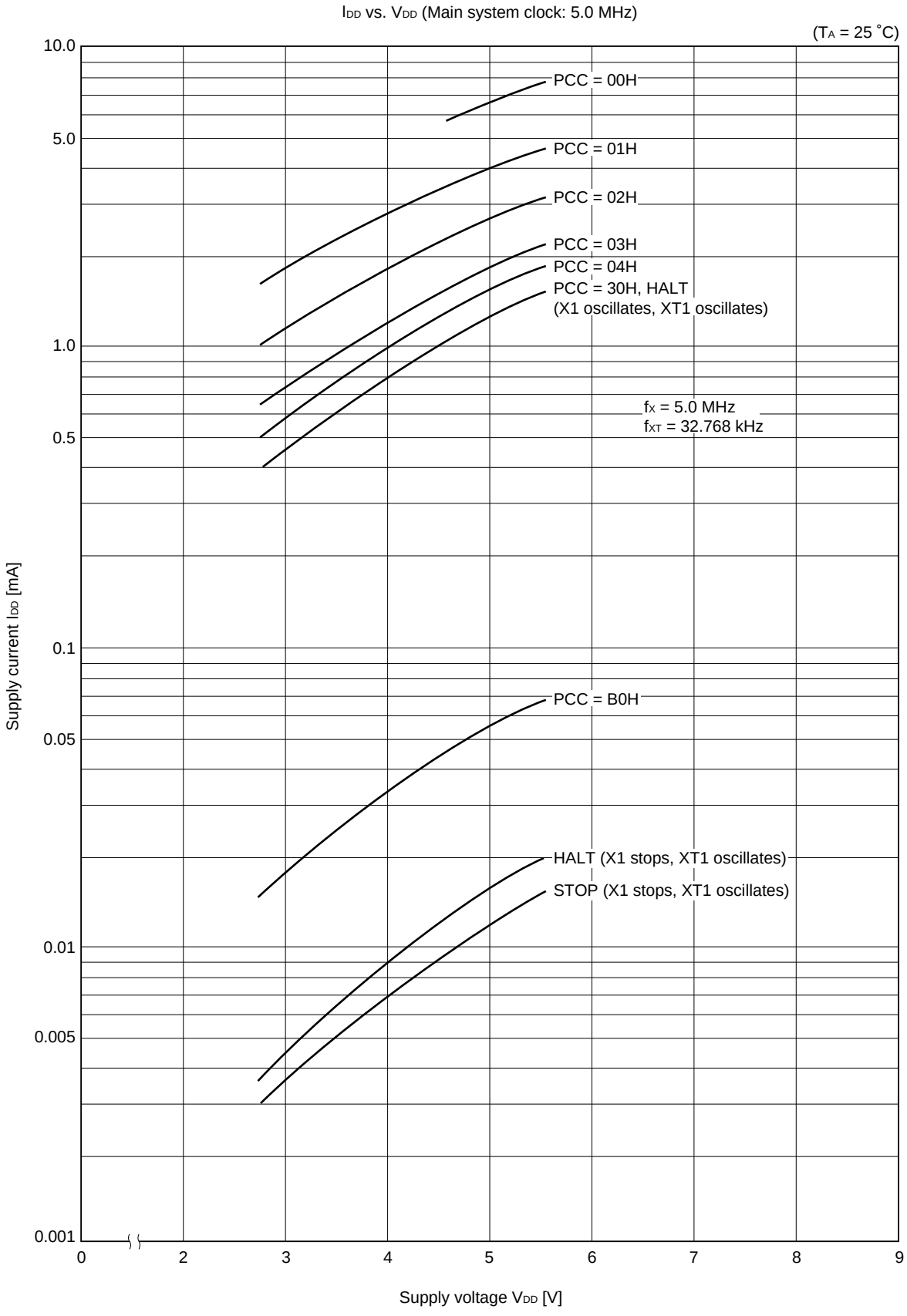


$\overline{\text{RESET}}$ input timing



11. CHARACTERISTIC CURVE (REFERENCE VALUE)

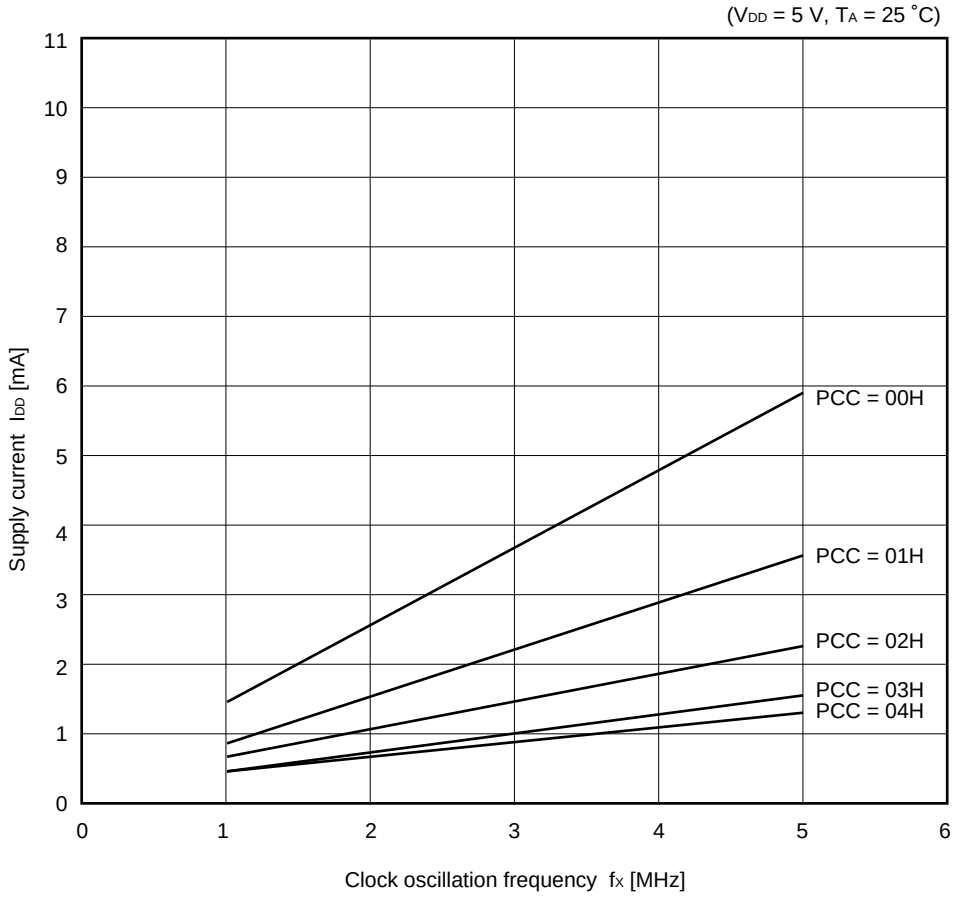
(1) μPD780204, 780205



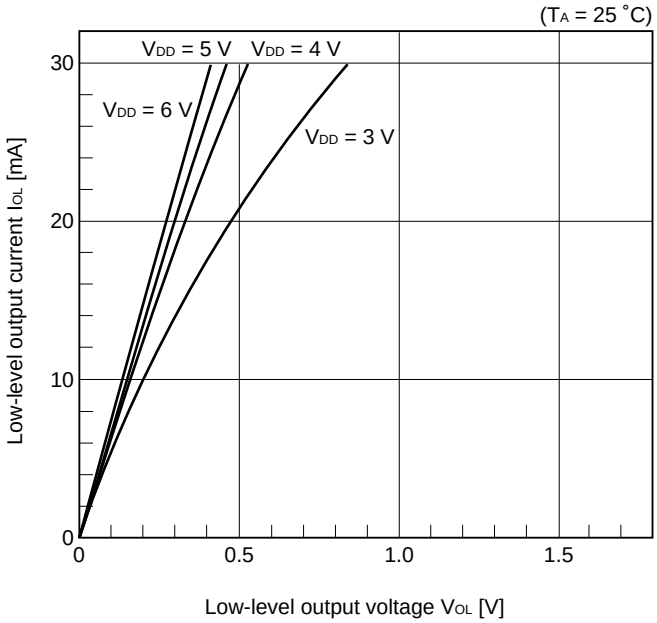
★

I_{DD} vs. f_X

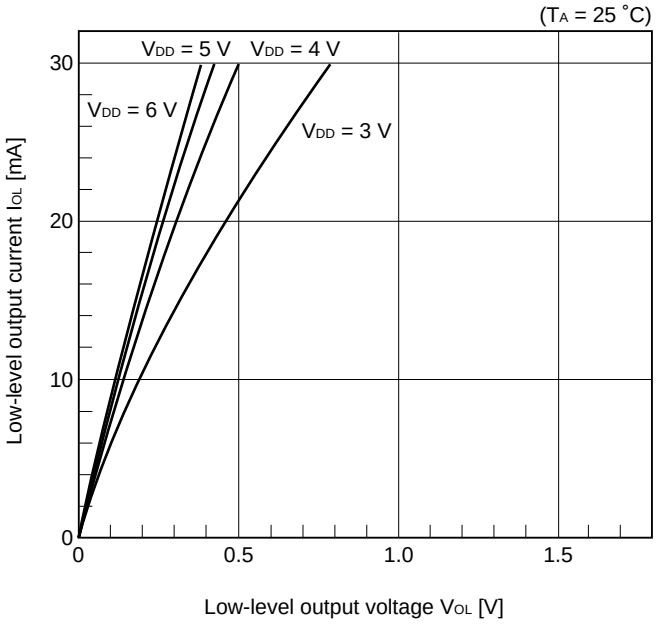
(V_{DD} = 5 V, T_A = 25 ˚C)



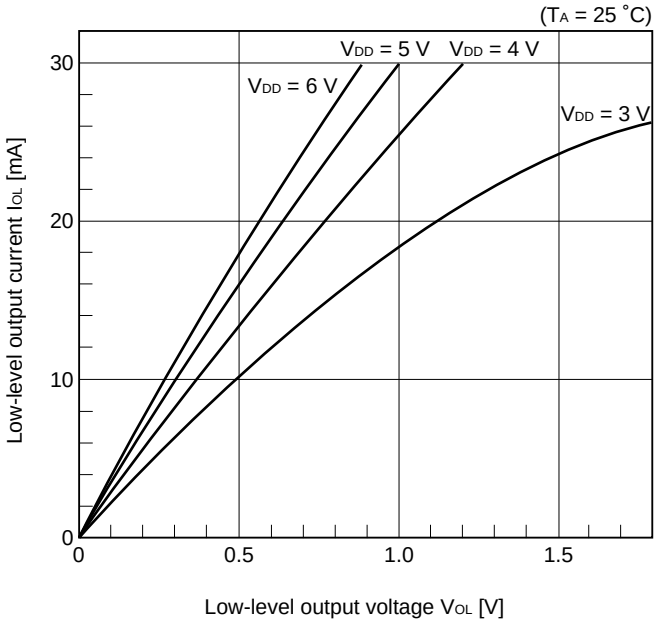
V_{OL} vs. I_{OL} (Port 1)



V_{OL} vs. I_{OL} (Ports 0, 2, 3)

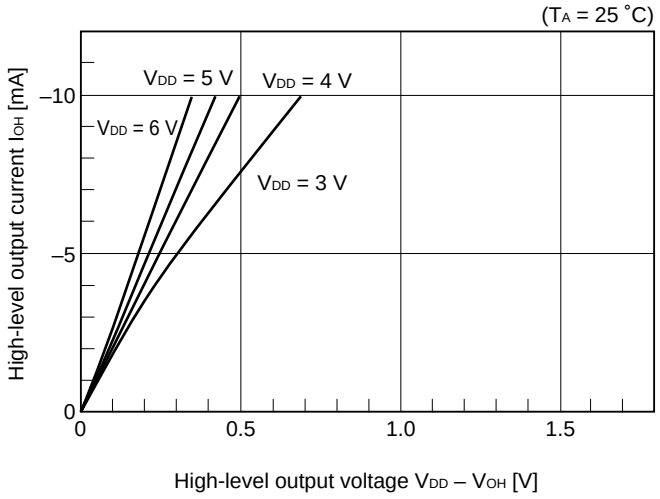


V_{OL} vs. I_{OL} (Port 7)

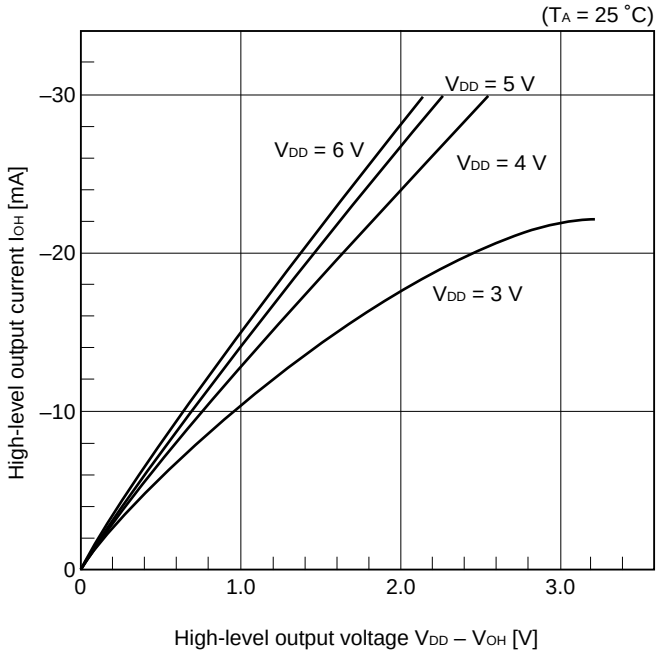


★

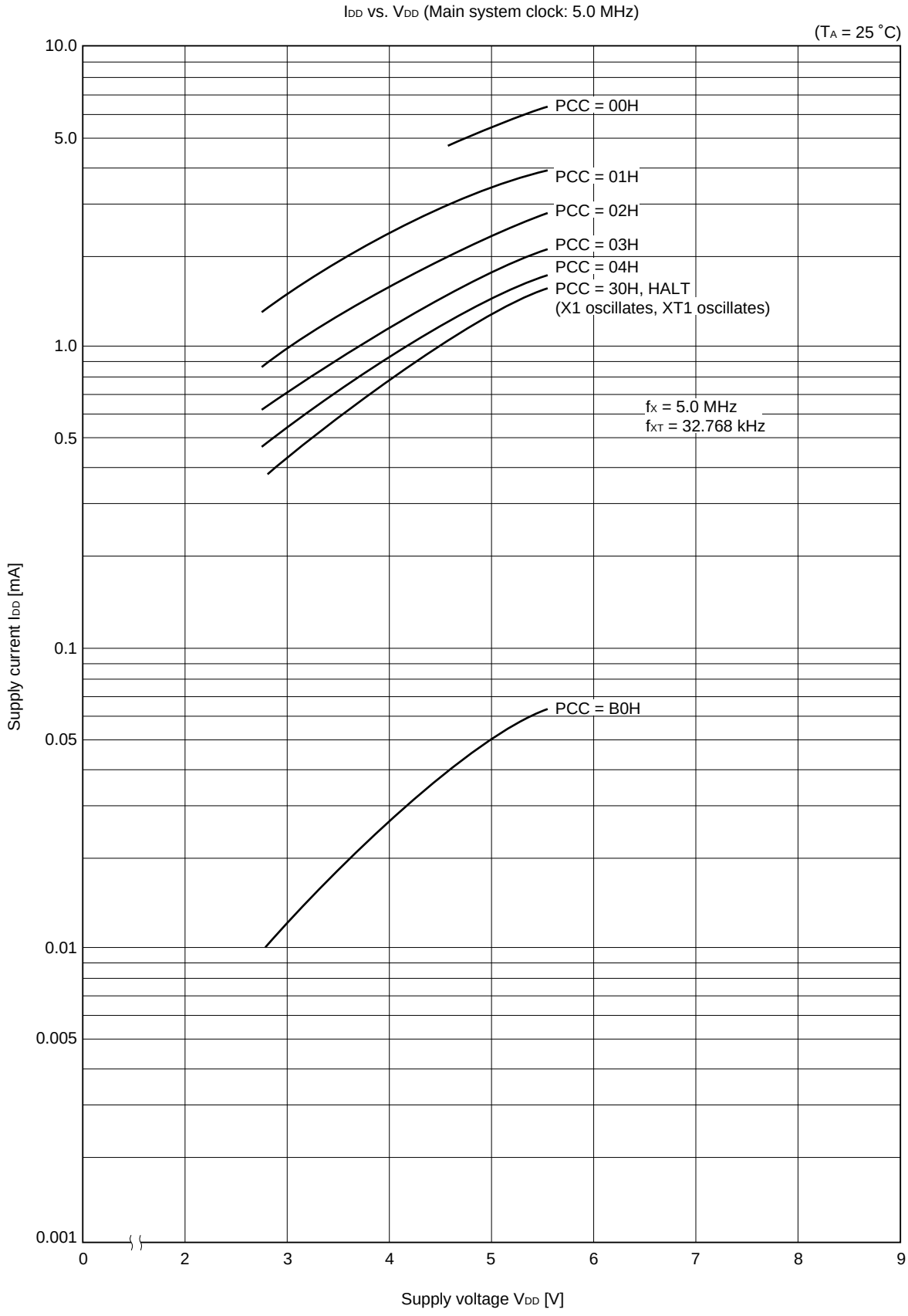
V_{DD} – V_{OH} vs. I_{OH} (Port 0 - Port 3)

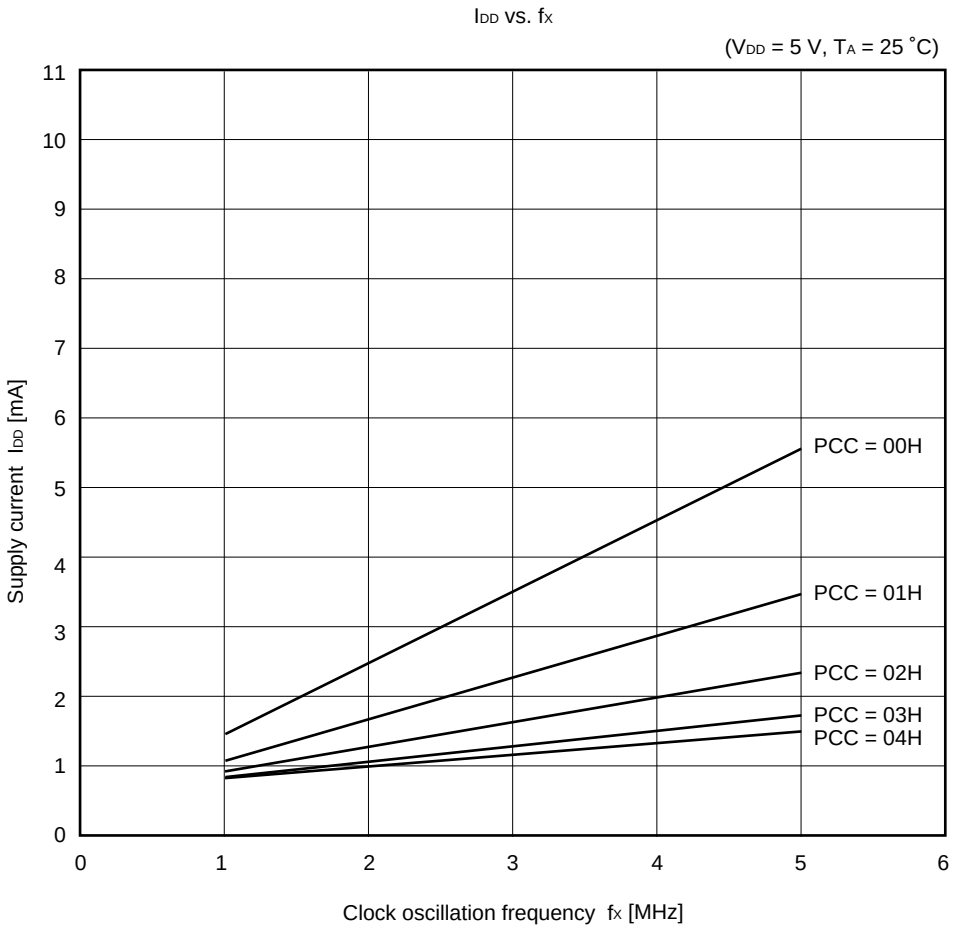


V_{DD} – V_{OH} vs. I_{OH} (Port 8 - Port 12)



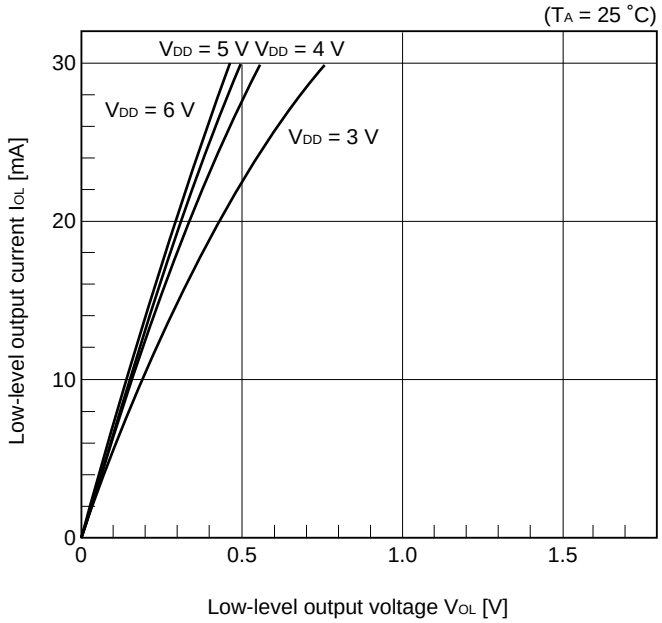
★ **(2) μPD780206, 780208**




IDD vs. fX
(VDD = 5 V, TA = 25 ˚C)
Supply current IDD [mA]
Clock oscillation frequency fX [MHz]
PCC = 00H
PCC = 01H
PCC = 02H
PCC = 03H
PCC = 04H
0
1
2
3
4
5
6
7
8
9
10
11

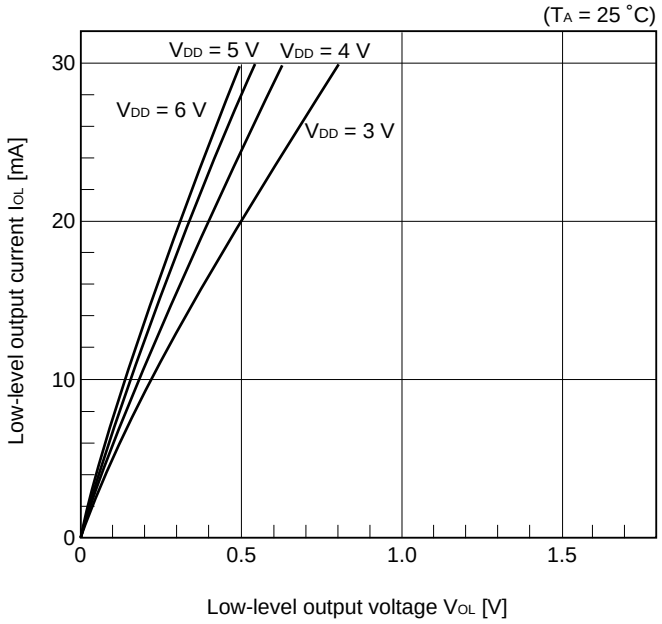
V_{OL} vs. I_{OL} (Port 1)

(T_A = 25 °C)

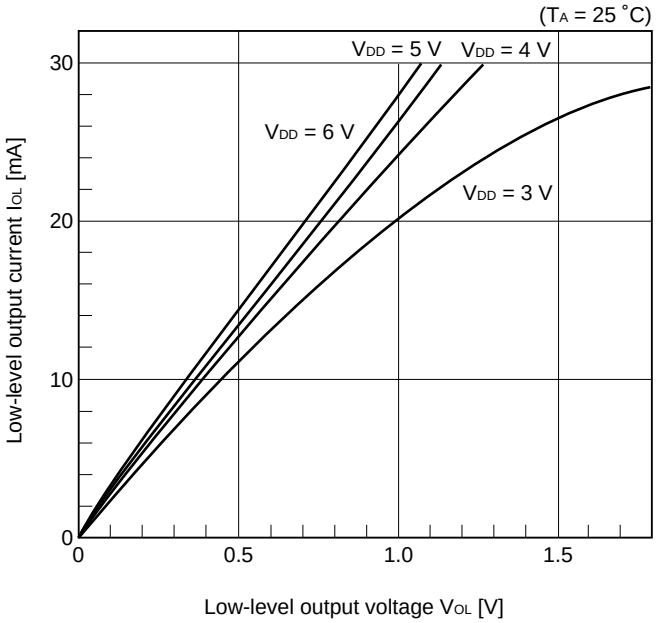


V_{OL} vs. I_{OL} (Ports 0, 2, 3)

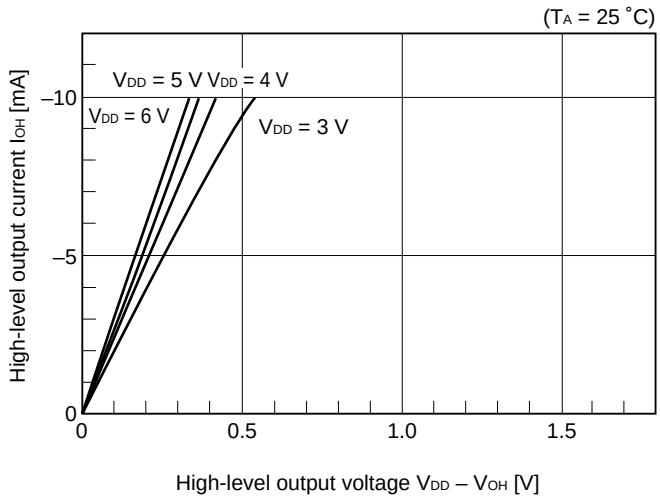
(T_A = 25 °C)



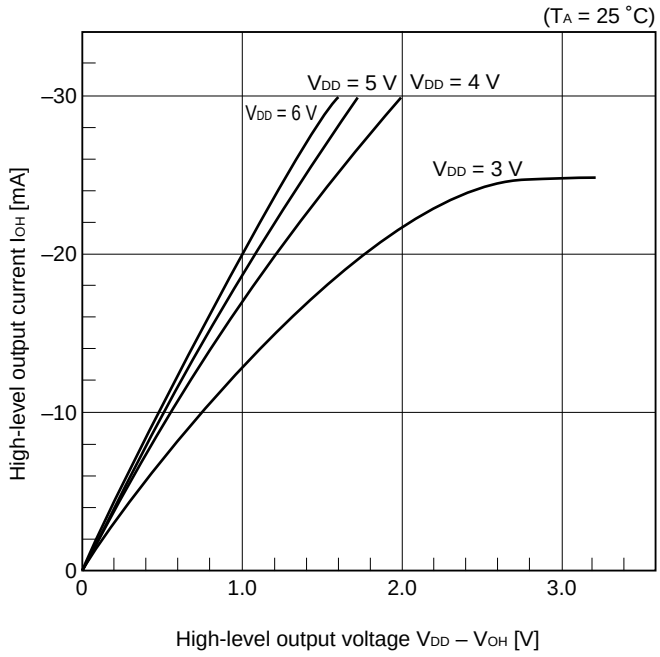
V_{OL} vs. I_{OL} (Port 7)



V_{DD} – V_{OH} vs. I_{OH} (Port 0 - Port 3)

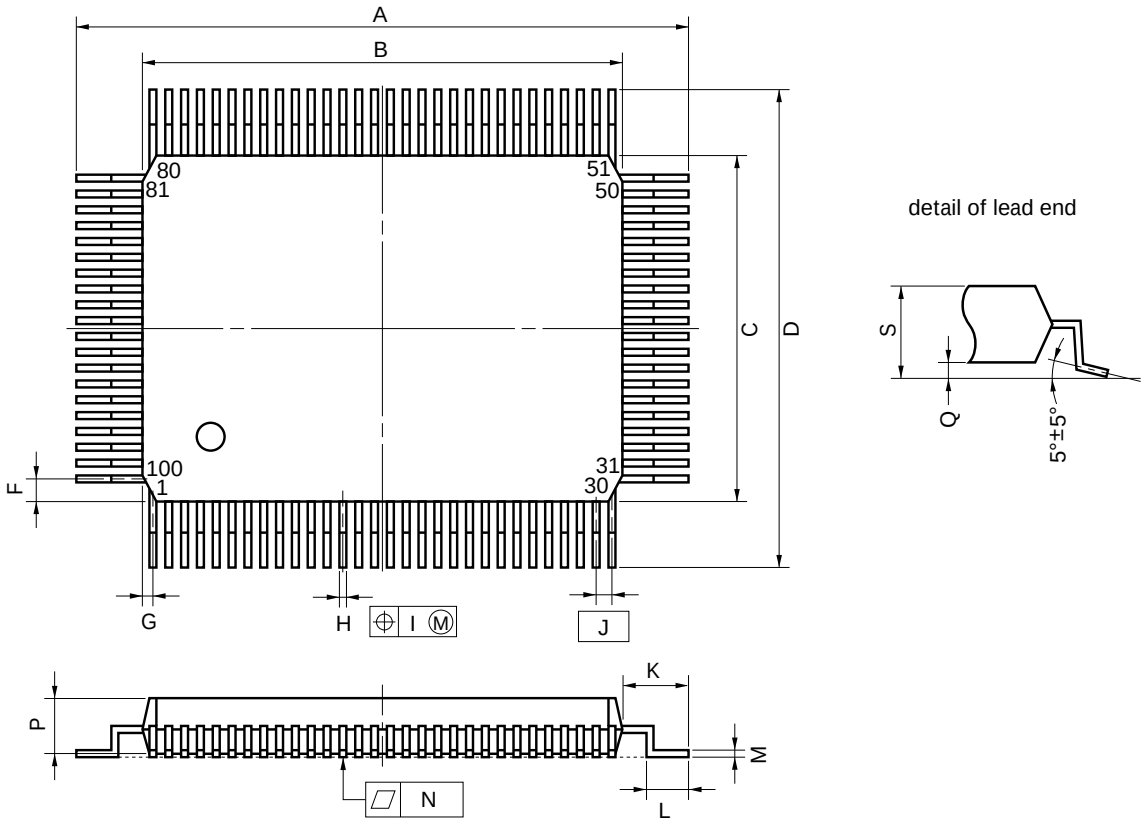


V_{DD} – V_{OH} vs. I_{OH} (Port 8 - Port 12)



12. PACKAGE DRAWING

100 PIN PLASTIC QFP (14 × 20)



P100GF-65-3BA1-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

Remark The dimensions and materials of the ES model are the same as the mass-produced model.

13. RECOMMENDED SOLDERING CONDITIONS

The conditions listed below shall be met when soldering the μPD780204, 780205, 780206, and 780208.

For details of the recommended soldering conditions, refer to our document **Semiconductor Device Mounting Technology Manual (C10535E)**.

Please consult with our sales offices in case any other soldering process is used, or in case soldering is done under different conditions.

Table 13-1. Soldering Conditions for Surface-Mount Type

μPD780204GF-×××-3BA: 100-pin plastic QFP (14 × 20 mm)
μPD780205GF-×××-3BA: 100-pin plastic QFP (14 × 20 mm)
μPD780206GF-×××-3BA: 100-pin plastic QFP (14 × 20 mm)
μPD780208GF-×××-3BA: 100-pin plastic QFP (14 × 20 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
★ Infrared reflow	Package peak temperature: 235 ˚C, Duration: 30 sec. max. (at 210 ˚C or above), Number of times: Thrice max.	IR35-00-3
★ VPS	Package peak temperature: 215 ˚C, Duration: 40 sec. max. (at 200 ˚C or above), Number of times: Thrice max.	VP15-00-3
Wave soldering	Solder bath temperature: 260 ˚C max. Duration: 10 sec. max. Number of times: Once Preliminary heat temperature: 120 ˚C max. (Package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300 ˚C max., Duration: 3 sec. max. (per device side)	—

Caution Using more than one soldering method should be avoided (except in the case of partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following tools are available for development of systems using the μPD780204, 780205, 780206, and 780208:

Language Processing Software

RA78K/0[Note 1, 2, 3, 4]	Assembler package common to 78K/0 series
CC78K/0[Note 1, 2, 3, 4]	C compiler package common to 78K/0 series
DF780208[Note 1, 2, 3, 4]	Device file for μPD780208 subseries
CC78K/0-L[Note 1, 2, 3, 4]	C compiler library source file common to 78K/0 series

PROM Writing Tools

PG-1500	PROM programmer
PA-78P0208GF PA-78P0208KL-T	Programmer adapter connectd to PG-1500
PG-1500 Controller[Note 1, 2]	Control program for PG-1500

Debugging Tools

	IE-78000-R	In-circuit emulator common to 78K/0 series
★	IE-78000-R-A	In-circuit emulator common to 78K/0 series (for integrated debugger)
	IE-78000-R-BK	Break board common to 78K/0 series
	IE-780208-R-EM	Emulation board for evaluating μPD780208 subseries
	EP-78064GF-R	Emulation probe common to μPD78064 subseries
	EV-9200GF-100	Socket mounted to target system created for 100-pin plastic QFP (GF-3BA type)
	SM78K0[Note 5, 6, 7]	System simulator common to 78K/0 series
★	ID78K0[Note 4, 5, 6, 7]	Integrated debugger for IE-78000-R-A
	SD78K/0[Note 1, 2]	Screen debugger for IE-78000-R
	DF780208[Note 1, 2, 4, 5, 6, 7]	Device file for μPD780208 subseries

Real-time OS

RX78K/0[Note 1, 2, 3, 4]	Real-time OS for 78K/0 series
MX78K0[Note 1, 2, 3, 4]	OS for 78K/0 series

Notes 1. PC-9800 series (MS-DOS™) based
2. IBM PC/AT™ and compatible (PC DOS™/IBM DOS™/MS-DOS) based
3. HP9000 series 300™ (HP-UX™) based
4. HP9000 series 700™ (HP-UX) based, SPARCstation™ (Sun OS™) based, EWS4800 series (EWS-UX/V) based
5. PC-9800 series (MS-DOS + Windows™) based
6. IBM PC/AT and compatible (PC DOS/IBM DOS/MS-DOS + Windows) based
7. NEWS™ (NEWS-OS™) based

Remarks 1. Please refer to the **78K/0 Series Selection Guide (U11126E)** for information on third party development tools.
2. RA78K/0, CC78K/0, SM78K0, ID78K0, SD78K/0, and RX78K/0 are used in combination with DF780208.

Fuzzy Inference Development Support System

FE9000[Note 1]/FE9200[Note 3]	Fuzzy knowledge data creation tool
FT9080[Note 1]/FT9085[Note 2]	Translator
FI78K0[Note 1, 2]	Fuzzy inference module
FD78K0[Note 1, 2]	Fuzzy inference debugger

Notes 1. PC-9800 series (MS-DOS) based

2. IBM PC/AT and compatible (PC DOS/IBM DOS/MS-DOS) based

3. IBM PC/AT and compatible (PC DOS/IBM DOS/MS-DOS + Windows) based

Remark Please refer to the **78K/0 Series Selection Guide (U11126E)** for information on third party development tools.

APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

Document Name	Document No.	
	Japanese	English
μPD780208 subseries user's manual	U11302J	U11302E
μPD780204, 780205, 780206, 780208 data sheet	U10436J	This document
μPD78P0208 data sheet	U11295J	U11295E
μPD780208 subseries special function register list	U10997J	—
78K/0 series user's manual - instruction	IEU-849	IEU-1372
78K/0 series instruction list	U10903J	—
78K/0 series instruction set	U10904J	—
78K/0 series application note - Basic (II)	U10121J	U10121E

Caution The documents listed above are subject to change without notice. Be sure to use the latest documents for designing your system.

Development Tool Documents (User's Manual)

	Document Name		Document No.	
			Japanese	English
	RA78K series assembler package	Operation	EEU-809	EEU-1399
		Language	EEU-815	EEU-1404
★	RA78K0 assembler package	Operation	U11802J	U11802E
★		Assembly language	U11801J	U11801E
★		Structured assembly language	U11789J	U11789E
	RA78K series structured assembler preprocessor		EEU-817	EEU-1402
	CC78K series C compiler	Operation	EEU-656	EEU-1280
		Language	EEU-655	EEU-1284
★	CC78K0 C compiler	Operation	U11517J	U11517E
★		Language	U11518J	U11518E
	CC78K series library source file		EEU-777	—
	CC78K/0 C compiler application note	Programming know-how	EEA-618	EEA-1208
	PG-1500 PROM programmer		EEU-651	EEU-1335
	PG-1500 controller PC-9800 series (MS-DOS) base		EEU-704	EEU-1291
	PG-1500 controller IBM PC series (PC DOS) base		EEU-5008	U10540E
	IE-78000-R		EEU-810	U11376E
	IE-78000-R-A		U10057J	U10057E
	IE-78000-R-BK		EEU-867	EEU-1427
	IE-780208-R-EM		EEU-977	EEU-1501
	EP-78064		EEU-934	EEU-1469
	SM78K0 system simulator	Reference	U10181J	U10181E
	SM78K series system simulator	External parts user-open interface specification	U10092J	U10092E
	SD78K/0 screen debugger PC-9800 series (MS-DOS) base	Introduction	EEU-852	U10539E
		Reference	U10952J	—
	SD78K/0 screen debugger IBM PC/AT (PC DOS) base	Introduction	EEU-5024	EEU-1414
		Reference	U11279J	U11279E
★	ID78K0 integrated debugger EWS based	Reference	U11151J	—
★	ID78K0 integrated debugger PC based	Reference	U11539J	U11539E
★	ID78K0 integrated debugger Windows based	Guide	U11649J	U11649E

Caution The documents listed above are subject to change without notice. Be sure to use the latest documents for designing your system.

Documents Related to Embedded Software (User's Manual)

Document Name		Document No.	
		Japanese	English
78K/0 series real-time OS	Fundamental	U11537J	—
	Installation	U11536J	—
	Technical	U11538J	—
78K/0 series OS MX78K0	Fundamental	EEU-5010	—
Fuzzy knowledge data creation tool		EEU-829	EEU-1438
78K/0, 78K/II, 87AD series fuzzy inference development suppport system - translator		EEU-862	EEU-1444
78K/0 series fuzzy inference development support system - fuzzy inference module		EEU-858	EEU-1441
78K/0 series fuzzy inference development support system - fuzzy inference debugger		EEU-921	EEU-1458

Other Related Documents

Document Name	Document No.	
	Japanese	English
IC package manual	C10943X	
Semiconductor device mounting technology manual	C10535J	C10535E
Quality grade on NEC semiconductor devices	C11531J	C11531E
NEC semiconductor device reliability/quality control system	C10983J	C10983E
Static electricity discharge (ESD) test	MEM-539	—
Semiconductor device quality guarantee guide	C11893J	MEI-1202
Product guide related to microcomputer - other manufacturers	U11416J	—

Caution The documents listed above are subject to change without notice. Be sure to use the latest documents for designing your system.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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