NEC

MOS INTEGRATED CIRCUIT

μPD780076, 780078, 780076Y, 780078Y

8-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μPD780076 and 780078 are products in the μPD780078 Subseries within the 78K/0 Series. They are based on the existing μPD780034A Subseries, with an enhanced timer and serial interface and greater ROM and RAM capacities.

The μPD780076Y and 780078Y are products based on the μPD780078 Subseries, with an I^2C bus interface supporting multimaster.

A flash memory version, the μPD78F0078 and 78F0078Y, and various development tools are available.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD780076, 780078, 780076Y, 780078Y Subseries User's Manual: U14260E

78K/0 Series User's Manual – Instructions: U12326E

FEATURES

- Internal large capacity ROM and RAM

Item / Part Number	Program Memory	Data Memory		Package
	Internal ROM	Internal High-Speed RAM	Internal Expansion RAM	
μPD780076, 780076Y	48 KB	1024 bytes	1024 bytes	• 64-pin plastic QFP (14 × 14) • 64-pin plastic TQFP (12 × 12)
★ μPD780078, 780078Y	60 KB			

- Minimum instruction execution time: 0.24 μs (at f_X = 8.38 MHz operation)
- I/O ports: 52 (N-ch open-drain 5 V withstand voltage: 4)
- 10-bit resolution A/D converter: 8 channels
- Serial interface: 3 channels (μPD780078 Subseries)
  4 channels (μPD780078Y Subseries)
- Timer: 6 channels
- Power supply voltage: V_{DD} = 1.8 to 5.5 V

APPLICATIONS

Personal computers, air conditioners, dash boards, air bags, car audios, etc.

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Printed in Japan

The mark ★ shows major revised points.

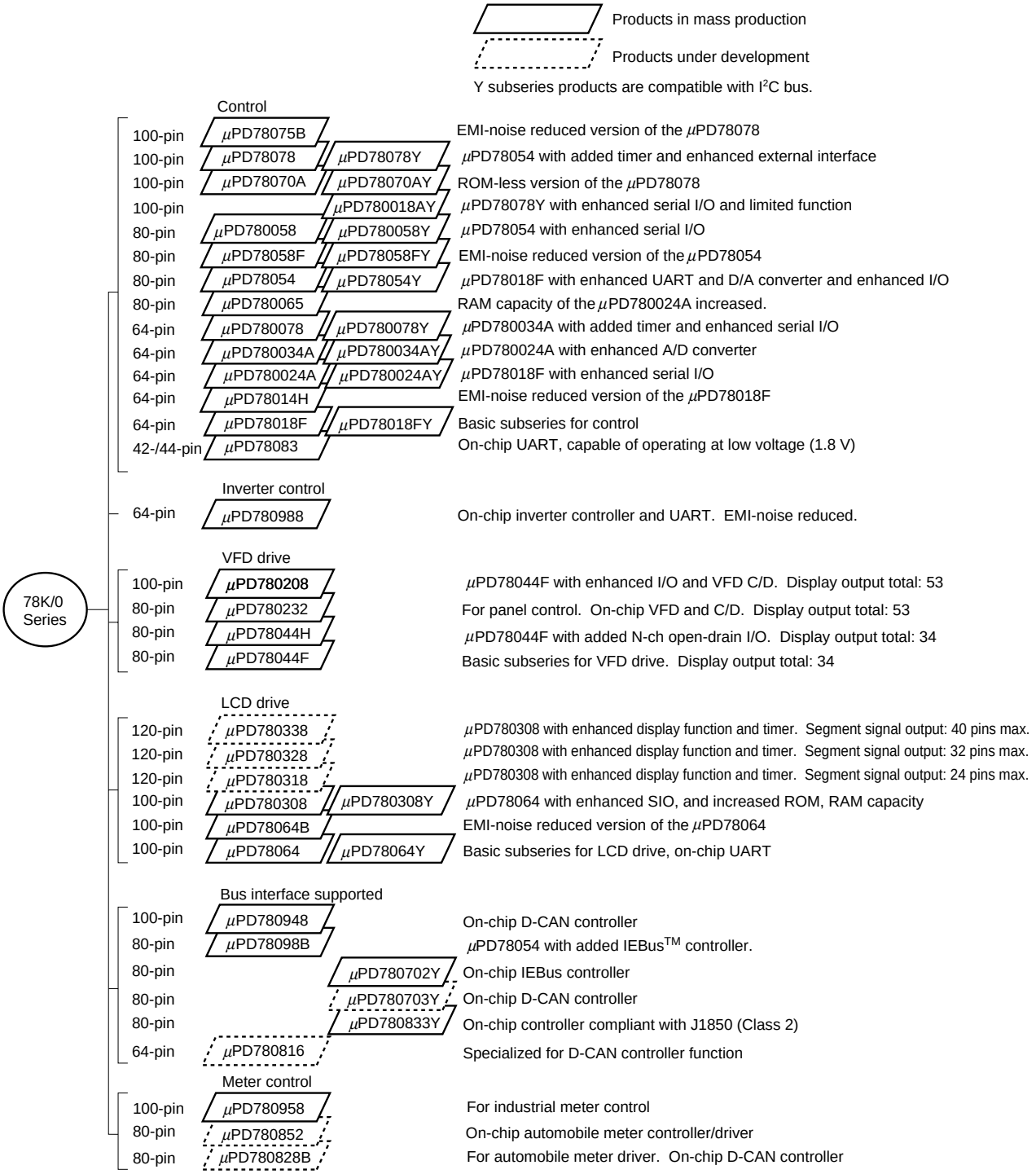
ORDERING INFORMATION

	Part Number	Package
	μPD780076GC-×××-AB8	64-pin plastic QFP (14 × 14)
★	μPD780076GK-×××-9ET	64-pin plastic TQFP (12 × 12)
	μPD780078GC-×××-AB8	64-pin plastic QFP (14 × 14)
★	μPD780078GK-×××-9ET	64-pin plastic TQFP (12 × 12)
	μPD780076YGC-×××-AB8	64-pin plastic QFP (14 × 14)
★	μPD780076YGK-×××-9ET	64-pin plastic TQFP (12 × 12)
	μPD780078YGC-×××-AB8	64-pin plastic QFP (14 × 14)
★	μPD780078YGK-×××-9ET	64-pin plastic TQFP (12 × 12)

Remark ××× indicates ROM code suffix.

★ 78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.



Remark VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major functional differences among the subseries are shown below.

- **Non Y Subseries**

Subseries Name \ Function		ROM Capacity (Bytes)	Timer				8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-Bit	16-Bit	Watch	WDT							
Control	μPD78075B	32 K to 40 K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch)	88	1.8 V	√
	μPD78078	48 K to 60 K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24 K to 60 K	2 ch							3 ch (time-division UART: 1 ch)	68	1.8 V	
	μPD78058F	48 K to 60 K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16 K to 60 K										2.0 V	
	μPD780065	40 K to 48 K							–	4 ch (UART: 1 ch)	60	2.7 V	
	μPD780078	48 K to 60 K		2 ch			–	8 ch		3 ch (UART: 2 ch)	52	1.8 V	
	μPD780034A	8 K to 32 K		1 ch						3 ch (UART: 1 ch)	51		
	μPD780024A						8 ch	–					
	μPD78014H									2 ch	53		
	μPD78018F	8 K to 60 K											
	μPD78083	8 K to 16 K		–	–					1 ch (UART: 1 ch)	33		–
Inverter control	μPD780988	16 K to 60 K	3 ch	**Note**	–	1 ch	–	8 ch	–	3 ch (UART: 2 ch)	47	4.0 V	√
VFD drive	μPD780208	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	2 ch	74	2.7 V	–
	μPD780232	16 K to 24 K	3 ch	–	–		4 ch				40	4.5 V	
	μPD78044H	32 K to 48 K	2 ch	1 ch	1 ch		8 ch			1 ch	68	2.7 V	
	μPD78044F	16 K to 40 K								2 ch			
LCD drive	μPD780338	48 K to 60 K	3 ch	2 ch	1 ch	1 ch	–	10 ch	1 ch	2 ch (UART: 1 ch)	54	1.8 V	–
	μPD780328										62		
	μPD780318										70		
	μPD780308	48 K to 60 K	2 ch	1 ch			8 ch	–	–	3 ch (time-division UART: 1 ch)	57	2.0 V	
	μPD78064B	32 K								2 ch (UART: 1 ch)			
	μPD78064	16 K to 32 K											
Bus interface supported	μPD780948	60 K	2 ch	2 ch	1 ch	1 ch	8 ch	–	–	3 ch (UART: 1 ch)	79	4.0 V	√
	μPD78098B	40 K to 60 K		1 ch					2 ch		69	2.7 V	–
	μPD780816	32 K to 64 K		2 ch			12 ch		–	2 ch (UART: 1 ch)	46	4.0 V	
Meter control	μPD780958	48 K to 60 K	4 ch	2 ch	–	1 ch	–	–	–	2 ch (UART: 1 ch)	69	2.2 V	–
Dash board control	μPD780852	32 K to 40 K	3 ch	1 ch	1 ch	1 ch	5 ch	–	–	3 ch (UART: 1 ch)	56	4.0 V	–
	μPD780828B	32 K to 60 K								2 ch (UART: 1 ch)	59		

Note 16-bit timer: 2 channels
10-bit timer: 1 channel

- **Y Subseries**

Subseries Name \ Function		ROM Capacity (Bytes)	Timer				8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-Bit	16-Bit	Watch	WDT							
Control	μPD78078Y	48 K to 60 K	4 ch	1 ch	1 ch	1 ch	8 ch	–	2 ch	3 ch (UART: 1 ch, I^2C: 1 ch)	88	1.8 V	√
	μPD78070AY	–									61	2.7 V	
	μPD780018AY	48 K to 60 K							–	3 ch (I^2C: 1 ch)	88		
	μPD780058Y	24 K to 60 K	2 ch						2 ch	3 ch (time division UART: 1 ch, I^2C: 1 ch)	68	1.8 V	
	μPD78058FY	48 K to 60 K								3 ch (UART: 1 ch, I^2C: 1 ch)	69	2.7 V	
	μPD78054Y	16 K to 60 K										2.0 V	
	μPD780078Y	48 K to 60 K		2 ch			–	8 ch	–	4 ch (UART: 2 ch, I^2C: 1 ch)	52	1.8 V	
	μPD780034AY	8 K to 32 K		1 ch						3 ch (UART: 1 ch, I^2C: 1 ch)	51		
	μPD780024AY						8 ch	–					
	μPD78018FY	8 K to 60 K								2 ch (I^2C: 1 ch)	53		
LCD drive	μPD780308Y	48 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	–	–	3 ch (time division UART: 1 ch, I^2C: 1 ch)	57	2.0 V	–
	μPD78064Y	16 K to 32 K								2 ch (UART: 1 ch, I^2C: 1 ch)			
For bus interface	μPD780702Y	60 K	3 ch	2 ch	1 ch	1 ch	16 ch	–	–	4 ch (UART: 1 ch, I^2C: 1 ch)	67	3.5 V	–
	μPD780703Y												
	μPD780833Y										65	4.5 V	

Remark The functions of non Y subseries and Y subseries products are the same, except for the serial interface.

FUNCTION OVERVIEW

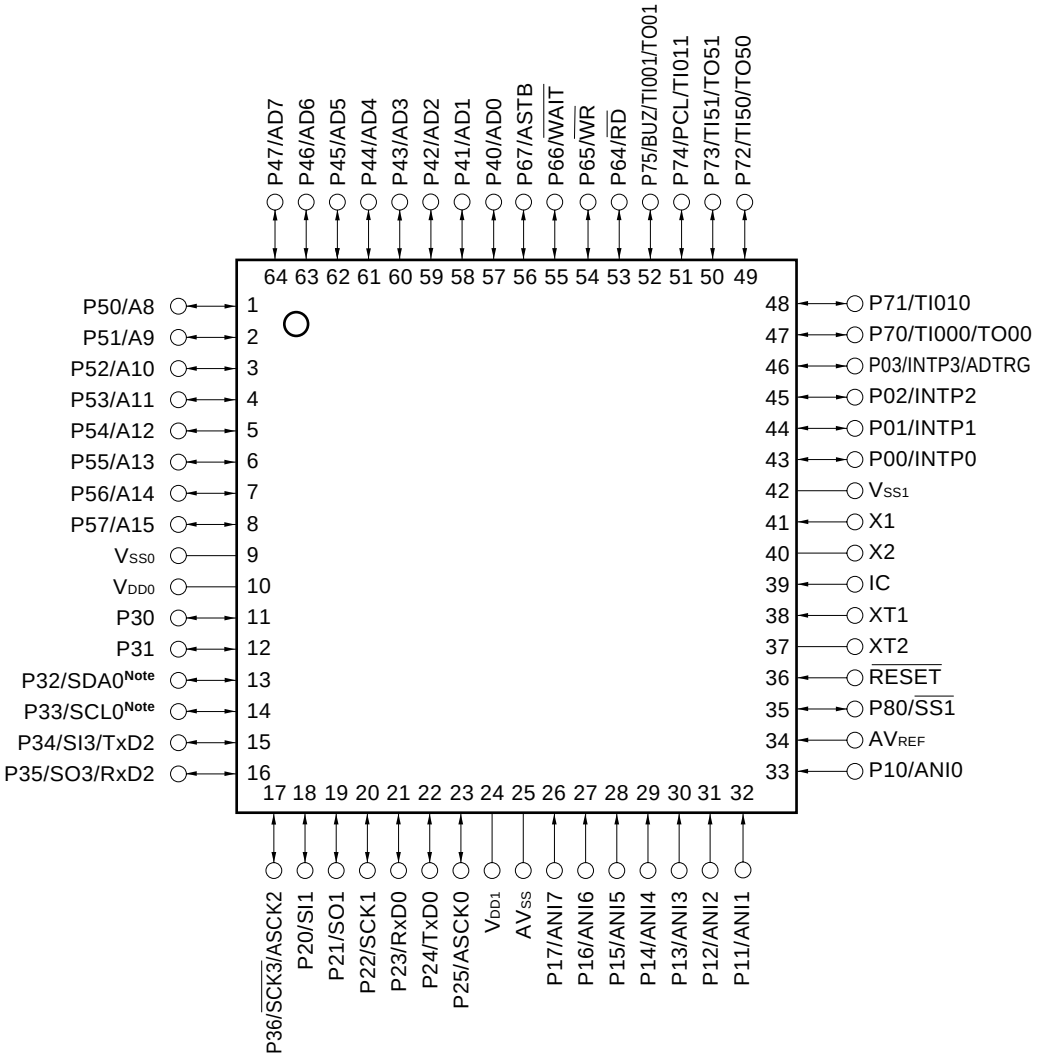
Item \ Part Number		μPD780076 μPD780076Y	μPD780078 μPD780078Y
Internal memory	ROM	48 KB	60 KB
	High-speed RAM	1024 bytes	
	Expansion RAM	1024 bytes	
Memory space		64 KB	
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		On-chip variable function of minimum instruction execution time	
	When main system clock selected	0.24 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (at 8.38 MHz operation)	
	When subsystem clock selected	122 μs (at 32.768 kHz operation)	
Instruction set		• 16-bit operation • Multiply/divide (8 bits × 8 bits,16 bits ÷ 8 bits) • Bit manipulate (set, reset, test, Boolean operation) • BCD adjust, etc.	
I/O ports		Total: 52 • CMOS input: 8 • CMOS I/O: 40 • N-ch open-drain I/O: 4	
★ A/D converter		• 10-bit resolution × 8 channels • Low-voltage operation available: AV_{DD} = 2.2 to 5.5 V	
Serial interface		• 3-wire serial I/O mode: 1 channel • UART mode: 1 channel • 3-wire serial I/O/UART mode selectable[Note]: 1 channel • I^2C bus mode (μPD780078Y Subseries only): 1 channel	
Timer		• 16-bit timer/event counter: 2 channels • 8-bit timer/event counter: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel	
Timer output		4 (8-bit PWM output capable: 2)	
Clock output		• 65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.10 MHz, 4.19 MHz, 8.38 MHz (at 8.38 MHz operation with main system clock) • 32.768 kHz (at 32.768 kHz operation with subsystem clock)	
Buzzer output		1.02 kHz, 2.05 kHz, 4.10 kHz, 8.19 kHz (at 8.38 MHz operation with main system clock)	
Vectored interrupt source	Maskable	Internal: 18 (μPD780078 Subseries) 19 (μPD780078Y Subseries) External: 5	
	Non-maskable	Internal: 1	
	Software	1	
Power supply voltage		V_{DD} = 1.8 to 5.5 V	
Operating ambient temperature		T_A = –40 to +85°C	
★ Package		• 64-pin plastic QFP (14 × 14) • 64-pin plastic TQFP (12 × 12)	

Note Pins are multiplexed. Select either of these interfaces.

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- **64-pin plastic QFP (14 × 14)**
  μPD780076GC-×××-AB8, 780078GC-×××-AB8, 780076YGC-×××-AB8, 780078YGC-×××-AB8
- ★ **64-pin plastic TQFP (12 × 12)**
  μPD780076GK-×××-9ET, 780078GK-×××-9ET, 780076YGK-×××-9ET, 780078YGK-×××-9ET



Note SDA0 and SCL0 are only provided on the μPD780078Y Subseries.

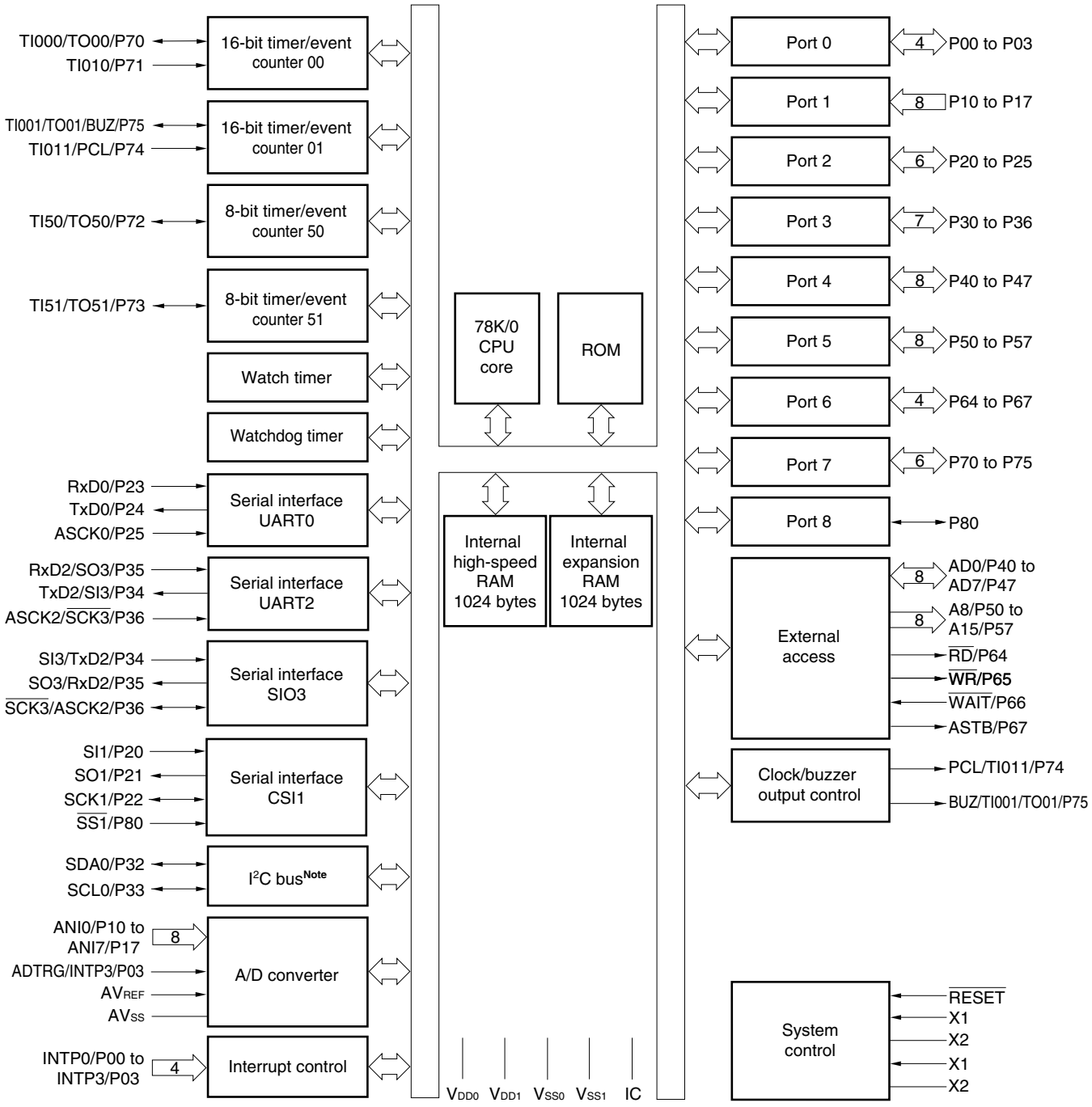
Cautions 1. Connect the IC (Internally Connected) pin directly to V_{SS0} or V_{SS1}.

2. Connect the AV_{SS} pin to V_{SS0}.

Remark When used in applications where the noise generated inside the microcontroller needs to be reduced, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

A8 to A15:	Address bus	PCL:	Programmable clock
AD0 to AD7:	Address/data bus	$\overline{RD}$:	Read strobe
ADTRG:	AD trigger input	$\overline{RESET}$:	Reset
ANI0 to ANI7:	Analog input	RxD0, RxD2:	Receive data
ASCK0, ASCK2:	Asynchronous serial clock	SCK1, $\overline{SCK3}$, SCL0:	Serial clock
ASTB:	Address strobe	SDA0:	Serial data
AV_{REF}:	Analog reference voltage	SI1, SI3:	Serial input
AV_{SS}:	Analog ground	SO1, SO3:	Serial output
BUZ:	Buzzer output	$\overline{SS1}$:	Serial interface chip select input
IC:	Internally connected	TI000, TI010, TI001,	
INTP0 to INTP3:	External interrupt input	TI011, TI50, TI51:	Timer input
P00 to P03:	Port 0	TO00, TO01, TO50, TO51:	Timer output
P10 to P17:	Port 1	TxD0, TxD2:	Transmit data
P20 to P25:	Port 2	V_{DD0}, V_{DD1}:	Power supply
P30 to P36:	Port 3	V_{SS0}, V_{SS1}:	Ground
P40 to P47:	Port 4	$\overline{WAIT}$:	Wait
P50 to P57:	Port 5	$\overline{WR}$:	Write strobe
P64 to P67:	Port 6	X1, X2:	Crystal (main system clock)
P70 to P75:	Port 7	XT1, XT2:	Crystal (subsystem clock)
P80:	Port 8		

2. BLOCK DIAGRAM



Note I²C bus is only provided on the μPD780078Y Subseries.

Remark The internal ROM capacity depends on the product.

3. PIN FUNCTIONS

3.1 Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P00	I/O	Port 0 4-bit input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by a software setting.		Input	INTP0
P01					INTP1
P02					INTP2
P03					INTP3/ADTRG
P10 to P17	Input	Port 1 8-bit input only port.		Input	ANI0 to ANI7
P20	I/O	Port 2 6-bit input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by a software setting.		Input	SI1
P21					SO1
P22					SCK1
P23					RxD0
P24					TxD0
P25					ASCK0
P30, P31	I/O	Port 3 7-bit input/output port. Input/output can be specified in 1-bit units.	N-ch open-drain input/output port. On-chip pull-up resistors can be specified by the mask option[Note 1]. LEDs can be driven directly.	Input	—
P32					SDA0[Note 2]
P33					SCL0[Note 2]
P34			An on-chip pull-up resistor can be specified by a software setting.		SI3/TxD2
P35					SO3/RxD2
P36					$\overline{\text{SCK3}}$/ASCK2
P40 to P47	I/O	Port 4 8-bit input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by a software setting. Interrupt request flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7
P50 to P57	I/O	Port 5 8-bit input/output port. LEDs can be driven directly. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by a software setting.		Input	A8 to A15
P64	I/O	Port 6 4-bit input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by a software setting.		Input	$\overline{\text{RD}}$
P65					$\overline{\text{WR}}$
P66					$\overline{\text{WAIT}}$
P67					ASTB

Notes 1. With the μPD780078Y Subseries, on-chip pull-up resistors can be specified using a mask option for P30 and P31.

2. These pins are only provided on the μPD780078Y Subseries.

3.1 Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P70	I/O	Port 7 6-bit input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by a software setting.	Input	TI000/TO00
P71				TI010
P72				TI50/TO50
P73				TI51/TO51
P74				TI011/PCL
P75				TI001/TO01/BUZ
P80	I/O	Port 8 1-bit input/output port. Input/output can be specified in 1-bit units. On-chip pull-up resistor can be specified by a software setting.	Input	$\overline{SS1}$

3.2 Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0 to INTP2	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.	Input	P00 to P02
INTP3				P03/ADTRG
SI1	Input	Serial interface serial data input.	Input	P20
SI3				P34/TxD2
SO1	Output	Serial interface serial data output.	Input	P21
SO3				P35/RxD2
SDA0[Note]	I/O	Serial interface serial data input/output.	Input	P32
SCK1	I/O	Serial interface serial clock input/output.	Input	P22
$\overline{SCK3}$				P36/ASCK2
SCL0[Note]				P33
$\overline{SS1}$	Input	Serial interface chip select input.	Input	P80
RxD0	Input	Serial data input for asynchronous serial interface.	Input	P23
RxD2				P35/SO3
TxD0	Output	Serial data output for asynchronous serial interface.	Input	P24
TxD2				P34/SI3
ASCK0	Input	Serial clock input for asynchronous serial interface.	Input	P25
ASCK2				P36/$\overline{SCK3}$
TI000	Input	External count clock input to 16-bit timer/event counter 00. Capture trigger input to capture register 000, 010 of 16-bit timer/event counter 00.	Input	P70/TO00
TI010		Capture trigger input to capture register 000 of 16-bit timer/event counter 00.		P71
TI001		External count clock input to 16-bit timer/event counter 01. Capture trigger input to capture register 001, 011 of 16-bit timer/event counter 01.		P75/TO01/BUZ
TI011		Capture trigger input to capture register 001 of 16-bit timer/event counter 01.		P74/PCL
TI50		External count clock input to 8-bit timer/event counter 50.		P72/TO50
TI51		External count clock input to 8-bit timer/event counter 51.		P73/TO51

Note These pins are only provided on the μPD780078Y Subseries.

3.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
TO00	Output	16-bit timer/event counter 00.	Input	P70/TI000
TO01		16-bit timer/event counter 01.		P75/TI001/ BUZ
TO50		8-bit timer/event counter 50.		P72/TI50
TO51		8-bit timer/event counter 51.		P73/TI51
PCL	Output	Clock output (for trimming of main system clock and subsystem clock).	Input	P74/TI011
BUZ	Output	Buzzer output.	Input	P75/TI001/ TO01
AD0 to AD7	I/O	Lower address/data bus for extending memory externally.	Input	P40 to P47
A8 to A15	Output	Higher address bus for extending memory externally.	Input	P50 to P57
$\overline{RD}$	Output	Strobe signal output for read operation of external memory.	Input	P64
$\overline{WR}$		Strobe signal output for write operation of external memory.		P65
$\overline{WAIT}$	Input	Inserting wait for accessing external memory.	Input	P66
ASTB	Output	Strobe output which externally latches address information output to port 4 and port 5 to access external memory.	Input	P67
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
ADTRG	Input	A/D converter trigger signal input.	Input	P03/INTP3
AV_{REF}	Input	A/D converter reference voltage and analog power supply.	—	—
AV_{SS}	—	A/D converter ground potential. Set the same potential as that of V_{SS0} or V_{SS1}.	—	—
X1	Input	Connecting crystal resonator for main system clock oscillation.	—	—
X2	—		—	—
XT1	Input	Connecting crystal resonator for subsystem clock oscillation.	—	—
XT2	—		—	—
$\overline{RESET}$	Input	System reset input.	Input	—
V_{DD0}	—	Positive power supply for ports.	—	—
V_{DD1}	—	Positive power supply (except ports).	—	—
V_{SS0}	—	Ground potential of ports.	—	—
V_{SS1}	—	Ground potential (except ports).	—	—
IC	—	Internally connected. Connect directly to V_{SS0} or V_{SS1}.	—	—

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

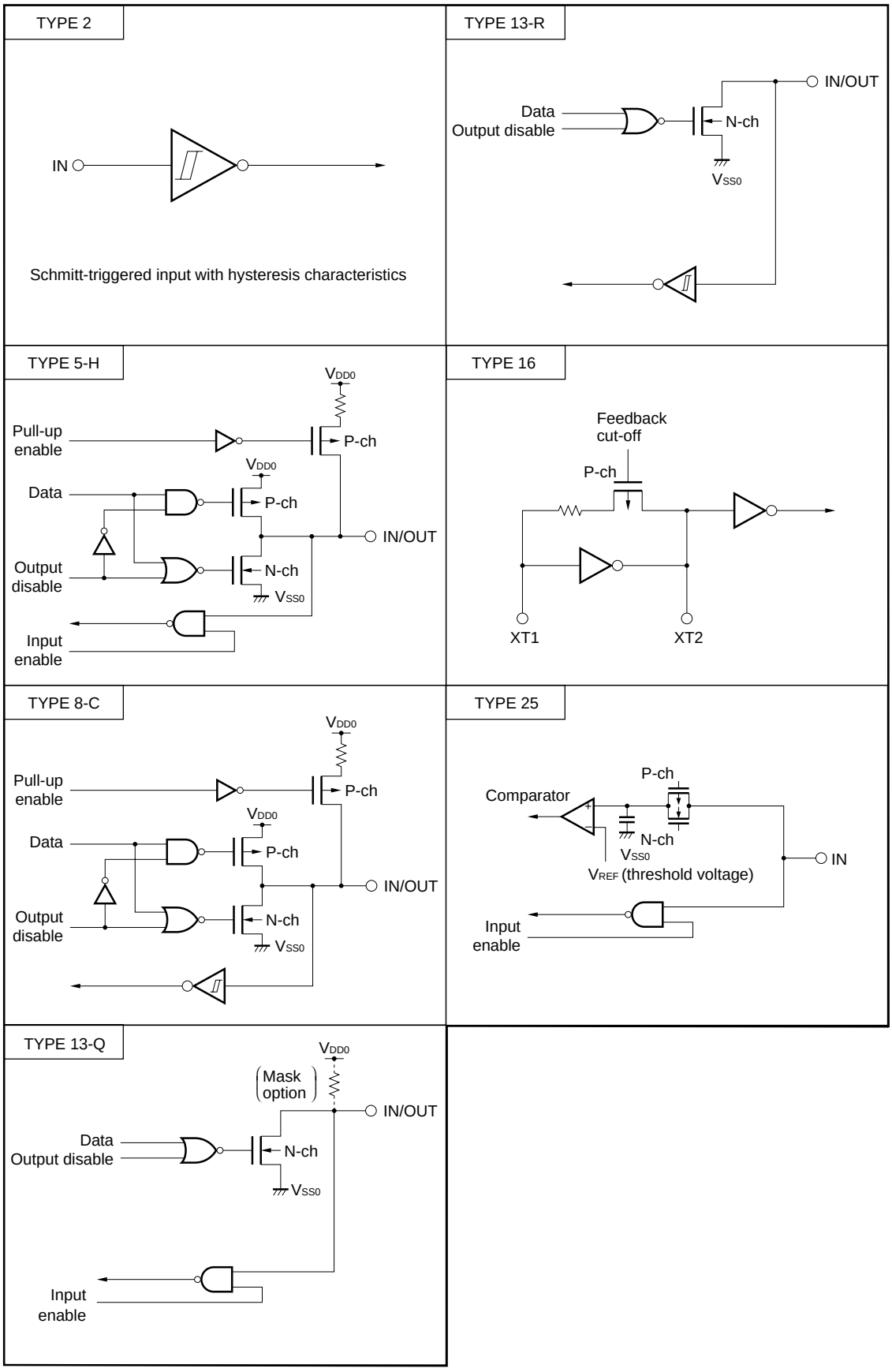
The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.

For the I/O circuit configuration of each type, see Figure 3-1.

★ **Table 3-1. Types of Pin I/O Circuits**

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0 to P02/INTP2	8-C	I/O	Input: Independently connect to V_{SS0} via a resistor.
P03/INTP3/ADTRG			Output: Leave open.
P10/ANI0 to P17/ANI7	25	Input	Connect to V_{DD0} or V_{SS0}.
P20/SI1	8-C	I/O	Input: Independently connect to V_{DD0} or V_{SS0} via a resistor.
P21/SO1	5-H		Output: Leave open.
P22/SCK1	8-C		
P23/RxD0			
P24/TxD0	5-H		
P25/ASCK0	8-C		
P30, P31	13-Q		Input: Independently connect to V_{DD0} via a resistor.
P32, P33 (μPD780078 Subseries only)			Output: Leave open.
P32/SDA0 (μPD780078Y Subseries only)	13-R		
P33/SCL0 (μPD780078Y Subseries only)			
P34/SI3/TxD2	8-C		Input: Independently connect to V_{DD0} or V_{SS0} via a resistor.
P35/SO3/RxD2			Output: Leave open.
P36/$\overline{SCK3}$/ASCK2			
P40/AD0 to P47/AD7	5-H		Input: Independently connect to V_{DD0} via a resistor. Output: Leave open.
P50/A8 to P57/A15			Input: Independently connect to V_{DD0} or V_{SS0} via a resistor.
P64/$\overline{RD}$			Output: Leave open.
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
P70/TI000/TO00	8-C		
P71/TI010			
P72/TI50/TO50			
P73/TI51/TO51			
P74/TI011/PCL			
P75/TI001/TO01/BUZ			
P80/$\overline{SS1}$			Input: Independently connect to V_{SS0} via a resistor. Output: Leave open.
$\overline{RESET}$	2	Input	—
XT1	16		Connect to V_{DD0}.
XT2		—	Leave open.
AV_{REF}	—		Connect to V_{SS0}.
AV_{SS}			
IC			Connect directly to V_{SS0} or V_{SS1}.

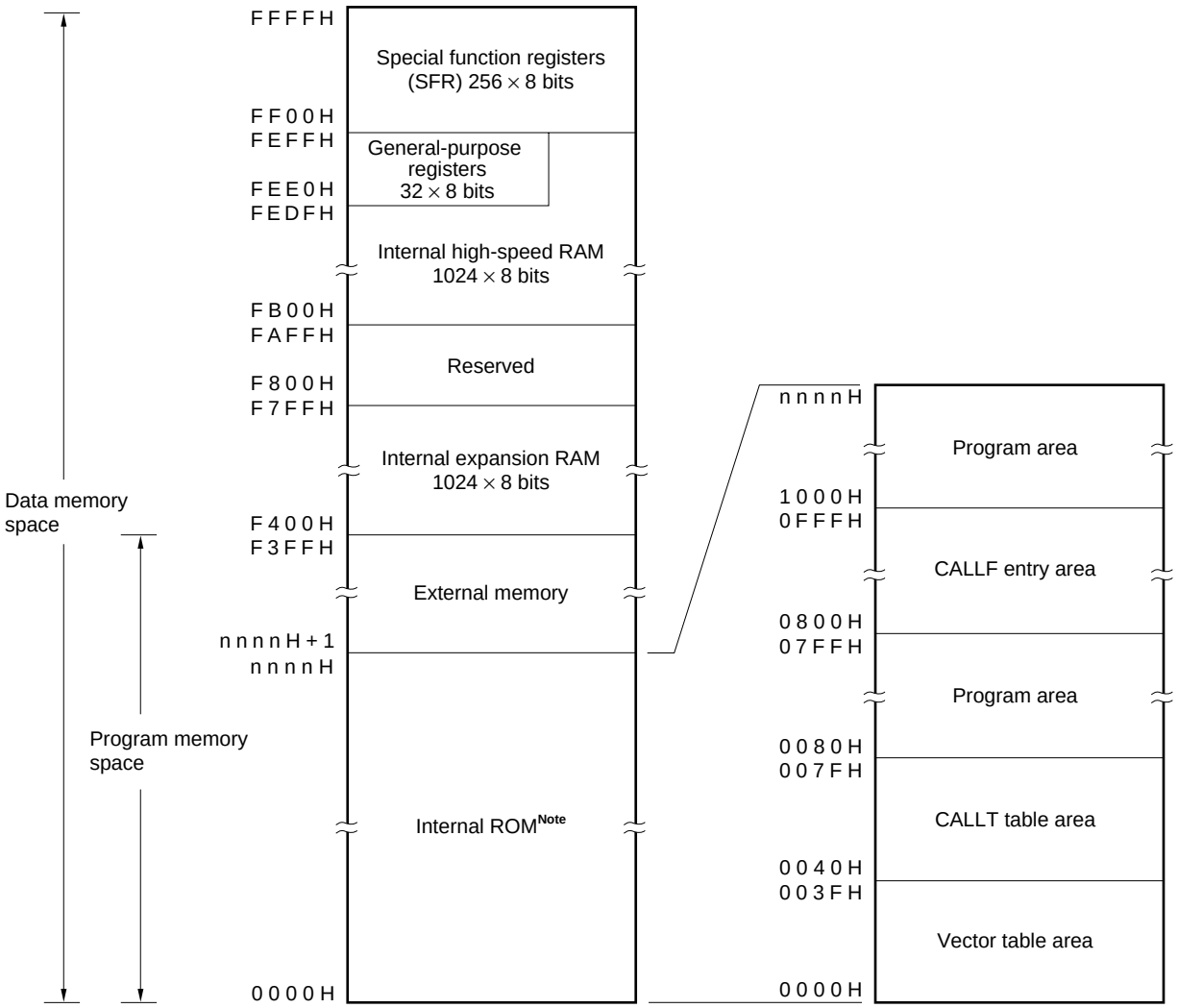
Figure 3-1. Pin I/O Circuits



4. MEMORY SPACE

Figure 4-1 shows the memory map of the μPD780076, 780078, 780076Y, and 780078Y.

Figure 4-1. Memory Map



Note The internal ROM capacity depends on the products (see the following table).

Part Number	Internal ROM Last Address nnnnH	Internal ROM Capacity
μPD780076, 780076Y	BFFFH	49152 × 8 bits
μPD780078, 780078Y	EFFFH	61440 × 8 bits

5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 Ports

The following 3 types of I/O ports are available.

- CMOS input (Port 1): 8
- CMOS input/output (Port 0, 2, P34 to P36, Port 4 to 8): 40
- N-channel open-drain input/output (P30 to P33): 4

Total: 52

Table 5-1. Port Functions

Name	Pin Name	Function
Port 0	P00 to P03	Input/output port pins. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by a software setting.
Port 1	P10 to P17	Input-only port pins.
Port 2	P20 to P25	Input/output port pins. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by a software setting.
Port 3	P30 to P33	N-ch open-drain input/output port pins. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by a mask option[Note]. LEDs can be driven directly.
	P34 to P36	Input/output port pins. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by a software setting.
Port 4	P40 to P47	Input/output port pins. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by a software setting. Test input flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	Input/output port pins. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by a software setting. LEDs can be driven directly.
Port 6	P64 to P67	Input/output port pins. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by a software setting.
Port 7	P70 to P75	Input/output port pins. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by a software setting.
Port 8	P80	Input/output port pins. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by a software setting.

Note With the μPD780078Y Subseries, on-chip pull-up resistors can be specified using a mask option for P30 and P31.

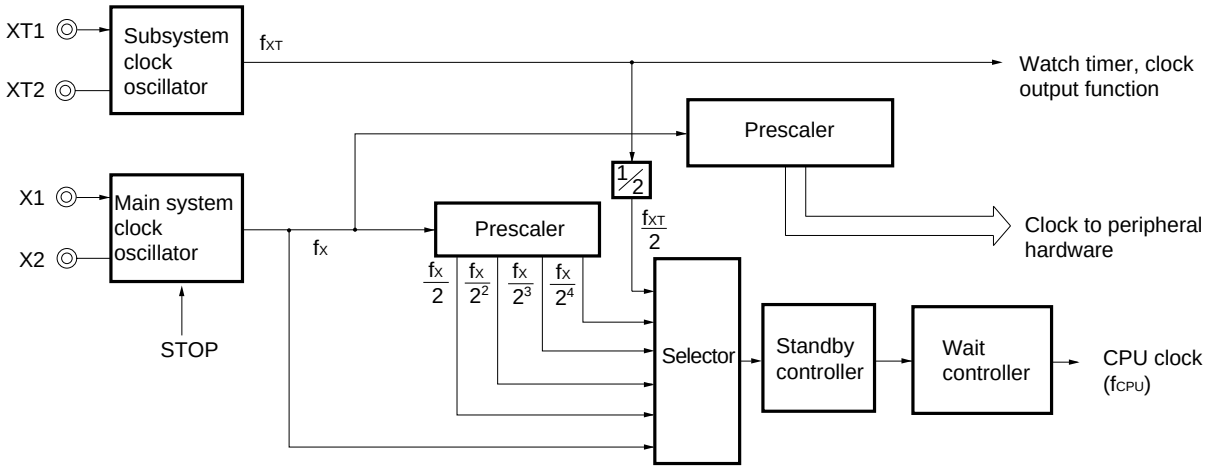
5.2 Clock Generator

A system clock generator is incorporated.

The minimum instruction execution time can be changed.

- 0.24 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (at 8.38 MHz operation with main system clock)
- 122 μs (at 32.768 kHz operation with subsystem clock)

Figure 5-1. Block Diagram of Clock Generator



5.3 Timer/Event Counter

Six timer/event counter channels are incorporated.

- 16-bit timer/event counter: 2 channels
- 8-bit timer/event counter: 2 channels
- Watch timer: 1 channel
- Watchdog timer: 1 channel

★ **Table 5-2. Operations of Timer/Event Counter**

		16-Bit Timer/Event Counter 00, 01	8-Bit Timer/Event Counter 50, 51	Watch Timer	Watchdog Timer
Operation mode	Interval timer	2 channels	2 channels	1 channel[Note 1]	1 channel[Note 2]
	External event counter	2 channels	2 channels	—	—
Function	Timer output	2 outputs	2 outputs	—	—
	PWM output	—	2 outputs	—	—
	PPG output	2 outputs	—	—	—
	Pulse width measurement	4 inputs	—	—	—
	Square wave output	2 outputs	2 outputs	—	—
	Interrupt source	4	2	2	1

Notes 1. The watch timer can perform both watch timer and interval timer functions at the same time.

2. The watchdog timer has the watchdog timer and interval timer functions. However, use the watchdog timer by selecting either the watchdog timer function or the interval timer function.

Figure 5-2. Block Diagram of 16-Bit Timer/Event Counter 00

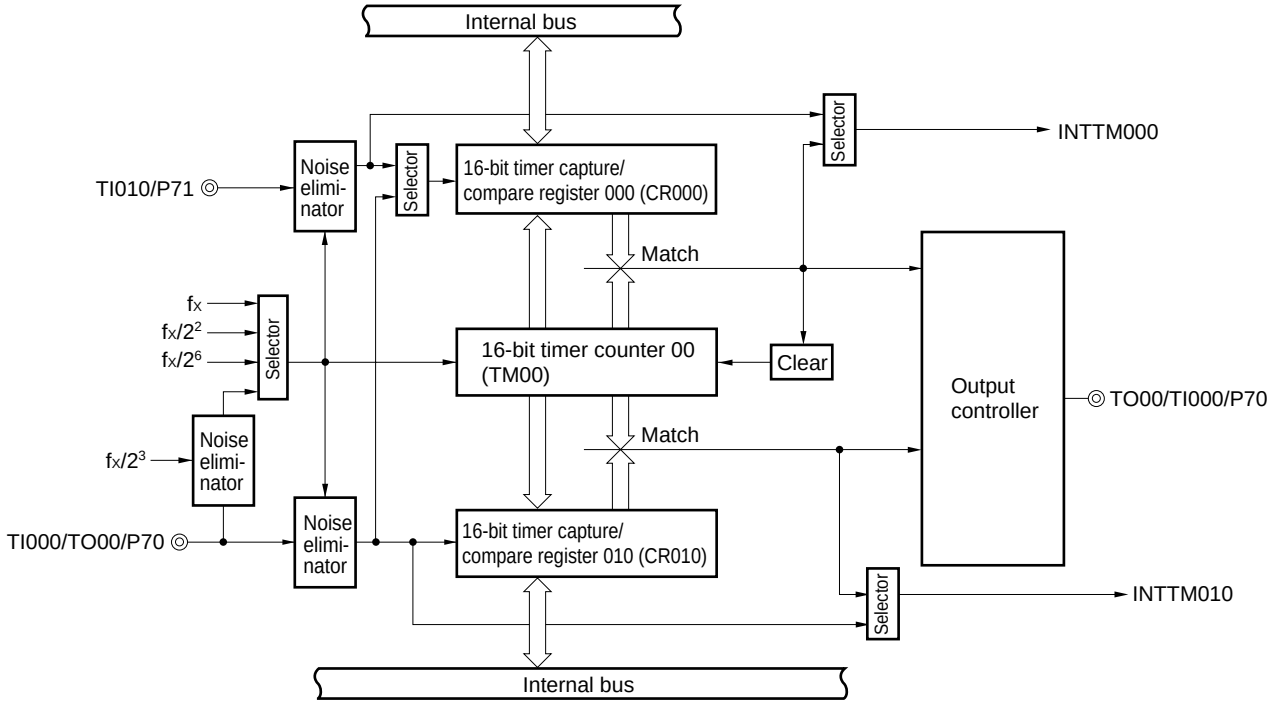
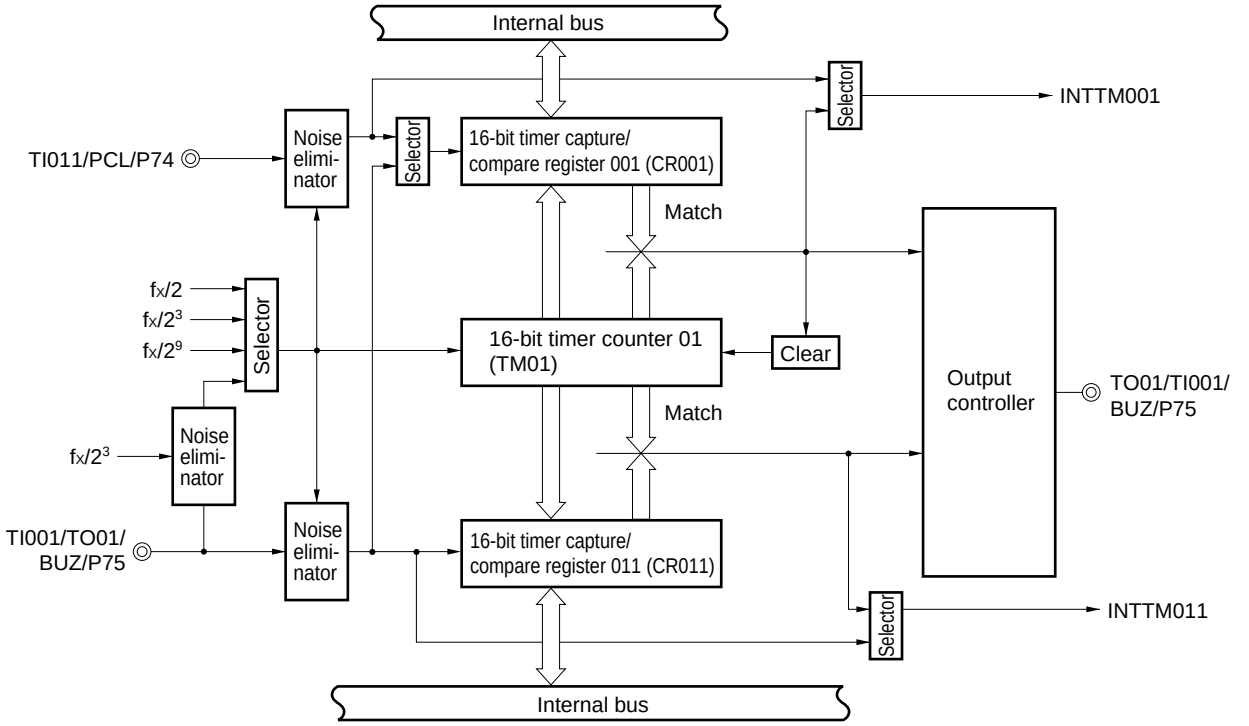


Figure 5-3. Block Diagram of 16-Bit Timer/Event Counter 01



Remark 16-bit timer/event counter 01 shares pins with the clock output (PCL) and buzzer output (BUZ) functions, in addition to the port function.

Figure 5-4. Block Diagram of 8-Bit Timer/Event Counter 50

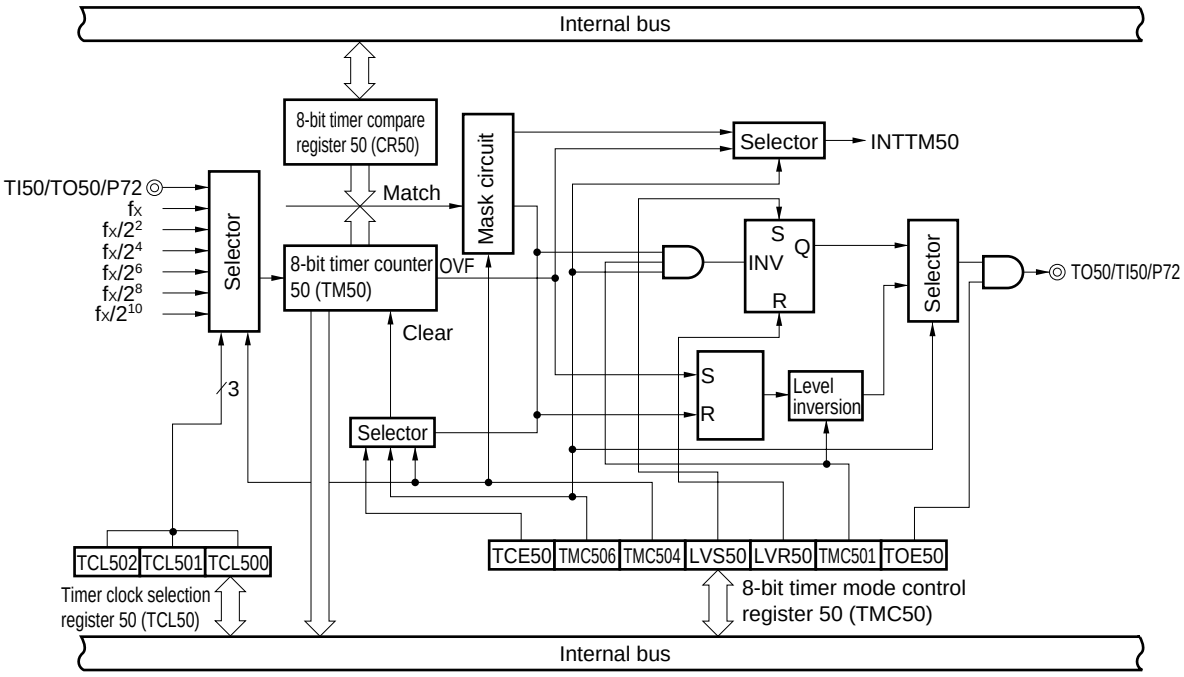
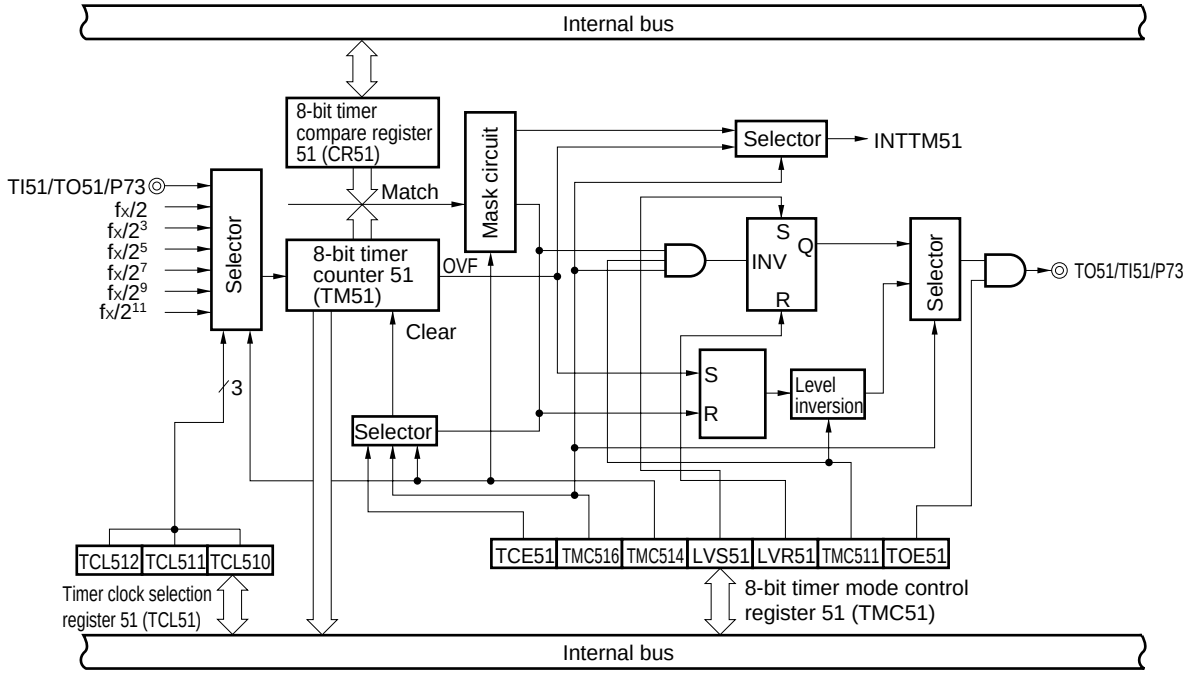
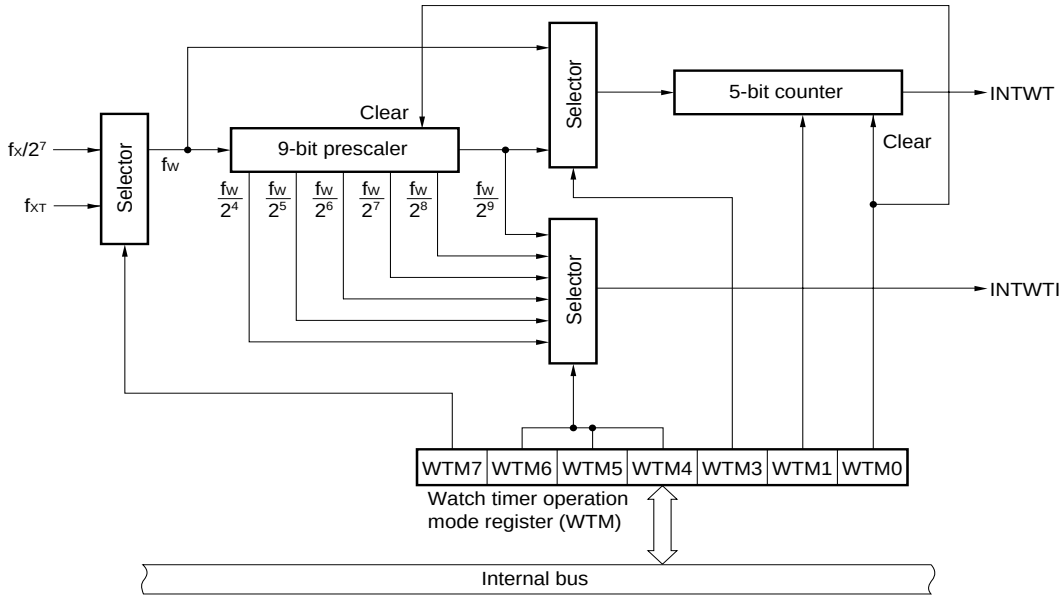


Figure 5-5. Block Diagram of 8-Bit Timer/Event Counter 51



★ **Figure 5-6. Block Diagram of Watch Timer**

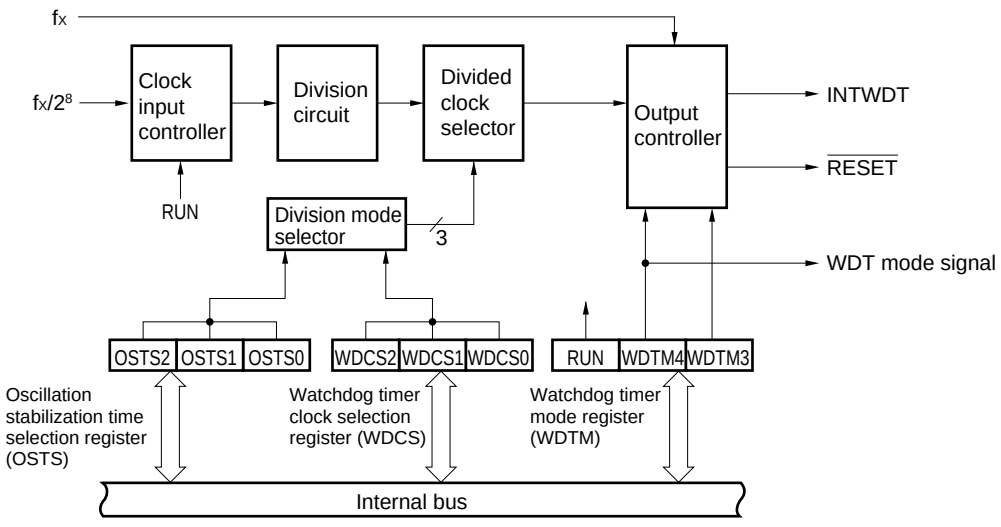


Remark f_X: Main system clock oscillation frequency

f_{XT}: Subsystem clock oscillation frequency

f_W: Watch timer clock frequency

Figure 5-7. Block Diagram of Watchdog Timer



5.4 Clock Output/Buzzer Output Controller

A clock output/buzzer output control circuit (CKU) is incorporated.

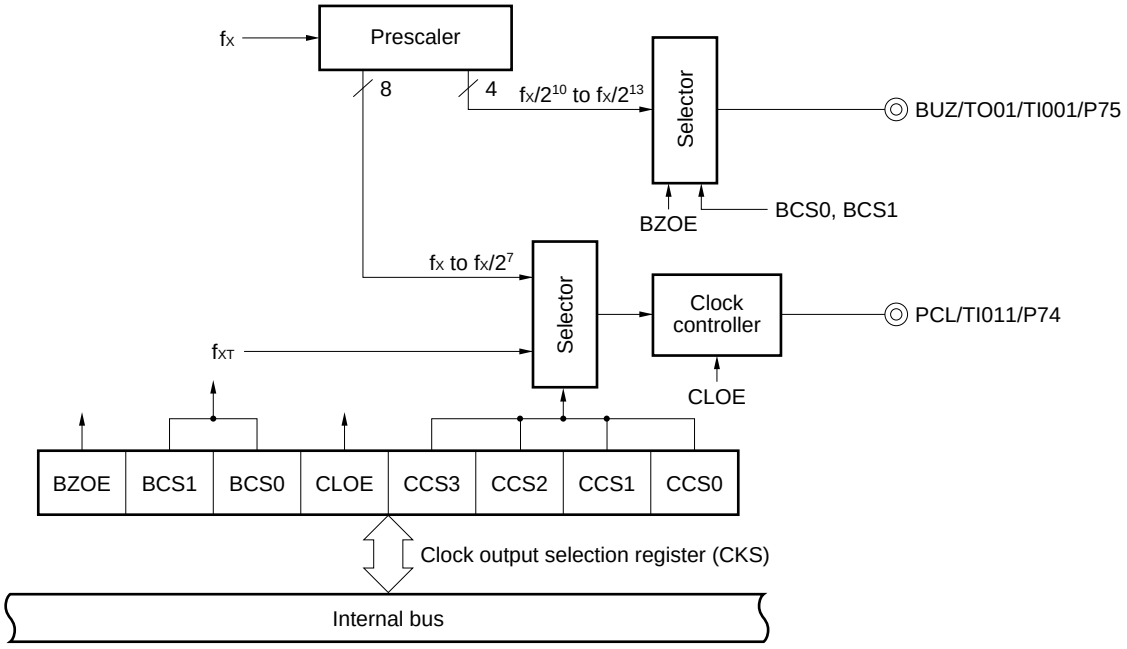
Clocks with the following frequencies can be output as clock output.

- 65.5 kHz/131 kHz/262 kHz/524 kHz/1.05 MHz/2.10 MHz/4.19 MHz/8.38 MHz (at 8.38 MHz operation with main system clock)
- 32.768 kHz (at 32.768 kHz operation with subsystem clock)

Clocks with the following frequencies can be output as buzzer output.

- 1.02 kHz/2.05 kHz/4.10 kHz/8.19 kHz (at 8.38 MHz operation with main system clock)

Figure 5-8. Block Diagram of Clock Output/Buzzer Output Controller



Remark The clock output/buzzer output controller shares pins with 16-bit timer/event counter 01, in addition to the port function.

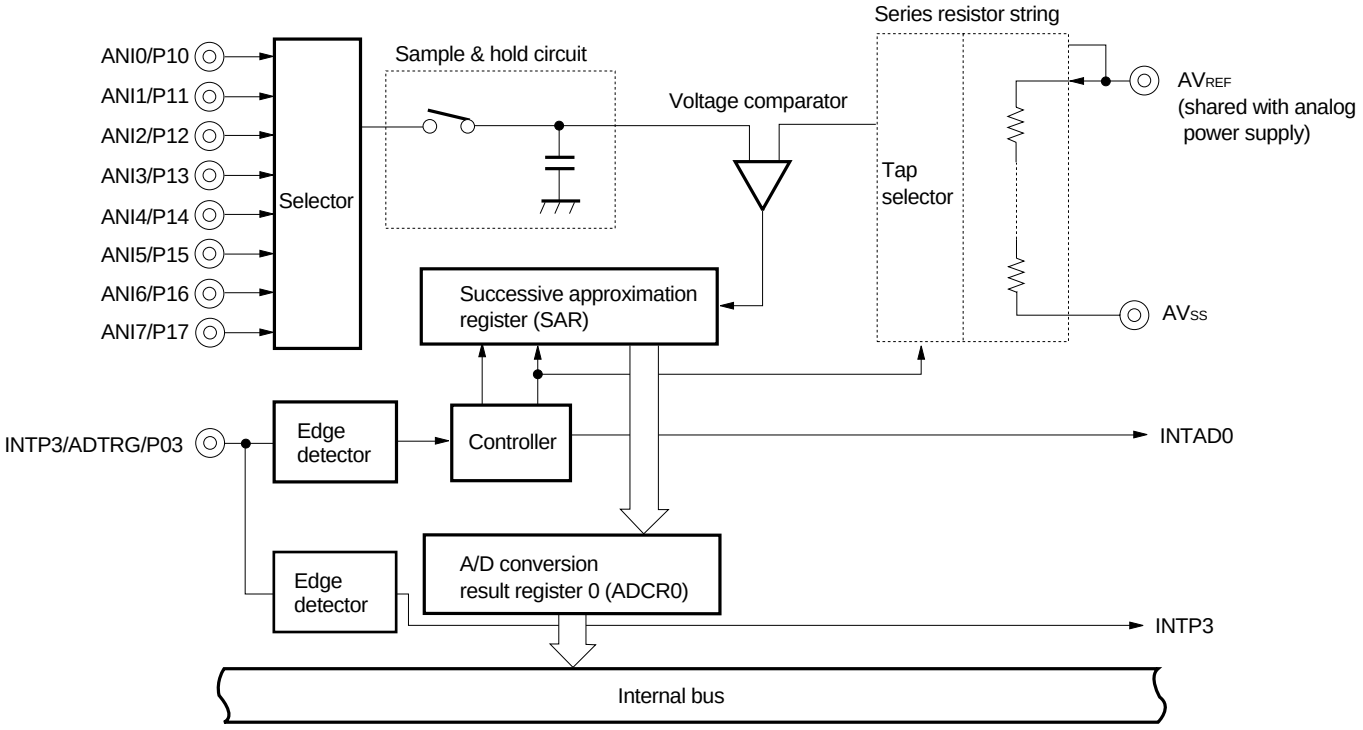
5.5 A/D Converter

An A/D converter of 10-bit resolution × 8 channels is incorporated.

The following two A/D conversion operation start-up methods are available.

- Hardware start
- Software start

Figure 5-9. Block Diagram of A/D Converter



5.6 Serial Interface

Three channels of the serial interface are incorporated (four channels for the μPD780078Y Subseries).

- Serial interface UART0
- Serial interface UART2/SIO3
- Serial interface CSI1
- Serial interface IIC0 (μPD780078Y Subseries only)

(1) Serial interface UART0

The serial interface UART0 has two modes, asynchronous serial interface (UART) mode and infrared data transfer mode.

- **Asynchronous serial interface (UART) mode**

  This mode enables full-duplex operation wherein one byte of data is transmitted and received after the start bit.

  The on-chip dedicated UART baud rate generator enables communication using a wide range of selectable baud rates.

  In addition, a baud rate can be also defined by dividing the clock input to the ASCK0 pin.

  The dedicated UART baud rate generator can also be used to generate a MIDI-standard baud rate (31.25 Kbps).

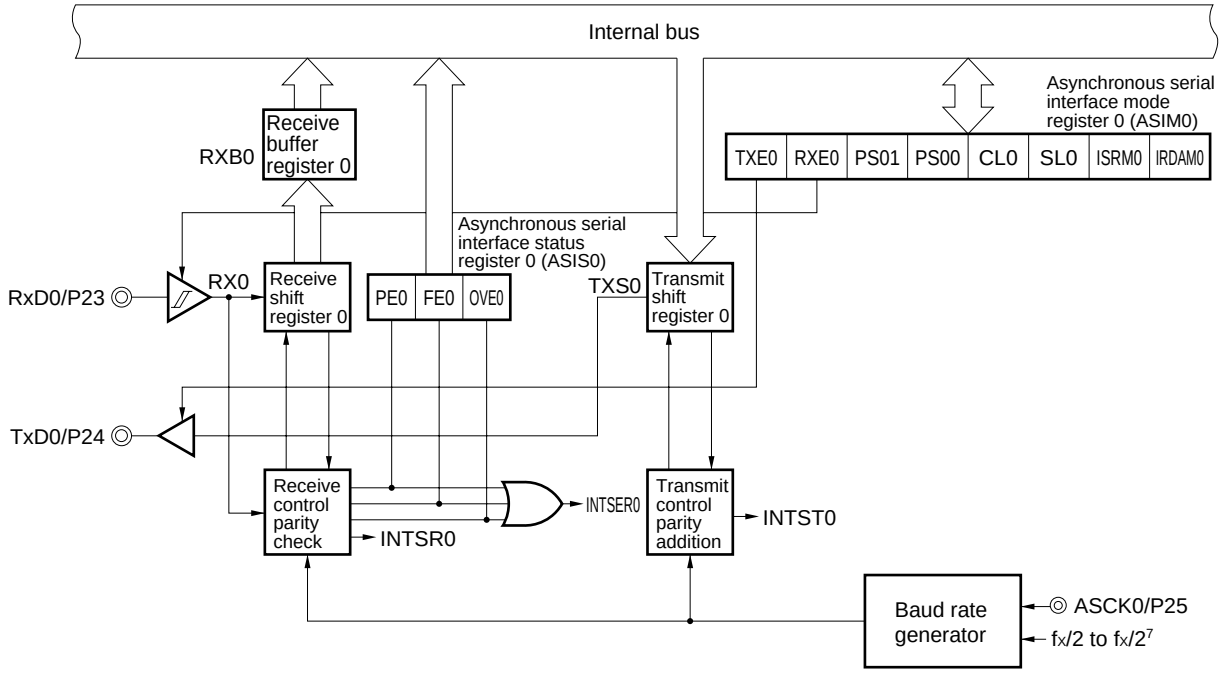
- **Infrared data transfer mode**

  This mode enables pulse output and pulse reception in an IrDA specification data format[Note].

  This mode can be used for office equipment applications such as personal computers.

Note Transfer rate differs with that of IrDA standard.

Figure 5-10. Block Diagram of Serial Interface UART0



(2) Serial interface UART2/SIO3

The serial interface UART2/SIO3 has two modes, asynchronous serial (UART) interface mode and 3-wire serial I/O mode.

Caution Do not enable UART2 and SIO3 at the same time.

(a) Serial interface UART2

The serial interface UART2 has three modes, asynchronous serial interface (UART) mode, multiprocessor transfer mode, and infrared data transfer mode.

- **Asynchronous serial interface (UART) mode**

  This mode enables full-duplex operation wherein one byte of data is transmitted and received after the start bit.

  The on-chip dedicated UART baud rate generator enables communication using a wide range of selectable baud rates.

  In addition, a baud rate can be also defined by dividing the clock input to the ASCK2 pin.

  The dedicated UART baud rate generator can also be used to generate a MIDI-standard baud rate (31.25 Kbps).

- **Multiprocessor transfer mode**

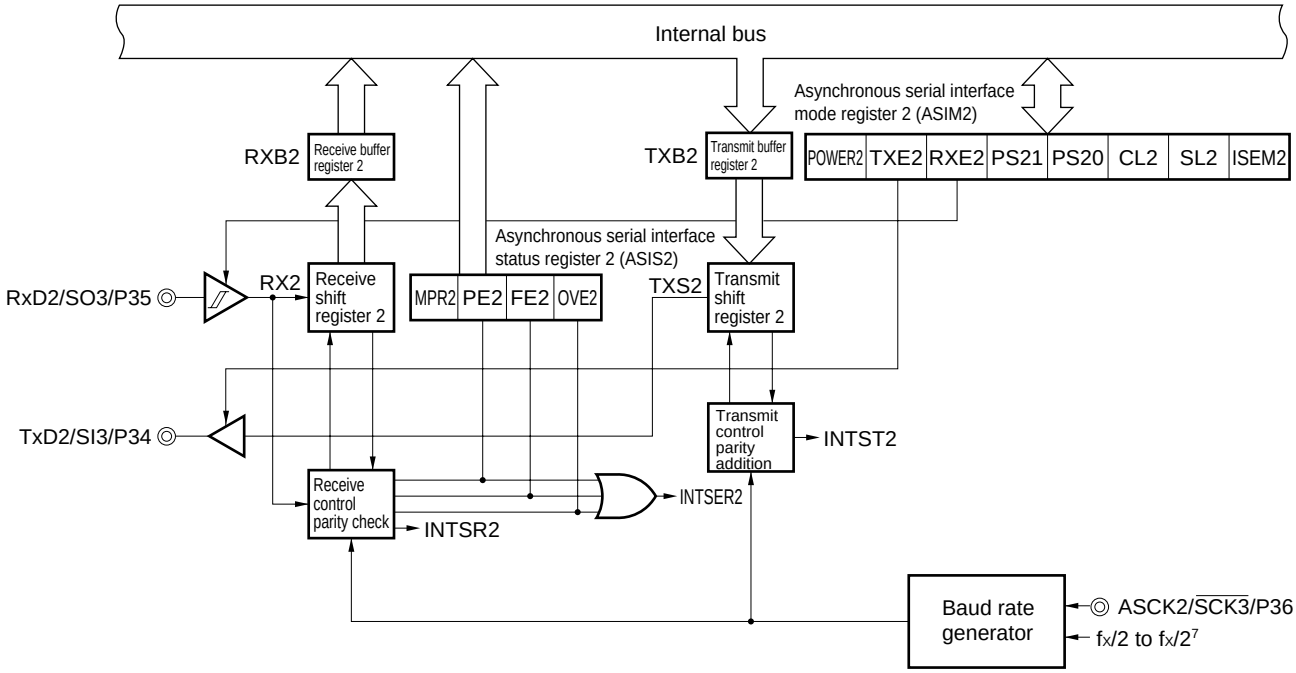
  This mode enables multiprocessor compatible data transmission/reception.

- **Infrared data transfer (IrDA) mode**

  This mode enables pulse output and pulse reception in an IrDA specification data format.

  This mode can be used for office equipment applications such as personal computers.

★ **Figure 5-11. Block Diagram of Serial Interface UART2**



(b) Serial interface SIO3

The serial interface SIO3 has the 3-wire serial I/O mode.

- **3-wire serial I/O mode (fixed as MSB first)**

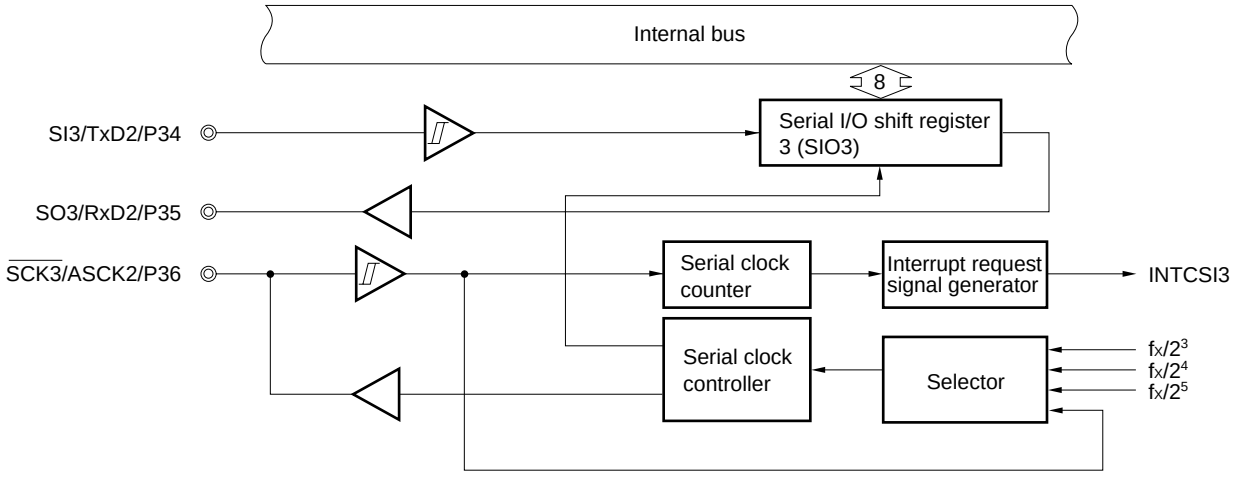
  This is an 8-bit data transfer mode using three lines: serial clock line ($\overline{\text{SCK3}}$), serial output line (SO3), and serial input line (SI3).

  Since simultaneous transmit and receive operations are available in the 3-wire serial I/O mode, the processing time for data transfer is reduced.

  The first bit in 8-bit data in the serial transfer is fixed as MSB.

  The 3-wire serial I/O mode is useful for connection to a peripheral I/O device that includes a clocked serial interface, a display controller, etc.

Figure 5-12. Block Diagram of Serial Interface SIO3



(3) Serial interface CSI1

The serial interface CSI1 has the 3-wire serial I/O mode.

- **3-wire serial I/O mode (MSB/LSB first selectable)**

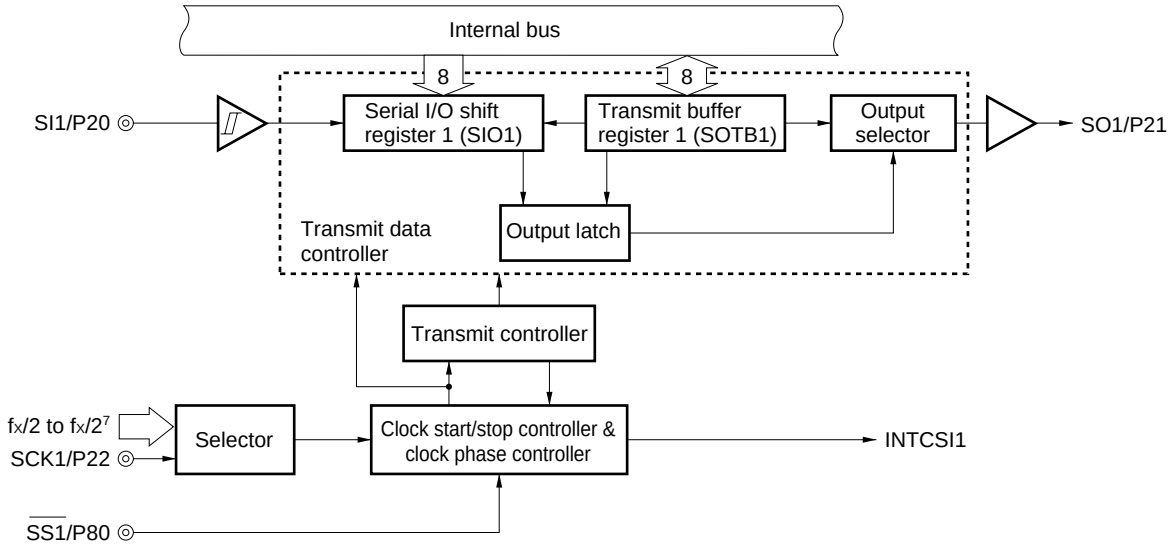
  This is an 8-bit data transfer mode using three lines: serial clock line (SCK1), serial output line (SO1), and serial input line (SI1).

  Since simultaneous transmit and receive operations are available in the 3-wire serial I/O mode, the processing time for data transfer is reduced.

  The serial transfer of 8-bit data can be switched between MSB or LSB first, enabling the chip to be connected to devices using either mode.

  The 3-wire serial I/O mode is useful for connection to a peripheral I/O device that includes a clocked serial interface, a display controller, etc.

Figure 5-13. Block Diagram of Serial Interface CSI1



(4) Serial interface IIC0 (μPD780078Y Subseries only)

The serial interface IIC0 has the I²C (Inter IC) bus mode (multimaster supported).

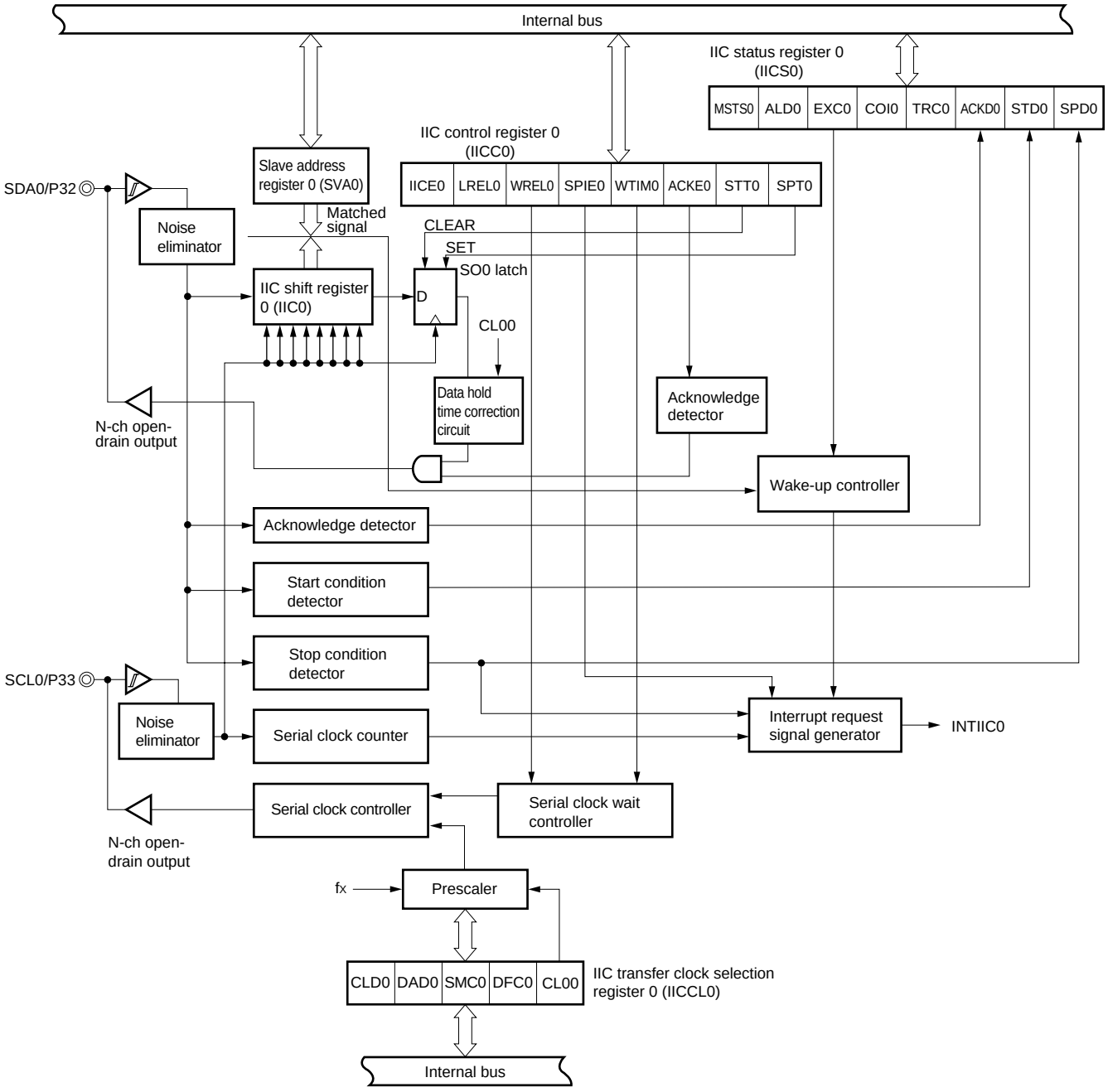
- **I²C bus mode (multimaster supported)**

  This is an 8-bit data transfer mode using two lines: serial clock line (SCL0) and serial data bus line (SDA0).

  This mode complies with the I²C bus format, and can output "start condition", "data", and "stop condition" during transmission via the serial data bus. These data are automatically detected by hardware during reception.

  Since the SCL0 and SDA0 are open-drain outputs in IIC0, pull-up resistors for the serial clock line and the serial data bus line are required.

Figure 5-14. Block Diagram of Serial Interface IIC0



6. INTERRUPT FUNCTIONS

A total of 25 interrupt sources (26 sources for the μPD780078Y Subseries) are provided, divided into the following three types.

- Non-maskable: 1
- Maskable: 23 (24 for the μPD780078Y Subseries)
- Software: 1

★ **Table 6-1. Interrupt Source List (1/2)**

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	—	INTWDT	Watchdog timer overflow (non-maskable interrupt selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTSER0	Generation of serial interface UART0 reception error	Internal	000EH	(B)
	6	INTSR0	End of serial interface UART0 reception		0010H	
	7	INTST0	End of serial interface UART0 transmission		0012H	
	8	INTCSI1	End of serial interface CSI1 transfer		0014H	
	9	INTCSI3	End of serial interface SIO3 transfer		0016H	
	10	INTIIC0[Note 3]	End of serial interface IIC0 transfer		0018H	
	11	INTWTI	Reference time interval signal from watch timer		001AH	
	12	INTTM000	Coincidence of TM00 and CR000 (when compare register is specified) or detection of valid edge of TI010 (when capture register is specified)		001CH	
	13	INTTM010	Coincidence of TM00 and CR010 (when compare register is specified) or detection of valid edge of TI000 (when capture register is specified)		001EH	
	14	INTTM50	Coincidence of TM50 and CR50		0020H	
	15	INTTM51	Coincidence of TM51 and CR51		0022H	
	16	INTAD0	End of conversion by A/D converter		0024H	
	17	INTWT	Watch timer overflow		0026H	
	18	INTKR	Falling edge detection of port 4	External	0028H	(D)

Notes 1. The default priority is a priority order when two or more maskable interrupt requests are generated simultaneously. 0 is the highest order and 23, the lowest.

2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 6-1, respectively.

3. μPD780078Y Subseries only.

Remark As the watchdog timer interrupt source (INTWDT), a non-maskable interrupt or maskable interrupt (internal) can be selected.

★ **Table 6-1. Interrupt Source List (2/2)**

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Maskable	19	INTSER2	Generation of UART2 reception error	Internal	002AH	(B)
	20	INTSR2	End of UART2 reception		002CH	
	21	INTST2	End of UART2 transmission/data transfer[Note 3]		002EH	
	22	INTTM001	Coincidence of TM01 and CR001 (when compare register specified) or detection of TI011 valid edge (when capture register specified)		0030H	
	23	INTTM011	Coincidence of TM01 and CR011 (when compare register specified) or detection of TI001 valid edge (when capture register specified)		0032H	
Software	—	BRK	BRK instruction execution	—	003EH	(E)

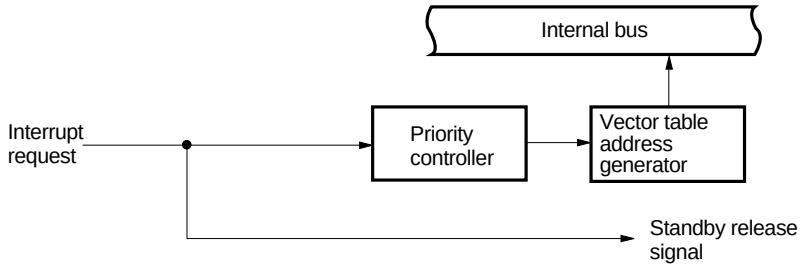
Notes 1. The default priority is a priority order when two or more maskable interrupt requests are generated simultaneously. 0 is the highest order and 23, the lowest.

2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 6-1, respectively.

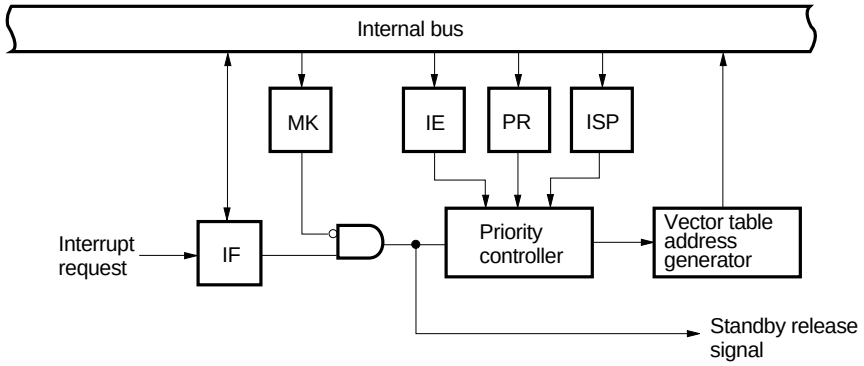
3. This source generates an interrupt request signal during data transfer from the transmit buffer register 2 (TXB2) to the transmit shift register. Interrupt sources can be selected by the transmit interrupt signal select flag (ISMD).

Figure 6-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0 to INTP3)

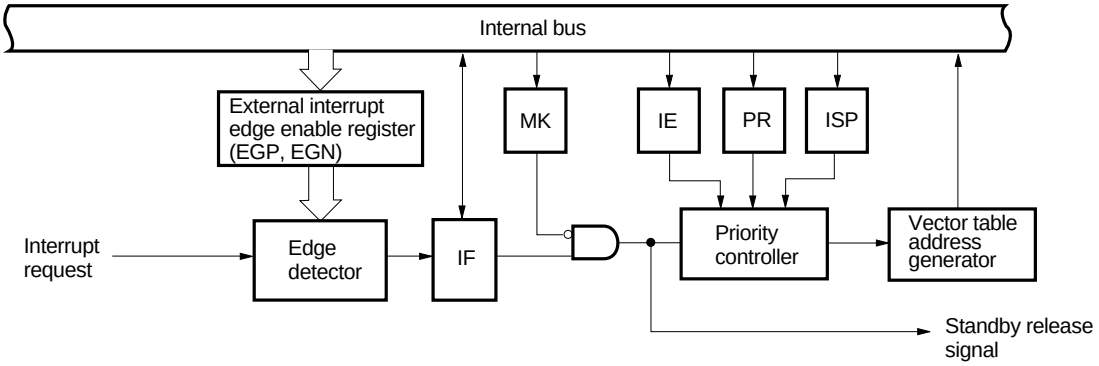
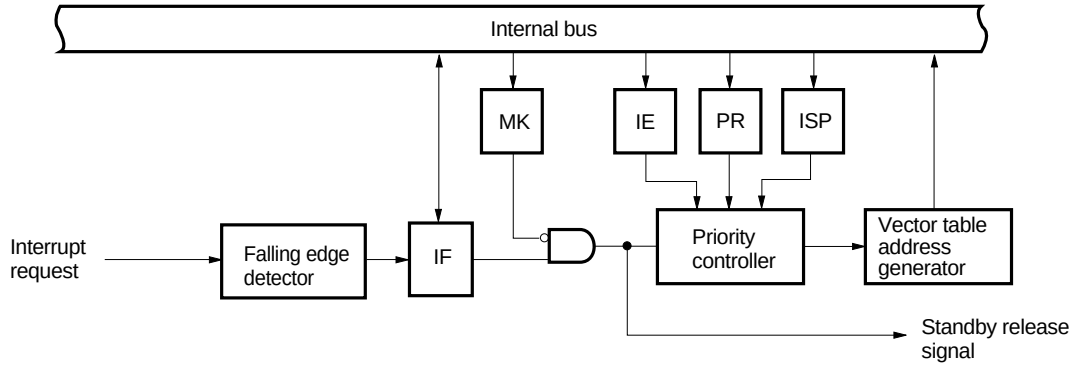
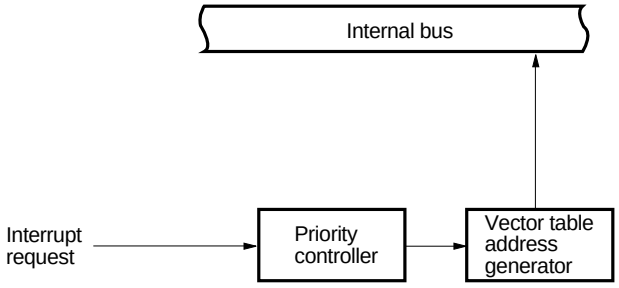


Figure 6-1. Basic Configuration of Interrupt Function (2/2)

(D) External maskable interrupt (INTKR)



(E) Software interrupt



IF: Interrupt request flag
IE: Interrupt enable flag
ISP: In-service priority flag
MK: Interrupt mask flag
PR: Priority specification flag

7. EXTERNAL DEVICE EXPANSION FUNCTIONS

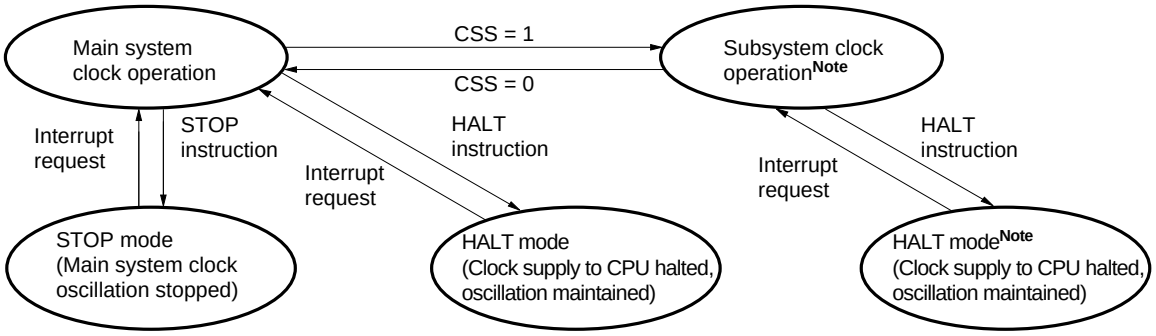
The external device expansion functions connect external devices to areas other than the internal ROM, RAM and SFR. Ports 4 to 6 are used for external device connection.

★ 8. STANDBY FUNCTION

There are the following two standby functions to reduce the consumption current.

- HALT mode: The CPU operating clock is stopped. The average consumption current can be reduced by intermittent operation in combination with the normal operating mode.
- STOP mode: The main system clock oscillation is stopped. The whole operation by the main system clock is stopped, so that the system operates with ultra-low power consumption. This mode can be used only when the main system clock is operating (it cannot be used to stop the subsystem clock).

Figure 8-1. Standby Function



Note The current consumption can be reduced by stopping the main system clock.
When the CPU is operating on the subsystem clock, set bit 7 (MCC) of the processor clock control register (PCC) to stop the main system clock. The STOP instruction cannot be used.

Caution When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

9. RESET FUNCTION

The following two reset methods are available.

- External reset by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer inadvertent program loop time detection

10. MASK OPTION

Table 10-1. Selection of Pin Mask Options

Subseries	Pin	Mask Option
μPD780078 Subseries	P30 to P33	An on-chip pull-up resistor can be specified in 1-bit units.
μPD780078Y Subseries	P30, P31	

P30 to P33[Note] on-chip pull-up resistor can be specified by mask option. The mask option can be specified in 1-bit units.

Note Only P30 and P31 can be specified on the μPD780078Y Subseries.

11. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

Second operand / First operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

First operand \ Second operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE or HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

First operand \ Second operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instructions/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

First operand \ Second operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

★ 12. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	AV_{REF}			–0.3 to V_{DD} + 0.3[Note]	V
	AV_{SS}			–0.3 to +0.3[Note]	V
Input voltage	V_{I1}	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, P80, X1, X2, XT1, XT2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3[Note]	V
	V_{I2}	P30 to P33	N-ch open-drain	–0.3 to V_{DD} + 0.3[Note]	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3[Note]	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pin	AV_{SS} – 0.3 to AV_{REF} + 0.3 and –0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin		–10	mA
		Total for P00 to P03, P40 to P47, P50 to P57, P64 to P67, P70 to P75, P80		–15	mA
		Total for P20 to P25, P30 to P36		–15	mA
Output current, low	I_{OL}	Per pin for P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75, P80		20	mA
		Per pin for P30 to P33, P50 to P57		30	mA
		Total for P00 to P03, P40 to P47, P64 to P67, P70 to P75, P80		50	mA
		Total for P20 to P25		20	mA
		Total for P30 to P36		100	mA
		Total for P50 to P57		100	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–40 to +150	°C

Note 6.5 V or below.

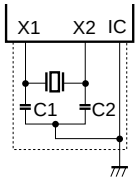
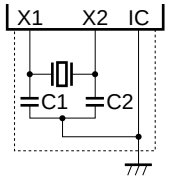
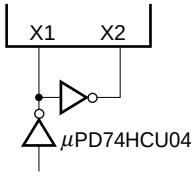
Caution Product quality may suffer if the absolute maximum rating is exceeded for even single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions ensuring that the absolute maximum ratings are not exceeded.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V.	P00 to P03, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, P80			15	pF
			P30 to P33			20	pF

Remark Unless specified otherwise, alternate-function pin characteristics are the same as port pin characteristics.

Main System Clock Oscillator Characteristics (T_A = –40 to 85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)**Note 1**	V_{DD} = 4.0 to 5.5 V	1.0		8.38	MHz
				1.0		5.0	MHz
		Oscillation stabilization time**Note 2**	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)**Note 1**	V_{DD} = 4.0 to 5.5 V	1.0		8.38	MHz
				1.0		5.0	MHz
		Oscillation stabilization time**Note 2**	V_{DD} = 4.0 to 5.5 V			10	ms
						30	ms
External clock		X1 input frequency (f_X)**Note 1**	V_{DD} = 4.0 to 5.5 V	1.0		8.38	MHz
						5.0	MHz
		X1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 4.0 to 5.5 V	50		500	ns
				85		500	ns

Notes 1. Indicates only oscillator characteristics.

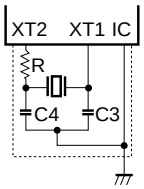
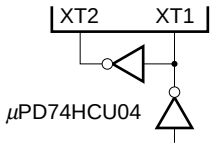
2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wiring in the area enclosed with the broken line in the above figures should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a line through which a high fluctuating current flows.**
- **Always keep the ground point of the oscillator to the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern in which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})**Note 1**		32	32.768	35	kHz
		Oscillation stabilization time**Note 2**	V_{DD} = 4.0 to 5.5 V		1.2	2	s
						10	s
External clock		XT1 input frequency (f_{XT})**Note 1**		32		38.5	kHz
		XT1 input high-/low- level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Indicates only oscillator characteristics.

2. Time required to stabilize oscillation after V_{DD} reaches oscillation voltage MIN.

Cautions 1. When using the subsystem clock oscillator, wiring in the area enclosed with the broken line in the above figures should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a line through which a high fluctuating current flows.**
- **Always keep the ground point of the oscillator to the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern in which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is a low-amplitude circuit in order to achieve a low consumption current, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Recommended Oscillator Constant

Main system clock: Ceramic resonator (T_A = –45 to +85°C)

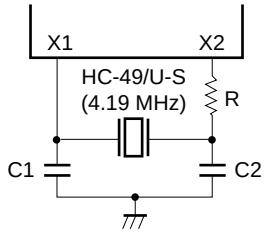
Manufacturer	Part Number	Frequency	Recommended Circuit Constant		Oscillation Voltage Range		Remarks
		(MHz)	C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
Murata Mfg. Co., Ltd.	CSB1000J	1.00	150	150	1.8	5.5	–
	CSBF1000J						
	CSA2.00MG040	2.00	100	100			
	CST2.00MG040		On-chip	On-chip			
	CSTCC2.00MG0H6				2.0	5.5	
	CSA3.58MG	3.58	30	30	1.8	5.5	
	CST3.58MGW		On-chip	On-chip			
	CSTCC3.58MG0H6				2.0	5.5	
	CSA4.00MG	4.00	30	30	1.8	5.5	
	CSTS0400MH06		On-chip	On-chip			
	CSTCC4.0MG0H6				2.0	5.5	
	CSA4.19MG	4.19	30	30	1.8	5.5	
	CSTS0419MG06		On-chip	On-chip			
	CSTCC4.19MG0H6				2.0	5.5	
	CSA4.91MG	4.91	30	30	1.8	5.5	
	CSTS0491MG03		On-chip	On-chip			
	CSTCC4.91MG0H6				2.0	5.5	
	CSA5.00MG	5.00	30	30	1.8	5.5	
	CSTS0500MG03		On-chip	On-chip			
	CSTCC5.00MG0H6				2.0	5.5	
	CSA8.00MTZ	8.00	30	30	4.0	5.5	
	CSTS0800MG03		On-chip	On-chip			
	CSTCC8.00MG						
	CSA8.38MTZ	8.38	30	30			
	CSTS0838MG03		On-chip	On-chip			
	CSTCC8.38MG						
TDK	CCR3.58MC3	3.58	On-chip	On-chip	1.8	5.5	
	CCR4.0MC3	4.00					
	CCR4.19MC3	4.19					
	CCR5.0MC3	5.00					
	CCR6.0MC3	6.00			4.0	5.5	
	CCR8.0MC5	8.00					
	CCR8.38MC5	8.38					

Caution The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. Oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation frequency must be adjusted on the implementation circuit. For details please contact directly the manufacturer of the resonator you will use.

Main system clock: Crystal resonator (T_A = –10 to +70°C)

Manufacturer	Part Number	Frequency	Recommended Circuit Constant		Oscillation Voltage Range		Remarks
		(MHz)	C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
Kinseki, Ltd.	HC-49/U-S[Note]	4.19	18	18	1.9	5.5	R = 4.7 kΩ
		8.38	27	27	4.0	5.5	–

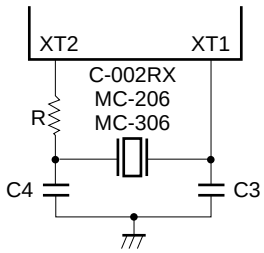
Note A limiting resistor (R = 4.7 kΩ) is required when the HU-49/U-S manufactured by Kinseki, Ltd. is used as the ceramic resonator (see the figure below) at f_X = 4.19 MHz.



Subsystem clock: Crystal resonator (T_A = –40 to +85°C)

Manufacturer	Part Number	Frequency	Recommended Circuit Constant		Oscillation Voltage Range		Remarks
		(MHz)	C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
Seiko Epson Inc.	C-002RX[Note] MC-206[Note] MC-306[Note]	32.768	15	15	1.8	5.5	R = 330 kΩ

Note A limiting resistor (R = 330 kΩ) is required when the C-002RX, MC-206, or MC-306 manufactured by Seiko Epson Inc. is used as the ceramic resonator (see the figure below).



Caution The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. Oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation frequency must be adjusted on the implementation circuit. For details please contact directly the manufacturer of the resonator you will use.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin				–1	mA
		All pins				–15	mA
Output current, low	I_{OL}	Per pin for P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75, P80				10	mA
		Per pin for P30 to P33, P50 to P57				15	mA
		Total for P00 to P03, P40 to P47, P64 to P67, P70 to P75, P80				20	mA
		Total for P20 to P25				10	mA
		Total for P30 to P36				70	mA
		Total for P50 to P57				70	mA
Input voltage, high	V_{IH1}	P10 to P17, P21, P24, P40 to P47, P50 to P57, P64 to P67	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				0.8V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P03, P20, P22, P23, P25, P34 to P36, P70 to P75, P80, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0.8V_{DD}		V_{DD}	V
				0.85V_{DD}		V_{DD}	V
	V_{IH3}	P30 to P33 (N-ch open-drain)	V_{DD} = 2.7 to 5.5 V	0.7V_{DD}		V_{DD}	V
				0.8V_{DD}		V_{DD}	V
	V_{IH4}	X1, X2	V_{DD} = 2.7 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
				V_{DD} – 0.2		V_{DD}	V
	V_{IH5}	XT1, XT2	V_{DD} = 4.0 to 5.5 V	0.8V_{DD}		V_{DD}	V
				0.9V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P17, P21, P24, P40 to P47, P50 to P57, P64 to P67	V_{DD} = 2.7 to 5.5 V	0		0.3V_{DD}	V
				0		0.2V_{DD}	V
	V_{IL2}	P00 to P03, P20, P22, P23, P25, P34 to P36, P70 to P75, P80, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 5.5 V	0		0.2V_{DD}	V
				0		0.15V_{DD}	V
	V_{IL3}	P30 to P33 (N-ch open-drain)	4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
			2.7 V ≤ V_{DD} < 4.0 V	0		0.2V_{DD}	V
			1.8 V ≤ V_{DD} < 2.7 V	0		0.1V_{DD}	V
	V_{IL4}	X1, X2	V_{DD} = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
	V_{IL5}	XT1, XT2	V_{DD} = 4.0 to 5.5 V	0		0.2V_{DD}	V
				0		0.1V_{DD}	V
Output voltage, high	V_{OH1}	I_{OH} = –1 mA	V_{DD} = 4.0 to 5.5 V	V_{DD} – 1.0		V_{DD}	V
		I_{OH} = –100 μA	V_{DD} = 1.8 to 5.5 V	V_{DD} – 0.5		V_{DD}	V
Output voltage, low	V_{OL1}	P30 to P33	V_{DD} = 4.0 to 5.5 V, I_{OL} = 15 mA			2.0	V
	V_{OL2}	P50 to P57	V_{DD} = 4.0 to 5.5 V, I_{OL} = 15 mA		0.4	2.0	V
	V_{OL3}	P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75, P80	V_{DD} = 4.0 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL4}	I_{OL} = 400 μA				0.5	V

Remark Unless specified otherwise, alternate-function pin characteristics are the same as port pin characteristics.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, P80, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
	I_{LIH3}	V_{IN} = 5.5 V	P30 to P33			3	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, P80, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
	I_{LIL3}		P30 to P33			–3	μA
Output leakage current, high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Mask option pull-up resistor	R_1	V_{IN} = 0 V, P30, P31, P32[Note], P33[Note]		15	30	90	kΩ
Software pull-up resistor	R_2	V_{IN} = 0 V, P00 to P03, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, P80		15	30	90	kΩ

Note μPD780078 Subseries only.

Remark Unless specified otherwise, alternate-function pin characteristics are the same as port pin characteristics.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}[Note 2]	8.38 MHz crystal oscillation operating mode	V_{DD} = 5.0 V ±10%[Note 3]	When A/D converter stopped		5.5	11.0	mA
				When A/D converter is operating		6.5	13.0	mA
		5.0 MHz crystal oscillation operating mode	V_{DD} = 3.0 V ±10%[Note 3]	When A/D converter stopped		2.0	4.0	mA
				When A/D converter is operating		3.0	6.0	mA
			V_{DD} = 2.0 V ±10%[Note 4]	When A/D converter stopped		0.4	1.5	mA
				When A/D converter is operating		1.4	4.2	mA
	I_{DD2}	8.38 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ±10%[Note 3]	When peripheral function stopped		1.1	2.2	mA
				When peripheral function is operating			4.7	mA
		5.0 MHz crystal oscillation HALT mode	V_{DD} = 3.0 V ±10%[Note 3]	When peripheral function stopped		0.35	0.7	mA
				When peripheral function is operating			1.7	mA
			V_{DD} = 2.0 V ±10%[Note 4]	When peripheral function stopped		0.15	0.4	mA
				When peripheral function is operating			1.1	mA
	I_{DD3}	32.768 kHz crystal oscillation operating mode[Note 5]	V_{DD} = 5.0 V ±10%			40	80	μA
			V_{DD} = 3.0 V ±10%			20	40	μA
			V_{DD} = 2.0 V ±10%			10	20	μA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode[Note 5]	V_{DD} = 5.0 V ±10%			30	60	μA
			V_{DD} = 3.0 V ±10%			6	18	μA
			V_{DD} = 2.0 V ±10%			2	10	μA
	I_{DD5}	STOP mode	V_{DD} = 5.0 V ±10%			0.1	30	μA
			V_{DD} = 3.0 V ±10%			0.05	10	μA
			V_{DD} = 2.0 V ±10%			0.05	10	μA

Notes 1. Total current flowing in the internal power supply (V_{DD0}, V_{DD1}).

2. Includes the peripheral operating current. However, the pull-up resistor on the port and the current flowing in the AV_{REF} pin are not included.

3. When the processor clock control register (PCC) is set to 00H.

4. When PCC is set to 02H.

5. When the main system clock has been stopped.

AC Characteristics

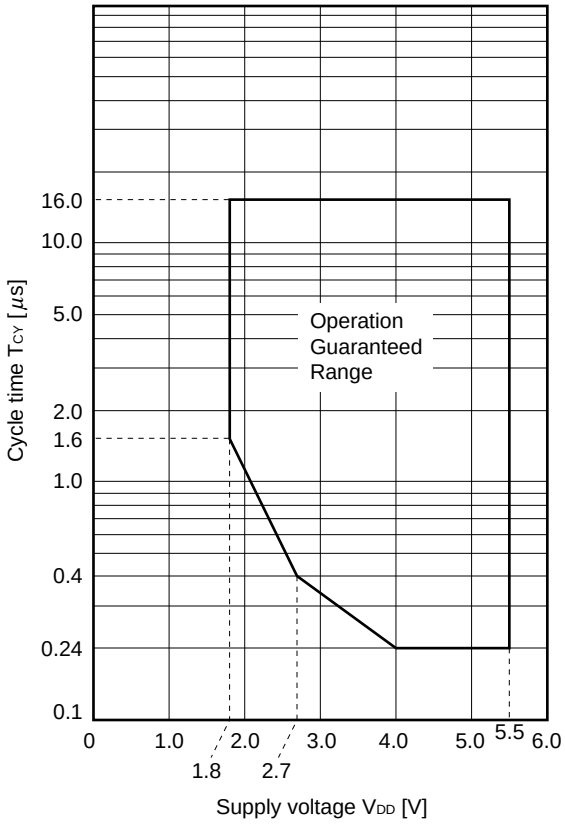
(1) Basic operation (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating with main system clock	4.0 V ≤ V_{DD} ≤ 5.5 V	0.24		16	μs
			2.7 V ≤ V_{DD} < 4.0 V	0.4		16	μs
			1.8 V ≤ V_{DD} < 2.7 V	1.6		16	μs
		Operating with subsystem clock		103.9 Note 1	122	125	μs
TI000, TI010, TI001, TI011 input high-/low-level width	t_{TIH0} t_{TIL0}		3.5 V ≤ V_{DD} ≤ 5.5 V	$2/f_{sam}$ + 0.1 Note2			μs
			2.7 V ≤ V_{DD} < 3.5 V	$2/f_{sam}$ + 0.2 Note2			μs
			1.8 V ≤ V_{DD} < 2.7 V	$2/f_{sam}$ + 0.5 Note2			μs
TI50, TI51 input frequency	f_{TI5}	V_{DD} = 2.7 to 5.5 V		0		4	MHz
				0		275	kHz
TI50, TI51 input high-/low-level width	t_{TIH5} t_{TIL5}	V_{DD} = 2.7 to 5.5 V		100			ns
				1.8			μs
Interrupt request input high-/low-level width	t_{INTH} t_{INTL}	INTP0 to INTP3, P40 to P47	V_{DD} = 2.7 to 5.5 V	1			μs
				2			μs
$\overline{RESET}$ low-level width	t_{RSL}	V_{DD} = 2.7 to 5.5 V		10			μs
				20			μs

Notes 1. Value when using the external clock. When using a crystal resonator, the value becomes 114 μs (MIN.).

2. Selection of f_{sam} = f_X, f_X/4, f_X/64 is available with bits 0 and 1 (PRM0n0, PRM0n1) of prescaler mode register 0n (PRM0n). However, if the TI00n valid edge is selected as the count clock, the value becomes f_{sam} = f_X/8 (n = 0, 1).

T_{CY} vs V_{DD} (at main system clock operation)



(2) Read/write operation (T_A = –40 to + 85°C, V_{DD} = 4.0 to 5.5 V) (1/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.3t_{CY}$		ns
Address setup time	t_{ADS}		20		ns
Address hold time	t_{ADH}		6		ns
Data input time from address	t_{ADD1}			$(2 + 2n)t_{CY}$ – 54	ns
	t_{ADD2}			$(3 + 2n)t_{CY}$ – 60	ns
Address output time from $\overline{RD}\downarrow$	t_{RDAD}		0	100	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			$(2 + 2n)t_{CY}$ – 87	ns
	t_{RDD2}			$(3 + 2n)t_{CY}$ – 93	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5 + 2n)t_{CY}$ – 33		ns
	t_{RDL2}		$(2.5 + 2n)t_{CY}$ – 33		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t_{RDWT1}			t_{CY} – 43	ns
	t_{RDWT2}			t_{CY} – 43	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t_{WRWT}			t_{CY} – 25	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5 + 2n)t_{CY}$ + 10	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		6		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(1.5 + 2n)t_{CY}$ – 15		ns
$\overline{RD}\downarrow$ delay time from ASTB↓	t_{ASTRD}		6		ns
$\overline{WR}\downarrow$ delay time from ASTB↓	t_{ASTWR}		$2t_{CY}$ – 15		ns
ASTB↑ delay time from $\overline{RD}\uparrow$ in external fetch	t_{RDAST}		$0.8t_{CY}$ – 15	$1.2t_{CY}$	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t_{RDADH}		$0.8t_{CY}$ – 15	$1.2t_{CY}$ + 30	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		10	60	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		$0.8t_{CY}$ – 15	$1.2t_{CY}$ + 30	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTRD}		$0.8t_{CY}$	$2.5t_{CY}$ + 25	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTWR}		$0.8t_{CY}$	$2.5t_{CY}$ + 25	ns

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L is the load capacitance of AD0 to AD7, A8 to A15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins)

(2) Read/write operation (T_A = –40 to + 85°C, V_{DD} = 2.7 to 4.0 V) (2/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.3t_{CY}$		ns
Address setup time	t_{ADS}		30		ns
Address hold time	t_{ADH}		10		ns
Data input time from address	t_{ADD1}			$(2 + 2n)t_{CY}$ – 108	ns
	t_{ADD2}			$(3 + 2n)t_{CY}$ – 120	ns
Address output time from $\overline{RD}\downarrow$	t_{RDAD}		0	200	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			$(2 + 2n)t_{CY}$ – 148	ns
	t_{RDD2}			$(3 + 2n)t_{CY}$ – 162	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5 + 2n)t_{CY}$ – 40		ns
	t_{RDL2}		$(2.5 + 2n)t_{CY}$ – 40		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t_{RDWT1}			t_{CY} – 75	ns
	t_{RDWT2}			t_{CY} – 75	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t_{WRWT}			t_{CY} – 50	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5 + 2n)t_{CY}$ + 10	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		10		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(1.5 + 2n)t_{CY}$ – 30		ns
$\overline{RD}\downarrow$ delay time from ASTB$\downarrow$	t_{ASTRD}		10		ns
$\overline{WR}\downarrow$ delay time from ASTB$\downarrow$	t_{ASTWR}		$2t_{CY}$ – 30		ns
ASTB$\uparrow$ delay time from $\overline{RD}\uparrow$ in external fetch	t_{RDAST}		$0.8t_{CY}$ – 30	$1.2t_{CY}$	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t_{RDADH}		$0.8t_{CY}$ – 30	$1.2t_{CY}$ + 60	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		20	120	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		$0.8t_{CY}$ – 30	$1.2t_{CY}$ + 60	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTRD}		$0.5t_{CY}$	$2.5t_{CY}$ + 50	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTWR}		$0.5t_{CY}$	$2.5t_{CY}$ + 50	ns

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L is the load capacitance of AD0 to AD7, A8 to A15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins)

(2) Read/write operation (T_A = –40 to + 85°C, V_{DD} = 1.8 to 2.7 V) (3/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.3t_{CY}$		ns
Address setup time	t_{ADS}		120		ns
Address hold time	t_{ADH}		20		ns
Data input time from address	t_{ADD1}			$(2 + 2n)t_{CY}$ – 233	ns
	t_{ADD2}			$(3 + 2n)t_{CY}$ – 240	ns
Address output time from $\overline{RD}\downarrow$	t_{RDAD}		0	400	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			$(2 + 2n)t_{CY}$ – 325	ns
	t_{RDD2}			$(3 + 2n)t_{CY}$ – 332	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5 + 2n)t_{CY}$ – 92		ns
	t_{RDL2}		$(2.5 + 2n)t_{CY}$ – 92		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t_{RDWT1}			t_{CY} – 350	ns
	t_{RDWT2}			t_{CY} – 350	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t_{WRWT}			t_{CY} – 100	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5 + 2n)t_{CY}$ + 10	$(2 + 2n)t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(1.5 + 2n)t_{CY}$ – 60		ns
$\overline{RD}\downarrow$ delay time from ASTB↓	t_{ASTRD}		20		ns
$\overline{WR}\downarrow$ delay time from ASTB↓	t_{ASTWR}		$2t_{CY}$ – 60		ns
ASTB↑ delay time from $\overline{RD}\uparrow$ in external fetch	t_{RDAST}		$0.8t_{CY}$ – 60	$1.2t_{CY}$	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t_{RDADH}		$0.8t_{CY}$ – 60	$1.2t_{CY}$ + 120	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		40	240	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		$0.8t_{CY}$ – 60	$1.2t_{CY}$ + 120	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTRD}		$0.5t_{CY}$	$2.5t_{CY}$ + 100	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t_{WTWR}		$0.5t_{CY}$	$2.5t_{CY}$ + 100	ns

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L is the load capacitance of AD0 to AD7, A8 to A15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins)

(3) Serial interface (T_A = –40 to +85°C, V_{DD} = 1.8 to 5.5 V)

(a) SIO3 3-wire serial I/O mode ($\overline{SCK3}$ ... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY1}	4.0 V ≤ V_{DD} ≤ 5.5 V	954			ns
		2.7 V ≤ V_{DD} < 4.0 V	1600			ns
		1.8 V ≤ V_{DD} < 2.7 V	3200			ns
$\overline{SCK3}$ high-/low-level width	t_{KH1} t_{KL1}	V_{DD} = 4.0 to 5.5 V	t_{KCY1}/2 – 50			ns
			t_{KCY1}/2 – 100			ns
SI3 setup time (to $\overline{SCK3}$↑)	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.0 V	150			ns
		1.8 V ≤ V_{DD} < 2.7 V	300			ns
SI3 hold time (from $\overline{SCK3}$↑)	t_{KSI1}		400			ns
Delay time from $\overline{SCK3}$↓ to SO3 output	t_{KSO1}	C = 100 pF**Note**			300	ns

Note C is the load capacitance of the $\overline{SCK3}$ and SO3 output lines.

(b) SIO3 3-wire serial I/O mode ($\overline{SCK3}$ ... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3}$ cycle time	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V	800			ns
		2.7 V ≤ V_{DD} < 4.0 V	1600			ns
		1.8 V ≤ V_{DD} < 2.7 V	3200			ns
$\overline{SCK3}$ high-/low-level width	t_{KH2} t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V	400			ns
		2.7 V ≤ V_{DD} < 4.0 V	800			ns
		1.8 V ≤ V_{DD} < 2.7 V	1600			ns
SI3 setup time (to $\overline{SCK3}$↑)	t_{SIK2}		100			ns
SI3 hold time (from $\overline{SCK3}$↑)	t_{KSI2}		400			ns
Delay time from $\overline{SCK3}$↓ to SO3 output	t_{KSO2}	C = 100 pF**Note**			300	ns

Note C is the load capacitance of the SO3 output line.

(c) CSI1 3-wire serial I/O mode (SCK1 ... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCK1 cycle time	t_{KCY3}	4.0 V ≤ V_{DD} ≤ 5.5 V	240			ns
		2.7 V ≤ V_{DD} < 4.0 V	500			ns
		1.8 V ≤ V_{DD} < 2.7 V	1			μs
SCK1 high-/low-level width	t_{KH3} t_{KL3}	4.0 V ≤ V_{DD} ≤ 5.5 V	t_{KCY3}/2–5			ns
		2.7 V ≤ V_{DD} < 4.0 V	t_{KCY3}/2–20			ns
		1.8 V ≤ V_{DD} < 2.7 V	t_{KCY3}/2–30			ns
SI1 setup time (to SCK1↑)	t_{SIK3}		25			ns
SI1 hold time (to SCK1↑)	t_{KSI3}		110			ns
Delay time from SCK1↓ to SO1 output	t_{KSO3}	C = 100 pF[Note]			150	ns

Note C is the load capacitance of the SCK1 and SO1 output lines.

(d) CSI1 3-wire serial I/O mode (SCK1 ... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCK1 cycle time	t_{KCY4}	4.0 V ≤ V_{DD} ≤ 5.5 V	200			ns
		2.7 V ≤ V_{DD} < 4.0 V	500			ns
		1.8 V ≤ V_{DD} < 2.7 V	1			μs
SCK1 high-/low-level width	t_{KH4} t_{KL4}	4.0 V ≤ V_{DD} ≤ 5.5 V	100			ns
		2.7 V ≤ V_{DD} < 4.0 V	250			ns
		1.8 V ≤ V_{DD} < 2.7 V	500			ns
SI1 setup time (to SCK1↑)	t_{SIK4}		25			ns
SI1 hold time (to SCK1↑)	t_{KSI4}		110			ns
Delay time from SCK1↓ to SO1 output	t_{KSO4}	C = 100 pF[Note]			150	ns

Note C is the load capacitance of the SO1 output line.

(e) UART0 mode (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V			131031	bps
		2.7 V ≤ V_{DD} < 4.0 V			78125	bps
		1.8 V ≤ V_{DD} < 2.7 V			39063	bps

(f) UART0 mode (External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK0 cycle time	t_{KCY5}	$4.0\ V \le V_{DD} \le 5.5\ V$	800			ns
		$2.7\ V \le V_{DD} < 4.0\ V$	1600			ns
		$1.8\ V \le V_{DD} < 2.7\ V$	3200			ns
ASCK0 high-/low-level width	t_{KH5} t_{KL5}	$4.0\ V \le V_{DD} \le 5.5\ V$	400			ns
		$2.7\ V \le V_{DD} < 4.0\ V$	800			ns
		$1.8\ V \le V_{DD} < 2.7\ V$	1600			ns
Transfer rate		$4.0\ V \le V_{DD} \le 5.5\ V$			39063	bps
		$2.7\ V \le V_{DD} < 4.0\ V$			19531	bps
		$1.8\ V \le V_{DD} < 2.7\ V$			9766	bps

(g) UART0 mode (Infrared data transfer mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 4.0 to 5.5 V			131031	bps
Bit rate allowable error		V_{DD} = 4.0 to 5.5 V			±0.87	%
Output pulse width		V_{DD} = 4.0 to 5.5 V	1.2		0.24/fbr**Note**	μs
Input pulse width		V_{DD} = 4.0 to 5.5 V	4/f_X			μs

Note fbr: Specified baud rate

(h) UART2 (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		$4.0\ V \le V_{DD} \le 5.5\ V$			262062	bps
		$2.7\ V \le V_{DD} < 4.0\ V$			156250	bps
		$1.8\ V \le V_{DD} < 2.7\ V$			62500	bps

(i) UART2 (External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK2 cycle time	t_{KCY6}	$4.0\ V \le V_{DD} \le 5.5\ V$	800			ns
		$2.7\ V \le V_{DD} < 4.0\ V$	1600			ns
		$1.8\ V \le V_{DD} < 2.7\ V$	3200			ns
ASCK2 high-/low-level width	t_{KH6} t_{KL6}	$4.0\ V \le V_{DD} \le 5.5\ V$	400			ns
		$2.7\ V \le V_{DD} < 4.0\ V$	800			ns
		$1.8\ V \le V_{DD} < 2.7\ V$	1600			ns
Transfer rate		$4.0\ V \le V_{DD} \le 5.5\ V$			78125	bps
		$2.7\ V \le V_{DD} < 4.0\ V$			39063	bps
		$1.8\ V \le V_{DD} < 2.7\ V$			19531	bps

(j) UART2 (Infrared data transfer mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.0 V ≤ V_{DD} ≤ 5.5 V			262062	bps
Bit rate allowable error		4.0 V ≤ V_{DD} ≤ 5.5 V			±0.87	%
Output pulse width		4.0 V ≤ V_{DD} ≤ 5.5 V	1.2		0.24/fbr[Note]	μs
Input pulse width		4.0 V ≤ V_{DD} ≤ 5.5 V	4/f_X			μs

Note fbr: Specified baud rate

(k) I^2C bus mode

Parameter		Symbol	Standard Mode		High-speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f_{SCL}	0	100	0	400	kHz
Bus free time (between stop and start condition)		t_{BUF}	4.7	—	1.3	—	μs
Hold time[Note 1]		$t_{HD:STA}$	4.0	—	0.6	—	μs
SCL0 clock low-level width		t_{LOW}	4.7	—	1.3	—	μs
SCL0 clock high-level width		t_{HIGH}	4.0	—	0.6	—	μs
Start/restart condition setup time		$t_{SU:STA}$	4.7	—	0.6	—	μs
Data hold time	CBUS compatible master	$t_{HD:DAT}$	5.0	—	—	—	μs
	I^2C bus		0[Note 2]	—	0[Note 2]	0.9[Note 3]	μs
Data setup time		$t_{SU:DAT}$	250	—	100[Note 4]	—	ns
SDA0 and SCL0 signal rise time		t_R	—	1000	20 + 0.1Cb[Note 5]	300	ns
SDA0 and SCL0 signal fall time		t_F	—	300	20 + 0.1Cb[Note 5]	300	ns
Stop condition setup time		$t_{SU:STO}$	4.0	—	0.6	—	μs
Capacitive load per each bus line		Cb	—	400	—	400	pF
Spike pulse width controlled by input filter		t_{SP}	—	—	0	50	ns

Notes 1. On start condition, the first clock pulse is generated after hold period.

2. To fulfill undefined area of the SCL0 falling edge, it is necessary for the device to provide internally SDA0 signal (on $V_{IHmin.}$ of SCL0 signal) with at least 300 ns of hold time.

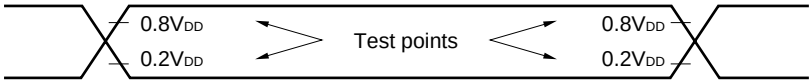
3. If the device does not extend the SCL0 signal low hold time (t_{LOW}), only maximum data hold time $t_{HD:DAT}$ needs to be fulfilled.

4. The high-speed mode I^2C bus is available in the standard mode I^2C bus system. At this time, the conditions described below must be satisfied.

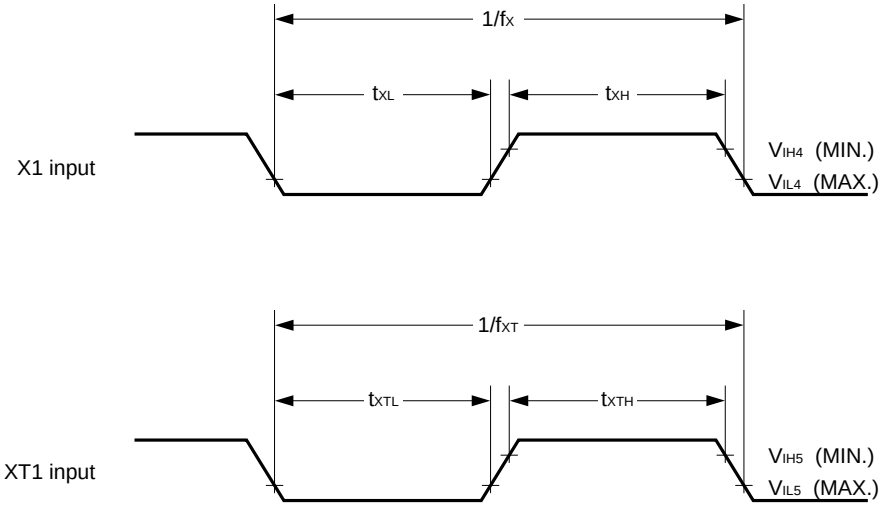
- If the device does not extend the SCL0 signal low state hold time
  $t_{SU:DAT} \geq 250$ ns
- If the device extends the SCL0 signal low state hold time
  Be sure to transmit the next data bit to the SDA0 line before the SCL0 line is released ($t_{Rmax.} + t_{SU:DAT}$ = 1000 + 250 = 1250 ns by standard mode I^2C bus specification).

5. Cb : total capacitance per one bus line (unit : pF)

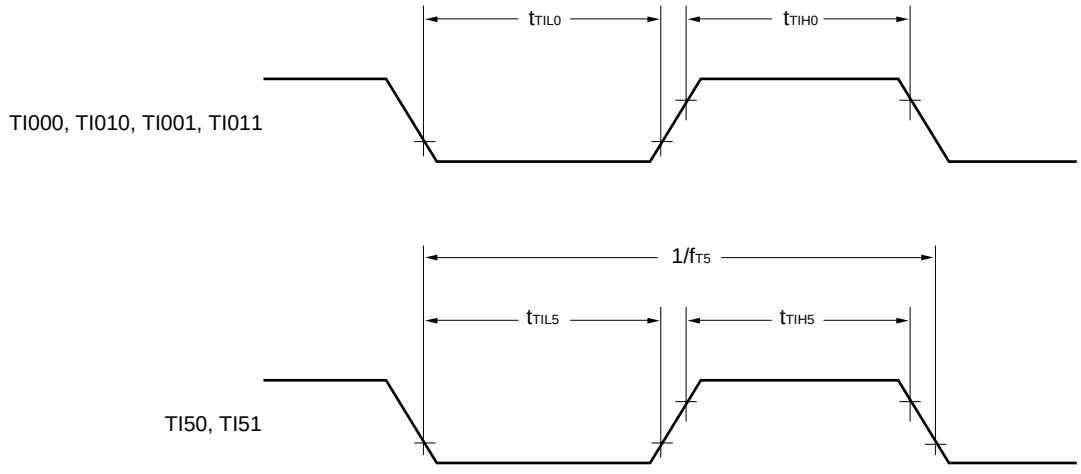
AC Timing Test Points (excluding X1, XT1 Inputs)



Clock Timing

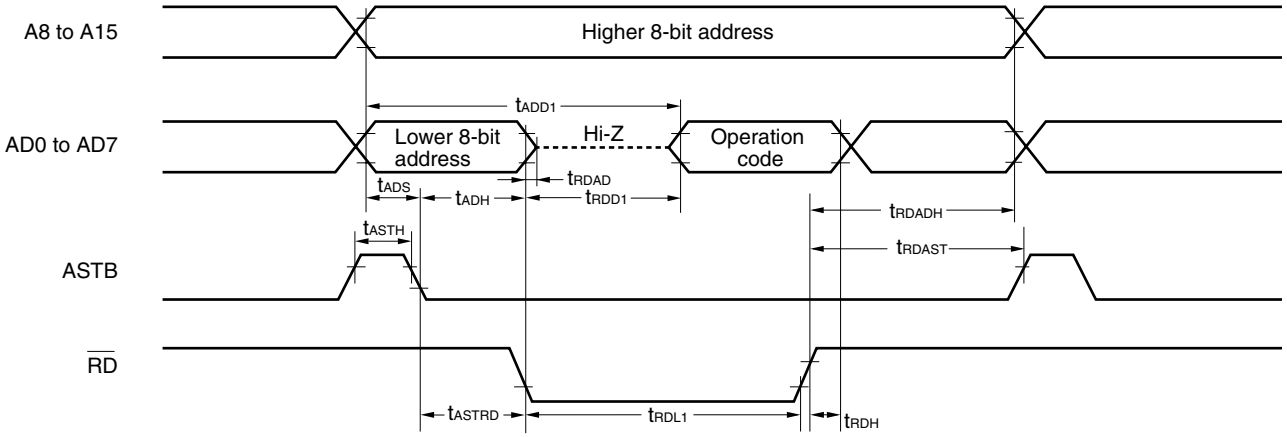


TI Timing

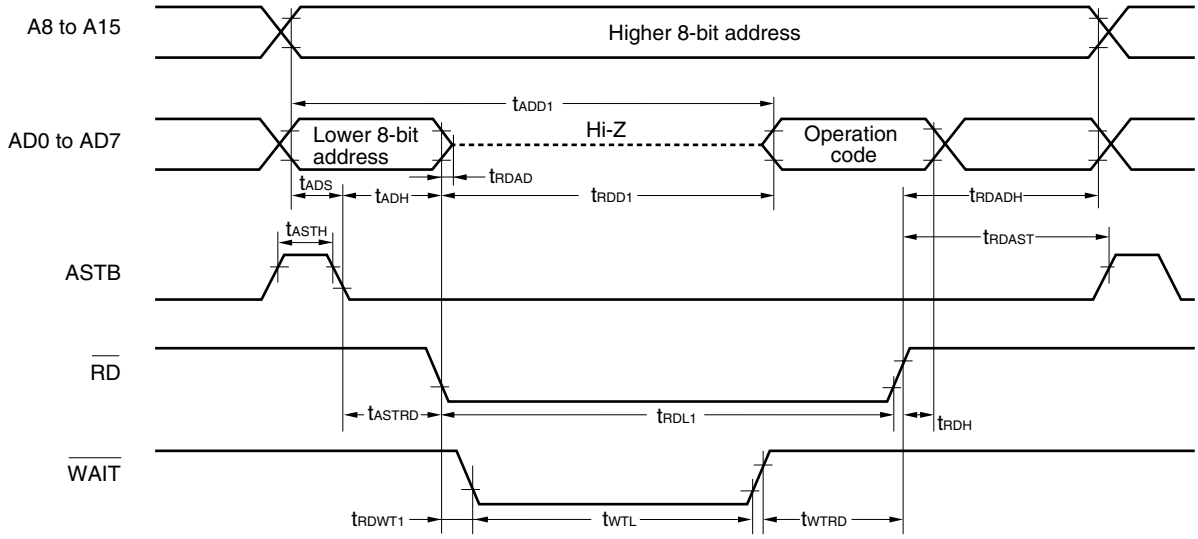


Read/Write Operation

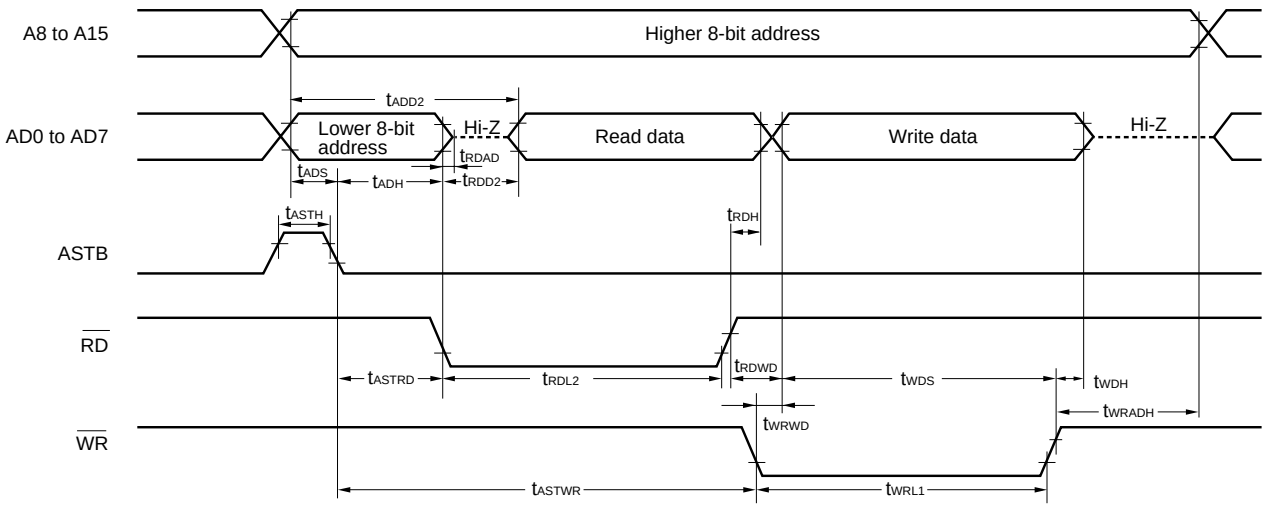
External fetch (no wait):



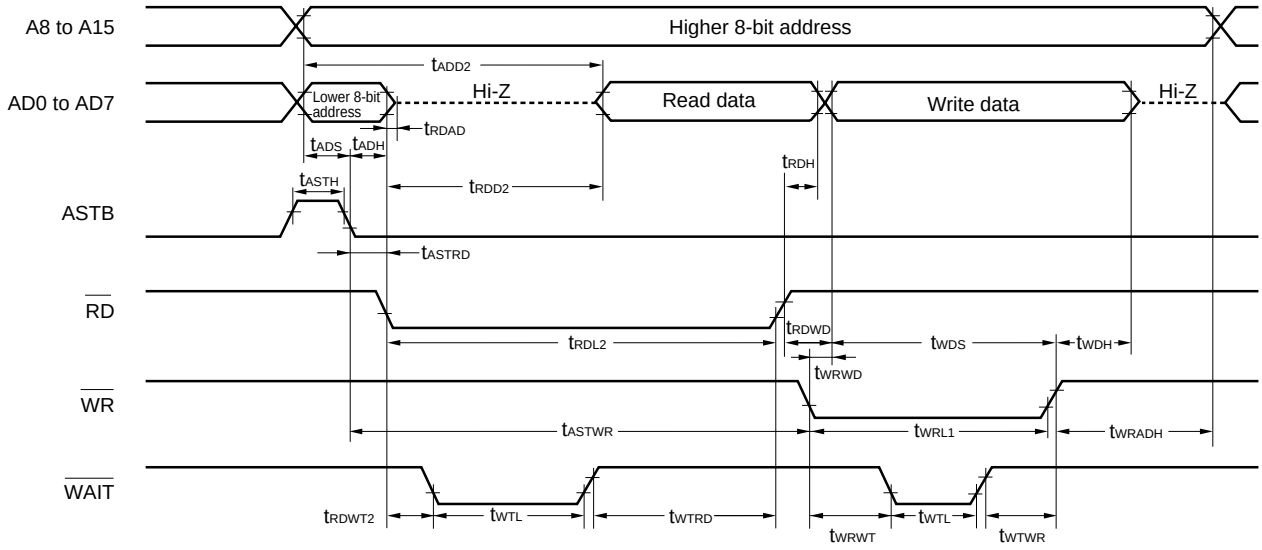
External fetch (wait insertion):



External data access (no wait):

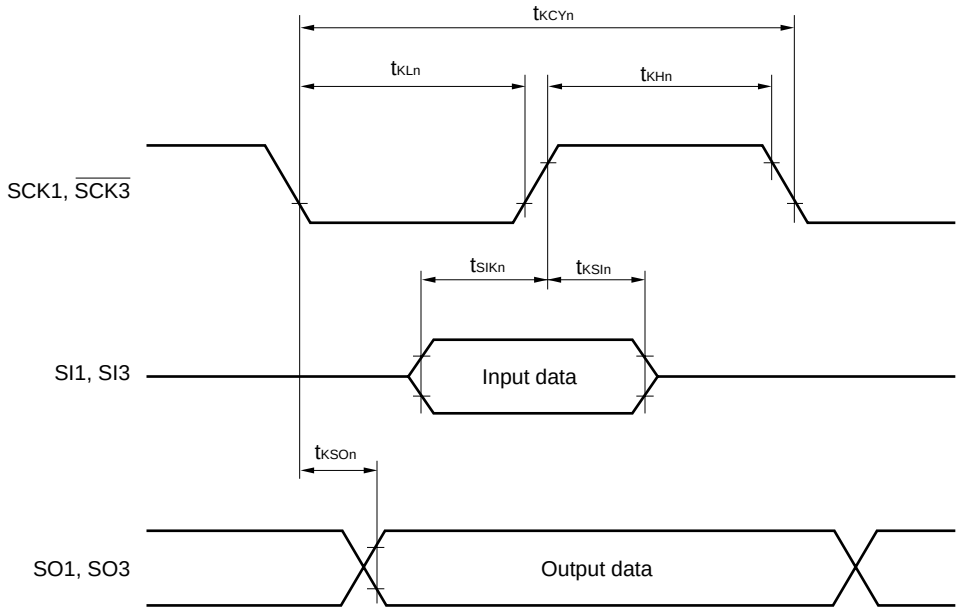


External data access (wait insertion):



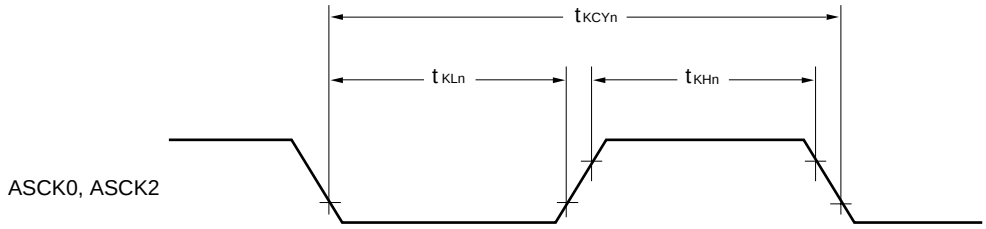
Serial Transfer Timing

3-wire serial I/O mode:



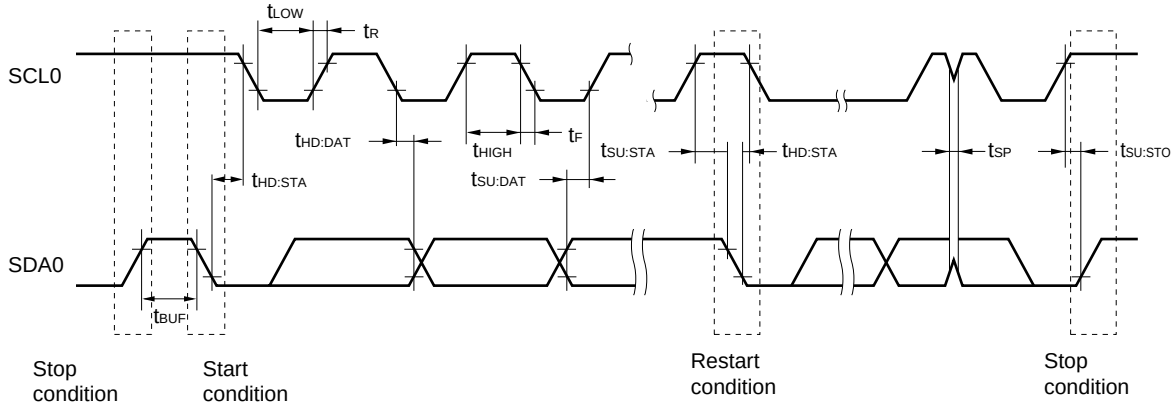
n = 1 to 4

UART mode (external clock input):



n = 5, 6

I²C bus mode:



A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{REF} = 2.2 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note]		4.0 V ≤ AV_{REF} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V		±0.3	±0.6	%FSR
		2.2 V ≤ AV_{REF} < 2.7 V		±0.6	±1.2	%FSR
Conversion time	t_{CONV}	4.0 V ≤ AV_{REF} ≤ 5.5 V	14		100	μs
		2.7 V ≤ AV_{REF} < 4.0 V	19		100	μs
		2.2 V ≤ AV_{REF} < 2.7 V	28		100	μs
Zero-scale error[Note]		4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		2.2 V ≤ AV_{REF} < 2.7 V			±1.2	%FSR
Full-scale error[Note]		4.0 V ≤ AV_{REF} ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV_{REF} < 4.0 V			±0.6	%FSR
		2.2 V ≤ AV_{REF} < 2.7 V			±1.2	%FSR
Integral linear error		4.0 V ≤ AV_{REF} ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±4.5	LSB
		2.2 V ≤ AV_{REF} < 2.7 V			±8.5	LSB
Differential linear error		4.0 V ≤ AV_{REF} ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV_{REF} < 4.0 V			±2.0	LSB
		2.2 V ≤ AV_{REF} < 2.7 V			±3.5	LSB
Analog input impedance		During sampling			100	kΩ
		Other than during sampling		10		MΩ
Analog input voltage	V_{IAN}		0		AV_{REF}	V
AV_{REF} resistance	R_{AIREF}	During A/D conversion	20	40		kΩ

Note Overall error excluding quantization error (±1/2 LSB). It is indicated as a ratio to the full-scale value.

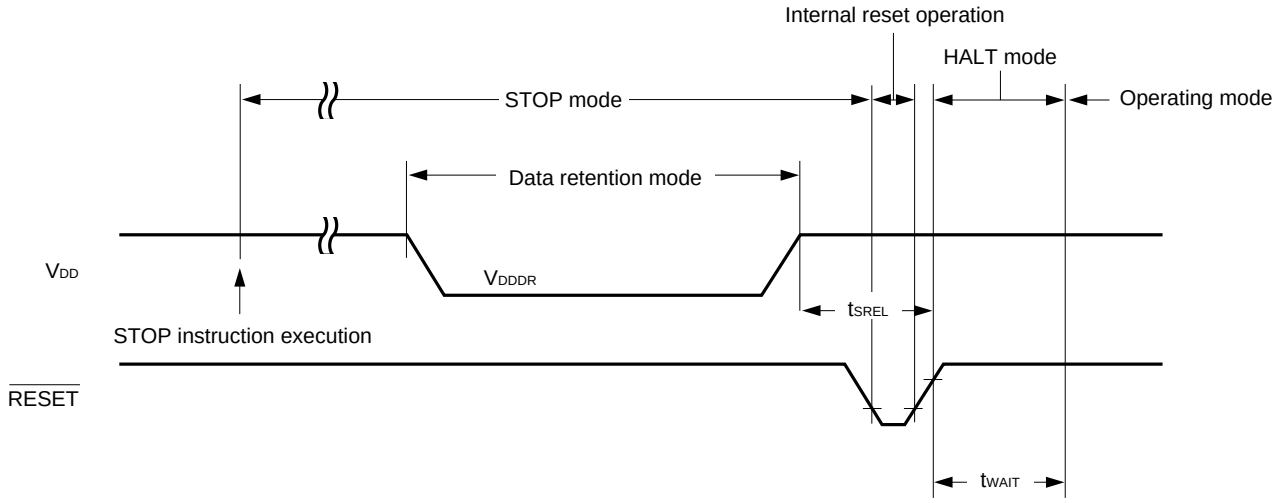
Remark FSR: Full-scale range

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

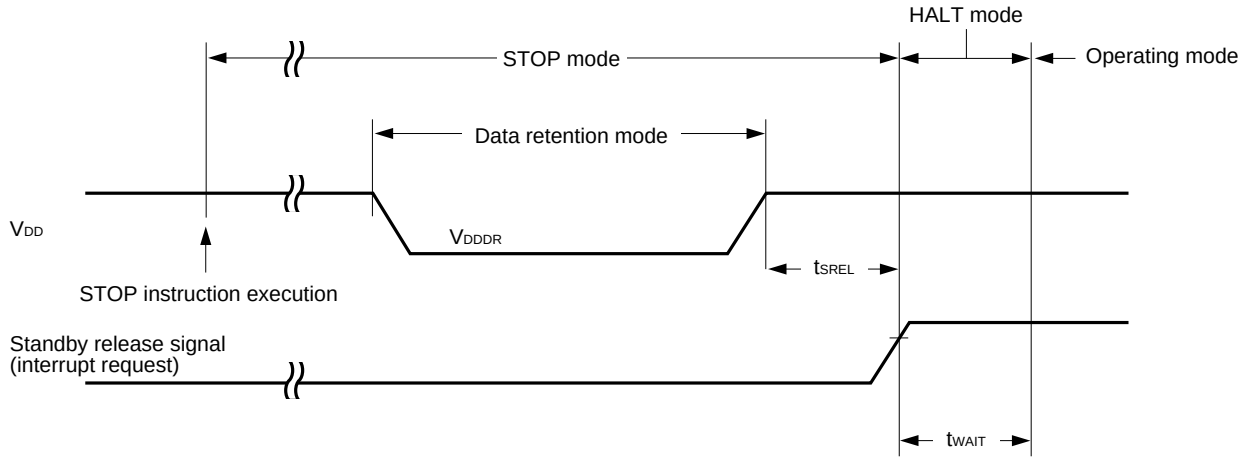
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.6		5.5	V
Data retention power supply current	I_{DDDR}	Subsystem clock is not used (XT1 = V_{DD}) and feed-back resistor disconnected		0.1	30	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		2^{17}/fx		ms
		Release by interrupt request		**Note**		ms

Note Selection of 2^{12}/fx and 2^{14}/fx to 2^{17}/fx is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

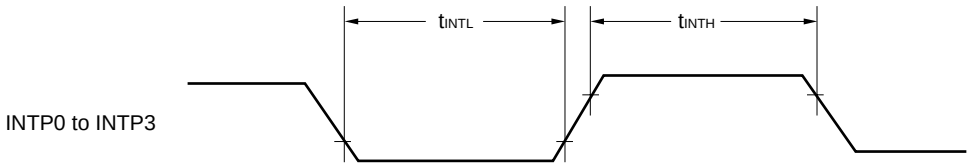
Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)



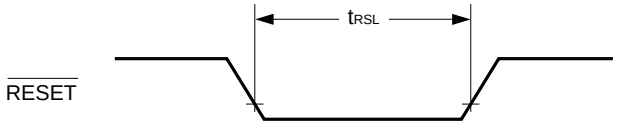
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)



Interrupt Request Input Timing

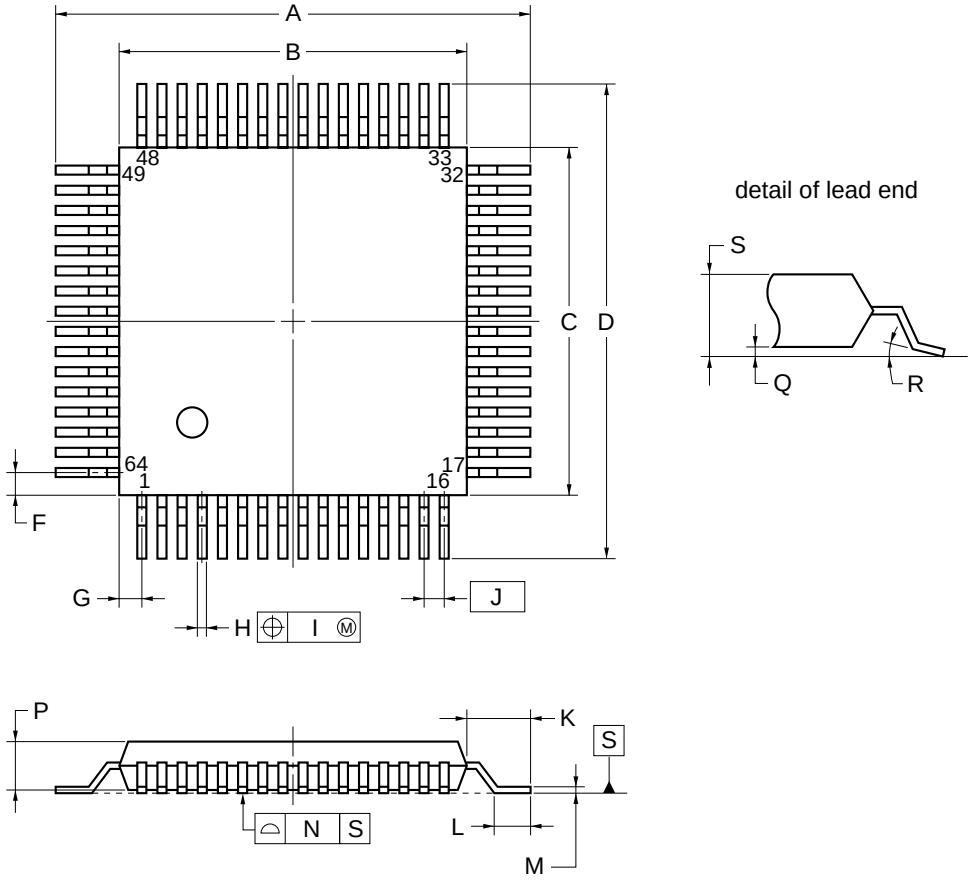


$\overline{\text{RESET}}$ Input Timing



13. PACKAGE DRAWINGS

64-PIN PLASTIC QFP (14x14)



NOTE

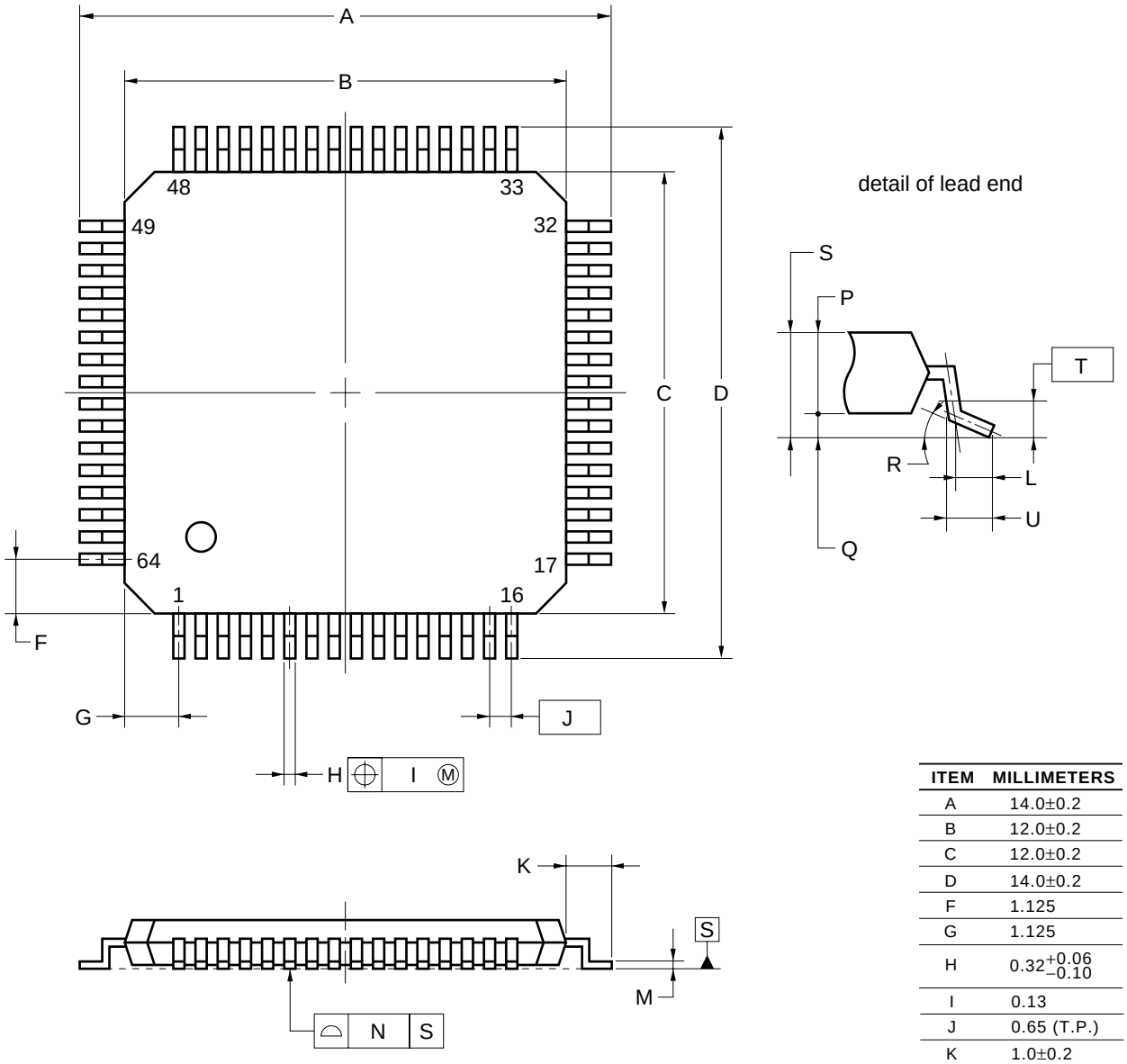
Each lead centerline is located within 0.15 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.6±0.4
B	14.0±0.2
C	14.0±0.2
D	17.6±0.4
F	1.0
G	1.0
H	$0.37^{+0.08}_{-0.07}$
I	0.15
J	0.8 (T.P.)
K	1.8±0.2
L	0.8±0.2
M	$0.17^{+0.08}_{-0.07}$
N	0.10
P	2.55±0.1
Q	0.1±0.1
R	5°±5°
S	2.85 MAX.

P64GC-80-AB8-5

Remark The external dimensions and material of the ES version are the same as those of the mass-produced version.

64-PIN PLASTIC TQFP (12x12)



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	14.0±0.2
B	12.0±0.2
C	12.0±0.2
D	14.0±0.2
F	1.125
G	1.125
H	$0.32^{+0.06}_{-0.10}$
I	0.13
J	0.65 (T.P.)
K	1.0±0.2
L	0.5
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	1.0
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.1±0.1
T	0.25
U	0.6±0.15

P64GK-65-9ET-3

Remark The external dimensions and material of the ES version are the same as those of the mass-produced version.

★ 14. RECOMMENDED SOLDERING CONDITIONS

The μPD780078, 780078Y Subseries should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 14-1. Surface Mounting Type Soldering Conditions

(1) μPD780076GC-×××-AB8: 64-pin plastic QFP (14 × 14)
μPD780078GC-×××-AB8: 64-pin plastic QFP (14 × 14)
μPD780076YGC-×××-AB8: 64-pin plastic QFP (14 × 14)
μPD780078YGC-×××-AB8: 64-pin plastic QFP (14 × 14)

Soldering	Soldering Conditions	Recommended Method Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. max. (at 210°C or higher), Count: two times or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 sec. max. (at 200°C or higher), Count: two times or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 sec. max., Count: once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 sec. max. (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating).

(2) μPD780076GK-×××-9ET: 64-pin plastic TQFP (12 × 12)
μPD780078GK-×××-9ET: 64-pin plastic TQFP (12 × 12)
μPD780076YGK-×××-9ET: 64-pin plastic TQFP (12 × 12)
μPD780078YGK-×××-9ET: 64-pin plastic TQFP (12 × 12)

Soldering	Soldering Conditions	Recommended Method Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 sec. max. (at 210°C or higher), Count: two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 sec. max. (at 200°C or higher), Count: two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	VP15-107-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 sec. max., Count: once, Preheating temperature: 120°C max. (package surface temperature), Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	WS60-107-1
Partial heating	Pin temperature: 300°C max., Time: 3 sec. max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD780078, 780078Y Subseries. Also refer to **(6) Cautions on using development tools.**

★ **(1) Software package**

SP78K0	Software package common to 78K/0 Series

(2) Language processing software

RA78K0	Assembler package common to 78K/0 Series
CC78K0	C compiler package common to 78K/0 Series
DF780078	Device file for μPD780078, 780078Y Subseries
CC78K0-L	C compiler library source file common to 78K/0 Series

(3) Flash memory writing tools

Flashpro III (FL-PR3, PG-FP3)	Flash programmer dedicated to on-chip flash memory microcontroller
★ FA-64GC FA-64GK-9ET	Adapter for flash memory writing • FA-64GC: For 64-pin plastic QFP (GC-AB8 type) • FA-64GK-9ET: For 64-pin plastic TQFP (GK-9ET type)

(4) Debugging tool

• When using in-circuit emulator IE-78K0-NS(–A)

IE-78K0-NS(–A)	In-circuit emulator common to 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-78K0-NS-PA	Performance board to enhance/expand functions of IE-78K0-NS
IE-70000-98-IF-C	Adapter when using PC-9800 series as host machine (excluding notebook PCs) (C bus compatible)
IE-70000-CD-IF-A	PC card and interface cable when using notebook PC as host machine (PCMCIA socket compatible)
IE-70000-PC-IF-C	Adapter when using IBM PC/AT™ compatible as host machine (ISA bus compatible)
★ IE-70000-PCI-IF-A	Adapter necessary when using on-chip PCI bus PC as host machine
★ IE-780078-NS-EM1	Emulation board to emulate μPD780078, 780078Y Subseries
NP-64GC NP-64GC-TQ	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
NP-64GK	Emulation probe for 64-pin plastic TQFP (GK-9ET type)
EV-9200GC-64	Conversion socket for connecting target system designed to mount a 64-pin plastic QFP (GC-AB8 type) and NP-64GC
TGC-064SAP	Conversion adapter for connecting target system designed to mount a 64-pin plastic QFP (GC-AB8 type) and NP-64GC-TQ
★ TGK-064SBP	Conversion adapter for connecting target system board designed to mount a 64-pin plastic TQFP (GK-9ET type) and NP-64GK
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
DF780078	Device file common to μPD780078, 780078Y Subseries

• **When using in-circuit emulator IE-78001-R-A**

IE-78001-R-A	In-circuit emulator common to 78K/0 Series
IE-70000-98-IF-C	Interface adapter when using PC-9800 series as host machine (excluding notebook PCs) (C bus compatible)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT compatible as host machine (ISA bus compatible)
★ IE-70000-PCI-IF-A	Adapter necessary when using on-chip PCI bus PC as host machine
IE-78000-R-SV3	Interface adapter and cable when using EWS as host machine
★ IE-780078-NS-EM1	Emulation board to emulate μPD780078, 780078Y Subseries
IE-78K0-R-EX1	Emulation probe conversion board necessary to use IE-780078-NS-EM1 on IE-78001-R-A
EP-78240GC-R	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
EP-78012GK-R	Emulation probe for 64-pin plastic TQFP (GK-9ET type)
EV-9200GC-64	Socket to be mounted on target system board manufactured for 64-pin plastic QFP (GC-AB8 type)
★ TGK-064SBP	Conversion adapter for connecting target system board designed to mount a 64-pin plastic TQFP (GK-9ET) and EP-78012GK-R.
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
DF780078	Device file common to μPD780078, 780078Y Subseries

(5) Real-time OS

RX78K0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series

★ **(6) Cautions on using development tools**

- The ID78K0-NS, ID78K0, and SM78K0 are used in combination with the DF780078.
- The CC78K0 and RX78K0 are used in combination with the RA78K0 and the DF780078.
- The FL-PR3, FA-64GC, FA64GK, NP-64GC, NP-64GC-TQ, and NP-64GK-9ET are products made by Naito Densei Machida Mfg. Co., Ltd. (+81-44-822-3813).
- The TGC-064SAP and TGK-064SBP are products made by Tokyo Eletech Corp.
  Refer to: Daimaru Kogyo, Ltd.
  Electronics Dept. (TEL: Tokyo +81-3-3820-7112)
  Electronics 2nd Dept. (TEL: Osaka +81-6-6244-6672)
- For third party development tools, see the **Single-Chip Microcontroller Development Tools Selection Guide (U11069E)**.
- The host machines and OSs supporting each software are as follows.

Host Machine / [OS] / Software	PC	EWS
	PC-9800 series [Japanese Windows™] IBM PC/AT compatible [Japanese/English Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™]
RA78K0	√ Note	√
CC78K0	√ Note	√
ID78K0-NS	√	—
ID78K0	√	—
SM78K0	√	—
RX78K0	√ Note	√
MX78K0	√ Note	√

Note DOS-based software

APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD780078, 780078Y Subseries User's Manual	U14260E
μPD780076, 780078, 780076Y, 780078Y Data Sheet	This document
μPD78F0078, 78F0078Y Data Sheet	U14258E
78K/0 Series User's Manual — Instructions	U12326E

★ **Documents Related to Development Tools (User's Manuals)**

Document Name		Document No.
RA78K0 Assembler Package	Operation	U14445E
	Language	U14446E
	Structured Assembly Language	U11789E
CC78K0 C Compiler	Operation	U14297E
	Language	U14298E
IE-78K0-NS In-Circuit Emulator		U13731E
IE-78001-R-A In-Circuit Emulator		U14142E
IE-78K0-R-EX1 In-Circuit Emulator		To be prepared
IE-780078-NS-EM1 Emulation Board		To be prepared
EP-78012GK-R Emulation Probe		EEU-1538
EP-78240 Emulation Probe		U10332E
SM78K0S, SM78K0 System Simulator Ver. 2.10 or Later Windows Based	Operation	U14611E
SM78K Series System Simulator Ver. 2.10 or Later	External Part User Open Interface Specifications	U15006E
ID78K0-NS Integrated Debugger Ver. 2.00 or Later Windows Based	Operation	U14379E
ID78K0 Integrated Debugger Ver. 2.00 or Later EWS Based	Reference	U11151E
ID78K0 Integrated Debugger Ver. 2.00 or Later Windows Based	Reference	U11539E
	Guide	U11649E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No.
78K/0 Series Real-time OS	Fundamentals	U11537E
	Installation	U11536E
78K/0 Series OS MX78K0	Fundamental	U12257E

Other Documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE - Programs & Packages - (CD-ROM)	X13769E
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Purchase of NEC I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

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- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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Santa Clara, California
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800-366-9782
Fax: 408-588-6130
800-729-9288

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Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

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Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

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