DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD78001B, 78002B

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78001B/78002B are products in the μPD78002 subseries within the 78K/0 series.

The μPD78001B/78002B have various peripheral hardware such as timer, serial interface and interrupt function.

A one-time PROM or EPROM product, the μPD78P014, capable of operating in the same power supply voltage range as that of the mask ROM product and other development tools is provided.

Functions are described in detail in the following User's Manual, which should be read when carring out design work.

μPD78002, 78002Y Series User's Manual: IEU-1334
78K/0 Series User's Manual -Instruction: IEU-1372

FEATURES

- Large on-chip ROM & RAM

Item / Product Name	Program Memory (ROM)	Data Memory (Internal High-Speed RAM)	Package
μPD78001B	8K bytes	256 bytes	• 64-pin plastic shrink DIP (750 mil)
μPD78002B	16K byte	384 bytes	• 64-pin plastic QFP (14 × 14 mm)

- External memory expansion space: 64K bytes
- Instruction execution time can be varied from high-speed (0.4 μs) to ultra-low-speed (122 μs)
- I/O ports: 53 (N-ch open-drain : 4)
- Serial interface : 1 channel
- Timer: 4 channels
- Supply voltage: V_{DD} = 2.7 to 6.0 V

APPLICATION

Cellular phone, VCR, audio, camera, home appliances, etc.

The information in this document is subject to change without notice.

The mark ★ shows major revised points.

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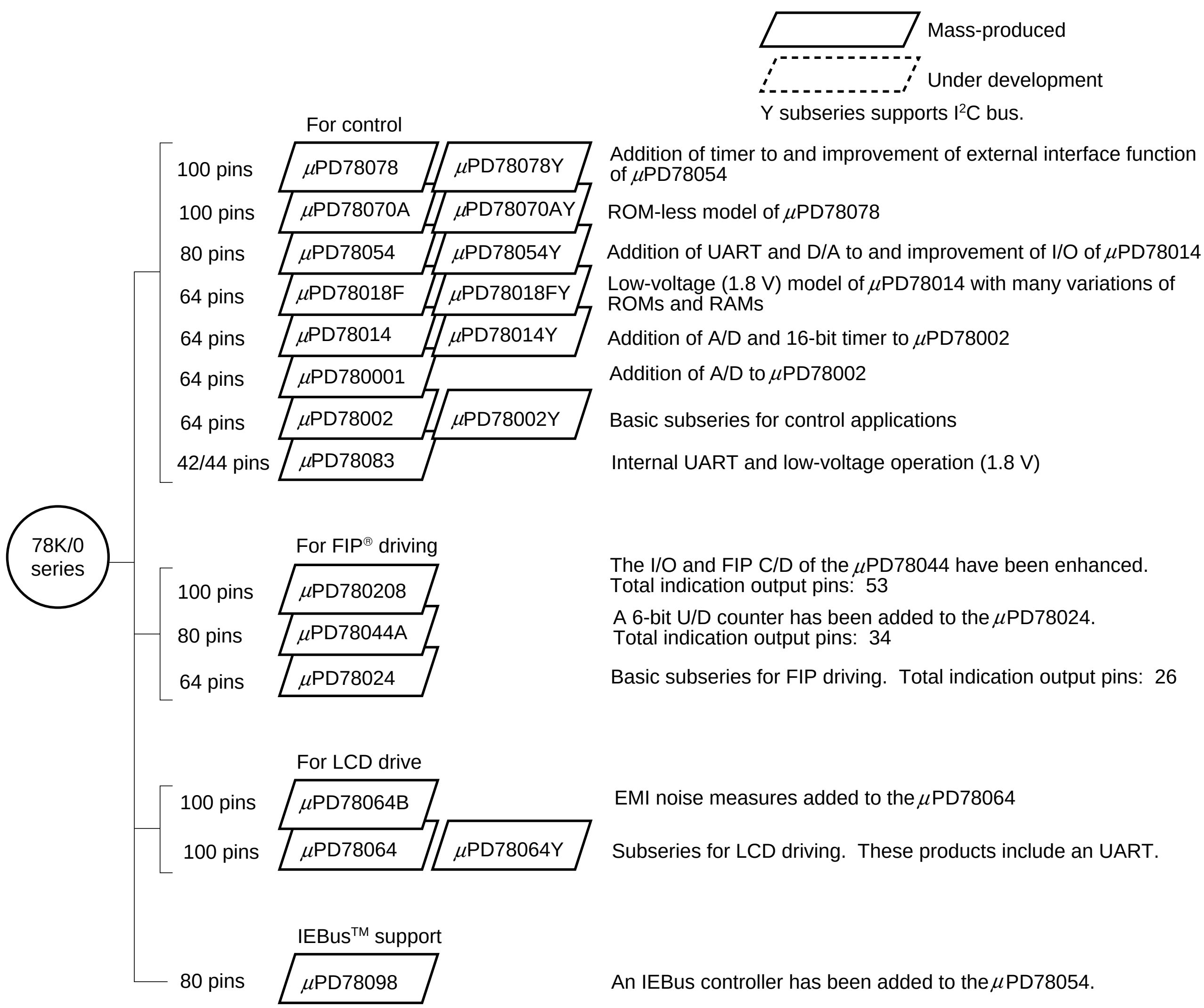
(Previous No. IC-3067)
Date Published December 1995 P
Printed in Japan

Ordering Information

Part Number	Package
μPD78001BCW-×××	64-pin plastic shrink DIP (750 mil)
μPD78001BGC-×××-AB8	64-pin plastic QFP (14 × 14 mm)
μPD78002BCW-×××	64-pin plastic shrink DIP (750 mil)
μPD78002BGC-×××-AB8	64-pin plastic QFP (14 × 14 mm)

Remark ××× indicates ROM code No.

★ DEVELOPMENT OF 78K/0 SERIES PRODUCT



The table below shows the main differences between subseries.

Subseries	Functions	ROM Capacity	Timer 8-bit	Timer 16-bit	Timer Watch	Timer WDT	8-bit A/D	8-bit A/D	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
For control	μPD78078	32 K-60 K	4ch	1ch	1ch	1ch	8ch	2ch	3ch (UART: 1ch)	88	1.8 V	○
	μPD78070A	—								61	2.7 V	
	μPD78054	16 K-60 K	2ch							69	2.0 V	
	μPD78018F	8 K-60 K						—	2 ch	53	1.8 V	
	μPD78014	8 K-32 K									2.7 V	
	μPD780001	8 K		—	—				1 ch	39		—
	μPD78002	8 K-16 K			1ch		—			53		○
	μPD78083				—		8ch		1ch (UART: 1ch)	33	1.8 V	—
For FIP drive	μPD780208	32 K-60 K	2ch	1ch	1ch	1ch	8ch	—	2ch	74	2.7 V	—
	μPD78044A	16 K-40 K								68		
	μPD78024	24 K-32 K								54		
For LCD drive	μPD78064B	32 K	2ch	1ch	1ch	1ch	8ch	—	2ch (UART: 1ch)	57	2.0 V	—
	μPD78064	16 K-32 K										
IEBus support	μPD78098	32 K-60 K	2ch	1ch	1ch	1ch	8ch	2ch	3ch (UART: 1ch)	69	2.7 V	○

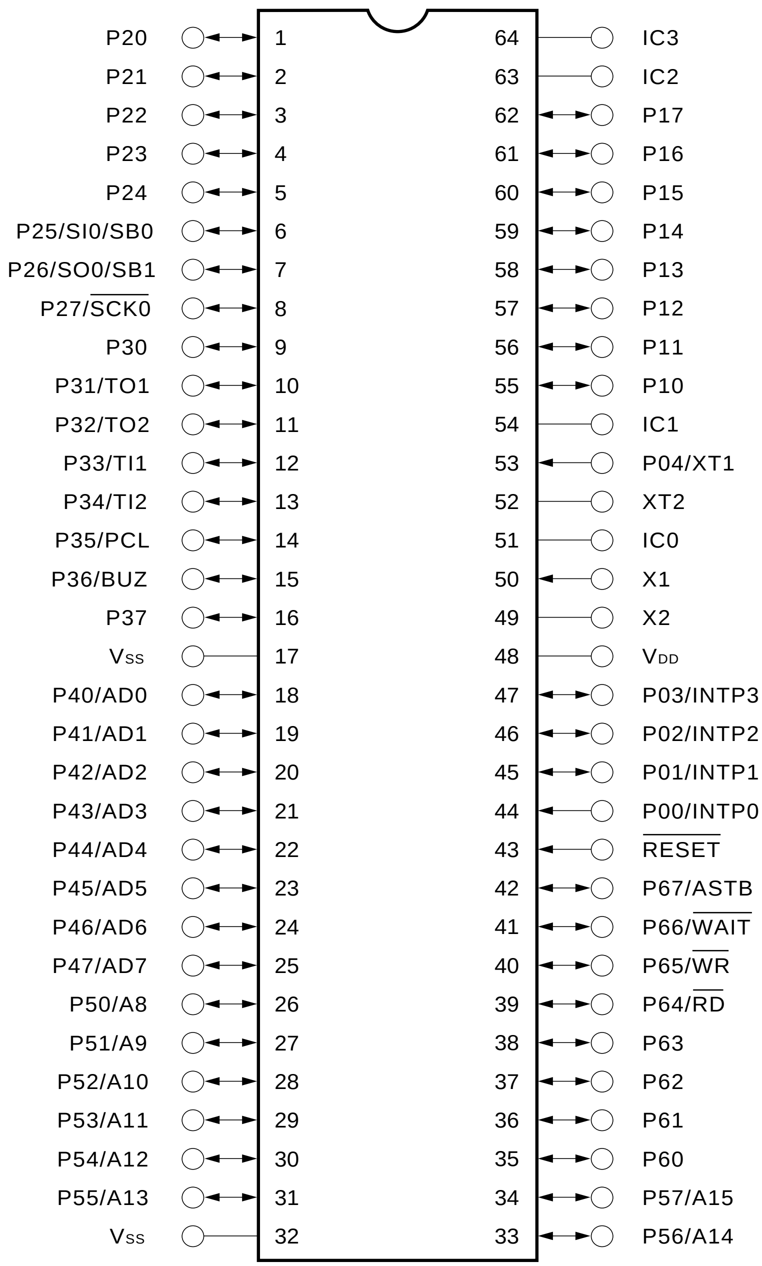
OVERVIEW OF FUNCTION

Item \ Product Name		μPD78001B	μPD78002B
Internal memory	ROM	8K bytes	16K bytes
	Internal high-speed RAM	256 bytes	384 bytes
Memory space		64K bytes	
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Instruction cycle		On-chip instruction execution time cycle modification function	
	When main system clock selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (at 10.0 MHz operation)	
	When subsystem clock selected	122 μs (at 32.768 kHz operation)	
Instruction set		• 16-bit operation • Bit manipulation (set, reset, test, boolean operation) • BCD correction, etc.	
I/O ports		Total : 53 • CMOS input : 2 • CMOS I/O : 47 • N-channel open-drain I/O (15 V withstand voltage) : 4	
Serial interface		• 3-wire/SBI/2-wire mode selectable	
Timer		• 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel	
Timer output		2	
Clock output		39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz (at main system clock: 10.0 MHz operation), 32.768 kHz (at subsystem clock: 32.768 kHz operation)	
Buzzer output		2.4 kHz, 4.9 kHz, 9.8 kHz (at main system clock: 10.0 MHz operation)	
Vectored interrupts	Maskable interrupts	Internal : 5 External : 4	
	Non-maskable interrupt	Internal : 1	
	Software interrupt	Internal : 1	
Test input		Internal : 1 External : 1	
Supply voltage		V_{DD} = 2.7 to 6.0 V	
Operating ambient temperature		T_A = –40 to +85°C	
Package		• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 14 mm)	

CONTENTS

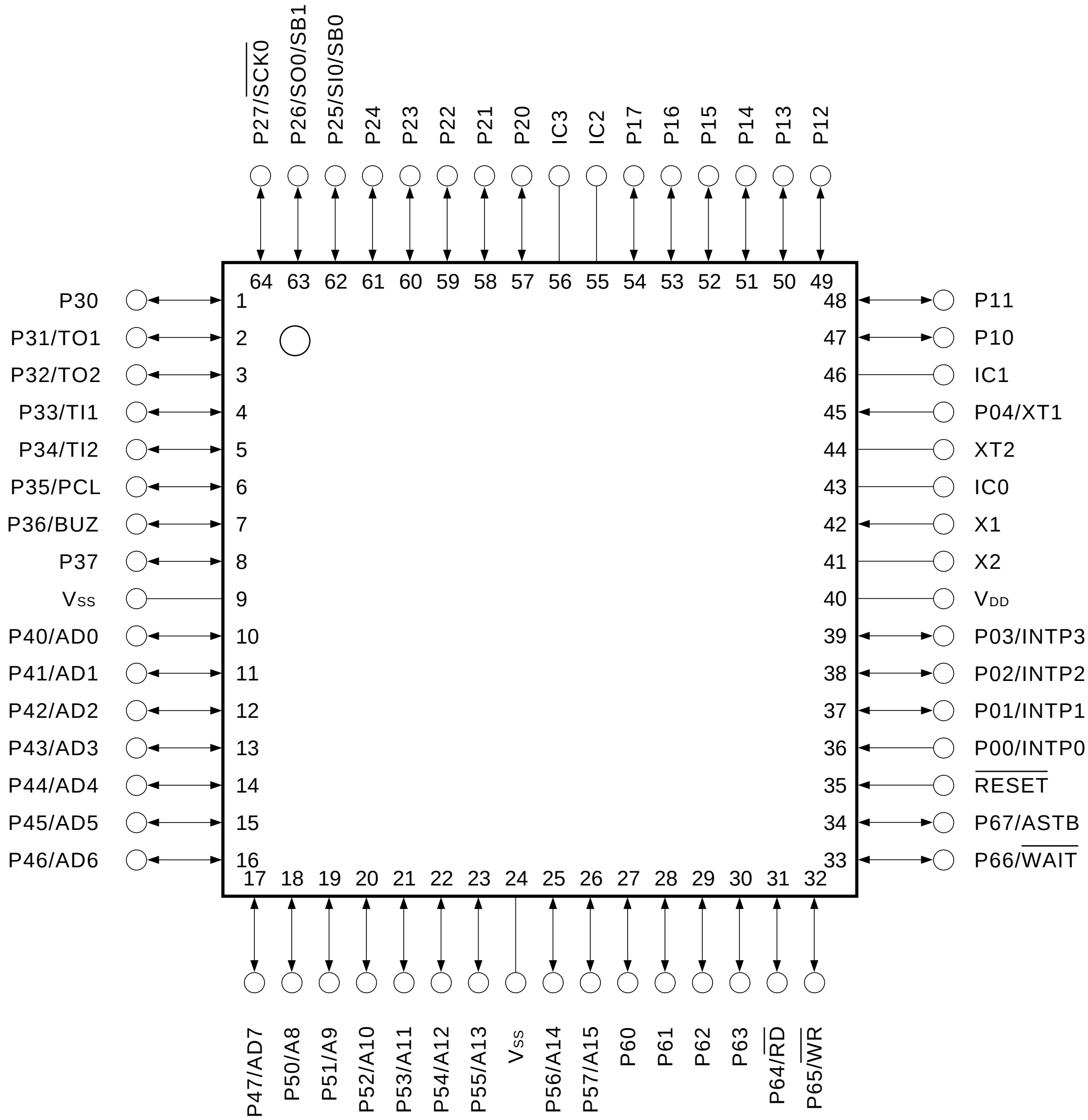
1. PIN CONFIGURATION (TOP VIEW)

- **64-Pin Plastic Shrink DIP (750 mil)**
  μ**PD78001BCW-**×××
  μ**PD78002BCW-**×××



Remark Always connect the IC0, IC1 and IC3 (Internally Connected) pins to V_{SS} directly.
Always connect the IC2 pin to V_{DD} directly.

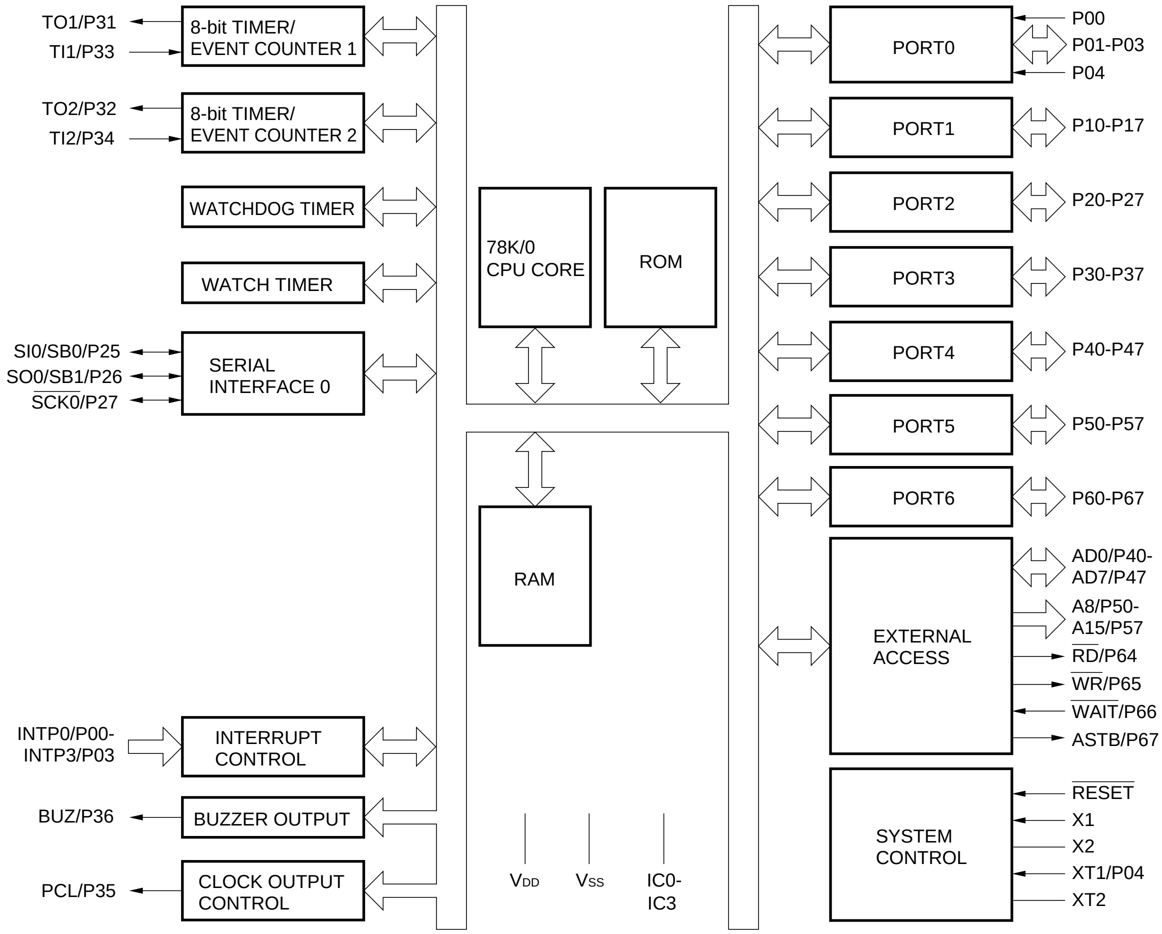
- **64-Pin Plastic QFP (14 × 14 mm)**
  μPD78001BGC-×××-AB8
  μPD78002BGC-×××-AB8



Remark Always connect the IC0, IC1 and IC3 (Internally Connected) pins to V_{SS} directly.
Always connect the IC2 pin to V_{DD} directly.

P00 to P04	:	Port 0	PCL	:	Programmable Clock
P10 to P17	:	Port 1	BUZ	:	Buzzer Clock
P20 to P27	:	Port 2	AD0 to AD7	:	Address/Data Bus
P30 to P37	:	Port 3	A8 to A15	:	Address Bus
P40 to P47	:	Port 4	$\overline{\text{RD}}$	:	Read Strobe
P50 to P57	:	Port 5	$\overline{\text{WR}}$	:	Write Strobe
P60 to P67	:	Port 6	$\overline{\text{WAIT}}$	:	Wait
INTP0 to INTP3	:	Interrupt from Peripherals	ASTB	:	Address Strobe
TI1, TI2	:	Timer Input	X1, X2	:	Crystal (Main System Clock)
TO1, TO2	:	Timer Output	XT1, XT2	:	Crystal (Subsystem Clock)
SB0, SB1	:	Serial Bus	$\overline{\text{RESET}}$	:	Reset
SI0	:	Serial Input	V_{DD}	:	Power Supply
SO0	:	Serial Output	V_{SS}	:	Ground
$\overline{\text{SCK0}}$	:	Serial Clock	IC0 to IC3	:	Internally Connected

2. BLOCK DIAGRAM ★



Remark Internal ROM & RAM capacity varies depending on the product.

3. PIN FUNCTIONS

3.1 Port Pins (1/2)

Pin Name	I/O	Function		On Reset	Dual-Function Pin
P00	Input	Port 0 5-bit I/O port	Input only	Input	INTP0
P01	Input/ output		Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.	Input	INTP1
P02					INTP2
P03					INTP3
P04 [Note]	Input		Input only	Input	XT1
P10 to P17	Input/ output	Port 1 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.			–
P20	Input/ output	Port 2 8-bit input/output port. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.		Input	–
P21					–
P22					–
P23					–
P24					–
P25					SI0/SB0
P26					SO0/SB1
P27					$\overline{SCK0}$
P30	Input/ output	Port 3 8-bit input/output port. Input/output can be specified in bit-wise. When used as an input port, pull-up resistor can be used by software.		Input	–
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					–
P40 to P47	Input/ output	Port 4 8-bit input/output port. Input/output can be specified in 8-bit unit. When used as an input port, pull-up resistor can be used by software. Test input flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7

Note When using the P04/XT1 pins as an input port, set 1 to bit 6 (FRC) of the processor control register. (Do not use the on-chip feedback register of the subsystem clock oscillator.)

3.1 Port Pins (2/2)

Pin Name	I/O	Function		On Reset	Dual-Function Pin
P50 to P57	Input/ output	Port 5 8-bit input/output port. LED can be driven directly. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.		Input	A8 to A15
P60	Input/ output	Port 6 8-bit input/output port. Input/output can be specified bit-wise.	N-ch open-drain input/output port. On-chip pull-up resistor can be specified by mask option. LED can be driven directly.	Input	–
P61					
P62					
P63					
P64			When used as an input port, pull-up resistor can be used by software.		$\overline{RD}$
P65					$\overline{WR}$
P66					$\overline{WAIT}$
P67					ASTB

3.2 Other Pins

Pin Name	I/O	Function	After Reset	Dual-Function Pin
INTP0	Input	Effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified. External interrupt input.	Input	P00
INTP1				P01
INTP2				P02
INTP3		Falling edge detection external interrupt input.		P03
SI0	Input	Serial interface serial data input.	Input	P25/SB0
SO0	Output	Serial interface serial data output.	Input	P26/SB1
SB0	Input /output	Serial interface serial data input/output.	Input	P25/SI0
SB1				P26/SO0
$\overline{SCK0}$	Input /output	Serial interface serial clock input/output.	Input	P27
TI1	Input	External count clock input to 8-bit timer (TM1).	Input	P33
TI2		External count clock input to 8-bit timer (TM2).		P34
TO1	Output	8-bit timer (TM1) output.	Input	P31
TO2		8-bit timer (TM2) output.		P32
PCL	Output	Clock output (for main system clock, subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
AD0 to AD7	Input /output	Low-order address/data bus at external memory expansion.	Input	P40 to P47
A8 to A15	Output	High-order address bus at external memory expansion.	Input	P50 to P57
$\overline{RD}$	Output	External memory read operation strobe signal output.	Input	P64
$\overline{WR}$		External memory write operation strobe signal output.		P65
$\overline{WAIT}$	Input	Wait insertion at external memory access.	Input	P66
ASTB	Output	Strobe output which latches the address information output at port 4 and port 5 to access external memory.	Input	P67
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection.	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection.	Input	P04
XT2	—		—	—
V_{DD}	—	Positive power supply.	—	—
V_{SS}	—	Ground potential.	—	—
IC0 to IC3	—	Internal connection. IC0/IC1/IC3 and IC2 should be connected directly to V_{SS} V_{DD}, respecitively.	—	—

3.3 Pin I/O Circuit and Recommended Connection of Unused Pins

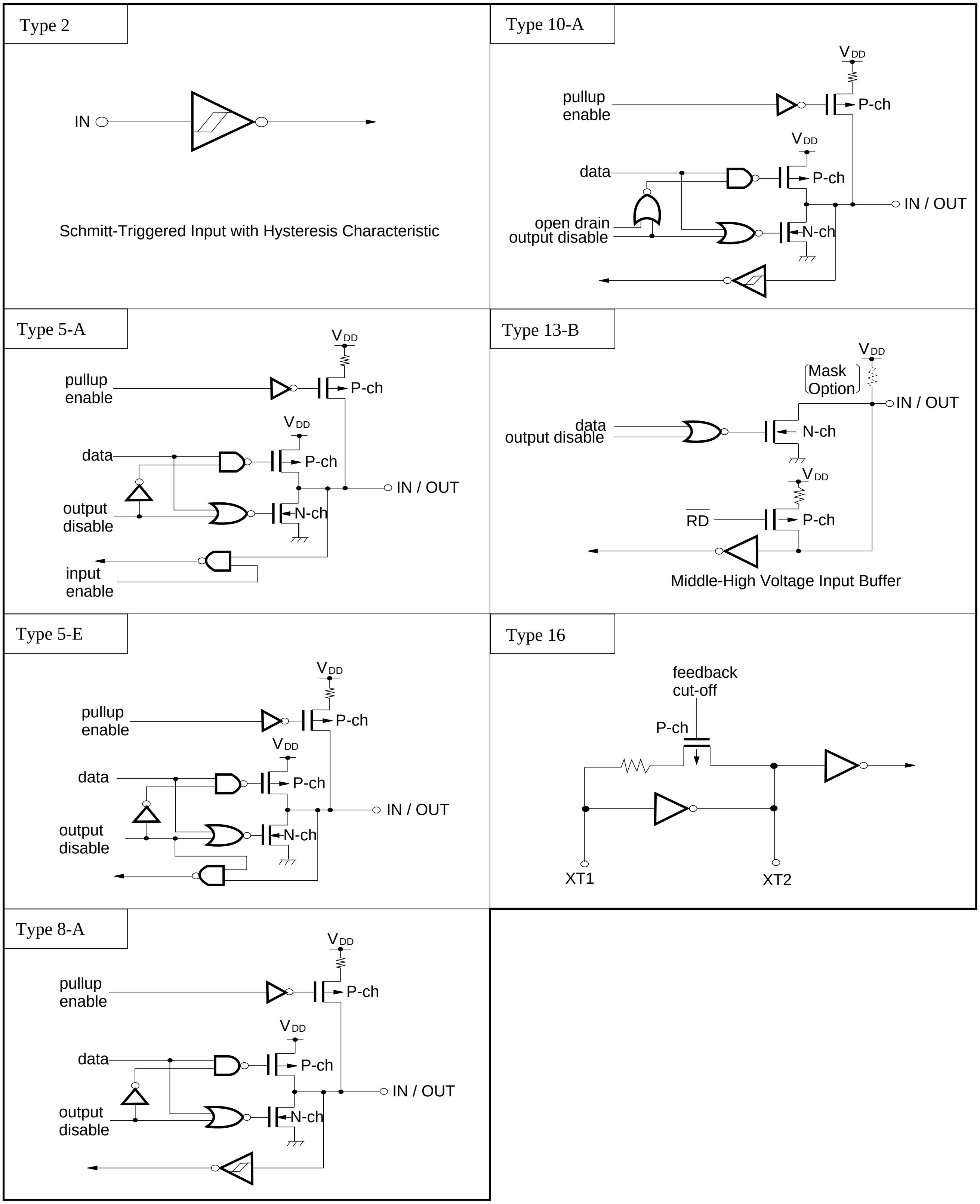
The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.

For the input/output circuit configuration of each type, see Figure 3-1.

Table 3-1. Input/Output Circuit Type of Each Pin

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection when Not Used
P00/INTP0	2	Input	Connected to V_{SS}.
P01/INTP1	8-A	Input/output	Connected to V_{SS} through resistor independently.
P02/INTP2			
P03/INTP3			
P04/XT1	16	Input	Connected to V_{DD} or V_{SS}.
P10 to P17	5-A	Input/output	Connected to V_{DD} or V_{SS} through resistor independently.
P20 to P24			
P25/SI0/SB0	10-A		
P26/SO0/SB1			
P27/$\overline{SCK0}$			
P30	5-A		
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0 to P47/AD7	5-E		Connected to V_{DD} through resistor independently.
P50/A8 to P57/A15	5-A		Connected to V_{DD} or V_{SS} through resistor independently.
P60 to P63	13-B		Connected to V_{DD} through resistor independently.
P64/$\overline{RD}$	5-A		Connected to V_{DD} or V_{SS} through resistor independently.
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
$\overline{RESET}$	2	Input	—
XT2	16	—	Leave open.
IC0, IC1, IC3	—		Connected to V_{SS} directly.
IC2			Connected to V_{DD} directly.

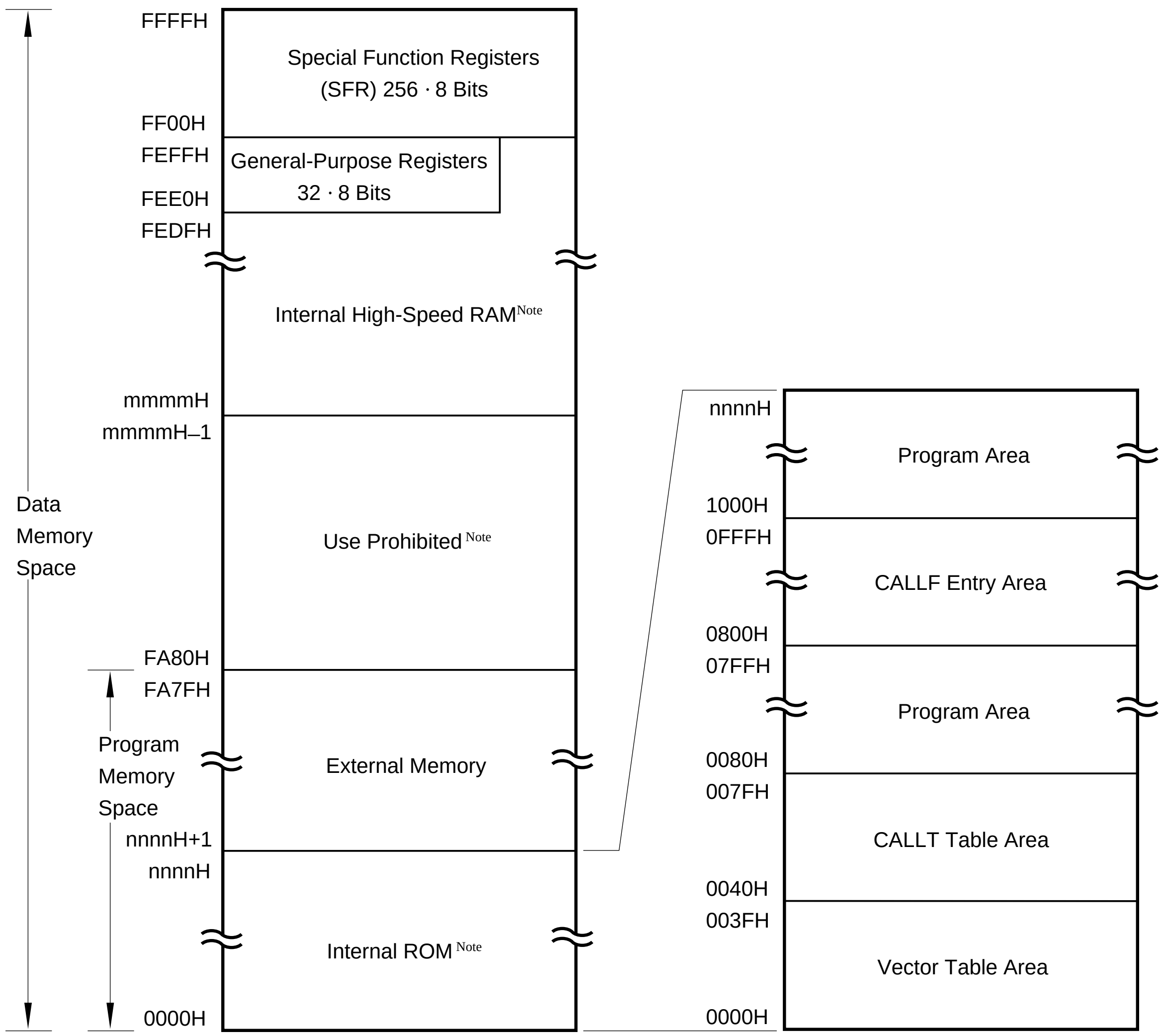
Figure 3-1. Pin Input/Output Circuits



4. MEMORY SPACE

The memory map of μPD78001B/78002B is shown in Figure 4-1.

Figure 4-1. Memory Map



Note Internal ROM and internal high-speed RAM capacities vary depending on the product (see the table below).

Product Name	Internal ROM End Address nnnnH	Internal High-Speed RAM Start Address mmmmH
μPD78001B	1FFFH	FE00H
μPD78002B	3FFFH	FD80H

5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 Ports

The I/O port has the following three types.

- CMOS input (P00, P04) : 2
- CMOS input/output (P01 to P03, port 1 to port 5, P64 to P67) : 47
- N-ch open-drain input/output (15V withstand voltage) (P60 to P63) : 4

Total : 53

Table 5-1. Functions of Ports

Port Name	Pin Name	Function
Port 0	P00, P04	Dedicated Input port
	P01 to P03	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.
Port 1	P10 to P17	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.
Port 2	P20 to P27	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.
Port 3	P30 to P37	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.
Port 4	P40 to P47	Input/output ports. Input/output can be specified in 8-bit units. When used as an input port, pull-up resistor can be used by software. Test input flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software. LED can be driven directly.
Port 6	P60 to P63	N-ch open-drain input/output port. Input/output can be specified bit-wise. On-chip pull-up resistor can be specified by mask option. LED can be driven directly.
	P64 to P67	Input/output ports. Input/output can be specified bit-wise. When used as an input port, pull-up resistor can be used by software.

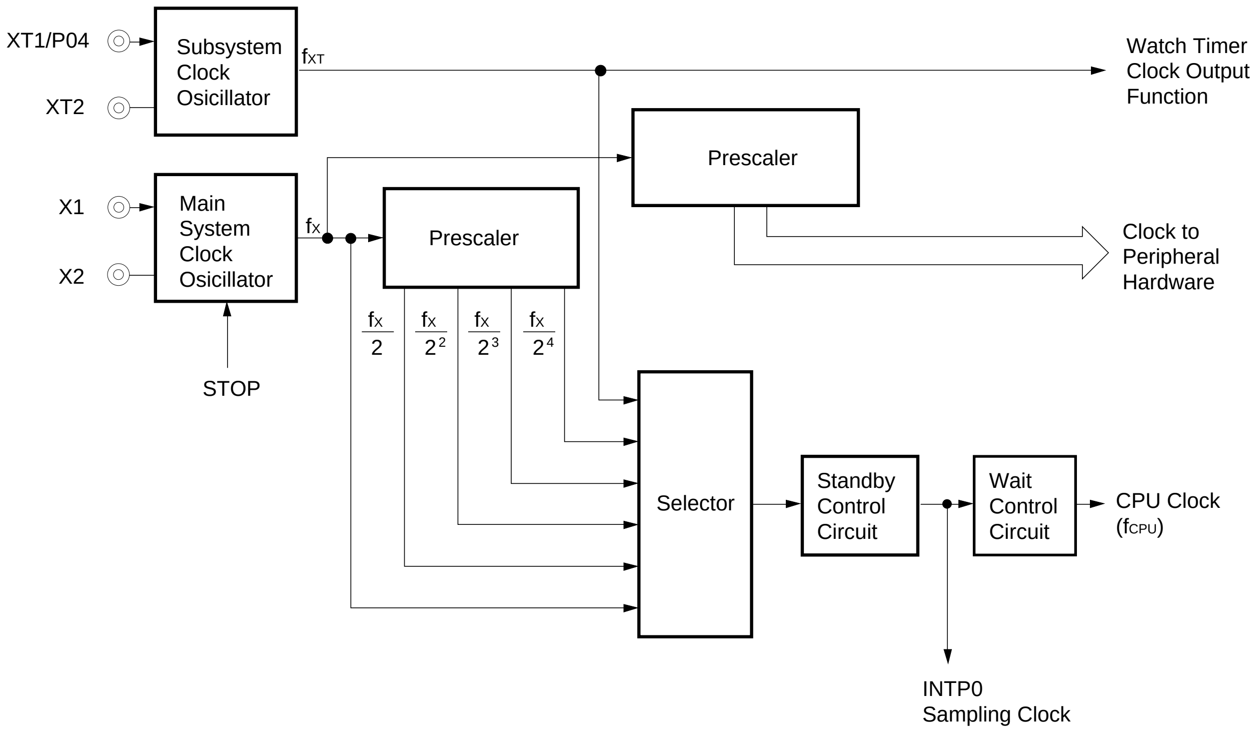
5.2 Clock Generator

There are two types of clock generator: main system clock and subsystem clock.

The instruction exection time can be changed.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (Main system clock: at 10.0 MHz operation)
- 122 μs (Subsystem clock: at 32.768 KHz operation)

Figure 5-1. Clock Generator Block Diagram



5.3 Timer/Event Counter

The following four channels are incorporated in the timer/event counter.

- 8-bit timer/event counter : 2 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2. Types and Features of Timer/Event Counter

		8-bit Timer/Event Counter	Watch Timer	Watchdog Timer
Type	Interval timer	2 channels	1 channel	1 channel
	External event counter	2 channels	–	–
Functions	Timer output	2 outputs	–	–
	Sqare wave output	2 outputs	–	–
	Interrupt request	2	1	1
	Test input	—	1	–

Figure 5-2. 8-Bit Timer/Event Counter Block Diagram

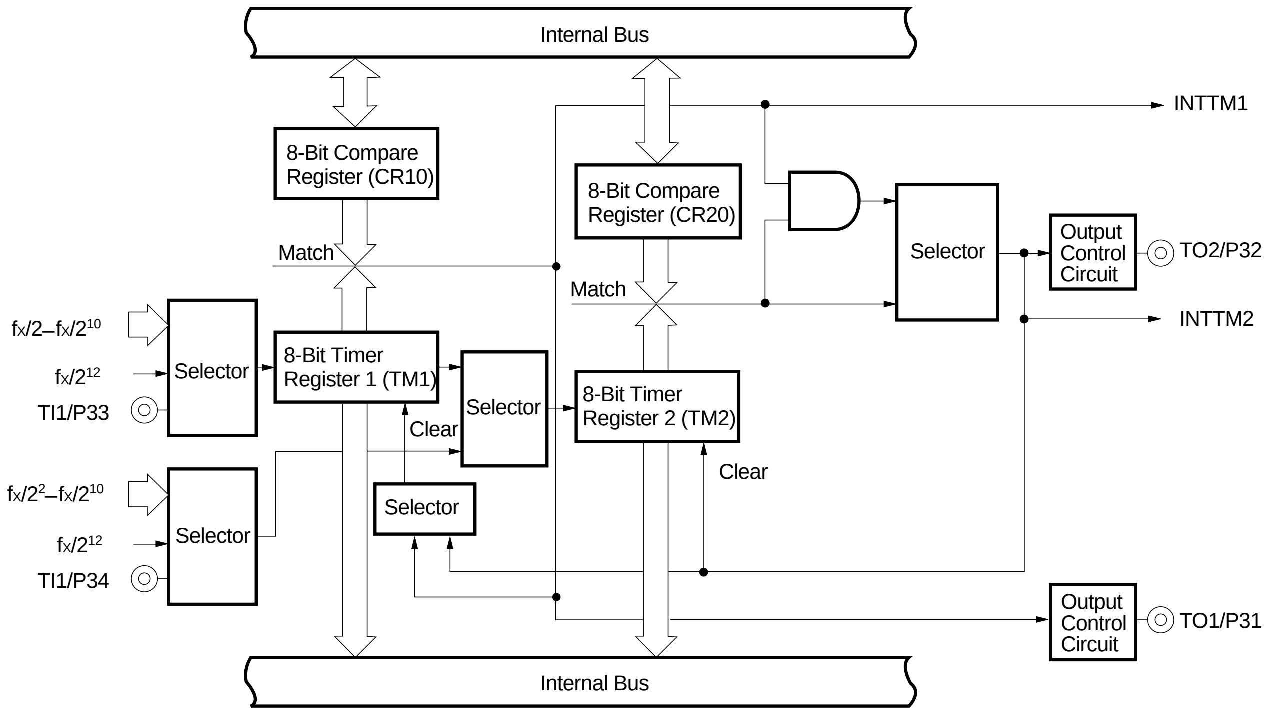


Figure 5-3. Watch Timer Block Diagram

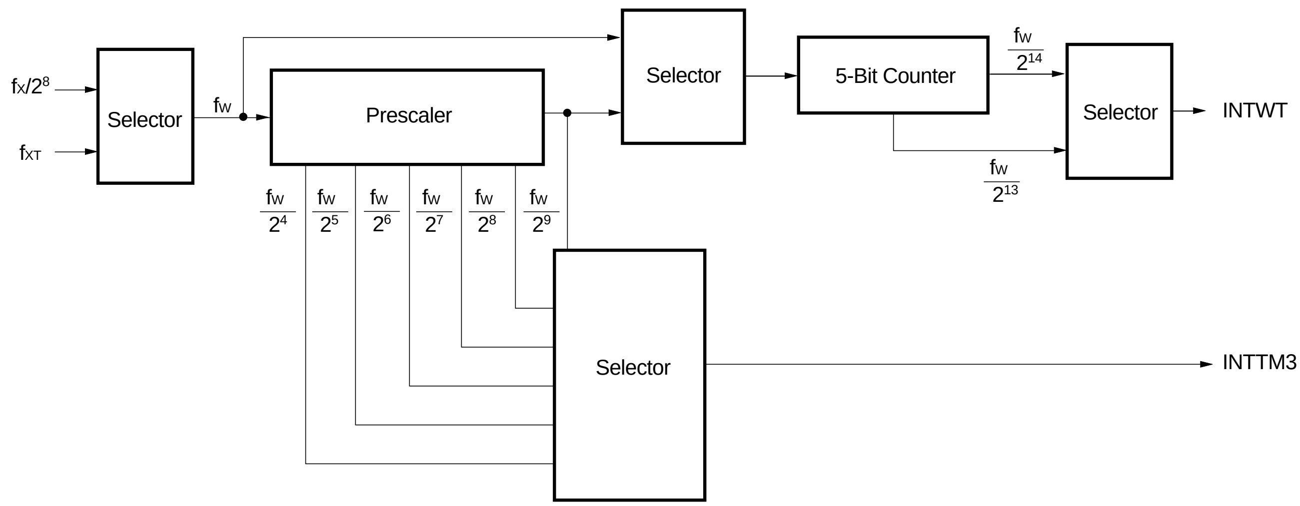
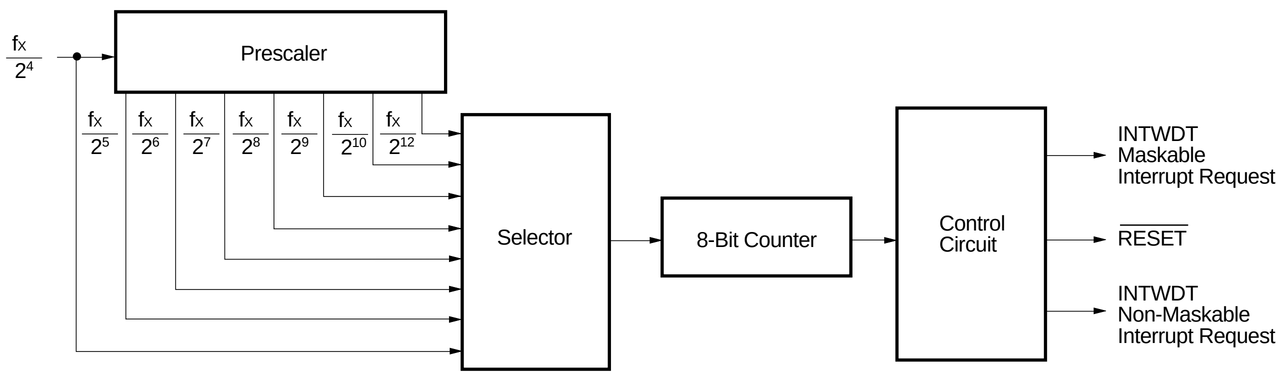


Figure 5-4. Watchdog Timer Block Diagram

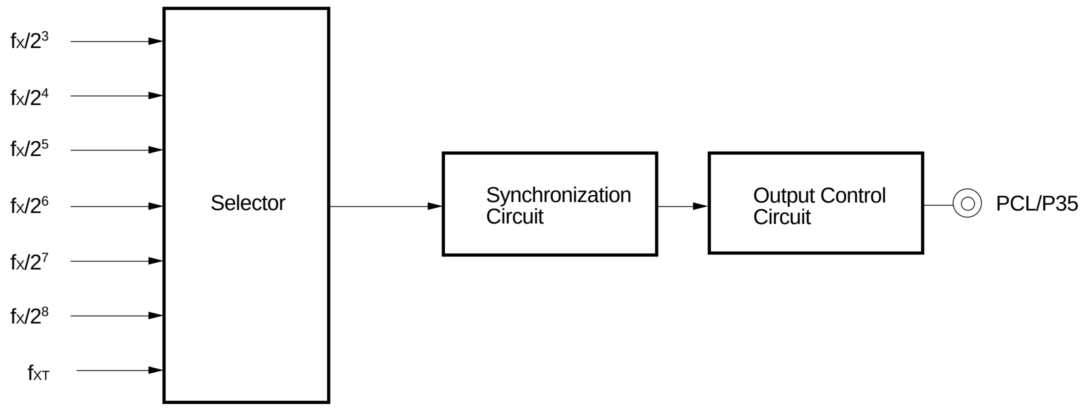


5.4 Clock Output Control Circuit

The clock with the following frequencies can be output for clock output.

- 39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz (Main system clock: at 10.0 MHz operation)
- 32.768 kHz (Subsystem clock: at 32.768 kHz operation)

Figure 5-5. Clock Output Control Block Diagram

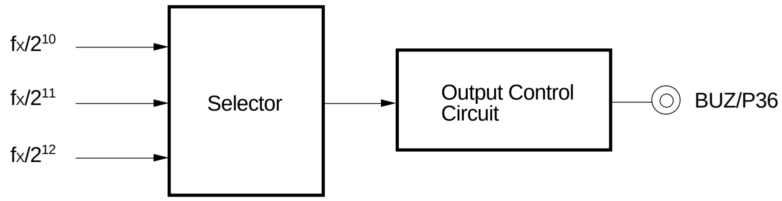


5.5 Buzzer Output Control Circuit

The clock with the following frequencies can be output for buzzer output.

- 2.4 kHz/4.9 kHz/9.8 kHz (Main system clock: at 10.0 MHz operation)

Figure 5-6. Buzzer Output Control Block Diagram



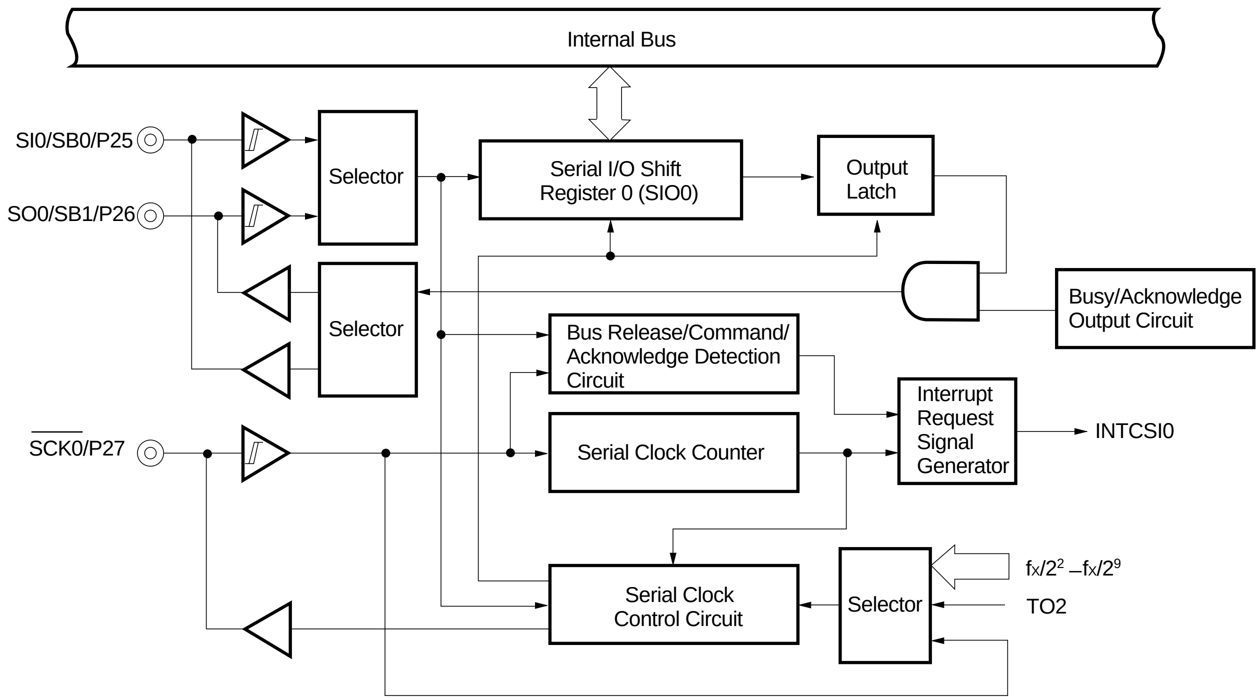
5.6 Serial Interfaces

There is one on-chip clocked serial interface.

Serial Interface channel 0 has the following three modes.

- 3-wire serial I/O mode : MSB/LSB-first switchable
- SBI (Serial Bus Interface) mode : MSB-first
- 2-wire serial I/O mode : MSB-first

Figure 5-7. Serial Interface Channel 0 Block Diagram



6. INTERRUPT FUNCTIONS AND DEST FUNCTIONS

6.1 Interrupt Functions

There are eleven interrupt functions of three different kinds as shown below.

- Non-maskable interrupt : 1
- Maskable interrupt : 9
- Software interrupt : 1

Table 6-1. Interrrupt Source List

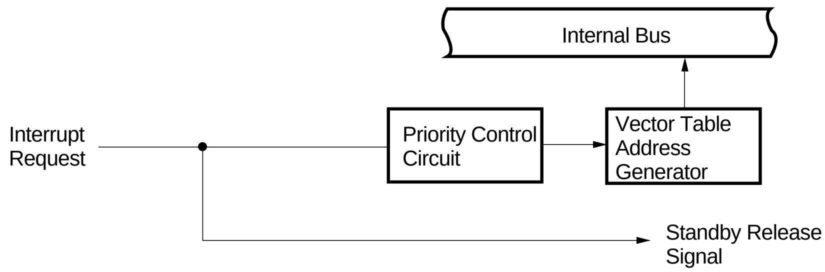
Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Adress	Basic Configuration Type Note 2
		Name	Trigger			
Non-maskable	——	INTWDT	Watchdog timer overflow (with watchdog timer mode interrupt selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	(D)
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTCSI0	Serial interface channel 0 transfer end	Internal	000EH	(B)
	6	INTTM3	Reference time interval signal from watch timer		0012H	
	7	INTTM1	8-bit timer/event counter 1 match signal generation		0016H	
	8	INTTM2	8-bit timer/event counter 2 match signal generation		0018H	
Software	——	BRK	BRK instruction execution	Internal	003EH	(E)

Notes 1. The default priority is the priority applicable when more priority than one maskable interrupt is generated. 0 is the highest and 11, the lowest.

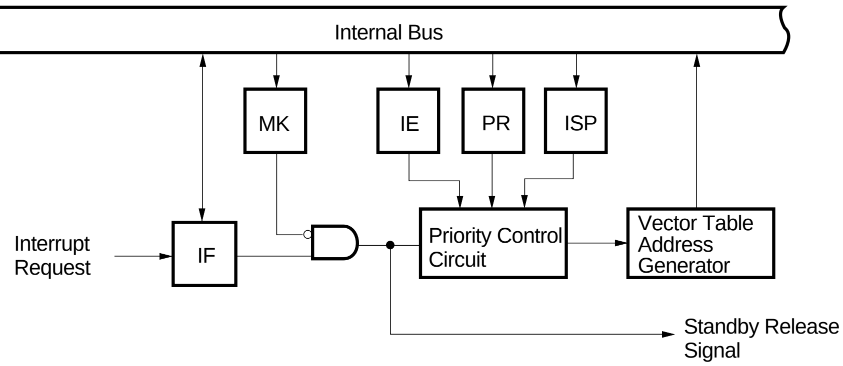
2. Basic configuration types (A) to (E) correspond to (A) to (E) on the next page.

Figure 6-1. Interrupt Function Basic Configuration (1/2)

(A) Internal Non-Maskable Interrupt



(B) Internal Maskable Interrupt



(C) External Maskable Interrupt (INTP0)

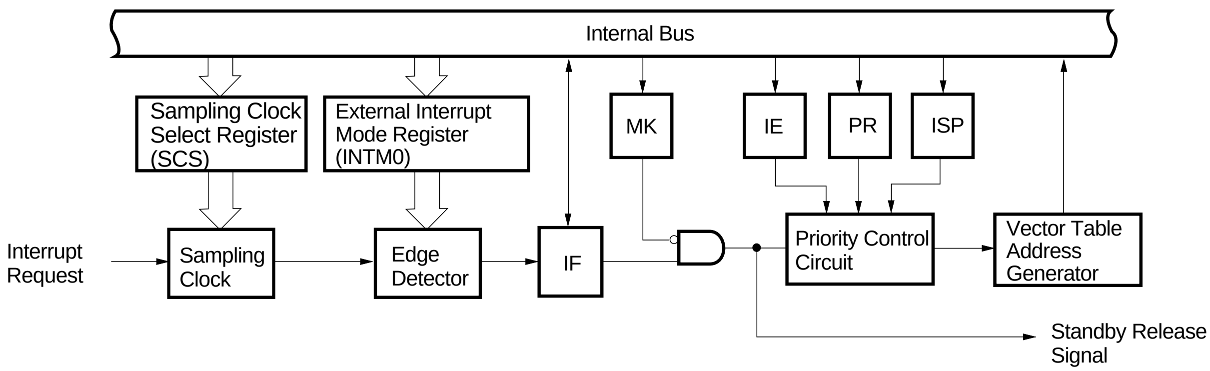
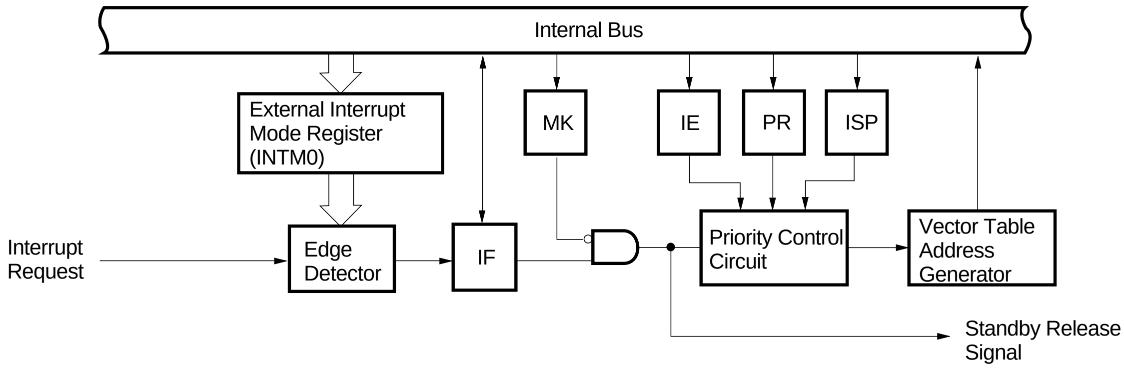
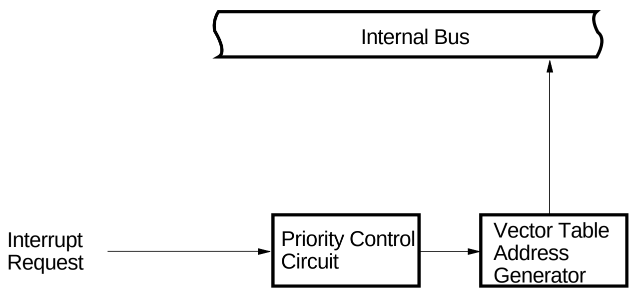


Figure 6-1. Interrupt Function Basic Configuration (2/2)

(D) External Maskable Interrupt (Except INTP0)



(E) Software Interrupt



IF : Interrupt request flag
IE : Interrupt enable flag
ISP : In-service priority flag
MK : Interrupt mask flag
PR : Priority spcification flag

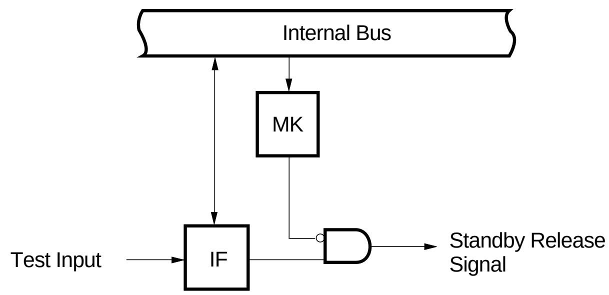
6.2 Test Functions

There are two test functions as shown in Table 6-2.

Table 6-2. Test Source List

Test Source		Internal/External
Name	Trigger	
INTWT	Watch timer overflow	Internal
NTPT4	Port 4 falling edge detection	External

Figure 6-2. Test Function Basic Configuration



IF : Test input flag
MK : Test mask flag

7. EXTERNAL DEVICE EXPANSION FUNCTIONS

The external device expansion function is used to connect external devices to areas other than the internal ROM, RAM and SFR.

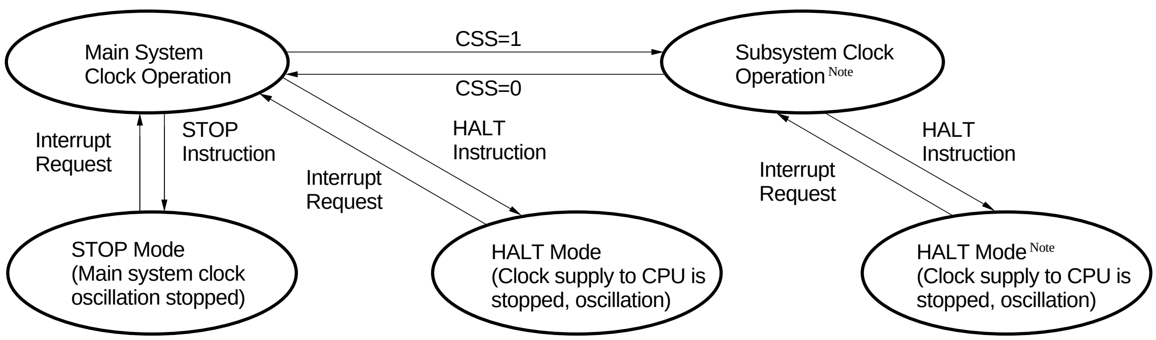
Ports 4 to 6 are used for connection with external devices.

8. STANDBY FUNCTIONS

There are the following two standby functions to reduce the current dissipation.

- HALT mode : The CPU operating clock is stopped. The average consumption current can be reduced by intermittent operation in combination with the normal operating mode.
- STOP mode : The main system clock oscillation is stopped. The whole operation by the main system clock is stopped, so that the system operates with ultra-low power consumption using only the subsystem clock.

Figure 8-1. Standby Functions



Note The power consumption can be reduced by stopping the main system clock. When the CPU is operating on the subsystem clock, set the MCC to stop the main system clock. The STOP instruction cannot be used.

Caution When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program by the program.

9. RESET FUNCTION

There are the following two reset methods.

- External reset input by $\overline{\text{RESET}}$ pin.
- Internal reset by watchdog timer runaway time detection.

10. INSTRUCTION SET

(1) 8-Bit Instruction

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

1st Operand \ 2nd Operand	#byte	A	r Note	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL+B] [HL+C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
r1											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL+byte] [HL+B] [HL+C]		MOV											

Note Except r = A

(2) 16-Bit Instruction

MOVW, XCHW ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

2nd Operand / 1st Operand	#word	AX	rp [Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW [Note]						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, HL.

(3) Bit Operation Instruction

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

2nd Operand / 1st Operand	A.bit	sfr.bit	saddr.bit	PWS.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call Instruction/Branch Instruction

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF,BTCLR, DBNZ

2nd Operand / 1st Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL, BR	CALLF	CALLT	BR, BC, BNC, BZ, BNZ
Compound instruction					BT, BF, BTCLR, DBNZ

(5) Other Instruction

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Test Conditions		Rating	Unit
Supply voltage	V_{DD}			–0.3 to + 7.0	V
Input voltage	V_{I1}	P00 to P04, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, X1, X2, XT2		–0.3 to V_{DD} + 0.3	V
	V_{I2}	P60 to P63	N-ch open-drain	–0.3 to +16	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current high	I_{OH}	1 pin		–10	mA
		P10 to P17, P20 to P27, P30 to P37 total		–15	mA
		P01 to P03, P40 to P47, P50 to P57, P60 to P67 total		–15	mA
Output current low	I_{OL} Note	1 pin	Peak value	30	mA
			RMS	15	mA
		P40 to P47, P50 to P55 total	Peak value	100	mA
			RMS	70	mA
		P01 to P03, P56, P57, P60 to P67 total	Peak value	100	mA
			RMS	70	mA
		P01 to P03, P64 to P67 total	Peak value	50	mA
			RMS	20	mA
		P10 to P17, P20 to P27, P30 to P37 total	Peak value	50	mA
			RMS	20	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note RMS should be calculated as follows: $[RMS] = [Peak\ value] \times \sqrt{duty}$

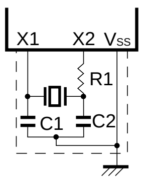
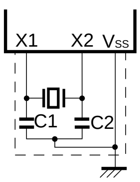
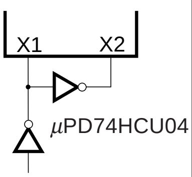
Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. That is, the absolute maximuam ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

Capacitance (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f=1 MHz Unmeasured pins returned to 0 V				15	pF
I/O capacitance	C_{IO}	f=1 MHz Unmeasured pins returned to 0 V	P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 toP47, P50 to P57, P64 to P67			15	pF
			P60 to P63			20	pF

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

Main System Clock Oscillation Circuit Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (f_X) Note 1	V_{DD} = Oscillator voltage range	1		10	MHz
		Oscillation stabilization time Note 2	After V_{DD} reaches oscillator voltage range MIN.			4	ms
Crystal resonator		Oscillator frequency (f_X) Note 1		1	8.38	10	MHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 6.0 V			10	ms
						30	
External clock		X1 input frequency (f_X) Note 1		1.0		10.0	MHz
		X1 input high/low level width (t_{XH} , t_{XL})		42.5		500	ns

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

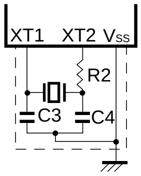
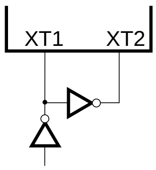
2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wiring the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

Subsystem Clock Oscillation Circuit Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillator frequency (f_{XT}) Note 1		32	32.768	35	kHz
		Oscillation stabilization time Note 2	V_{DD} = 4.5 to 6.0 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT}) Note 1		32		100	kHz
		XT1 input high/low level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillator voltage MIN.

Cautions 1. When using the subsystem clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground wiring to a ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. The subsystem clock oscillation circuit is a circuit with a low amplification level, more prone to misoperation due to noise than the main system clock. When using the subsystem clock, special care is needed regarding the wiring method.

Recommended Oscillation Circuit Constant

Main System Clock Ceramic Resonator (T_A = –40 to +85 °C)

Manufacturer	Products	Frequency (MHz)	Recommended Oscillation Constant			Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)
Murata m.f.g.	CSB1000J	1.00	100	100	6.8	2.9	6.0
	CSB××××J	1.01-1.25	100	100	4.7	2.7	6.0
	CSA×.×××MK	1.26-1.79	100	100	0	2.7	6.0
	CSA×.××MG	1.80-2.44	100	100	0	2.7	6.0
	CST×.××MG		On-chip	On-chip	0	2.7	6.0
	CSA×.××MG	2.45-4.18	30	30	0	2.7	6.0
	CST×.××MGW		On-chip	On-chip	0	2.7	6.0
	CSA×.××MG	4.19-6.00	30	30	0	2.7	6.0
	CST×.××MGW		On-chip	On-chip	0	2.7	6.0
	CSA×.××MT	6.01-10.0	30	30	0	2.9	6.0
	CST×.××MTW		On-chip	On-chip	0	2.9	6.0
Kyocera Corporation	KBR-4.19MWS	4.19	–	–	–	2.7	6.0
	KBR-4.19MKS						
	KBR-4.19MSA	4.19	33	33	–	2.7	6.0
	PBRC4.19A						
	KBR-10.0M	10.0	33	33	–	2.8	6.0
	KBR-1000F	1.00	100	100	2.2	2.7	6.0
	KBR-1000Y						

Remark ××××, ×.×××, ×.×× indicates frequency.

Subsystem Clock: Crystal Resonator (T_A = –40 to +60 °C)

Manufacturer	Products	Frequency (MHz)	Recommended Circuit Constant			Oscillation Voltage Range	
			C3 (pF)	C4 (pF)	R2 (kΩ)	MIN. (V)	MAX. (V)
Daishinku corp.	DT-38 (1TA632E00, Load capacitance 6.3pF)	32.768	8	8	100	2.7	6.0

Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency of the resonator in the application circuit. For this, it is necessary to directly contact the manufacturer of the resonator being used. ★

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

<table>
<tr><th>Parameter</th><th>Symbol</th><th colspan="3">Test Conditions</th><th>MIN.</th><th>TYP.</th><th>MAX.</th><th>Unit</th></tr>
<tr><td rowspan="6">Input voltage high</td><td>V_{IH1}</td><td colspan="3">P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67</td><td>0.7 V_{DD}</td><td></td><td>V_{DD}</td><td>V</td></tr>
<tr><td>V_{IH2}</td><td colspan="3">P00 to P03, P20, P22, P24 to P27, P33, P34, $\overline{RESET}$</td><td>0.8 V_{DD}</td><td></td><td>V_{DD}</td><td>V</td></tr>
<tr><td>V_{IH3}</td><td>P60 to P63</td><td colspan="2">Open-drain</td><td>0.7 V_{DD}</td><td></td><td>15</td><td>V</td></tr>
<tr><td>V_{IH4}</td><td colspan="3">X1, X2</td><td>V_{DD}–0.5</td><td></td><td>V_{DD}</td><td>V</td></tr>
<tr><td rowspan="2">V_{IH5}</td><td rowspan="2">XT1/P04, XT2</td><td colspan="2">V_{DD} = 4.5 to 6.0 V</td><td>V_{DD}–0.5</td><td></td><td>V_{DD}</td><td>V</td></tr>
<tr><td colspan="2"></td><td>V_{DD}–0.3</td><td></td><td>V_{DD}</td><td>V</td></tr>
<tr><td rowspan="8">Input voltage low</td><td>V_{IL1}</td><td colspan="3">P10 to P17, P21, P23, P30 to P32, P35 to P37
P40 to P47, P50 to P57, P64 to P67</td><td>0</td><td></td><td>0.3 V_{DD}</td><td>V</td></tr>
<tr><td>V_{IL2}</td><td colspan="3">P00 to P03, P20, P22, P24 to P27, P33, P34, $\overline{RESET}$</td><td>0</td><td></td><td>0.2 V_{DD}</td><td>V</td></tr>
<tr><td rowspan="2">V_{IL3}</td><td rowspan="2">P60 to P63</td><td colspan="2">V_{DD} = 4.5 to 6.0 V</td><td>0</td><td></td><td>0.3 V_{DD}</td><td>V</td></tr>
<tr><td colspan="2"></td><td>0</td><td></td><td>0.2 V_{DD}</td><td>V</td></tr>
<tr><td>V_{IL4}</td><td colspan="3">X1, X2</td><td>0</td><td></td><td>0.4</td><td>V</td></tr>
<tr><td rowspan="2">V_{IL5}</td><td rowspan="2">XT1/P04, XT2</td><td colspan="2">V_{DD} = 4.5 to 6.0 V</td><td>0</td><td></td><td>0.4</td><td>V</td></tr>
<tr><td colspan="2"></td><td>0</td><td></td><td>0.3</td><td>V</td></tr>
<tr><td rowspan="2">Output voltage high</td><td rowspan="2">V_{OH1}</td><td colspan="3">V_{DD} = 4.5 to 6.0 V, I_{OH} = –1 mA</td><td>V_{DD}–1.0</td><td></td><td></td><td>V</td></tr>
<tr><td colspan="3">I_{OH} = –100 μA</td><td>V_{DD}–0.5</td><td></td><td></td><td>V</td></tr>
<tr><td rowspan="4">Output voltage low</td><td rowspan="2">V_{OL1}</td><td>P50 to P57, P60 to P63</td><td colspan="2">V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA</td><td></td><td>0.4</td><td>2.0</td><td>V</td></tr>
<tr><td>P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67</td><td colspan="2">V_{DD} = 4.5 to 6.0 V, I_{OL} = 1.6 mA</td><td></td><td></td><td>0.4</td><td>V</td></tr>
<tr><td>V_{OL2}</td><td>SB0, SB1, $\overline{SCK0}$</td><td colspan="2">V_{DD} = 4.5 to 6.0 V,
open-drain
pulled-up (R = 1 KΩ)</td><td></td><td></td><td>0.2 V_{DD}</td><td>V</td></tr>
<tr><td>V_{OL3}</td><td colspan="3">I_{OL} = 400 μA</td><td></td><td></td><td>0.5</td><td>V</td></tr>
<tr><td rowspan="3">Input leakage current high</td><td>I_{LIH1}</td><td rowspan="2">V_{IN} = V_{DD}</td><td colspan="2">P00 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, $\overline{RESET}$</td><td></td><td></td><td>3</td><td>μA</td></tr>
<tr><td>I_{LIH2}</td><td colspan="2">X1, X2, XT1/P04, XT2</td><td></td><td></td><td>20</td><td>μA</td></tr>
<tr><td>I_{LIH3}</td><td>V_{IN} = 15 V</td><td colspan="2">P60 to P63</td><td></td><td></td><td>80</td><td>μA</td></tr>
<tr><td rowspan="4">Input leakage current high</td><td>I_{LIL1}</td><td rowspan="4">V_{IN} = 0 V</td><td colspan="2">P00 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, $\overline{RESET}$</td><td></td><td></td><td>–3</td><td>μA</td></tr>
<tr><td>I_{LIL2}</td><td colspan="2">X1, X2, XT1/P04, XT2</td><td></td><td></td><td>–20</td><td>μA</td></tr>
<tr><td rowspan="2">I_{LIL3}</td><td rowspan="2">P60 to P63</td><td>Note 1</td><td></td><td></td><td>–200</td><td>μA</td></tr>
<tr><td>Other than above</td><td></td><td></td><td>–3 Note 2</td><td>μA</td></tr>
</table>

Notes 1. When memory expansion mode is used by the memory expansion mode register (MM) with no on-chip pull-up resistor by mask option.

2. When pull-up resistors are not used (specified by mask option), the low-level input leakage current increases with –200 μA (MAX.) under either of the following conditions.

<1> When the external device expansion function is used and a low level is input to the pin.

<2> During the 3-clock period when a read instruction is executed on port 6 (P6) and the port mode registor (PM6).

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit	
Output leakage current high	I_{LOH1}	$V_{OUT} = V_{DD}$				3	μA	
Output leakage current low	I_{LOL}	V_{OUT} = 0 V				–3	μA	
Mask option pull-up resistor	R_1	V_{IN} = 0 V, P60 to P63		20	40	90	kΩ	
Software pull-up resistor	R_2	VIN = 0 V, P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67	4.5 V ≤ V_{DD} ≤ 6.0 V	15	40	90	kΩ	
				15		90	kΩ	★
Power supply current Note 3	I_{DD1}	8.38 MHz Crystal oscillation operating mode	V_{DD} = 5.0 V ± 10 % Note 1		7.5	22.5	mA	
			V_{DD} = 3.0 V ± 10 % Note 2		0.8	2.4	mA	
	I_{DD2}	8.38 MHz Crystal oscillation HALT mode	V_{DD} = 5.0 V ± 10 %		1.4	4.2	mA	
			V_{DD} = 3.0 V ± 10 %		550	1650	μA	
	I_{DD3}	32.768 kHz Crystal oscillation operating mode	V_{DD} = 5.0 V ± 10 %		60	120	μA	
			V_{DD} = 3.0 V ± 10 %		35	70	μA	
	I_{DD4}	32.768 kHz Crystal oscillation HALT mode	V_{DD} = 5.0 V ± 10 %		25	50	μA	
			V_{DD} = 3.0 V ± 10 %		5	10	μA	
	I_{DD5}	XT1 = 0 V STOP mode When feedback resistor is used	V_{DD} = 5.0 V ± 10 %		1	20	μA	
			V_{DD} = 3.0 V ± 10 %		0.5	10	μA	
	I_{DD6}	XT1 = 0 V STOP mode When feedback resistor is unused	V_{DD} = 5.0 V ± 10 %		0.1	20	μA	
			V_{DD} = 3.0 V ± 10 %		0.05	10	μA	

Notes 1. Operating in high-speed mode (when set the processor clock control register (PCC) to 00H).

2. Operating in low-speed mode (when set the PCC to 04H).

3. Port current are excluded.

Remark The characteristics of a dual-function pin and a port pin are the same unless specified otherwise.

AC Characteristics (T_A = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

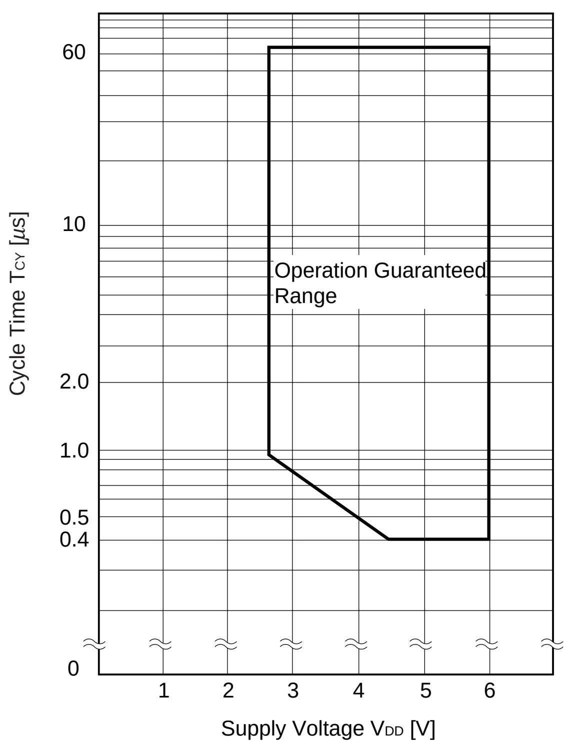
(1) Basic Operation

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Min. instruction execution time)	T_{CY}	Operating on main system clock	V_{DD} = 4.5 to 6.0 V	0.4		64	μs
				0.96		64	μs
		Operationg on subsystem clock		40	122	125	μs
TI, TI2 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		4	MHz
				0		275	kHz
TI, TI2 input high/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		100			ns
				1.8			μs
Interrupt input high/low-level width	t_{INTH}, t_{INTL}	INTP0		$8/f_{sam}$ Note			μs
		INTP1 to INTP3		10			μs
		KR0 to KR7		10			μs
$\overline{\text{RESET}}$ low level width	t_{RSL}			10			μs

Notes In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register (SCS), selection of f_{sam} is possible between $f_X/2^{N+1}$, $f_X/64$ and $f_X/128$ (when N = 0 to 4).

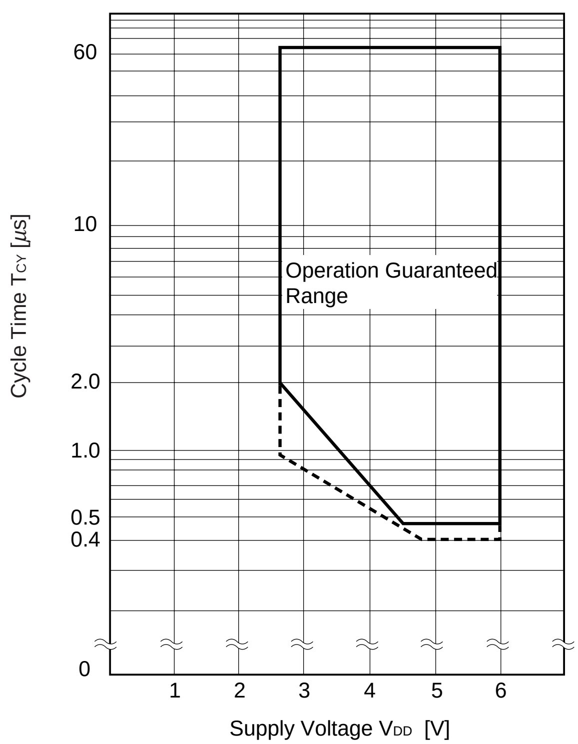
μPD78001B, 78002B

T_{CY} vs V_{DD} (At main system clock operation)



μPD78P014 (Reference)

T_{CY} vs V_{DD} (At main system clock operation)



Remark - - - - indicates T_A = –40 to +40 °C
——— indicates T_A = –40 to +85 °C

Caution The operation guaranteed range of the μPD78001B, and 78002B differs from that of the μPD78P014.

(2) Read/Write Operation (T_A = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.5t_{CY}$		ns
Address setup time	t_{ADS}		$0.5t_{CY}–30$		ns
Address hold time	t_{ADH}	Load resistance ≥ 5 kΩ	10		ns
Data input time from address	t_{ADD1}			$(2+2n)t_{CY}–50$	ns
	t_{ADD2}		5	$(3+2n)t_{CY}–100$	ns
Data input time from $\overline{\text{RD}}\downarrow$	t_{RDD1}			$(1+2n)t_{CY}–25$	ns
	t_{RDD2}			$(2.5+2n)t_{CY}–100$	ns
Read data hold time	t_{RDH}		0		ns
$\overline{\text{RD}}$ low-level width	t_{RDL1}		$(1.5+2n)t_{CY}–20$		ns
	t_{RDL2}		$(2.5+2n)t_{CY}–20$		ns
$\overline{\text{WAIT}}\downarrow$ input time from $\overline{\text{RD}}\downarrow$	t_{RDWT1}			$0.5t_{CY}$	ns
	t_{RDWT2}			$1.5t_{CY}$	ns
$\overline{\text{WAIT}}\downarrow$ input time from $\overline{\text{WR}}\downarrow$	t_{WRWT}			$0.5t_{CY}$	ns
$\overline{\text{WAIT}}$ low-level width	t_{WTL}		$(0.5+2n)t_{CY}$ +10	$(2+2n)t_{CY}$	ns
Write data setup time	t_{WDS}		100		ns
Write data hold time	t_{WDH}		5		ns
$\overline{\text{WR}}$ low-level width	t_{WRL}		$(2.5+2n)t_{CY}$ –20		ns
$\overline{\text{RD}}\downarrow$ delay time from ASTB$\downarrow$	t_{ASTRD}		$0.5t_{CY}–30$		ns
$\overline{\text{WR}}\downarrow$ delay time from ASTB$\downarrow$	t_{ASTWR}		$1.5t_{CY}$ –30		ns
ASTB$\uparrow$ delay time from $\overline{\text{RD}}\uparrow$ in external fetch	t_{RDAST}		$t_{CY}–10$	$t_{CY}+40$	ns
Address hold time from $\overline{\text{RD}}\uparrow$ in external fetch	t_{RDADH}		t_{CY}	$t_{CY}+50$	ns
Write data output time from $\overline{\text{RD}}\uparrow$	t_{RDWD}		10		ns
$\overline{\text{WR}}\downarrow$ delay time from write data	t_{WDWR}	V_{DD} = 4.5 to 6.0 V	$0.5t_{CY}–120$	$0.5t_{CY}$	ns
			$0.5t_{CY}–170$	$0.5t_{CY}$	ns
Address hold time from $\overline{\text{WR}}\uparrow$	t_{WRADH}	V_{DD} =4.5 to 6.0 V	t_{CY}	$t_{CY}+60$	ns
			t_{CY}	$t_{CY}+100$	ns
$\overline{\text{RD}}\uparrow$ delay time from $\overline{\text{WAIT}}\uparrow$	t_{WTRD}		$0.5t_{CY}$	$2.5t_{CY}+80$	ns
$\overline{\text{WR}}\uparrow$ delay time from $\overline{\text{WAIT}}\uparrow$	t_{WTWR}		$0.5t_{CY}$	$2.5t_{CY}+80$	ns

Remarks **1.** $t_{CY} = T_{CY}/4$

2. n indicates number of waits.

3. C_L = 100 pF (C_L indicates load capacitance of P40/AD0 to P47/AD7, P50/A8 to P57/A15, P64/$\overline{\text{RD}}$, P65/$\overline{\text{WR}}$, P66/$\overline{\text{WAIT}}$, P67/ASTB pins).

(3) Serial Interface (T_A = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

(a) 3-wire serial I/O mode ($\overline{\text{SCK0}}$... Internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V	800			ns
$\overline{\text{SCK0}}$ cycle time	t_{KCY1}		3200			ns
$\overline{\text{SCK0}}$ high/low-level width	t_{KH1}	V_{DD} = 4.5 to 6.0 V	t_{KCY1}/2–50			ns
$\overline{\text{SCK0}}$ high/low-level width	t_{KL1}		t_{KCY1}/2–150			ns
SI0 setup time (to $\overline{\text{SCK0}}$↑)	t_{SIK1}		100			ns
SI0 hold time (from $\overline{\text{SCK0}}$↑)	t_{KSI1}		400			ns
SO0 output delay time from $\overline{\text{SCK0}}$↓	t_{KSO1}	C = 100 pF Note, V_{DD} = 4.5 to 6.0 V			300	ns
SO0 output delay time from $\overline{\text{SCK0}}$↓	t_{KSO1}	C = 100 pF Note			1000	ns

Note C is the load capacitance of SO0 output line.

(b) 3-wire serial I/O mode ($\overline{\text{SCK0}}$... External clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK0}}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V	800			ns
$\overline{\text{SCK0}}$ cycle time	t_{KCY2}		3200			ns
$\overline{\text{SCK0}}$ high/low-level width	t_{KH2}	V_{DD} = 4.5 to 6.0 V	400			ns
$\overline{\text{SCK0}}$ high/low-level width	t_{KL2}		1600			ns
SI0 setup time (to $\overline{\text{SCK0}}$↑)	t_{SIK2}		100			ns
SI0 hold time (from $\overline{\text{SCK0}}$↑)	t_{KSI2}		400			ns
SO0 output delay time from $\overline{\text{SCK0}}$↓	t_{KSO2}	C = 100 pF Note, V_{DD} = 4.5 to 6.0 V			300	ns
SO0 output delay time from $\overline{\text{SCK0}}$↓	t_{KSO2}	C = 100 pF Note			1000	ns
$\overline{\text{SCK0}}$ rise, fall time	t_{R2}	When external device expansion function is used			160	ns
$\overline{\text{SCK0}}$ rise, fall time	t_{F2}	When external device expansion function is not used			1000	ns

Note C is the load capacitance of SO0 output line.

(c) SBI mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK0}$ high/low-level width	t_{KH3}	V_{DD} = 4.5 to 6.0 V		t_{KCY3}/2–50			ns
	t_{KL3}			t_{KCY3}/2–150			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK3}	V_{DD} = 4.5 to 6.0 V		100			ns
				300			ns
SB0, SB1 hold time from $\overline{SCK0}$↓	t_{KSI3}			t_{KCY3}/2			ns
SB0, SB1 output delay time (from $\overline{SCK0}$↑)	t_{KSO3}	R = 1 kΩ, C = 100 pF Note	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output line.

(d) SBI mode ($\overline{SCK0}$... External clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK0}$ high/low-level width	t_{KH4}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KL4}			1600			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK4}	V_{DD} = 4.5 to 6.0 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK0}$↓)	t_{KSI4}			t_{KCY4}/2			ns
SB0, SB1 output delay time from $\overline{SCK0}$↑	t_{KSO4}	R = 1 kΩ, C = 100 pF Note	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK0}$↓ from SB0, SB10↓	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns
$\overline{SCK0}$ rise, fall time	t_{R4}	When external device expansion function is used				160	ns
	t_{F4}	When external device expansion function is not used				1000	ns

Note R and C are the load resistance and load capacitance of the SB0 and SB1 output line.

(e) 2-wire serial I/O mode ($\overline{SCK0}$... Internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK0}$ high-level width	t_{KH5}	R = 1 kΩ, C = 100 pF Note		t_{KCY5}/2–50			ns
$\overline{SCK0}$ low-level width	t_{KL5}			t_{KCY5}/2–50			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK5}			300			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI5}			600			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO5}	R = 1 kΩ, C = 100 pF Note	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns

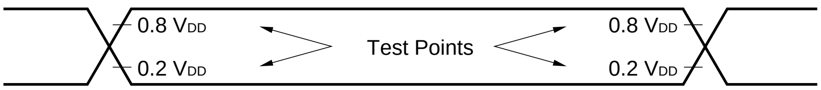
Note R and C are the load resistance and load capacitance of the $\overline{SCK0}$, SB0 and SB1 output line.

(f) 2-wire serial I/O mode ($\overline{SCK0}$... External clock input)

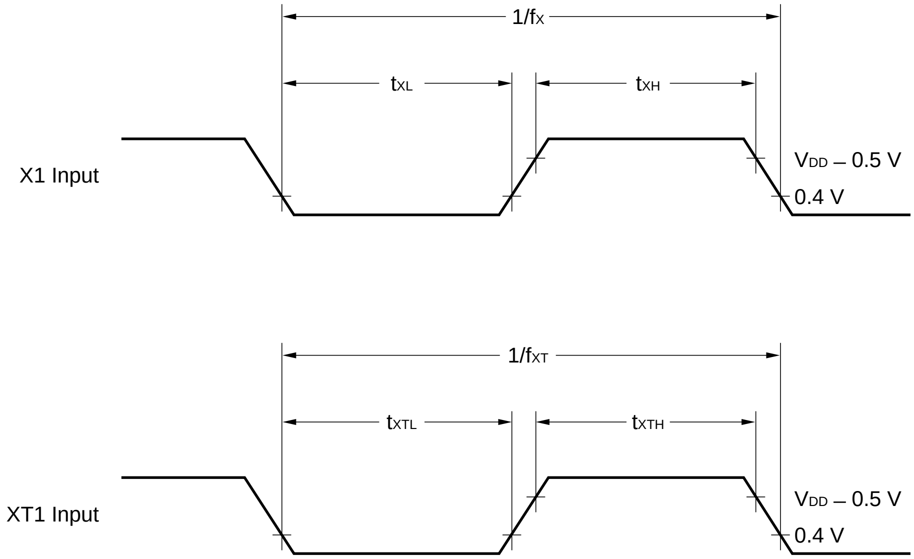
Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK0}$ high-level width	t_{KH6}			650			ns
$\overline{SCK0}$ low-level width	t_{KL6}			800			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK6}			100			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI6}			t_{KCY6}/2			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO6}	R = 1 kΩ, C = 100 pF Note	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
$\overline{SCK0}$ rise, fall time	t_{R6}, t_{F6}	When external device expansion function is used				160	ns
		When external device expansion function is not used				1000	ns

Note R and C are the load resistance and load capacitance of the $\overline{SCK0}$, SB0 and SB1 output line.

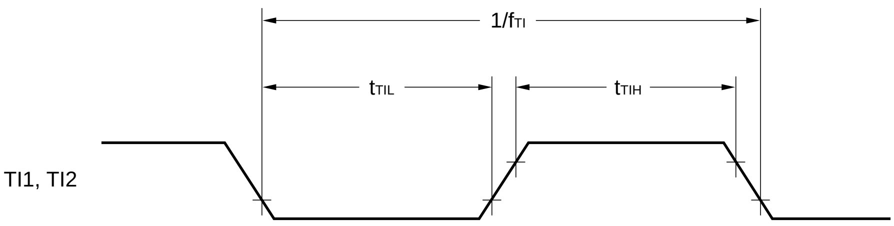
AC Timing Test Point (Excluding X1, XT1 Input)



Clock Timing

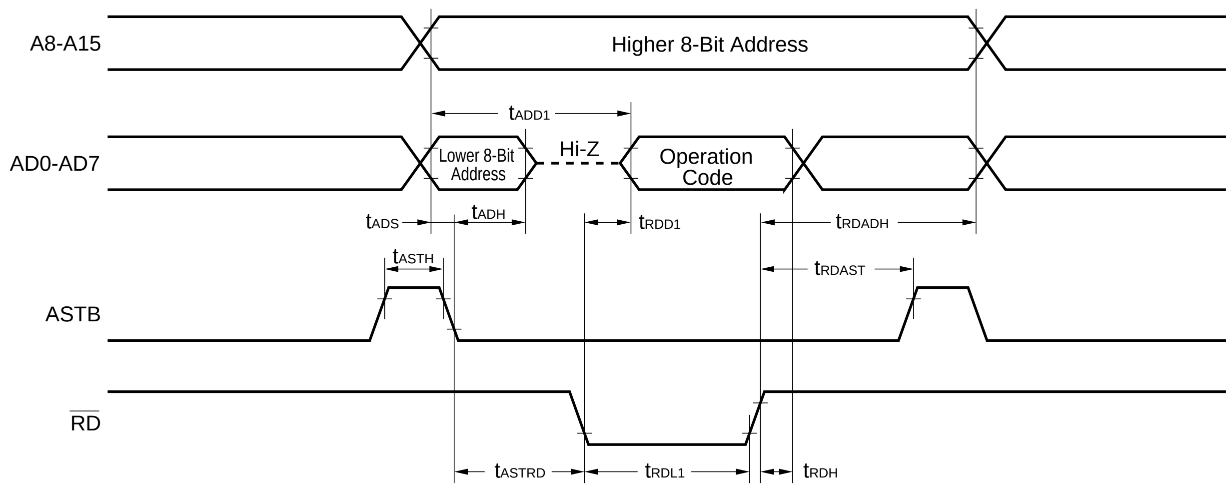


TI Timing

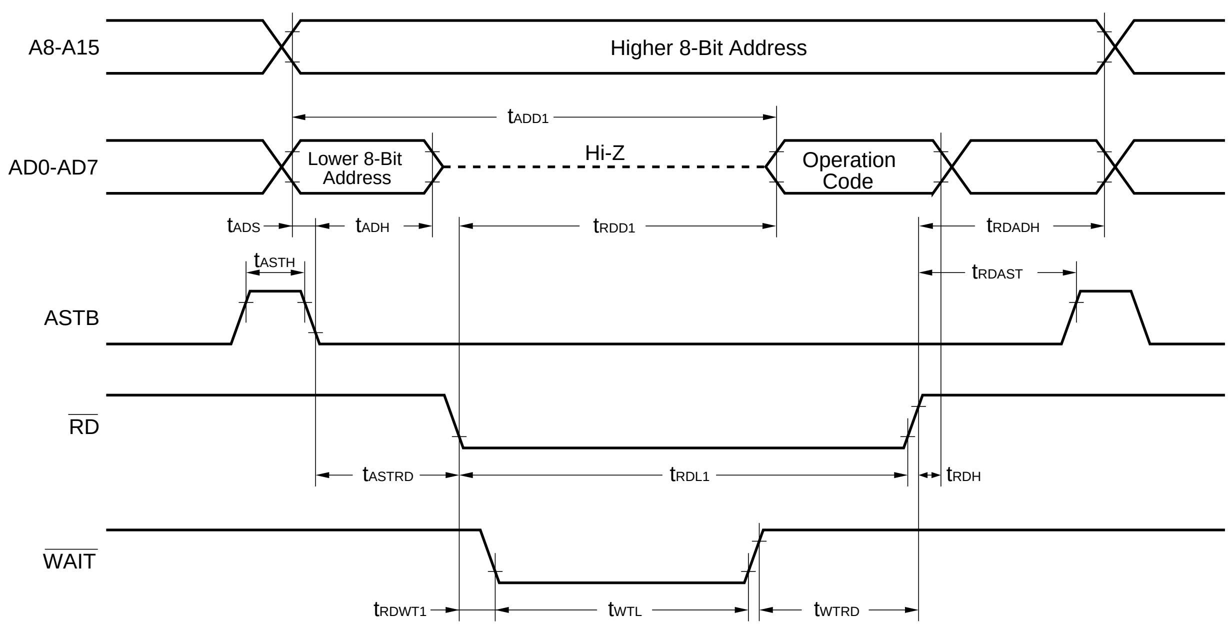


Read/Write Operation

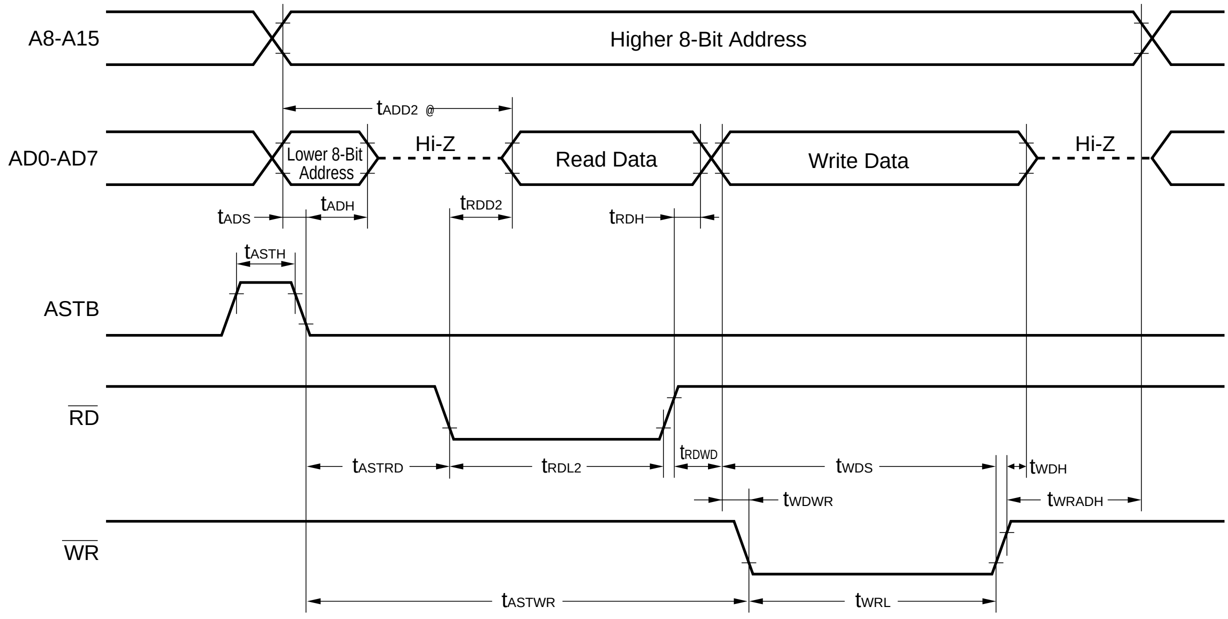
External fetch (no wait):



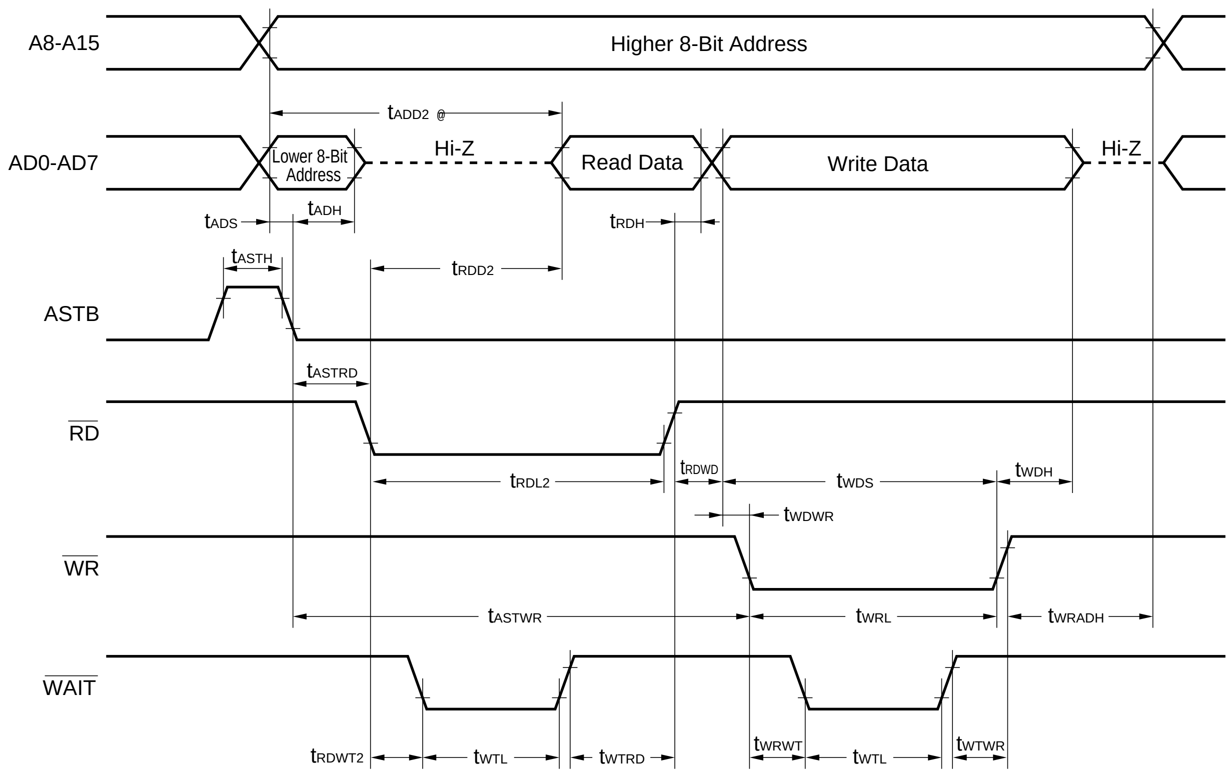
External fetch (wait insertion):



External data access (No wait):

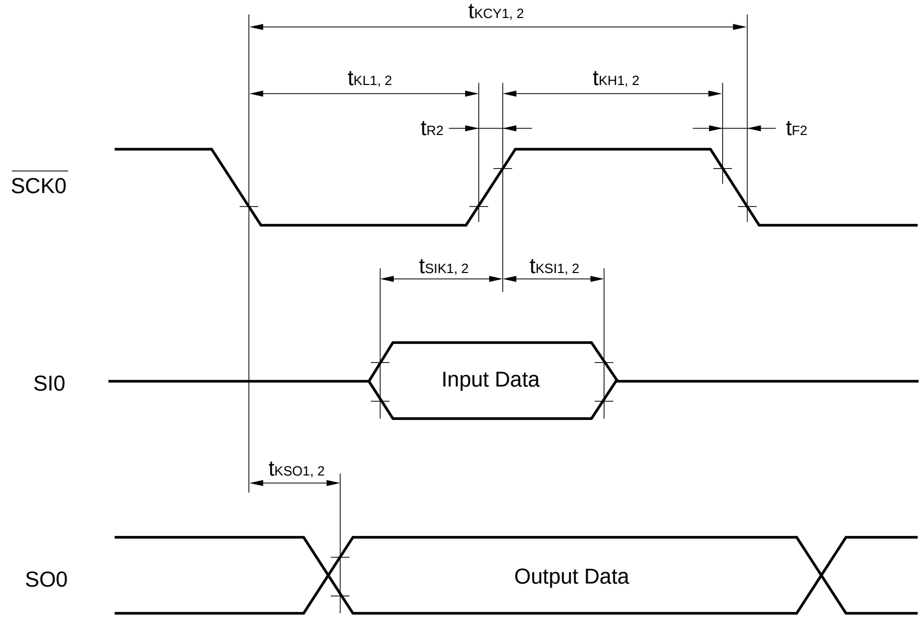


External data access (Wait insertion):

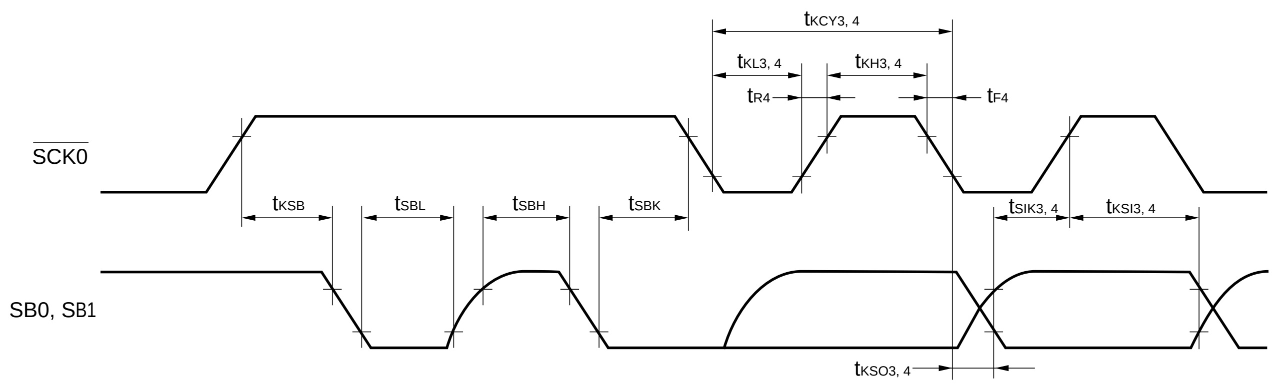


Serial Transfer Timing

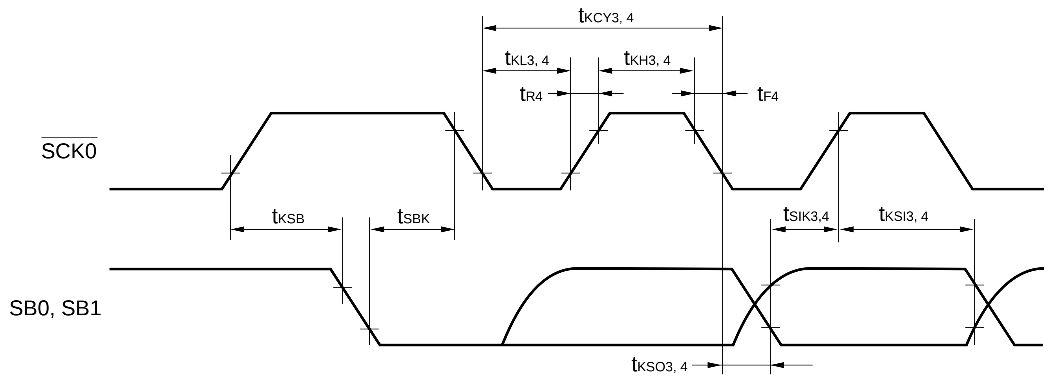
3-wire serial I/O mode:



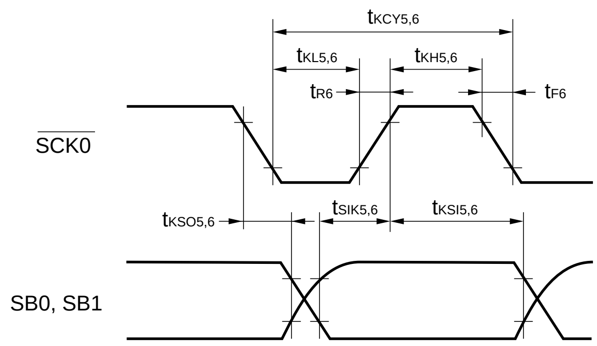
SBI mode (Bus release signal transfer):



SBI mode (Command signal transfer):



2-wire serial I/O mode:

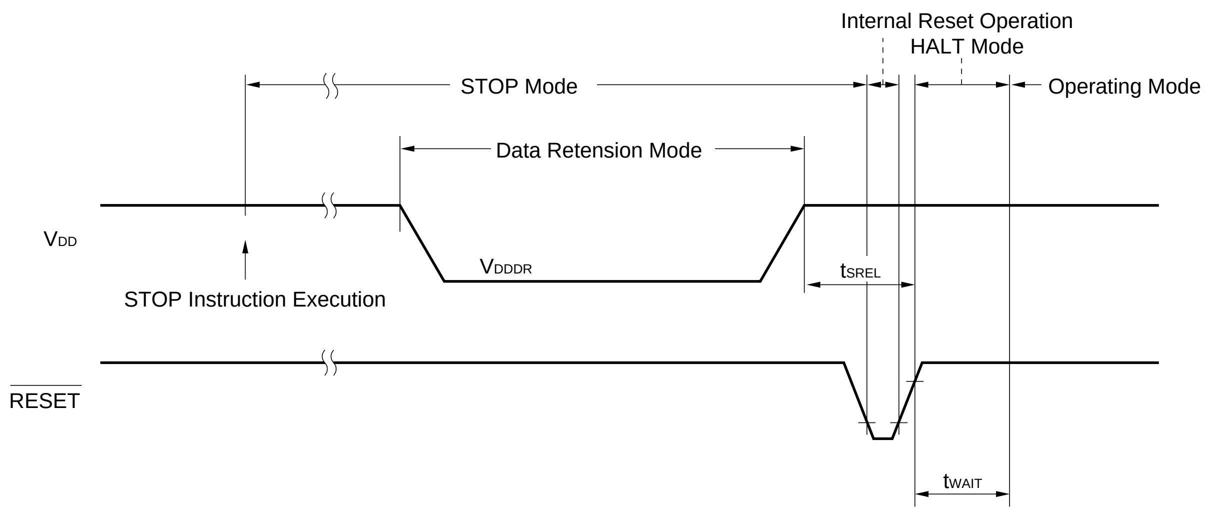


Data Memory Stop Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85 °C)

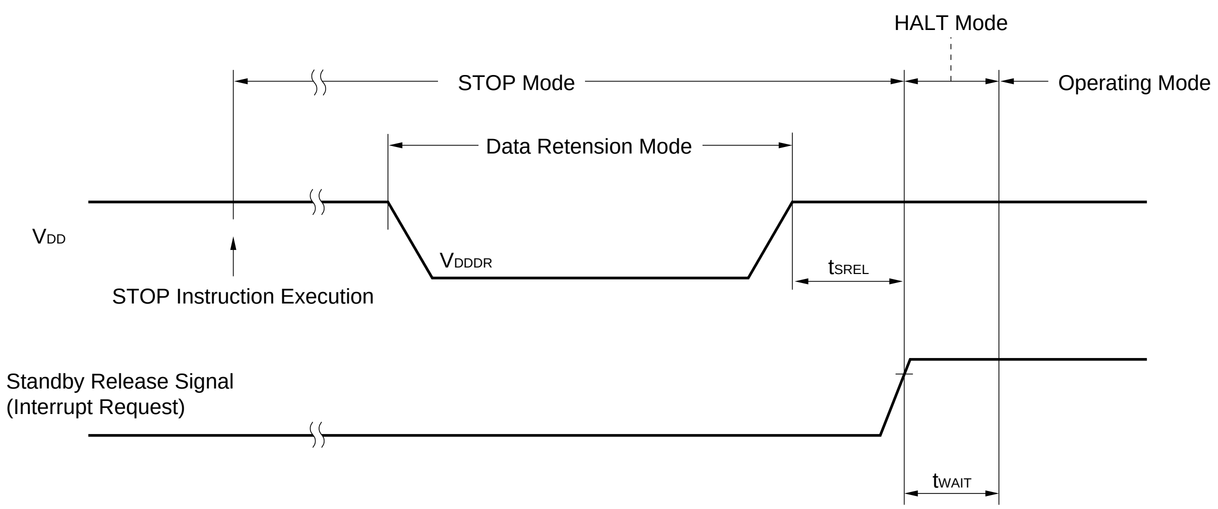
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		2.0		6.0	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 2.0 V Subsystem clock stop and feed-back resistor disconnected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{18}/f_X$		ms
		Release by interrupt		**Note**		ms

Note In combination with bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register (OSTS), selection of $2^{13}/f_X$ and $2^{15}/f_X$ to $2^{18}/f_X$ is possible.

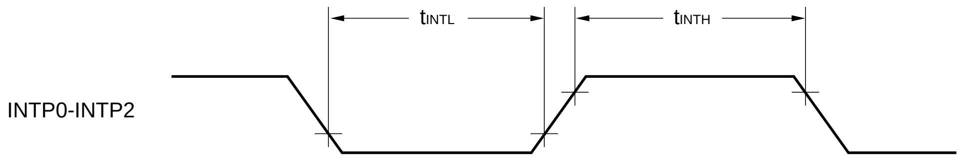
Data Retention Timing (STOP Mode Release by $\overline{RESET}$)

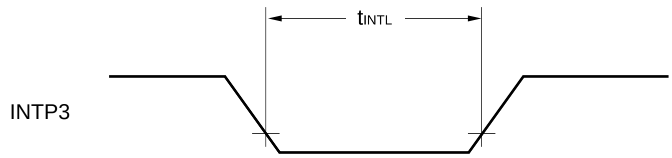


Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)

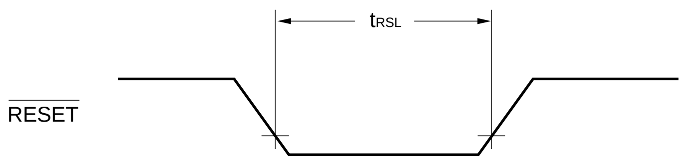


Interrupt Input Timing



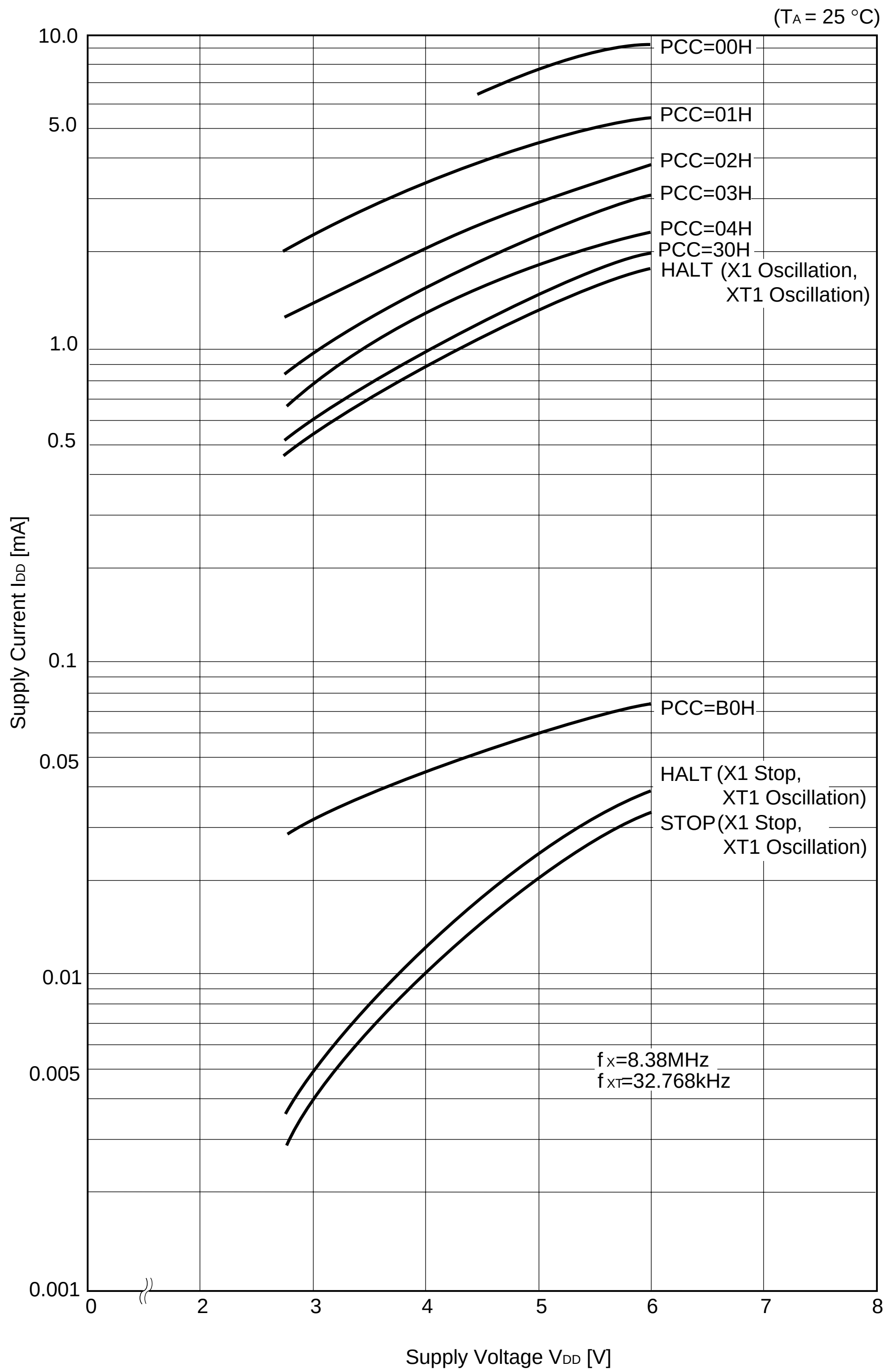


$\overline{\text{RESET}}$ Input Timing

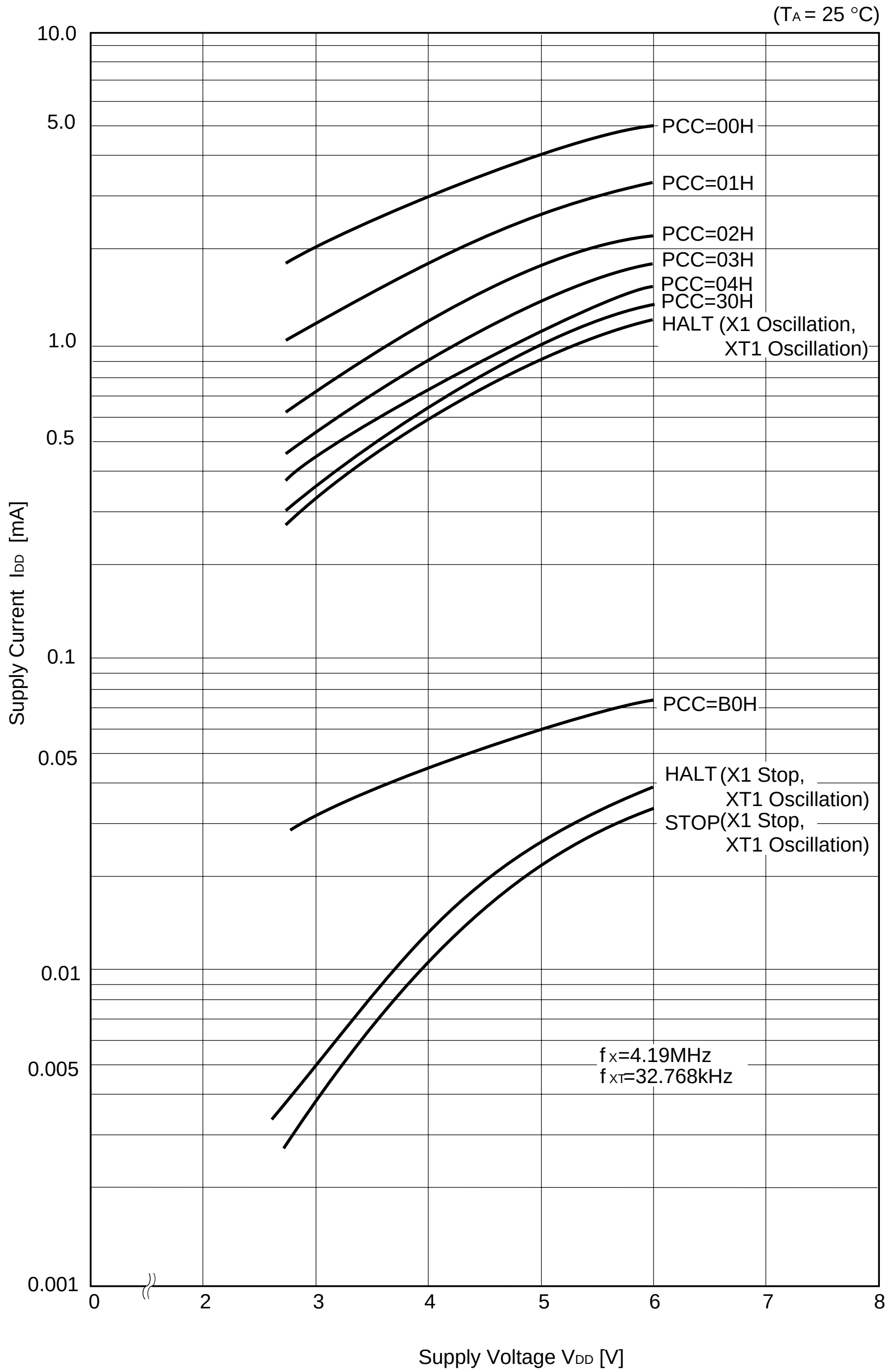


12. CHARACTERISTIC CURVE (REFERENCE VALUES)

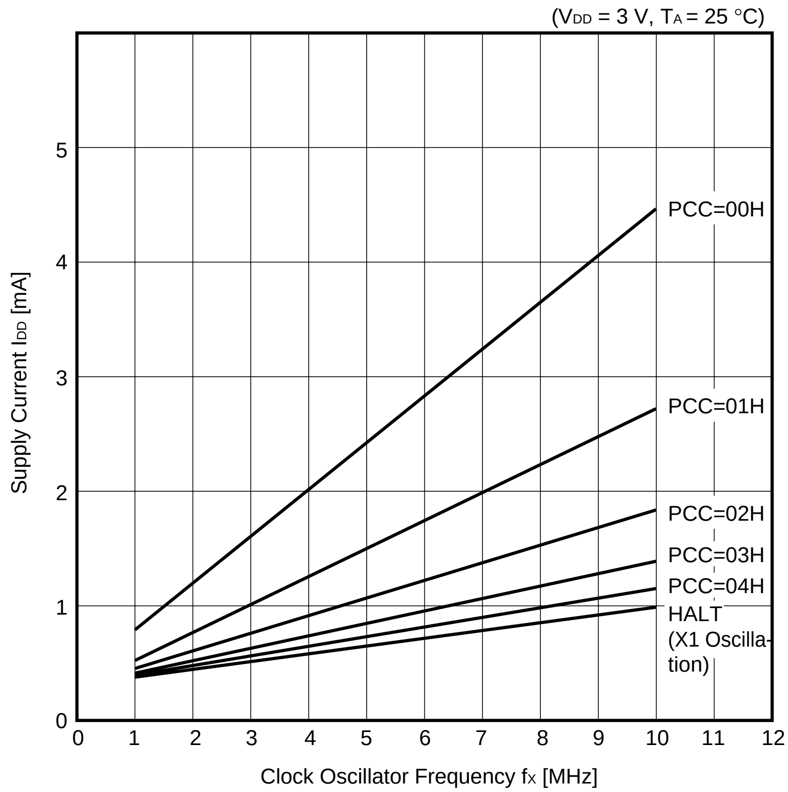
I_{DD} vs V_{DD} (Main System Clock : 8.38 MHz)



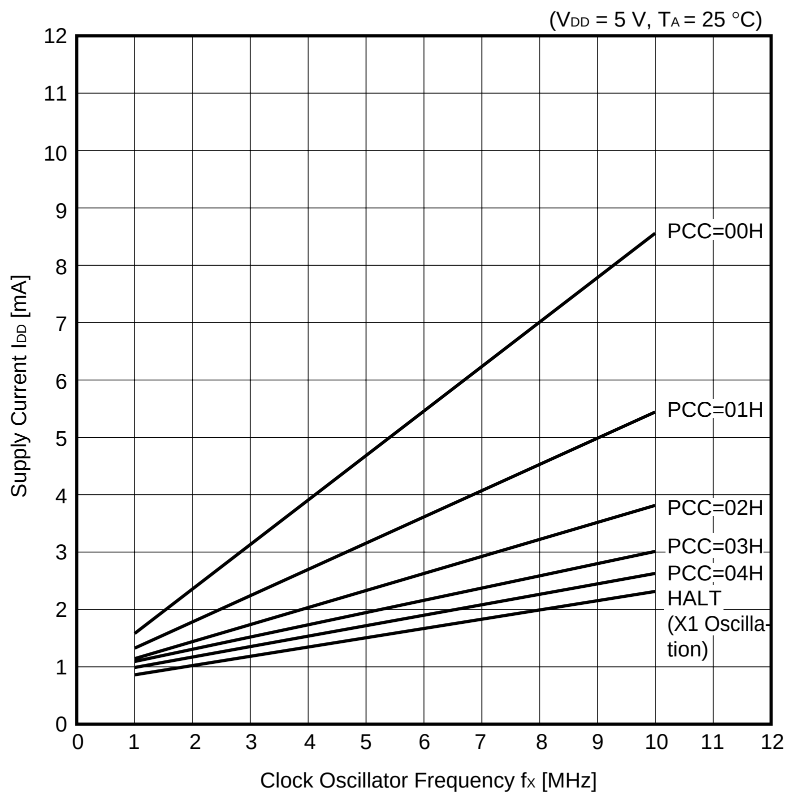
I_{DD} vs V_{DD} (Main System Clock : 4.19 MHz)



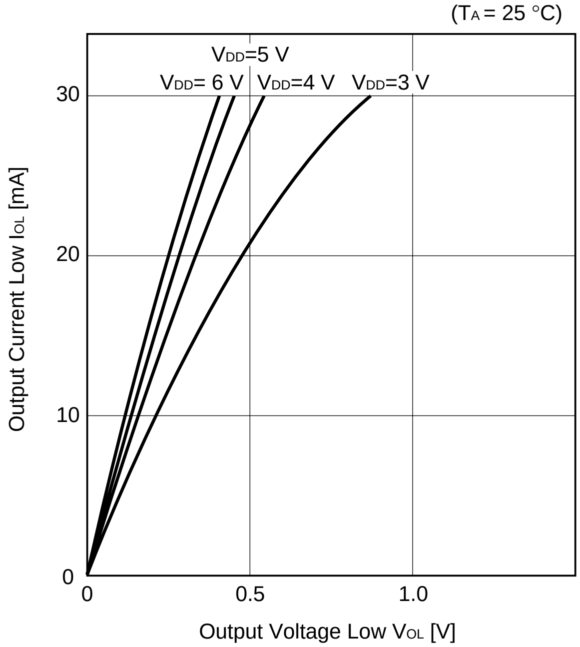
I_{DD} vs f_X



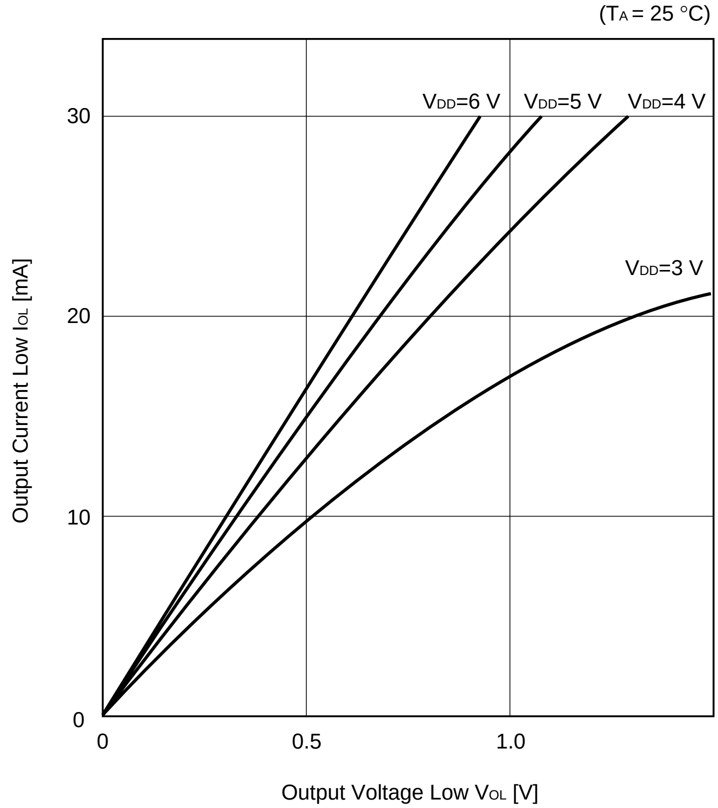
I_{DD} vs f_X



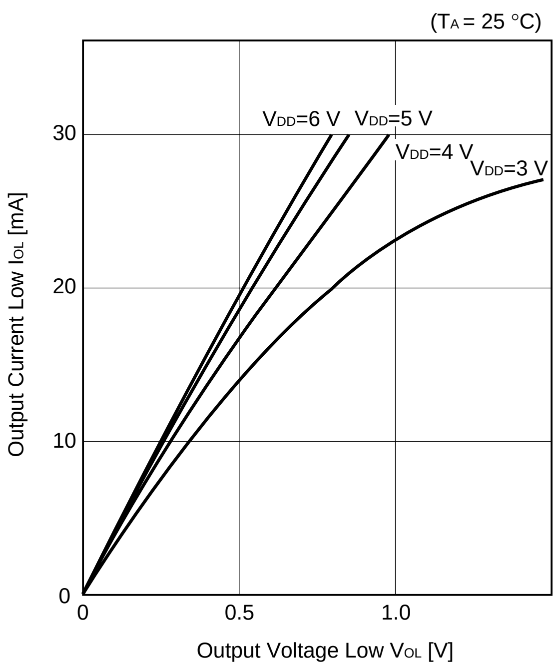
V_{OL} vs I_{OL} (Port 0, 2 to 5, P64 to P67)



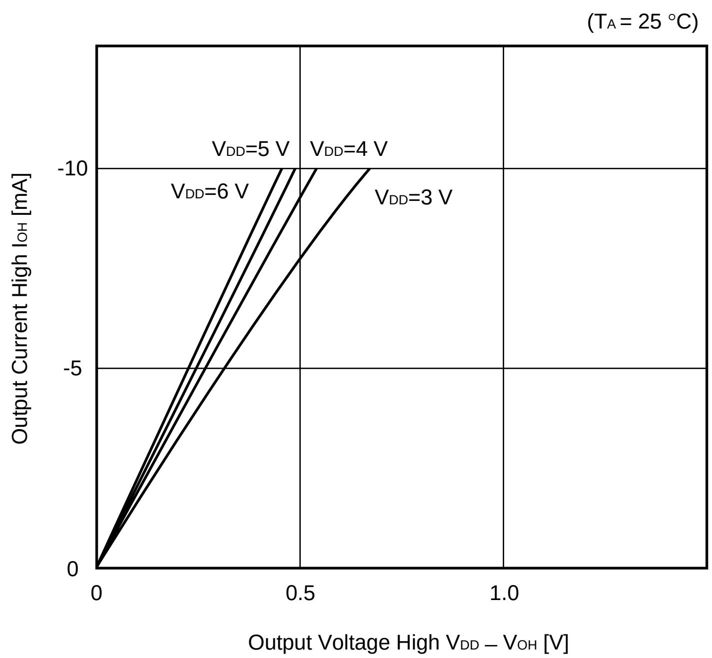
V_{OL} vs I_{OL} (P60 to P63)



V_{OL} vs I_{OL} (Port 1)



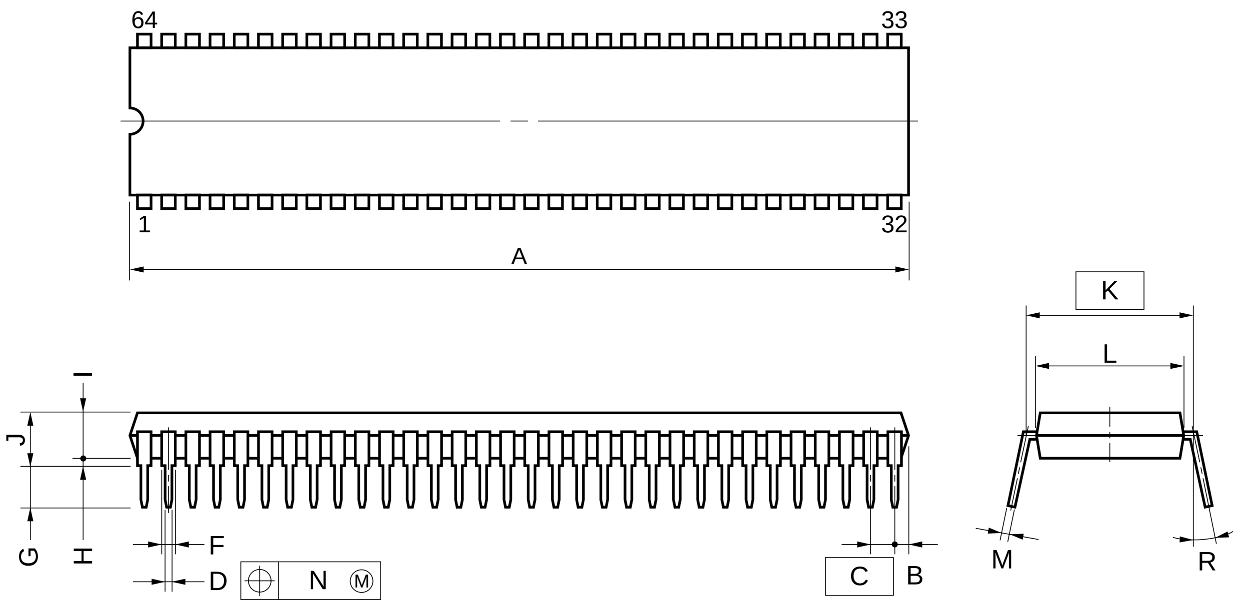
V_{OH} vs I_{OH} (Port 0 to 5, P64 to P67)



13. PACKAGE DRAWINGS

DRAWINGS OF MASS-PRODUCTION PRODUCT PACKAGES (1/2)

64-PIN PLASTIC SHRINK DIP (750 mil)



NOTE

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

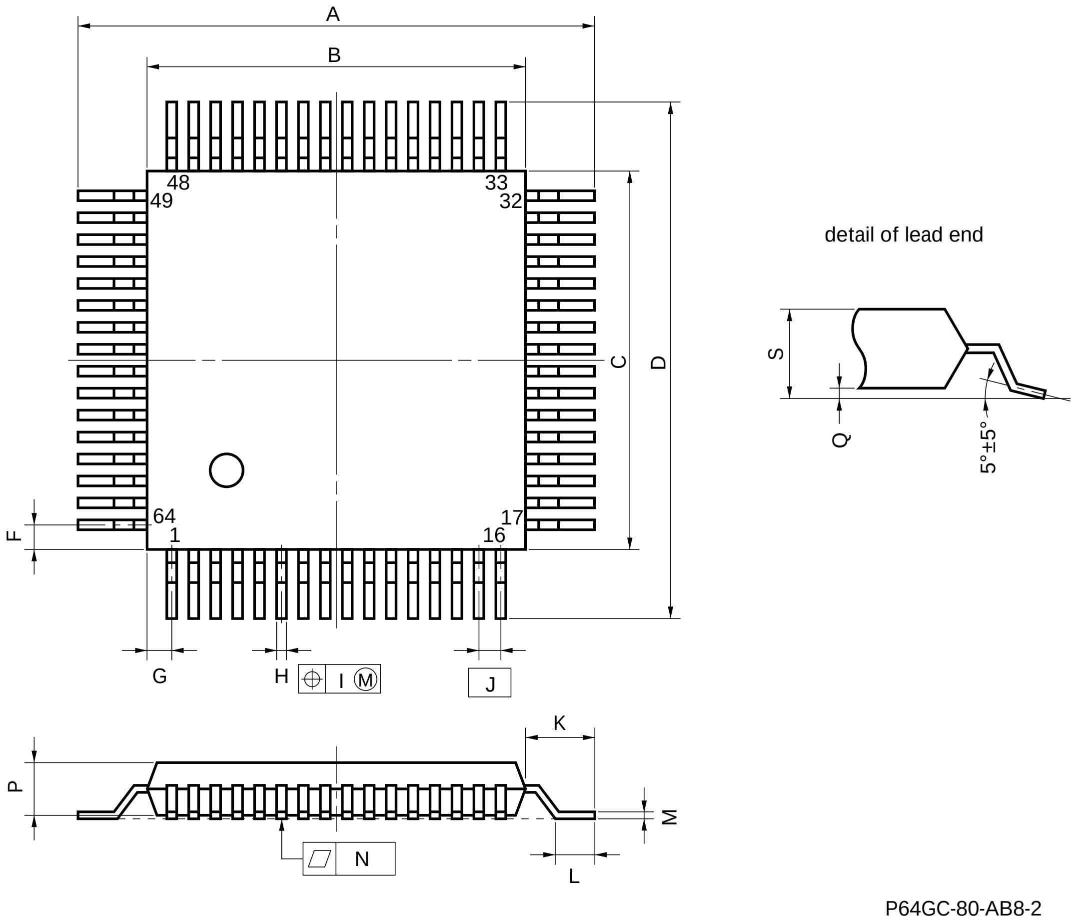
ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

Caution Dimensions and materials of ES products are different from those of mass-production products. Refer to DRAWINGS OF ES PRODUCT PACKAGES (1/2).

DRAWINGS OF MASS-PRODUCTION PRODUCT PACKAGES (2/2)

64-PIN PLASTIC QFP (□14)



NOTE

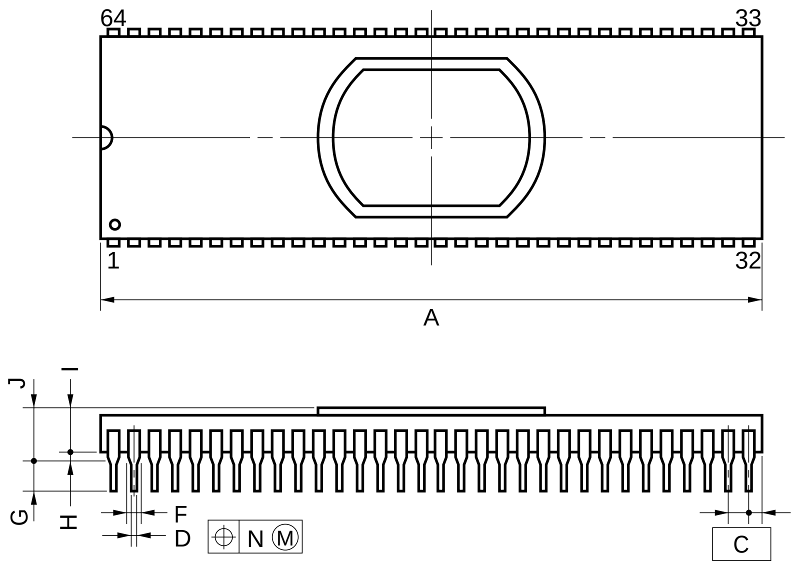
Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

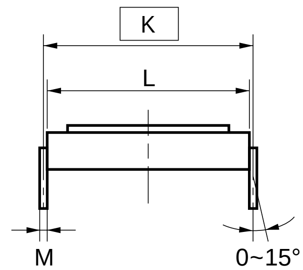
ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

Caution Dimensions and materials are different from those of mass-production products. Refer to DRAWINGS OF ES PRODUCT PACKAGES (2/2).

DRAWINGS OF ES PRODUCT PACKAGES (1/2)

64PIN CERAMIC SHRINK DIP (SEAM WELD) (750 mil)





P64D-70-750A1

NOTES

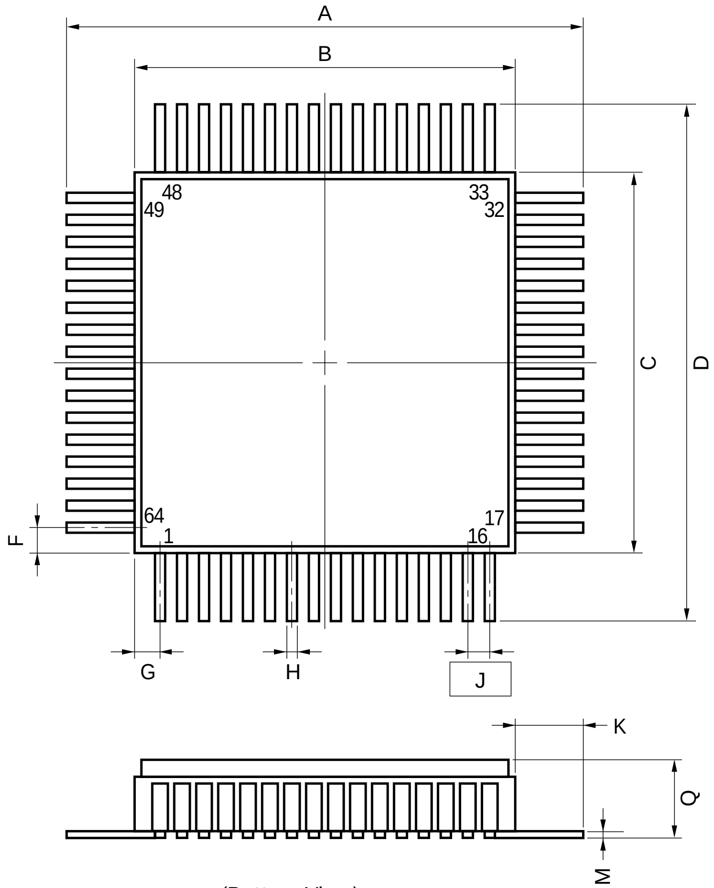
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

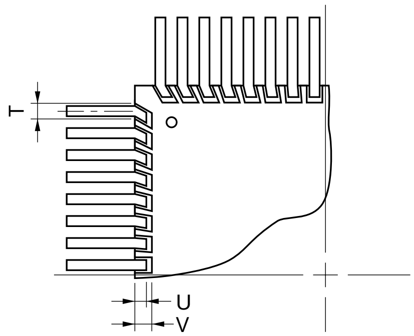
ITEM	MILLIMETERS	INCHES
A	58.16 MAX.	2.290 MAX.
B	1.521 MAX.	0.060 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.46±0.05	0.018±0.002
F	0.8 MIN.	0.031 MIN.
G	3.5±0.3	0.138±0.012
H	1.02 MIN.	0.040 MIN.
I	3.14	0.124
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	18.8	0.740
M	0.25±0.05	$0.010^{+0.002}_{-0.003}$
N	0.25	0.01

DRAWINGS OF ES PRODUCT PACKAGES (2/2)

64 PIN CERAMIC QFP (14 × 14) (FOR ES)



(Bottom View)



X64B-80A-1

ITEM	MILLIMETERS	INCHES
A	22.0±0.4	0.866±0.016
B	14.0	0.551
C	14.0	0.551
D	22.0±0.4	0.866±0.016
F	1.0	0.039
G	1.0	0.039
H	0.32	0.013
J	0.8 (T.P.)	0.031 (T.P.)
K	4.0±0.15	$0.157^{+0.007}_{-0.006}$
M	0.25	0.01
Q	3.0 MAX.	0.119 MAX.
T	0.55	0.022
U	1.0	0.039
V	1.2	0.047

14. RECOMMENDED SOLDERING CONDITIONS

The μPD78001B/78002B should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **“Semiconductor Device Mounting Technology Manual” (IEI-1207)**.

For soldering methods and conditions other than those recommended below, contact our sales personnel.

Table 14-1. Surface Mounting Type Soldering Conditions

μPD78001BGC-×××-AB8 : 64-Pin Plastic QFP (14 × 14 mm)
μPD78002BGC-×××-AB8 : 64-Pin Plastic QFP (14 × 14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Duration: 30 sec. max. (at 210°C or above), Number of times: Twice max. < Points to note > (1) Start the second reflow after the device temprature by the first reflow returns to normal. (2) Flux washing by the water after the first reflow should be avoided.	IR35-00-2
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above) Number of times: Twice max. < Points to note > (1) Start the second reflow after the device temprature by the first reflow returns to normal. (2) Flux washing by the water after the first reflow should be avoided.	VP15-00-2
Pin part heating	Pin temperature: 300°C max., Duration: 3 sec. max. (per device side)	—

Caution Use of more than one soldering method should be avoided (except in the case of pin part heating).

Table 14-2. Insertion Type Soldering Conditions

μPD78001BCW-××× : 64-Pin Plastic Shrink DIP (750 mil)
μPD78002BCW-××× : 64-Pin Plastic Shrink DIP (750 mil)

Soldering Method	Soldering Conditions
Wave soldering (Pin only)	Solder bath temperature: 260°C max., Duration: 10 sec. max.
Pin part heating	Pin temperature: 300°C max., Duration: 3 sec. max. (per pin)

Caution Wave soldering is only for the pins in order that jet solder can not contact with the chip directly.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78001B, 78002B.

Language Processing Software

RA78K/0 Note 1, 2, 3	78K/0 series common assembler package
CC78K/0 Note 1, 2, 3	78K/0 series common C compiler package
DF78002 Note 1, 2, 3	μPD78002 subseries device file
CC78K/0-L Note 1, 2, 3	78K/0 series common C compiler library source file

PROM Programming Tools

PG-1500	PROM programmer
PA-78P014CW PA-78P014GC	Programmer adapter connected to PG-1500
PG-1500 controller Note 1, 2	PG-1500 control program

Debugging Tools

IE-78000-R	78K/0 series common in-circuit emulator
IE-78000-R-BK	78K/0 series common break board
IE-78014-R-EM	μPD78002/78014 subseries evaluation emulation board (V_{DD} = 5.0 V)
IE-78014-R-EM-A	μPD78002, 78014, 78018F subseries evaluation emulation board (V_{DD} = 3.0 to 6.0) ★
EP-78240CW-R EP-78240GC-R	Emulation probe common to μPD78244 subseries
EV-9200GC-64	Socket to be mounted on user system board created for the 64-pin plastic QFP
SM78K/0 Note 4, 5	78K/0 series common system simulator
SD78K/0 Note 1, 2	IE-78000-R screen debugger
DF78002 Note 1, 2, 4, 5	μPD78002 subseries device file

Real-time OS

MX78K0 Note 1, 2, 3	78K/0 series OS ★

Fuzzy Inference Development Support System

FE9000 Note 1/FE9200 Note 5	Fuzzy knowledge data creation tool
FT9080 Note 1/FT9085 Note 2	Translator
FI78K0 Note 1, 2	Fuzzy inference module
FD78K0 Note 1, 2	Fuzzy inference debugger

Notes 1. PC-9800 series (MS-DOS™) based.

2. IBM PC/AT™ (PC DOS™) based.

3. HP9000 series 300™, HP9000 series 700™ (HP-UX™) based, SPARCstation™, (SunOS™) based, EWS-4800 series (EWS-UX/V) based.

4. PC-9800 series (MS-DOS + Windows™) based.

5. IBM PC/AT (PC DOS + Windows) based.

Remarks 1. For development tools manufactured by a third party, see **78K/0 Series Selection Guide (IF-1185)**.

2. RA78K/0, CC78K/0, SM78K0, and SD78K/0 are used in combination with DF78002.

APPENDIX B. RELATED DOCUMENTS ★

Device Related Documents

Document Name		Document No.	
		Japanese	Engligh
μPD78002, 78002Y Subseries User's Manual		U10039J	IEU-1334
78K/0 Series User's Manual - Instruction		IEU-849	IEU-1372
78K/0 Series Instruction List		IEM-5522	—
78K/0 Series Instruction Set		IEM-5521	—
μPD78002, 78002Y Subseries Special Function Register List		IEM-5547	—
78K/0 Series Application Note	Fundamental (I)	IEA-715	IEA-1288

Development Tools Documents (User's Manual)

Document Name		Document No.	
		Japanese	Engligh
RA78K Series Assembler Package	Operation	EEU-809	EEU-1399
	Language	EEU-815	EEU-1404
RA78K Series Structured Assembler Preprocessor		EEU-817	EEU-1402
CC78K Series C Compiler	Operation	EEU-656	EEU-1280
	Language	EEU-655	EEU-1284
CC78K/0 C Compiler Application Note	Programming Know-how	EEA-618	EEA-1208
CC78K Series Library Source File		EEU-777	—
PG-1500 PROM Programmer		EEU-651	EEU-1335
PG-1500 Controller PC-9800 Series (MS-DOS) Base		EEU-704	Planned to publish
PG-1500 Controller IBM PC Series (PC DOS) Base		EEU-5008	EEU-1291
IE-78000-R		EEU-810	EEU-1398
IE-78000-R-BK		EEU-867	EEU-1427
IE-78014-R-EM		EEU-805	EEU-1400
IE-78014-R-EM-A		EEU-962	EEU-1487
EP-78240		EEU-986	EEU-1513
SM78K0 System Simulator	Reference	EEU-5002	U10181E
SM78K Series System Simulator	External Parts User-open Interface Specification	U10092J	U10092E
SD78K/0 Screen Debugger PC-9800 Series (MS-DOS) Base	Introduction	EEU-852	—
	Reference	EEU-816	—
SD78K/0 Screen Debugger IBM PC/AT (PC DOS) Base	Introduction	EEU-5024	EEU-1414
	Reference	EEU-993	EEU-1413

Embedded Software Documents (User's Manual)

Document Name		Document No.	
		Japanese	Engligh
78K/0 Series OS MX78K0	Fundamental	EEU-5010	—
Fuzzy Knowledge Data Creation Tool		EEU-829	EEU-1438
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System - Translator		EEU-862	EEU-1444
78K/0 Series Fuzzy Inference Development Support System - Fuzzy Inference Module		EEU-858	EEU-1441
78K/0 Series Fuzzy Inference Development Support System - Fuzzy Inference Debugger		EEU-921	EEU-1458

Caution The contents of the above related documents are subject to change without notice. The latest documents should be used for design, etc.

Other Documents

Document Name	Document No.	
	Japanese	Engligh
Package Manual	IEI-635	IEI-1213
Semiconductor Device Mounting Technology Manual	IEI-616	IEI-1207
Quality Grades on NEC Semiconductor Device	IEI-620	IEI-1209
NEC Semiconductor Device Reliability/Quality Control System	IEM-5068	—
Electrostatic Discharge (ESD) Test	MEM-539	—
Guide to Quality Assurance for Semiconductor Device	MEI-603	MEI-1202
Guide for Products Related to Micro-Computer: Other Companies	MEI-604	—

Caution The contents of the above related documents are subject to change without notice. The latest documents should be used for design, etc.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]