NEC

MOS INTEGRATED CIRCUIT

μPD75P3216

4-BIT SINGLE-CHIP MICROCONTROLLER

The μPD75P3216 replaces the μPD753208's internal mask ROM with a one-time PROM, and features expanded ROM capacity.

Because the μPD75P3216 supports programming by users, it is suitable for use in prototype testing for system development using the μPD753204, 753206, or 753208, and for use in small-lot production.

The functions are explained in detail in the following user's manual. Be sure to read this manual when designing your system.

μPD753208 User's Manual: U10158E

FEATURES

- Compatible with μPD753208
- Memory capacity:
  - PROM : 16384 × 8 bits
  - RAM : 512 × 4 bits
- Can operate in same power supply voltage range as the mask version μPD753208
  - V_{DD} = 1.8 to 5.5 V
- LCD controller/driver

ORDERING INFORMATION

Part Number	Package
μPD75P3216GT	48-pin plastic shrink SOP (375 mil, 0.65-mm pitch)

Caution Mask-option pull-up resistors are not provided in this device.

The information in this document is subject to change without notice.

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The mark ★ shows major revised points.

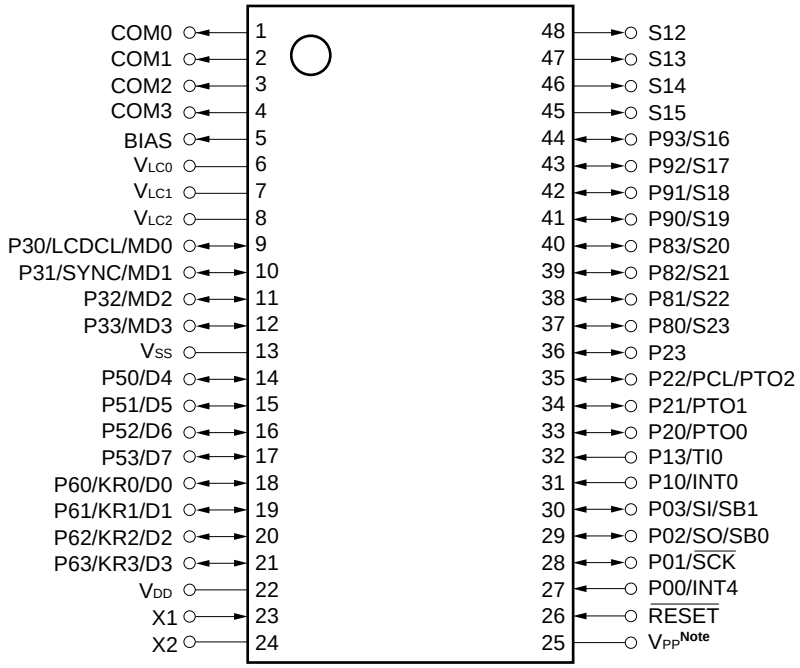
FUNCTION OUTLINE

Parameter		Function	
Instruction execution time		• 0.95, 1.91, 3.81, 15.3 μs (@ 4.19-MHz operation with system clock) • 0.67, 1.33, 2.67, 10.7 μs (@ 6.0-MHz operation with system clock)	
Internal memory	PROM	16384 × 8 bits	
	RAM	512 × 4 bits	
General-purpose register		• 4-bit operation: 8 × 4 banks • 8-bit operation: 4 × 4 banks	
Input/ output port	CMOS input	6	Connecting on-chip pull-up resistors can be specified by software: 5
	CMOS input/output	20	Connecting on-chip pull-up resistors can be specified by software: 20 Also used for segment pins: 8
★	N-ch open-drain I/O	4	13-V withstand
	Total	30	
LCD controller/driver		• Segment selection: 4/8/12 segments (can be changed to CMOS input/ output port in 4-time units; max. 8) • Display mode selection: Static 1/2 duty (1/2 bias) 1/3 duty (1/2 bias) 1/3 duty (1/3 bias) 1/4 duty (1/3 bias)	
Timer		5 channels • 8-bit timer/event counter: 1 channel • 8-bit timer counter: 2 channels (can be used as the 16-bit timer counter, carrier generator, timer with gate) • Basic interval timer/watchdog timer: 1 channel • Watch timer: 1 channel	
Serial interface		• 3-wire serial I/O mode ... MSB or LSB can be selected for transferring first bit • 2-wire serial I/O mode • SBI mode	
Bit sequential buffer (BSB)		16 bits	
Clock output (PCL)		• Φ, 524, 262, 65.5 kHz (@ 4.19-MHz operation with system clock) • Φ, 750, 375, 93.8 kHz (@ 6.0-MHz operation with system clock)	
Buzzer output (BUZ)		• 2, 4, 32 kHz (@ 4.19-MHz operation with system clock) • 2.93, 5.86, 46.9 kHz (@ 6.0-MHz with system clock)	
Vectored interrupts		External: 2, Internal: 5	
Test input		External: 1, Internal: 1	
System clock oscillator		Ceramic or crystal oscillator for system clock oscillation	
Standby function		STOP/HALT mode	
Power supply voltage		V_{DD} = 1.8 to 5.5 V	
Package		48-pin plastic shrink SOP (375 mil, 0.65-mm pitch)	

CONTENTS

1. PIN CONFIGURATION (Top View)

- **48-pin plastic shrink SOP (375 mil, 0.65-mm pitch)**
  μPD75P3216GT

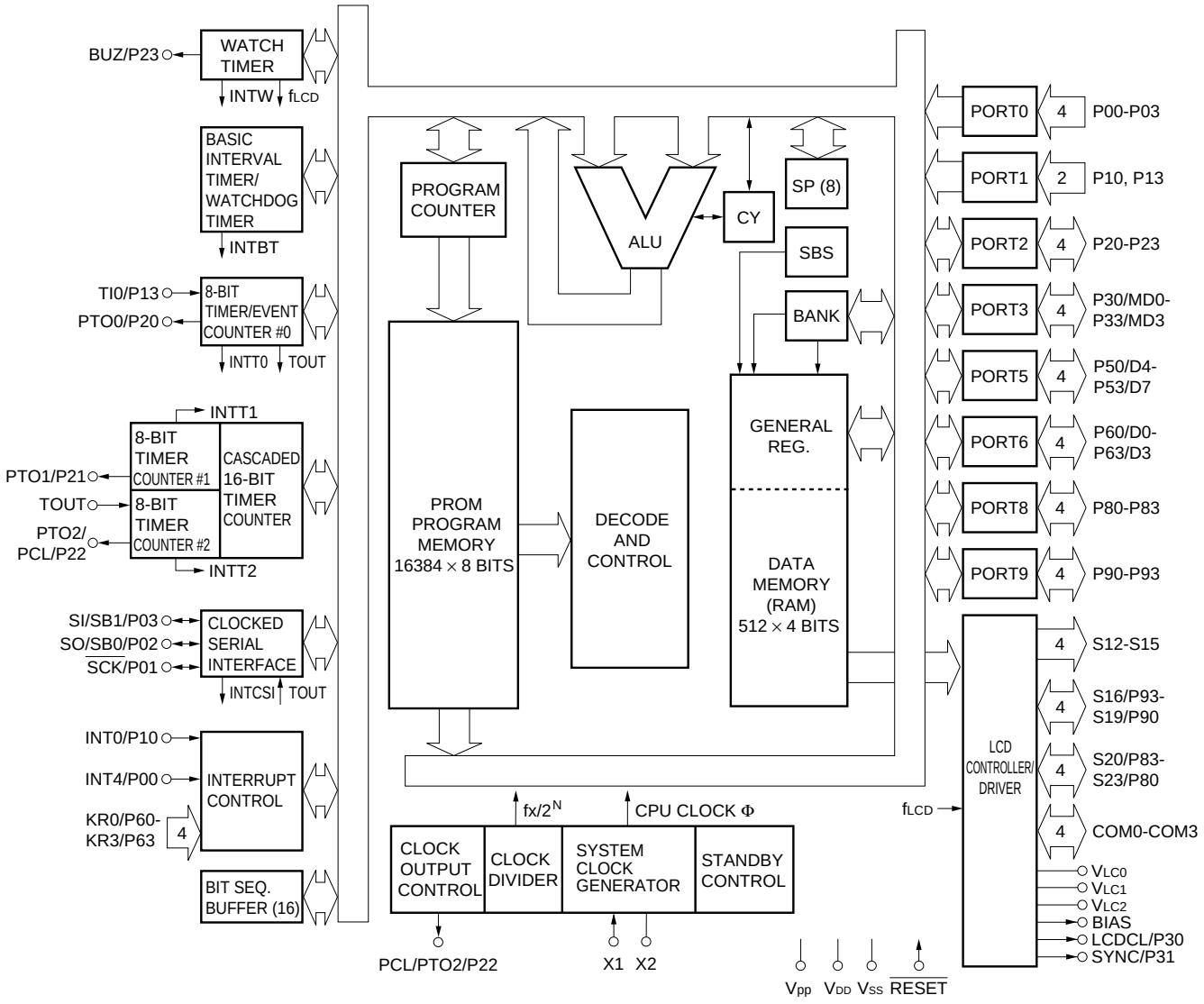


Note Be sure to connect V_{PP} to V_{DD} directly in normal operation mode.

PIN IDENTIFICATIONS

BIAS	:	LCD Power Supply Bias Control
BUZ	:	Buzzer Clock
COM0-COM3	:	Common Output 0 to 3
D0-D7	:	Data Bus 0 to 7
INT0, INT4	:	External Vectored Interrupt 0, 4
KR0-KR3	:	Key Return 0 to 3
LCDCL	:	LCD Clock
MD0-MD3	:	Mode Selection 0 to 3
P00-P03	:	Port0
P10, P13	:	Port1
P20-P23	:	Port2
P30-P33	:	Port3
P50-P53	:	Port5
P60-P63	:	Port6
P80-P83	:	Port8
P90-P93	:	Port9
PCL	:	Programmable Clock
PTO0-PTO2	:	Programmable Timer Output 0 to 2
$\overline{\text{RESET}}$	:	Reset Input
S12-S23	:	Segment Output 12 to 23
SB0, SB1	:	Serial Bus 0, 1
$\overline{\text{SCK}}$	:	Serial Clock
SI	:	Serial Input
SO	:	Serial Output
SYNC	:	LCD Synchronization
TI0	:	Timer Input 0
V_{DD}	:	Positive Power Supply
V_{LC0}-V_{LC2}	:	LCD Power Supply 0 to 2
V_{PP}	:	Programming Power Supply
V_{SS}	:	Ground
X1, X2	:	System Clock Oscillation 1, 2

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins

	Pin Name	I/O	Shared by	Function	8-bit I/O	Status After Reset	I/O Circuit Type[Note 1]
	P00	Input	INT4	This is a 4-bit input port (PORT0). P01 to P03 are 3-bit pins for which an internal pull-up resistor can be connected by software.	×	Input	<B>
	P01	I/O	$\overline{SCK}$				<F>-A
	P02	I/O	SO/SB0				<F>-B
	P03	I/O	SI/SB1				<M>-C
	P10	Input	INT0	This is a 1-bit input port (PORT1). These are 1-bit pins for which an internal pull-up resistor can be connected by software. P10/INT0 can select noise elimination circuit.	×	Input	<B>-C
	P13		TI0				
	P20	I/O	PTO0	This is a 4-bit I/O port (PORT2). These are 4-bit pins for which an internal pull-up resistor can be connected by software.	×	Input	E-B
	P21		PTO1				
	P22		PCL/PTO2				
	P23		BUZ				
	P30	I/O	LCDCL/MD0	This is a programmable 4-bit I/O port (PORT3). Input and output in single-bit units can be specified. When set for 4-bit units, an internal pull-up resistor can be connected by software.	×	Input	E-B
	P31		SYNC/MD1				
	P32		MD2				
	P33		MD3				
★	P50[Note 2]	I/O	D4	This is an N-ch open-drain 4-bit I/O port (PORT5). When set to open-drain, voltage is 13 V. Also functions as data I/O pin (upper 4 bits) for program memory (PROM) write/verify.	×	High impedance	M-E
	P51[Note 2]		D5				
	P52[Note 2]		D6				
	P53[Note 2]		D7				
★	P60	I/O	KR0/D0	This is a programmable 4-bit I/O port (PORT6). Input and output in single-bit units can be specified. When set for 4-bit units, an internal pull-up resistor can be connected by software. Also functions as data I/O pin (lower 4 bits) for program memory (PROM) write/verify.	×	Input	<F>-A
	P61		KR1/D1				
	P62		KR2/D2				
	P63		KR3/D3				
	P80	I/O	S23	This is a 4-bit I/O port (PORT8). When set for 4-bit units, an internal pull-up resistor can be connected by software.	○	Input	H
	P81		S22				
	P82		S21				
	P83		S20				
	P90	I/O	S19	This is a programmable 4-bit I/O port (PORT9). When set for 4-bit units, an internal pull-up resistor can be connected by software.		Input	H
	P91		S18				
	P92		S17				
	P93		S16				

Notes 1. Circuit types enclosed in brackets indicate Schmitt trigger circuits.

2. Low level input current leakage increases when input instructions or bit manipulation instructions are executed.

3.2 Non-port Pins

Pin Name	I/O	Shared by	Function	Status After Reset	I/O Circuit Type[Note 1]
TI0	Input	P13	External event pulse input to timer/event counter	Input	<B>-C
PTO0	Output	P20	Timer/event counter output	Input	E-B
PTO1		P21	Timer counter output		
PTO2		P22/PCL			
PCL		P22/PTO2	Clock output		
BUZ		P23	Any frequency output (for buzzer or system clock trimming)		
$\overline{SCK}$	I/O	P01	Serial clock I/O	Input	<F>-A
SO/SB0		P02	Serial data output Serial data bus I/O		<F>-B
SI/SB1		P03	Serial data input Serial data bus I/O		<M>-C
INT4	Input	P00	Edge detection vectored interrupt input (detecting both rising and falling edges)	Input	<B>
INT0	Input	P10	Edge detection vectored interrupt input (detected edge is selectable). INT0/P10 can select noise elimination circuit. Noise elimination circuit/asynch is selectable	Input	<B>-C
KR0 to KR3	Input	P60/D0-P63/D3	Falling edge detection testable input	Input	<F>-A
X1	Input	—	Ceramic/crystal oscillation circuit connection for system clock. If using an external clock, input to X1 and input inverted phase to X2.	—	—
X2	—				
$\overline{RESET}$	Input	—	System reset input	—	<B>
MD0 to MD3	Input	P30 to P33	Mode selection for program memory (PROM) write/verify	Input	<F>-A
★ D0 to D3	I/O	P60/KR0-P63/KR3	Data bus pin for program memory (PROM) write/verify.	Input	<F>-A
★ D4 to D7		P50 to P53			M-E
V_{PP}	—	—	Programmable power supply voltage for program memory (PROM) write/verify. For normal operation, connect directly to V_{DD}. Apply +12.5 V for PROM write/verify.	—	—
V_{DD}	—	—	Positive power supply	—	—
V_{SS}	—	—	Ground	—	—
S12 to S15	Output	—	Segment signal output	**Note 2**	G-A
S16 to S19	Output	P93 to P90	Segment signal output	Input	H
S20 to S23		P83 to P80			
COM0 to COM3	Output	—	Common signal output	**Note 2**	G-B
V_{LC0} to V_{LC2}	—	—	Power source for LCD drive	—	—
BIAS	Output	—	Output for external split resistor cut	**Note 3**	—
LCDCL[Note 4]	Output	P30/MD0	Clock output for driving external expansion driver	Input	E-B
SYNC[Note 4]		P31/MD1	Clock output for synchronization of external expansion driver		

Notes 1. Circuit types enclosed in brackets indicate Schmitt trigger circuits.

2. The V_{LCX} (X = 0, 1, 2) shown below are selected as the input source for the display outputs.
S12 to S15: V_{LC1}, COM1 to COM2: V_{LC2}, COM3: V_{LC0}

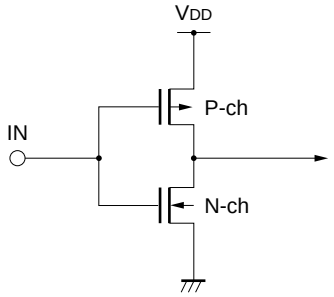
3. When the split resistor is incorporated : Low level
When the split resistor is not incorporated : High impedance

4. These pins are provided for future system expansion. Currently, only P30 and P31 are used.

3.3 Equivalent Circuits for Pins

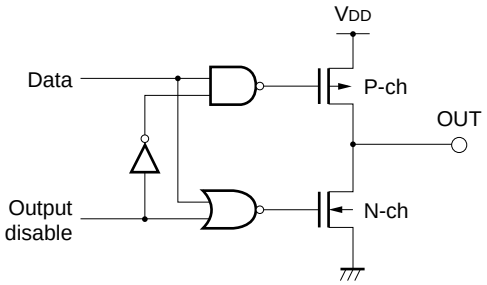
The equivalent circuits for the μPD75P3216's pins are shown in abbreviated form below.

TYPE A



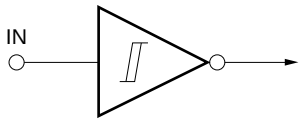
CMOS standard input buffer

TYPE D



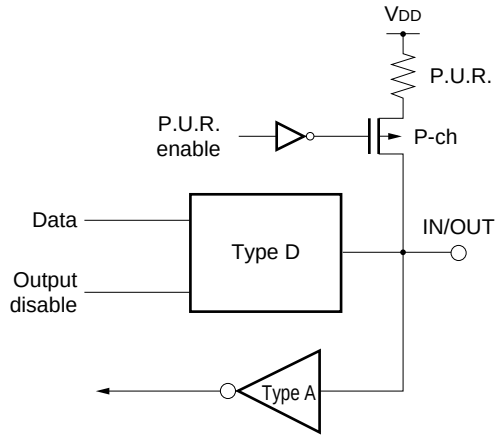
Push-pull output that can be set to high impedance output (with both P-ch and N-ch OFF).

TYPE B



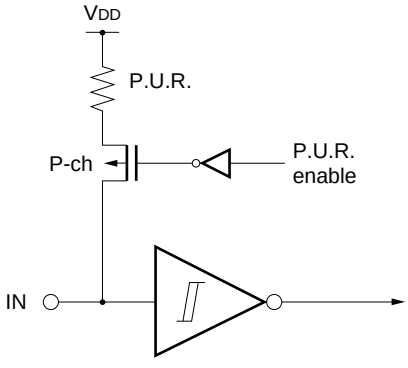
Schmitt trigger input with hysteresis characteristics.

TYPE E-B



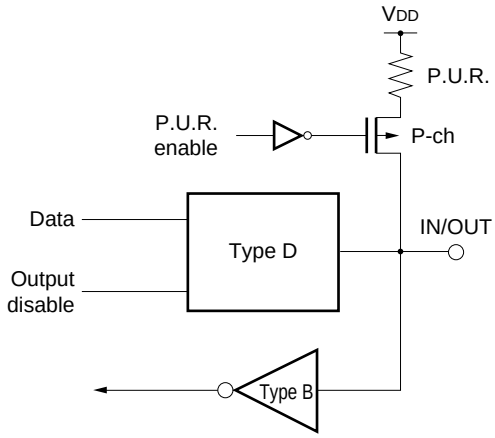
P.U.R. : Pull-Up Resistor

TYPE B-C



P.U.R. : Pull-Up Resistor

TYPE F-A

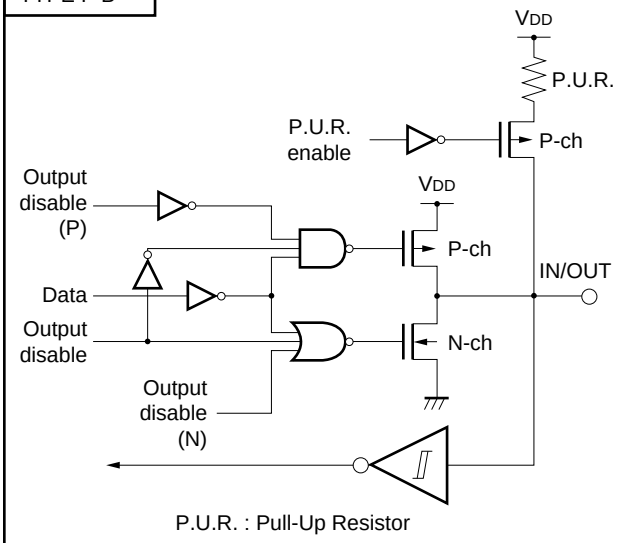


P.U.R. : Pull-Up Resistor

(Continued)

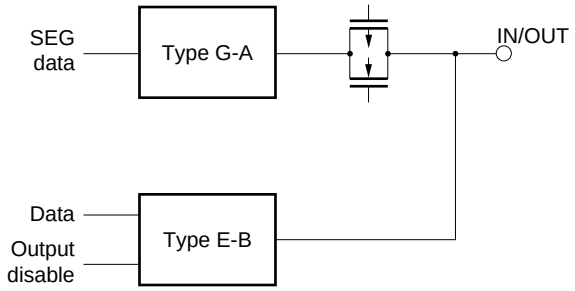
(Continued)

TYPE F-B

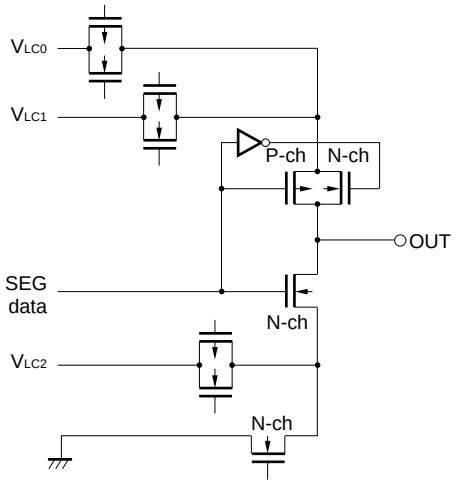


P.U.R. : Pull-Up Resistor

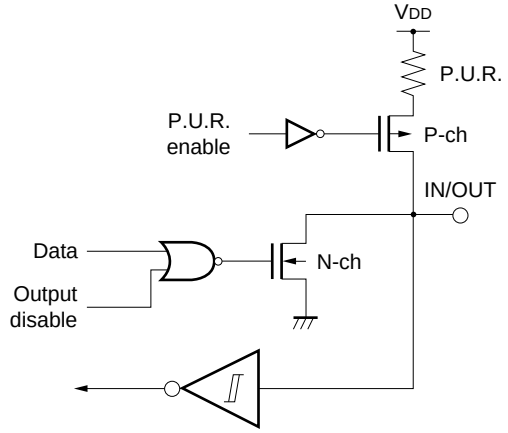
TYPE H



TYPE G-A★

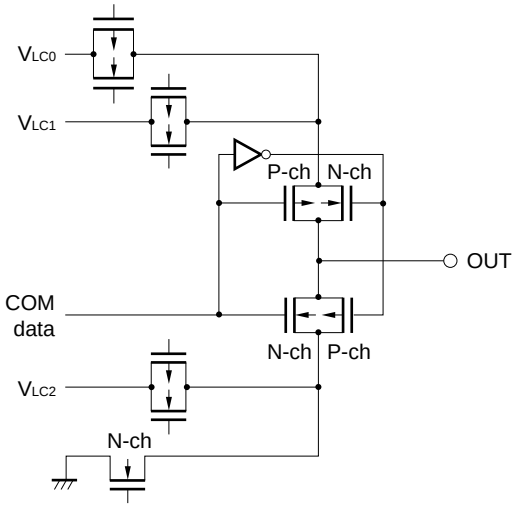


TYPE M-C

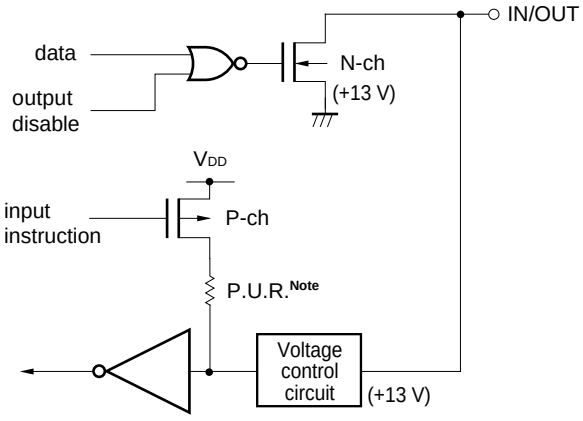


P.U.R. : Pull-Up Resistor

TYPE G-B★



TYPE M-E★



Note This pull-up resistor is effective only when an input instruction is executed (when the pin level is low, current flows from V_{DD} to the pin).

★ 3.4 Recommended Connection of Unused Pins

Pin	Recommended Connection
P00/INT4	Connect to Vss or V_{DD}
P01/$\overline{SCK}$	Connect to Vss or V_{DD} through a resistor individually
P02/SO/SB0	
P03/SI/SB1	Connect to Vss
P10/INT0	Connect to Vss or V_{DD}
P13/TI0	
P20/PTO0	Input status : connect to Vss or V_{DD} through a resistor individually Output status: open
P21/PTO1	
P22/PTO2/PCL	
P23/BUZ	
P30/MD0/LCDCL	
P31/MD1/SYNC	
P32/MD2	
P33/MD3	
P50/D4 to P53/D7	Connect to Vss
P60/KR0/D0 to P63/KR3/D3	Input status : connect to Vss or V_{DD} through a resistor individually Output status: open
S12 to S15	Open
COM0 to COM3	
S16/P93 to S19/P90	Input status : connect to Vss or V_{DD} through a resistor individually Output status: open
S20/P83 to S23/P80	
V_{LC0} to V_{LC2}	Connect to Vss
BIAS	Connect to Vss only when V_{LC0} to V_{LC2} are all not used. In other cases, leave open.
V_{PP}	Be sure to connect V_{DD} directly.

4. Mk I AND Mk II MODE SELECTION FUNCTION

Setting a stack bank selection (SBS) register for the μPD75P3216 enables the program memory to be switched between Mk I mode and Mk II mode. This function is applicable when using the μPD75P3216 to evaluate the μPD753204, 753206, or 753208.

When the SBS bit 3 is set to 1: sets Mk I mode (supports Mk I mode for μPD753204, 753206, and 753208)
When the SBS bit 3 is set to 0: sets Mk II mode (supports Mk II mode for μPD753204, 753206, and 753208)

4.1 Difference between Mk I Mode and Mk II Mode

Table 4-1 lists points of difference between the Mk I mode and the Mk II mode for the μPD75P3216.

Table 4-1. Difference between Mk I Mode and Mk II Mode

Item		Mk I Mode	Mk II Mode
Program counter		PC_{13-0}	
Program memory (bytes)		16384	
Data memory (bits)		512 × 4	
Stack	Stack bank	Selectable via memory banks 0, 1	
	No. of stack bytes	2 bytes	3 bytes
Instruction	BRA !addr1 instruction	None	Provided
	CALLA !addr1 instruction		
Instruction execution time	CALL !addr instruction	3 machine cycles	4 machine cycles
	CALLF !faddr instruction	2 machine cycles	3 machine cycles
Supported mask ROMs		When set to Mk I mode: μPD753204, 753206, and 753208	When set to Mk II mode: μPD753204, 753206, and 753208

★ **Caution The Mk II mode supports a program area which exceeds 16K bytes in the 75X and 75XL series. This mode enhances the software compatibility with products which have more than 16K bytes. When the Mk II mode is selected, the number of stack bytes used in execution of a subroutine call instruction increases by 1 per stack for the usable area compared to the Mk I mode. Furthermore, when a CALL !addr, or CALLF !faddr instruction is used, each instruction takes another machine cycle. Therefore, when more importance is attached to RAM utilization or throughput than software compatibility, use the Mk I mode.**

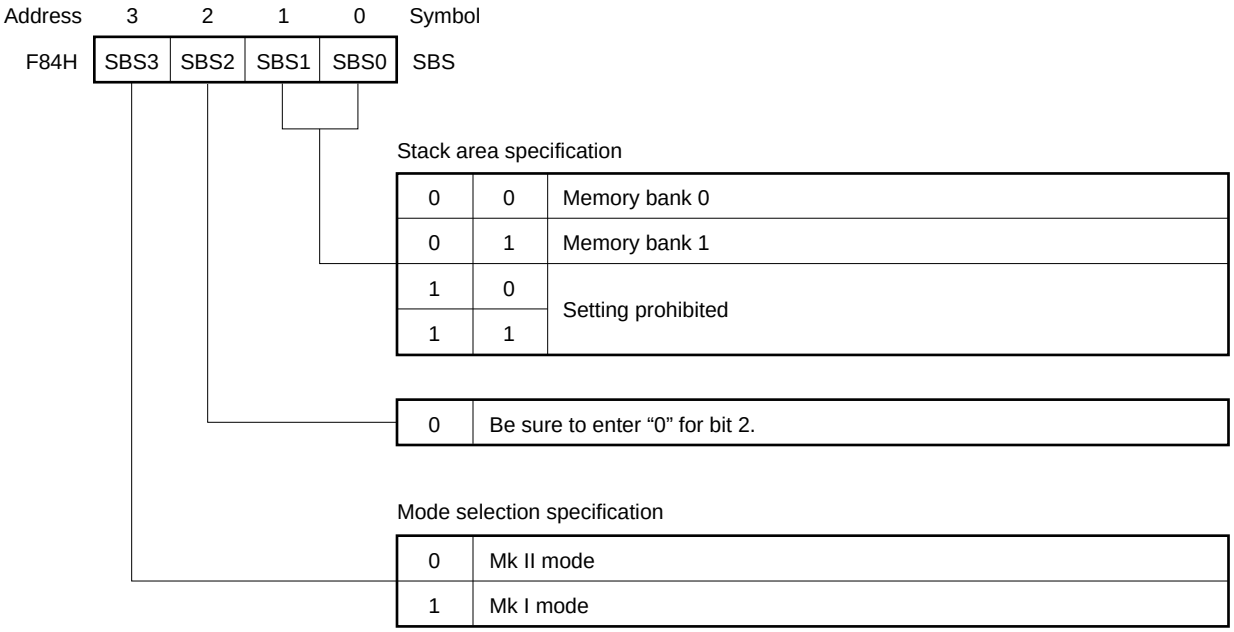
4.2 Setting of Stack Bank Selection (SBS) Register

Use the stack bank selection register to switch between Mk I mode and Mk II mode. Figure 4-1 shows the format for doing this.

The stack bank selection register is set using a 4-bit memory manipulation instruction. When using the Mk I mode, be sure to initialize the stack bank selection register to 100XB[Note] at the beginning of the program. When using the Mk II mode, be sure to initialize it to 000XB[Note].

Note Set the desired value for X.

Figure 4-1. Format of Stack Bank Selection Register



Cautions 1. SBS3 is set to "1" after $\overline{\text{RESET}}$ input, and consequently the CPU operates in Mk I mode. When using instructions for Mk II mode, set SBS3 to "0" and set Mk II mode before using the instructions.

2. When using Mk II mode, execute a subroutine call instruction and an interrupt instruction after $\overline{\text{RESET}}$ input and after setting the stack bank selection register.

5. DIFFERENCES BETWEEN μPD75P3216 AND μPD753204, 753206, AND 753208

The μPD75P3216 replaces the internal mask ROM in the μPD753204, 753206, and 753208 with a one-time PROM and features expanded ROM capacity. The μPD75P3216's Mk I mode supports the Mk I mode in the μPD753204, 753206, and 753208 and the μPD75P3216's Mk II mode supports the Mk II mode in the μPD753204, 753206, and 753208.

Table 5-1 lists differences among the μPD75P3216 and the μPD753204, 753206, and 753208. Be sure to check the differences among these products before using them with PROMs for debugging or prototype testing of application systems or, later, when using them with a mask ROM for full-scale production.

For details on the CPU functions and internal hardware, refer to **μPD753208 User's Manual (U10158E)**.

Table 5-1. Differences between μPD75P3216 and μPD753204, 753206, and 753208

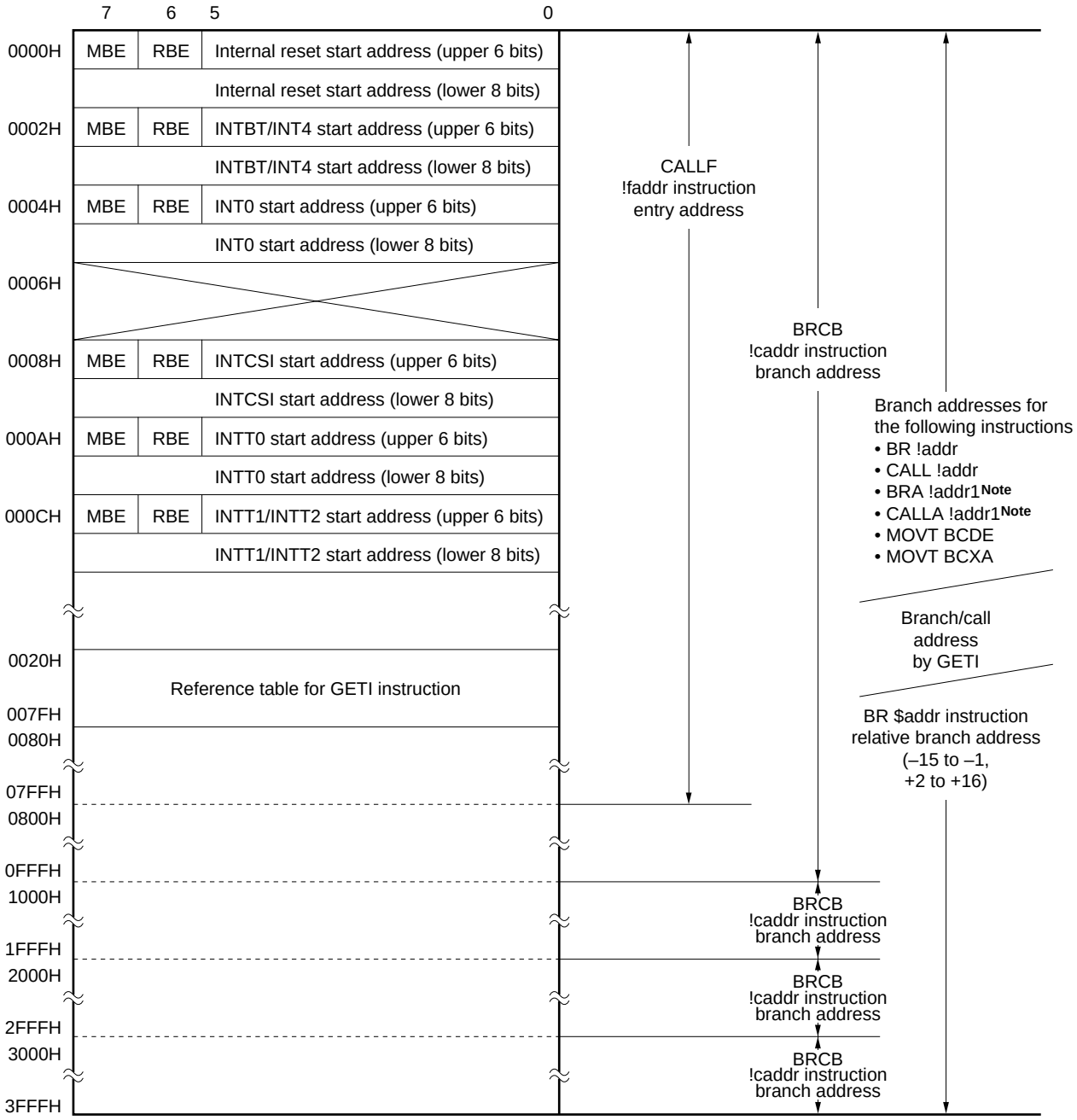
Item		μPD753204	μPD753206	μPD753208	μPD75P3216
Program counter		12 bits	13 bits		14 bits
Program memory (bytes)		Mask ROM 4096	Mask ROM 6144	Mask ROM 8192	One-time PROM 16384
Data memory (× 4 bits)		512			
Mask options	Pull-up resistor for port 5	Yes (specifiable)			No (off chip)
	Waiting time in $\overline{\text{RESET}}$	Yes (selectable from $2^{17}/f_X$ and $2^{15}/f_X$)**Note**			No (Fixed to $2^{15}/f_X$ ms)
Pin configuration	Pin 9 to 12	P30 to P33			P30/MD0-P33/MD3
★	Pin 14 to 17	P50 to P53			P50/D4-P53/D7
★	Pin 18 to 20	P60/KR0 to P63/KR3			P60/KR0/D0-P63/KR3/D3
	Pin 25	IC			V_{PP}
Other		Noise resistance and noise radiation may differ due to the different circuit sizes and mask layouts.			

Note $2^{17}/f_X$ = 21.8 ms (@6.0 MHz), 31.3 ms (@4.19 MHz)
$2^{15}/f_X$ = 5.46 ms (@6.0 MHz), 7.81 ms (@4.19 MHz)

Caution Noise resistance and noise radiation are different in PROM and mask ROMs. In transferring to mask ROM versions from the PROM version in a process between prototype development and full production, be sure to fully evaluate the mask ROM version's CS (not ES).

6. MEMORY CONFIGURATION

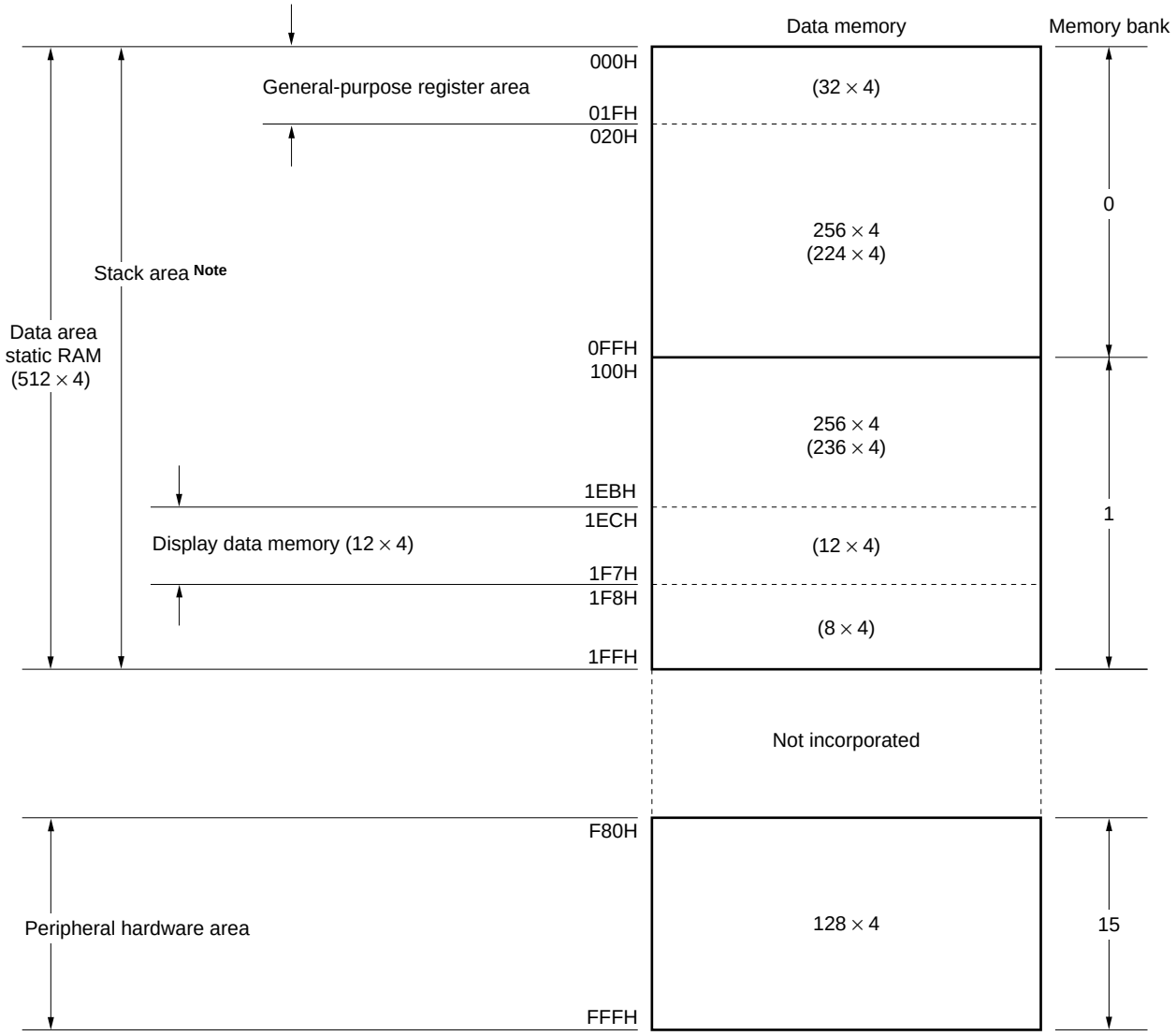
Figure 6-1. Program Memory Map



Note Can be used only in Mk II mode.

Remark For instructions other than those noted above, the BR PCDE and BR PCXA instructions can be used to branch to addresses with changes in the PC's lower 8 bits only.

Figure 6-2. Data Memory Map



Note Memory bank 0 or 1 can be selected as the stack area.

7. INSTRUCTION SET

(1) Representation and coding formats for operands

In the instruction's operand area, use the following coding format to describe operands corresponding to the instruction's operand representations (for further description, refer to **RA75X Assembler Package User's Manual –Language (EEU-1343)**). When there are several codes, select and use just one. Codes that consist of upper-case letters and + or – symbols are key words that should be entered as they are.

For immediate data, enter an appropriate numerical value or label.

Enter register flag symbols as label descriptors instead of mem, fmem, pmem, bit, etc. (for further description, refer to **μPD753208 User's Manual (U10158E)**). The number of labels that can be entered for fmem and pmem are restricted.

Representation	Coding Format
reg	X, A, B, C, D, E, H, L
reg1	X, B, C, D, E, H, L
rp	XA, BC, DE, HL
rp1	BC, DE, HL
rp2	BC, DE
rp'	XA, BC, DE, HL, XA', BC', DE', HL'
rp'1	BC, DE, HL, XA', BC', DE', HL'
rpa	HL, HL+, HL–, DE, DL
rpa1	DE, DL
n4	4-bit immediate data or label
n8	8-bit immediate data or label
mem	8-bit immediate data or label[Note]
bit	2-bit immediate data or label
fmem	FB0H to FBFH, FF0H to FFFH immediate data or label
pmem	FC0H to FFFH immediate data or label
addr	0000H to 3FFFH immediate data or label
addr1	0000H to 3FFFH immediate data or label (Mk II mode only)
caddr	12-bit immediate data or label
faddr	11-bit immediate data or label
taddr	20H to 7FH immediate data (however, bit0 = 0) or label
PORTn	PORT0 to PORT3, PORT5, PORT6, PORT8, PORT9
IEXXX	IEBT, IECSI, IET0, IET1, IET2, IE0, IE2, IE4, IEW
RBn	RB0 to RB3
MBn	MB0, MB1, MB15

Note When processing 8-bit data, only even-numbered addresses can be specified.

(2) Operation legend

A	:	A register; 4-bit accumulator
B	:	B register
C	:	C register
D	:	D register
E	:	E register
H	:	H register
L	:	L register
X	:	X register
XA	:	Register pair (XA); 8-bit accumulator
BC	:	Register pair (BC)
DE	:	Register pair (DE)
HL	:	Register pair (HL)
XA'	:	Expansion register pair (XA')
BC'	:	Expansion register pair (BC')
DE'	:	Expansion register pair (DE')
HL'	:	Expansion register pair (HL')
PC	:	Program counter
SP	:	Stack pointer
CY	:	Carry flag; bit accumulator
PSW	:	Program status word
MBE	:	Memory bank enable flag
RBE	:	Register bank enable flag
PORTn	:	Port n (n = 0 to 3, 5, 6, 8, 9)
IME	:	Interrupt master enable flag
IPS	:	Interrupt priority selection register
IEXXX	:	Interrupt enable flag
RBS	:	Register bank selection register
MBS	:	Memory bank selection register
PCC	:	Processor clock control register
.	:	Delimiter for address and bit
(XX)	:	Addressed data
XXH	:	Hexadecimal data

(3) Description of symbols used in addressing area

*1	MB = MBE • MBS MBS = 0, 1, 15	Data memory addressing
*2	MB = 0	
*3	MBE = 0 : MB = 0 (000H to 07FH) MB = 15 (F80H to FFFH) MBE = 1 : MB = MBS MBS = 0, 1, 15	
*4	MB = 15, fmem = FB0H to FBFH, FF0H to FFFH	
*5	MB = 15, pmem = FC0H to FFFH	
*6	addr = 0000H to 3FFFH	
*7	addr, addr1 = (Current PC) – 15 to (Current PC) – 1 (Current PC) +2 to (Current PC) +16	Program memory addressing
*8	caddr = 0000H to 0FFFH ($PC_{13, 12}$ = 00B) or 1000H to 1FFFH ($PC_{13, 12}$ = 01B) or 2000H to 2FFFH ($PC_{13, 12}$ = 10B) or 3000H to 3FFFH ($PC_{13, 12}$ = 11B)	
*9	faddr = 0000H to 07FFH	
*10	taddr = 0020H to 007FH	
*11	addr1 = 0000H to 3FFFH (Mk II mode only)	

Remarks 1. MB indicates access-enabled memory banks.

2. In area *2, MB = 0 for both MBE and MBS.

3. In areas *4 and *5, MB = 15 for both MBE and MBS.

4. Areas *6 to *11 indicate corresponding address-enabled areas.

(4) Description of machine cycles

S indicates the number of machine cycles required for skipping of skip-specified instructions. The value of S varies as shown below.

- No skip ..... S = 0
- Skipped instruction is 1-byte or 2-byte instruction .. S = 1
- Skipped instruction is 3-byte instruction**Note** ..... S = 2

Note 3-byte instructions: BR !addr, BRA !addr1, CALL !addr, and CALLA !addr1

Caution The GETI instruction is skipped for one machine cycle.

One machine cycle equals one cycle (= tCY) of the CPU clock F. Use the PCC setting to select among four cycle times.

Instruction Group	Mnemonic	Operand	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Transfer	MOV	A, #n4	1	1	A←n4		String-effect A
		reg1, #n4	2	2	reg1←n4		
		XA, #n8	2	2	XA←n8		String-effect A
		HL, #n8	2	2	HL←n8		String-effect B
		rp2, #n8	2	2	rp2←n8		
		A, @HL	1	1	A←(HL)	*1	
		A, @HL+	1	2+S	A←(HL), then L←L+1	*1	L=0
		A, @HL–	1	2+S	A←(HL), then L←L–1	*1	L=FH
		A, @rpa1	1	1	A←(rpa1)	*2	
		XA, @HL	2	2	XA←(HL)	*1	
		@HL, A	1	1	(HL)←A	*1	
		@HL, XA	2	2	(HL)←XA	*1	
		A, mem	2	2	A←(mem)	*3	
		XA, mem	2	2	XA←(mem)	*3	
		mem, A	2	2	(mem)←A	*3	
		mem, XA	2	2	(mem)←XA	*3	
		A, reg	2	2	A←reg		
		XA, rp’	2	2	XA←rp’		
		reg1, A	2	2	reg1←A		
		rp’1, XA	2	2	rp’1←XA		
	XCH	A, @HL	1	1	A↔(HL)	*1	
		A, @HL+	1	2+S	A↔(HL), then L←L+1	*1	L=0
		A, @HL–	1	2+S	A↔(HL), then L←L–1	*1	L=FH
		A, @rpa1	1	1	A↔(rpa1)	*2	
		XA, @HL	2	2	XA↔(HL)	*1	
		A, mem	2	2	A↔(mem)	*3	
		XA, mem	2	2	XA↔(mem)	*3	
		A, reg1	1	1	A↔reg1		
		XA, rp’	2	2	XA↔rp’		
Table reference	MOVT	XA, @PCDE	1	3	XA←$(PC_{13-8}+DE)_{ROM}$		
		XA, @PCXA	1	3	XA←$(PC_{13-8}+XA)_{ROM}$		
		XA, @BCDE**Note**	1	3	XA←$(B_{2-0}+BCDE)_{ROM}$	*6	
		XA, @BCXA**Note**	1	3	XA←$(B_{2-0}+BCXA)_{ROM}$	*6	

Note Only the lower 2 bits in the B register are valid.

Instruction Group	Mnemonic	Operand	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Bit transfer	MOV1	CY, fmem.bit	2	2	CY←(fmem.bit)	*4	
		CY, pmem.@L	2	2	CY←(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY←(H+mem$_{3-0}$.bit)	*1	
		fmem.bit, CY	2	2	(fmem.bit)←CY	*4	
		pmem.@L, CY	2	2	(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))←CY	*5	
		@H+mem.bit, CY	2	2	(H+mem$_{3-0}$.bit)←CY	*1	
Arithmetic	ADDS	A, #n4	1	1+S	A←A+n4		carry
		XA, #n8	2	2+S	XA←XA+n8		carry
		A, @HL	1	1+S	A←A+(HL)	*1	carry
		XA, rp'	2	2+S	XA←XA+rp'		carry
		rp'1, XA	2	2+S	rp'1←rp'1+XA		carry
	ADDC	A, @HL	1	1	A, CY←A+(HL)+CY	*1	
		XA, rp'	2	2	XA, CY←XA+rp'+CY		
		rp'1, XA	2	2	rp'1, CY←rp'1+XA+CY		
	SUBS	A, @HL	1	1+S	A←A–(HL)	*1	borrow
		XA, rp'	2	2+S	XA←XA–rp'		borrow
		rp'1, XA	2	2+S	rp'1←rp'1–XA		borrow
	SUBC	A, @HL	1	1	A, CY←A–(HL)–CY	*1	
		XA, rp'	2	2	XA, CY←XA–rp'–CY		
		rp'1, XA	2	2	rp'1, CY←rp'1–XA–CY		
	AND	A, #n4	2	2	A←A∧n4		
		A, @HL	1	1	A←A∧(HL)	*1	
		XA, rp'	2	2	XA←XA∧rp'		
		rp'1, XA	2	2	rp'1←rp'1∧XA		
	OR	A, #n4	2	2	A←A∨n4		
		A, @HL	1	1	A←A∨(HL)	*1	
		XA, rp'	2	2	XA←XA∨rp'		
		rp'1, XA	2	2	rp'1←rp'1∨XA		
	XOR	A, #n4	2	2	A←A∨̲n4		
		A, @HL	1	1	A←A∨̲(HL)	*1	
		XA, rp'	2	2	XA←XA∨̲rp'		
		rp'1, XA	2	2	rp'1←rp'1∨̲XA		
Accumulator manipulation	RORC	A	1	1	CY←A$_0$, A$_3$←CY, A$_{n-1}$←A$_n$		
	NOT	A	2	2	A←$\overline{A}$		
Increment/ decrement	INCS	reg	1	1+S	reg←reg+1		reg=0
		rp1	1	1+S	rp1←rp1+1		rp1=00H
		@HL	2	2+S	(HL)←(HL)+1	*1	(HL)=0
		mem	2	2+S	(mem)←(mem)+1	*3	(mem)=0
	DECS	reg	1	1+S	reg←reg–1		reg=FH
		rp'	2	2+S	rp'←rp'–1		rp'=FFH

Instruction Group	Mnemonic	Operand	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Comparison	SKE	reg, #n4	2	2+S	Skip if reg=n4		reg=n4
		@HL, #n4	2	2+S	Skip if(HL)=n4	*1	(HL)=n4
		A, @HL	1	1+S	Skip if A=(HL)	*1	A=(HL)
		XA, @HL	2	2+S	Skip if XA=(HL)	*1	XA=(HL)
		A, reg	2	2+S	Skip if A=reg		A=reg
		XA, rp'	2	2+S	Skip if XA=rp'		XA=rp'
Carry flag manipulation	SET1	CY	1	1	CY←1		
	CLR1	CY	1	1	CY←0		
	SKT	CY	1	1+S	Skip if $\overline{CY}$=1		CY=1
	NOT1	CY	1	1	CY←$\overline{CY}$		
Memory bit manipulation	SET1	mem.bit	2	2	(mem.bit)←1	*3	
		fmem.bit	2	2	(fmem.bit)←1	*4	
		pmem.@L	2	2	(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))←1	*5	
		@H+mem.bit	2	2	(H+mem$_{3-0}$.bit)←1	*1	
	CLR1	mem.bit	2	2	(mem.bit)←0	*3	
		fmem.bit	2	2	(fmem.bit)←0	*4	
		pmem.@L	2	2	(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))←0	*5	
		@H+mem.bit	2	2	(H+mem$_{3-0}$.bit)←0	*1	
	SKT	mem.bit	2	2+S	Skip if(mem.bit)=1	*3	(mem.bit)=1
		fmem.bit	2	2+S	Skip if(fmem.bit)=1	*4	(fmem.bit)=1
		pmem.@L	2	2+S	Skip if(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))=1	*5	(pmem.@L)=1
		@H+mem.bit	2	2+S	Skip if(H+mem$_{3-0}$.bit)=1	*1	(@H+mem.bit)=1
	SKF	mem.bit	2	2+S	Skip if(mem.bit)=0	*3	(mem.bit)=0
		fmem.bit	2	2+S	Skip if(fmem.bit)=0	*4	(fmem.bit)=0
		pmem.@L	2	2+S	Skip if(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))=0	*5	(pmem.@L)=0
		@H+mem.bit	2	2+S	Skip if(H+mem$_{3-0}$.bit)=0	*1	(@H+mem.bit)=0
	SKTCLR	fmem.bit	2	2+S	Skip if(fmem.bit)=1 and clear	*4	(fmem.bit)=1
		pmem.@L	2	2+S	Skip if(pmem$_{7-2}$+L$_{3-2}$.bit (L$_{1-0}$))=1 and clear	*5	(pmem.@L)=1
		@H+mem.bit	2	2+S	Skip if(H+mem$_{3-0}$.bit)=1 and clear	*1	(@H+mem.bit)=1
	AND1	CY, fmem.bit	2	2	CY←CY∧(fmem.bit)	*4	
		CY, pmem.@L	2	2	CY←CY∧(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY←CY∧(H+mem$_{3-0}$.bit)	*1	
	OR1	CY, fmem.bit	2	2	CY←CY∨(fmem.bit)	*4	
		CY, pmem.@L	2	2	CY←CY∨(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY←CY∨(H+mem$_{3-0}$.bit)	*1	
	XOR1	CY, fmem.bit	2	2	CY←CY∀ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY←CY∀(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY←CY∀(H+mem$_{3-0}$.bit)	*1	

Instruction Group	Mnemonic	Operand	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Branch	BR**Note**	addr	—	—	PC_{13-0}←addr (Use the assembler to select the most appropriate instruction among the following. • BR !addr • BRCB !caddr • BR $addr)	*6	
		addr1	—	—	PC_{13-0}←addr1 (Use the assembler to select the most appropriate instruction among the following. • BRA !addr1 • BR !addr • BRCB !caddr • BR $addr1)	*11	
		!addr	3	3	PC_{13-0}←addr	*6	
		$addr	1	2	PC_{13-0}←addr	*7	
		$addr1	1	2	PC_{13-0}←addr1		
		PCDE	2	3	PC_{13-0}←PC_{13-8}+DE		
		PCXA	2	3	PC_{13-0}←PC_{13-8}+XA		
		BCDE	2	3	PC_{13-0}←BCDE	*6	
		BCXA	2	3	PC_{13-0}←BCXA	*6	
	BRA**Note**	!addr1	3	3	PC_{13-0}←addr1	*11	
	BRCB	!caddr	2	2	PC_{13-0}←$PC_{13, 12}$+$caddr_{11-0}$	*8	

Note Shaded areas indicate support for Mk II mode only. Other areas indicate support for Mk I mode only.

Instruction Group	Mnemonic	Operand	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Subroutine stack control	CALLA[Note]	!addr1	3	3	(SP–6)(SP–3)(SP–4)←PC11-0 (SP–5)←0, 0, PC13, 12 (SP–2)←X, X, MBE, RBE PC13–0←addr1, SP←SP–6		
	CALL[Note]	!addr	3	3	(SP–4)(SP–1)(SP–2)←PC11-0 (SP–3)←MBE, RBE, PC13, 12 PC13–0←addr, SP←SP–4	*6	
				4	(SP–6)(SP–3)(SP–4)←PC11-0 (SP–5)←0, 0, PC13, 12 (SP–2)←X, X, MBE, RBE PC13-0←addr, SP←SP–6		
	CALLF[Note]	!faddr	2	2	(SP–4)(SP–1)(SP–2)←PC11-0 (SP–3)←MBE, RBE, PC13, 12 PC13-0←000+faddr, SP←SP–4	*9	
				3	(SP–6)(SP–3)(SP–4)←PC11-0 (SP–5)←0, 0, PC13, 12 (SP–2)←X, X, MBE, RBE PC13-0←000+faddr, SP←SP–6		
	RET[Note]		1	3	MBE, RBE, PC13, 12←(SP+1) PC11-0←(SP)(SP+3)(SP+2) SP←SP+4		
					X, X, MBE, RBE←(SP+4) PC11-0←(SP)(SP+3)(SP+2) MBE, 0, PC13, 12←(SP+1) SP←SP+6		
	RETS[Note]		1	3+S	MBE, RBE, PC13, 12←(SP+1) PC11-0←(SP)(SP+3)(SP+2) SP←SP+4 then skip unconditionally		Unconditional
					X, X, MBE, RBE←(SP+4) PC11-0←(SP)(SP+3)(SP+2) 0, 0, PC13, 12←(SP+1) SP←SP+6 then skip unconditionally		
	RETI[Note]		1	3	MBE, RBE, PC13, 12←(SP+1) PC11-0←(SP)(SP+3)(SP+2) PSW←(SP+4)(SP+5), SP←SP+6		
					0, 0, PC13, 12←(SP+1) PC11-0←(SP)(SP+3)(SP+2) PSW←(SP+4)(SP+5), SP←SP+6		
	PUSH	rp	1	1	(SP–1)(SP–2)←rp, SP←SP–2		
		BS	2	2	(SP–1)←MBS, (SP–2)←RBS, SP←SP–2		
	POP	rp	1	1	rp←(SP+1)(SP), SP←SP+2		
		BS	2	2	MBS←(SP+1), RBS←(SP), SP←SP+2		

Note Shaded areas indicate support for Mk II mode only. Other areas indicate support for Mk I mode only.

Instruction Group	Mnemonic	Operand	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Interrupt control	EI		2	2	IME(IPS.3)←1		
		IEXXX	2	2	IEXXX←1		
	DI		2	2	IME(IPS.3)←0		
		IEXXX	2	2	IEXXX←0		
I/O	IN Note 1	A, PORTn	2	2	A←PORTn (n=0-3, 5, 6, 8, 9)		
		XA, PORTn	2	2	XA←PORTn+1, PORTn (n=8)		
	OUT Note 1	PORTn, A	2	2	PORTn←A (n=2-3, 5, 6, 8, 9)		
		PORTn, XA	2	2	PORTn+1, PORTn←XA (n=8)		
CPU control	HALT		2	2	Set HALT Mode(PCC.2←1)		
	STOP		2	2	Set STOP Mode(PCC.3←1)		
	NOP		1	1	No Operation		
Special	SEL	RBn	2	2	RBS←n (n=0-3)		
		MBn	2	2	MBS←n (n=0, 1, 15)		
	GETI Note 2, 3	taddr	1	3	• When using TBR instruction PC_{13-0}←(taddr)$_{5-0}$+(taddr+1)	*10	
					• When using TCALL instruction (SP–4)(SP–1)(SP–2)←PC_{11-0} (SP+1)←MBE, RBE, $PC_{13, 12}$ PC_{13-0}←(taddr)$_{5-0}$+(taddr+1) SP←SP–4		
					• When using instruction other than TBR or TCALL Execute (taddr)(taddr+1) instructions		Determined by referenced instruction
			1	3	• When using TBR instruction PC_{13-0}←(taddr)$_{5-0}$+(taddr+1)	*10	
				4	• When using TCALL instruction (SP–6)(SP–3)(SP–4)←PC_{11-0} (SP–2)←X, X, MBE, RBE PC_{13-0}←(taddr)$_{5-0}$+(taddr+1) SP←SP–6		
				3	• When using instruction other than TBR or TCALL Execute (taddr)(taddr+1) instructions		Determined by referenced instruction

Notes 1. Before executing the IN or OUT instruction, set MBE to 0 or 1 and set MBE to 15.

2. TBR and TCALL instructions are assembler directives for the GETI instruction's table definitions.

3. Shaded areas indicate support for Mk II mode only. Other areas indicate support for Mk I mode only.

8. ONE-TIME PROM (PROGRAM MEMORY) WRITE AND VERIFY

The program memory contained in the μPD75P3216 is a 16384 × 8-bit one-time PROM that can be electrically written one time only. The pins listed in the table below are used for this PROM's write/verify operations. Clock input from the X1 pin is used instead of address input as a method for updating addresses.

Pin	Function
V_{PP}	Pin where program voltage is applied during program memory write/verify (usually V_{DD} potential)
X1, X2	Clock input pins for address updating during program memory write/verify. Input the X1 pin's inverted signal to the X2 pin.
MD0 to MD3	Operation mode selection pin for program memory write/verify
D0/P60/KR0-D3/P63/KR3 (lower 4 bits) D4/P50-D7/P53 (upper 4 bits)	8-bit data I/O pins for program memory write/verify
V_{DD}	Pin where power supply voltage is applied. Applies 1.8 to 5.5 V in normal operation mode and +6 V for program memory write/verify.

Caution Pins not used for program memory write/verify should be connected to Vss.

8.1 Operation Modes for Program Memory Write/Verify

When +6 V is applied to the V_{DD} pin and +12.5 V to the V_{PP} pin, the μPD75P3216 enters the program memory write/verify mode. The following operation modes can be specified by setting pins MD0 to MD3 as shown below.

Operation Mode Specification						Operation Mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Zero-clear program memory address
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	X	H	H	Program inhibit mode

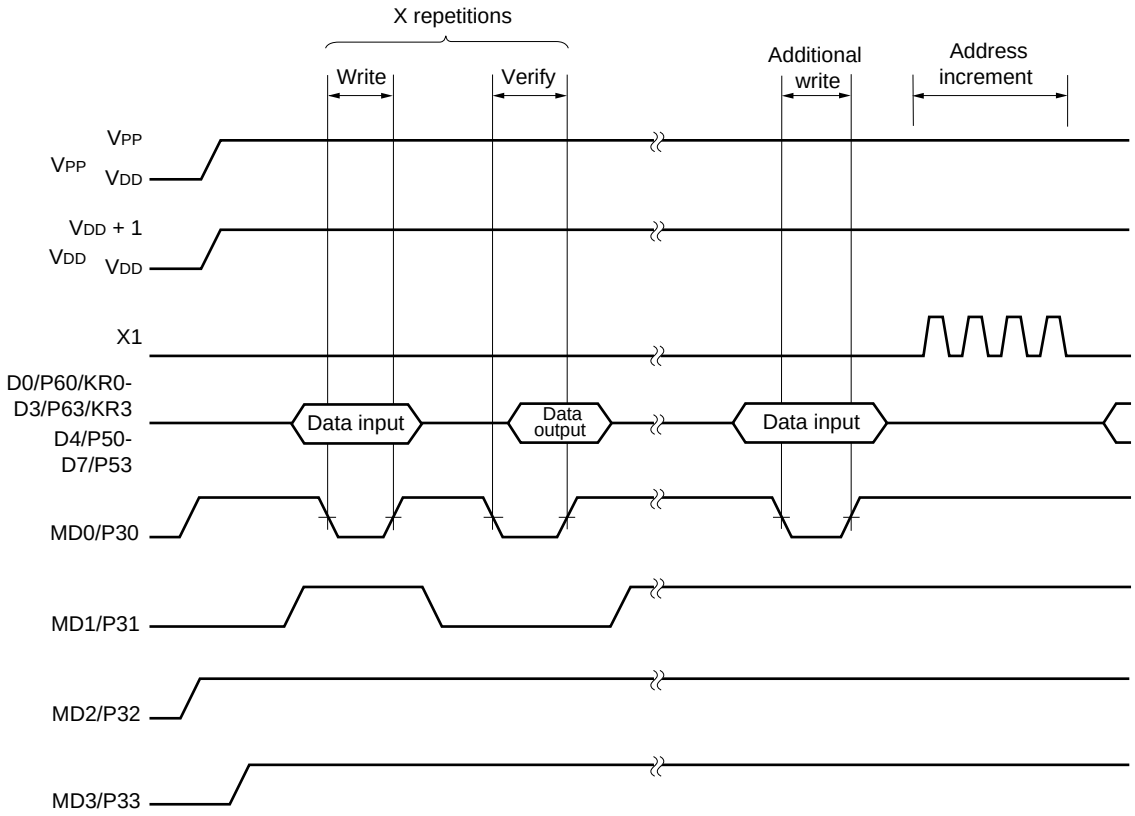
X: L or H

★ 8.2 Program Memory Write Procedure

Program memory can be written at high speed using the following procedure.

(1) Pull down unused pins to Vss through resistors. Set the X1 pin low.
(2) Supply 5 V to the V_{DD} and V_{PP} pins.
(3) Wait 10 μs.
(4) Select the zero-clear program memory address mode.
(5) Supply 6 V to the V_{DD} and 12.5 V to the V_{PP} pins.
(6) Write data in the 1 ms write mode.
(7) Select the verify mode. If the data is correct, go to step (8) and if not, repeat steps (6) and (7).
(8) (X : number of write operations from steps (6) and (7)) × 1 ms additional write.
(9) Apply four pulses to the X1 pin to increment the program memory address by one.
(10) Repeat steps (6) to (9) until the end address is reached.
(11) Select the zero-clear program memory address mode.
(12) Return the V_{DD} and V_{PP} pins back to 5 V.
(13) Turn off the power.

The following figure shows steps (2) to (9).

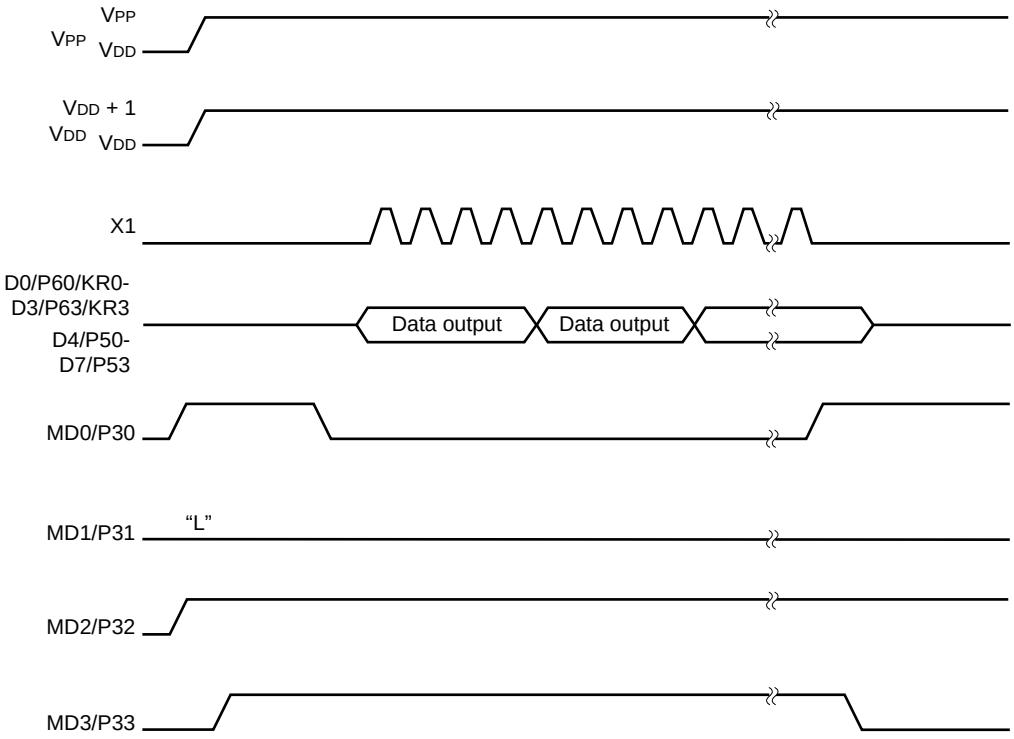


★ 8.3 Program Memory Read Procedure

The μPD75P3216 can read program memory contents using the following procedure.

(1) Pull down unused pins to V_{SS} through resistors. Set the X1 pin low.
(2) Supply 5 V to the V_{DD} and V_{PP} pins.
(3) Wait 10 μs.
(4) Select the zero-clear program memory address mode.
(5) Supply 6 V to the V_{DD} and 12.5 V to the V_{PP} pins.
(6) Select the verify mode. Apply four pulses to the X1 pin. Every four clock pulses will output the data stored in one address.
(7) Select the zero-clear program memory address mode.
(8) Return the V_{DD} and V_{PP} pins back to 5 V.
(9) Turn off the power.

The following figure shows steps (2) to (9).



8.4 One-time PROM Screening

Due to its structure, the one-time PROM cannot be fully tested before shipment by NEC. Therefore, NEC recommends that after the required data is written and the PROM is stored under the temperature and time conditions shown below, the PROM should be verified via a screening.

Storage Temperature	Storage Time
125 ˚C	24 hours

★ 9. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Test Conditions	Rating	Unit
Supply voltage	V_{DD}		–0.3 to +7.0	V
PROM supply voltage	V_{PP}		–0.3 to +13.5	V
Input voltage	V_{I1}	Except port 5	–0.3 to V_{DD} + 0.3	V
	V_{I2}	Port 5 N-ch open-drain	–0.3 to +14	V
Output voltage	V_O		–0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin	–10	mA
		Total for all pins	–30	mA
Output current, low	I_{OL}	Per pin	30	mA
		Total for all pins	220	mA
Operating ambient temperature	T_A		–40 to +85[Note]	°C
Storage temperature	T_{stg}		–65 to +150	°C

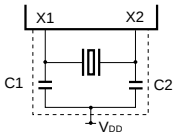
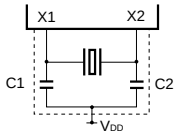
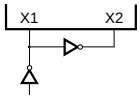
Note When LCD is driven in normal mode: T_A = –10 to +85 °C

Caution Exposure to Absolute Maximum Ratings even for instant may affect device reliability; exceeding the ratings could cause parmanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.

CAPACITANCE (T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz			15	pF
Output capacitance	C_{OUT}	Unmeasured pins returned to 0 V.			15	pF
I/O capacitance	C_{IO}				15	pF

SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Resonator	Recommended Constant	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillator frequency (fx) Note 1		1.0		6.0 Note 2	MHz
		Oscillation stabilization time Note 3	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillator frequency (fx) Note 1		1.0		6.0 Note 2	MHz
		Oscillation stabilization time Note 3	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (fx) Note 1		1.0		6.0 Note 2	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		83.3		500	ns

Notes 1. The oscillator frequency and X1 input frequency indicate characteristics of the oscillator only. For the instruction execution time, refer to the AC characteristics.

2. When the oscillator frequency is 4.19 MHz < fx ≤ 6.0 MHz, setting the processor clock control register (PCC) to 0011 results in 1 machine cycle being less than the required 0.95 μs. Therefore, set PCC to a value other than 0011.

3. The oscillation stabilization time is necessary for oscillation to stabilize after applying V_{DD} or releasing the STOP mode.

Caution When using the system clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as V_{SS}.**
- **Do not ground it to the ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions			MIN.	TYP.	MAX.	Unit
Output current, low	I_{OL}	Per pin					15	mA
		Total for all pins					150	mA
Input voltage, high	V_{IH1}	Ports 2, 3, 8, 9		2.7 ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		V_{DD}	V
				1.8 ≤ V_{DD} < 2.7 V	0.9V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, $\overline{\text{RESET}}$		2.7 ≤ V_{DD} ≤ 5.5 V	0.8V_{DD}		V_{DD}	V
				1.8 ≤ V_{DD} < 2.7 V	0.9V_{DD}		V_{DD}	V
	V_{IH3}	Port 5	N-ch open-drain	2.7 ≤ V_{DD} ≤ 5.5 V	0.7V_{DD}		13	V
				1.8 ≤ V_{DD} < 2.7 V	0.9V_{DD}		13	V
	V_{I14}	X1			V_{DD} – 0.1		V_{DD}	V
Input voltage, low	V_{IL1}	Ports 2, 3, 5, 8, 9		2.7 ≤ V_{DD} ≤ 5.5 V	0		0.3V_{DD}	V
				1.8 ≤ V_{DD} < 2.7 V	0		0.1V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, $\overline{\text{RESET}}$		2.7 ≤ V_{DD} ≤ 5.5 V	0		0.2V_{DD}	V
				1.8 ≤ V_{DD} < 2.7 V	0		0.1V_{DD}	V
	V_{IL3}	X1			0		0.1	V
Output voltage, high	V_{OH}	$\overline{\text{SCK}}$, SO, ports 2, 3, 6, 8, 9 I_{OH} = –1 mA			V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	$\overline{\text{SCK}}$, SO, ports 2, 3, 5, 6, 8, 9		I_{OL} = 15 mA, V_{DD} = 4.5 to 5.5 V		0.2	2.0	V
				I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1	N-ch open-drain pull-up resistor ≥ 1 kΩ				0.2V_{DD}	V
Input leakage current, high	I_{LIH1}	V_{IN} = V_{DD}	Other pins than X1				3	μA
	I_{LIH2}		X1				20	μA
	I_{LIH3}	V_{IN} = 13 V	Port 5 (N-ch open-drain)				20	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	Other pins than port 5 and X1				–3	μA
	I_{LIL2}		X1				–20	μA
	I_{LIL3}		Port 5 (N-ch open-drain) When an input instruction is not executed				–3	μA
			Port 5 (N-ch open-drain) When an input instruction is executed				–30	μA
				V_{DD} = 5.0 V		–10	–27	μA
				V_{DD} = 3.0 V		–3	–8	μA
Output leakage current, high	I_{LOH1}	V_{OUT} = V_{DD}	$\overline{\text{SCK}}$, SO/SB0, SB1, ports 2, 3, 6, 8, 9				3	μA
	I_{LOH2}	V_{OUT} = 13 V	Port 5 (N-ch open-drain)				20	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V					–3	μA
Pull-up resistor	R_L	V_{IN} = 0 V	Ports 0, 1, 2, 3, 6, 8, 9 (Excluding P00 pin)		50	100	200	kΩ

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions			MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}	VAC0 = 0	T_A = –40 to +85 °C		2.7		V_{DD}	V
			T_A = –10 to +85 °C		2.2		V_{DD}	V
		VAC0 = 1			1.8		V_{DD}	V
VAC current	I_{VAC}	VAC0 = 1, V_{DD} = 2.0 V ± 10%				1	4	μA
LCD output voltage deviation Note 1 (common)	V_{ODC}	Io = ±1 μA	$V_{LCD0} = V_{LCD}$ $V_{LCD1} = V_{LCD} \times 2/3$		0		±0.2	V
LCD output voltage deviation Note 1 (segment)	V_{ODS}	Io = ±0.5 μA	$V_{LCD2} = V_{LCD} \times 1/3$ 2.2 V ≤ V_{LCD} ≤ V_{DD} Note 1		0		±0.2	V
Supply current Note 2	I_{DD1}	6.0 MHz Crystal oscillation C1 = C2 = 22 pF	V_{DD} = 5.0 V ± 10% Note 3			2.6	7.8	mA
			V_{DD} = 3.0 V ± 10% Note 4			0.47	1.4	mA
	I_{DD2}		HALT mode	V_{DD} = 5.0 V ± 10%		0.72	2.1	mA
				V_{DD} = 3.0 V ± 10%		0.27	0.8	mA
	I_{DD1}	4.19 MHz Crystal oscillation C1 = C2 = 22 pF	V_{DD} = 5.0 V ± 10% Note 3			1.9	5.7	mA
			V_{DD} = 3.0 V ± 10% Note 4			0.36	1.1	mA
	I_{DD2}		HALT mode	V_{DD} = 5.0 V ± 10%		0.7	2.0	mA
				V_{DD} = 3.0 V ± 10%		0.23	0.7	mA
	I_{DD5}	STOP mode Note 5	V_{DD} = 5.0 V ± 10%			0.05	10	μA
			V_{DD} = 3.0 V ±10%			0.02	5	μA
				T_A = 25°C		0.02	3	μA

Notes 1. The voltage deviation is the difference from the output voltage corresponding to the ideal value of the segment and common outputs (V_{LCDn}; n = 0, 1, 2).

2. Not including current flowing in on-chip pull-up resistors.

3. When the processor clock control register (PCC) is set to 0011 and the device is operated in the high-speed mode.

4. When PCC is set to 0000 and the device is operated in the low-speed mode.

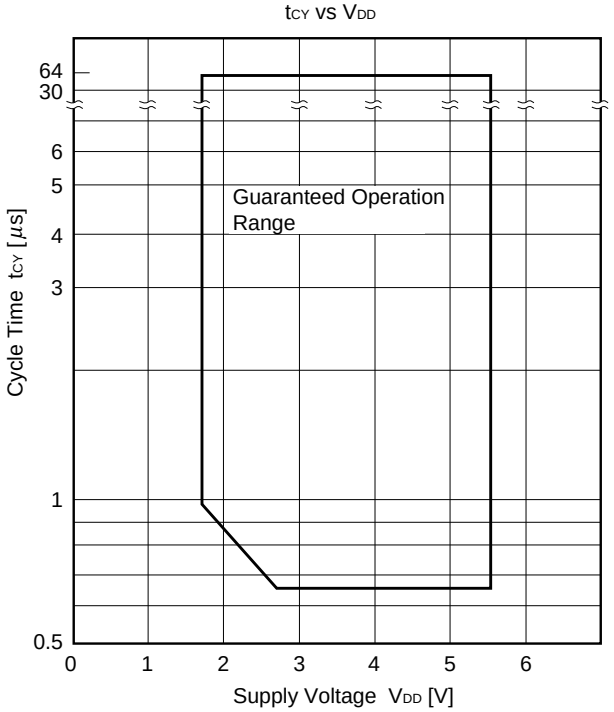
5. Set VAC0 to 0 when setting the STOP mode. If VAC0 is set to 1, the current increases by about 1 μA.

AC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
CPU clock cycle time Note 1	t_{CY}	V_{DD} = 2.7 to 5.5 V		0.67		64	μs
				0.95		64	μs
TI0 input frequency	f_{TI}	V_{DD} = 2.7 to 5.5 V		0		1	MHz
				0		275	kHz
TI0 input high/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 2.7 to 5.5 V		0.48			μs
				1.8			μs
Interrupt input high/low-level width	t_{INTH}, t_{INTL}	INT0	IM02 = 0	**Note 2**			μs
			IM02 = 1	10			μs
		INT4		10			μs
		KR0 to KR3		10			μs
$\overline{\text{RESET}}$ low level width	t_{RSL}			10			μs

Notes 1. The cycle time (minimum instruction execution time) of the CPU clock (Φ) is determined by the oscillation frequency of the connected resonator (and external clock) and the processor clock control register (PCC). The figure at the right indicates the cycle time t_{CY} versus supply voltage V_{DD} characteristic.

2. $2t_{CY}$ or 128/fx is set by setting the interrupt mode register (IM0).



SERIAL TRANSFER OPERATION

2-Wire and 3-Wire Serial I/O Mode ($\overline{SCK}$...Internal clock output): (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 2.7 to 5.5 V		1300			ns
				3800			ns
$\overline{SCK}$ high/low-level width	t_{KL1}, t_{KH1}	V_{DD} = 2.7 to 5.5 V		t_{KCY1}/2–50			ns
				t_{KCY1}/2–150			ns
SI[Note 1] setup time (to $\overline{SCK}\uparrow$)	t_{SIK1}	V_{DD} = 2.7 to 5.5 V		150			ns
				500			ns
SI[Note 1] hold time (from $\overline{SCK}\uparrow$)	t_{KSI1}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
SO[Note 1] output delay time from $\overline{SCK}\downarrow$	t_{KSO1}	R_L = 1 kΩ, C_L = 100 pF [Note 2]	V_{DD} = 2.7 to 5.5 V	0		250	ns
				0		1000	ns

Notes 1. In the 2-wire serial I/O mode, read SB0 or SB1 instead.

2. R_L and C_L are the load resistance and load capacitance of the SO output lines.

2-Wire and 3-Wire Serial I/O Mode ($\overline{SCK}$...External clock input): (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK}$ high/low-level width	t_{KL2}, t_{KH2}	V_{DD} = 2.7 to 5.5 V		400			ns
				1600			ns
SI[Note 1] setup time (to $\overline{SCK}\uparrow$)	t_{SIK2}	V_{DD} = 2.7 to 5.5 V		100			ns
				150			ns
SI[Note 1] hold time (from $\overline{SCK}\uparrow$)	t_{KSI2}	V_{DD} = 2.7 to 5.5 V		400			ns
				600			ns
SO[Note 1] output delay time from $\overline{SCK}\downarrow$	t_{KSO2}	R_L = 1 kΩ, C_L = 100 pF [Note 2]	V_{DD} = 2.7 to 5.5 V	0		300	ns
				0		1000	ns

Notes 1. In the 2-wire serial I/O mode, read SB0 or SB1 instead.

2. R_L and C_L are the load resistance and load capacitance of the SO output lines.

SBI Mode ($\overline{SCK}$...Internal clock output (master)): (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 2.7 to 5.5 V		1300			ns
				3800			ns
$\overline{SCK}$ high/low-level width	t_{KL3}, t_{KH3}	V_{DD} = 2.7 to 5.5 V		t_{KCY3}/2–50			ns
				t_{KCY3}/2–150			ns
SB0, 1 setup time (to $\overline{SCK}$↑)	t_{SIK3}	V_{DD} = 2.7 to 5.5 V		150			ns
				500			ns
SB0, 1 hold time (from $\overline{SCK}$↑)	t_{KSI3}	V_{DD} = 2.7 to 5.5 V		t_{KCY3}/2			ns
SB0, 1 output delay time from $\overline{SCK}$↓	t_{KSO3}	R_L = 1 kΩ,[Note]	V_{DD} = 2.7 to 5.5 V	0		250	ns
		C_L = 100 pF		0		1000	ns
SB0, 1↓ from $\overline{SCK}$↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK}$↓ from SB0, 1↑	t_{SBK}			t_{KCY3}			ns
SB0, 1 low-level width	t_{SBL}			t_{KCY3}			ns
SB0, 1 high-level width	t_{SBH}			t_{KCY3}			ns

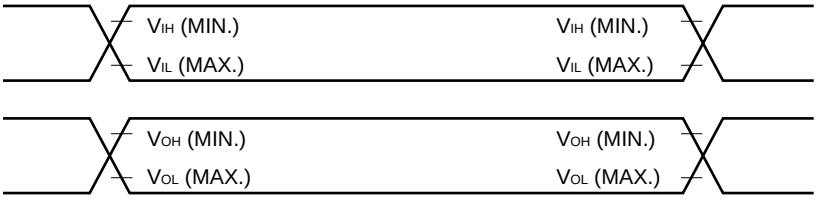
Note R_L and C_L are the load resistance and load capacitance of the SB0 and SB1 output lines.

SBI Mode ($\overline{SCK}$...External clock input (slave)): (T_A = –40 to +85 °C, V_{DD} = 1.8 to 5.5 V)

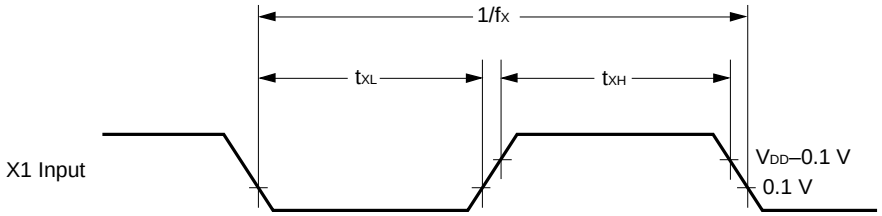
Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 2.7 to 5.5 V		800			ns
				3200			ns
$\overline{SCK}$ high/low-level width	t_{KL4}, t_{KH4}	V_{DD} = 2.7 to 5.5 V		400			ns
				1600			ns
SB0, 1 setup time (to $\overline{SCK}$↑)	t_{SIK4}	V_{DD} = 2.7 to 5.5 V		100			ns
				150			ns
SB0, 1 hold time (from SCK↑)	t_{KSI4}	V_{DD} = 2.7 to 5.5 V		t_{KCY4}/2			ns
SB0, 1 output delay time from $\overline{SCK}$↓	t_{KSO4}	R_L = 1 kΩ,[Note]	V_{DD} = 2.7 to 5.5 V	0		300	ns
		C_L = 100 pF		0		1000	ns
SB0, 1↓ from $\overline{SCK}$↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK}$↓ from SB0, 1↑	t_{SBK}			t_{KCY4}			ns
SB0, 1 low-level width	t_{SBL}			t_{KCY4}			ns
SB0, 1 high-level width	t_{SBH}			t_{KCY4}			ns

Note R_L and C_L are the load resistance and load capacitance of the SB0 and SB1 output lines.

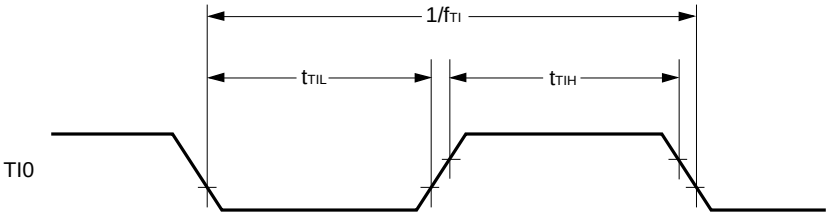
AC Timing Test Point (Excluding X1 Input)



Clock Timing

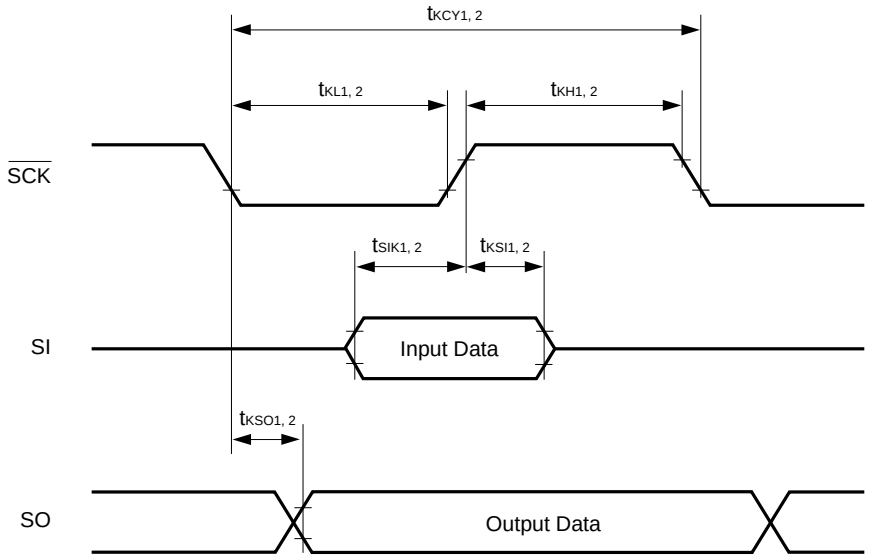


TI0 Timing

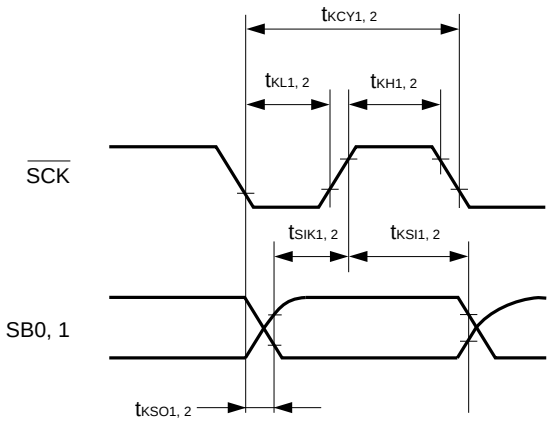


Serial Transfer Timing

3-wire serial I/O mode

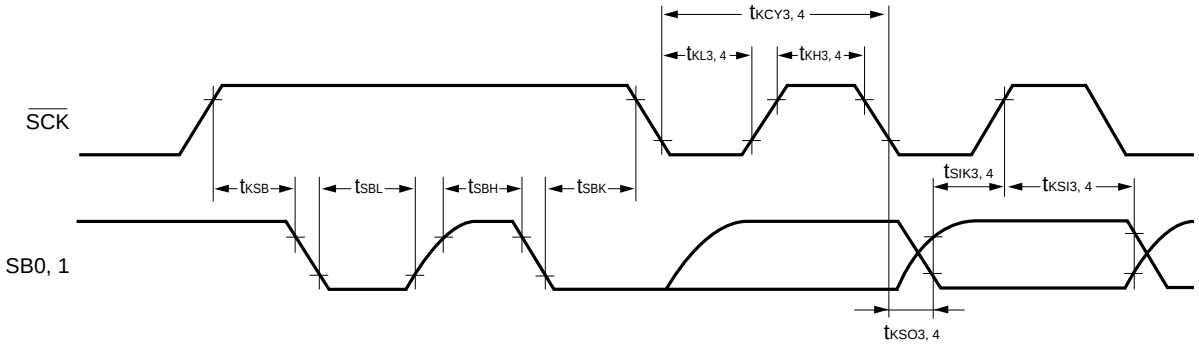


2-wire serial I/O mode

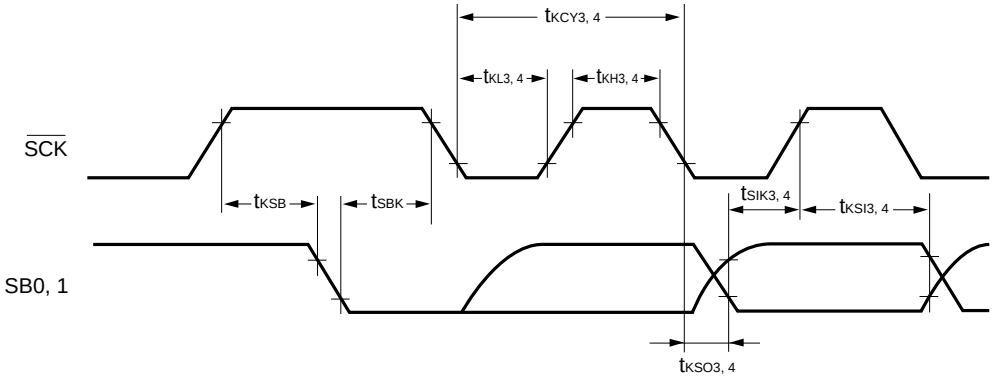


Serial Transfer Timing

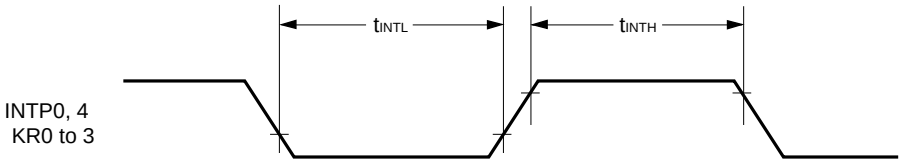
Bus release signal transfer



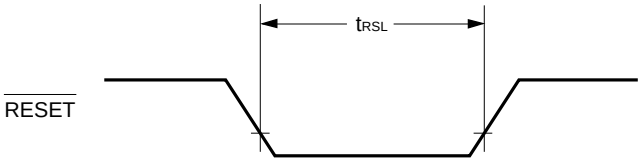
Command signal transfer



Interrupt input timing



RESET input timing



DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS

(T_A = –40 to +85 °C)

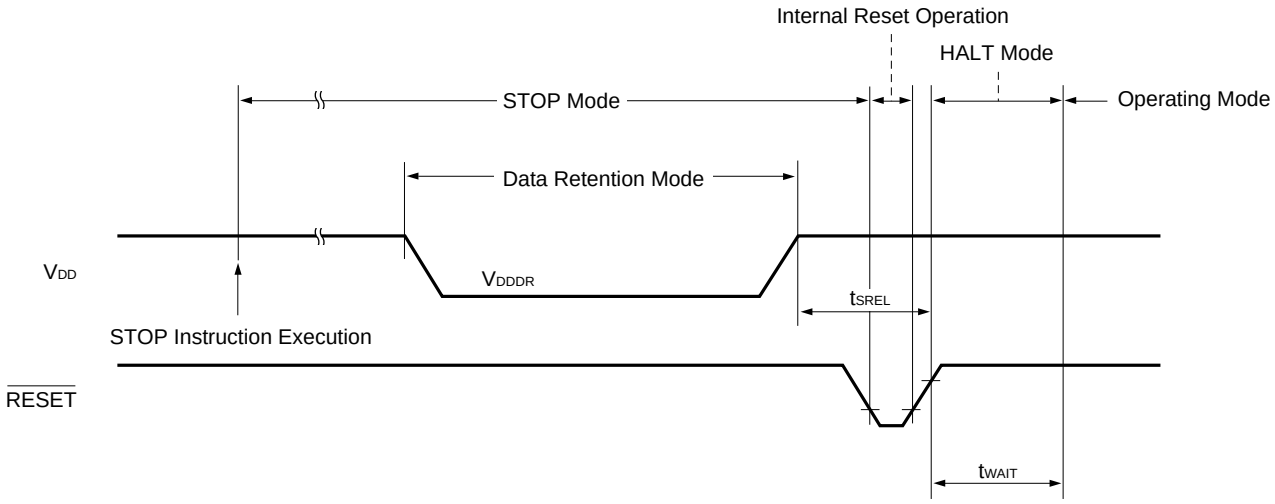
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time Note 1	t_{WAIT}	Release by $\overline{RESET}$		$2^{15}/f_X$		ms
		Release by interrupt		**Note 2**		ms

Notes 1. The oscillation stabillization wait time is the time during which the CPU operation is stopped to prevent unstable operation at the oscillation start.

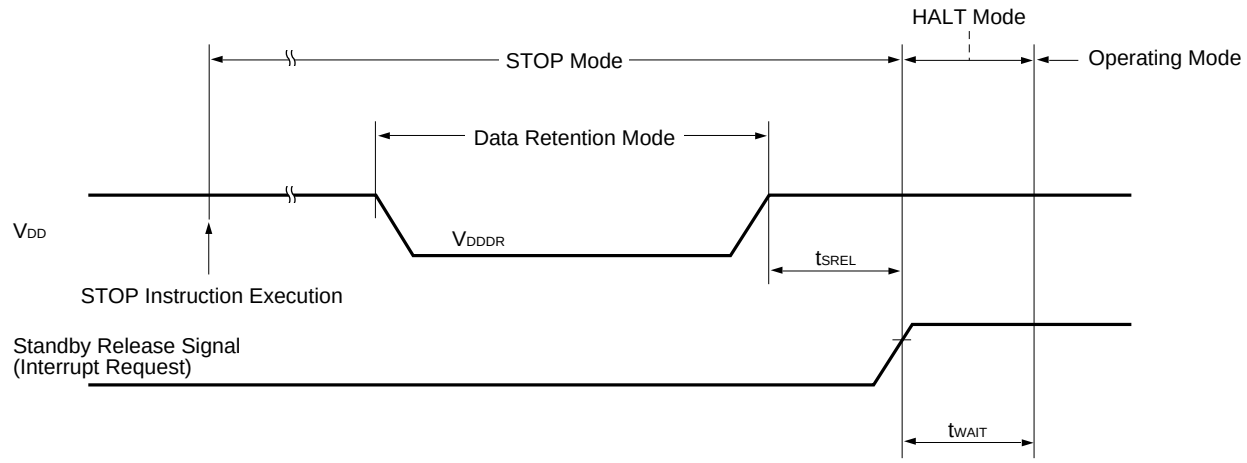
2. Depends on the basic interval timer mode register (BTM) settings (See the table below).

BTM3	BTM2	BTM1	BTM0	Wait Time	
				When fx = 4.19-MHz operation	When fx = 6.0-MHz operation
—	0	0	0	2^{20}/fx (approx. 250 ms)	2^{20}/fx (approx. 175 ms)
—	0	1	1	2^{17}/fx (approx. 31.3 ms)	2^{17}/fx (approx. 21.8 ms)
—	1	0	1	2^{15}/fx (approx. 7.81 ms)	2^{15}/fx (approx. 5.46 ms)
—	1	1	1	2^{13}/fx (approx. 1.95 ms)	2^{13}/fx (approx. 1.37 ms)

Data Retention Timing (STOP Mode Release by $\overline{RESET}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



DC Programming Characteristics (T_A = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	Other than X1, X2 pins	0.7 V_{DD}		V_{DD}	V
	V_{IH2}	X1, X2	V_{DD} – 0.5		V_{DD}	V
Input voltage, low	V_{IL1}	Other than X1, X2 pins	0		0.3 V_{DD}	V
	V_{IL2}	X1, X2	0		0.4	V
Input leakage current	I_{LI}	V_{IN} = V_{IL} or V_{IH}			10	μA
Output voltage, high	V_{OH}	I_{OH} = – 1 mA	V_{DD} – 1.0			V
Output voltage, low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
V_{DD} supply current	I_{DD}				30	mA
V_{PP} supply current	I_{PP}	MD0 = V_{IL}, MD1 = V_{IH}			30	mA

Cautions 1. Keep V_{PP} to within +13.5 V, including overshoot.

2. Apply V_{DD} before V_{PP} and turn it off after V_{PP}.

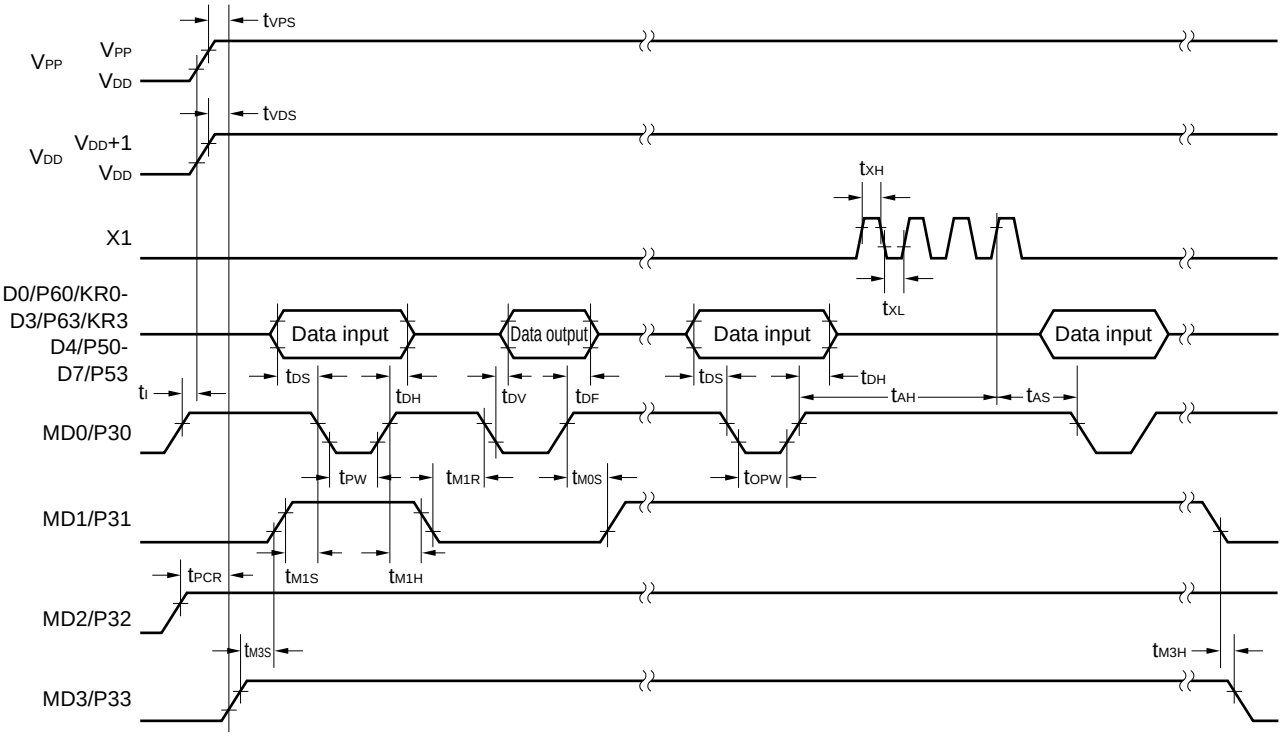
AC Programming Characteristics (T_A = 25 ± 5 °C, V_{DD} = 6.0 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	**Note 1**	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time **Note 2** (vs. MD0 ↓)	t_{AS}	t_{AS}		2			μs
MD1 setup time (vs. MD0 ↓)	t_{M1S}	t_{OES}		2			μs
Data setup time (vs. MD0 ↓)	t_{DS}	t_{DS}		2			μs
Address hold time **Note 2** (vs. MD0 ↑)	t_{AH}	t_{AH}		2			μs
Data hold time (vs. MD0 ↑)	t_{DH}	t_{DH}		2			μs
MD0 ↑ → data output float delay time	t_{DF}	t_{DF}		0		130	ns
V_{PP} setup time (vs. MD3 ↑)	t_{VPS}	t_{VPS}		2			μs
V_{DD} setup time (vs. MD3 ↑)	t_{VDS}	t_{VCS}		2			μs
Initial program pulse width	t_{PW}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}	t_{OPW}		0.95		21.0	ms
MD0 setup time (vs. MD1 ↑)	t_{M0S}	t_{CES}		2			μs
MD0 ↓ → data output delay time	t_{DV}	t_{DV}	MD0 = MD1 = V_{IL}			1	μs
MD1 hold time (vs. MD0 ↑)	t_{M1H}	t_{OEH}	t_{M1H} + t_{M1R} ≥ 50 μs	2			μs
MD1 recovery time (vs. MD0 ↓)	t_{M1R}	t_{OR}		2			μs
Program counter reset time	t_{PCR}	—		10			μs
X1 input high-, low-level width	t_{XH}, t_{XL}	—		0.125			μs
X1 input frequency	f_X	—				4.19	MHz
Initial mode set time	t_1	—		2			μs
MD3 setup time (vs. MD1 ↑)	t_{M3S}	—		2			μs
MD3 hold time (vs. MD1 ↓)	t_{M3H}	—		2			μs
MD3 setup time (vs. MD0 ↓)	t_{M3SR}	—	When program memory is read	2			μs
Address **Note 2** → data output delay time	t_{DAD}	t_{ACC}	When program memory is read			2	μs
Address **Note 2** → data output hold time	t_{HAD}	t_{OH}	When program memory is read	0		130	ns
MD3 hold time (vs. MD0 ↑)	t_{M3HR}	—	When program memory is read	2			μs
MD3 ↓ → data output float delay time	t_{DFR}	—	When program memory is read			2	μs

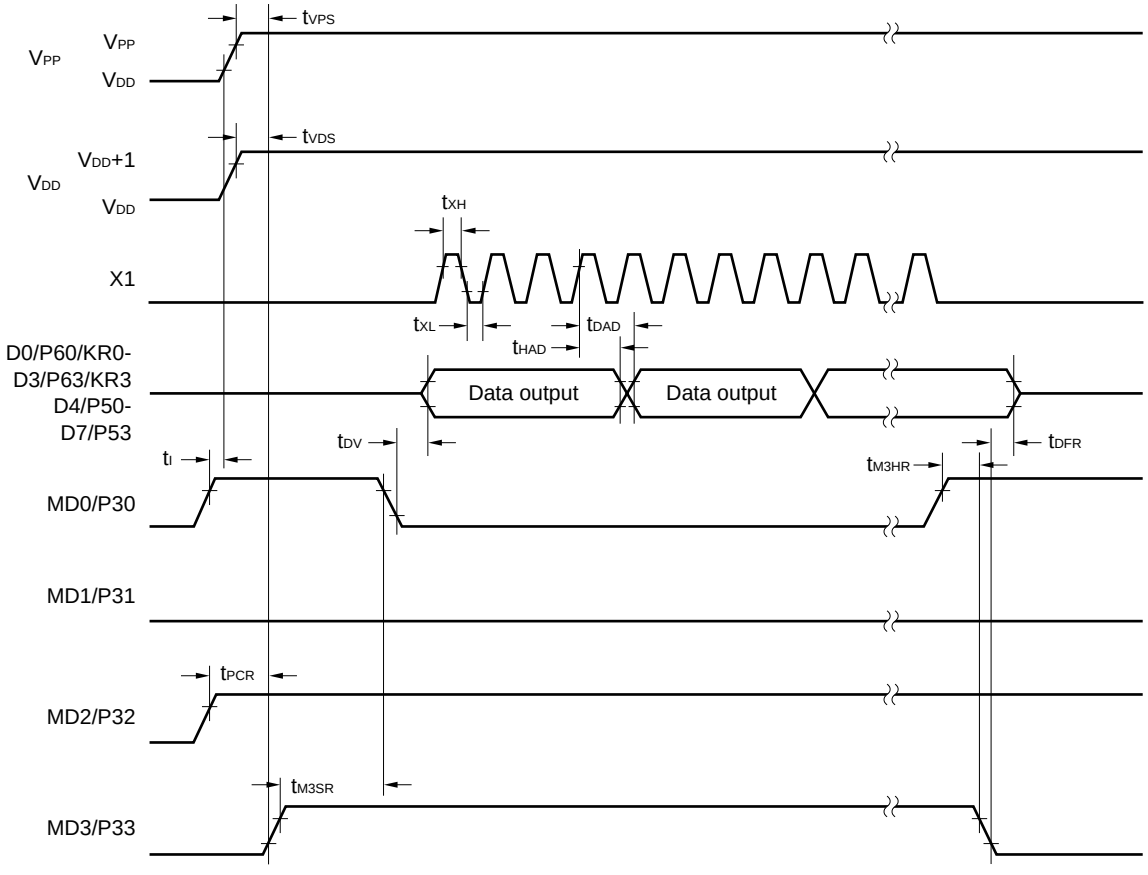
Notes 1. Symbol of corresponding μPD27C256A

2. The internal address signal is incremented by one at the rising edge of the fourth X1 input and is not connected to a pin.

Program Memory Write Timing

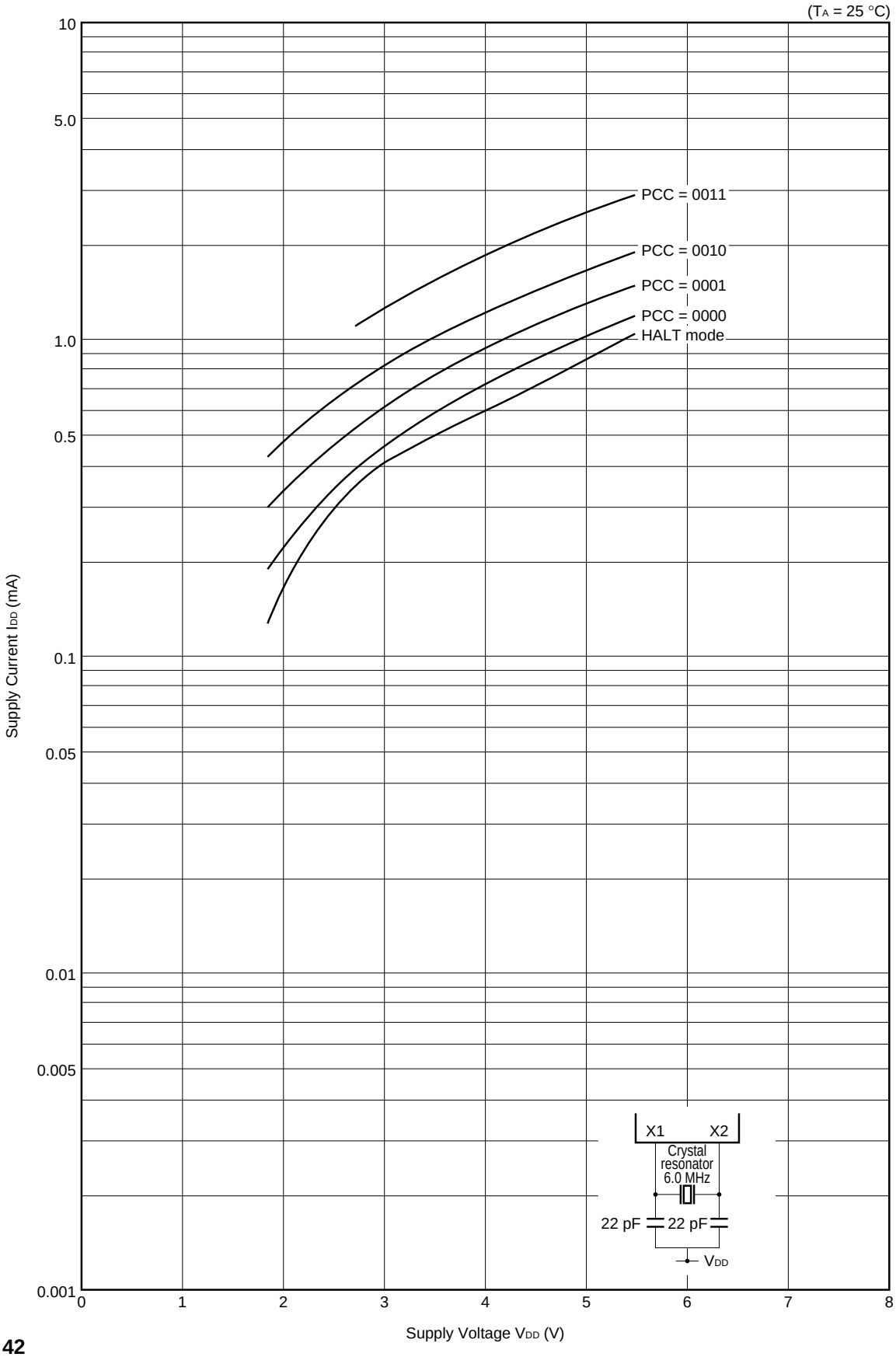


Program Memory Read Timing



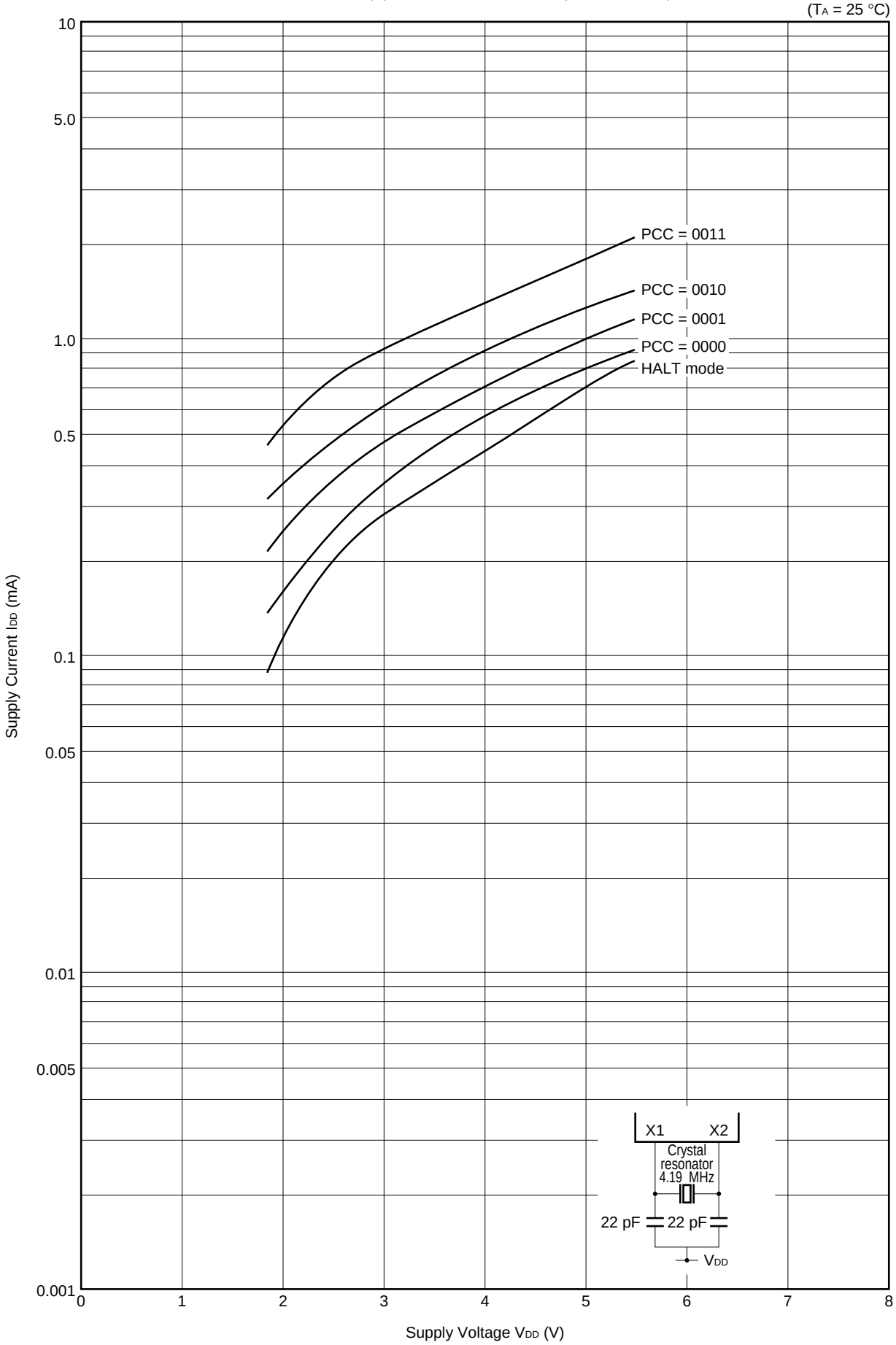
★ 10. CHARACTERISTIC CURVE (REFERENCE VALUE)

I_{DD} vs V_{DD} (System clock : 6.0 MHz Crystal resonator)



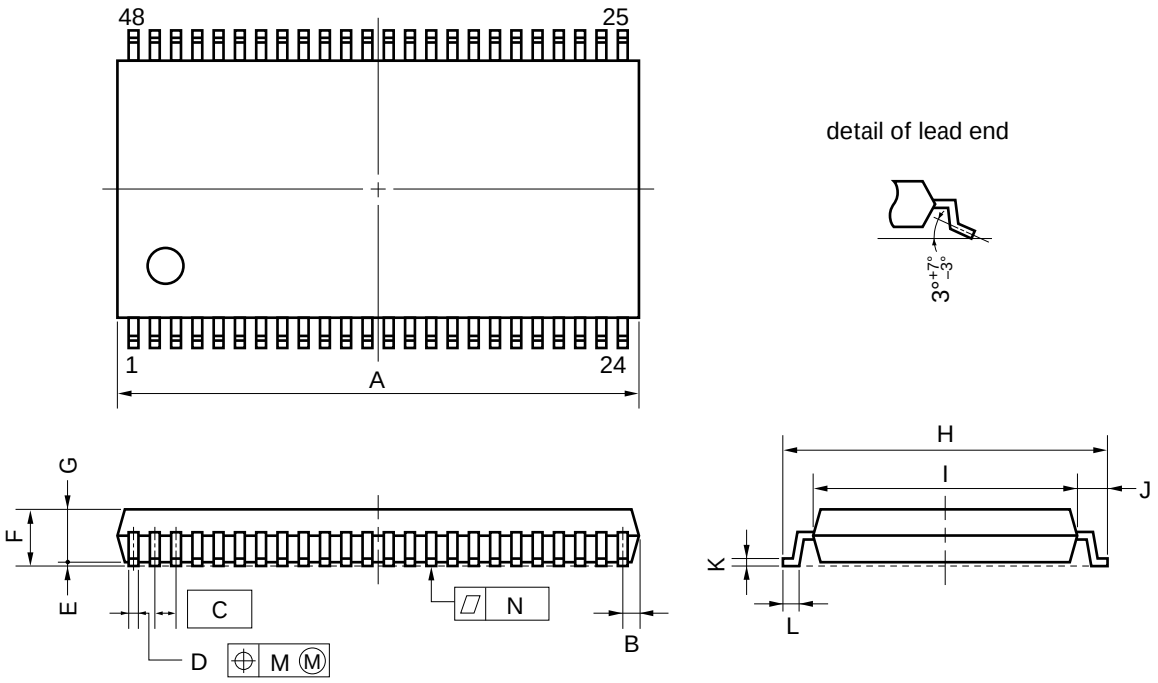
I_{DD} vs V_{DD} (System clock : 4.19 MHz Crystal resonator)

(T_A = 25 °C)



11. PACKAGE DRAWINGS

48 PIN PLASTIC SHRINK SOP (375 mil)



P48GT-65-375B-1

NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.21 MAX.	0.639 MAX.
B	0.63 MAX.	0.025 MAX.
C	0.65 (T.P.)	0.026 (T.P.)
D	0.30±0.10	$0.012^{+0.004}_{-0.005}$
E	0.125±0.075	0.005±0.003
F	2.0 MAX.	0.079 MAX.
G	1.7±0.1	0.067±0.004
H	10.0±0.3	$0.394^{+0.012}_{-0.013}$
I	8.0±0.2	0.315±0.008
J	1.0±0.2	$0.039^{+0.009}_{-0.008}$
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	0.10	0.004
N	0.10	0.004

★ 12. RECOMMENDED SOLDERING CONDITIONS

The μPD75P3216 should be soldered and mounted under the conditions recommended in the table below.

For details of recommended soldering conditions, refer to the information document **"Semiconductor Device Mounting Technology Manual" (C10535E).**

For soldering methods and conditions other than those recommended below, contact an NEC Sales representative.

Table 12-1. Surface Mounting Type Soldering Conditions

μPD75P3216GT: 48-pin plastic shrink SOP (375 mil, 0.65-mm pitch)

Soldering Method	Soldering Conditions	Symbol
Infrared rays reflow	Peak package's surface temperature: 235 ˚C, Reflow time: 30 seconds or less (at 210 ˚C or higher), Number of reflow processes: Twice max. Number of days: 7[Note] (after that, prebaking is necessary at 125 °C for 10 hours) <Precaution> Products other than those supplied in thermal-resistant tray (magazine, taping, and non-thermal-resistant tray) cannot be baked in their packs.	IR35-107-2
VPS	Peak package's surface temperature: 215 ˚C, Reflow time: 40 seconds or less (at 200 ˚C or higher), Number of reflow processes: Twice max. Number of days: 7[Note] (after that, prebaking is necessary at 125 °C for 10 hours) <Precaution> Products other than those supplied in thermal-resistant tray (magazine, taping, and non-thermal-resistant tray) cannot be baked in their packs.	VP15-107-2
Wave soldering	Solder temperature: 260 ˚C or below, Flow time: 10 seconds or less, Number of flow process: 1, Preheating temperature: 120 ˚C or below (Package surface temperature) Number of days: 7[Note] (after that, prebaking is necessary at 125 °C for 10 hours)	WS60-107-1
Partial heating	Pin temperature: 300 ˚C or below, Time: 3 seconds or less (per device side)	—

Note The number of days during which the product can be stored at 25 °C, 65 % RH max. after the dry pack has been opened.

Caution Use of more than one soldering method should be avoided (except for partial heating).

★ APPENDIX A. μPD753108, 753208, AND 75P3216 FUNCTIONAL LIST

Parameter		μPD753108	μPD753208	μPD75P3216
Program memory		Mask ROM 0000H-1FFFH (8192 × 8 bits)		One-time PROM 0000H-3FFFH (16384 × 8 bits)
Data memory		000H-1FFH (512 × 4 bits)		
CPU		75XL CPU		
Instruction execution time	When main system clock is selected	• 0.95, 1.91, 3.81, 15.3 μs (@ 4.19-MHz operation) • 0.67, 1.33, 2.67, 10.7 μs (@ 6.0-MHz operation)		
	When subsystem clock is selected	122 μs (@ 32.768-kHz operation)	None	
I/O port	CMOS input	8 (on-chip pull-up resistors can be specified by software: 7)	6 (on-chip pull-up resistors can be specified by software: 5)	
	CMOS input/output	20 (on-chip pull-up resistors can be specified by software)		
	N-ch open drain input/output	4 (on-chip pull-up resistors can be specified by software, withstand voltage is 13 V)		4 (no mask option, withstand voltage is 13 V)
	Total	32	30	
LCD controller/driver		Segment selection: 16/20/24 (can be changed to CMOS input/output port in 4 time-unit; max. 8)	Segment selection: 4/8/12 segments (can be changed to CMOS input/output port in 4 time-unit; max. 8)	
		Display mode selection: static, 1/2 duty (1/2 bias), 1/3 duty (1/2 bias), 1/3 duty (1/3 bias), 1/4 duty (1/3 bias)		
		On-chip split resistor for LCD driver can be specified by using mask option.		No on-chip split resistor for LCD driver
Timer		5 channels • 8-bit timer/event counter: 3 channels (Can be used as 16-bit timer/event counter, carrier generator, timer with gate) • Basic interval timer/ watchdog timer: 1 channel • Watch timer: 1 channel	5 channels • 8-bit timer counter: 2 channels (Can be used as 16-bit timer counter, carrier generator, timer with gate) • 8-bit timer/event counter: 1 channel • Basic interval timer/watchdog timer: 1 channel • Watch timer: 1 channel	
Clock output (PCL)		• Φ, 524, 262, 65.5 kHz (Main system clock: @ 4.19-MHz operation) • Φ, 750, 375, 93.8 kHz (Main system clock: @ 6.0-MHz operation)		
Buzzer output (BUZ)		• 2, 4, 32 kHz (Main system clock: @ 4.19-MHz operation or sub-system clock: @ 32.768-kHz operation) • 2.86, 5.72, 45.8 kHz (Main system clock: @ 6.0-MHz operation)	• 2, 4, 32 kHz (Main system clock: @ 4.19-MHz operation) • 2.93, 5.86, 46.9 kHz (Main system clock: @ 6.0-MHz operation)	
Serial interface		3 modes are available • 3-wire serial I/O mode ... MSB/LSB can be selected for transfer top bit • 2-wire serial I/O mode • SBI mode		
SCC register		Contained	None	
SOS register				
Vectored interrupt		External: 3, internal: 5	External: 2, internal: 5	

Parameter	μPD753108	μPD753208	μPD75P3216
Test input	External: 1, internal: 1		
Operation supply voltage	V_{DD} = 1.8 to 5.5 V		
Operating ambient temperature	T_A = –40 to +85°C		
Package	• 64-pin plastic QFP (14 × 14 mm) • 64-pin plastic QFP (12 × 12 mm)	• 48-pin plastic shrink SOP (375 mil, 0.65-mm pitch)	

APPENDIX B. DEVELOPMENT TOOLS

The following development tools have been provided for system development using the μPD75P3216.

In the 75XL series, relocatable assemblers common to the series can be used in combination with the device files for each product type.

RA75X relocatable assembler	Host machine			Part No. (name)
		OS	Supply medium	
	PC-9800 Series	MS-DOS™ (Ver.3.30 to Ver.6.2[Note])	3.5” 2HD	μS5A13RA75X
			5” 2HD	μS5A10RA75X
	IBM PC/AT™ or compatible	Refer to **“OS for IBM PCs”**	3.5” 2HC	μS7B13RA75X
			5” 2HC	μS7B10RA75X

Device file	Host machine			Part No. (name)
		OS	Supply medium	
	PC-9800 Series	MS-DOS™ (Ver.3.30 to Ver.6.2[Note])	3.5” 2HD	μS5A13DF753208
			5” 2HD	μS5A10DF753208
	IBM PC/AT or compatible	Refer to **“OS for IBM PCs”**	3.5” 2HC	μS7B13DF753208
			5” 2HC	μS7B10DF753208

Note Ver. 5.00 or later includes a task swapping function, but this software is not able to use that function.

Remark Operation of the PG-1500 controller is guaranteed only when using the host machine and OS described above.

PROM Write Tools

<table>
<tr><td rowspan="2">Hardware</td><td>PG-1500</td><td colspan="4">This is a PROM programmer that can program single-chip microcomputer with PROM in stand alone mode or under control of host machine when connected with supplied accessory board and optional programmer adapter.
It can also program typical PROMs in capacities ranging from 256 K to 4 M bits.</td></tr>
<tr><td>PA-75P3216GT</td><td colspan="4">This is a PROM programmer adapter for the μPD75P3216GT.
It can be used when connected to a PG-1500.</td></tr>
<tr><td rowspan="6">Software</td><td rowspan="6">PG-1500 controller</td><td colspan="4">Connects PG-1500 to host machine with serial and parallel interface and controls PG-1500 on host machine.</td></tr>
<tr><td rowspan="2">Host machine</td><td colspan="2" rowspan="2">OS</td><td>Supply medium</td><td rowspan="2">Part No. (name)</td></tr>
<tr><td>Supply medium</td></tr>
<tr><td>PC-9800 Series</td><td colspan="2">MS-DOS
(Ver.3.30 to Ver.6.2^{Note})</td><td>3.5” 2HD</td><td>μS5A13PG1500</td></tr>
<tr><td>PC-9800 Series</td><td colspan="2">MS-DOS
(Ver.3.30 to Ver.6.2^{Note})</td><td>5” 2HD</td><td>μS5A10PG1500</td></tr>
<tr><td>IBM PC/AT or compatible</td><td colspan="2">Refer to “OS for IBM PCs”</td><td>3.5” 2HD</td><td>μS7B13PG1500</td></tr>
<tr><td>IBM PC/AT or compatible</td><td colspan="2">Refer to “OS for IBM PCs”</td><td>5” 2HC</td><td>μS7B10PG1500</td></tr>
</table>

Note Ver. 5.00 or later includes a task swapping function, but this software is not able to use that function.

Remark Operation of the PG-1500 controller is guaranteed only when using the host machine and OS described above.

Debugging Tools

In-circuit emulators (IE-75000-R and IE-75001-R) are provided as program debugging tools for the μPD75P3216. Various system configurations using these in-circuit emulators are listed below.

Hardware	IE-75000-R[Note 1]	The IE-75000-R is an in-circuit emulator to be used for hardware and software debugging during development of application systems using the 75X or 75XL Series products. For development of the μPD753208 subseries, the IE-75000-R is used with optional emulation board (IE-75300-R-EM) and emulation probe (EP-753208GT-R). Highly efficient debugging can be performed when connected to host machine and PROM programmer. The IE-75000-R includes a connected emulation board (IE-75000-R-EM).			
	IE-75001-R	The IE-75001-R is an in-circuit emulator to be used for hardware and software debugging during development of application systems using the 75X or 75XL Series products. The IE-75001-R is used in combination with optional emulation board (IE-75300-R-EM) and emulation probe (EP-753208GT-R). Highly efficient debugging can be performed when connected to host machine and PROM programmer.			
	IE-75300-R-EM	This is an emulation board for evaluating application systems using the μPD75P3216. It is used in combination with the IE-75000-R or IE-75001-R.			
	EP-753208GT-R	This is an emulation probe for the μPD75P3216GK. When being used, it is connected with the IE-75000-R or IE-75001-R and the IE-75300-R-EM.			
	EV-9500GT-48	It includes a flexible board (EV-9500GT-48) to facilitate connections with target system.			
Software	IE control program	This program can control the IE-75000-R or IE-75001-R on a host machine when connected to the IE-75000-R or IE-75001-R via an RS-232-C or Centronics interface.			
		Host machine			Part No. (name)
			OS	Supply medium	
		PC-9800 Series	MS-DOS (Ver.3.30 to Ver.6.2[Note 2])	3.5” 2HD	μS5A13IE75X
				5” 2HD	μS5A10IE75X
		IBM PC/AT or compatible	Refer to **“OS for IBM PCs”**	3.5” 2HC	μS7B13IE75X
				5” 2HC	μS7B10IE75X

Notes 1. This is a maintenance product.

2. Ver. 5.00 or later includes a task swapping function, but this software is not able to use that function.

Remarks 1. Operation of the IE control program is guaranteed only when using the host machine and OS described above.

2. The generic name for the μPD753204, 753206, 753208, and 75P3216 is the μPD753208 subseries.

OS for IBM PCs

The following operating systems for the IBM PC are supported.

OS	Version
PC DOS™	Ver.5.02 to Ver.6.3 J6.1/V[Note] to J6.3/V[Note]
MS-DOS	Ver.5.0 to Ver.6.22 5.0/V[Note] to 6.2/V[Note]
IBM DOS™	J5.02/V[Note]

Note Only English version is supported.

Caution Ver. 5.0 or later include a task swapping function, but this software is not able to use that function.

APPENDIX C. RELATED DOCUMENTS

Some of the related documents are preliminary but are not marked as such.

Device related documents

Document Name	Document Number	
	Japanese	English
μPD753204, 753206, 753208 preliminary product information	U10166J	U10166E
μPD75P3216 data sheet	U10241J	This document
μPD753208 user's manual	U10158J	U10158E
75XL series selection guide	U10453J	U10453E

Development tool related documents

Document Name			Document Number	
			Japanese	English
Hardware	IE-75000-R/IE-75001-R user's manual		EEU-846	EEU-1416
	IE-75300-R-EM user's manual		U11354J	U11354E
	EP-753208GT-R user's manual		U10739J	U10739E
	PG-1500 user's manual		EEU-651	EEU-1335
Software	RA75X assembler package user's manual	Operation	EEU-731	EEU-1346
		Language	EEU-730	EEU-1363
	PG-1500 controller user's manual	PC-9800 series (MS-DOS) base	EEU-704	EEU-1291
		IBM PC series (PC DOS) base	EEU-5008	U10540E

Other related documents

Document Name	Document Number	
	Japanese	English
IC package manual	C10943X	
Semiconductor device mounting technology manual	C10535J	C10535E
Quality grade on NEC semiconductor devices	C11531J	C11531E
NEC semiconductor device reliability/quality control system	C10983J	C10983E
Static electricity discharge (ESD) test	MEM-539	–
Semiconductor device quality guarantee guide	MEI-603	MEI-1202
Microcomputer related product guide - other manufacturers	U11416J	–

Caution The related documents listed above are subject to change without notice. Be sure to use the latest documents for designing, etc.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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Fax: 800-729-9288

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Fax: 0211-65 03 490

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Fax: 250-3583

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NEC do Brasil S.A.
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[MEMO]

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