NEC

MOS INTEGRATED CIRCUIT

μPD75P116

4-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD75P116 is a version of the μPD75116 in which the on-chip mask ROM is replaced by one-time PROM which can be written to once only.

Since the μPD75P116 is capable of program write by a user, it is suitable for evaluation in system development and limited production.

Detailed functional descriptions are shown in the following User's Manual. Be sure to read for design purposes.

μPD751×× Series User's Manual : IEM-922

FEATURES

- μPD75116 compatible
- Program memory (PROM) capacitance : 16256 × 8 bits
- Data memory (RAM) capacitance : 512 × 4 bits
- Single power supply 5 V ± 10%

ORDERING INFORMATION

Ordering Code	Package	Quality Grade	★
μPD75P116CW	64-pin plastic shrink DIP (750 mil)	Standard	
μPD75P116GF-3BE	64-pin plastic QFP (14 × 20 mm)	Standard	

Please refer to "Quality Grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Note There are no on-chip pull-up resistor and power-on reset function by means of a mask option.

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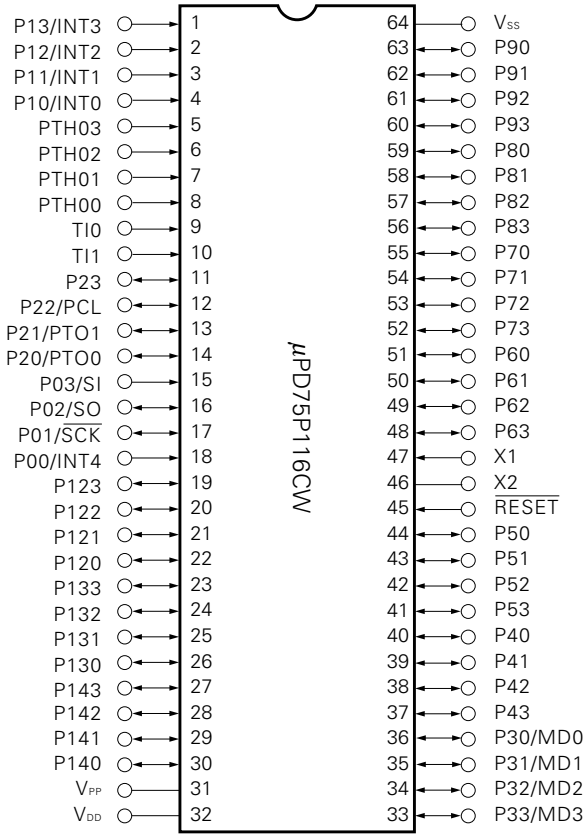
Date Published February 1994 P
Printed in Japan

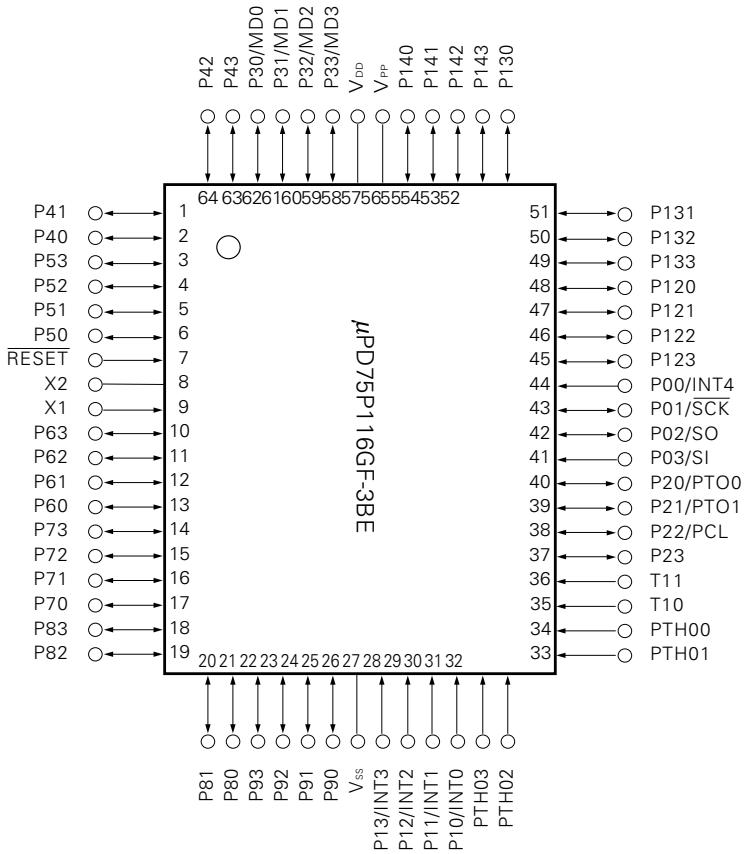
The mark ★ shows major revised points.

PIN CONFIGURATION (TOP VIEW)

64-pin plastic shrink DIP (750 mil)



64-pin plastic QFP (14 × 20 mm)



Pin Name

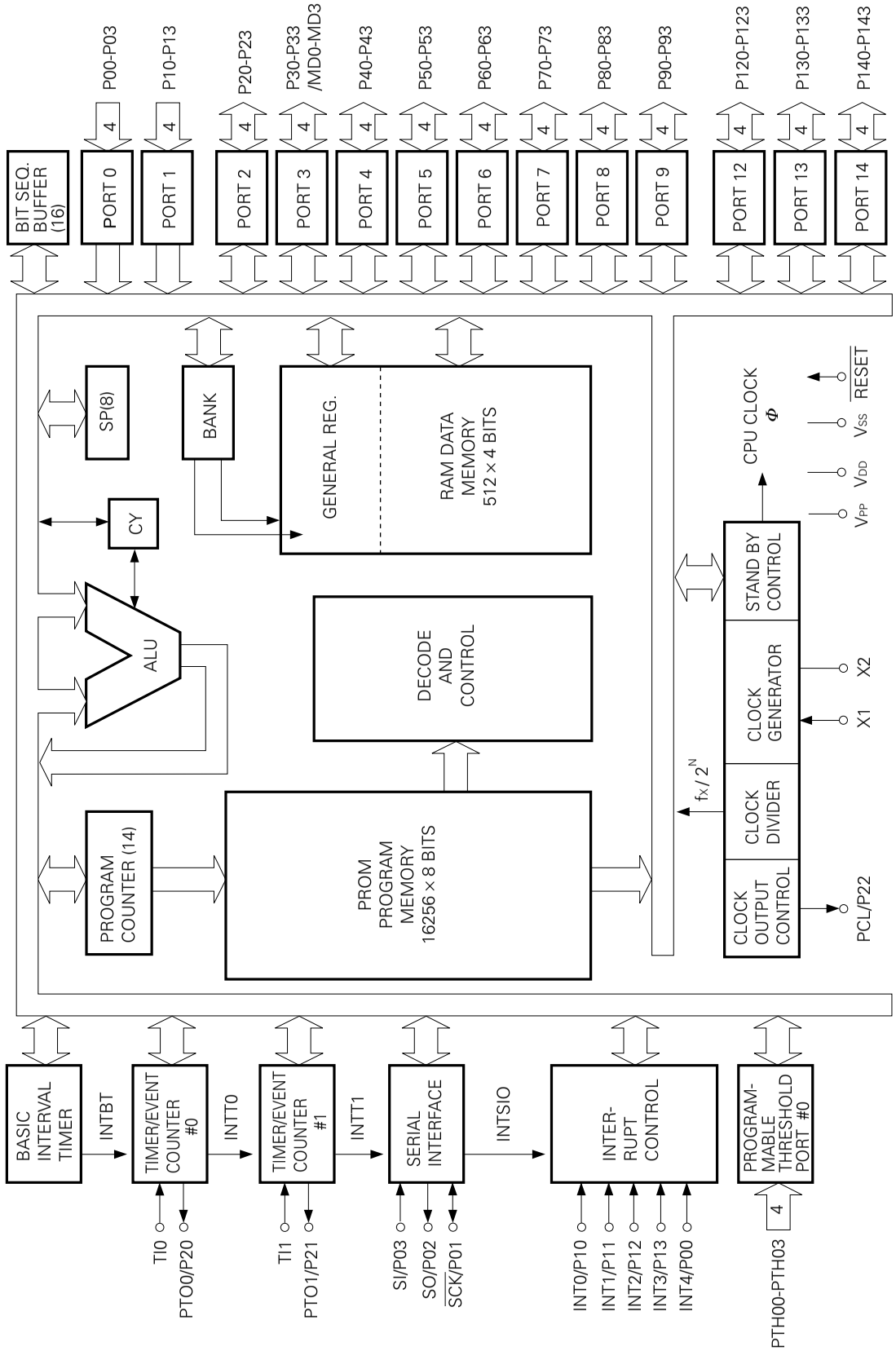
P00 to P03 : Port 0
P10 to P13 : Port 1
P20 to P23 : Port 2
P30 to P33 : Port 3
P40 to P43 : Port 4
P50 to P53 : Port 5
P60 to P63 : Port 6
P70 to P73 : Port 7
P80 to P83 : Port 8
P90 to P93 : Port 9
P120 to P123 : Port 12
P130 to P133 : Port 13
P140 to P143 : Port 14

$\overline{\text{SCK}}$	: Serial Clock
SO	: Serial Output
SI	: Serial Input
PTO0, PTO1	: Programmable Timer Output
PCL	: Clock Output
PTH00 to PTH03	: Programmable Threshold Input
INT0, INT1, INT4	: External Vectored Interrupt Input
INT2, INT3	: External Test Input
TI0, TI1	: Timer Input
X1, X2	: Clock Oscillation
$\overline{\text{RESET}}$	: Reset
NC	: No Connection
V_{DD}	: Positive Power Supply
V_{SS}	: Ground
V_{PP}	: Programming Power Supply
MD0 to MD3	: Mode Selection

OVERVIEW OF FUNCTIONS

Item		Description
Basic instructions		43
Minimum instruction execution time		0.95 μs, 1.91 μs, 15.3 μs (4.19 MHz operation) 3-stage switching capability
Internal memory	ROM	16256 × 8
	RAM	512 × 4
General register		4 bits × 8 × 4 banks (memory mapping)
Accumulator		3 types of accumulators corresponding to bit length of manipulated data • 1-bit accumulator (CY), 4-bit accumulator (A), 8-bit accumulator (XA)
Input/output port		Total 58 • CMOS input pins : 10 • CMOS input/output pins (LED direct drive capability) : 32 • Middle-high voltage N-ch open-drain input/output pins (LED direct drive capability) : 12 • Comparator input pins (4-bit precision) : 4
Timer/counter		• 8-bit timer/event counter × 2 • 8-bit basic interval timer (watchdog timer applicable)
Serial interface		• 8 bits • LSB-first/MSB-first switchable • Two transfer modes (transmit-receive/receive-only mode)
Vectored interrupt		External : 3, internal : 4
Test input		External : 2
Standby		• STOP/HALT mode
Instruction set		• Various bit manipulation instructions (set, reset, test, boolean operation) • 8-bit data transfer, comparison, operation, increment/decrement instructions • 1-byte relative branch instruction • GETI instruction that can implement arbitrary 2-byte/3-byte instructions with 1 byte
Operating temperature range		–40 to +85 °C
Operating voltage		5 V ± 10 %
Others		• Bit manipulation memory (bit sequential buffer : 16 bits) on-chip
Package		• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 20mm)

BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

1.1 PORT PINS

Pin Name	Input/Output	Dual-Function Pin	Function	8-bit I/O	After Reset	I/O Circuit Type *1
P00	Input	INT4	4-bit input port (PORT 0).	×	Input	Ⓑ
P01	Input/output	$\overline{SCK}$				Ⓕ
P02	Input/output	SO				E
P03	Input	SI				Ⓑ
P10	Input	INT0	4-bit input port (PORT 1).		Input	Ⓑ
P11		INT1				
P12		INT2				
P13		INT3				
P20	Input/output	PTO0	4-bit input/output port (PORT 2). *2		Input	E
P21		PTO1				
P22		PCL				
P23		—				
P30 to P33	Input/output	MD0 to MD3	Programmable 4-bit input/output port (PORT 3). Input/output can be specified bit-wise. *2		Input	E
P40 to P43	Input/output	—	4-bit input/output port (PORT 4). Data input/output pin for program memory (PROM) write/verify (low-order 4 bits). *2	○	Input	E
P50 to P53	Input/output	—	4-bit input/output port (PORT 5). Data input/output pin for program memory (PROM) write/verify (high-order 4 bits). *2		Input	E
P60 to P63	Input/output	—	Programmable 4-bit input/output port (PORT 6). Input/output can be specified bit-wise. *2	○	Input	E
P70 to P73	Input/output	—	4-bit input/output port (PORT 7). *2		Input	E
P80 to P83	Input/output	—	4-bit input/output port (PORT 8). *2	○	Input	E
P90 to P93	Input/output	—	4-bit input/output port (PORT 9). *2		Input	E
P120-P123	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 12). +12 V withstand voltage. *2	○	Input	M-A
P130-P133	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 13). +12 V withstand voltage. *2		Input	M-A
P140-P143	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 14). +12 V withstand voltage. *2	—	Input	M-A

* **1.** ○ indicates Schmitt-triggered input.
2. LED direct drive capability

1.2 OTHER PINS

Pin Name	Input/Output	Dual-Function Pin	Function	After Reset	I/O Circuit Type *1
PTH00 to PTH03	Input	—	Variable threshold voltage 4-bit analog input port.		N
TI0	Input	—	External event pulse input to timer/event counter. Or edge detection vectored interrupt input pin, or 1-bit input is also possible.		Ⓑ
TI1					
PTO0	Input/output	P20	Timer/event counter output pin.	Input	E
PTO1		P21			
$\overline{SCK}$	Input/output	P01	Serial clock input/output pin.	Input	Ⓕ
SO	Input/output	P02	Serial data output pin.	Input	E
SI	Input	P03	Serial data input pin.	Input	Ⓑ
INT4	Input	P00	Edge detection vector interrupt input pin (detection of both rising and falling edges).		Ⓑ
INT0	Input	P10	Edge detection vector interrupt input pin (detection edge selectable).		Ⓑ
INT1		P11			
INT2	Input	P12	Edge detection testable input pin (rising edge detection)		Ⓑ
INT3		P13			
PCL	Input/output	P22	Clock output pin	Input	E
X1, X2		—	System clock oscillation crystal/ceramic connection pin. When an external clock is used, the clock is input to X1 and the inverted clock is input to X2.		
$\overline{RESET}$	Input	—	System reset input pin (low-level active).		Ⓑ
MD0 to MD3	Input/output	P30 to P33	Mode selection pin for program memory (PROM) write/verify.	Input	E
V_{DD}		—	Positive power supply pin. Applies +6 V for write/verify.		
V_{SS}		—	GND potential pin.		
V_{PP} *2		—	Program voltage impression pin for program memory (PROM) write/verify. Connected to V_{DD} directly in normal operation. Applies +12.5 V for PROM write/verify.		

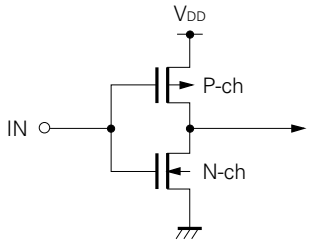
* **1.** ○ indicates Schmitt-triggered input.

2. The device will not operate correctly unless V_{PP} is connected to V_{DD} directly in normal use.

1.3 PIN INPUT/OUTPUT CIRCUITS

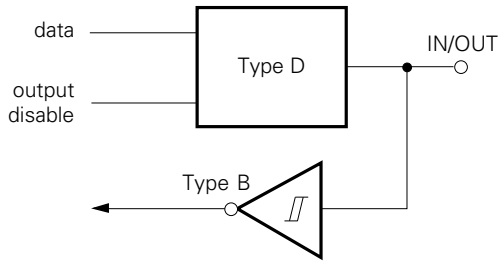
The input/output circuits of each pin of the μPD75P116 are shown by in abbreviated form.

Type A



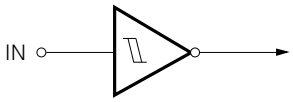
CMOS specification input buffer

Type F



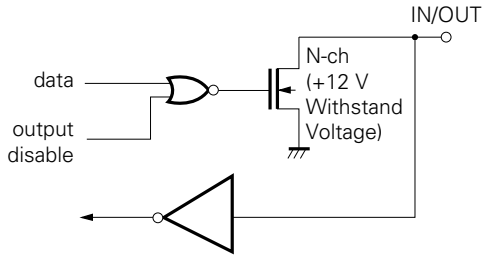
Input/output circuit made up to a Type D push-pull output and Type B Schmitt-triggered input.

Type B



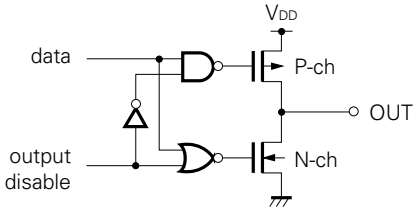
Schmitt-triggered input with hysteresis characteristic

Type M-A



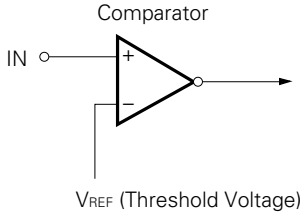
Middle-High Voltage Input Buffer
(+12 V Withstand Voltage)

Type D



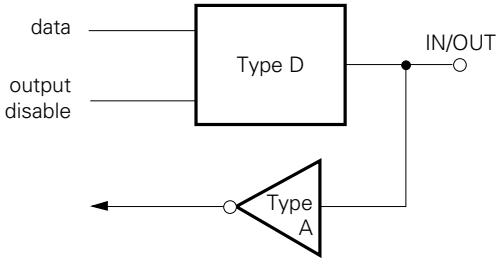
Push-pull output with high impedance output capability
(P-ch and N-ch both OFF)

Type N



VREF (Threshold Voltage)

Type E



This is an input/output circuit made up of a Type D push-pull output and Type A input buffer.

1.4 RECOMMENDED CONNECTION OF μPD75P116 UNUSED PINS

Pin	Recommended Connection
PTH00 to PTH03 TI0 TI1	Connect to V_{SS} or V_{DD}.
P00	Connect to V_{SS}.
P01 to P03	Connect to V_{SS} or V_{DD}.
P10 to P13	Connect to V_{SS}.
P20 to P23 P30 to P33 P40 to P43 P50 to P53 P60 to P63 P70 to P73 P80 to P83 P90 to P93 P120 to P123 P130 to P133 P140 to P143	Input status : Connect to V_{SS} or V_{DD}. Output status : Leave open.

1.5 NOTES ON USING P00/INT4 PIN AND $\overline{\text{RESET}}$ PIN

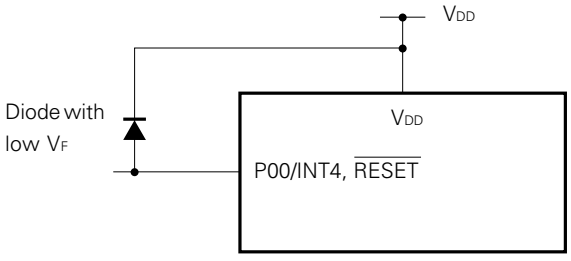
The P00/INT4 and $\overline{\text{RESET}}$ pins have a test mode setting function (for IC test) which tests internal operations of pin of the μPD75P116 in addition to those functions given in 1.1 and 1.2.

The test mode is set when voltage greater than V_{DD} is applied to either pin. Therefore, even during normal operation, the test mode is engaged when noise greater than V_{DD} is added, thus causing interference with normal operation.

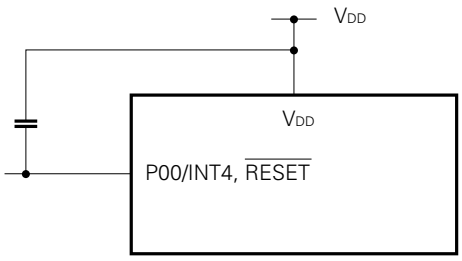
For example, this problem may occur if the P00/INT4 and $\overline{\text{RESET}}$ pins wiring is too long, causing line noise.

To avoid this, try to suppress line noise in wiring. If line noise is still high, try elimminating the noise using the exterior add-on components shown in the Figures below.

○ **Connect a Diode with Low V_F (0.3 V max.) Between the V_{DD} and the Pin.**



○ **Connect a Capacitor Between the V_{DD} and the Pin.**



2. DIFFERENCES BETWEEN μPD75P116 AND μPD75116

The μPD75P116 is a product in which the program memory (mask ROM) of the μPD75116 is changed to a user programmable PROM. Other functions of the μPD75P116 and μPD75116 are virtually the same only with the differences shown in Table 2-1.

For details of CPU functions and on-chip hardware, see the "**μPD75116 User's Manual (IEM-922)**".

Table 2-1 Differences between μPD75P116 and μPD75116 ★

Item		μPD75P116	μPD75116
Program memory		One-time PROM	Mask ROM
		0000H-3F7FH (16256 × 8 bits)	
Data memory		0000H-01FFH (512 × 4 bits)	
Pull-up resistor (ports 12 to 14)		No	Mask option
Power-on reset function			
Operating voltage range		5 V ± 10 %	2.7 to 6.0 V
Pin function	31 pins (SDIP)	V_{PP}	NC
	57 pins (QFP)		
	33 to 36 pins (SDIP)	P33/MD3 to P30/MD0	P33 to P30
	59 to 62 pins (QFP)		
Electrical specification		Different consumption current, operating temperature range, etc. Refer to the electrical specifications parameters for each data sheet for details.	
Other		Different noise resistance, noise radiation, etc., due to difference in the size of circuits and mask layout.	

Note The PROM and ROM products differ in noise resistance and noise radiation. If you are considering replacement of the PROM products by the mask ROM product in the transition from preproduction to volume production, this should be thoroughly evaluated with the mask ROM CS product (not ES product).

3. PROM (PROGRAM MEMORY) WRITE AND VERIFY

The ROM built into the μPD75P116 is a 16256 × 8-bit PROM. The pins shown in the table below are used to write/verify this PROM. There is no address input; instead, a method to update the address by the clock input from the X1 pin is adopted.

Pin Name	Function
V_{PP}	Voltage application pin for program memory write/verify (normally V_{DD} potential).
X1, X2	Address update clock inputs for program memory write/verify. Inverse of X1 pin signal is input to X2 pin.
MD0 to MD3	Operating mode selection pin for program memory write/verify.
P40 to P43 (low-order 4 bits) P50 to P53 (high-order 4 bits)	8-bit data input/output pins for progrm memory write/verify.
V_{DD}	Supply voltage application pin. Applies 5 V ± 10 % in normal operation, and 6 V for program memory write/verify.

Note Since the μPD75P116 is a one-time PROM version, UV-ray erasure is not possible.

3.1 PROGRAM MEMORY WRITE/VERIFY OPERATING MODES

The μPD75P116 assumes the program memory write/verify mode is +6 V and +12.5 V are applied respectively to the V_{DD} and V_{PP} pins. The table below shows the operating modes available by the MD0 to MD3 pin setting in this mode. The rest of pins are all set at the V_{SS} potential by the pull-down resistor.

Operating Mode Setting						Operating Mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Program memory address zero-clear
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	×	H	H	Program inhibit mode

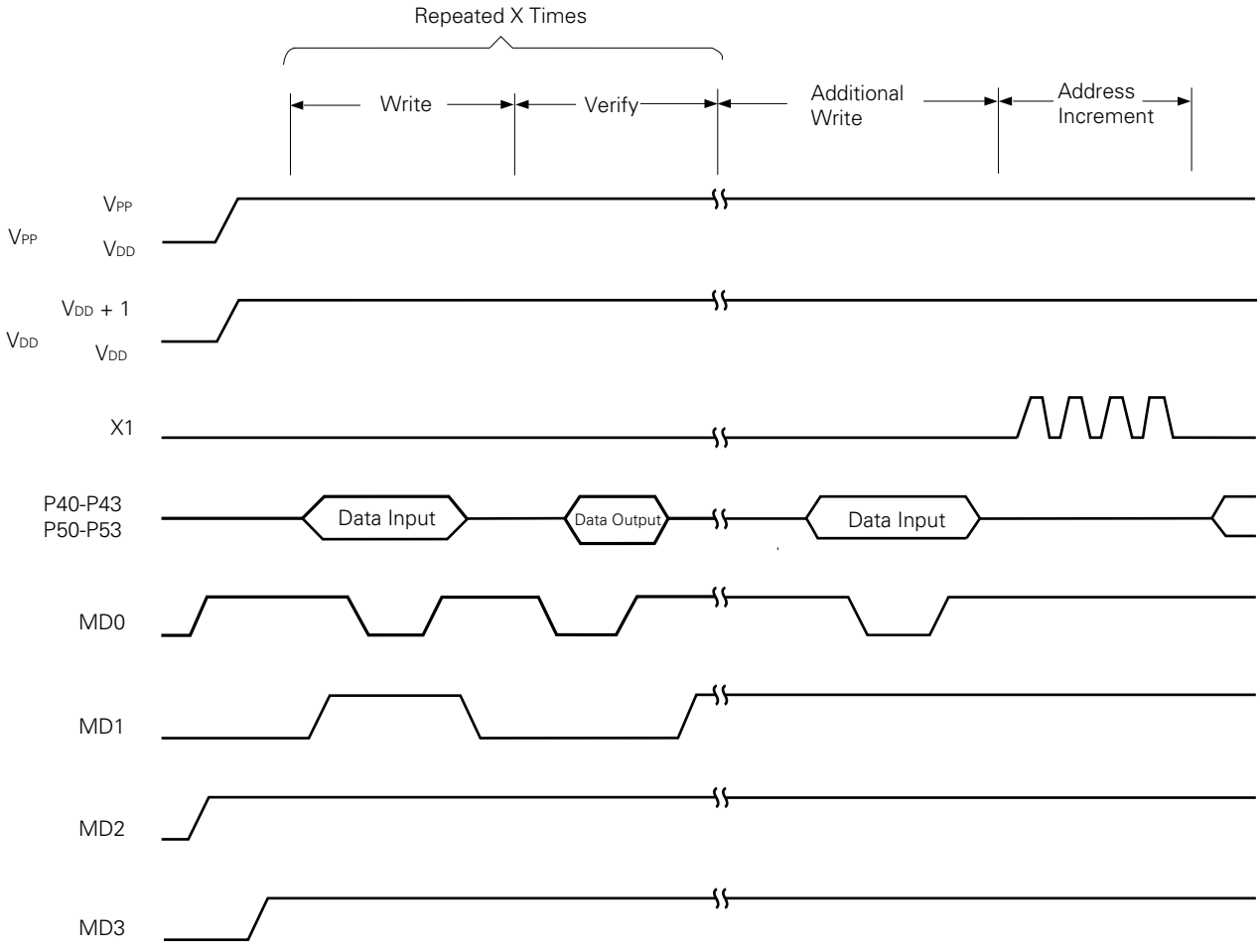
×: L or H

3.2 PROGRAM MEMORY WRITE PROCEDURE

The program memory writing procedure is shown below. High-speed write is possible.

(1) Pull down a pin which is not used to V_{SS} via the resistor. A low-level signal is input to the X1 pin.
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) 10 μs wait.
(4) The program memory address 0 clear mode.
(5) Supply +6 V and +12.5 V respectively to V_{DD} and V_{PP}.
(6) The program inhibit mode.
(7) Write data in the 1-ms write mode.
(8) The program inhibit mode.
(9) The verify mode. If written, proceed to (10); if not written, repeat (7) to (9).
(10) (Number of times written in (7) to (9): X) × 1-ms additional write.
(11) The program inhibit mode.
(12) Update (+1) the program memory address by inputting 4 pulses to the X1 pin.
(13) Repeat (7) to (12) up to the last address.
(14) The program memory address 0 clear mode.
(15) Change the V_{DD} and V_{PP} pins voltage to +5 V.
(16) Power off.

The diagram below shows the procedure of the above (2) to (12).

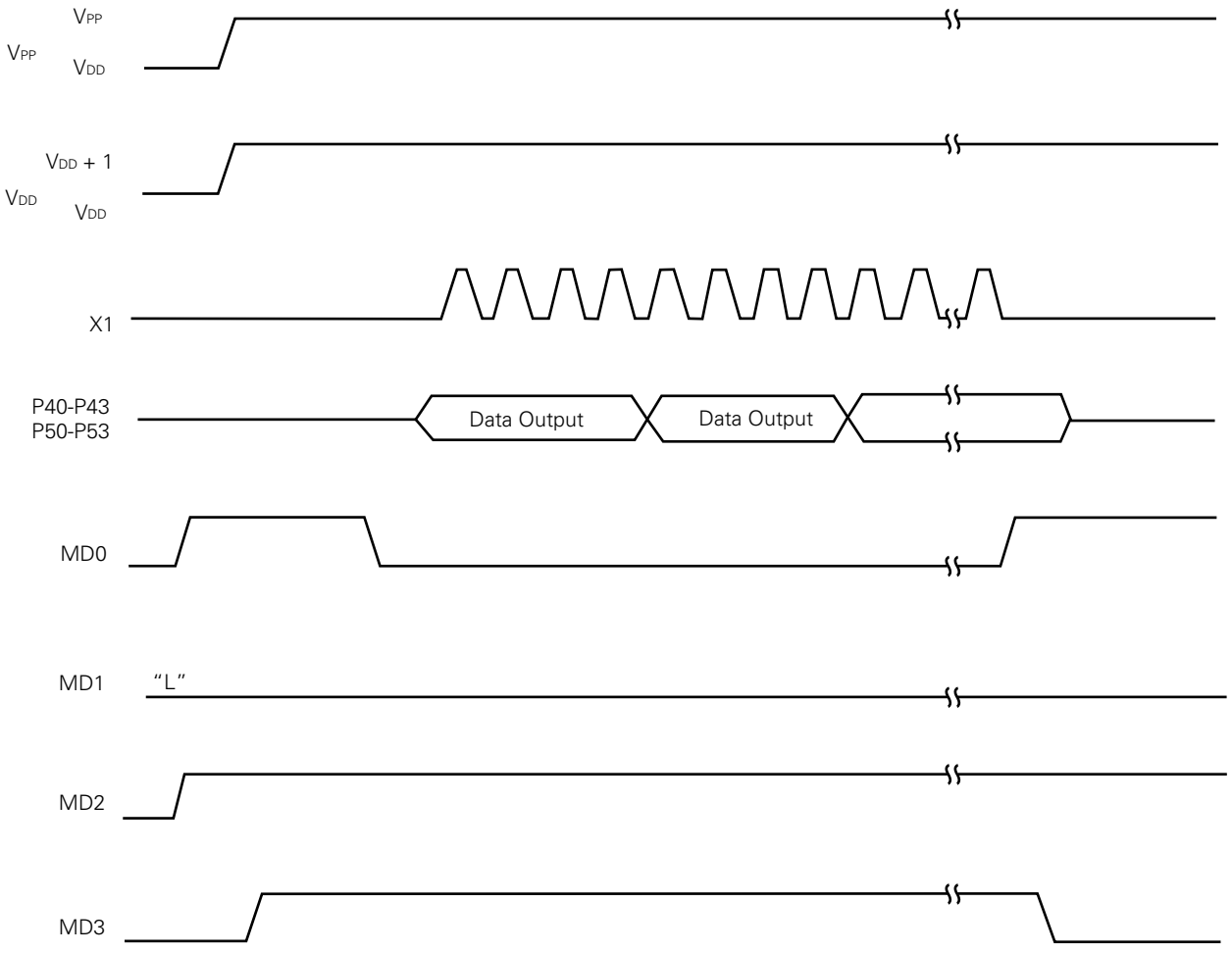


3.3 PROGRAM MEMORY READ PROCEDURE

The μPD75P116 can read the content of the program memory in the following procedure.

(1) Pull down a pin which is not used to V_{SS} via the resistor. A low-level signal is input to the X1 pin.
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) 10 μs wait.
(4) The program memory address 0 clear mode.
(5) Supply +6 V and +12.5 V respectively to V_{DD} and V_{PP}.
(6) The program inhibit mode.
(7) The verify mode. If clock pulses are input to the X1 pin, data is output sequentially 1 address at a time at the period of inputting 4 pulses.
(8) The program inhibit mode.
(9) The program memory address 0 clear mode.
(10) Change the V_{DD} and V_{PP} pins voltage to +5 V.
(11) Power off.

The diagram below shows the procedure of the above (2) to (9).



4. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

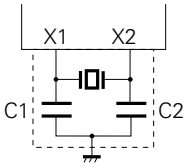
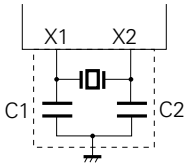
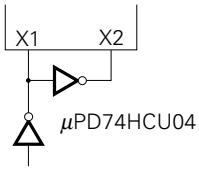
PARAMETER	SYMBOL	TEST CONDITIONS		RATING	UNIT
Supply voltage	V_{DD}			–0.3 to + 7.0	V
Supply voltage	V_{PP}			–0.3 to 13.5	V
Input voltage	V_{I1}	Except ports 12 to 14		–0.3 to V_{DD} + 0.3	V
	V_{I2} ***1**	Ports 12 to 14		–0.3 to +13	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current high	I_{OH}	1 pin		–15	mA
		Total pins		–30	mA
Output current low	I_{OL}***2**	1 pin	Peak value	30	mA
			Effective value	15	mA
		Ports 0, 2 to 4, 12 to 14 total	Peak value	100	mA
			Effective value	36	mA
		Ports 5 to 9 total	Peak value	100	mA
			Effective value	36	mA
Operating temperature	T_{opt}			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +125	°C

*** 1. The power supply impedance (pull-up resistor) should be 50 kΩ or more when the voltage exceeding 10 V applied to ports 12, 13 and 14.**

2. Effective value should be calculated as follows: [Effective value] = [Peak value] $\times \sqrt{\text{duty}}$

Note Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter or even momentarily. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

OSCILLATION CIRCUIT CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 5 V ± 10 %)

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ceramic resonator		Oscillator frequency (f_{XX}) ***1**		2.0		***3** 5.0	MHz
		Oscillation stabilization time ***2**	After V_{DD} reaches 4.5 V.			4	ms
Crystal resonator		Oscillator frequency (f_{XX}) ***1**		2.0	4.19	***3** 5.0	MHz
		Oscillation stabilization time ***2**	After V_{DD} reaches 4.5 V.			10	ms
External clock		X1 input frequency (f_X) ***1**		2.0		***3** 5.0	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		100		250	ns

*** 1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristics" for instruction execution time.**

2. Time required to stabilize oscillation after V_{DD} reaches oscillation voltage range MIN. or STOP mode release.

★ **3. When the oscillator frequency is 4.19 MHz < f_{XX} ≤ 5.0MHz, PCC = 0011 should not be selected as instruction execution time. If PCC = 0011 is selected, 1 machine cycle becomes less than 0.95 μs, with the result that the specified MIN value of 0.95 μs cannot be observed.**

★ **Note When the system clock oscillator is used, the following points should be noted concerning wiring in the section enclosed by dots, in order to prevent the effects of wiring capacitance, etc.**

- **Keep the wiring as short as possible.**
- **Do not cross any other signal lines.**
- **Keep away from lines in which a high fluctuating current flows.**
- **Ensure that oscillator capacitor connection points are always at the same potential as V_{SS}. Do not ground in a ground pattern in which a high current flows.**
- **Do not take a signal from the oscillator.**

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 5 V ± 10 %)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input voltage high	V_{IH1}	Other than below		0.7V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0 & 1, TI0 & 1, $\overline{RESET}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	Ports 12 to 14		0.7V_{DD}		12	V
	V_{IH4}	X1, X2		V_{DD}–0.5		V_{DD}	V
Input voltage low	V_{IL1}	Other than below		0		0.3V_{DD}	V
	V_{IL2}	Ports 0 & 1, TI0 & 1, $\overline{RESET}$		0		0.2V_{DD}	V
	V_{IL3}	X1, X2		0		0.4	V
Output voltage high	V_{OH}	I_{OH} = –1 mA		V_{DD}–1.0			V
Output voltage low	V_{OL}	I_{OL} = 15 mA	Ports 0, 2, to 9		0.55	2.0	V
		I_{OL} = 10 mA	Ports 12 to 14		0.35	2.0	V
		I_{OL} = 1.6 mA				0.4	V
Input leakage current high	I_{LIH1}	V_{IN} = V_{DD}	Other than below			3	μA
	I_{LIH2}		X1, X2			20	μA
	I_{LIH3}	V_{IN} = 12 V	Ports 12 to 14			20	μA
Input leakage current low	I_{LIL1}	V_{IN} = 0 V	Except X1 & X2			–3	μA
	I_{LIL2}		X1, X2			–20	μA
Output leakage current high	I_{LOH1}	V_{OUT} = V_{DD}	Other than below			3	μA
	I_{LOH2}	V_{OUT} = 12 V	Ports 12 to 14			20	μA
Output leakage current low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Power supply current ***1**	I_{DD1}	4.19 MHz Crystal oscillation C1 = C2 = 22 pF	V_{DD} = 5 V ± 5 % ***2**		5	10	mA
	I_{DD2}		HALT mode***3** V_{DD} = 5 V ± 5 %		500	1500	μA
	I_{DD3}	STOP mode, V_{DD} = 5 V ± 5 %			0.5	20	μA

* **1.** Not including current flowing in comparator.

2. When processor clock control register (PCC) is set to 0011 operating in high-speed mode.

3. When PCC is set to 0100 and CPU is halted in HALT mode.

CAPACITANCE (Ta = 25 °C, V_{DD} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.			15	pF
Output capacitance	C_{OUT}				15	pF
I/O capacitance	C_{IO}				15	pF

COMPARATOR CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 5 V ± 10 %)

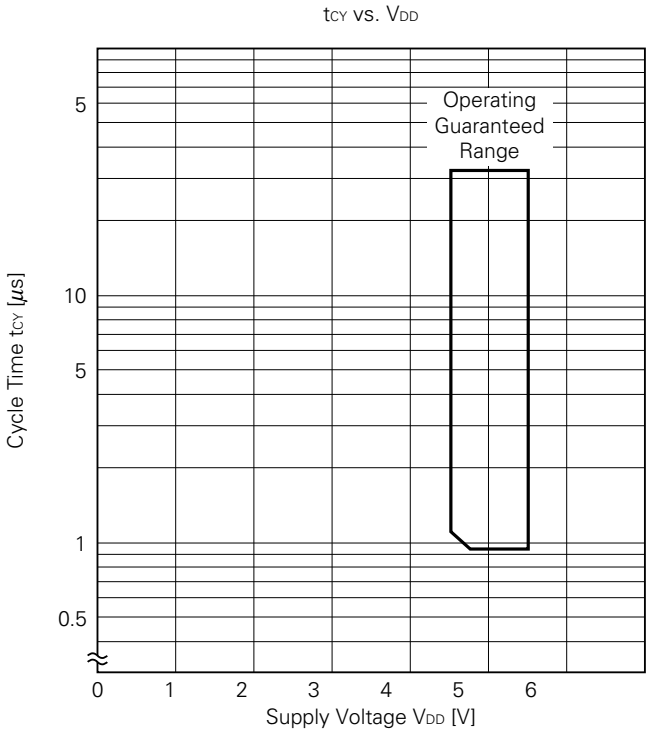
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Comparison accuracy	V_{ACOMP}				±100	mV
Threshold voltage	V_{TH}		0		V_{DD}	V
PTH input voltage	V_{IPTH}		0		V_{DD}	V
Comparator circuit current consumption		PTHM7 set to "1"		1		mA

AC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CPU clock cycle time* (minimum instruction execution time = 1 machine cycle)	t_{CY}		V_{DD} = 4.75 to 5.5 V	0.95		32	μs
				1.1		32	μs
TI input frequency	f_{TI}			0		1	MHz
TI input high/low-level width	t_{TIH}, t_{TIL}			0.48			μs
$\overline{SCK}$ cycle time	t_{KCY}		Input	0.8			μs
			Output	0.95			μs
$\overline{SCK}$ high/low-level width	t_{KH}, t_{KL}		Intput	0.4			μs
			Output	t_{KCY}/2–50			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK}			100			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI}			400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO}					300	ns
INT0 to INT4 high/low-level width	t_{INTH}, t_{INTL}			5			μs
$\overline{RESET}$ low level width	t_{RSL}			5			μs

* The cycle time of the CPU clock (Φ) is determined by the oscillator frequency of the connected resonator and the processor clock control register (PCC).
The graph on the below shows the cycle time t_{CY} characteristics against supply voltage V_{DD}.

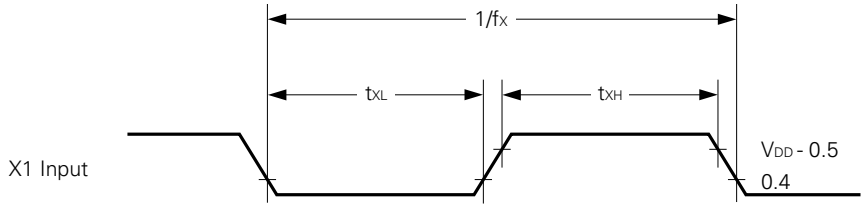
Relation between Cycle Time and Supply Voltage



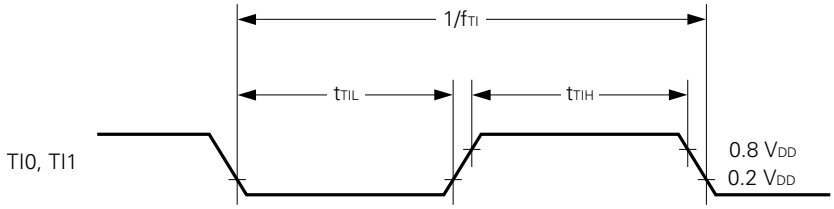
Note t_{CY} vs. V_{DD} characteristics are different from those of the μPD75P108

AC Timing Test Point (Excluding ports 0 & 1, TI0, TI1, X1, X2, $\overline{\text{RESET}}$)

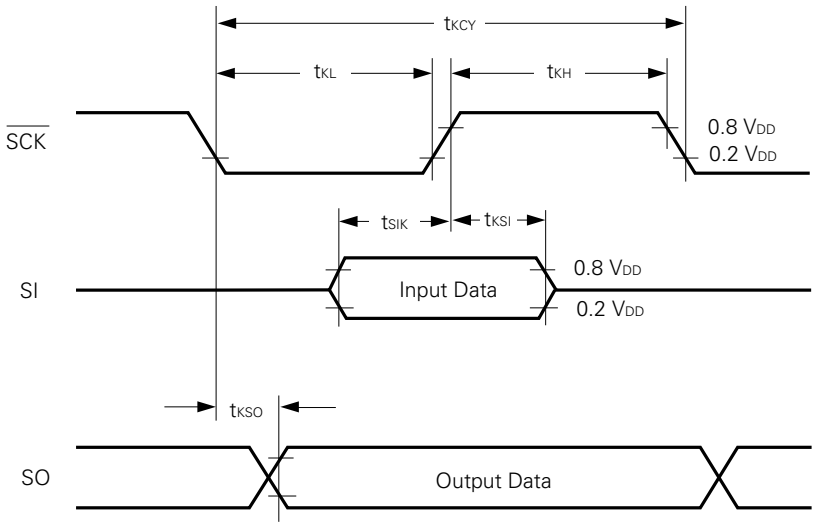
Clock Timing



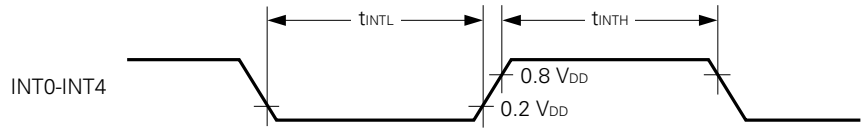
TI Input Timing



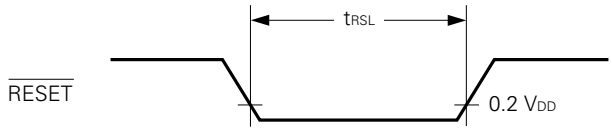
Serial Transfer Timing



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (Ta = –40 to +85 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention supply voltage	V_{DDDR}		2.0		5.5	V
Data retention power supply current ***1**	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time ***2**	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_x$		ms
		Release by interrupt request		***3**		ms

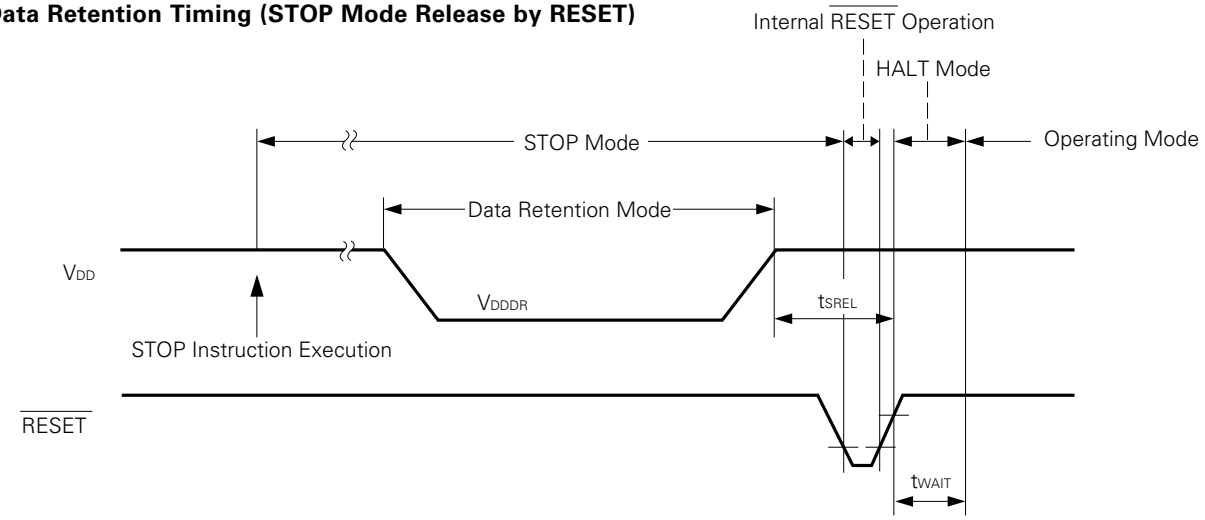
* **1.** Does not include current flowing in the comparator.

2. The oscillator stabilization wait time is the time during which CPU operation is halted to prevent unstable operation when oscillation begins.

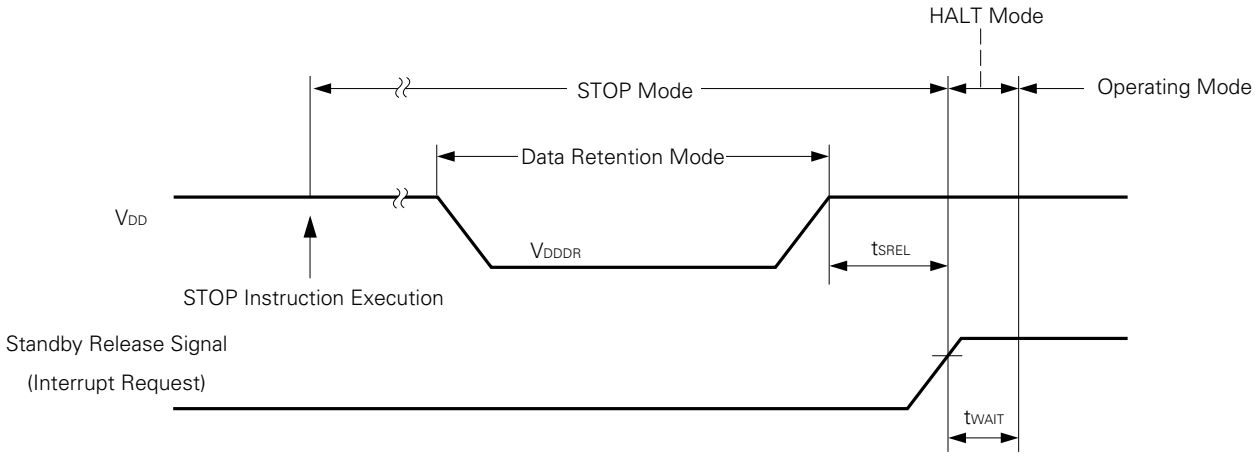
3. Depends on the setting of the basic interval timer mode register (BTM) (table below).

BTM3	BTM2	BTM1	BTM0	WAIT Time (Figure in Parentheses is for f_{XX} = 4.19 MHz)
–	0	0	0	$2^{20}/f_{XX}$ (Approx. 250 ms)
–	0	1	1	$2^{17}/f_{XX}$ (Approx. 31.3 ms)
–	1	0	1	$2^{15}/f_{XX}$ (Approx. 7.82 ms)
–	1	1	1	$2^{13}/f_{XX}$ (Approx. 1.95 ms)

Data Retention Timing (STOP Mode Release by $\overline{RESET}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



DC PROGRAMMING CHARACTERISTICS (Ta = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.3 V, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input voltage high	V_{IH1}	Except X1 & X2	$0.7V_{DD}$		V_{DD}	V
	V_{IH2}	X1, X2	V_{DD}–0.5		V_{DD}	V
Input voltage low	V_{IL1}	Except X1 & X2	0		$0.3 V_{DD}$	V
	V_{IL2}	X1, X2	0		0.4	V
Input leakage current	I_{LI}	$V_{IN} = V_{IL}$ or V_{IH}			10	μA
Output voltage high	V_{OH}	I_{OH} = –1 mA	V_{DD}–1.0			V
Output voltage low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
V_{DD} supply current	I_{DD}				30	mA
V_{PP} supply current	I_{PP}	MD0 = V_{IL}, MD1 = V_{IH}			30	mA

Note 1. Ensure that V_{PP} does not reach +13.5 V or above including overshot.

2. Ensure that V_{DD} is applied before V_{PP} and cut off after V_{PP}.

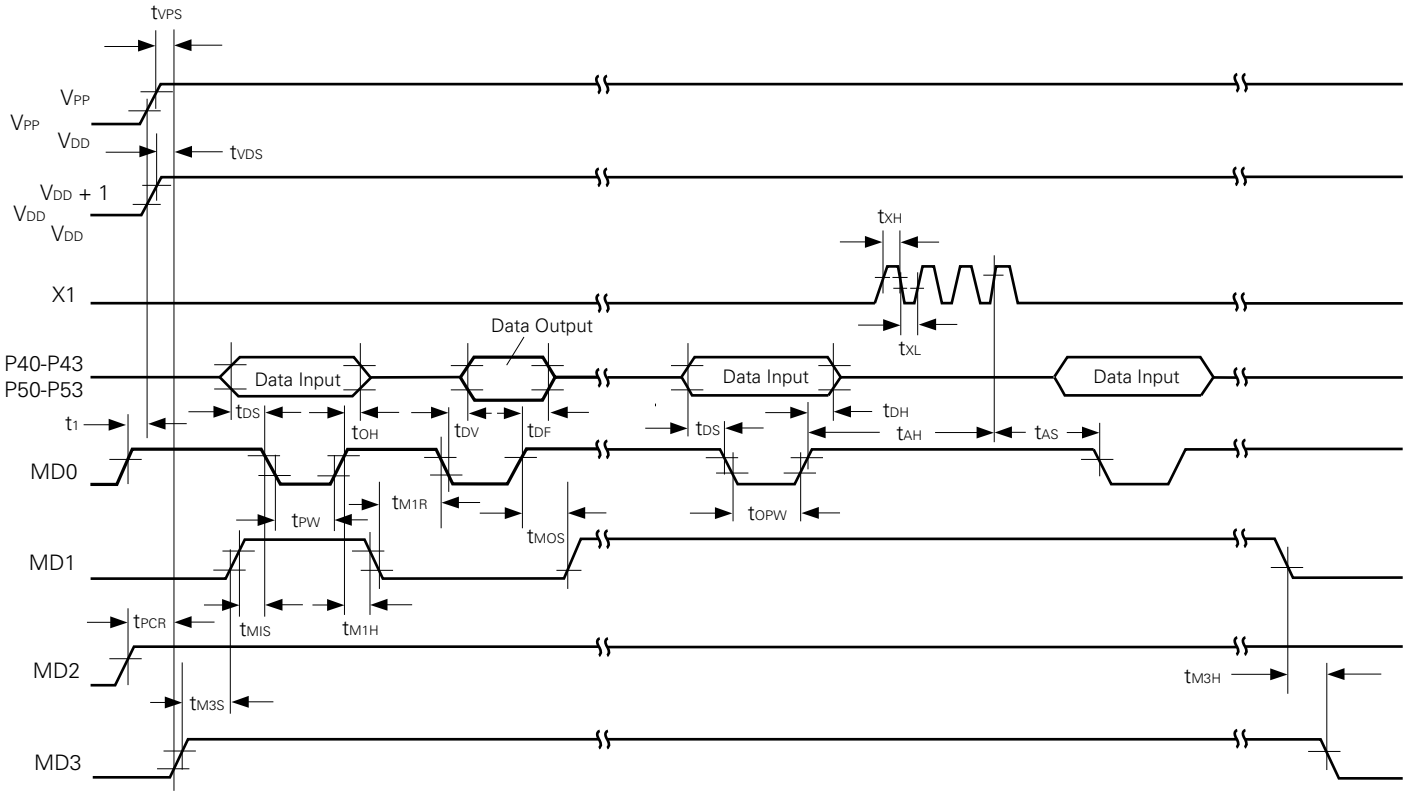
AC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.3 V, V_{SS} = 0 V)

PARAMETER	SYMBOL	*1	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Address setup time *2 (to MD0↓)	t_{AS}	t_{AS}		2			μs
MD1 setup time (to MD0↓)	t_{M1S}	t_{OES}		2			μs
Data setup time (to MD0↓)	t_{DS}	t_{DS}		2			μs
Address hold time *2 (from MD0↑)	t_{AH}	t_{AH}		2			μs
Data hold time (from MD0↑)	t_{DH}	t_{DH}		2			μs
Data output float delay time from MD0↑	t_{DF}	t_{DF}		0		130	ns
V_{PP} setup time (to MD3↑)	t_{VPS}	t_{VPS}		2			μs
V_{DD} setup time (to MD3↑)	t_{VDS}	t_{VCS}		2			μs
Initial program pulse width	t_{PW}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{OPW}	t_{OPW}		0.95		21.0	ms
MD0 setup time (to MD1↑)	t_{MOS}	t_{CES}		2			μs
Data output delay time from MD0↓	t_{DV}	t_{DV}	MD0 = MD1 = V_{IL}			1	μs
MD1 hold time (from MD0↑)	t_{M1H}	t_{OEH}	$t_{M1H} + t_{M1R} \geq 50$ μs	2			μs
MD1 recovery time (from MD0↓)	t_{M1R}	t_{OR}		2			μs
Program counter reset time	t_{PCR}	—		10			μs
X1 input high-/low-level width	t_{XH}, t_{XL}	—		0.125			μs
X1 input frequency	f_X	—				4.19	MHz
Initial mode setting time	t_I	—		2			μs
MD3 setup time (to MD1↑)	t_{M3S}	—		2			μs
MD3 hold time (from MD1↓)	t_{M3H}	—		2			μs
MD3 setup time (to MD0↓)	t_{M3SR}	—	In program memory read	2			μs
Data output delay time from address *2	t_{DAD}	t_{ACC}	In program memory read	2			μs
Data output hold time from address *2	t_{HAD}	t_{OH}	In program memory read	0		130	ns
MD3 hold time (from MD0↑)	t_{M3HR}	—	In program memory read	2			μs
Data output float delay time from MD3↓	t_{DFR}	—	In program memory read	2			μs

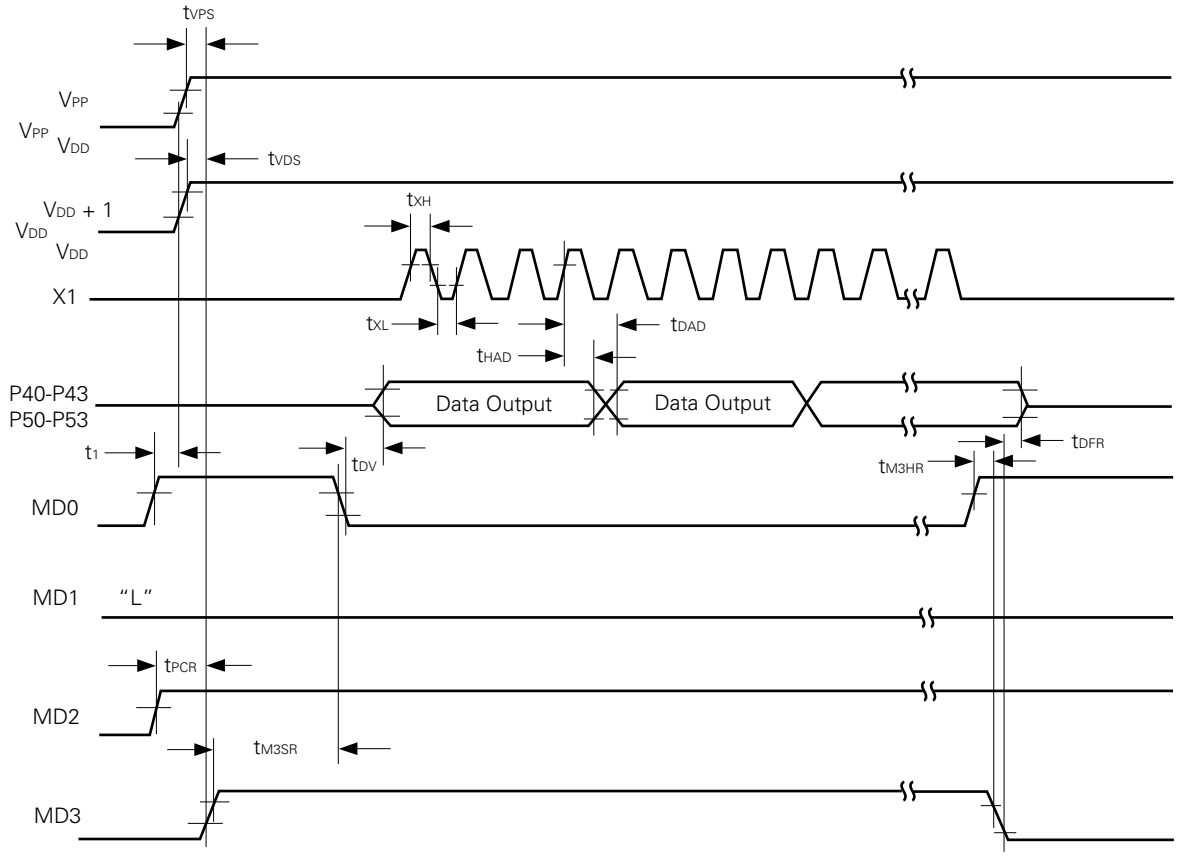
* **1.** Corresponding to μPD27C256 symbol.

2. Internal address signal is incremented by 1 on rise of 4th X1 input, and is not connected to a pin.

Program Memory Write Timing

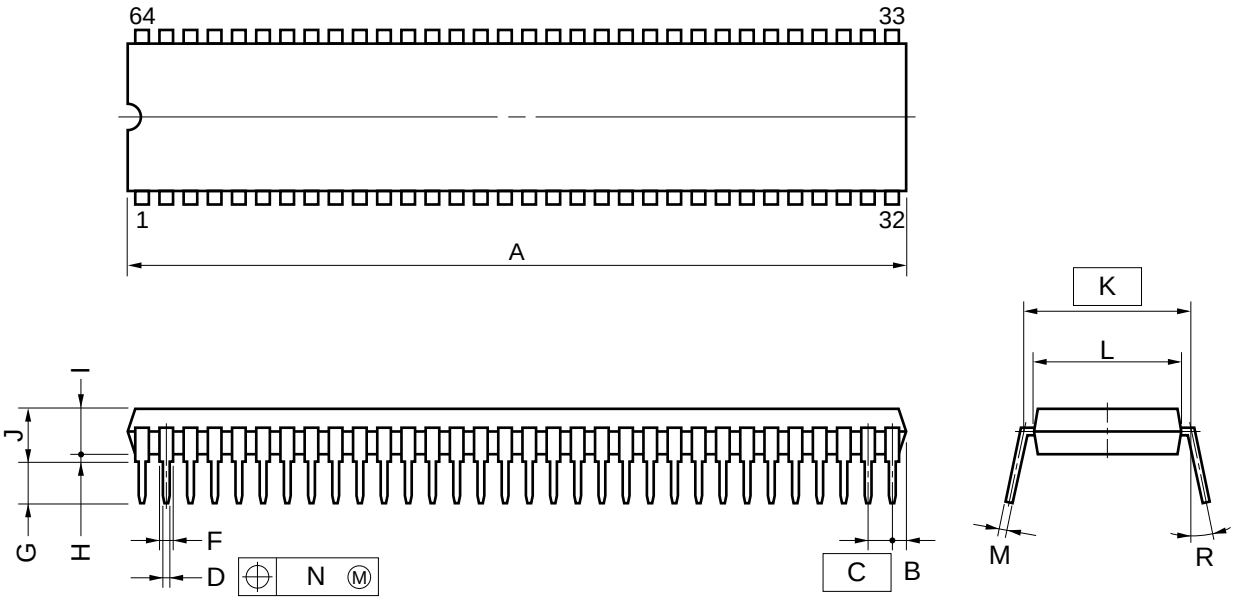


Program Memory Read Timing



5. PACKAGE INFORMATION

64 PIN PLASTIC SHRINK DIP (750 mil)



NOTE

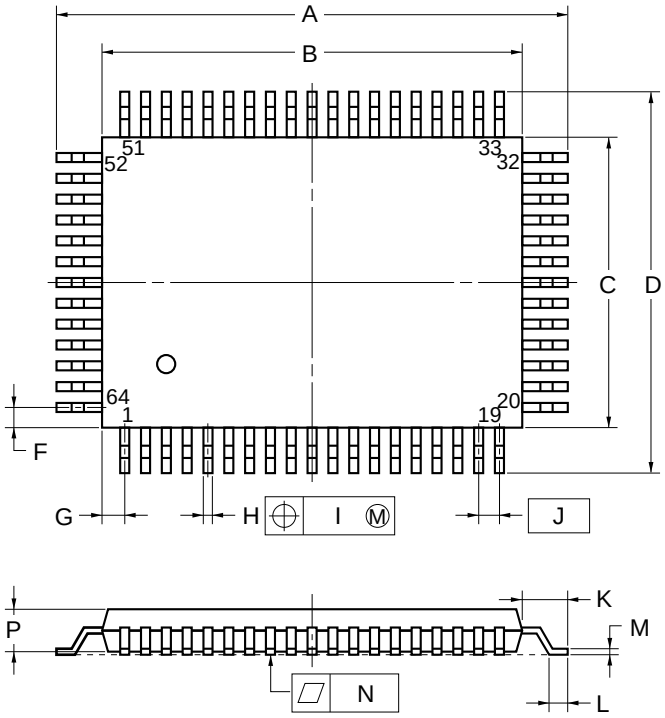
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

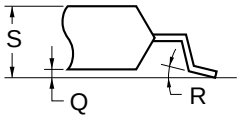
P64C-70-750A,C-1

64 PIN PLASTIC QFP (14×20)

★



detail of lead end



NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.008}_{-0.009}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P64GF-100-3B8,3BE,3BR-2

★ 6. RECOMMENDED SOLDERING CONDITIONS

The μPD75P116 should be mounted under the conditions recommended in the table below.

For details of recommended soldering conditions, refer to the information document **"Surface Mount Technology Manual" (IEI-1207).**

For soldering methods and conditions other than those recommended below, contact our salesman.

Table 6-1 Surface Mount Type Soldering Conditions

μPD75P116GF-3BE : 64-pin plastic QFP (14 × 20 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230°C, Duration: 30 sec. max. (at 210°C or above), Number of times: Once Time limit: 2 days* (thereafter 16 hours prebaking required at 125°C)	IR30-162-1
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above), Number of times: Once Time limit: 2 days* (thereafter 16 hours prebaking required at 125°C)	VP15-162-1
Wave soldering	Solder bath temperature: 260°C max., Duration: 10 sec. max Number of times: Once Preheating temperature: 120°C max. (package surface temperature), Time limit: 2 days* (thereafter 16 hours prebaking required at 125°C)	WS60-162-1
Pin part heating	Pin part temperature: 300°C max., Duration: 3 sec. max. (per device side)	—

***** For the storage period after dry-pack decapsulation, storage conditions are max. 25°C, 65% 1H.

Note Use of more than one soldering method should be avoided (except in the case of pin part heating).

Table 6-2 Insertion Type Soldering Conditions

μPD75P116CW : 64-pin plastic shrink DIP (750 mil)

Soldering Method	Soldering Conditions
Wave Soldering (lead part only)	Solder bath temperature: 260°C max., Duration: 10sec. max.
Pin part heating	Pin part temperature: 260°C max., Duration: 10sec. max.

Note Ensure that the application of (wave soldering) is limited to the lead part and no solder touches the main unit directly.

Notice

A version of this product with improved recommended soldering conditions is available. For details (improvements such as infrared reflow peak temperature extension (230 °C), number of times: twice, relaxation of time limit, etc.), contact NEC sales personnel.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD75P116.

Hardware	IE-75000-R ***1** IE-75001-R		In-circuit emulator for 75X series
	IE-75000-R-EM ***2**		Emulation board for IE-75000-R and IE-75001-R
	EP-75108CW-R		Emulation probe for μPD75P116CW
	EP-75108GF-R	EV-9200G-64	Emulation probe for μPD75P116GF A 64-pin conversion socket EV-9200G-64 is provided.
	PG-1500		PROM programmar
	PA-75P108CW		This is a PROM programmar adapter for μPD75P116CW and connects to PG-1500.
	PA-75P116GF		This is a PROM programmar adapter for μPD75P116GF and connects to PG-1500.
Software	IE control program		Host machine • PC-9800 series (MS-DOS™ Ver.3.30 to Ver.5.00A ***3**) • IBM PC/AT™ series (PC DOS™ Ver.3.1)
	PG-1500 controller		
	RA75X relocatable assembler		

***** **1** Maintenance product

2 This is not incorporated in the IE-75001-R.

3 A task swap function is provided with Ver.5.00/5.00A; however, a task swap function cannot be used with this software.

Remarks For development tools manufactured by a third pary, see the **"75X Series Selection Guide" (IF-151)**.

★ APPENDIX B. RELATED DOCUMENTATION

List of Device-Related Documents

Document Name		Document No.
User's Manual		
Instruction Application Table		
Application Note	(I) Introductory Volume	
	(II) Remote-Controlled Reception Volume	
	(III) Bar-Code Reader-Volume	
	(IV) IC Control for MSK Transmission/Reception Volume	
75X Series Selection Guide		

List of Development Tool Related Documents

Document Name			Document No.
Hardware	IE-75000-R/IE-75001-R User's Manual		
	IE-75000-R-EM User's Manual		
	EP-75108CW-R User's Manual		
	EP-75108GF-R User's Manual		
	PG-1500 User's Manual		
Software	RA75X Assembler Package User's Manual	Operation Volume	
		Language Volume	
	PG-1500 Controller User's Manual		

Other Documents

Document Name	Document No.
Package Manual	
Surface Mount Technology Manual	
Quality Grade on NEC Semiconductor Devices	
NEC Semiconductor Device Reliability Quality Control	
Electrostatic Discharge (ESD) Test	
Semiconductor Device Quality Guarantee Guide	
Microcomputer Related Product Guide Other Manufacturer Volume	

Note The above related documents may be changed without notice. Be sure to use the latest documents for design purposes.

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