NEC

MOS INTEGRATED CIRCUIT

μPD75P108B

4-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD75P108B is a version of the μPD75108 in which the on-chip mask ROM is replaced by one-time PROM which can be written to once only, or EPROM which is capable of program write, erasure and rewrite.

Also, since the μPD75P108B is capable of program write by a user, it can easily be exchanged with the mask version, allowing evaluation at low voltage.

Detailed functional descriptions are shown in the following User's Manual. Be sure to read for designations.

μPD751×× Series User's Manual : IEM-922

FEATURES

- Version with on-chip PROM, allowing low-voltage operation V_{DD} = 2.7 to 6.0 V
- μPD75108 compatible
- Memory capacity
  - Program memory (PROM) : 8064 × 8 bits
  - Data memory (RAM) : 512 × 4 bits
- Correspondence to QTOP™ microcomputer

ORDERING INFORMATION

Ordering Code	Package	On-Chip ROM	
μPD75P108BCW	64-pin plastic shrink DIP (750 mil)	One-time PROM	
μPD75P108BDW	64-pin ceramic shrink DIP (with window)	EPROM	★
μPD75P108BGF-3BE	64-pin plastic QFP (14 × 20 mm, 1.0 mm pitch)	One-time PROM	

Note There is no on-chip pull-up resistor function by means of a mask option.

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

In this ducument, common parts of one-time PROM products and EPROM products are represented as PROM.

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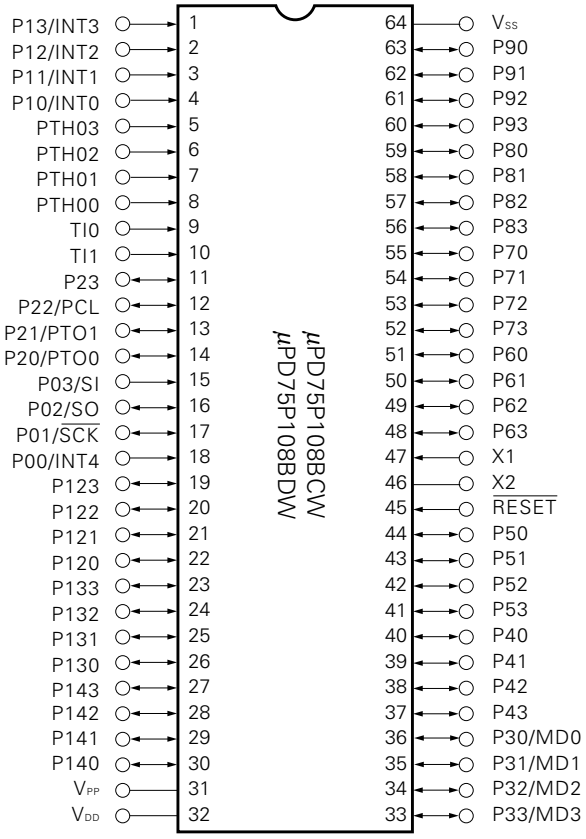
(O. D. No. IC-7987C)
Date Published December 1993 P
Printed in Japan

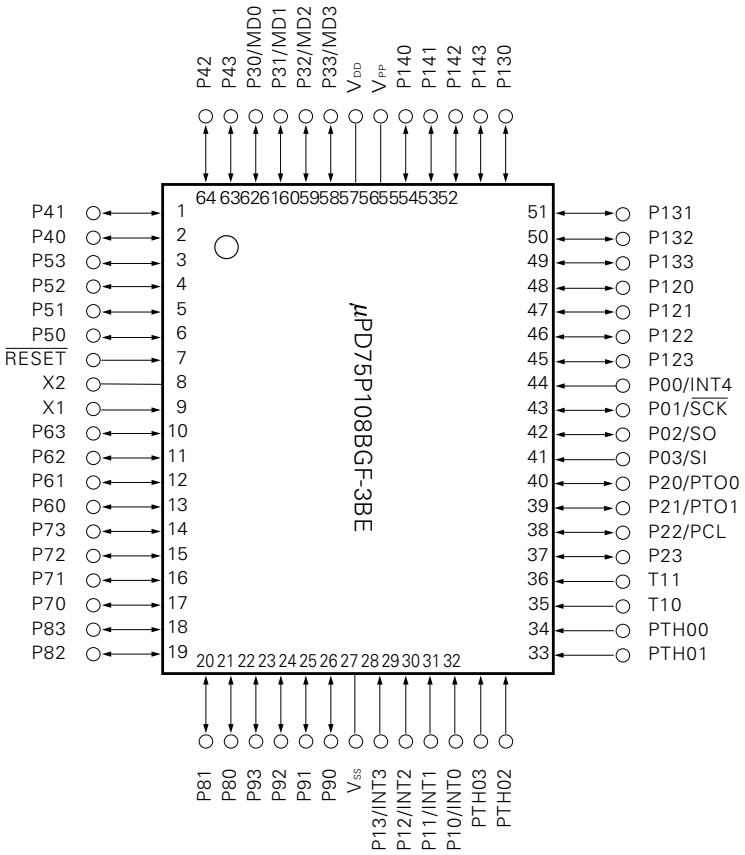
The mark ★ shows major revised points.

PIN CONFIGURATION (TOP VIEW)

64-pin plastic shrink DIP (750 mil)
64-pin ceramic shrink DIP
(with window)



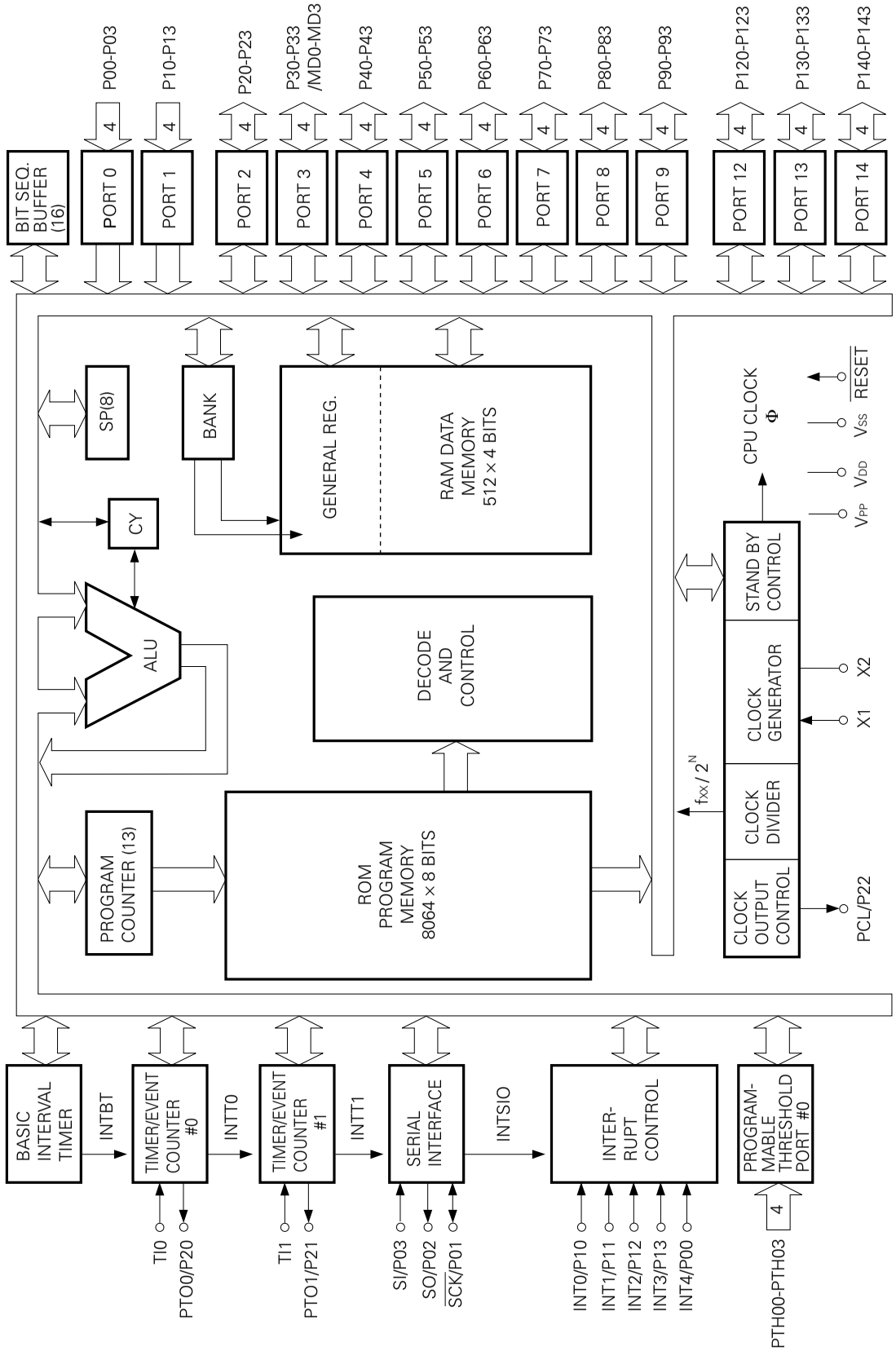
64-pin plastic QFP (14 × 20 mm, 1.0 mm pitch)



OVERVIEW OF FUNCTIONS

Item		Description
Basic instructions		43
Minimum instruction execution time		0.95 μs, 1.91 μs, 15.3 μs (4.19 MHz operation) 3-stage switching capability
Internal memory	ROM	8064 × 8
	RAM	512 × 4
General register		4-bits × 8 × 4 banks (memory mapping)
Accumulator		3 types of accumulators corresponding to bit length of manipulated data • 1-bit accumulator (CY), 4-bit accumulator (A), 8-bit accumulator (XA)
Input/output port		Total 58 • CMOS input pins : 10 • CMOS input/output pins (LED direct drive capability) : 32 • Middle-high voltage N-ch open-drain input/output pins (LED direct drive capability) : 12 • Comparator input pins (4-bit precision) : 4
Timer/counter		• 8-bit timer/event counter × 2 • 8-bit basic interval timer (watchdog timer applicable)
8-bit serial interface		• Two transfer modes • Serial transmity receive mode • Serial receive mode • LSB-first/MSB-first switchable
Vectored interrupt		External : 3, internal : 4
Test input		External : 2
Standby		• STOP/HALT mode
Instruction set		• Various bit manipulation instructions (set, reset, test, boolean operation) • 8-bit data transfer, comparison, operation, increment/decrement instructions • 1-byte relative branch instruction • GETI instruction that can implement arbitrary 2-byte/3-byte instructions with 1 byte
Others		• Bit manipulation memory (bit sequential buffer : 16 bits) on-chip
★ Package		• 64-pin plastic shrink DIP (750 mil) • 64-pin ceramic shrink DIP (with window) • 64-pin plastic QFP (14 × 20mm, 1.0 mm pitch)

BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

1.1 PORT PINS

Pin Name	Input/Output	Dual-Function Pin	Function	8-bit I/O	After Reset	I/O Circuit Type *1
P00	Input	INT4	4-bit input port (PORT 0).	×	Input	Ⓑ
P01	Input/output	$\overline{SCK}$				Ⓕ
P02	Input/output	SO				E
P03	Input	SI				Ⓑ
P10	Input	INT0	4-bit input port (PORT 1).		Input	Ⓑ
P11		INT1				
P12		INT2				
P13		INT3				
P20	Input/output	PTO0	4-bit input/output port (PORT 2). *2	×	Input	E
P21		PTO1				
P22		PCL				
P23		—				
P30 to P33	Input/output	MD0 to MD3	Programmable 4-bit input/output port (PORT 3). Input/output can be specified bit-wise. *2		Input	E
P40 to P43	Input/output	—	4-bit input/output port (PORT 4). Data input/output pin for program memory (PROM) write/verify (low-order 4 bits). *2	○	Input	E
P50 to P53	Input/output	—	4-bit input/output port (PORT 5). Data input/output pin for program memory (PROM) write/verify (high-order 4 bits). *2		Input	E
P60 to P63	Input/output	—	Programmable 4-bit input/output port (PORT 6). Input/output can be specified bit-wise. *2	○	Input	E
P70 to P73	Input/output	—	4-bit input/output port (PORT 7). *2		Input	E
P80 to P83	Input/output	—	4-bit input/output port (PORT 8). *2	○	Input	E
P90 to P93	Input/output	—	4-bit input/output port (PORT 9). *2		Input	E
P120-P123	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 12). +12 V withstand voltage. *2	○	Input	M-A
P130-P133	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 13). +12 V withstand voltage. *2		Input	M-A
P140-P143	Input/output	—	N-ch open-drain 4-bit input/output port (PORT 14). +12 V withstand voltage. *2	—	Input	M-A

* **1.** ◯ indicates Schmitt-triggered input.
2. LED direct drive capability

1.2 OTHER PINS

Pin Name	Input/Output	Dual-Function Pin	Function	After Reset	I/O Circuit Type *1
PTH00 to PTH03	Input	—	Variable threshold voltage 4-bit analog input port.		N
TI0	Input	—	External event pulse input to timer/event counter. Or edge detection vectored interrupt input pin, or 1-bit input is also possible.		Ⓑ
TI1					
PTO0	Input/output	P20	Timer/event counter output pin.	Input	E
PTO1		P21			
$\overline{SCK}$	Input/output	P01	Serial clock input/output pin.	Input	Ⓕ
SO	Input/output	P02	Serial data output pin.	Input	E
SI	Input	P03	Serial data input pin.	Input	Ⓑ
INT4	Input	P00	Edge detection vector interrupt input pin (detection of both rising and falling edges).		Ⓑ
INT0	Input	P10	Edge detection vector interrupt input pin (detection edge selectable).		Ⓑ
INT1		P11			
INT2	Input	P12	Edge detection testable input pin (rising edge detection)		Ⓑ
INT3		P13			
PCL	Input/output	P22	Clock output pin	Input	E
X1, X2		—	System clock oscillation crystal/ceramic connection pin. When an external clock is used, the clock is input to X1 and the inverted clock is input to X2.		
$\overline{RESET}$	Input	—	System reset input pin (low-level active).		Ⓑ
MD0 to MD3	Input/output	P30 to P33	Mode selection pin for program memory (PROM) write/verify.	Input	E
V_{DD}		—	Positive power supply pin. Applies +6 V for write/verify.		
V_{SS}		—	GND potential pin.		
V_{PP} *2		—	Program voltage impression pin for program memory (PROM) write/verify. Connected to V_{DD} in normal operation. Applies +12.5 V for PROM write/verify.		

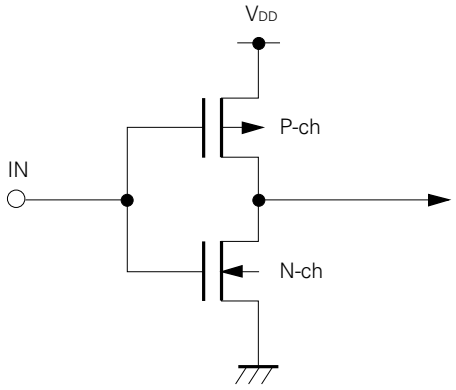
* **1.** ◯ indicates Schmitt-triggered input.

2. The device will not operate correctly unless V_{PP} is connected to V_{DD} in normal use.

1.3 PIN INPUT/OUTPUT CIRCUITS

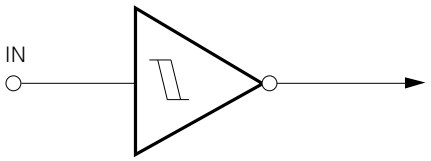
The input/output circuits of each pin of the μPD75P108B are shown by in abbreviated form.

(1) Type A (for Type E)



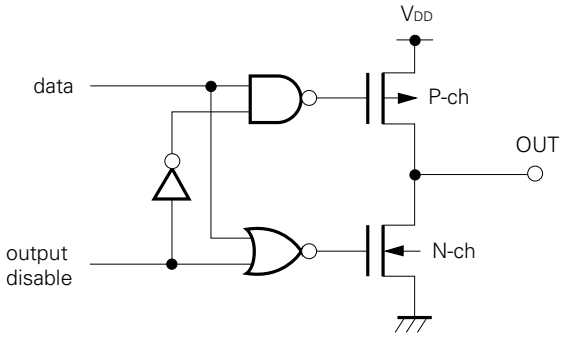
CMOS standard input buffer

(2) Type B



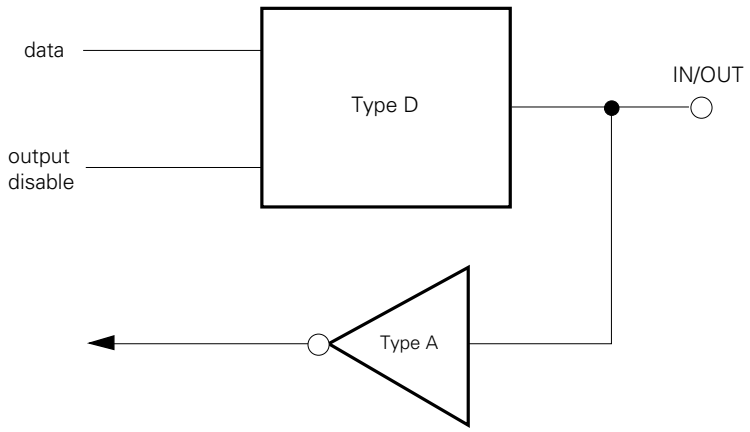
Schmitt-triggered input with hysteresis characteristic

(3) Type D (for Type E, F)



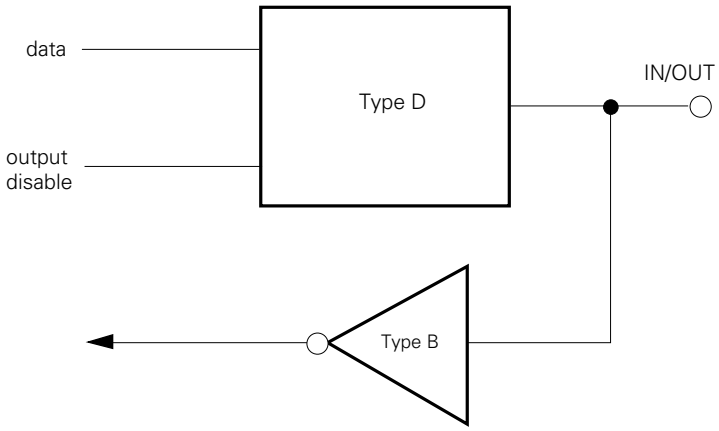
Push-pull output that can be made high-impedance output (P-ch and N-ch OFF)

(4) Type E



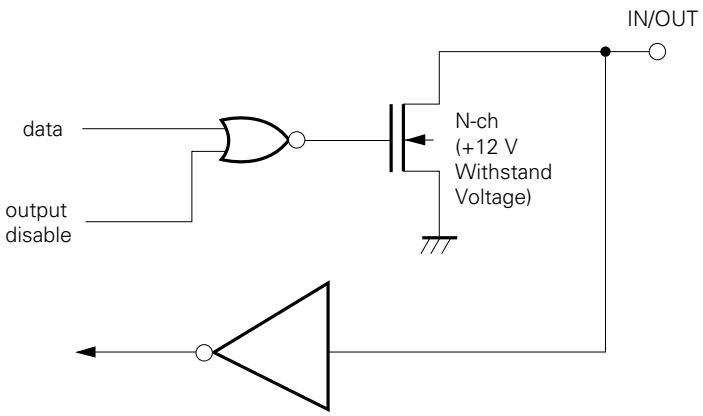
This is an input/output circuit made up of a Type D push-pull output and Type A input buffer.

(5) Type F



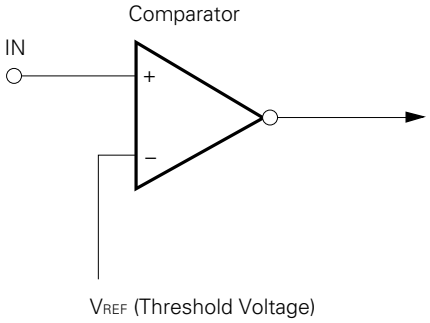
This is an input/output circuit made up of a Type D push-pull output and Type B Schmitt-triggered input.

(6) Type M-A



Middle-High Voltage Input Buffer
(+12 V Withstand Voltage)

(7) Type N



1.4 RECOMMENDED CONNECTION OF UNUSED PINS

Pin	Recommended Connection
PTH00 to PTH03 TI0 TI1	Connect to V_{SS} or V_{DD}.
P00	Connect to V_{SS}.
P01 to P03	Connect to V_{SS} or V_{DD}.
P10 to P13	Connect to V_{SS}.
P20 to P23 P30 to P33 P40 to P43 P50 to P53 P60 to P63 P70 to P73 P80 to P83 P90 to P93 P120 to P123 P130 to P133 P140 to P143	Input status : Connect to V_{SS} or V_{DD}. Output status : Leave open.
$\overline{\text{RESET}}$	Connect to V_{DD}.

1.5 CAUTION ON USING P00/INT4 PIN AND $\overline{\text{RESET}}$ PIN

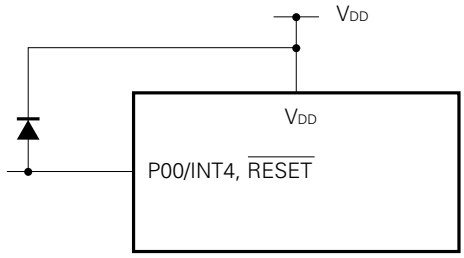
The P00/INT4 and $\overline{\text{RESET}}$ pins have a test mode setting function (for IC test) which tests internal operations of pin of the μPD75P108B in addition to those functions given in 1.1 and 1.2.

The test mode is set when voltage greater than V_{DD} is applied to either pin. Therefore, even during normal operation, the test mode is engaged when noise greater than V_{DD} is added, thus causing interference with normal operation.

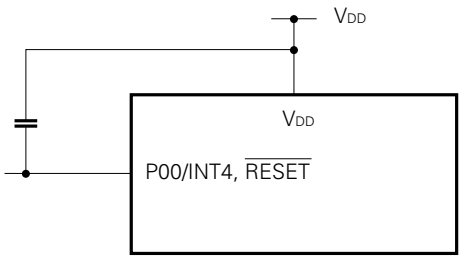
For example, this problem may occure if the P00/INT4 and $\overline{\text{RESET}}$ pins wiring is too long, causing line noise.

To avoid this, try to suppress line noise in wiring. If line noise is still high, try elimminating the noise using the exterior add-on components shown in the Figures below.

○ **CONNECT A DIODE WITH LOW VF BETWEEN THE V_{DD} AND THE PIN.**



○ **CONNECT A CONDENSER BETWEEN THE V_{DD} AND THE PIN.**



★ 2. DIFFERENCES BETWEEN μPD75P108B AND μPD75P116

In addition to the μPD75P108B, the μPD75P116 is available as μPD751×× series on-chip PROM device.

Parameter	μPD75P108B	μPD75P116
PROM capacity	8064 × 8 bits	16256 × 8 bits
Operating voltage range	2.7 to 6.0 V	5 V ±10%
Write voltage	12.5 V	12.5 V
Operating temperature range	–40 to +85 °C	–40 to +85 °C
Supply current TYP. value during operation	4 mA	5 mA
Supply current TYP. value in STOP mode	0.1 μA	0.5 μA
Power-on reset function	No	No
Package	• 64-pin plastic shrink DIP • 64-pin ceramic shrink DIP (with window) • 64-pin plastic QFP (14 × 20 mm, 1.0 mm pitch)	• 64-pin plastic shrink DIP • 64-pin plastic QFP (14 × 20 mm, 1.0 mm pitch)

3. DIFFERENCES BETWEEN MASK VERSION (μPD75108) AND PROM VERSION (μPD75P108B) ★

Parameter		μPD75P108B (PROM product)	μPD75108 (Mask ROM product)
Program memory		• 0000H to 1F7FH • 8064 × 8 bits	
Pull-up resistor of ports 12,13 and 14		No	Mask option
Power-on reset circuit		No	Mask option
Power-on reset			
Power-on Flag		2.7 to 6.0 V	
Operating voltage range			
Pin connection	SDIP (Nos. 33 to 36) QFP (Nos. 39 to 62)	P33/MD3 to P30/MD0	P33 to P30
	SDIP (No. 31) QFP (No. 57)	V_{PP}	NC
Electrical specification		Different consumption current, etc. Refer to the parameter for each data sheet for details.	
Other		Different noise resistance, noise radiation, etc., due to difference in the size of circuits and mask layout	

Note The PROM and ROM products differ in noise resistance and noise radiation. If you are considering replacement of the PROM product by the ROM product in the transition from preproduction to volume production, this should be evaluated thoroughly with the mask ROM CS product (not ES product).

4. PROM (PROGRAM MEMORY) WRITE AND VERIFY

The ROM built into the μPD75P108B is a 8064 × 8-bit PROM. The pins shown in the table below are used to write/verify this PROM. There is no address input; instead, a method to update the address by the clock input from the X1 pin is adopted.

Pin Name	Function
V_{PP}	Voltage applecation pin for program memory write/verify (normally V_{DD} potential).
X1, X2	Address update clock inputs for program memory write/ verify. Inverse of X1 pin signal is input to X2 pin.
MD0 to MD3	Operating mode selection pin for program memory write/ verify.
P40 to P43 (low-order 4 bits) P50 to P53 (high-order 4 bits)	8-bit data input/output pins for progrm memory write/ verify.
V_{DD}	Supply voltage application pin. Applies 2.7 to 6.0 V in normal operation, and 6 V for program memory write/verify.

Note Pins not used in a program memory write/verify operation should be connected to V_{SS} with a pull-down resistor.

4.1 PROGRAM MEMORY WRITE/VERIFY OPERATING MODES

The μPD75P108B assumes the program memory write/verify mode is +6 V and +12.5 V are applied respectively to the V_{DD} and V_{PP} pins. The table below shows the operating modes available by the MD0 to MD3 pin setting in this mode.

Operating Mode Setting						Operating Mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Program memory address zero-clear
		L	H	H	H	Write mode
		L	L	H	H	Verify mode
		H	×	H	H	Program inhibit mode

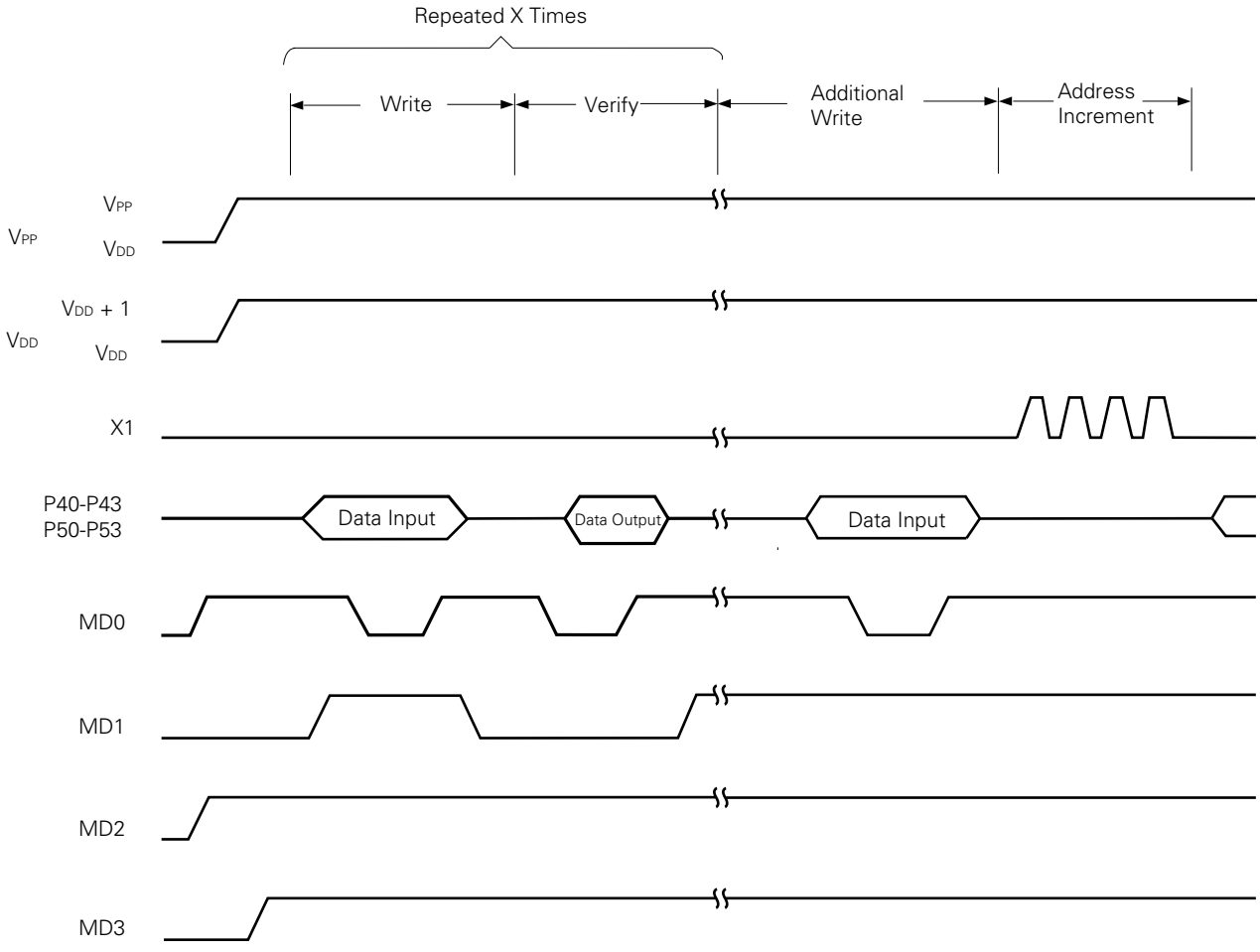
×: L or H

4.2 PROGRAM MEMORY WRITE PROCEDURE

The program memory writing procedure is shown below. High-speed write is possible.

(1) Pull down a pin which is not used to V_{SS} via the resistor. A low-level signal is input to the X1 pin.
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) 10 μs wait.
(4) The program memory address 0 clear mode.
(5) Supply +6 V and +12.5 V respectively to V_{DD} and V_{PP}.
(6) The program inhibit mode.
(7) Write data in the 1-ms write mode.
(8) The program inhibit mode.
(9) The verify mode. If written, proceed to (10); if not written, repeat (7) to (9).
(10) (Number of times written in (7) to (9): X) x 1-ms additional write.
(11) The program inhibit mode.
(12) Update (+1) the program memory address by inputting 4 pulses to the X1 pin.
(13) Repeat (7) to (12) up to the last address.
(14) The program memory address 0 clear mode.
(15) Change the V_{DD} and V_{PP} pins voltage to +5 V.
(16) Power off.

The diagram below shows the procedure of the above (2) to (12).

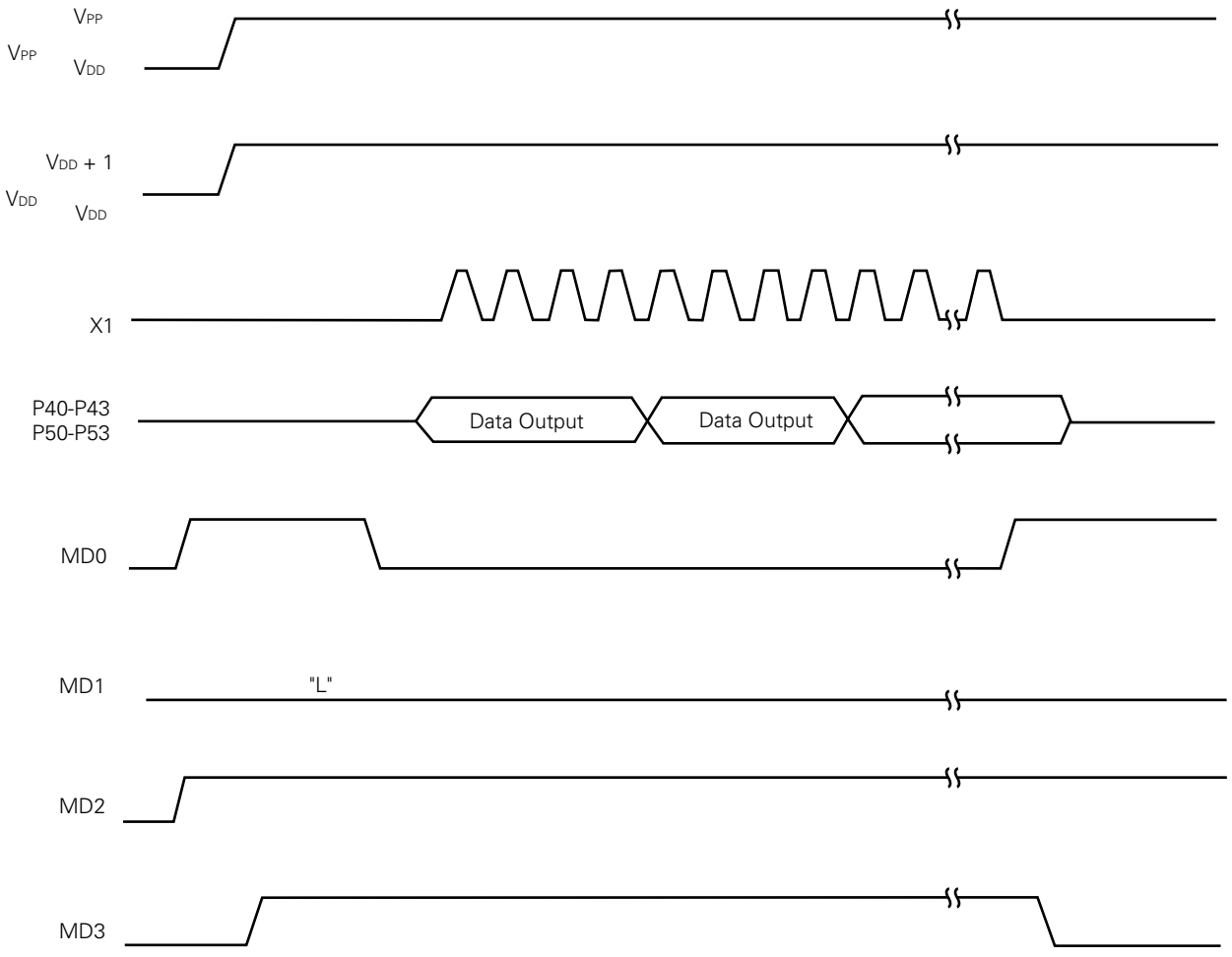


4.3 PROGRAM MEMORY READ PROCEDURE

The μPD75P108B can read the content of the program memory in the following procedure.

(1) Pull down a pin which is not used to V_{SS} via the resistor. A low-level signal is input to the X1 pin.
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) 10 μs wait.
(4) The program memory address 0 clear mode.
(5) Supply +6 V and +12.5 V respectively to V_{DD} and V_{PP}.
(6) The program inhibit mode.
(7) The verify mode. If clock pulses are input to the X1 pin, data is output sequentially 1 address at a time at the period of inputting 4 pulses.
(8) The program inhibit mode.
(9) The program memory address 0 clear mode.
(10) Change the V_{DD} and V_{PP} pins voltage to +5 V.
(11) Power off.

The diagram below shows the procedure of the above (2) to (9).



4.4 ERASURE METHOD (μPD75P108BDW only) ★

The data contents programmed in the μPD75P108BDW can be erased by exposure to ultra-violet rays via the upper window.

The wavelength of erasable UVR is approx. 250 nm. The irradiation amount required for complete erasure is 15Ws/cm² (UVR intensity × erasure time).

Erasure requires approx. 15 to 20 minutes if a commercially available UVR lamp (wavelength 254 nm, intensity 12 mW/cm²).

Note 1. If exposed directly to sunshine or a fluorescent light for a long period, the contents may be erased. For protection of the contents, mask the upper window with the lightshield cover film. Use the lightshield cover film provided by NEC for UV EPROM products.

2. When performing erasure, ensure that the distance between the UV lamp and the μPD75P108BDW is 2.5 cm or less.

Remarks The erasure time may be increased due to deterioration of the UV lamp, dirt or stains on the package window surface.

4.5 SCREENING OF ONE-TIME PROM PRODUCTS

Due to the nature of their construction, it is not possible for NEC to fully test one-time PROM products (μPD75P108BCW, μPD75P108BGF-3BE) before shipment. It is therefore recommended that screening which performs PROM verification be carried out after high-temperature storage under the conditions shown below once the necessary data has been written to the device.

Storage Temperature	Storage Time
125 °C	24 hours

NEC offers a fee-paying service under the QTOP microcomputer name which covers one-time PROM writing, marking, screening and verification. Please contact our salesman for details.

5. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS		RATING	UNIT
Supply voltage	V_{DD}			–0.3 to + 7.0	V
Supply voltage		V_{PP}		–0.3 to 13.5	V
Input voltage	V_{I1}	Except ports 12 to 14		–0.3 to V_{DD} + 0.3	V
	V_{I2} ***1**	Ports 12 to 14		–0.3 to +13	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Output current high	I_{OH}	1 pin		–15	mA
		Total pins		–30	mA
Output current low	I_{OL}***2**	1 pin	Peak value	30	mA
			Effective value	15	mA
		Ports 0, 2 to 4, 12 to 14 total	Peak value	100	mA
			Effective value	60	mA
		Ports 5 to 9 total	Peak value	100	mA
			Effective value	60	mA
Operating temperature	T_{opt}			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

* **1.** The power supply impedance (pull-up resistor) should be 50 kΩ or more when the voltage exceeding 10 V applied to ports 12, 13 and 14.

2. Effective value should be calculated as follows: [Effective value] = [Peak value] $\times \sqrt{\text{duty}}$

OPERATING VOLTAGES (Ta = –40 to +85 °C)

PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
CPU ***1**		***2**	6.0	V
Programmable threshold port (comparator input)		4.5	6.0	V
Other hardware ***1**		2.7	6.0	V

* **1.** Excluding system clock oscillation circuit and programmable threshold ports.

2. The operating voltage range varies depending on the CPU clock cycle time. See "AC characteristics".

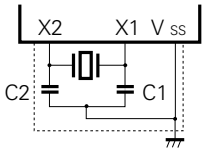
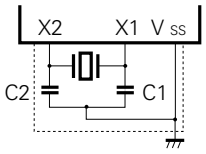
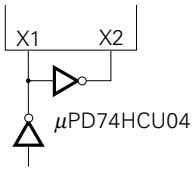
CAPACITANCE (Ta = 25 °C, V_{DD} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.			15	pF
Output capacitance	C_{OUT}				15	pF
I/O capacitance	C_{IO}				15	pF

COMPARATOR CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 4.5 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Comparison accuracy	V_{ACOMP}				±100	mV
Threshold voltage	V_{TH}		0		V_{DD}	V
PTH input voltage	V_{IPTH}		0		V_{DD}	V
Comparator circuit current consumption		PTHM7 set to "1"		1		mA

SYSTEM CLOCK OSCILLATION CIRCUIT CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

	RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
★	Ceramic resonator		Oscillator frequency (f_{XX}) ***1**	V_{DD} = Oscillation voltage range	2.0		***3** 5.0	MHz
			Oscillation stabilization time ***2**	After V_{DD} reaches oscillator voltage range MIN.			4	ms
★	Crystal resonator		Oscillator frequency (f_{XX}) ***1**		2.0	4.19	***3** 5.0	MHz
			Oscillation stabilization time ***2**	V_{DD} = 4.5 to 6.0 V			10	ms
							30	ms
	External clock		X1 input frequency (f_X) ***1**		2.0		5.0	MHz
			X1 input high/low level width (t_{XH}, t_{XL})		100		250	ns

*** 1.** Indicates only oscillation circuit characteristics.
Refer to "AC Characteristics" for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} impression or STOP mode release.

★ **3.** When using a value of f_X such that 4.19MHz<f_{XX}≤5.0MHz, if the maximum speed mode:$\Phi=f_X/4$ is set as the CPU clock frequency, 1 machine cycle becomes less than 0.95μs, with the result that the specified MIN value of 0.95 cannot be observed.

★ **Note When the system clock oscillator is used, the following points should be noted concerning wiring in the section enclosed by dots, in order to prevent the effects of wiring capacitance, etc.**

- Keep the wiring as short as possible.
- Do not cross any other signal lines, and keep clear of lines in which a high fluctuating current flows.
- Ensure that oscillator capacitor connection points are always at the same potential as V_{SS}. Do not ground in a ground pattern in which a high current flows.
- Do not take a signal from the oscillator.

RECOMMENDED CERAMIC RESONATOR

MANUFACTURER	PART NAME	FREQUENCY (MHz)	EXTERNAL CAPACITANCE		OSCILLATION VOLTAGE RANGE	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Murata Mfg. Co., Ltd.	CSAx.xxMG	2.00 to 5.00	30	30	2.7	6.0
	CSTx.xxMG	2.00 to 5.00	30	30		
	CSTx.xxMGW	2.45 to 5.00	30	30		
Kyocera Corporation	KBR-x.xMS	2.0 to 2.5	100	100	2.7	6.0
		2.6 to 6.0	33	33		
Toko, Inc.	CRHFx.xx	3.00 to 4.19	27	27	3.0	6.0

RECOMMENDED CRYSTAL RESONATOR

MANUFACTURER	PART NAME	FREQUENCY (MHz)	EXTERNAL CAPACITANCE		OSCILLATION VOLTAGE RANGE	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Kinseki, Ltd.	HC-49/U	2.00 to 5.00	22	22	2.7	6.0

DC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input voltage high	V_{IH1}	Other than below		0.7V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0 & 1, TI0 & 1, $\overline{RESET}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	Ports 12 to 14		0.7V_{DD}		12	V
	V_{IH4}	X1, X2		V_{DD}–0.5		V_{DD}	V
Input voltage low	V_{IL1}	Other than below		0		0.3V_{DD}	V
	V_{IL2}	Ports 0 & 1, TI0 & 1, $\overline{RESET}$		0		0.2V_{DD}	V
	V_{IH3}	X1, X2		0		0.4	V
Output voltage high	V_{OH}	V_{DD} = 4.5 to 6.0 V,	I_{OH} = –1 mA	V_{DD}–1.0			V
			I_{OH} = –100 μA	V_{DD}–0.5			V
Output voltage low	V_{OL}	V_{DD} = 4.5 to 6.0 V	Ports 0, 2, to 9, I_{OL} = 15 mA		0.35	2.0	V
			Ports 12 to 14, I_{OL} = 10 mA		0.35	2.0	V
		V_{DD} = 4.5 to 6.0 V,	I_{OL} = 1.6 mA			0.4	V
			I_{OL} = 400 μA			0.5	V
Input leakage current high	I_{LIH1}	V_{IN} = V_{DD}	Other than below			3	μA
	I_{LIH2}		X1, X2			20	μA
	I_{LIH3}	V_{IN} = 12 V	Ports 12 to 14			20	μA
Input leakage current low	I_{LIL1}	V_{IN} = 0 V	Except X1 & X2			–3	μA
	I_{LIL2}		X1, X2			–20	μA
Output leakage current high	I_{LOH1}	V_{OUT} = V_{DD}	Other than below			3	μA
	I_{LOH2}	V_{OUT} = 12 V	Ports 12 to 14			20	μA
Output leakage current low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Power supply current ***1**	I_{DD1}	4.19 MHz Crystal oscillation C1 = C2 = 22 pF	V_{DD} = 5 V ± 10 % ***2**		4	10	mA
			V_{DD} = 3 V ± 10 % ***3**		1	2.5	mA
	I_{DD2}		HALT mode V_{DD} = 5 V ± 10 %		600	1800	μA
			HALT mode V_{DD} = 3 V ± 10 %		200	600	μA
	I_{DD3}	STOP mode, V_{DD} = 3 V ± 10 %			0.1	10	μA

* **1.** Not including current flowing in comparator.

2. When processor clock control register (PCC) is set to 0011 and CPU is operating in high-speed mode.

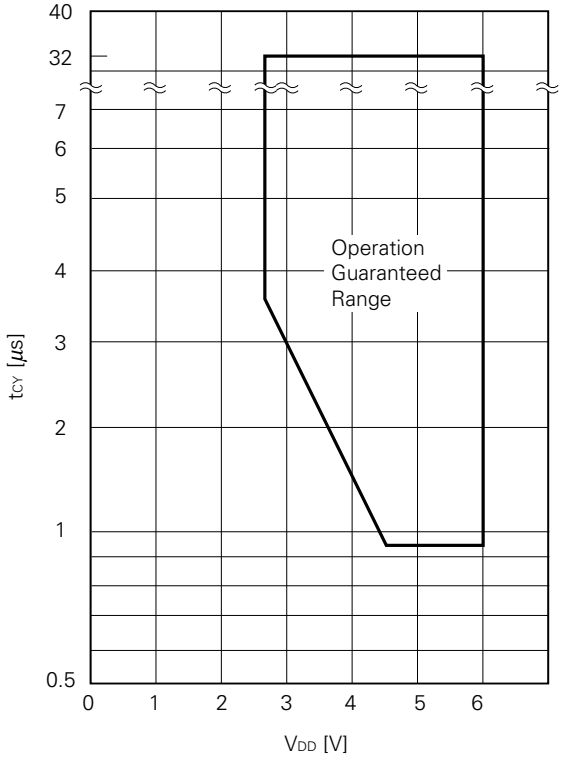
3. When PCC is set to 0000 and CPU is operating in low-speed mode.

AC CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
CPU clock cycle time* (minimum instruction execution time = 1 machine cycle)	t_{CY}	V_{DD} = 4.5 to 6.0 V		0.95		32	μs ★
				3.8		32	μs
TI0, TI1 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		1	MHz
				0		275	kHz
TI0, TI1 input high/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.48			μs
				1.8			μs
$\overline{SCK}$ cycle time	t_{KCY}	V_{DD} = 4.5 to 6.0 V	Input	0.8			μs
			Output	0.95			μs
			Input	3.2			μs
			Output	3.8			μs
$\overline{SCK}$ high/low-level width	t_{KH}, t_{KL}	V_{DD} = 4.5 to 6.0 V	Input	0.4			μs
			Output	t_{KCY}/2–50			ns
			Input	1.6			μs
			Output	t_{KCY}/2–150			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK}			100			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI}			400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO}	V_{DD} = 4.5 to 6.0 V				300	ns
						1000	ns
INT0 to INT4 high/low-level width	t_{INTH}, t_{INTL}			5			μs
$\overline{RESET}$ low level width	t_{RSL}			5			μs

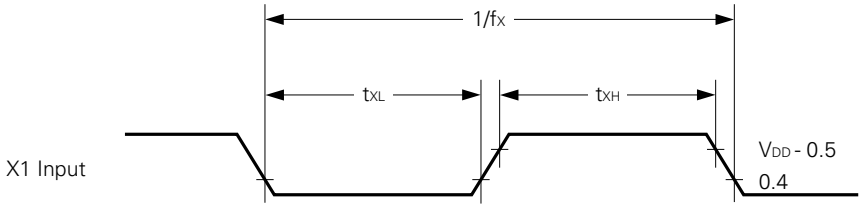
* The cycle time of the CPU clock (Φ) is determined by the oscillator frequency of the connected resonator and the processor clock control register (PCC). The graph on the right shows cycle time t_{CY} characteristics against supply voltage V_{DD} when system clock is operated.

t_{CY} vs. V_{DD} ★

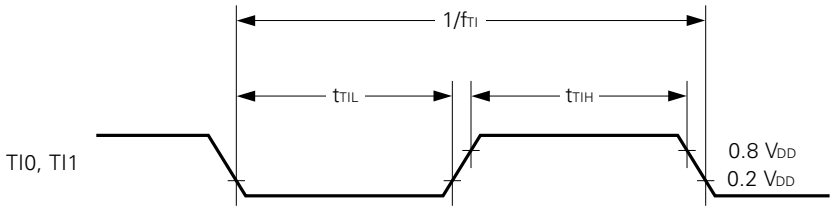


AC Timing Test Point (Excluding ports 0 & 1, TI0, TI1, X1, X2, $\overline{\text{RESET}}$)

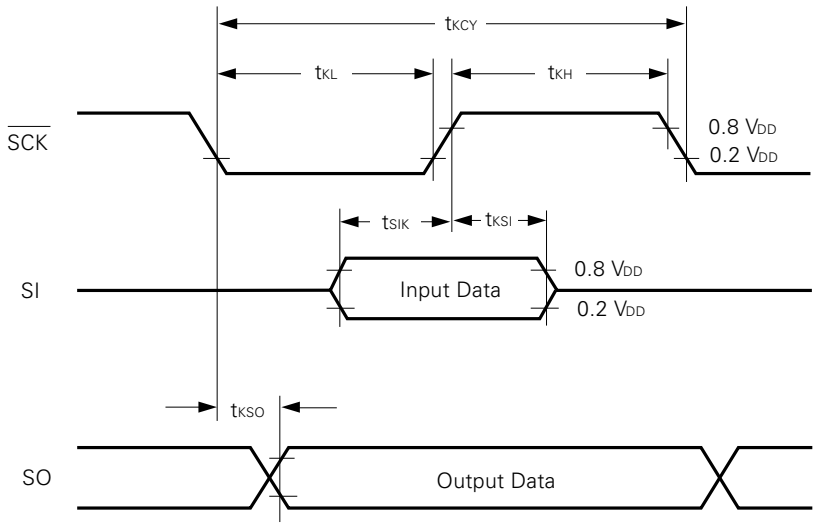
Clock Timing



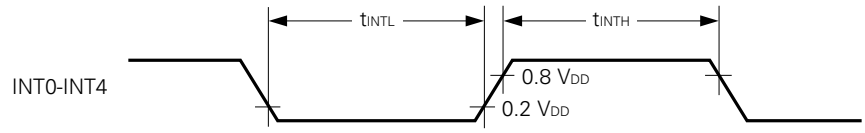
TI0, TI1 Input Timing



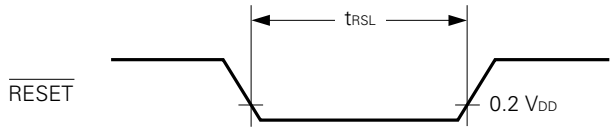
Serial Transfer Timing



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (Ta = –40 to +85 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention supply voltage	V_{DDDR}		2.0		6.0	V
Data retention power supply current ***1**	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_x$		ms
		Release by interrupt request		***3**		ms

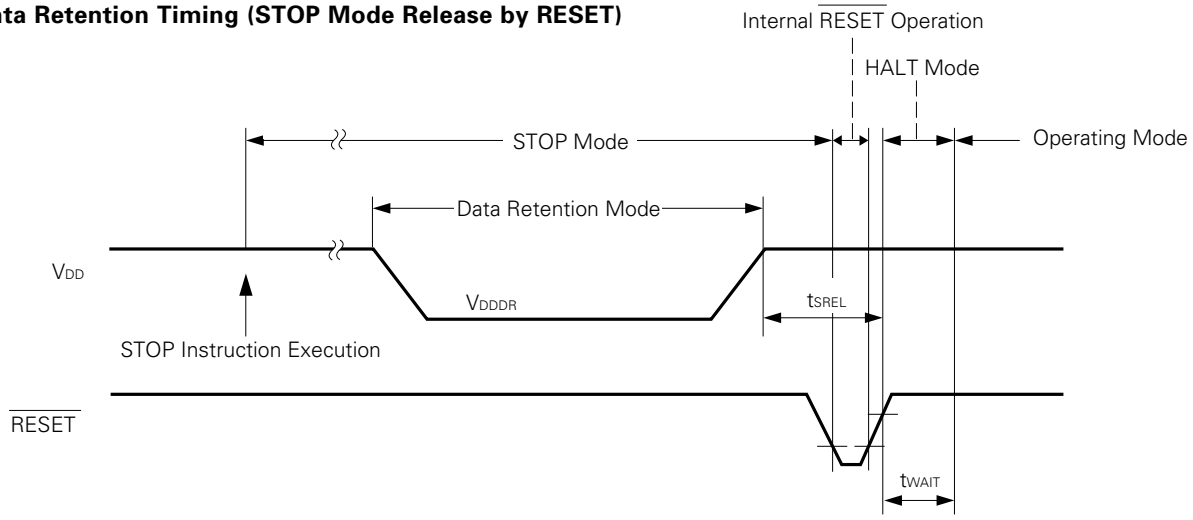
* **1.** Does not include current flowing in the comparator.

2. The oscillator stabilization wait time is the time during which CPU operation is halted to prevent unstable operation when oscillation begins.

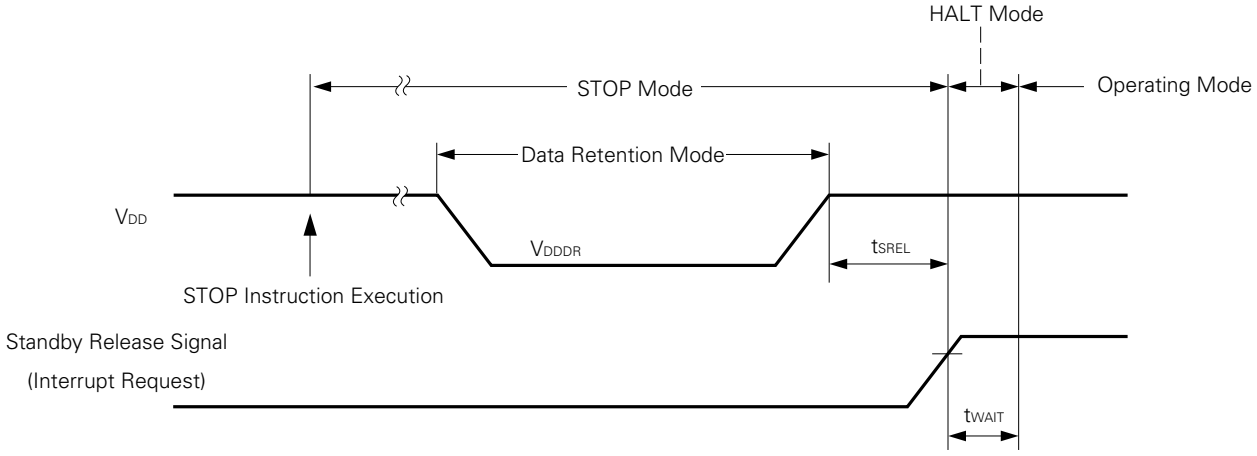
3. Depends on the setting of the basic interval timer mode register (BTM) (table below).

BTM3	BTM2	BTM1	BTM0	WAIT Time (Figure in Parentheses is for f_{XX} = 4.19 MHz)
–	0	0	0	$2^{20}/f_{XX}$ (Approx. 250 ms)
–	0	1	1	$2^{17}/f_{XX}$ (Approx. 31.3 ms)
–	1	0	1	$2^{15}/f_{XX}$ (Approx. 7.82 ms)
–	1	1	1	$2^{13}/f_{XX}$ (Approx. 1.95 ms)

Data Retention Timing (STOP Mode Release by $\overline{RESET}$)



Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



DC PROGRAMMING CHARACTERISTICS (Ta = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.3 V, V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input voltage high	V_{IH1}	Except X1 & X2	$0.7V_{DD}$		V_{DD}	V
	V_{IH2}	X1, X2	V_{DD}–0.5		V_{DD}	V
Input voltage low	V_{IL1}	Except X1 & X2	0		$0.3V_{DD}$	V
	V_{IL2}	X1, X2	0		0.4	V
Input leakage current	I_{LI}	$V_{IN} = V_{IL}$ or V_{IH}			10	μA
Output voltage high	V_{OH}	I_{OH} = –1 mA	V_{DD}–1.0			V
Output voltage low	V_{OL}	I_{OL} = 1.6 mA			0.4	V
V_{DD} supply current	I_{DD}				30	mA
V_{PP} supply current	I_{PP}	MD0 = V_{IL}, MD1 = V_{IH}			30	mA

Note 1. Ensure that V_{PP} does not reach +13.5 V or above including overshot.

2. Ensure that V_{DD} is applied before V_{PP} and cut off after V_{PP}.

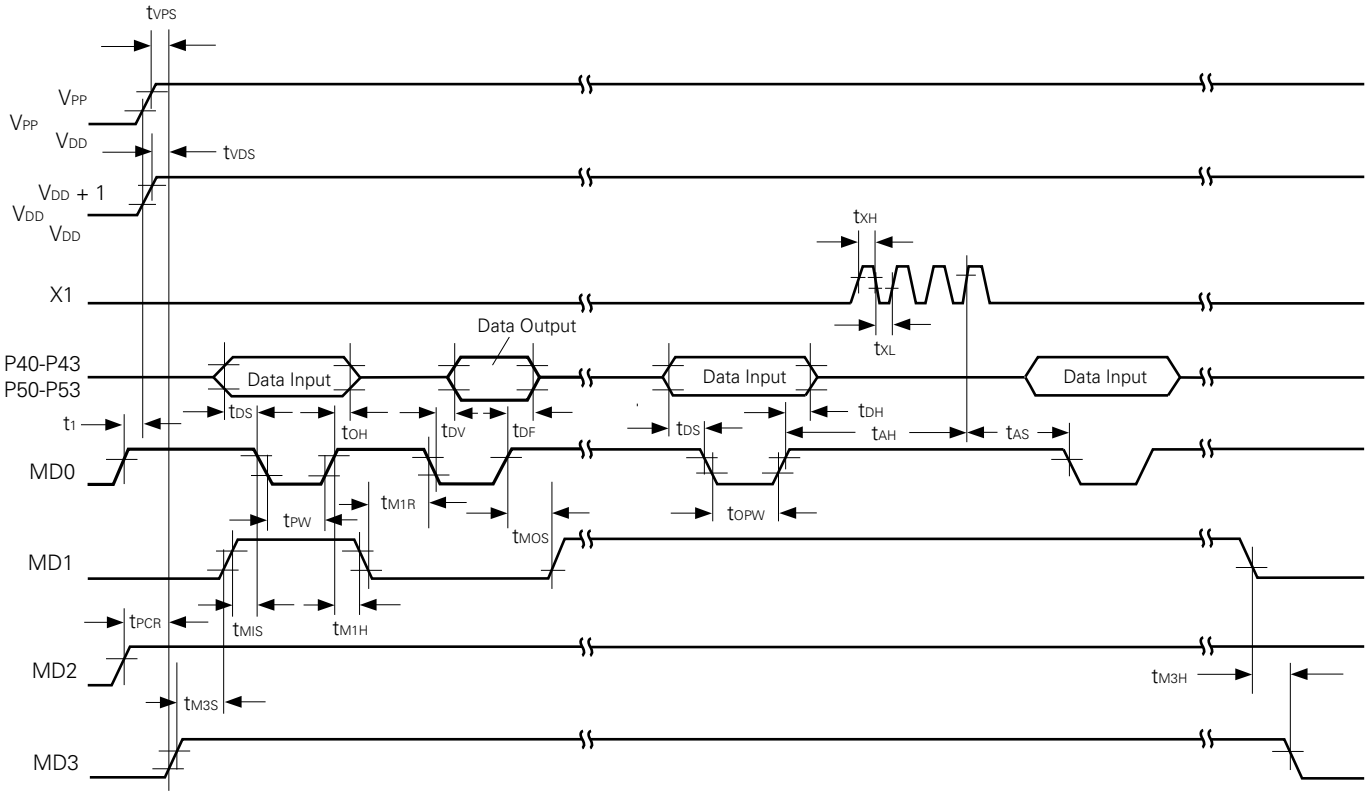
AC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.3 V, V_{SS} = 0 V)

	PARAMETER	SYMBOL	*1	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Address setup time *2 (to MD0↓)	t_{AS}	t_{AS}		2			μs
	MD1 setup time (to MD0↓)	t_{M1S}	t_{OES}		2			μs
	Data setup time (to MD0↓)	t_{DS}	t_{DS}		2			μs
	Address hold time *2 (from MD0↑)	t_{AH}	t_{AH}		2			μs
	Data hold time (from MD0↑)	t_{DH}	t_{DH}		2			μs
	Data output float delay time from MD0↑	t_{DF}	t_{DF}		0		130	ns
	V_{PP} setup time (to MD3↑)	t_{VPS}	t_{VPS}		2			μs
	V_{DD} setup time (to MD3↑)	t_{VDS}	t_{VCS}		2			μs
	Initial program pulse width	t_{PW}	t_{PW}		0.95	1.0	1.05	ms
	Additional program pulse width	t_{OPW}	t_{OPW}		0.95		21.0	ms
	MD0 setup time (to MD1↑)	t_{MOS}	t_{CES}		2			μs
	Data output delay time from MD0↓	t_{DV}	t_{DV}	MD0 = MD1 = V_{IL}			1	μs
	MD1 hold time (from MD0↑)	t_{M1H}	t_{OEH}	$t_{M1H} + t_{M1R} \geq 50$ μs	2			μs
	MD1 recovery time (from MD0↓)	t_{M1R}	t_{OR}		2			μs
	Program counter reset time	t_{PCR}	—		10			μs
	X1 input high-/low-level width	t_{XH}, t_{XL}	—		0.125			μs
	X1 input frequency	f_X	—				4.19	MHz
	Initial mode setting time	t_I	—		2			μs
	MD3 setup time (to MD1↑)	t_{M3S}	—		2			μs
	MD3 hold time (from MD1↓)	t_{M3H}	—		2			μs
	MD3 setup time (to MD0↓)	t_{M3SR}	—	In program memory read	2			μs
★	Address *2 data output delay time	t_{DAD}	t_{ACC}	In program memory read			2	μs
	Address *2 data output hold time	t_{HAD}	t_{OH}	In program memory read	0		130	ns
	MD3 hold time (from MD0↑)	t_{M3HR}	—	In program memory read	2			μs
★	Data output float delay time from MD3↓	t_{DFR}	—	In program memory read			2	μs

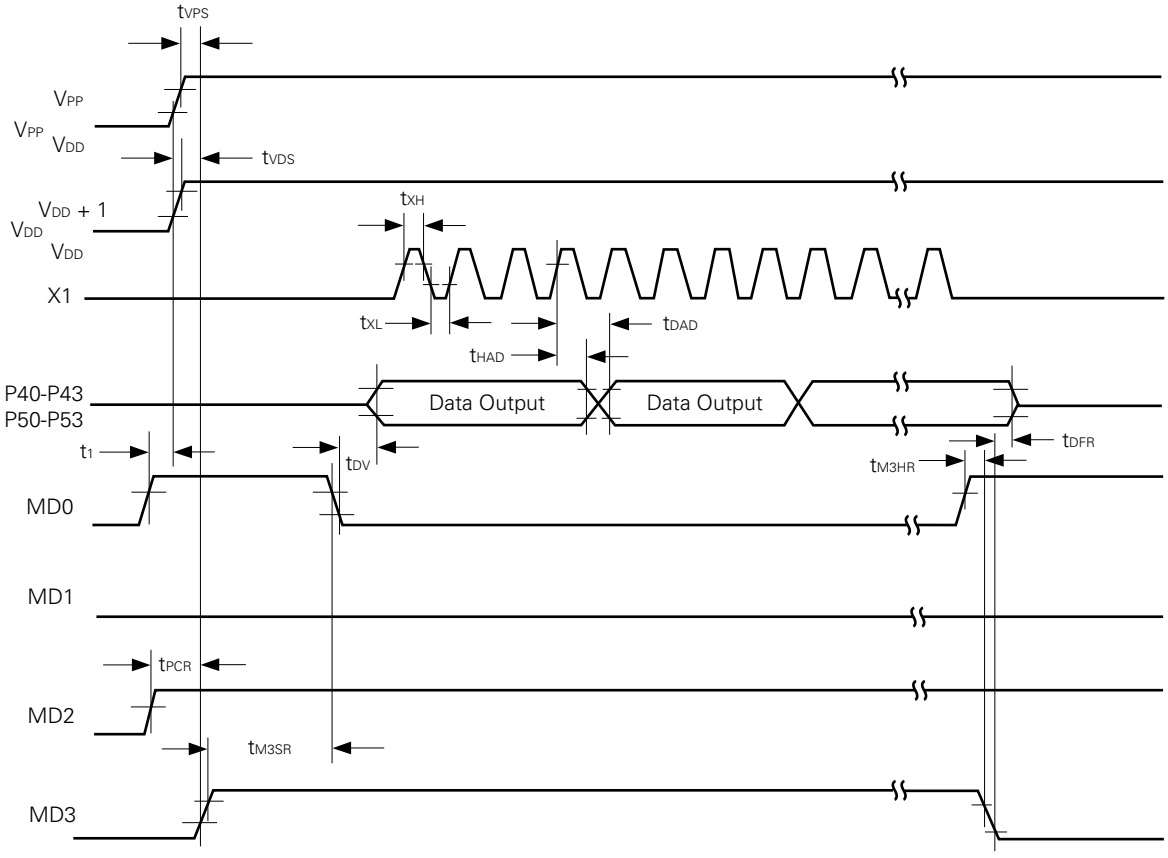
★ * **1.** Corresponding to μPD27C256A symbol.

2. Internal address signal is incremented by 1 on rise of 4th X1 input, and is not connected to a pin.

Program Memory Write Timing

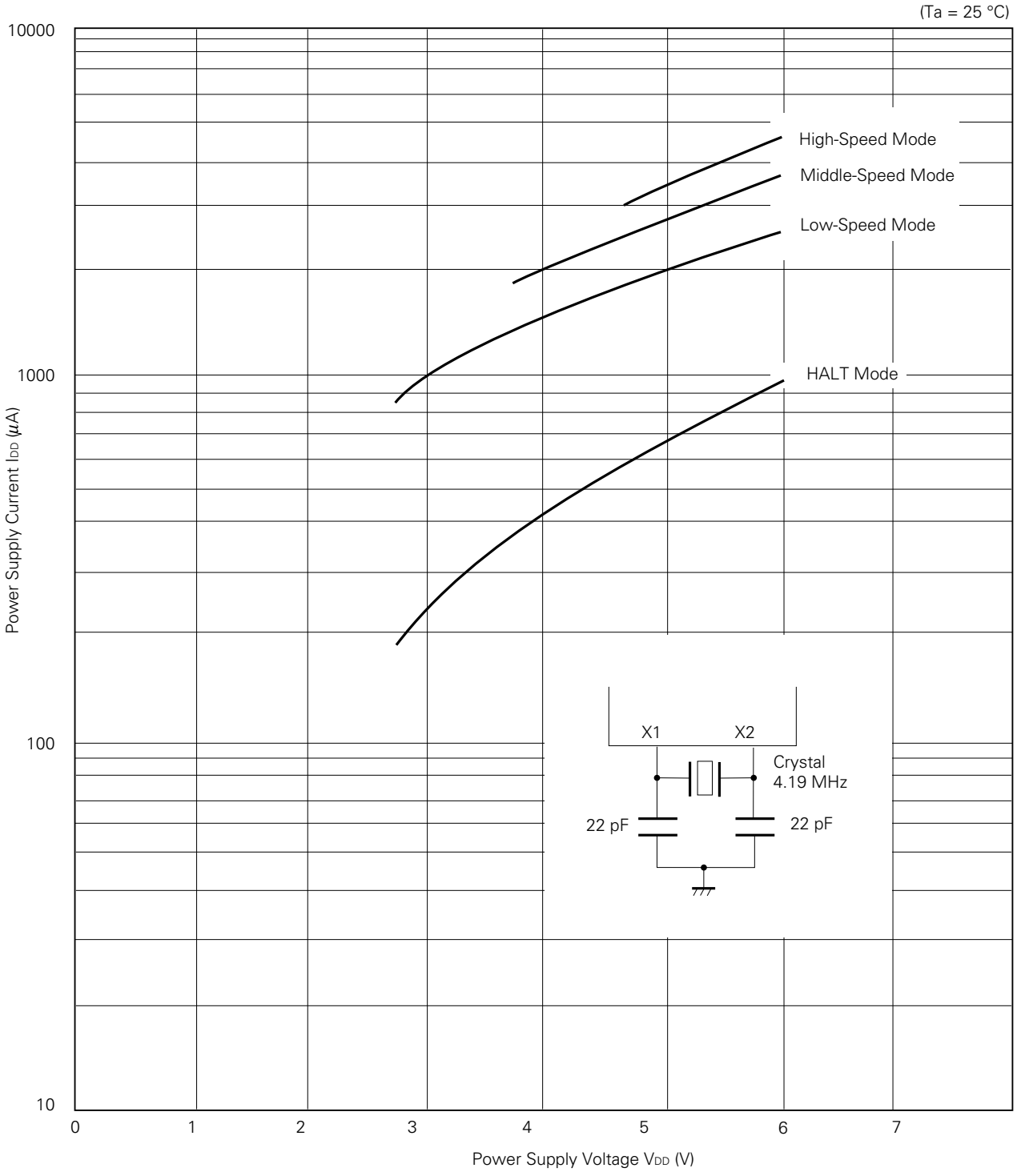


Program Memory Read Timing

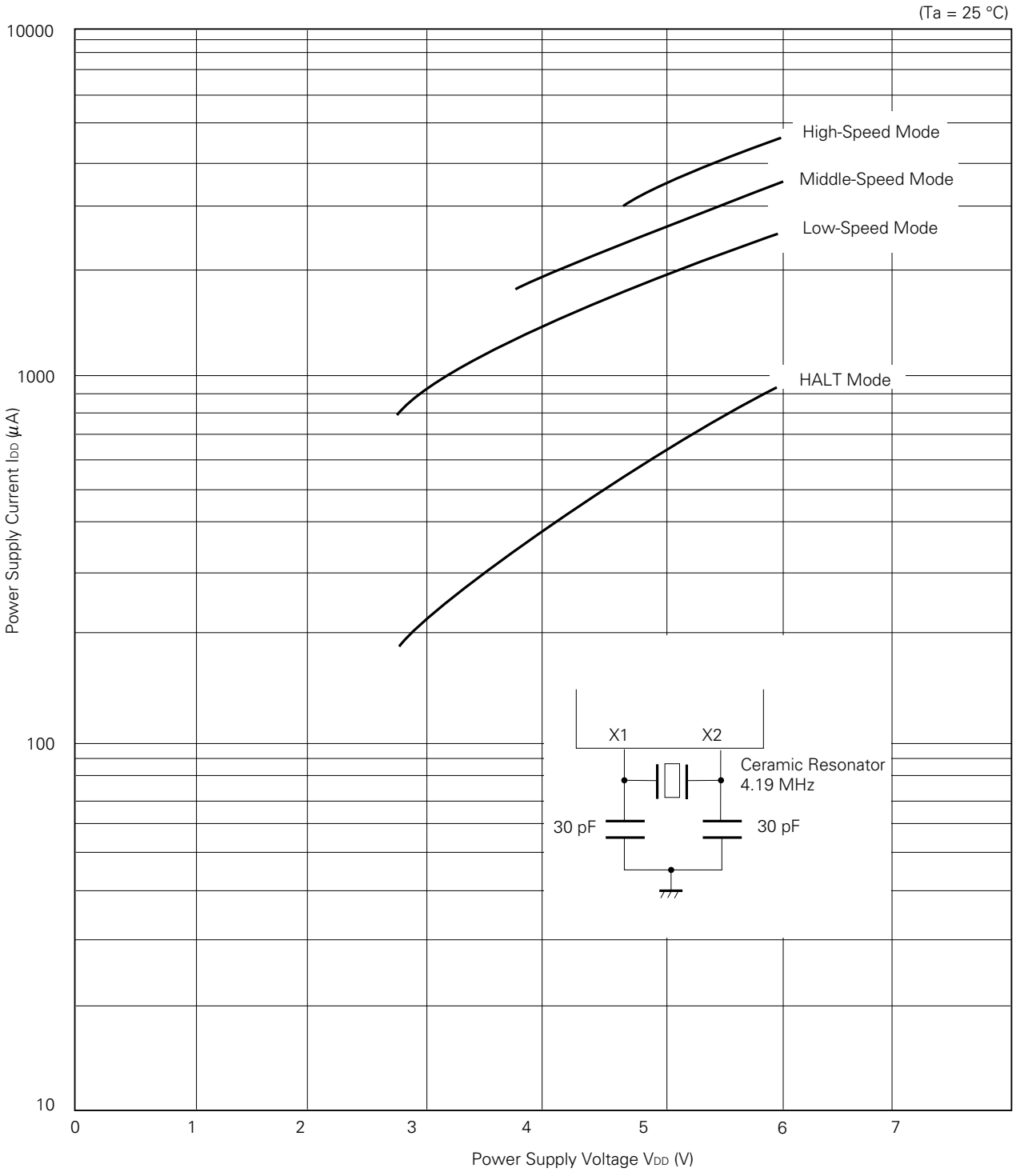


6. CHARACTERISTIC CURVE (REFERENCE VALUE)

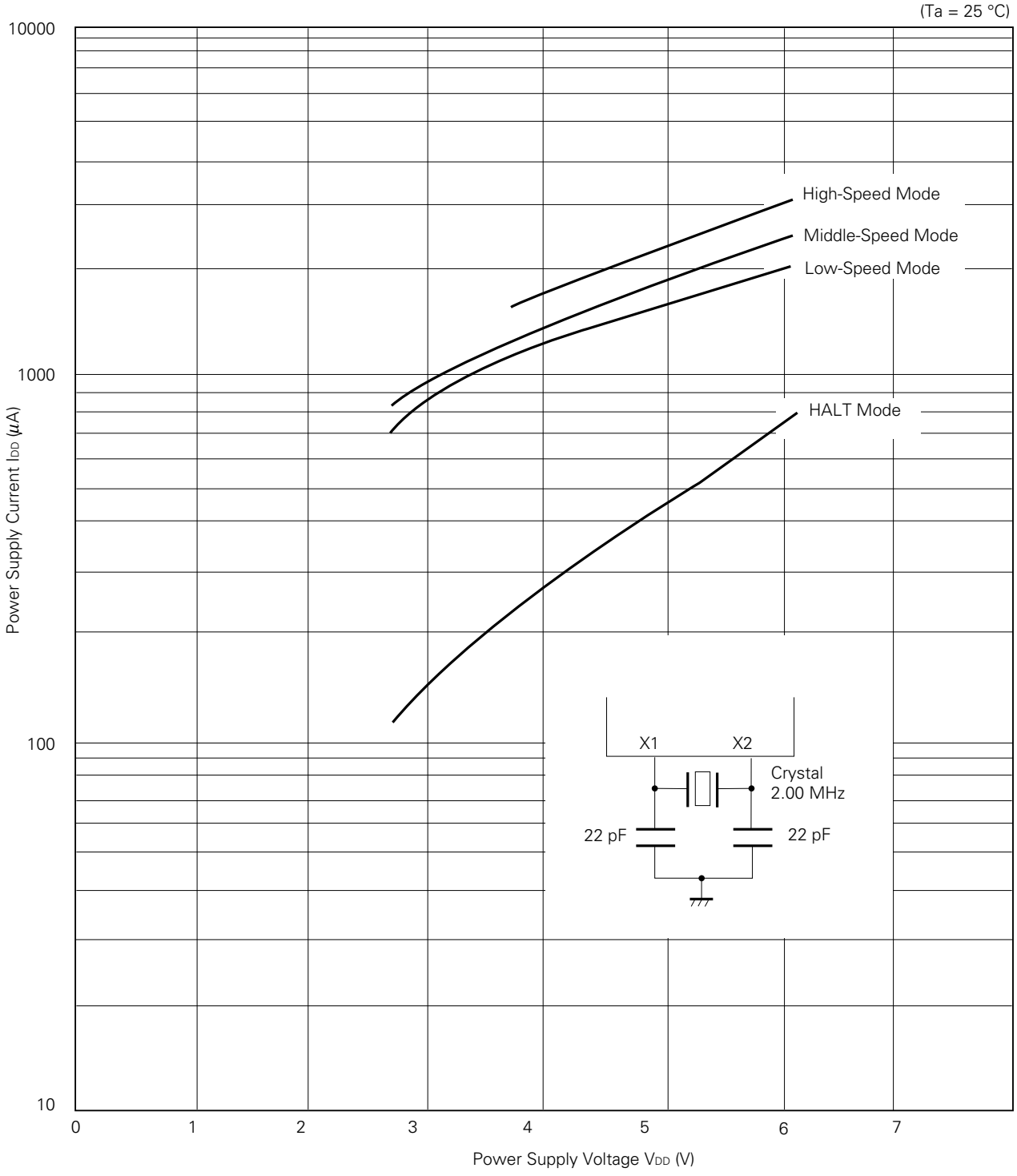
I_{DD} vs V_{DD} (Crystal Oscillation)



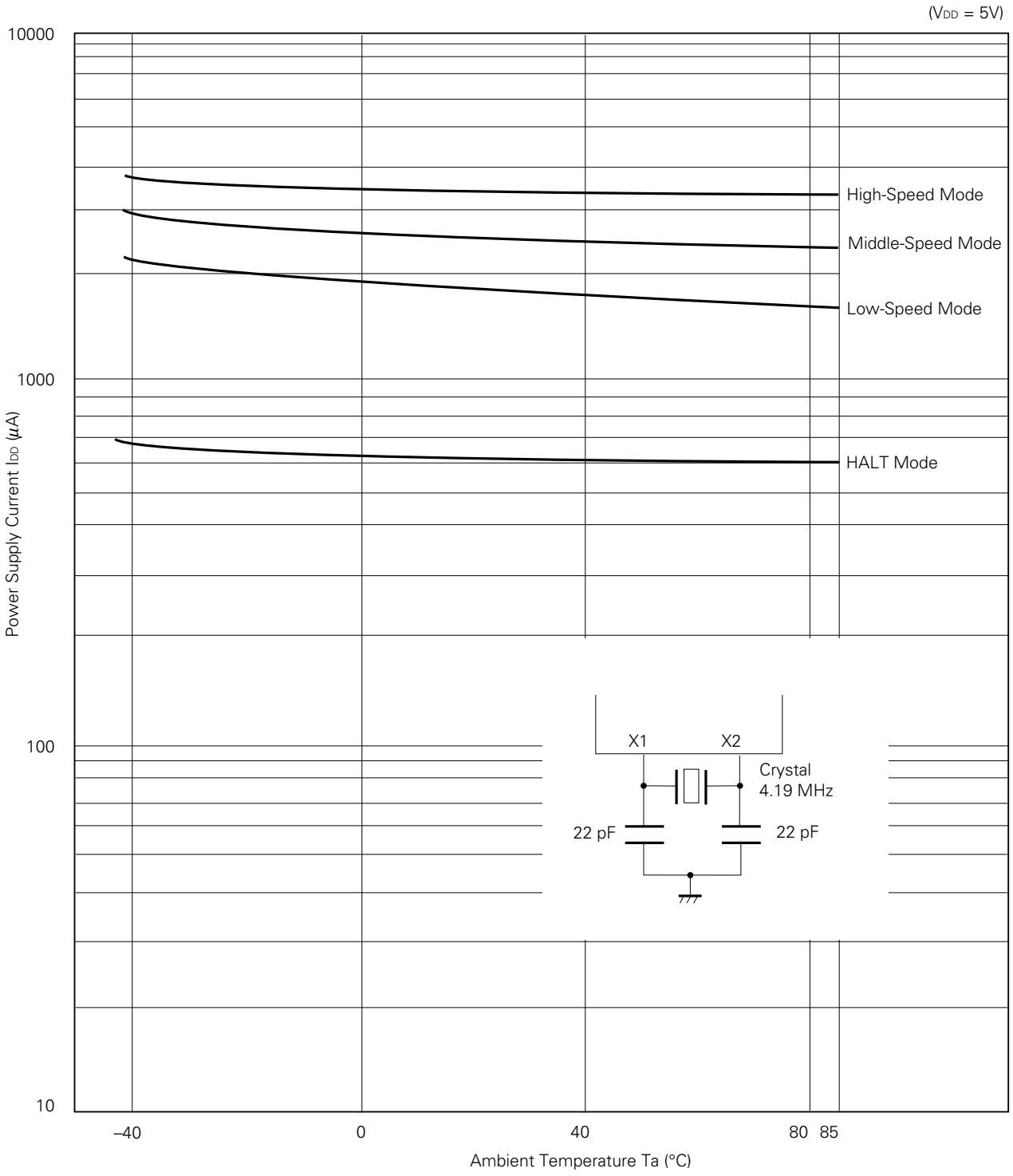
I_{DD} vs V_{DD} (Ceramic Oscillation)



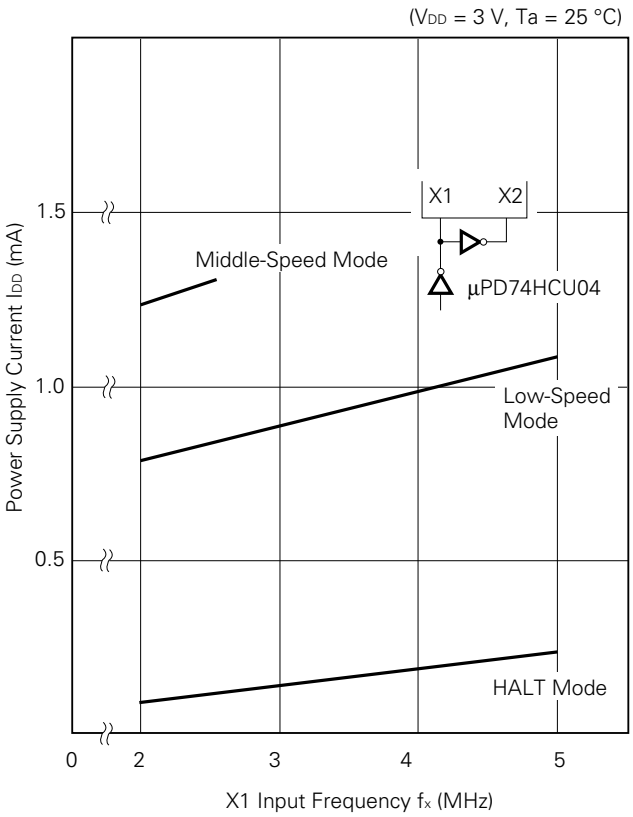
I_{DD} vs V_{DD} (Crystal Oscillation)



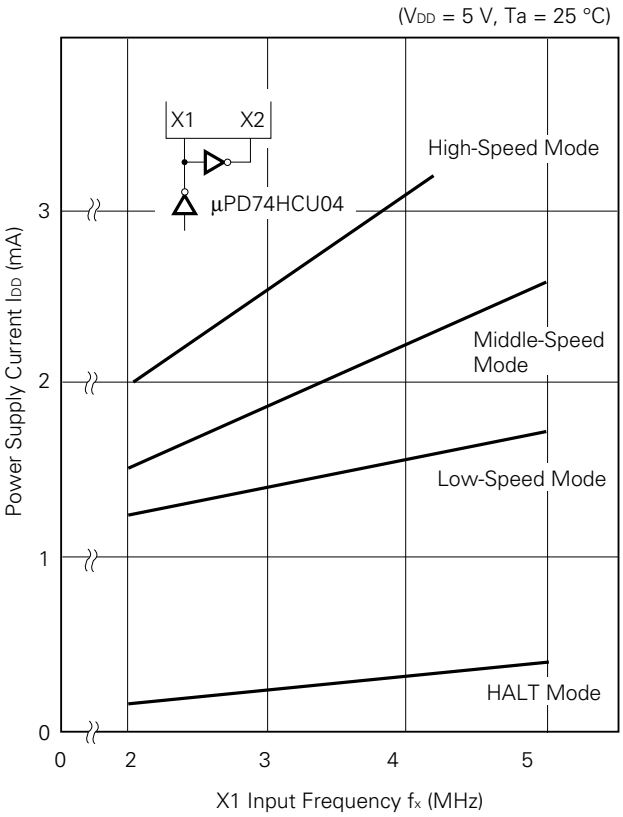
I_{DD} vs T_a (Crystal Oscillation)



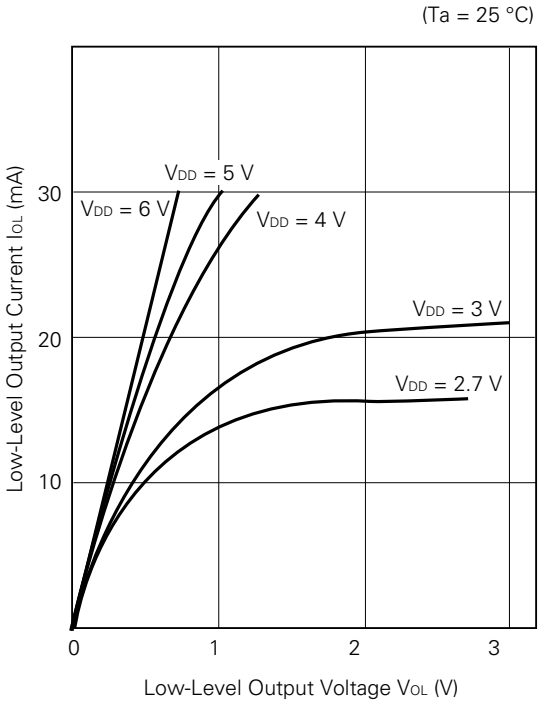
I_{DD} vs f_X (External Clock)



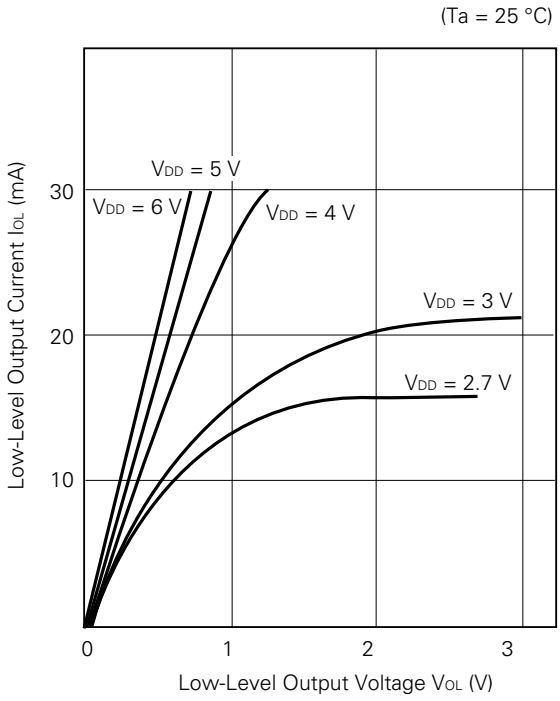
I_{DD} vs f_X (External Clock)



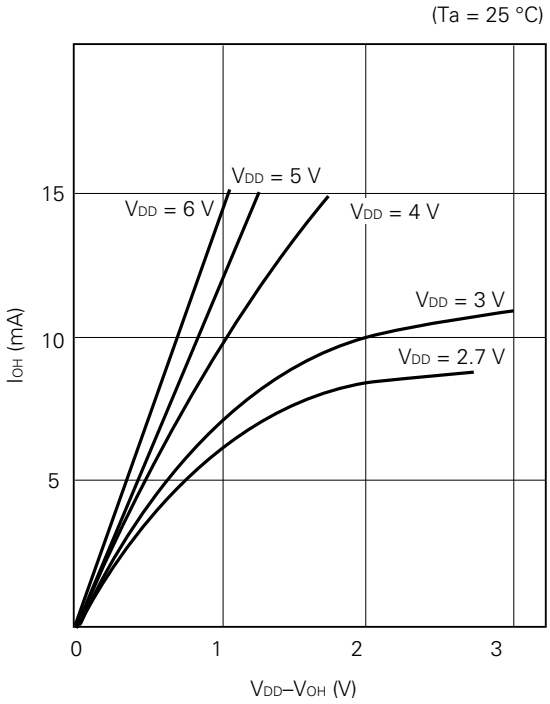
V_{OL} vs I_{OL} (Ports 12, 13 and 14)



V_{OL} vs I_{OL} (Ports 0 and 2 to 9)



V_{DD} – V_{OH} vs I_{OH}



★ 7. RECOMMENDED SOLDERING CONDITIONS

The μPD75P108B should be mounted under the conditions recommended in the table below.

For details of recommended soldering conditions for the surface mounting type, refer to the information document "Surface Mount Technology Manual" (IEI-1207)

For soldering methods and conditions other than those recommended below, contact our salesman.

Table 7-1 Surface Mount Type Soldering Conditions

μPD75P108BGF-3BE : 64-pin plastic QFP (14 × 20 mm, 1.0 mm pitch)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230°C, Duration: 30 sec. max. (at 210°C or above), Number of times: Once Time limit: 2 days* (thereafter 16 hours prebaking required at 125°C)	IR30-162-1
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (at 200°C or above), Number of times: 0nce Time limit: 2 days* (thereafter 16 hours prebaking required at 125°C)	VP15-162-1
Wave soldering	Solder bath temperature: 260°C max., Duration: 10 sec. max Number of times: Once Preheating temperature: 120°C max. (package surface temperature), Time limit: 2days* (thereafter 16 hours prebaking required at 125°C)	WS60-162-1
Pin part heating	Pin part temperature: 300°C max., Duration 3 sec. max. (per device lead)	Pin part heating

***** For the storage period after dry-pack decapsulation, storage conditions are max. 25°C, 65% 1H.

Note Use of more than one soldering method should be avoided (except in the case of pin part heating).

Table 7-2 Insertion Type Soldering Conditions

μPD75P108BCW : 64-pin plastic shrink DIP (750 mil)
μPD75P108BDW : 64-pin ceramic shrink DIP (with window)

Soldering Method	Soldering Conditions
Wave Soldering (lead part only)	Solder bath temperature: 260°C max., Duration: 10sec. max.
Pin part heating	Pin part temperature: 260°C max., Duration: 10sec. max.

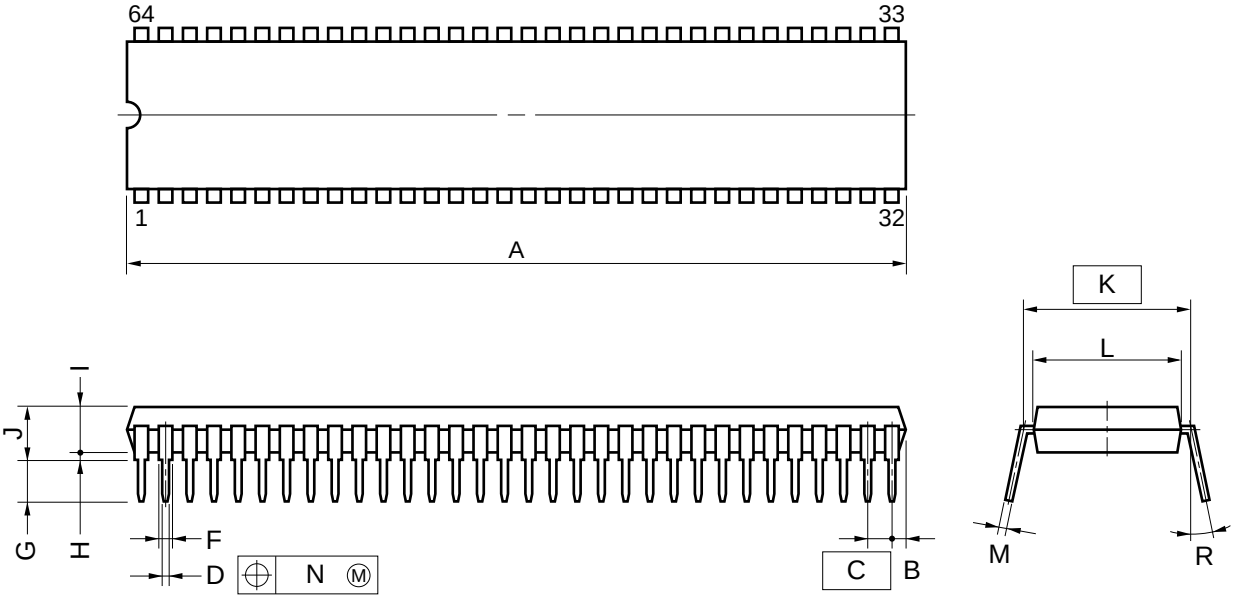
Note Ensure that the application of (wave soldering) is limited to the lead part and no solder touches the main unit directly.

For Your Information

Products to improve the recommended soldering conditions are available.
(Improvements: Extension of the infrared reflow peak temperature to 235°C, doubled frequency, increased life, etc.)
For further details, consult our sales personnel.

8. PACKAGE INFORMATION

64 PIN PLASTIC SHRINK DIP (750 mil)



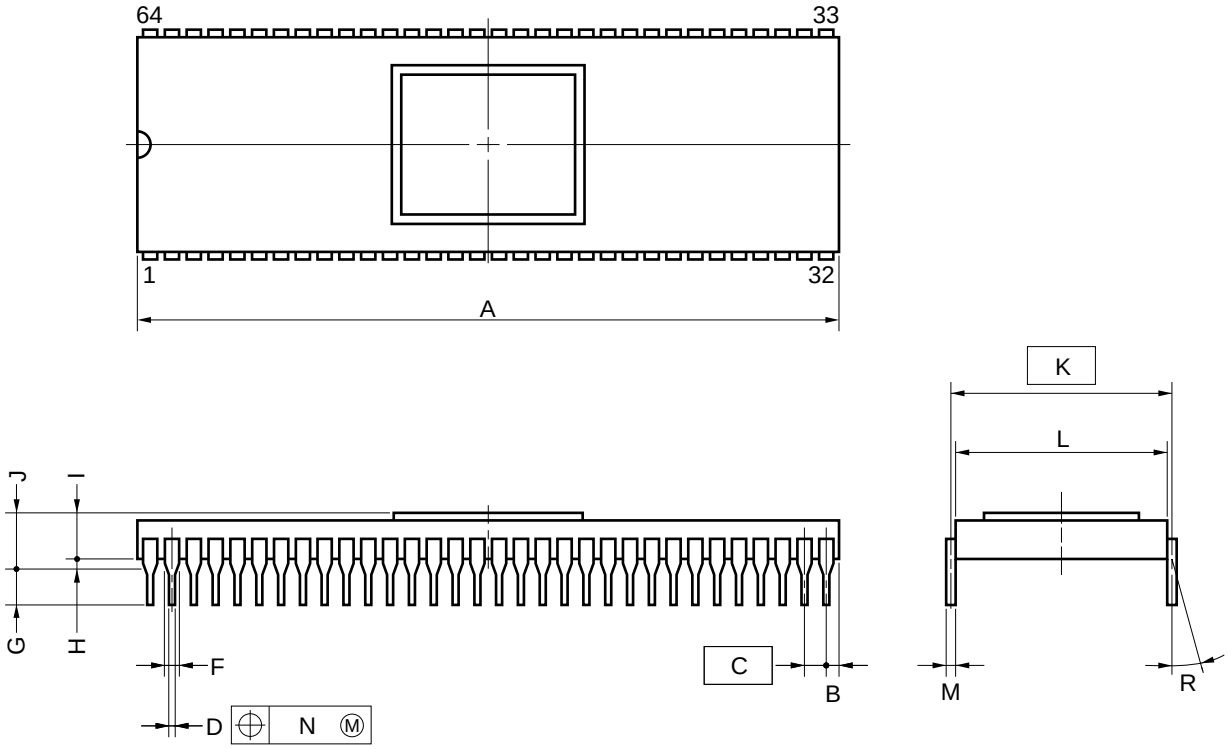
NOTE

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

64 PIN CERAMIC SHRINK DIP (SEAM WELD) (750 mil)



NOTES

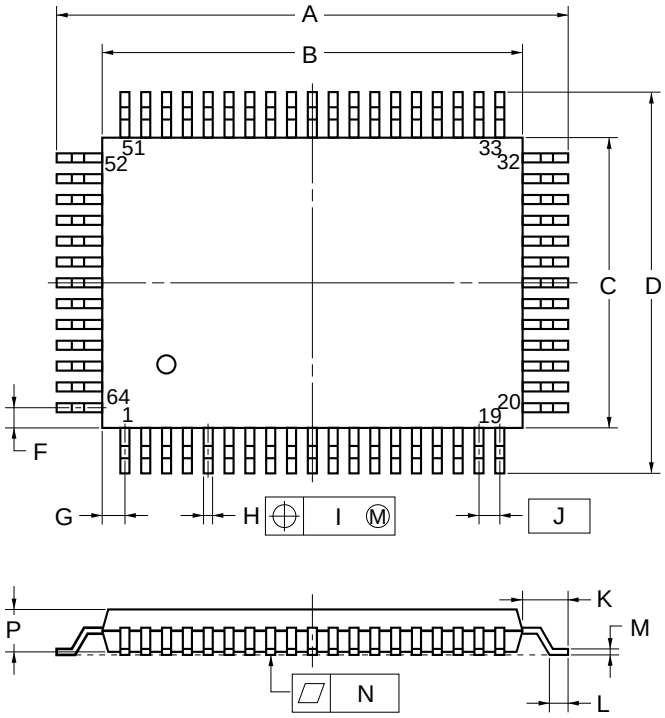
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

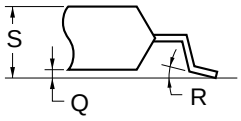
ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.310 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.46±0.05	0.018±0.002
F	0.8 MIN.	0.031 MIN.
G	3.5±0.3	0.138±0.012
H	1.0 MIN.	0.039 MIN.
I	2.62	0.103
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	18.8	0.740
M	0.25±0.05	$0.010^{+0.002}_{-0.003}$
N	0.25	0.01
R	0~15°	0~15°

P64D-70-750A-1

64 PIN PLASTIC QFP (14×20)



detail of lead end



NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.008}_{-0.009}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P64GF-100-3B8,3BE,3BR-2

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD75P108B.

Hardware	IE-75000-R ***1** IE-75001-R		In-circuit emulator for 75X series
	IE-75000-R-EM ***2**		Emulation board for IE-75000-R and IE-75001-R
	EP-75108CW-R		Emulation probe for μPD75P108BCW
	EP-75108GF-R	EV-9200G-64	Emulation probe for μPD75P108BGF A 64-pin conversion socket EV-9200G-64 is provided.
	PG-1500		PROM programmar
	PA-75P108CW		This is a PROM programmar adopter for μPD75P108BCW and connects to PG-1500.
	PA-75P116GF		This is a PROM programmar adopter for μPD75P108BGF and connects to PG-1500.
Software	IE control program		Host machine PC-9800 series (MS-DOS™ Ver.3.30 to Ver.5.00A ***3**) PC/AT™ series (PC-DOS™ Ver.3.10)
	PG-1500 controller		
	RA75X relocatable assembler		

***** **1** Maintenance product

2 This is not incorporated in the IE-75001-R.

3 A task swap function is not provided with Ver.5.00/5.00A; however, a task swap function cannot be used with this software.

APPENDIX B. RELATED DOCUMENTATIONS

List of Device-Related Documentations

Document Name		Document No.
User's Manual		IEM-922
Instruction Using Table		IEM-902
Application Note	(I) Introductory Volume	IEM-980
	(II) Remote-Controlled Reception Volume	IEM-5003
	(III) Bar-Code Reade-Volume	IEM-5065
	(IV) IC Control for MSK Transmission/Reception Volume	IEA-694
75X Series Selection Guide		IF-151

List of Development Tool Related Documentations

Document Name			Document No.
Hardware	IE-75000-R/IE-75001-R User's Manual		EEU-846
	IE-75000-R-EM User's Manual		EEU-673
	EP-75108CW-R User's Manual		EEU-696
	EP-75108GF-R User's Manual		EEU-695
	PG-1500 User's Manual		EEU-651
Software	RA75X Assembler Package User's Manual	Operation Volume	EEU-731
		Language Volume	EEU-730
	PG-1500 Controller User's Manual		EEU-704

Other Documentations

Document Name	Document No.
Package Manual	IEI-635
Surface Mount Technology Manual	IEI-1207
Quality Grade on NEC Semiconductor Devices	IEI-1209
NEC Semiconductor Device Reliability Quality Control	IEM-5068
Static Discharge (ESD) Test	MEM-539
Semiconductor Device Quality Guarantee Guide	MEI-603
Microcomputer Related Product Guide Other Manufacturer Volume	MEI-604

Note The above related documentations may be changed without notice. Be sure to use the latest documentations for designations.

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APPENDIX C. FONCTIONAL DIFFERENCES AMONG μPD751×× SERIES

Item \ Product Name		μPD75104/106/108/112/116	μPD75104A/108A	μPD75108F/112F/116F
ROM (byte)		4K/6K/8K/12K/16K (Mask ROM)	4K/8K (Mask ROM)	8K/12K/16K (Mask ROM)
RAM (× 4 bits)		320/320/512/512/512	320/512	512
Instruction set		75X High-End		
I/O Port	Total	58		
	CMOS input	10	10 (Pull resistor mask option : 4)	10
	CMOS input/output	32 (LED can be driver directly)	32 (Pull-up resistor mask option : 24, LED can be driverndirectly)	32 (LED can be driver directly)
	N-ch open-drain output	12 (LED can be driven directly)		
	Withstand Voltage	+12 V		+10 V
	Pull-up resistor	Can be incorporated by mask option		
	Analog input	4 (4-bit accuracy)		
Power-on reset circuit		Incorporated (mask option)		No
Power-on flag				
Operating voltage		2.7 to 6.0 V		2.7 to 5.0 V (Ta = –40 to +50°C) 2.8 to 5.0 V
Operating temperature rang		–40 to 85C°		–40 to +60 °C
Minimum instruction excution time		0.95 μs (Operation at 4.5 to 6.0 V) 3.8 μs (Operation at 2.7 V)		0.95 μs (Operation at 4.5 to 5.0 V) 1.91 μs (Operation at 2.7 V)
Package ***3**		• 64-pin plastic shrink DIP • 64-pin plastic QFP (GF-3BE)	• 64-pin plastic QFP (GC-AB8) • 64-pin plastic QFP (G-22) : μPD75108A only	• 64-pin plastic QFP (GF-3BE)

* **1.** Under development

2. Can be used as 75X High-End by 16K-byte mode/24K-byte mode switching function

3. There are four kinds of plastic QFP.

- •GC-AB8 ..... 14 × 14 × 2.55 mm, 0.8 mm pitch
- •GF-3BE ..... 14 × 20 × 2.7 mm, 1.0 mm pitch
- •G-22 ..... 14 × 14 × 1.5 mm, 0.8 mm pitch
- •GK-8A8 ..... 12 × 12 × 1.4 mm, 0.65 mm pitch

μPD75116H/117H	μPD75P108B	μPD75P116	μPD75P117H
16K/24K (Mask ROM)	8K (One-time PROM, EPROM)	8K (One-time PROM)	24K (One-time PROM)
768	512		768
75X High-End/expanded High-End	75X High-End		75X expanded High-End ***2**
58			
10			
32 (LED can be driver directly : 8)	32 (LED can be driver directly)		32 (LED can be driver directly : 8)
12	12 (LED can be driver directly)		12
+6 V	+12 V		+6 V
Can be incorporated by mask option	No		
4 (4-bit accuracy)			
No	No		
1.8 to 5.0 V	2.7 to 6.0 V	5 V ±10%	1.8 to 5.0 V
–40 to +60 °C	–40 to +85 °C		–40 to +60 °C
0.95 μs (Operation at 2.7 V) 1.91 μs (Operation at 1.8 V)	0.95 μs (Operation at 4.5 to 6.0 V) 3.8 μs (Operation at 2.7 V)	0.95 μs (Operation at 4.75 to 5.5 V)	0.95 μs (Operation at 2.7 V) 1.91 μs (Operation at 1.8 V)
• 64-pin plastic QFP (GC-AB8) • 64-pin plastic QFP (GK-8A8)	• 64-pin plastic shrink DIP • 64-pin ceramic shrink DIP (with window) • 64-pin plastic QFP (GF-3BE)	• 64-pin plastic shrink DIP • 64-pin plastic QFP (GF-3BE)	• 64-pin plastic QFP (GC-AB8) • 64-pin plastic QFP (GK-8A8) ***1**

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