

MOS INTEGRATED CIRCUIT  
 **$\mu$ PD754202, 754202(A)****4-BIT SINGLE-CHIP MICROCONTROLLERS**

The  $\mu$ PD754202 is a member of the 75XL Series of 4-bit single-chip microcontrollers that enable data processing equivalent to that of an 8-bit microcontroller.

It features expanded CPU functions compared to the 75X Series and enables high-speed, low-voltage operation at 1.8 V, making it suitable for battery-driven applications.

The  $\mu$ PD754202(A) is a higher-reliability product compared to the  $\mu$ PD754202.

**Detailed function descriptions, etc., are provided in the following user's manual. Be sure to read it when designing.**

**$\mu$ PD754202 User's Manual: U11132E**

**FEATURES**

- Key return reset function for keyless entry
- Low-voltage operation:  $V_{DD} = 1.8$  to  $6.0$  V
- On-chip memory
  - Program memory (ROM):  $2048 \times 8$  bits
  - Data memory (RAM) :  $128 \times 4$  bits
- Variable instruction execution time useful for high-speed operation and power save
  - $0.95, 1.91, 3.81, 15.3 \mu s$  (at 4.19-MHz operation)
  - $0.67, 1.33, 2.67, 10.7 \mu s$  (at 6.0-MHz operation)
- Compact package (20-pin plastic shrink SOP (300 mil, 0.65-mm pitch))

**APPLICATIONS**

Automotive electronics such as keyless entry units

The  $\mu$ PD754202 and  $\mu$ PD754202(A) have different quality grades. Unless otherwise specified, descriptions in this data sheet apply to the  $\mu$ PD754202.

The information in this document is subject to change without notice.

**ORDERING INFORMATION**

| Part Number            | Package  | Quality Grade |
|------------------------|--|---------------|
| μPD754202GS-xxx-BA5    | 20-pin plastic SOP (300 mil, 1.27-mm pitch)        | Standard      |
| μPD754202GS-xxx-GJG    | 20-pin plastic shrink SOP (300 mil, 0.65-mm pitch) | Standard      |
| μPD754202GS(A)-xxx-BA5 | 20-pin plastic SOP (300 mil, 1.27-mm pitch)        | Special       |
| μPD754202GS(A)-xxx-GJG | 20-pin plastic shrink SOP (300 mil, 0.65-mm pitch) | Special       |

**Remark** xxx indicates the ROM code suffix.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

**Differences between μPD754202 and μPD754202(A)**

| Part Number   | μPD754202 | μPD754202(A) |
|---------------|-----------|--------------|
| Item          |           |              |
| Quality grade | Standard  | Special      |

FUNCTION LIST

| Parameter                        |                   | Function  |  |
|----------------------------------|-------------------|---|--|
| Instruction execution time       |                   | <ul style="list-style-type: none"> <li>• 0.95, 1.91, 3.81, 15.3 μs (system clock: at 4.19-MHz operation)</li> <li>• 0.67, 1.33, 2.67, 10.7 μs (system clock: at 6.0-MHz operation)</li> </ul> |  |
| On-chip memory                   | ROM               | 2048 × 8 bits   |  |
|                                  | RAM               | 128 × 4 bits  |  |
| General-purpose register         |                   | <ul style="list-style-type: none"> <li>• 4-bit manipulation: 8 × 4 banks</li> <li>• 8-bit manipulation: 4 × 4 banks</li> </ul>  |  |
| I/O port                         | CMOS input        | 4   | Mask option-specifiable on-chip pull-up resistor         |
|                                  | CMOS input/output | 9   | Software-specifiable on-chip pull-up resistor connection |
|                                  | Total             | 13  |  |
| Timer                            |                   | 4 channels <ul style="list-style-type: none"> <li>• 8-bit timer counter: 3 channels<br/>(Usable as 16-bit timer counter)</li> <li>• Basic interval timer/watchdog timer: 1 channel</li> </ul> |  |
| Bit sequential buffer (BSB)      |                   | 16 bits   |  |
| Vectored interrupt               |                   | External: 1, Internal: 4  |  |
| Test input                       |                   | External: 1 (key return reset function provided)  |  |
| System clock oscillation circuit |                   | Ceramic/crystal oscillation circuit   |  |
| Standby function                 |                   | STOP/HALT mode  |  |
| Operating ambient temperature    |                   | T <sub>A</sub> = -40 to +85 °C  |  |
| Supply voltage                   |                   | V <sub>DD</sub> = 1.8 to 6.0 V  |  |
| Package                          |                   | <ul style="list-style-type: none"> <li>• 20-pin plastic SOP (300 mil, 1.27-mm pitch)</li> <li>• 20-pin plastic shrink SOP (300 mil, 0.65-mm pitch)</li> </ul>                                 |  |

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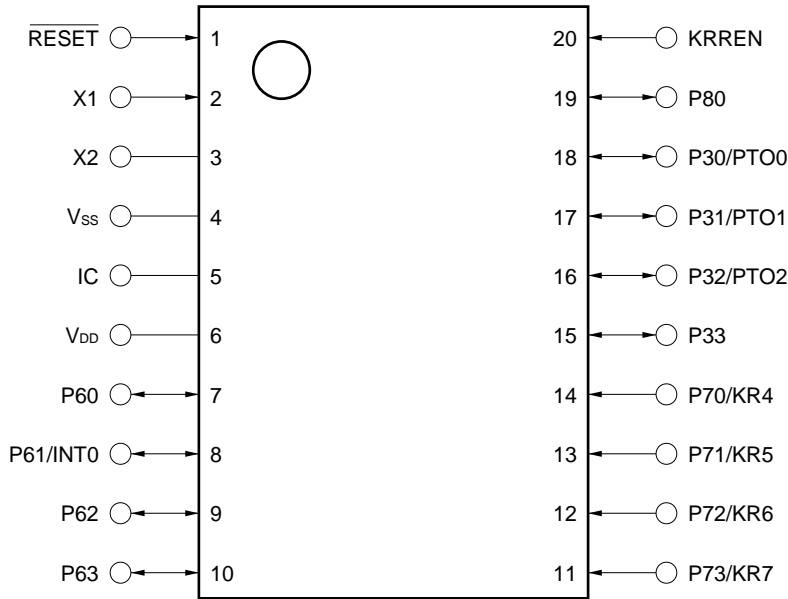
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1. PIN CONFIGURATION (Top View)

- 20-pin plastic SOP (300 mil, 1.27-mm pitch)  
 μPD754202GS-xxx-BA5  
 μPD754202GS(A)-xxx-BA5
- 20-pin plastic shrink SOP (300 mil, 0.65-mm pitch)  
 μPD754202GS-xxx-GJG  
 μPD754202GS(A)-xxx-GJG

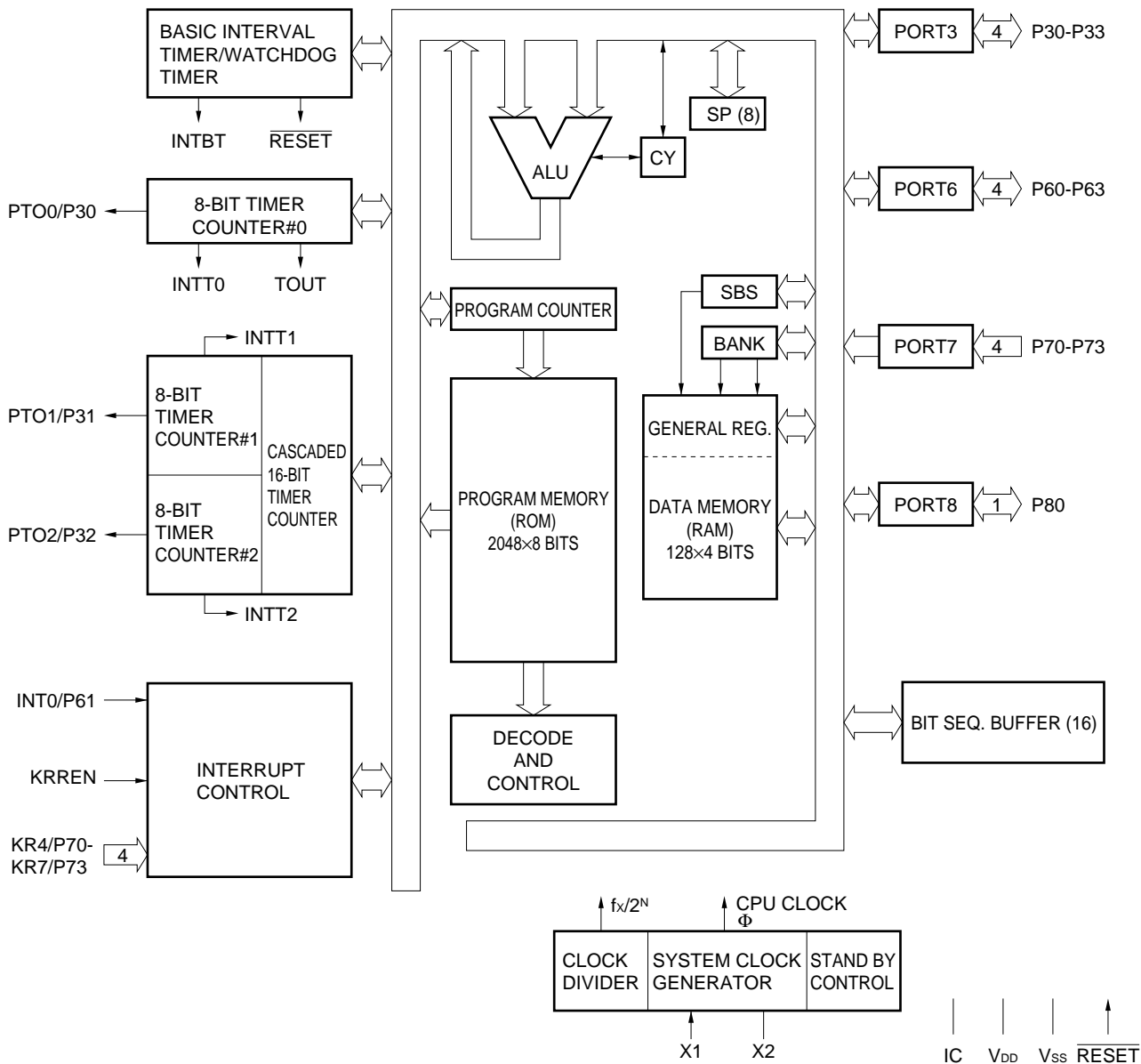


IC: Internally Connected (Connect directly to V<sub>DD</sub>)

Pin Identification

- IC : Internally Connected
- INT0 : External Vectored Interrupt
- KR4 to KR7 : Key Return 4 to 7
- KRREN : Key Return Reset Enable
- P30 to P33 : Port 3
- P60 to P63 : Port 6
- P70 to P73 : Port 7
- P80 : Port 8
- PTO0 to PTO2 : Programmable Timer Output 0 to 2
- RESET : Reset
- V<sub>DD</sub> : Positive Power Supply
- V<sub>SS</sub> : Ground
- X1, X2 : System Clock (Ceramic/Crystal)

2. BLOCK DIAGRAM



3. PIN FUNCTION

3.1 Port Pins

| Pin Name | Input/Output | Alternate Function | Function   | 8-bit I/O | After Reset | I/O Circuit Type <sup>Note</sup> |
|----------|--------------|--------------------|--|-----------|-------------|----------------------------------|
| P30      | Input/Output | PTO0               | Programmable 4-bit input/output port (PORT3).<br>This port can be specified input/output bit-wise.<br>On-chip pull-up resistor can be specified by software in 4-bit units.  | -         | Input       | E-B                              |
| P31      |              | PTO1               |  |           |             |                                  |
| P32      |              | PTO2               |  |           |             |                                  |
| P33      |              | -                  |  |           |             |                                  |
| P60      | Input/Output | -                  | Programmable 4-bit input/output port (PORT6).<br>This port can be specified input/output bit-wise.<br>On-chip pull-up resistor can be specified by software in 4-bit units.<br>Noise eliminator can be selected on P61/INT0. | -         | Input       | ⓕ-A                              |
| P61      |              | INT0               |  |           |             |                                  |
| P62      |              | -                  |  |           |             |                                  |
| P63      |              | -                  |  |           |             |                                  |
| P70      | Input        | KR4                | 4-bit input port (PORT7).<br>On-chip pull-up resistor can be specified bit-wise (mask option).   | -         | Input       | Ⓑ-A                              |
| P71      |              | KR5                |  |           |             |                                  |
| P72      |              | KR6                |  |           |             |                                  |
| P73      |              | KR7                |  |           |             |                                  |
| P80      | Input/Output | -                  | 1-bit input/output port (PORT8).<br>On-chip pull-up resistor can be specified by software.   | -         | Input       | ⓕ-A                              |

**Note** Circled characters indicate Schmitt trigger input.



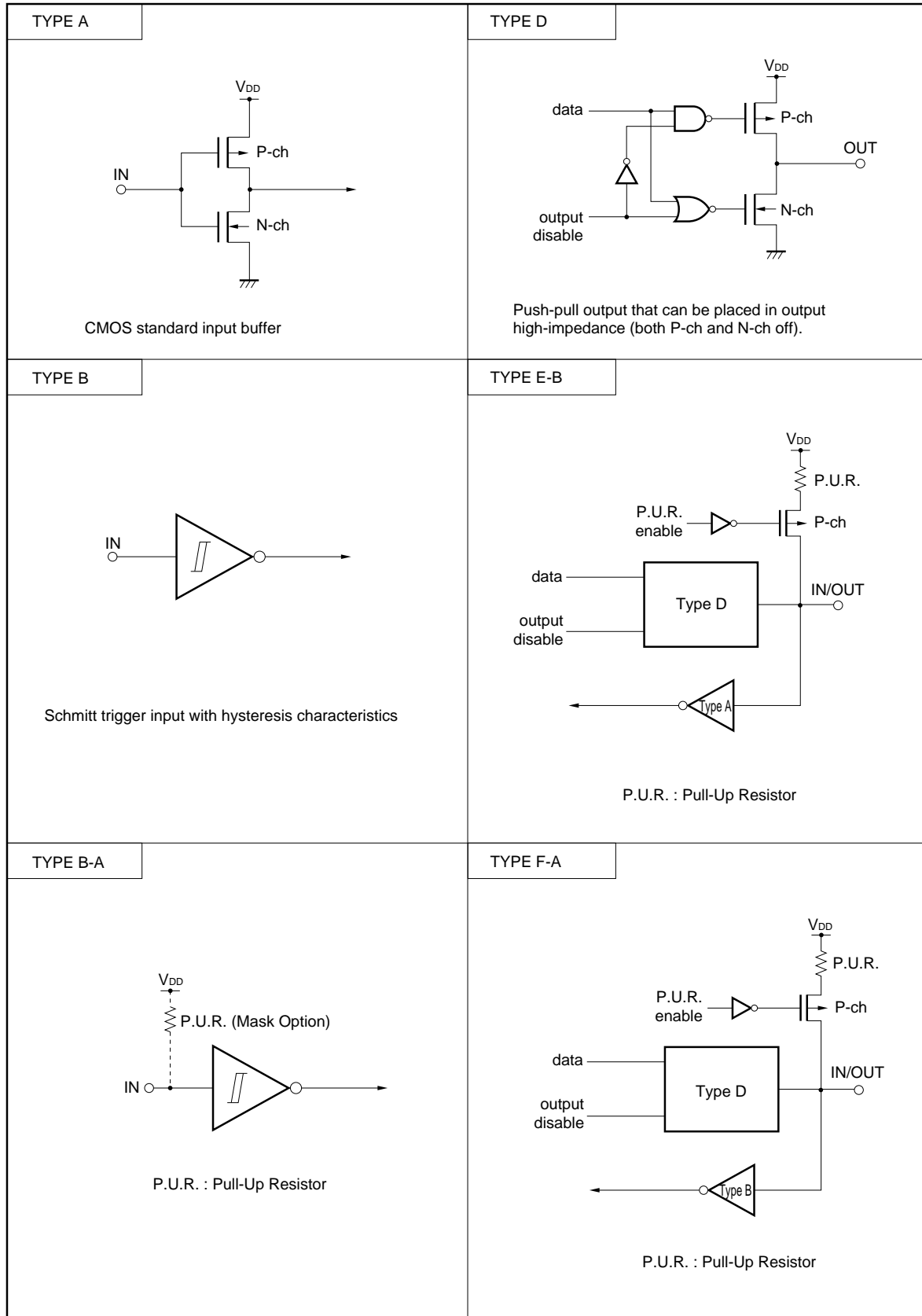
3.2 Non-port Pins

| Pin Name        | Input/Output | Alternate Function | Function   |  | After Reset | I/O Circuit Type <sup>Note</sup> |
|-----------------|--------------|--------------------|--|--|-------------|----------------------------------|
| PTO0            | Output       | P30                | Timer counter output   |  | Input       | E-B                              |
| PTO1            |              | P31                |  |  |             |                                  |
| PTO2            |              | P32                |  |  |             |                                  |
| INT0            | Input        | P61                | Edge detection vectored interrupt input (detected edge is selectable)<br>Noise eliminator selectable                         | Noise eliminator/asynchronous selectable | Input       | Ⓕ-A                              |
| KR4 to KR7      | Input        | P70 to P73         | Falling edge detection testable input  |  | Input       | Ⓑ-A                              |
| KRREN           | Input        | –                  | Key return reset enable.<br>When KRREN = high level in STOP mode, reset signal is generated at falling edge of KRn.          |  | Input       | Ⓑ                                |
| X1              | Input        | –                  | System clock oscillation crystal/ceramic connection pin.<br>If using an external clock, input to X1 and reverse input to X2. |  | –           | –                                |
| X2              | –            |                    |  |  |             |                                  |
| RESET           | Input        | –                  | System reset input (low-level active).<br>Pull-up resistor can be incorporated on-chip (mask option).                        |  | –           | Ⓑ-A                              |
| IC              | –            | –                  | Internally connected. Connect directly to V <sub>DD</sub> .  |  | –           | –                                |
| V <sub>DD</sub> | –            | –                  | Positive power supply  |  | –           | –                                |
| V <sub>SS</sub> | –            | –                  | Ground potential   |  | –           | –                                |

**Note** Circled characters indicate Schmitt trigger input.

### 3.3 Pin Input/Output Circuits

The μPD754202 pin input/output circuits are shown schematically.



3.4 Recommended Connection of Unused Pins

Table 3-1. List of Recommended Connection of Unused Pins

| Pin      | Recommended Connecting Method   |
|----------|---|
| P30/PTO0 | Input state : Independently connect to $V_{SS}$ or $V_{DD}$ via a resistor.<br>Output state: Leave open.  |
| P31/PTO1 |   |
| P32/PTO2 |   |
| P33      |   |
| P60      |   |
| P61/INT0 |   |
| P62      |   |
| P63      |   |
| P70/KR4  |   |
| P71/KR5  |   |
| P72/KR6  |   |
| P73/KR7  |   |
| P80      | Input state : Independently connect to $V_{SS}$ or $V_{DD}$ via a resistor.<br>Output state: Leave open.  |
| KRREN    | When this pin is connected to $V_{DD}$ , internal reset signal is generated at the falling edge of the $KR_n$ pin in the STOP mode.<br>When this pin is connected to $V_{SS}$ , internal reset signal is not generated even if the falling edge of $KR_n$ pin is detected in the STOP mode. |
| IC       | Connect directly to $V_{DD}$ .  |

#### 4. SWITCHING FUNCTION BETWEEN Mk I MODE AND Mk II MODE

##### 4.1 Differences between Mk I Mode and Mk II Mode

The μPD754202 75XL CPU has the following two modes: Mk I and Mk II, either of which can be selected. The mode can be switched by bit 3 of the stack bank select register (SBS).

- Mk I mode : Instructions are compatible with the 75X Series. Can be used in the 75XL CPU with a ROM capacity of up to 16 Kbytes.
- Mk II mode: Incompatible with 75X Series. Can be used in all the 75XL CPU's including those products whose ROM capacity is more than 16 Kbytes.

**Table 4-1. Differences between Mk I Mode and Mk II Mode**

|  | Mk I mode        | Mk II mode       |
|--|------------------|------------------|
| Number of stack bytes for subroutine instructions  | 2 bytes          | 3 bytes          |
| BRA !addr1 instruction<br>CALLA !addr1 instruction | Not available    | Available        |
| CALL !addr instruction                             | 3 machine cycles | 4 machine cycles |
| CALLF !faddr instruction                           | 2 machine cycles | 3 machine cycles |

**Caution** The Mk II mode supports a program area exceeding 16 Kbytes for the 75X and 75XL Series. Therefore, this mode is effective for enhancing software compatibility with products that have a program area of more than 16 Kbytes.

The number of stack bytes (usable area) during execution of subroutine call instructions increases by 1 byte per stack compared to the Mk I mode when the Mk II mode is selected.

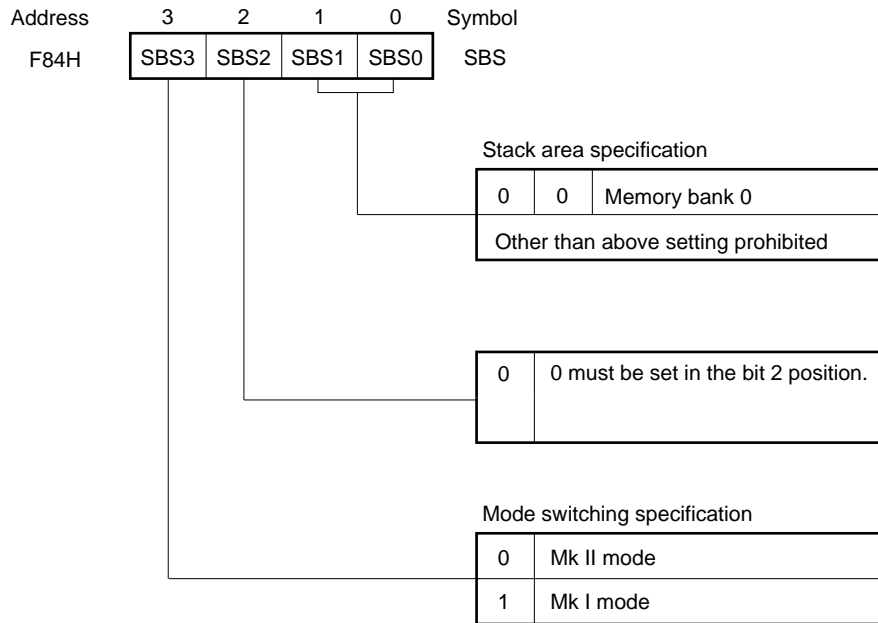
However, when the CALL !addr and CALL !faddr instructions are used, the machine cycle becomes longer by 1 machine cycle. Therefore, if more emphasis is placed on RAM use efficiency and processing performance than on software compatibility, the Mk I mode should be used.

### 4.2 Setting Method of Stack Bank Select Register (SBS)

Switching between the Mk I mode and Mk II mode can be done by the SBS. Figure 4-1 shows the format. The SBS is set by a 4-bit memory manipulation instruction.

When using the Mk I mode, the SBS must be initialized to 1000B at the beginning of a program. When using the Mk II mode, it must be initialized to 0000B.

**Figure 4-1. Stack Bank Select Register Format**



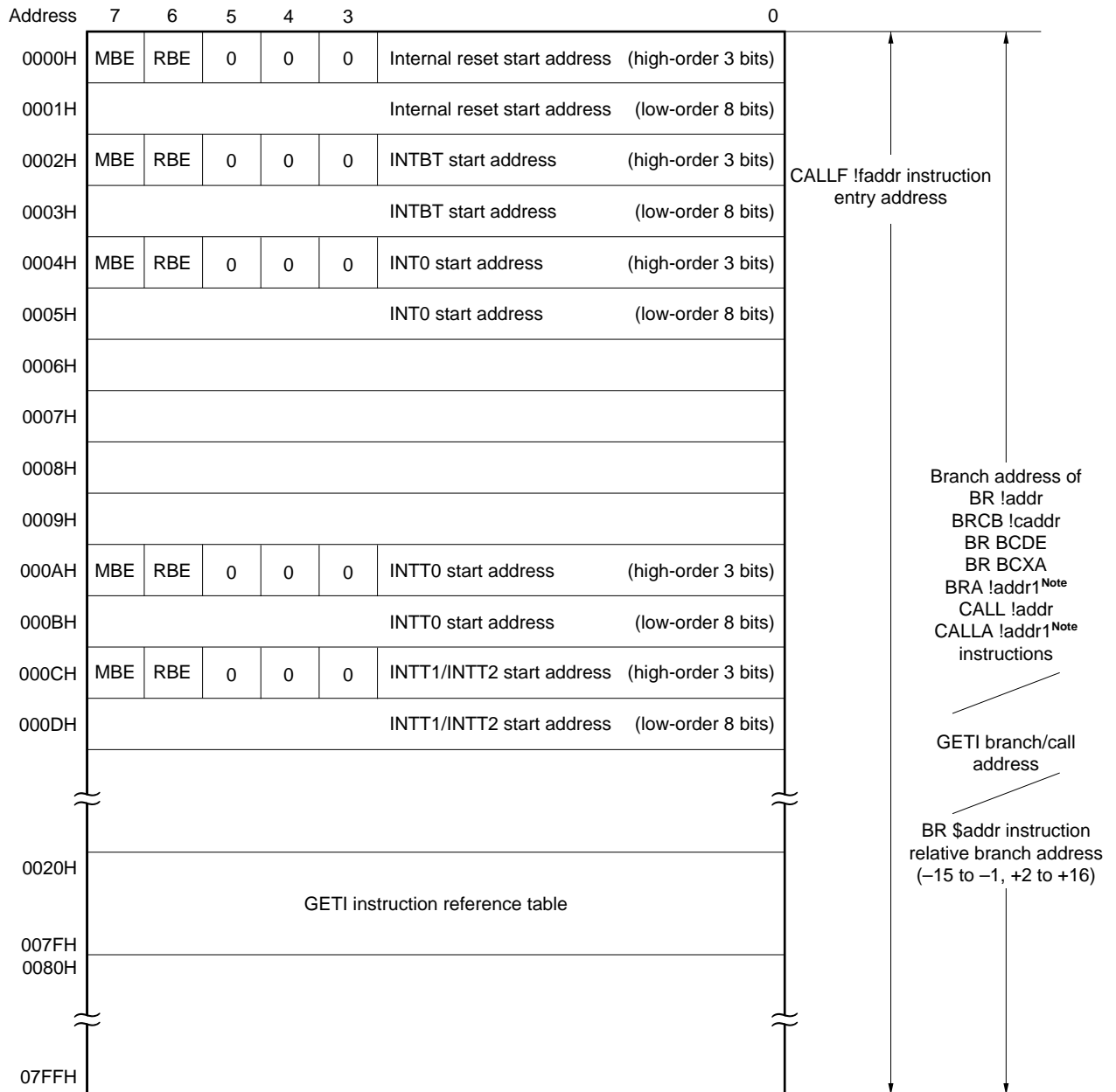
**Caution** Because SBS.3 is set to “1” after a RESET signal is generated, the CPU operates in the Mk I mode. When executing an instruction in the Mk II mode, set SBS.3 to “0” to select the Mk II mode.

## 5. MEMORY CONFIGURATION

- Program Memory (ROM): 2048  $\times$  8 bits (0000H-07FFH)
  - Addresses 0000H and 0001H  
Vector table wherein the program start address and the values set for the RBE and MBE at the time a  $\overline{\text{RESET}}$  signal is generated are written. Reset start is possible from any address.
  - Addresses 0002H to 000DH  
Vector table wherein the program start address and values set for the RBE and MBE by the vectored interrupts are written. Interrupt service can start from any address.
  - Addresses 0020H to 007FH  
Table area referenced by the GETI instruction<sup>Note</sup>.

**Note** The GETI instruction realizes a 1-byte instruction on behalf of any 2-byte instruction, 3-byte instruction, or two 1-byte instructions. It is used to decrease the number of program steps.
- Data Memory (RAM)
  - Data area: 128 words  $\times$  4 bits (000H-07FH)
  - Peripheral hardware area: 128 words  $\times$  4 bits (F80H-FFFH)

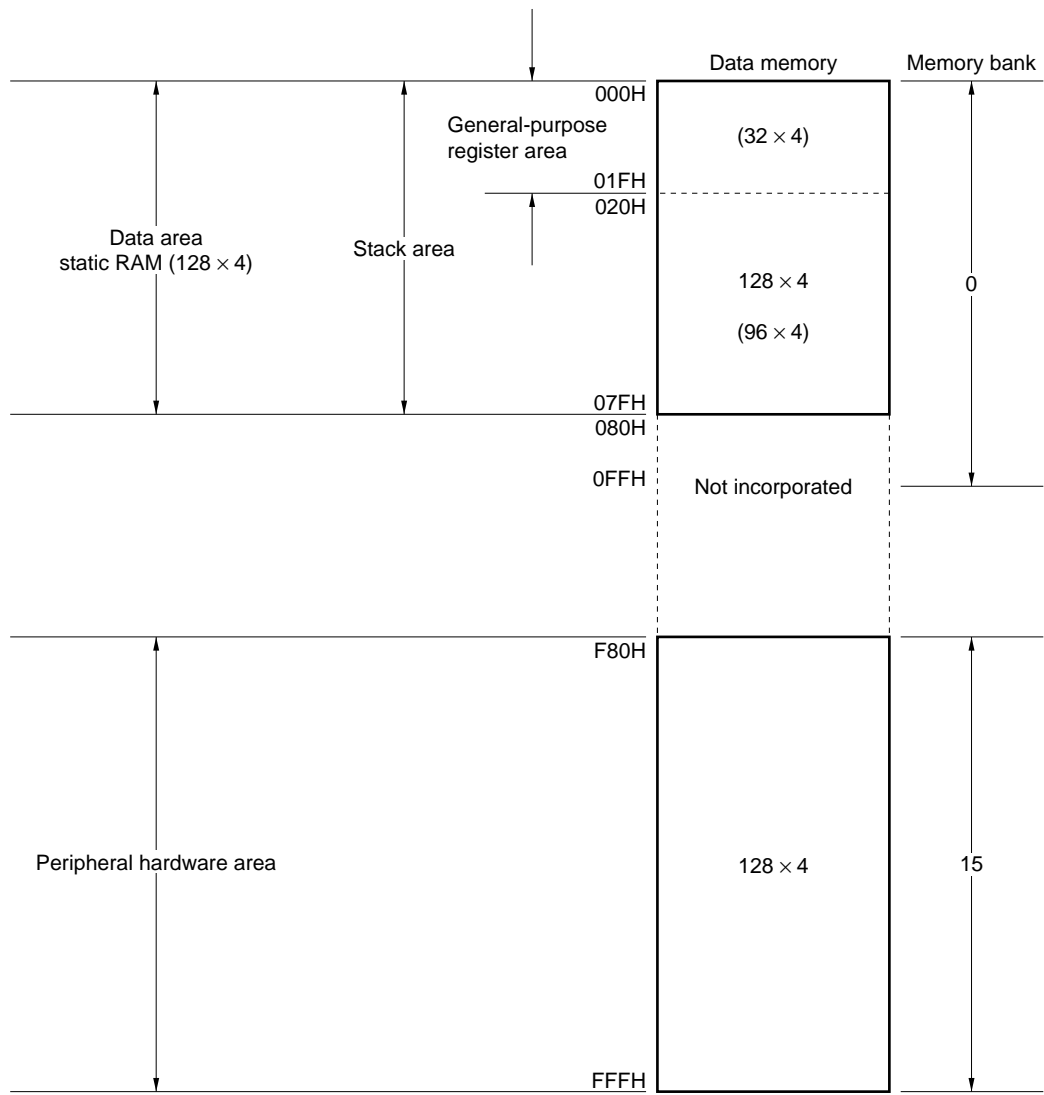
Figure 5-1. Program Memory Map



**Note** Can be used in Mk II mode only.

**Remark** In addition to the above, a branch can be made to an address with only the low-order 8 bits of the PC changed by means of a BR PCDE or BR PCXA instruction.

Figure 5-2. Data Memory Map





## 6. PERIPHERAL HARDWARE FUNCTION

### 6.1 Digital I/O Port

The following two types of I/O ports are provided.

|                                   |     |
|-----------------------------------|-----|
| • CMOS Input (PORT7)              | : 4 |
| • CMOS Input/Output (PORT3, 6, 8) | : 9 |
| Total                             | 13  |

**Table 6-1. Types and Features of Digital Ports**

| Port Name | Function    | Operation and Features  | Remarks                          |
|-----------|-------------|---|----------------------------------|
| PORT3     | 4-bit I/O   | Can be set to input or output mode bit-wise.  | Also used for PTO0 to PTO2 pins. |
| PORT6     |             |   | Also used for INT0 pin.          |
| PORT7     | 4-bit input | 4-bit input only port<br>On-chip pull-up resistor can be specified by mask option bit-wise. | Also used for KR4 to KR7 pins.   |
| PORT8     | 1-bit I/O   | Can be set to input or output mode bit-wise.  | –                                |

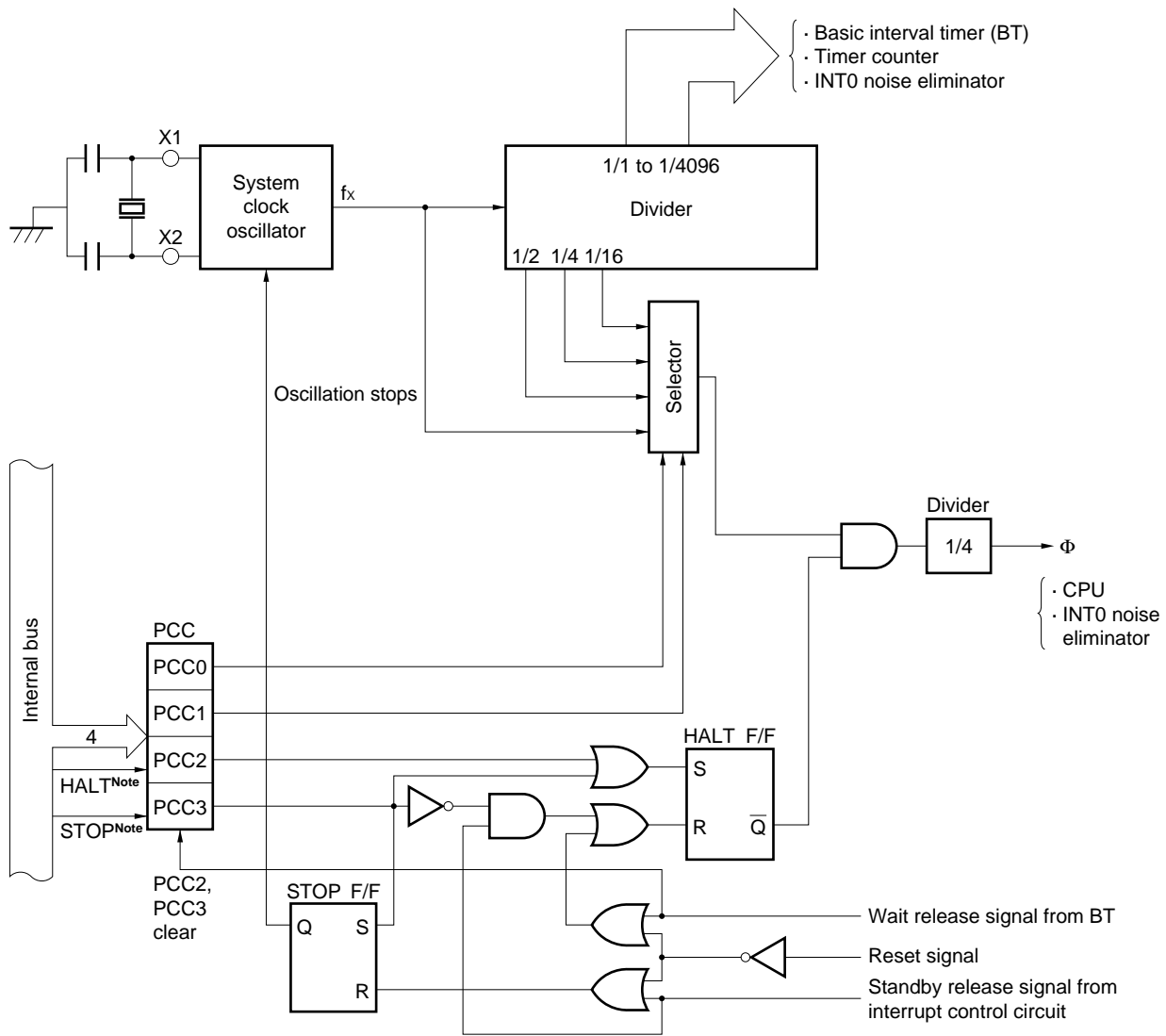
### 6.2 Clock Generator

The clock generator provides the clock signals to the CPU and peripheral hardware. Its configuration is shown in Figure 6-1.

The operation of the clock generator is set with the processor clock control register (PCC). The instruction execution time can be changed as follows.

- 0.95, 1.91, 3.81, 15.3 μs (system clock operating at 4.19 MHz)
- 0.67, 1.33, 2.67, 10.7 μs (system clock operating at 6.0 MHz)

Figure 6-1. Clock Generator Block Diagram



**Note** Instruction execution

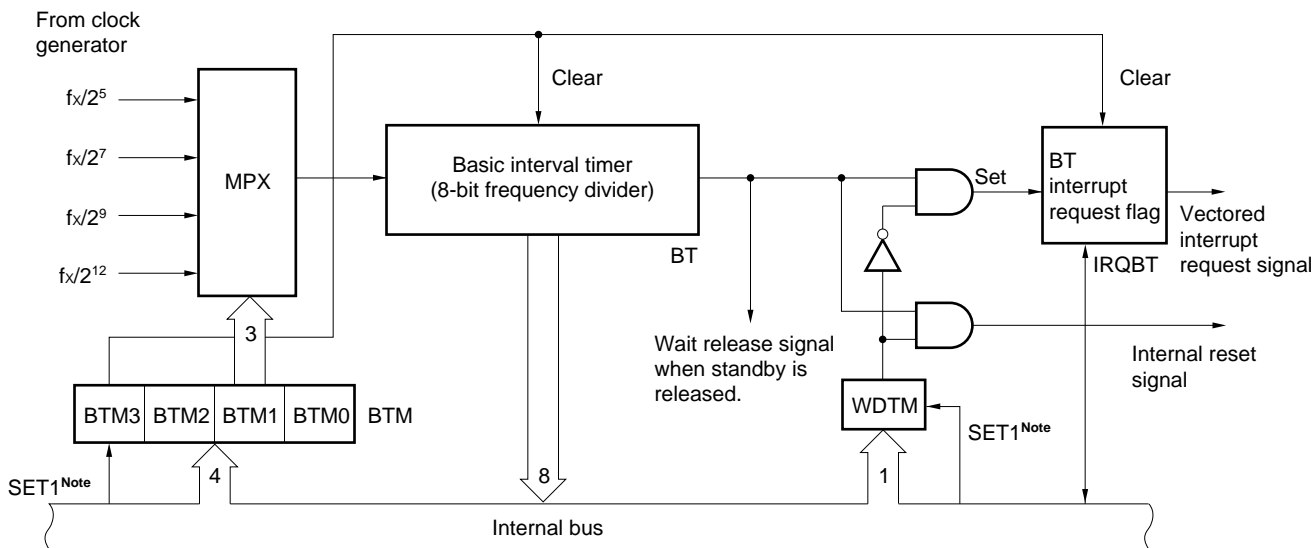
- Remarks**
1.  $f_x$ : System clock frequency
  2.  $\Phi$  = CPU clock
  3. PCC: Processor Clock Control Register
  4. One clock cycle ( $t_{cy}$ ) of the CPU clock is equal to one machine cycle of the instruction.

### 6.3 Basic Interval Timer/Watchdog Timer

The basic interval timer/watchdog timer has the following functions.

- (a) Interval timer operation to generate a reference time interrupt
- (b) Watchdog timer operation to detect a runaway of program and reset the CPU
- (c) Selects and counts the wait time when the standby mode is released
- (d) Reads the contents of counting

Figure 6-2. Basic Interval Timer/Watchdog Timer Block Diagram



**Note** Instruction execution

### 6.4 Timer Counter

The μPD754202 incorporates three timer counters. Its configuration is shown in Figures 6-3, 6-4, and 6-5. The timer counter functions are shown below.

- (a) Programmable interval timer operation
- (b) Square wave output of any frequency to PTO0-PTO2 pins
- (c) Count value read function

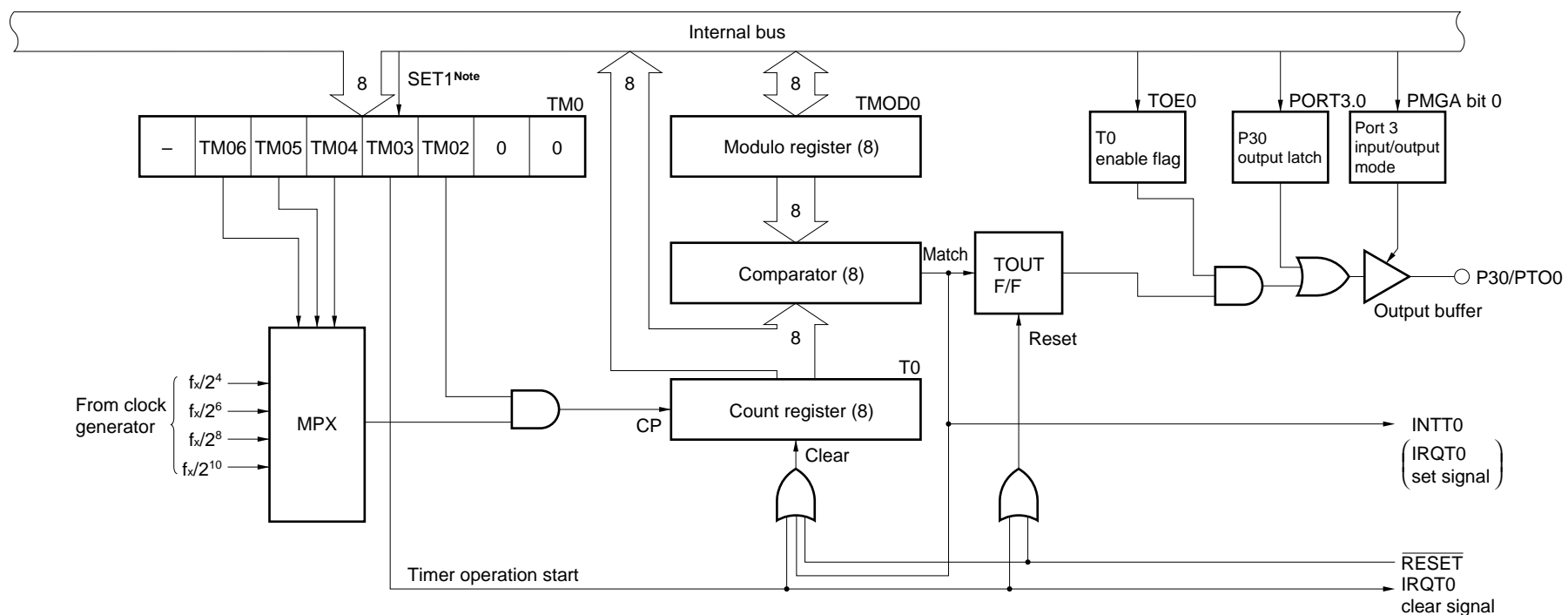
The timer counter can operate in the following four modes as set by the mode register.

**Table 6-2. Mode List**

| Mode \ Channel            | Channel 0 | Channel 1 | Channel 2 | TM11 | TM10 | TM21 | TM20 |
|---------------------------|-----------|-----------|-----------|------|------|------|------|
| 8-bit timer counter mode  | ○         | ○         | ○         | 0    | 0    | 0    | 0    |
| PWM pulse generator mode  | ×         | ×         | ○         | 0    | 0    | 0    | 1    |
| 16-bit timer counter mode | ×         | ○         |           | 1    | 0    | 1    | 0    |
| Carrier generator mode    | ×         | ○         |           | 0    | 0    | 1    | 1    |

**Remark** ○: Available  
 ×: Not available

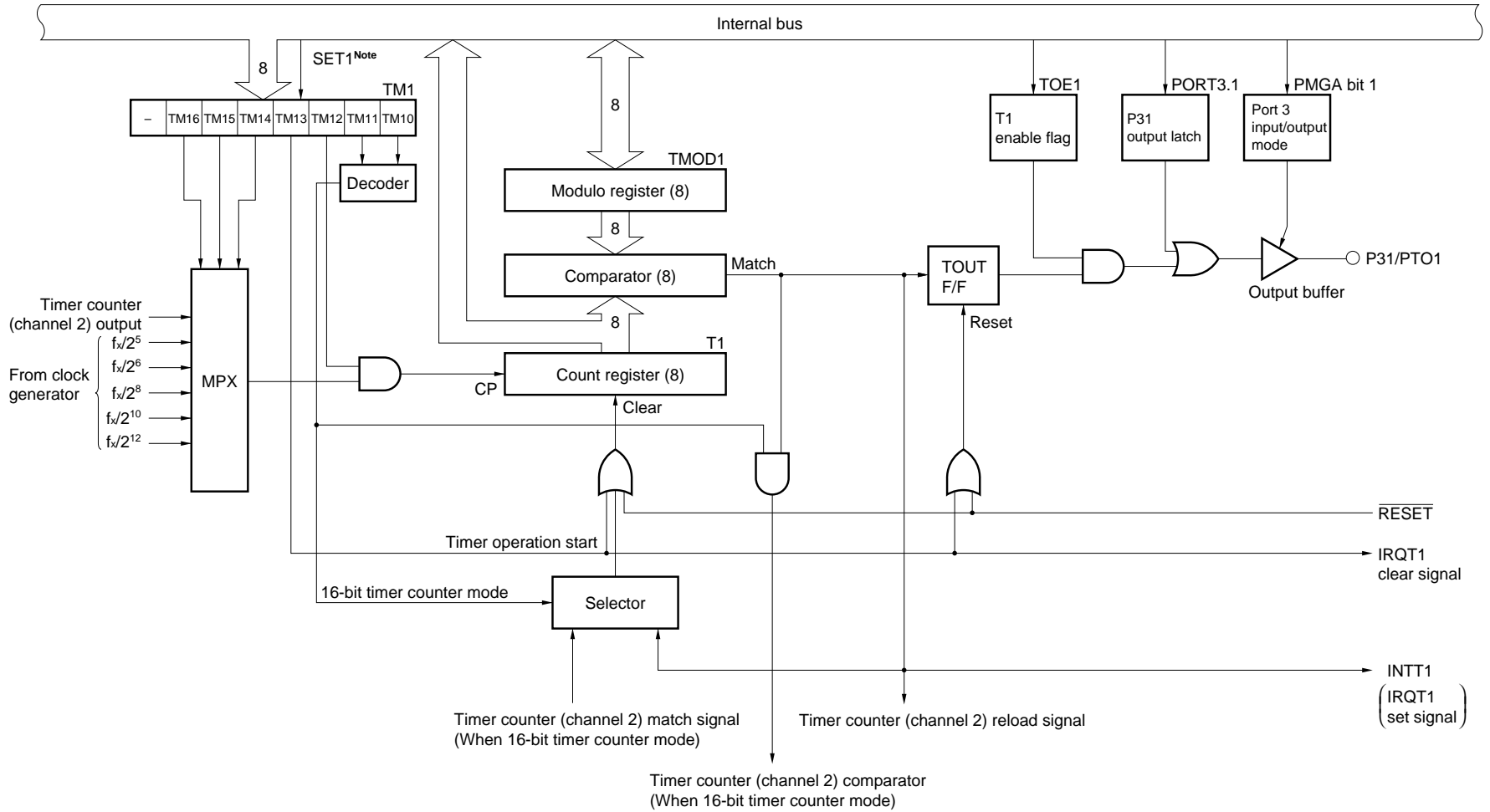
Figure 6-3. Timer Counter (Channel 0) Block Diagram



**Note** Instruction execution

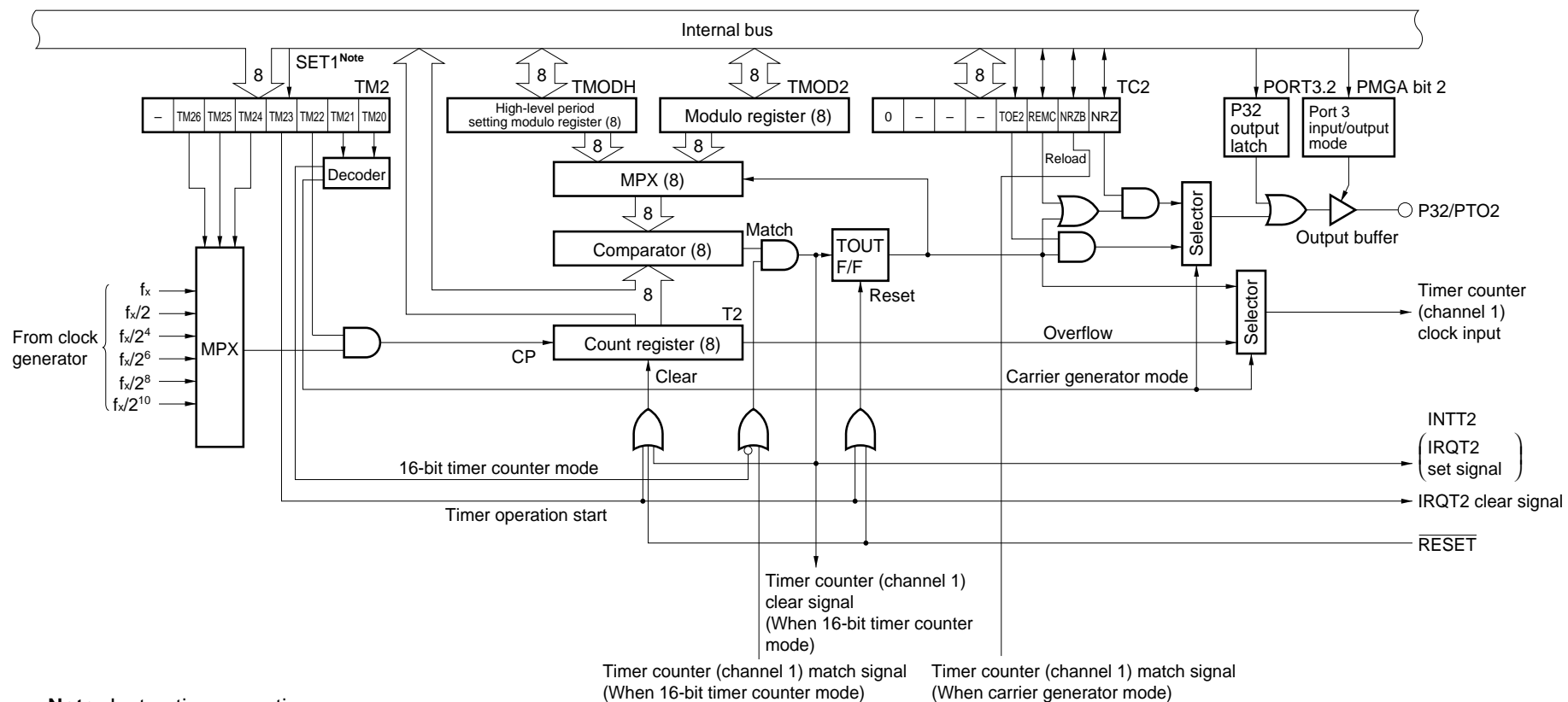
**Caution** Always set bits 0 and 1 to 0 when setting data to TM0.

Figure 6-4. Timer Counter (Channel 1) Block Diagram



**Note** Instruction execution

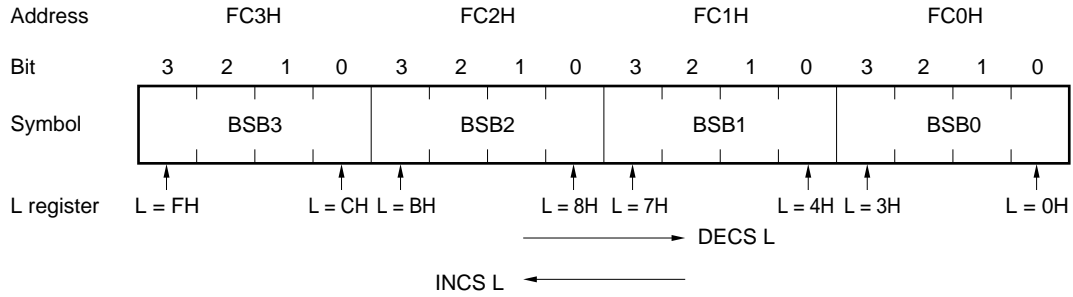
Figure 6-5. Timer Counter (Channel 2) Block Diagram



### 6.5 Bit Sequential Buffer ..... 16 Bits

The bit sequential buffer (BSB) is a special data memory for bit manipulation and the bit manipulation can be easily performed by changing the address specification and bit specification in sequence, therefore it is useful when processing large data bit-wise.

**Figure 6-6. Bit Sequential Buffer Format**



- Remarks 1.** In the pmem.@L addressing, the specified bit moves corresponding to the L register.  
**2.** In the pmem.@L addressing, the BSB can be manipulated regardless of MBE/MBS specification.



## 7. INTERRUPT FUNCTION AND TEST FUNCTION

The  $\mu$ PD754202 is provided with five types of interrupt sources and one test source to enable a variety of applications.

The interrupt control circuit of the  $\mu$ PD754202 has the following functions.

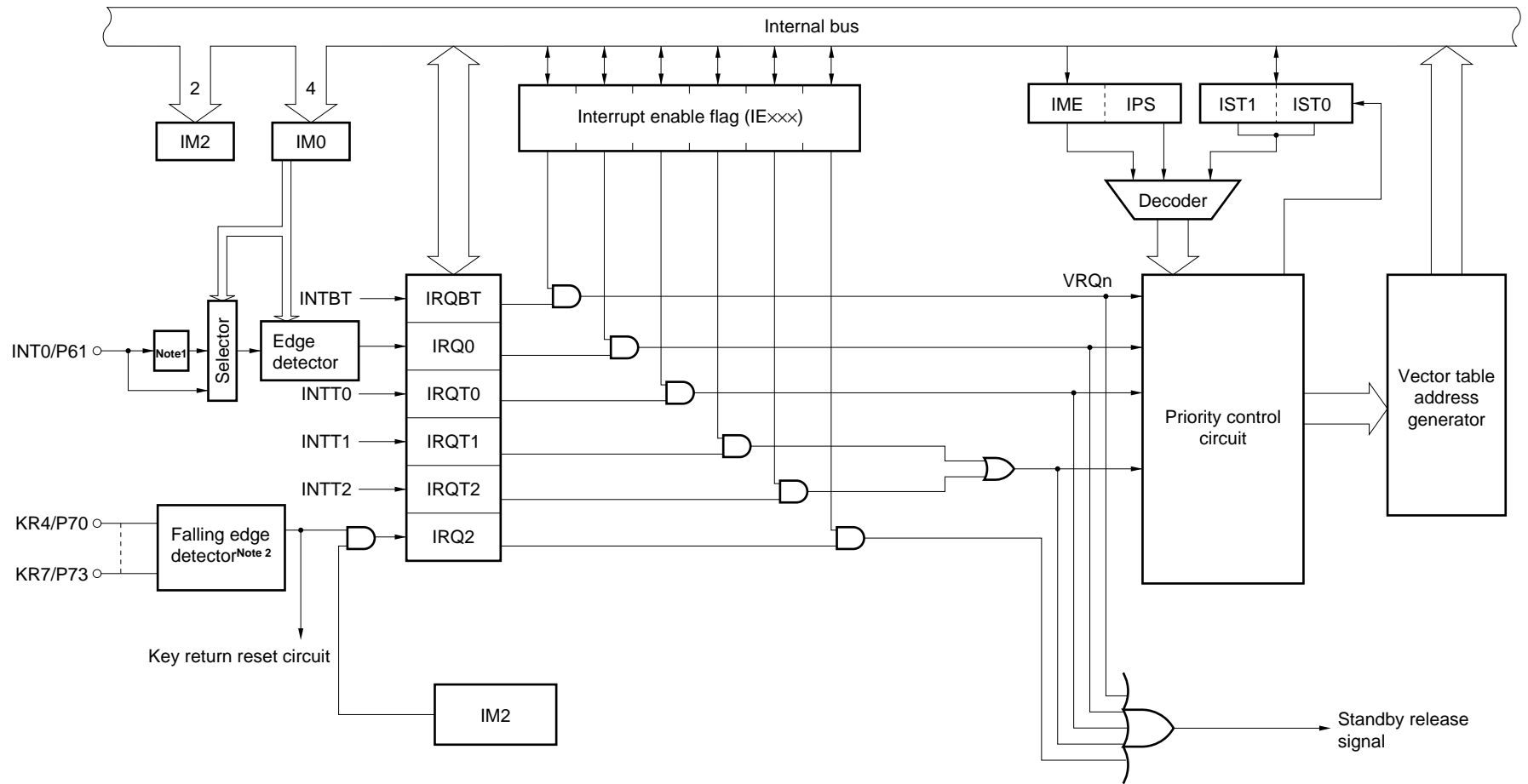
### (1) Interrupt function

- Vectored interrupt function for hardware control, enabling/disabling the interrupt acknowledgement by the interrupt enable flag (IE $\times\times\times$ ) and interrupt master enable flag (IME).
- Can set any interrupt start address.
- Multiple interrupts wherein the order of priority can be specified by the interrupt priority select register (IPS).
- Test function of interrupt request flag (IRQ $\times\times\times$ ). An interrupt generated can be checked by software.
- Release the standby mode. The interrupt to be released can be selected by the interrupt enable flag.

### (2) Test function

- Test request flag (IRQ2) generation can be checked by software.
- Release the standby mode. The test source to be released can be selected by the test enable flag.

Figure 7-1. Interrupt Control Circuit Block Diagram



**Notes 1.** Noise eliminator (Standby release is disabled when noise eliminator is selected.)

**2.** The INT2 pin is not available. Interrupt request flag (IRQ2) is set at the KRn pin falling edge when IM20 = 1 and IM21 = 0.

8. STANDBY FUNCTION

In order to reduce power dissipation while a program is in standby mode, two types of standby modes (STOP mode and HALT mode) are provided for the μPD754202.

Table 8-1. Operation Status in Standby Mode

| Item             |   | Mode | STOP mode   | HALT mode   |
|------------------|---|------|---|---|
| Set instruction  |   |      | STOP instruction  | HALT instruction  |
| Operation status | Clock generator                         |      | Operation stops.  | Only the CPU clock $\Phi$ halts (oscillation continues).  |
|                  | Basic interval timer/<br>watchdog timer |      | Operation stops.  | Operable<br>(BT mode : The IRQBT is set in the reference time interval.<br>WT mode: Reset signal generation by BT overflow.)              |
|                  | Timer counter                           |      | Operation stops.  | Operable.   |
|                  | External interrupt                      |      | The INT0 is not operable <sup>Note</sup> .<br>The INT2 is operable at the falling edge of KRn.  |   |
|                  | CPU                                     |      | Operation stops.  |   |
| Release signal   |   |      | <ul style="list-style-type: none"> <li>• Reset signal</li> <li>• Interrupt request signal sent from interrupt enabled hardware</li> <li>• System reset signal (key return reset) generated by KRn falling edge when KRREN pin = 1.</li> </ul> | <ul style="list-style-type: none"> <li>• Reset signal</li> <li>• Interrupt request signal sent from interrupt enabled hardware</li> </ul> |

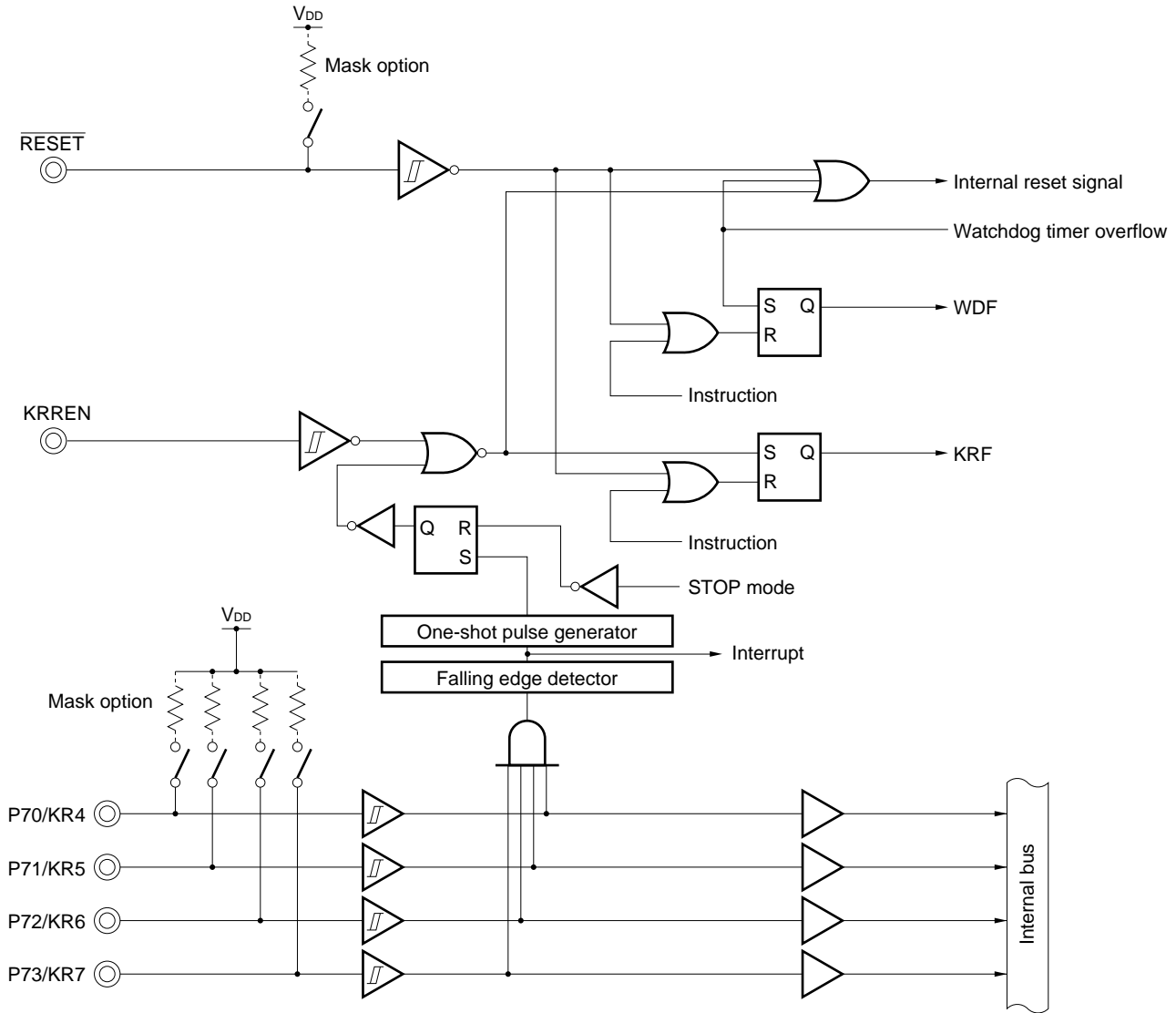
**Note** Can operate only when the noise eliminator is not used (IM02 = 1) by bit 2 of the edge detection mode register (IM0).

## 9. RESET FUNCTION

### 9.1 Configuration and Operation Status of Reset Function

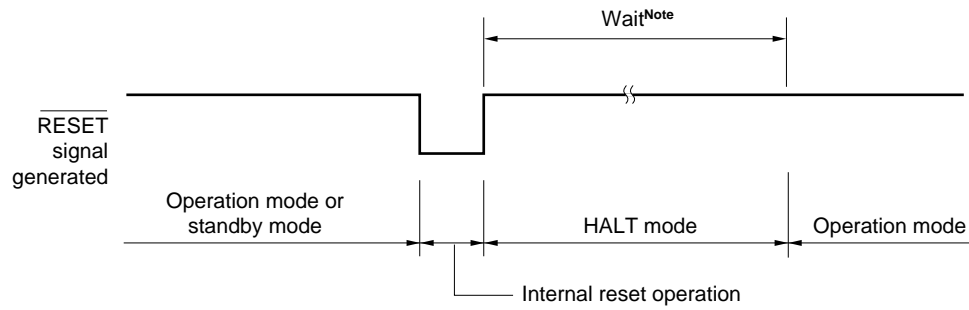
There are three kinds of reset input: the external reset signal ( $\overline{\text{RESET}}$ ), the reset signal sent from the basic interval/watchdog timer, and the reset signal generated by a falling edge signal from KRn in the STOP mode. When any of these reset signals is input, an internal reset signal is generated. The configuration is shown in Figure 9-1.

Figure 9-1. Configuration of Reset Function



The  $\overline{\text{RESET}}$  signal generation initializes each hardware as listed in Table 9-1. Figure 9-2 shows the timing chart of the reset operation.

**Figure 9-2. Reset Operation by  $\overline{\text{RESET}}$  Signal Generation**



**Note** The following 2 time modes can be specified with mask option.  
 $2^{17}/f_x$  (21.8 ms: at 6.0-MHz operation, 31.3 ms: at 4.19-MHz operation)  
 $2^{15}/f_x$  (5.46 ms: at 6.0-MHz operation, 7.81 ms: at 4.19-MHz operation)

Table 9-1. Hardware Status After Reset (1/3)

| Hardware  |  | $\overline{\text{RESET}}$ signal generation in the standby mode   | $\overline{\text{RESET}}$ signal generation in operation  |
|---|--|---|---|
| Program counter (PC)                              |  | Sets the low-order 3 bits of program memory's address 0000H to the PC10-PC8 and the contents of address 0001H to the PC7-PC0. | Sets the low-order 3 bits of program memory's address 0000H to the PC10-PC8 and the contents of address 0001H to the PC7-PC0. |
| PSW   | Carry flag (CY)                                    | Held  | Undefined   |
|   | Skip flag (SK0-SK2)                                | 0   | 0   |
|   | Interrupt status flag (IST0, IST1)                 | 0   | 0   |
|   | Bank enable flag (MBE, RBE)                        | Sets the bit 6 of program memory's address 0000H to the RBE and bit 7 to the MBE.   | Sets the bit 6 of program memory's address 0000H to the RBE and bit 7 to the MBE.   |
| Stack pointer (SP)                                |  | Undefined   | Undefined   |
| Stack bank select register (SBS)                  |  | 1000B   | 1000B   |
| Data memory (RAM)                                 |  | Held  | Undefined   |
| General-purpose register (X, A, H, L, D, E, B, C) |  | Held  | Undefined   |
| Bank select register (MBS, RBS)                   |  | 0, 0  | 0, 0  |
| Basic interval                                    | Counter (BT)                                       | Undefined   | Undefined   |
| timer/watchdog                                    | Mode register (BTM)                                | 0   | 0   |
| timer   | Watchdog timer enable flag (WDTM)                  | 0   | 0   |
| Timer counter (T0)                                | Counter (T0)                                       | 0   | 0   |
|   | Modulo register (TMOD0)                            | FFH   | FFH   |
|   | Mode register (TM0)                                | 0   | 0   |
|   | TOE0, TOUT F/F                                     | 0, 0  | 0, 0  |
| Timer counter (T1)                                | Counter (T1)                                       | 0   | 0   |
|   | Modulo register (TMOD1)                            | FFH   | FFH   |
|   | Mode register (TM1)                                | 0   | 0   |
|   | TOE1, TOUT F/F                                     | 0, 0  | 0, 0  |
| Timer counter (T2)                                | Counter (T2)                                       | 0   | 0   |
|   | Modulo register (TMOD2)                            | FFH   | FFH   |
|   | High-level period setting modulo register (TMOD2H) | FFH   | FFH   |
|   | Mode register (TM2)                                | 0   | 0   |
|   | TOE2, TOUT F/F                                     | 0, 0  | 0, 0  |
|   | REMC, NRZ, NRZB                                    | 0, 0, 0   | 0, 0, 0   |

**Table 9-1. Hardware Status After Reset (2/3)**

| Hardware                          |  | $\overline{\text{RESET}}$ signal generation in the standby mode | $\overline{\text{RESET}}$ signal generation in operation |
|-----------------------------------|--|---|--|
| Clock generator                   | Processor clock control register (PCC)         | 0   | 0  |
| Interrupt function                | Interrupt request flag (IRQ <sub>xxx</sub> )   | Reset (0)   | Reset (0)  |
|                                   | Interrupt enable flag (IE <sub>xxx</sub> )     | 0   | 0  |
|                                   | Interrupt master enable flag (IME)             | 0   | 0  |
|                                   | Interrupt priority selection register (IPS)    | 0   | 0  |
|                                   | INT0, 2 mode registers (IM0, IM2)              | 0, 0  | 0, 0   |
| Digital port                      | Output buffer                                  | Off   | Off  |
|                                   | Output latch                                   | Cleared (0)   | Cleared (0)  |
|                                   | I/O mode registers (PMGA, PMGC)                | 0   | 0  |
|                                   | Pull-up resistor setting register (POGA, POGB) | 0   | 0  |
| Bit sequential buffer (BSB0-BSB3) |  | Held  | Undefined  |

**Table 9-1. Hardware Status After Reset (3/3)**

| Hardware              | $\overline{\text{RESET}}$ signal generation by key return reset | $\overline{\text{RESET}}$ signal generation in the standby mode | $\overline{\text{RESET}}$ signal generation by WDT during operation | $\overline{\text{RESET}}$ signal generation during operation |
|-----------------------|---|---|---|--|
| Watchdog flag (WDF)   | Hold the previous status  | 0   | 1   | 0  |
| Key return flag (KRF) | 1   | 0   | Hold the previous status  | 0  |

### 9.2 Watchdog Flag (WDF), Key Return Flag (KRF)

The WDF is set by a watchdog timer overflow signal, and the KRF is set by a reset signal generated by the KRn pins. As a result, by checking the contents of WDF and KRF, it is possible to know what kind of reset signal is generated.

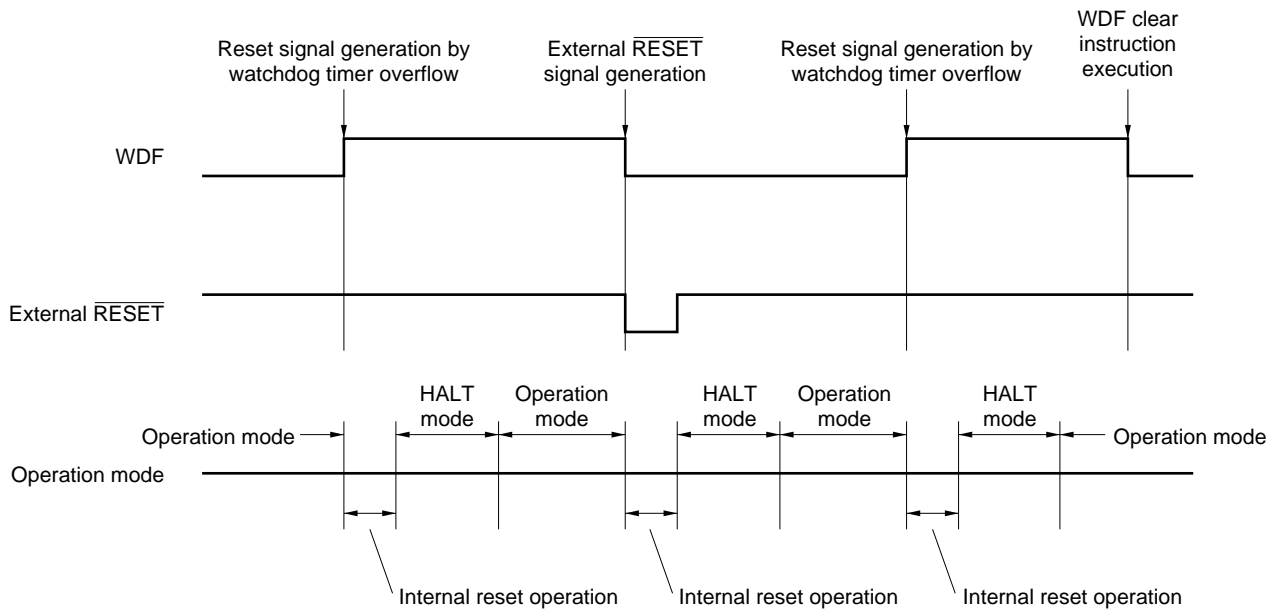
As the WDF and KRF are cleared only by external signal or instruction execution, if once these flags are set, they are not cleared until an external signal is generated or a clear instruction is executed. Check and clear the contents of WDF and KRF after reset start operation by executing SKTCLR instruction and so on.

Table 9-2 lists the contents of WDF and KRF corresponding to each signal. Figure 9-3 shows the WDF operation in generating each signal, and Figure 9-4 shows the KRF operation in generating each signal.

**Table 9-2. WDF and KRF Contents Correspond to Each Signal**

| Hardware              | External $\overline{\text{RESET}}$ signal generation | Reset signal generation by watchdog timer overflow | Reset signal generation by the KRn input | WDF clear instruction execution | KRF clear instruction execution |
|-----------------------|--|--|--|---------------------------------|---------------------------------|
| Watchdog flag (WDF)   | 0  | 1  | Hold                                     | 0                               | Hold                            |
| Key return flag (KRF) | 0  | Hold   | 1  | Hold                            | 0                               |

**Figure 9-3. WDF Operation in Generating Each Signal**







## 10. MASK OPTION

The  $\mu$ PD754202 has the following mask options:

- Mask option of P70/KR4 through P73/KR7  
Pull-up resistors can be connected to these pins.
  - (1) No pull-up resistor connection
  - (2) Connection of a 30-k $\Omega$  (typ.) pull-up resistor in 1-bit units.
  - (3) Connection of a 100-k $\Omega$  (typ.) pull-up resistor in 1-bit units.
  
- Mask option of  $\overline{\text{RESET}}$  pin  
Pull-up resistors can be connected to these pins.
  - (1) No pull-up resistor connection
  - (2) Connection of a 100-k $\Omega$  (typ.) pull-up resistor.
  
- Standby function mask option  
The wait time after  $\overline{\text{RESET}}$  signal can be selected.
  - (1)  $2^{17}/f_x$  (21.8 ms:  $f_x = 6.0\text{-MHz}$  operation, 31.3 ms:  $f_x = 4.19\text{-MHz}$  operation)
  - (2)  $2^{15}/f_x$  (5.46 ms:  $f_x = 6.0\text{-MHz}$  operation, 7.81 ms:  $f_x = 4.19\text{-MHz}$  operation)

11. INSTRUCTION SETS

(1) Expression formats and description methods of operands

The operand is described in the operand column of each instruction in accordance with the description method for the operand expression format of the instruction. For details, refer to “**RA75X ASSEMBLER PACKAGE USERS’ MANUAL — LANGUAGE (EEU-1363)**”. If there are several elements, one of them is selected. Capital letters and the + and – symbols are key words and are described as they are.

For immediate data, appropriate numbers and labels are described.

Instead of the labels such as mem, fmem, pmem, and bit, the symbols of the register flags can be described. However, there are restrictions in the labels that can be described for fmem and pmem. For details, see **μPD754202 User’s Manual (U11132E)**.

| Expression format                                   | Description method   |
|---|--|
| reg<br>reg1   | X, A, B, C, D, E, H, L<br>X, B, C, D, E, H, L  |
| rp<br>rp1<br>rp2<br>rp'<br>rp'1                     | XA, BC, DE, HL<br>BC, DE, HL<br>BC, DE<br>XA, BC, DE, HL, XA', BC', DE', HL'<br>BC, DE, HL, XA', BC', DE', HL'                                 |
| rpa<br>rpa1   | HL, HL+, HL–, DE, DL<br>DE, DL   |
| n4<br>n8  | 4-bit immediate data or label<br>8-bit immediate data or label   |
| mem<br>bit  | 8-bit immediate data or label <sup>Note</sup><br>2-bit immediate data or label   |
| fmem<br>pmem  | FB0H-FBFH, FF0H-FFFH immediate data or label<br>FC0H-FFFH immediate data or label  |
| addr<br>addr1(only in Mk II mode)<br>caddr<br>faddr | 0000H-07FFH immediate data or label<br>0000H-07FFH immediate data or label<br>12-bit immediate data or label<br>11-bit immediate data or label |
| taddr   | 20H-7FH immediate data (where bit0 = 0) or label   |
| PORTn<br>IExxx<br>RBn<br>MBn                        | PORT3, 6, 7, 8<br>IEBT, IET0-IET2, IE0, IE2<br>RB0-RB3<br>MB0, MB15  |

**Note** mem can be only used for even address in 8-bit data processing.

**(2) Legend in explanation of operation**

|                   |   |
|-------------------|---|
| A                 | : A register; 4-bit accumulator         |
| B                 | : B register                            |
| C                 | : C register                            |
| D                 | : D register                            |
| E                 | : E register                            |
| H                 | : H register                            |
| L                 | : L register                            |
| X                 | : X register                            |
| XA                | : XA register pair; 8-bit accumulator   |
| BC                | : BC register pair                      |
| DE                | : DE register pair                      |
| HL                | : HL register pair                      |
| XA'               | : XA' extended register pair            |
| BC'               | : BC' extended register pair            |
| DE'               | : DE' extended register pair            |
| HL'               | : HL' extended register pair            |
| PC                | : Program counter                       |
| SP                | : Stack pointer                         |
| CY                | : Carry flag; bit accumulator           |
| PSW               | : Program status word                   |
| MBE               | : Memory bank enable flag               |
| RBE               | : Register bank enable flag             |
| PORT <sub>n</sub> | : Port n (n = 3, 6, 7, 8)               |
| IME               | : Interrupt master enable flag          |
| IPS               | : Interrupt priority selection register |
| IE <sub>xxx</sub> | : Interrupt enable flag                 |
| RBS               | : Register bank selection register      |
| MBS               | : Memory bank selection register        |
| PCC               | : Processor clock control register      |
| .                 | : Separation between address and bit    |
| (xx)              | : The contents addressed by xx          |
| xxH               | : Hexadecimal data                      |

**(3) Explanation of symbols under addressing area column**

|     |   |  |
|-----|---|--|
| *1  | MB = MBE•MBS<br>(MBS = 0, 15)   |  |
| *2  | MB = 0  |  |
| *3  | MBE = 0 : MB = 0 (000H-07FH)<br>MB = 15 (F80H-FFFH)<br>MBE = 1 : MB = MBS (MBS = 0, 15)   |  |
| *4  | MB = 15, fmem = FB0H-FBFH, FF0H-FFFH  |  |
| *5  | MB = 15, pmem = FC0H-FFFH   |  |
| *6  | addr = 0000H-07FFH  |  |
| *7  | addr = (Current PC) – 15 to (Current PC) – 1<br>(Current PC) + 2 to (Current PC) + 16<br>addr1 = (Current PC) – 15 to (Current PC) – 1<br>(Current PC) + 2 to (Current PC) + 16 |  |
| *8  | caddr = 0000H-07FFH   |  |
| *9  | faddr = 0000H-07FFH   |  |
| *10 | taddr = 0020H-007FH   |  |
| *11 | addr1 = 0000H-07FFH   |  |

- Remarks**
1. MB indicates memory bank that can be accessed.
  2. In \*2, MB = 0 independently of how MBE and MBS are set.
  3. In \*4 and \*5, MB = 15 independently of how MBE and MBS are set.
  4. \*6 to \*11 indicate the areas that can be addressed.

**(4) Explanation of number of machine cycles column**

S denotes the number of machine cycles required by skip operation when a skip instruction is executed. The value of S varies as follows.

- When no skip is made: S = 0
- When the skipped instruction is a 1- or 2-byte instruction: S = 1
- When the skipped instruction is a 3-byte instruction<sup>Note</sup>: S = 2

**Note** 3-byte instruction: BR !addr, BRA !addr1, CALL !addr, or CALLA !addr1 instruction

**Caution** The GETI instruction is skipped in one machine cycle.

One machine cycle is equal to one cycle of the CPU clock (= tcy); time can be selected from among four types by setting PCC.

| Instruction group    | Mnemonic                     | Operand   | Number of bytes | Number of machine cycles | Operation                                    | Addressing area                              | Skip condition  |
|----------------------|------------------------------|-----------|-----------------|--------------------------|--|--|-----------------|
| Transfer instruction | MOV                          | A, #n4    | 1               | 1                        | A ← n4                                       |  | String effect A |
|                      |                              | reg1, #n4 | 2               | 2                        | reg1 ← n4                                    |  |                 |
|                      |                              | XA, #n8   | 2               | 2                        | XA ← n8                                      |  | String effect A |
|                      |                              | HL, #n8   | 2               | 2                        | HL ← n8                                      |  | String effect B |
|                      |                              | rp2, #n8  | 2               | 2                        | rp2 ← n8                                     |  |                 |
|                      |                              | A, @HL    | 1               | 1                        | A ← (HL)                                     | *1   |                 |
|                      |                              | A, @HL+   | 1               | 2+S                      | A ← (HL), then L ← L+1                       | *1   | L = 0           |
|                      |                              | A, @HL-   | 1               | 2+S                      | A ← (HL), then L ← L-1                       | *1   | L = FH          |
|                      |                              | A, @rpa1  | 1               | 1                        | A ← (rpa1)                                   | *2   |                 |
|                      |                              | XA, @HL   | 2               | 2                        | XA ← (HL)                                    | *1   |                 |
|                      |                              | @HL, A    | 1               | 1                        | (HL) ← A                                     | *1   |                 |
|                      |                              | @HL, XA   | 2               | 2                        | (HL) ← XA                                    | *1   |                 |
|                      |                              | A, mem    | 2               | 2                        | A ← (mem)                                    | *3   |                 |
|                      |                              | XA, mem   | 2               | 2                        | XA ← (mem)                                   | *3   |                 |
|                      |                              | mem, A    | 2               | 2                        | (mem) ← A                                    | *3   |                 |
|                      |                              | mem, XA   | 2               | 2                        | (mem) ← XA                                   | *3   |                 |
|                      |                              | A, reg    | 2               | 2                        | A ← reg                                      |  |                 |
|                      |                              | XA, rp'   | 2               | 2                        | XA ← rp'                                     |  |                 |
|                      |                              | reg1, A   | 2               | 2                        | reg1 ← A                                     |  |                 |
|                      |                              | rp'1, XA  | 2               | 2                        | rp'1 ← XA                                    |  |                 |
|                      | XCH                          | A, @HL    | 1               | 1                        | A ↔ (HL)                                     | *1   |                 |
|                      |                              | A, @HL+   | 1               | 2+S                      | A ↔ (HL), then L ← L+1                       | *1   | L = 0           |
|                      |                              | A, @HL-   | 1               | 2+S                      | A ↔ (HL), then L ← L-1                       | *1   | L = FH          |
|                      |                              | A, @rpa1  | 1               | 1                        | A ↔ (rpa1)                                   | *2   |                 |
|                      |                              | XA, @HL   | 2               | 2                        | XA ↔ (HL)                                    | *1   |                 |
|                      |                              | A, mem    | 2               | 2                        | A ↔ (mem)                                    | *3   |                 |
|                      |                              | XA, mem   | 2               | 2                        | XA ↔ (mem)                                   | *3   |                 |
|                      |                              | A, reg1   | 1               | 1                        | A ↔ reg1                                     |  |                 |
|                      |                              | XA, rp'   | 2               | 2                        | XA ↔ rp'                                     |  |                 |
|                      | Table reference instructions | MOVT      | XA, @PCDE       | 1                        | 3  | XA ← (PC <sub>10-8</sub> +DE) <sub>ROM</sub> |                 |
| XA, @PCXA            |                              |           | 1               | 3                        | XA ← (PC <sub>10-8</sub> +XA) <sub>ROM</sub> |  |                 |
| XA, @BCDE            |                              |           | 1               | 3                        | XA ← (BCDE) <sub>ROM</sub> <sup>Note</sup>   | *6   |                 |
| XA, @BCXA            |                              |           | 1               | 3                        | XA ← (BCXA) <sub>ROM</sub> <sup>Note</sup>   | *6   |                 |

**Note** "0" must be set to the B register.

| Instruction group                     | Mnemonic | Operand        | Number of bytes | Number of machine cycles       | Operation  | Addressing area | Skip condition |
|---------------------------------------|----------|----------------|-----------------|--------------------------------|--|-----------------|----------------|
| Bit transfer instructions             | MOV1     | CY, fmem.bit   | 2               | 2                              | $CY \leftarrow (fmem.bit)$                                     | *4              |                |
|                                       |          | CY, pmem.@L    | 2               | 2                              | $CY \leftarrow (pmem_{7-2+L_{3-2}.bit(L_{1-0}))$               | *5              |                |
|                                       |          | CY, @H+mem.bit | 2               | 2                              | $CY \leftarrow (H+mem_{3-0}.bit)$                              | *1              |                |
|                                       |          | fmem.bit, CY   | 2               | 2                              | $(fmem.bit) \leftarrow CY$                                     | *4              |                |
|                                       |          | pmem.@L, CY    | 2               | 2                              | $(pmem_{7-2+L_{3-2}.bit(L_{1-0})) \leftarrow CY$               | *5              |                |
|                                       |          | @H+mem.bit, CY | 2               | 2                              | $(H+mem_{3-0}.bit) \leftarrow CY$                              | *1              |                |
| Operation instructions                | ADDS     | A, #n4         | 1               | 1+S                            | $A \leftarrow A+n4$  |                 | carry          |
|                                       |          | XA, #n8        | 2               | 2+S                            | $XA \leftarrow XA+n8$  |                 | carry          |
|                                       |          | A, @HL         | 1               | 1+S                            | $A \leftarrow A+(HL)$  | *1              | carry          |
|                                       |          | XA, rp'        | 2               | 2+S                            | $XA \leftarrow XA+rp'$   |                 | carry          |
|                                       |          | rp'1, XA       | 2               | 2+S                            | $rp'1 \leftarrow rp'1+XA$                                      |                 | carry          |
|                                       | ADDC     | A, @HL         | 1               | 1                              | $A, CY \leftarrow A+(HL)+CY$                                   | *1              |                |
|                                       |          | XA, rp'        | 2               | 2                              | $XA, CY \leftarrow XA+rp'+CY$                                  |                 |                |
|                                       |          | rp'1, XA       | 2               | 2                              | $rp'1, CY \leftarrow rp'1+XA+CY$                               |                 |                |
|                                       | SUBS     | A, @HL         | 1               | 1+S                            | $A \leftarrow A-(HL)$  | *1              | borrow         |
|                                       |          | XA, rp'        | 2               | 2+S                            | $XA \leftarrow XA-rp'$   |                 | borrow         |
|                                       |          | rp'1, XA       | 2               | 2+S                            | $rp'1 \leftarrow rp'1-XA$                                      |                 | borrow         |
|                                       | SUBC     | A, @HL         | 1               | 1                              | $A, CY \leftarrow A-(HL)-CY$                                   | *1              |                |
|                                       |          | XA, rp'        | 2               | 2                              | $XA, CY \leftarrow XA-rp'-CY$                                  |                 |                |
|                                       |          | rp'1, XA       | 2               | 2                              | $rp'1, CY \leftarrow rp'1-XA-CY$                               |                 |                |
|                                       | AND      | A, #n4         | 2               | 2                              | $A \leftarrow A \wedge n4$                                     |                 |                |
|                                       |          | A, @HL         | 1               | 1                              | $A \leftarrow A \wedge (HL)$                                   | *1              |                |
|                                       |          | XA, rp'        | 2               | 2                              | $XA \leftarrow XA \wedge rp'$                                  |                 |                |
|                                       |          | rp'1, XA       | 2               | 2                              | $rp'1 \leftarrow rp'1 \wedge XA$                               |                 |                |
|                                       | OR       | A, #n4         | 2               | 2                              | $A \leftarrow A \vee n4$                                       |                 |                |
|                                       |          | A, @HL         | 1               | 1                              | $A \leftarrow A \vee (HL)$                                     | *1              |                |
|                                       |          | XA, rp'        | 2               | 2                              | $XA \leftarrow XA \vee rp'$                                    |                 |                |
|                                       |          | rp'1, XA       | 2               | 2                              | $rp'1 \leftarrow rp'1 \vee XA$                                 |                 |                |
|                                       | XOR      | A, #n4         | 2               | 2                              | $A \leftarrow A \vee n4$                                       |                 |                |
|                                       |          | A, @HL         | 1               | 1                              | $A \leftarrow A \vee (HL)$                                     | *1              |                |
| XA, rp'                               |          | 2              | 2               | $XA \leftarrow XA \vee rp'$    |  |                 |                |
| rp'1, XA                              |          | 2              | 2               | $rp'1 \leftarrow rp'1 \vee XA$ |  |                 |                |
| Accumulator manipulation instructions | RORC     | A              | 1               | 1                              | $CY \leftarrow A_0, A_3 \leftarrow CY, A_{n-1} \leftarrow A_n$ |                 |                |
|                                       | NOT      | A              | 2               | 2                              | $A \leftarrow \bar{A}$   |                 |                |

| Instruction group                    | Mnemonic | Operand    | Number of bytes | Number of machine cycles | Operation   | Addressing area | Skip condition   |
|--------------------------------------|----------|------------|-----------------|--------------------------|---|-----------------|------------------|
| Increment and Decrement instructions | INCS     | reg        | 1               | 1+S                      | reg ← reg+1   |                 | reg = 0          |
|                                      |          | rp1        | 1               | 1+S                      | rp1 ← rp1+1   |                 | rp1 = 00H        |
|                                      |          | @HL        | 2               | 2+S                      | (HL) ← (HL)+1   | *1              | (HL) = 0         |
|                                      |          | mem        | 2               | 2+S                      | (mem) ← (mem)+1   | *3              | (mem) = 0        |
|                                      | DECS     | reg        | 1               | 1+S                      | reg ← reg-1   |                 | reg = FH         |
|                                      |          | rp'        | 2               | 2+S                      | rp' ← rp'-1   |                 | rp' = FFH        |
| Comparison instruction               | SKE      | reg, #n4   | 2               | 2+S                      | Skip if reg = n4  |                 | reg = n4         |
|                                      |          | @HL, #n4   | 1               | 2+S                      | Skip if (HL) = n4   | *1              | (HL) = n4        |
|                                      |          | A, @HL     | 2               | 1+S                      | Skip if A = (HL)  | *1              | A = (HL)         |
|                                      |          | XA, @HL    | 2               | 2+S                      | Skip if XA = (HL)   | *1              | XA = (HL)        |
|                                      |          | A, reg     | 2               | 2+S                      | Skip if A = reg   |                 | A = reg          |
|                                      |          | XA, rp'    | 2               | 2+S                      | Skip if XA = rp'  |                 | XA = rp'         |
| Carry flag manipulation instruction  | SET1     | CY         | 1               | 1                        | CY ← 1  |                 |                  |
|                                      | CLR1     | CY         | 1               | 1                        | CY ← 0  |                 |                  |
|                                      | SKT      | CY         | 1               | 1+S                      | Skip if CY = 1  |                 | CY = 1           |
|                                      | NOT1     | CY         | 1               | 1                        | CY ← $\overline{CY}$  |                 |                  |
| Memory bit manipulation instructions | SET1     | mem.bit    | 2               | 2                        | (mem.bit) ← 1   | *3              |                  |
|                                      |          | fmem.bit   | 2               | 2                        | (fmem.bit) ← 1  | *4              |                  |
|                                      |          | pmem.@L    | 2               | 2                        | (pmem <sub>7-2</sub> +L <sub>3-2</sub> .bit(L <sub>1-0</sub> )) ← 1         | *5              |                  |
|                                      |          | @H+mem.bit | 2               | 2                        | (H+mem <sub>3-0</sub> .bit) ← 1   | *1              |                  |
|                                      | CLR1     | mem.bit    | 2               | 2                        | (mem.bit) ← 0   | *3              |                  |
|                                      |          | fmem.bit   | 2               | 2                        | (fmem.bit) ← 0  | *4              |                  |
|                                      |          | pmem.@L    | 2               | 2                        | (pmem <sub>7-2</sub> +L <sub>3-2</sub> .bit(L <sub>1-0</sub> )) ← 0         | *5              |                  |
|                                      |          | @H+mem.bit | 2               | 2                        | (H+mem <sub>3-0</sub> .bit) ← 0   | *1              |                  |
|                                      | SKT      | mem.bit    | 2               | 2+S                      | Skip if (mem.bit) = 1   | *3              | (mem.bit) = 1    |
|                                      |          | fmem.bit   | 2               | 2+S                      | Skip if (fmem.bit) = 1  | *4              | (fmem.bit) = 1   |
|                                      |          | pmem.@L    | 2               | 2+S                      | Skip if (pmem <sub>7-2</sub> +L <sub>3-2</sub> .bit(L <sub>1-0</sub> )) = 1 | *5              | (pmem.@L) = 1    |
|                                      |          | @H+mem.bit | 2               | 2+S                      | Skip if (H+mem <sub>3-0</sub> .bit) = 1                                     | *1              | (@H+mem.bit) = 1 |
|                                      | SKF      | mem.bit    | 2               | 2+S                      | Skip if (mem.bit) = 0   | *3              | (mem.bit) = 0    |
|                                      |          | fmem.bit   | 2               | 2+S                      | Skip if (fmem.bit) = 0  | *4              | (fmem.bit) = 0   |
|                                      |          | pmem.@L    | 2               | 2+S                      | Skip if (pmem <sub>7-2</sub> +L <sub>3-2</sub> .bit(L <sub>1-0</sub> )) = 0 | *5              | (pmem.@L) = 0    |
|                                      |          | @H+mem.bit | 2               | 2+S                      | Skip if (H+mem <sub>3-0</sub> .bit) = 0                                     | *1              | (@H+mem.bit) = 0 |



| Instruction group                    | Mnemonic              | Operand        | Number of bytes | Number of machine cycles                   | Operation   | Addressing area | Skip condition   |
|--------------------------------------|-----------------------|----------------|-----------------|--|---|-----------------|------------------|
| Memory bit manipulation instructions | SKTCLR                | fmem.bit       | 2               | 2+S  | Skip if (fmem.bit) = 1 and clear  | *4              | (fmem.bit) = 1   |
|                                      |                       | pmem.@L        | 2               | 2+S  | Skip if (pmem <sub>7-2+L3-2</sub> .bit(L <sub>1-0</sub> )) = 1 and clear  | *5              | (pmem.@L) = 1    |
|                                      |                       | @H+mem.bit     | 2               | 2+S  | Skip if (H+mem <sub>3-0</sub> .bit) = 1 and clear   | *1              | (@H+mem.bit) = 1 |
|                                      | AND1                  | CY, fmem.bit   | 2               | 2  | CY ← CY ∧ (fmem.bit)  | *4              |                  |
|                                      |                       | CY, pmem.@L    | 2               | 2  | CY ← CY ∧ (pmem <sub>7-2+L3-2</sub> .bit(L <sub>1-0</sub> ))  | *5              |                  |
|                                      |                       | CY, @H+mem.bit | 2               | 2  | CY ← CY ∧ (H+mem <sub>3-0</sub> .bit)   | *1              |                  |
|                                      | OR1                   | CY, fmem.bit   | 2               | 2  | CY ← CY ∨ (fmem.bit)  | *4              |                  |
|                                      |                       | CY, pmem.@L    | 2               | 2  | CY ← CY ∨ (pmem <sub>7-2+L3-2</sub> .bit(L <sub>1-0</sub> ))  | *5              |                  |
|                                      |                       | CY, @H+mem.bit | 2               | 2  | CY ← CY ∨ (H+mem <sub>3-0</sub> .bit)   | *1              |                  |
|                                      | XOR1                  | CY, fmem.bit   | 2               | 2  | CY ← CY ⊕ (fmem.bit)  | *4              |                  |
|                                      |                       | CY, pmem.@L    | 2               | 2  | CY ← CY ⊕ (pmem <sub>7-2+L3-2</sub> .bit(L <sub>1-0</sub> ))  | *5              |                  |
|                                      |                       | CY, @H+mem.bit | 2               | 2  | CY ← CY ⊕ (H+mem <sub>3-0</sub> .bit)   | *1              |                  |
| Branch instructions                  | BR <sup>Note 1</sup>  | addr           | –               | –  | PC <sub>10-0</sub> ← addr<br>(Select appropriate instruction among BR !addr, BRCB !caddr, and BR \$addr according to the assembler being used.)               | *6              |                  |
|                                      |                       | addr1          | –               | –  | PC <sub>10-0</sub> ← addr1<br>(Select appropriate instruction among BR !addr, BRA !addr1, BRCB !caddr, and BR \$addr1 according to the assembler being used.) | *11             |                  |
|                                      |                       | !addr          | 3               | 3  | PC <sub>10-0</sub> ← addr   | *6              |                  |
|                                      |                       | \$addr         | 1               | 2  | PC <sub>10-0</sub> ← addr   | *7              |                  |
|                                      |                       | \$addr1        | 1               | 2  | PC <sub>10-0</sub> ← addr1  |                 |                  |
|                                      |                       | PCDE           | 2               | 3  | PC <sub>10-0</sub> ← PC <sub>10-8</sub> +DE   |                 |                  |
|                                      |                       | PCXA           | 2               | 3  | PC <sub>10-0</sub> ← PC <sub>10-8</sub> +XA   |                 |                  |
|                                      |                       | BCDE           | 2               | 3  | PC <sub>10-0</sub> ← BCDE <sup>Note 2</sup>   | *6              |                  |
|                                      |                       | BCXA           | 2               | 3  | PC <sub>10-0</sub> ← BCXA <sup>Note 2</sup>   | *6              |                  |
|                                      | BRA <sup>Note 1</sup> | !addr1         | 3               | 3  | PC <sub>10-0</sub> ← addr1  | *11             |                  |
| BRCB                                 | !caddr                | 2              | 2               | PC <sub>10-0</sub> ← caddr <sub>10-0</sub> | *8  |                 |                  |

**Notes 1.** The above operations in the shaded boxes can be performed only in the Mk II mode. The other operations can be performed only in the MK I mode.

**2.** “0” must be set to the B register.

| Instruction group   | Mnemonic              | Operand | Number of bytes | Number of machine cycles              | Operation  | Addressing area | Skip condition |
|---|-----------------------|---------|-----------------|---------------------------------------|--|-----------------|----------------|
| Subroutine stack control instructions   | CALLA <sup>Note</sup> | !addr1  | 3               | 3                                     | (SP-2) ← x, x, MBE, RBE<br>(SP-6) (SP-3) (SP-4) ← 0, PC <sub>10-0</sub><br>(SP-5) ← 0, 0, 0, 0<br>PC <sub>10-0</sub> ← addr1, SP ← SP-6            | *11             |                |
|   | CALL <sup>Note</sup>  | !addr   | 3               | 3                                     | (SP-3) ← MBE, RBE, 0, 0<br>(SP-4) (SP-1) (SP-2) ← 0, PC <sub>10-0</sub><br>PC <sub>10-0</sub> ← addr, SP ← SP-4                                    | *6              |                |
|   |                       |         |                 | 4                                     | (SP-2) ← x, x, MBE, RBE<br>(SP-6) (SP-3) (SP-4) ← 0, PC <sub>10-0</sub><br>(SP-5) ← 0, 0, 0, 0<br>PC <sub>10-0</sub> ← addr, SP ← SP-6             |                 |                |
|   | CALLF <sup>Note</sup> | !faddr  | 2               | 2                                     | (SP-3) ← MBE, RBE, 0, 0<br>(SP-4) (SP-1) (SP-2) ← 0, PC <sub>10-0</sub><br>PC <sub>10-0</sub> ← 0+faddr, SP ← SP-4                                 | *9              |                |
|   |                       |         |                 | 3                                     | (SP-2) ← x, x, MBE, RBE<br>(SP-6) (SP-3) (SP-4) ← 0, PC <sub>10-0</sub><br>(SP-5) ← 0, 0, 0, 0<br>PC <sub>10-0</sub> ← 0+faddr, SP ← SP-6          |                 |                |
|   | RET <sup>Note</sup>   |         | 1               | 3                                     | PC <sub>10-0</sub> ← (SP) <sub>2-0</sub> (SP+3) (SP+2)<br>MBE, RBE, 0, 0 ← (SP+1), SP ← SP+4   |                 |                |
|   |                       |         |                 |                                       | x, x, MBE, RBE ← (SP+4)<br>0, 0, 0, 0 ← (SP+1)<br>PC <sub>10-0</sub> ← (SP) <sub>2-0</sub> (SP+3) (SP+2), SP ← SP+6                                |                 |                |
|   | RETS <sup>Note</sup>  |         | 1               | 3+S                                   | MBE, RBE, 0, 0 ← (SP+1)<br>PC <sub>10-0</sub> ← (SP) <sub>2-0</sub> (SP+3) (SP+2)<br>SP ← SP+4<br>then skip unconditionally                        |                 | Unconditional  |
|   |                       |         |                 |                                       | 0, 0, 0, 0 ← (SP+1)<br>PC <sub>10-0</sub> ← (SP) <sub>2-0</sub> (SP+3) (SP+2)<br>x, x, MBE, RBE ← (SP+4)<br>SP ← SP+6<br>then skip unconditionally |                 |                |
|   | RETJ <sup>Note</sup>  |         | 1               | 3                                     | MBE, RBE, 0, 0 ← (SP+1)<br>PC <sub>10-0</sub> ← (SP) <sub>2-0</sub> (SP+3) (SP+2)<br>PSW ← (SP+4) (SP+5), SP ← SP+6                                |                 |                |
| 0, 0, 0, 0 ← (SP+1)<br>PC <sub>10-0</sub> ← (SP) <sub>2-0</sub> (SP+3) (SP+2)<br>PSW ← (SP+4) (SP+5), SP ← SP+6 |                       |         |                 |                                       |  |                 |                |
| PUSH  | rp                    | 1       | 1               | (SP-1) (SP-2) ← rp, SP ← SP-2         |  |                 |                |
|   | BS                    | 2       | 2               | (SP-1) ← MBS, (SP-2) ← RBS, SP ← SP-2 |  |                 |                |
| POP   | rp                    | 1       | 1               | rp ← (SP+1) (SP), SP ← SP+2           |  |                 |                |
|   | BS                    | 2       | 2               | MBS ← (SP+1), RBS ← (SP), SP ← SP+2   |  |                 |                |

**Note** The above operations in the shaded boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

| Instruction group   | Mnemonic                               | Operand               | Number of bytes | Number of machine cycles | Operation  | Addressing area | Skip condition |  |
|---|--|-----------------------|-----------------|--------------------------|--|-----------------|----------------|--|
| Interrupt control instructions  | EI                                     |                       | 2               | 2                        | IME (IPS.3) ← 1  |                 |                |  |
|   |  | IE <sub>xxx</sub>     | 2               | 2                        | IE <sub>xxx</sub> ← 1  |                 |                |  |
|   | DI                                     |                       | 2               | 2                        | IME (IPS.3) ← 0  |                 |                |  |
|   |  | IE <sub>xxx</sub>     | 2               | 2                        | IE <sub>xxx</sub> ← 0  |                 |                |  |
| Input/output instructions   | IN <sup>Note 1</sup>                   | A, PORT <sub>n</sub>  | 2               | 2                        | A ← PORT <sub>n</sub> (n = 3, 6, 7, 8)   |                 |                |  |
|   | OUT <sup>Note 1</sup>                  | PORT <sub>n</sub> , A | 2               | 2                        | PORT <sub>n</sub> ← A (n = 3, 6, 8)  |                 |                |  |
| CPU control instructions  | HALT                                   |                       | 2               | 2                        | Set HALT Mode (PCC.2 ← 1)  |                 |                |  |
|   | STOP                                   |                       | 2               | 2                        | Set STOP Mode (PCC.3 ← 1)  |                 |                |  |
|   | NOP                                    |                       | 1               | 1                        | No Operation   |                 |                |  |
| Special instructions  | SEL                                    | RB <sub>n</sub>       | 2               | 2                        | RBS ← n (n = 0-3)  |                 |                |  |
|   |  | MB <sub>n</sub>       | 2               | 2                        | MBS ← n (n = 0, 15)  |                 |                |  |
|   | GETI <sup>Notes 2, 3</sup>             | taddr                 | 1               | 3                        | <ul style="list-style-type: none"> <li>When TBR instruction<br/>PC<sub>10-0</sub> ← (taddr)<sub>2-0</sub> + (taddr+1)</li> </ul>   | *10             |                |  |
|   |  |                       |                 |                          | <ul style="list-style-type: none"> <li>When TCALL instruction<br/>(SP-4) (SP-1) (SP-2) ← 0, PC<sub>10-0</sub><br/>(SP-3) ← MBE, RBE, 0, 0<br/>PC<sub>10-0</sub> ← (taddr)<sub>2-0</sub> + (taddr+1)<br/>SP ← SP-4</li> </ul> |                 |                |  |
|   |  |                       |                 |                          | <ul style="list-style-type: none"> <li>When instruction other than TBR and TCALL instructions (taddr) (taddr+1) instruction is executed.</li> </ul>  |                 |                | Depending on the reference instruction |
|   |  |                       |                 |                          | <ul style="list-style-type: none"> <li>When TBR instruction<br/>PC<sub>10-0</sub> ← (taddr)<sub>2-0</sub> + (taddr+1)</li> </ul>   |                 |                | *10                                    |
| <ul style="list-style-type: none"> <li>When TCALL instruction<br/>(SP-6) (SP-3) (SP-4) ← PC<sub>10-0</sub><br/>(SP-5) ← 0, 0, 0, 0<br/>(SP-2) ← x, x, MBE, RBE<br/>PC<sub>10-0</sub> ← (taddr)<sub>2-0</sub> + (taddr+1)<br/>SP ← SP-6</li> </ul> |  |                       |                 |                          |  |                 |                |  |
| <ul style="list-style-type: none"> <li>When instruction other than TBR and TCALL instructions (taddr) (taddr+1) instruction is executed.</li> </ul>   | Depending on the reference instruction |                       |                 |                          |  |                 |                |  |

- Notes**
- While the IN instruction and OUT instruction are being executed, MBS must be set to 0, or MBE must be set to 1 and MBS must be set to 15.
  - The TBR and TCALL instructions are the table definition assembler pseudo instructions of the GETI instruction.
  - The above operations in the shaded boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

12. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T<sub>A</sub> = 25 °C)

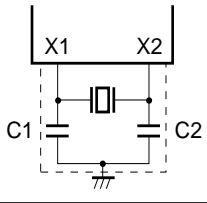
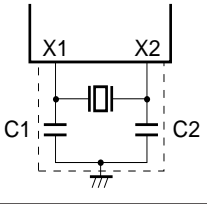
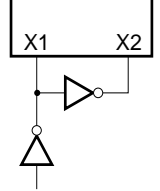
| Parameter                     | Symbol           | Test Conditions |                 | Ratings                       | Unit |
|-------------------------------|------------------|-----------------|-----------------|-------------------------------|------|
| Supply voltage                | V <sub>DD</sub>  |                 |                 | -0.3 to +7.0                  | V    |
| Input voltage                 | V <sub>I</sub>   |                 |                 | -0.3 to V <sub>DD</sub> + 0.3 | V    |
| Output voltage                | V <sub>O</sub>   |                 |                 | -0.3 to V <sub>DD</sub> + 0.3 | V    |
| Output current, high          | I <sub>OH</sub>  | Per pin         | Pins except P32 | -10                           | mA   |
|                               |                  |                 | Only P32        | -20                           | mA   |
|                               |                  | All pins total  |                 | -30                           | mA   |
| Output current, low           | I <sub>OL</sub>  | Per pin         |                 | 20                            | mA   |
|                               |                  | All pins total  |                 | 90                            | mA   |
| Operating ambient temperature | T <sub>A</sub>   |                 |                 | -40 to +85                    | °C   |
| Storage temperature           | T <sub>stg</sub> |                 |                 | -65 to +150                   | °C   |

**Caution** If any of the parameters exceeds the absolute maximum ratings, even momentarily, the quality of the product may be impaired. The absolute maximum ratings are values that may physically damage the products. Be sure to use the products within the ratings.

Capacitance (T<sub>A</sub> = 25 °C, V<sub>DD</sub> = 0 V)

| Parameter          | Symbol           | Test Conditions                 | MIN. | TYP. | MAX. | Unit |
|--------------------|------------------|---------------------------------|------|------|------|------|
| Input capacitance  | C <sub>IN</sub>  | f = 1 MHz                       |      |      | 15   | pF   |
| Output capacitance | C <sub>OUT</sub> | Unmeasured pins returned to 0 V |      |      | 15   | pF   |
| I/O capacitance    | C <sub>IO</sub>  |                                 |      |      | 15   | pF   |

**System Clock Oscillator Characteristics (T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 1.8 to 6.0 V)**

| Resonator         | Recommended Constant  | Parameter  | Testing Conditions  | MIN. | TYP. | MAX.                  | Unit |
|-------------------|---|--|---|------|------|-----------------------|------|
| Ceramic resonator |  | Oscillation frequency (f <sub>x</sub> ) <sup>Note 1</sup>                |   | 1.0  |      | 6.0 <sup>Note 2</sup> | MHz  |
|                   |   | Oscillation stabilization time <sup>Note 3</sup>                         | After V <sub>DD</sub> reaches MIN. value of oscillation voltage range |      |      | 4                     | ms   |
| Crystal resonator |  | Oscillation frequency (f <sub>x</sub> ) <sup>Note 1</sup>                |   | 1.0  |      | 6.0 <sup>Note 2</sup> | MHz  |
|                   |   | Oscillation stabilization time <sup>Note 3</sup>                         | V <sub>DD</sub> = 4.5 to 6.0 V  |      |      | 10                    | ms   |
|                   |   |  |   |      |      | 30                    | ms   |
| External clock    |  | X1 input frequency (f <sub>x</sub> ) <sup>Note 1</sup>                   |   | 1.0  |      | 6.0 <sup>Note 2</sup> | MHz  |
|                   |   | X1 input high- and low-level widths (t <sub>xH</sub> , t <sub>xL</sub> ) |   | 83.3 |      | 500                   | ns   |

- Notes 1.** Only the oscillator characteristics are shown. For the instruction execution time, refer to **AC Characteristics**.
- If the oscillation frequency is 4.19 MHz < f<sub>x</sub> ≤ 6.0 MHz at 1.8 V ≤ V<sub>DD</sub> < 2.7 V, set the processor clock control register (PCC) to a value other than 0011. If the PCC is set to 0011, the rated machine cycle time of 0.95 μs is not satisfied.
  - The oscillation stabilization time is the time required for oscillation to stabilize after application of V<sub>DD</sub>, or after the STOP mode has been released.

**Caution** When using the oscillation circuit of the system clock, wire the portion enclosed in dotted lines in the figures as follows to avoid adverse influences on the wiring capacitance:

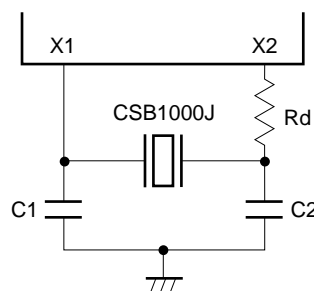
- Keep the wire length as short as possible.
- Do not cross other signal lines.
- Do not route the wiring in the vicinity of lines through which a high fluctuating current flows.
- Always keep the ground point of the capacitor of the oscillation circuit as the same potential as V<sub>SS</sub>.
- Do not connect the power source pattern through which a high current flows.
- Do not extract signals from the oscillation circuit.

RECOMMENDED CIRCUIT CONSTANTS

Ceramic Resonator (TA = -20 to +80 °C)

| Manufacturer          | Product                  | Frequency (MHz) | Circuit constant (pF) |                        | Oscillation voltage range (VDD) |                        | Remark      |
|-----------------------|--------------------------|-----------------|-----------------------|------------------------|---------------------------------|------------------------|-------------|
|                       |                          |                 | C1                    | C2                     | MIN.(V)                         | MAX.(V)                |             |
| Murata Mfg. Co., Ltd. | CSB1000J <sup>Note</sup> | 1.0             | 100                   | 100                    | 2.0                             | 6.0                    | Rd = 2.2 kΩ |
|                       | CSA2.00MG040             | 2.0             | 100                   | 100                    |                                 |                        | -           |
|                       | CST2.00MG040             |                 | -                     | -                      | Capacitor incorporated          |                        |             |
|                       | CSA4.00MG                | 4.0             | 30                    | 30                     | -                               |                        |             |
|                       | CST4.00MGW               |                 | -                     | -                      | Capacitor incorporated          |                        |             |
|                       | CSA4.00MGU               | 4.0             | 30                    | 30                     | 1.8                             | -                      |             |
|                       | CST4.00MGWU              |                 | -                     | -                      | Capacitor incorporated          |                        |             |
|                       | CSA4.19MG                | 4.19            | 30                    | 30                     | 2.0                             | -                      |             |
|                       | CST4.19MGW               |                 | -                     | -                      | Capacitor incorporated          |                        |             |
|                       | CSA4.19MGU               | 4.19            | 30                    | 30                     | 1.8                             | -                      |             |
|                       | CST4.19MGWU              |                 | -                     | -                      | Capacitor incorporated          |                        |             |
|                       | CSA6.00MG                | 6.0             | 30                    | 30                     | 2.9                             | -                      |             |
|                       | CST6.00MGW               |                 | -                     | -                      | Capacitor incorporated          |                        |             |
|                       | CSA6.00MGU               | 6.0             | 30                    | 30                     | 2.4                             | -                      |             |
| CST6.00MGWU           | -                        |                 | -                     | Capacitor incorporated |                                 |                        |             |
| Kyocera Corp.         | KBR-1000F/Y              | 1.0             | 100                   | 100                    | 1.8                             | 6.0                    | -           |
|                       | KBR-2.0MS                | 2.0             | 68                    | 68                     | 2.0                             |                        | -           |
|                       | KBR-4.19MKC              | 4.19            | -                     | -                      | 1.8                             | Capacitor incorporated |             |
|                       | KBR-4.19MSB              |                 | 33                    | 33                     |                                 | -                      |             |
|                       | PBRC4.19A                | 4.19            | -                     | -                      | 1.8                             | Capacitor incorporated |             |
|                       | PBRC4.19B                |                 | -                     | -                      |                                 | -                      |             |
|                       | KBR-6.0MKC               | 6.0             | 33                    | 33                     | 1.8                             | -                      |             |
|                       | KBR-6.0MSB               |                 | 33                    | 33                     |                                 | -                      |             |
|                       | PBRC6.00A                |                 | -                     | -                      |                                 | -                      |             |
|                       | PBRC6.00B                |                 | -                     | -                      |                                 | Capacitor incorporated |             |

**Note** If using Murata's CSB1000J (1.0 MHz) as the ceramic resonator, a limited resistor (Rd = 2.2 kΩ) is required (see figure below). If using any other recommended resonator, no limited resistor is needed.



**Caution** The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation, but do not guarantee oscillation frequency accuracy. If oscillation frequency accuracy is required for actual circuits, it is necessary to adjust the oscillation frequency of the resonator in the circuit. Please inquire directly to the maker of the resonator for data as needed.

DC Characteristics (T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 1.8 to 6.0 V)

| Parameter                      | Symbol              | Conditions  |   | MIN.                 | TYP.            | MAX.                | Unit |
|--------------------------------|---------------------|---|---|----------------------|-----------------|---------------------|------|
| High-level output current      | I <sub>OH</sub>     | Per pin   | Pins except P32   |                      |                 | -5                  | mA   |
|                                |                     |   | Only P32,<br>V <sub>DD</sub> = 3.0 V,<br>V <sub>OH</sub> = V <sub>DD</sub> -2.0 V |                      | -7              | -15                 | mA   |
|                                |                     | All pins total  |   |                      |                 | -20                 | mA   |
| Low-level output current       | I <sub>OL</sub>     | Per pin   |   |                      |                 | 15                  | mA   |
|                                |                     | All pins total  |   |                      |                 | 45                  | mA   |
| High-level input voltage       | V <sub>IH1</sub>    | Port 3  | 2.7 V ≤ V <sub>DD</sub> ≤ 6.0 V   | 0.7 V <sub>DD</sub>  |                 | V <sub>DD</sub>     | V    |
|                                |                     |   | 1.8 V ≤ V <sub>DD</sub> < 2.7 V   | 0.9 V <sub>DD</sub>  |                 | V <sub>DD</sub>     | V    |
|                                | V <sub>IH2</sub>    | Ports 6-8, KRREN,<br>RESET                                | 2.7 V ≤ V <sub>DD</sub> ≤ 6.0 V   | 0.8 V <sub>DD</sub>  |                 | V <sub>DD</sub>     | V    |
|                                |                     |   | 1.8 V ≤ V <sub>DD</sub> < 2.7 V   | 0.9 V <sub>DD</sub>  |                 | V <sub>DD</sub>     | V    |
| V <sub>IH3</sub>               | X1                  |   | V <sub>DD</sub> -0.1  |                      | V <sub>DD</sub> | V                   |      |
| Low-level input voltage        | V <sub>IL1</sub>    | Port 3  | 2.7 V ≤ V <sub>DD</sub> ≤ 6.0 V   | 0                    |                 | 0.3 V <sub>DD</sub> | V    |
|                                |                     |   | 1.8 V ≤ V <sub>DD</sub> < 2.7 V   | 0                    |                 | 0.1 V <sub>DD</sub> | V    |
|                                | V <sub>IL2</sub>    | Ports 6-8, KRREN,<br>RESET                                | 2.7 V ≤ V <sub>DD</sub> ≤ 6.0 V   | 0                    |                 | 0.2 V <sub>DD</sub> | V    |
|                                |                     |   | 1.8 V ≤ V <sub>DD</sub> < 2.7 V   | 0                    |                 | 0.1 V <sub>DD</sub> | V    |
| V <sub>IL3</sub>               | X1                  |   | 0   |                      | 0.1             | V                   |      |
| High-level output voltage      | V <sub>OH</sub>     | V <sub>DD</sub> = 4.5 to 6.0 V, I <sub>OH</sub> = -1.0 mA |   | V <sub>DD</sub> -1.0 |                 |                     | V    |
|                                |                     | V <sub>DD</sub> = 1.8 to 6.0 V, I <sub>OH</sub> = -100 μA |   | V <sub>DD</sub> -0.5 |                 |                     | V    |
| Low-level output voltage       | V <sub>OL</sub>     | V <sub>DD</sub> = 4.5 to 6.0 V                            | Port 3, I <sub>OL</sub> = 15 mA   |                      | 0.6             | 2.0                 | V    |
|                                |                     |   | Ports 6, 8,<br>I <sub>OL</sub> = 1.6 mA   |                      |                 | 0.4                 | V    |
|                                |                     | V <sub>DD</sub> = 1.8 to 6.0 V, I <sub>OL</sub> = 400 μA  |   |                      |                 |                     | 0.5  |
| High-level input leak current  | I <sub>LIH1</sub>   | V <sub>IN</sub> = V <sub>DD</sub>                         | Pins except X1  |                      |                 | 3.0                 | μA   |
|                                | I <sub>LIH2</sub>   |   | X1  |                      |                 | 20                  | μA   |
| Low-level input leak current   | I <sub>LIL1</sub>   | V <sub>IN</sub> = 0 V                                     | Pins except X1  |                      |                 | -3.0                | μA   |
|                                | I <sub>LIL2</sub>   |   | X1  |                      |                 | -20                 | μA   |
| High-level output leak current | I <sub>LOH</sub>    | V <sub>OUT</sub> = V <sub>DD</sub>                        |   |                      |                 | 3.0                 | μA   |
| Low-level output leak current  | I <sub>LOL</sub>    | V <sub>OUT</sub> = 0 V                                    |   |                      |                 | -3.0                | μA   |
| On-chip pull-up resistance     | R <sub>L1</sub>     | V <sub>IN</sub> = 0 V                                     | Ports 3, 6, 8   | 50                   | 100             | 200                 | kΩ   |
|                                |                     |   | Port 7 (mask option)  | 15                   | 30              | 60                  | kΩ   |
|                                | RESET (mask option) |   |   | 50                   | 100             | 200                 | kΩ   |
|                                |                     |   | R <sub>L2</sub>   |                      |                 |                     |      |

DC Characteristics (T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 1.8 to 6.0 V)

| Parameter                        | Symbol           | Test Conditions                |  | MIN.                           | TYP. | MAX. | Unit |    |
|----------------------------------|------------------|--------------------------------|--|--------------------------------|------|------|------|----|
| Supply current <sup>Note 1</sup> | I <sub>DD1</sub> | 4.19 MHz                       | V <sub>DD</sub> = 5.0 V ± 10 % <sup>Note 2</sup> |                                | 1.5  | 5.0  | mA   |    |
|                                  |                  | Crystal resonator              | V <sub>DD</sub> = 3.0 V ± 10 % <sup>Note 3</sup> |                                | 0.23 | 1.0  | mA   |    |
|                                  | I <sub>DD2</sub> | C1 = C2 = 22 pF                | HALT mode  | V <sub>DD</sub> = 5.0 V ± 10 % |      | 0.64 | 3.0  | mA |
|                                  |                  |                                |  | V <sub>DD</sub> = 3.0 V ± 10 % |      | 0.20 | 0.9  | mA |
|                                  | I <sub>DD3</sub> | X1 = 0 V<br>STOP mode          | V <sub>DD</sub> = 1.8 to 6.0 V                   | T <sub>A</sub> = 25 °C         |      |      | 5    | μA |
|                                  |                  |                                |  |                                |      |      | 1    | μA |
|                                  |                  |                                | V <sub>DD</sub> = 3.0 V ± 10 %                   |                                | 0.1  | 3    | μA   |    |
|                                  |                  | T <sub>A</sub> = -40 to +40 °C |  | 0.1                            | 1    | μA   |      |    |

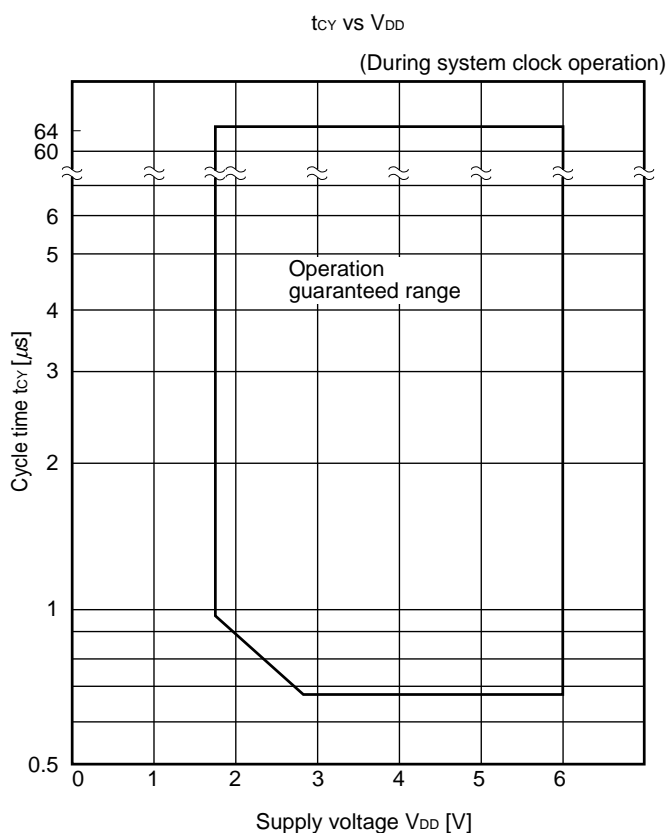
- Notes**
1. Does not include current fed to on-chip pull-up resistor.
  2. When processor clock control register (PCC) is set to 0011, during high-speed mode.
  3. When PCC is set to 0000, during low-speed mode.



AC Characteristics (T<sub>A</sub> = -40 to +85 °C, V<sub>DD</sub> = 1.8 to 6.0 V)

| Parameter  | Symbol                                | Test Conditions           | MIN.                            | TYP.          | MAX. | Unit |    |
|--|---------------------------------------|---------------------------|---------------------------------|---------------|------|------|----|
| CPU clock cycle time <sup>Note 1</sup><br>(Minimum instruction execution time = 1 machine cycle) | t <sub>cy</sub>                       | When system clock is used | 2.7 V ≤ V <sub>DD</sub> ≤ 6.0 V | 0.67          |      | 64.0 | μs |
|  |                                       |                           | 1.8 V ≤ V <sub>DD</sub> < 2.7 V | 0.95          |      | 64.0 | μs |
| Interrupt input high- and low-level widths   | t <sub>INTH</sub> , t <sub>INTL</sub> | INT0                      | IM02 = 0                        | <b>Note 2</b> |      | μs   |    |
|  |                                       |                           | IM02 = 1                        | 10            |      | μs   |    |
|  |                                       | KR4-KR7                   | 10                              |               | μs   |      |    |
| RESET low-level width  | t <sub>RSL</sub>                      |                           | 10                              |               |      | μs   |    |

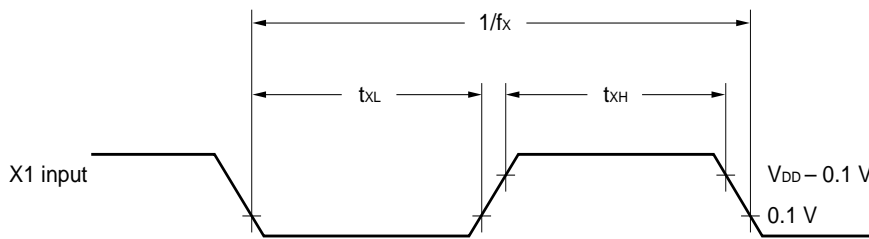
- Notes 1.** The CPU clock (Φ) cycle time (minimum instruction execution time) is determined by the oscillation frequency of the connected resonator (and external clock) and the processor clock control register (PCC). The figure on the right shows the cycle time t<sub>cy</sub> characteristics against the supply voltage V<sub>DD</sub> when the system clock is used.
- 2.** 2t<sub>cy</sub> or 128/f<sub>x</sub> depending on the setting of the interrupt mode register (IM0).



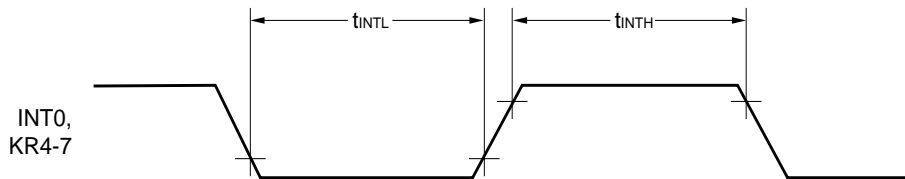
AC Timing Test Points (Excluding X1 Input)



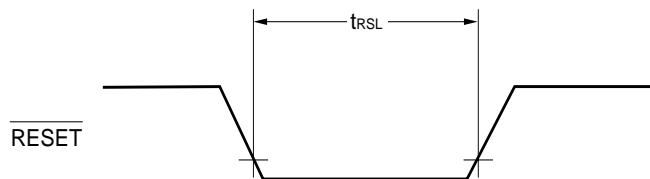
Clock Timing



Interrupt Input Timing



$\overline{RESET}$  Input Timing



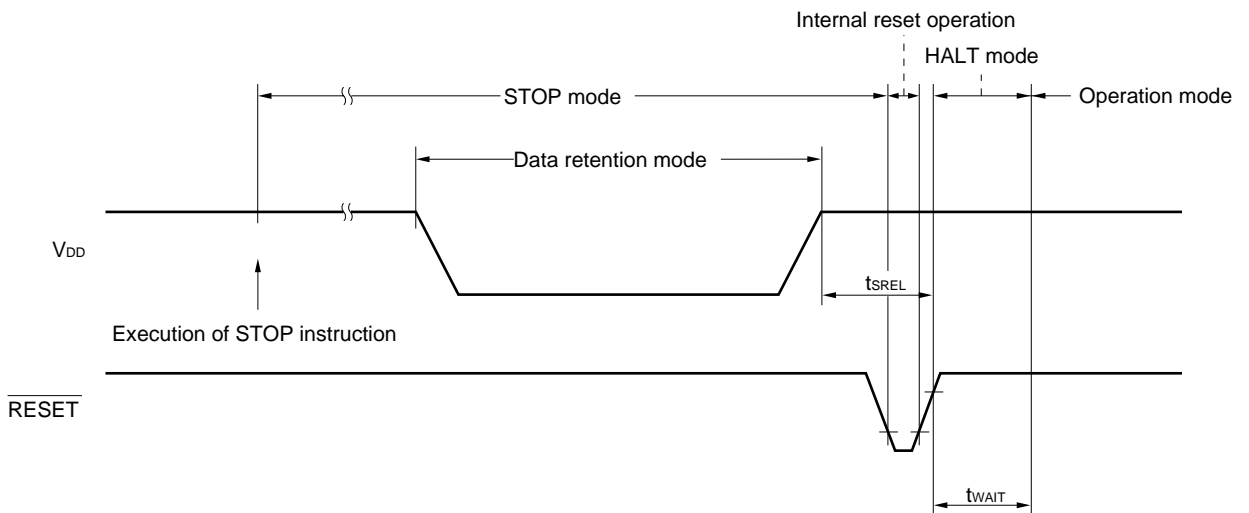
**Data Memory STOP Mode Low-Supply Voltage Data Retention Characteristics (T<sub>A</sub> = -40 to +85 °C)**

| Parameter   | Symbol            | Test Conditions                      | MIN. | TYP.          | MAX. | Unit |
|---|-------------------|--------------------------------------|------|---------------|------|------|
| Release signal set time                               | t <sub>SREL</sub> |                                      | 0    |               |      | μs   |
| Oscillation stabilization wait time <sup>Note 1</sup> | t <sub>WAIT</sub> | Release by $\overline{\text{RESET}}$ |      | <b>Note 2</b> |      | ms   |
|   |                   | Release by interrupt request         |      | <b>Note 3</b> |      | ms   |

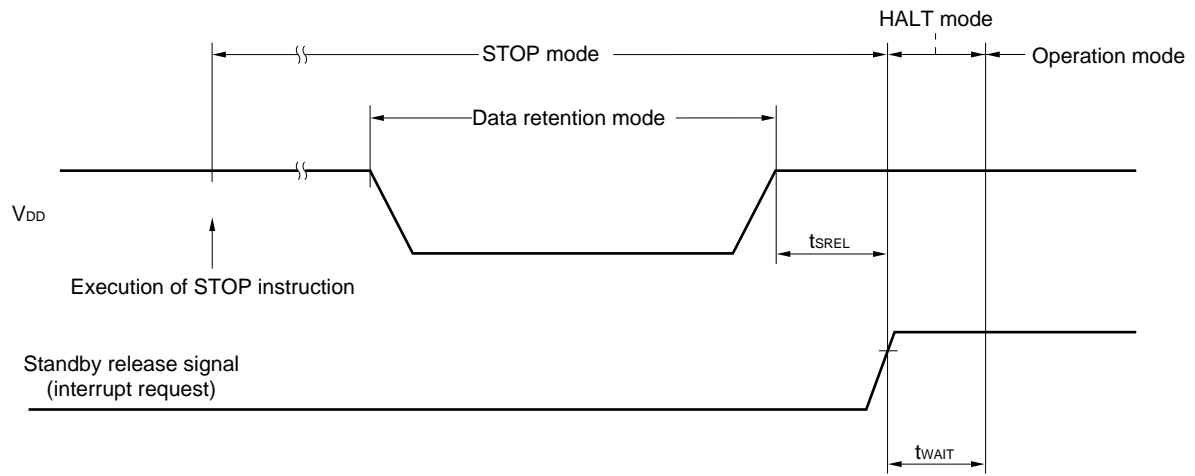
- Notes**
- The oscillation stabilization wait time is the time during which the CPU operation is stopped to avoid unstable operation at oscillation start.
  - $2^{17}/f_x$  and  $2^{15}/f_x$  can be selected with mask option.
  - Depends on setting of basic interval timer mode register (BTM) (see table below).

| BTM3 | BTM2 | BTM1 | BTM0 | Wait Time   |   |
|------|------|------|------|---|---|
|      |      |      |      | When f <sub>x</sub> = 4.19 MHz                    | When f <sub>x</sub> = 6.0 MHz                     |
| -    | 0    | 0    | 0    | 2 <sup>20</sup> /f <sub>x</sub> (Approx. 250 ms)  | 2 <sup>20</sup> /f <sub>x</sub> (Approx. 175 ms)  |
| -    | 0    | 1    | 1    | 2 <sup>17</sup> /f <sub>x</sub> (Approx. 31.3 ms) | 2 <sup>17</sup> /f <sub>x</sub> (Approx. 21.8 ms) |
| -    | 1    | 0    | 1    | 2 <sup>15</sup> /f <sub>x</sub> (Approx. 7.81 ms) | 2 <sup>15</sup> /f <sub>x</sub> (Approx. 5.46 ms) |
| -    | 1    | 1    | 1    | 2 <sup>13</sup> /f <sub>x</sub> (Approx. 1.95 ms) | 2 <sup>13</sup> /f <sub>x</sub> (Approx. 1.37 ms) |

**Data Retention Timing (on releasing STOP mode by  $\overline{\text{RESET}}$ )**



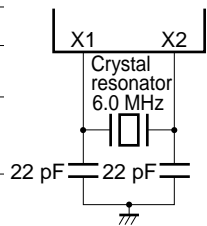
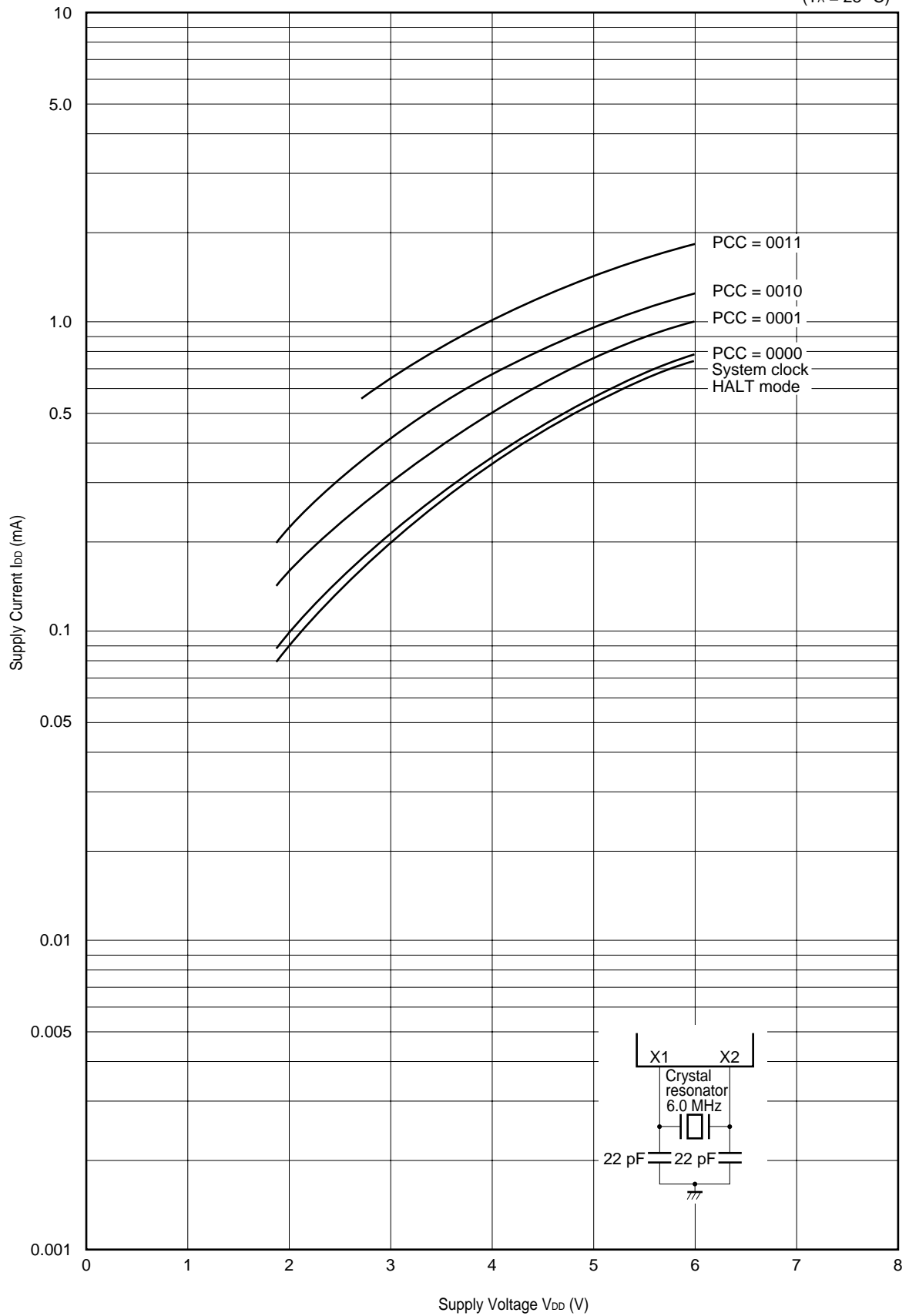
Data Retention Timing (Standby release signal: on releasing STOP mode by interrupt signal)



13. CHARACTERISTIC CURVES (REFERENCE VALUES)

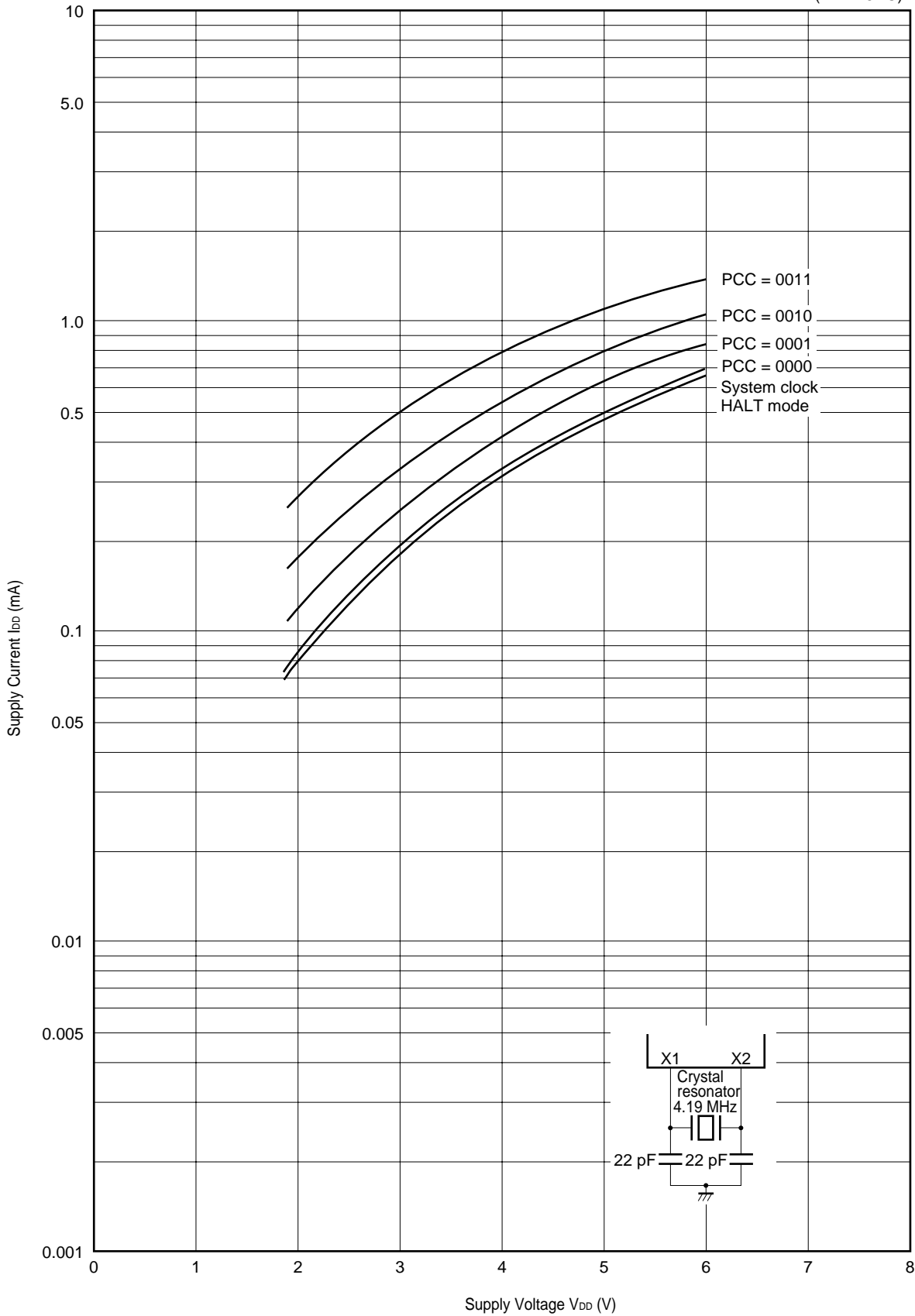
$I_{DD}$  vs  $V_{DD}$  (System clock: 6.0-MHz crystal resonator)

( $T_A = 25^\circ\text{C}$ )



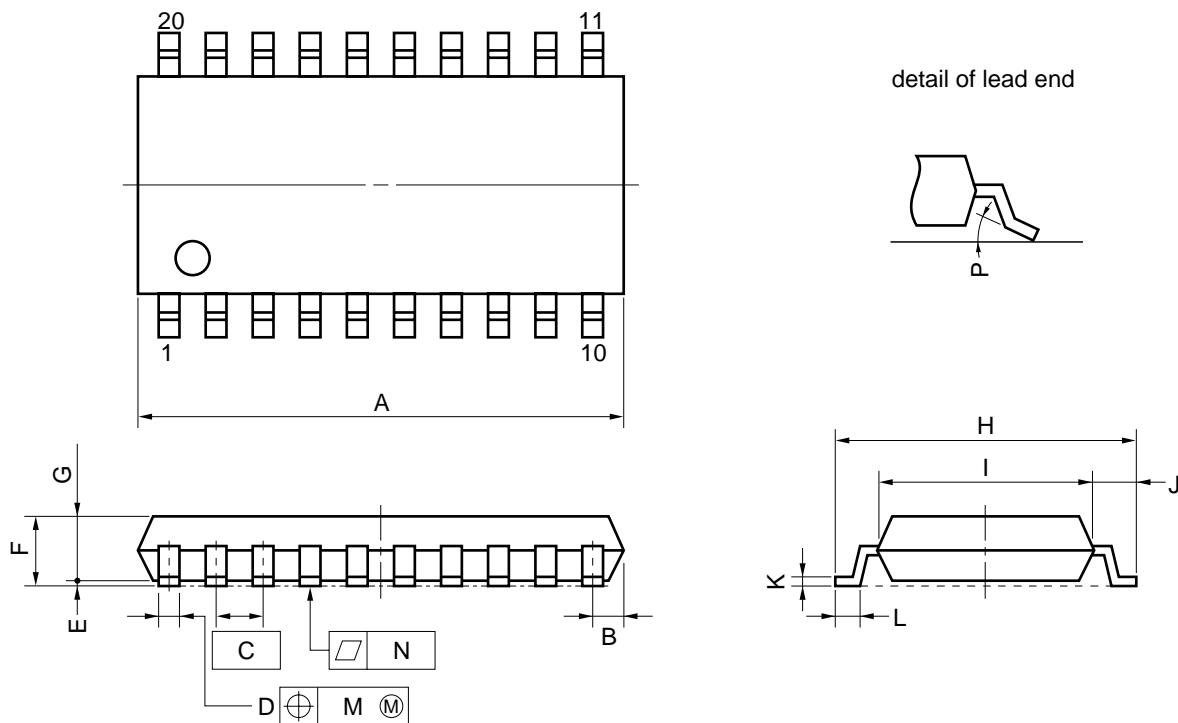
I<sub>DD</sub> vs V<sub>DD</sub> (System clock: 4.19-MHz crystal resonator)

(T<sub>A</sub> = 25 °C)



14. PACKAGE DRAWINGS

20 PIN PLASTIC SOP (300 mil)



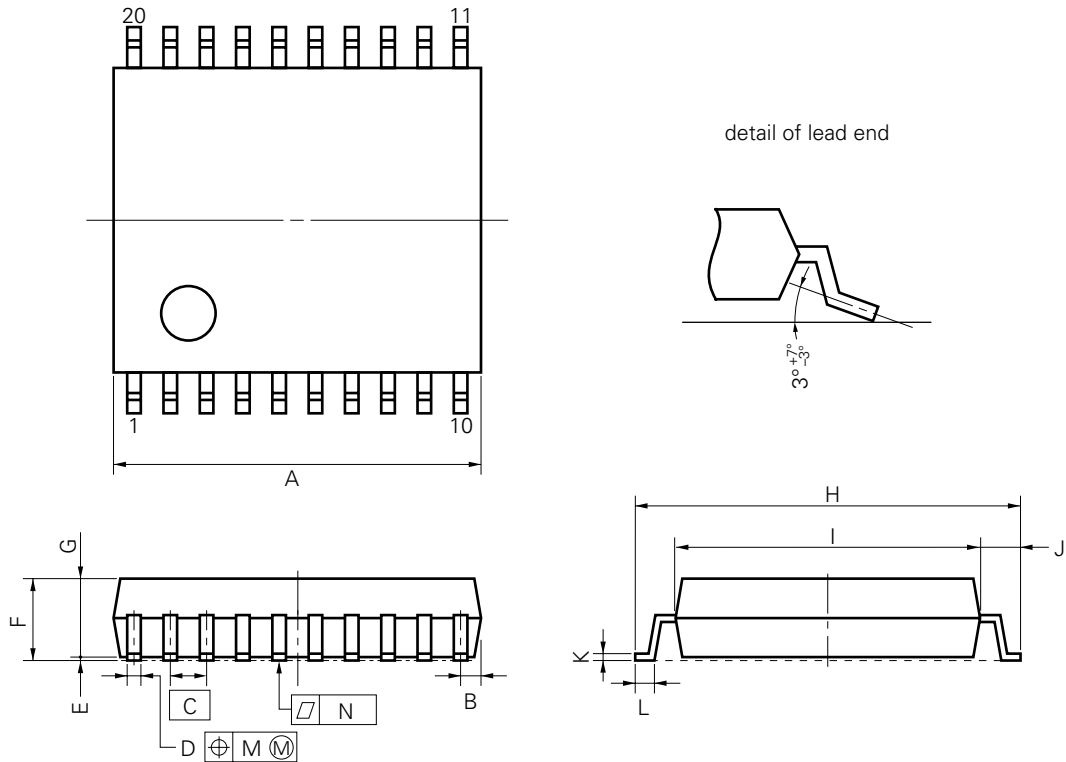
**NOTE**

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS                            | INCHES                                    |
|------|--|---|
| A    | 13.00 MAX.                             | 0.512 MAX.                                |
| B    | 0.78 MAX.                              | 0.031 MAX.                                |
| C    | 1.27 (T.P.)                            | 0.050 (T.P.)                              |
| D    | 0.40 <sup>+0.10</sup> <sub>-0.05</sub> | 0.016 <sup>+0.004</sup> <sub>-0.003</sub> |
| E    | 0.1±0.1                                | 0.004±0.004                               |
| F    | 1.8 MAX.                               | 0.071 MAX.                                |
| G    | 1.55                                   | 0.061                                     |
| H    | 7.7±0.3                                | 0.303±0.012                               |
| I    | 5.6                                    | 0.220                                     |
| J    | 1.1                                    | 0.043                                     |
| K    | 0.20 <sup>+0.10</sup> <sub>-0.05</sub> | 0.008 <sup>+0.004</sup> <sub>-0.002</sub> |
| L    | 0.6±0.2                                | 0.024 <sup>+0.008</sup> <sub>-0.009</sub> |
| M    | 0.12                                   | 0.005                                     |
| N    | 0.10                                   | 0.004                                     |
| P    | 3° <sup>+7°</sup> <sub>-3°</sub>       | 3° <sup>+7°</sup> <sub>-3°</sub>          |

P20GM-50-300B, C-4

20 PIN PLASTIC SHRINK SOP (300 mil)



**NOTE**

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

P20GM-65-300B-2

| ITEM | MILLIMETERS                            | INCHES                                    |
|------|--|---|
| A    | 7.00 MAX.                              | 0.276 MAX.                                |
| B    | 0.575 MAX.                             | 0.023 MAX.                                |
| C    | 0.65 (T.P.)                            | 0.026 (T.P.)                              |
| D    | 0.30±0.10                              | 0.012 <sup>+0.004</sup> <sub>-0.005</sub> |
| E    | 0.125±0.075                            | 0.005±0.003                               |
| F    | 2.0 MAX.                               | 0.079 MAX.                                |
| G    | 1.7                                    | 0.067                                     |
| H    | 8.1±0.3                                | 0.319±0.012                               |
| I    | 6.1±0.2                                | 0.240±0.008                               |
| J    | 1.0±0.2                                | 0.039 <sup>+0.009</sup> <sub>-0.008</sub> |
| K    | 0.15 <sup>+0.10</sup> <sub>-0.05</sub> | 0.006 <sup>+0.004</sup> <sub>-0.002</sub> |
| L    | 0.5±0.2                                | 0.020 <sup>+0.008</sup> <sub>-0.009</sub> |
| M    | 0.12                                   | 0.005                                     |
| N    | 0.10                                   | 0.004                                     |



**15. RECOMMENDED SOLDERING CONDITIONS**

The μPD754202 should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

**Table 15-1. Surface Mounting Type Soldering Conditions**

- μPD754202GS-xxx-BA5 : 20-pin plastic SOP (300 mil, 1.27-mm pitch)
- μPD754202GS-xxx-GJG : 20-pin plastic shrink SOP (300 mil, 0.65-mm pitch)
- μPD754202GS(A)-xxx-BA5 : 20-pin plastic SOP (300 mil, 1.27-mm pitch)
- μPD754202GS(A)-xxx-GJG : 20-pin plastic shrink SOP (300 mil, 0.65-mm pitch)

| Soldering Method | Soldering Conditions  | Symbol    |
|------------------|---|-----------|
| Infrared reflow  | Package peak temperature: 235 °C, Reflow time: 30 seconds or below (at 210 °C or higher), Number of reflow processes: Twice or less                                       | IR35-00-2 |
| VPS              | Package peak temperature: 215 °C, Reflow time: 40 seconds or below (at 200 °C or higher), Number of reflow processes: Twice or less                                       | VP15-00-2 |
| Wave soldering   | Solder temperature: 260 °C or below, Flow time: 10 seconds or below, Number of flow processes: 1<br>Preheating temperature: 120 °C or below (package surface temperature) | WS60-00-1 |
| Partial heating  | Pin temperature: 300 °C or below, Time: 3 seconds or below (per side of device)   | —         |

**Caution Do not use different soldering methods together (except for partial heating).**

APPENDIX A. μPD754202, 75F4264 FUNCTION LIST

| Item                          |                   | μPD754202   | μPD75F4264 <sup>Note</sup>   |
|-------------------------------|-------------------|---|--|
| Program memory                |                   | Mask ROM<br>0000H-07FFH<br>(2048 × 8 bits)  | Flash memory<br>0000H-0FFFH<br>(4096 × 8 bits)   |
| Data memory                   | Static RAM        | 000H-07FH (128 × 4 bits)  |  |
|                               | EEPROM™           | None  | 400H-43FH (32 × 8 bits)  |
| CPU                           |                   | 75XL CPU  |  |
| General-purpose register      |                   | (4 bits × 8 or 8 bits × 4) × 4 banks  |  |
| Instruction execution time    |                   | <ul style="list-style-type: none"> <li>• 0.95, 1.91, 3.81, 15.3 μs (system clock: at 4.19-MHz operation)</li> <li>• 0.67, 1.33, 2.67, 10.7 μs (system clock: at 6.0-MHz operation)</li> </ul>   |  |
| I/O port                      | CMOS input        | 4 (on-chip pull-up resistor can be connected by mask option)  |  |
|                               | CMOS input/output | 9 (on-chip pull-up resistor can be specified by software)   |  |
|                               | Total             | 13  |  |
| System clock oscillator       |                   | Ceramic/crystal oscillator  |  |
| Boot time after reset         |                   | 2 <sup>17</sup> /f <sub>x</sub> or 2 <sup>15</sup> /f <sub>x</sub><br>(selected by mask option)   | 2 <sup>15</sup> /f <sub>x</sub>  |
| Timer                         |                   | 4 channels <ul style="list-style-type: none"> <li>• 8-bit timer counter: 3 channels (can be used for 16-bit timer counter)</li> <li>• Basic interval timer/watchdog timer: 1 channel</li> </ul> |  |
| A/D converter                 |                   | None  | <ul style="list-style-type: none"> <li>• 8-bit resolution × 2 channels (successive approximation register)</li> <li>• Operable V<sub>DD</sub> = 1.8 V or higher</li> </ul> |
| Programmable threshold port   |                   | None  | 2 channels   |
| Vectored interrupt            |                   | External: 1, Internal: 4  | External: 1, Internal: 5   |
| Test input                    |                   | External: 1 (key return reset function provided)  |  |
| Supply voltage                |                   | V <sub>DD</sub> = 1.8 to 6.0 V  |  |
| Operating ambient temperature |                   | T <sub>A</sub> = -40 to +85 °C  |  |
| Package                       |                   | <ul style="list-style-type: none"> <li>• 20-pin plastic SOP (300 mil, 1.27-mm pitch)</li> <li>• 20-pin plastic shrink SOP (300 mil, 0.65-mm pitch)</li> </ul>                                   | <ul style="list-style-type: none"> <li>• 20-pin plastic SOP (300 mil, 1.27-mm pitch)</li> </ul>  |

**Note** Under development

**APPENDIX B. DEVELOPMENT TOOLS**

The following development tools are provided for system development using the μPD754202.

In the 75XL Series, the relocatable assembler which is common to the series is used in combination with the device file of each product.

**Language processor**

| RA75X relocatable assembler                  | Host machine                | OS             | Supply media | Part number<br>(product name) |
|--|-----------------------------|----------------|--------------|-------------------------------|
|  |                             | PC-9800 Series | MS-DOS™      |                               |
| ( Ver. 3.30 to<br>Ver. 6.2 <sup>Note</sup> ) | 5-inch 2HD                  |                | μS5A10RA75X  |                               |
| IBM PC/AT™ and compatible machines           | Refer to<br>"OS for IBM PC" | 3.5-inch 2HC   | μS7B13RA75X  |                               |
|  |                             | 5-inch 2HC     | μS7B10RA75X  |                               |

| Device file                                  | Host machine                | OS             | Supply media   | Part number<br>(product name) |
|--|-----------------------------|----------------|----------------|-------------------------------|
|  |                             | PC-9800 Series | MS-DOS         |                               |
| ( Ver. 3.30 to<br>Ver. 6.2 <sup>Note</sup> ) | 5-inch 2HD                  |                | μS5A10DF754202 |                               |
| IBM PC/AT and compatible machines            | Refer to<br>"OS for IBM PC" | 3.5-inch 2HC   | μS7B13DF754202 |                               |
|  |                             | 5-inch 2HC     | μS7B10DF754202 |                               |

**Note** Ver. 5.00 or later have the task swap function, but it cannot be used for this software.

**Remark** Operations of the assembler and device file are guaranteed only on the above host machines and OSs.

**Debugging tool**

The in-circuit emulators (IE-75000-R and IE-75001-R) are available as the program debugging tool for the μPD754202.

The system configurations are described as follows.

|            |   |  |  |              |                            |
|------------|---|--|--|--------------|----------------------------|
| Hardware   | IE-75000-R <sup>Note 1</sup>                  | In-circuit emulator for debugging the hardware and software when developing application systems that use the 75X Series and 75XL Series. When developing a μPD754202, the emulation board IE-75300-R-EM and emulation probe EP-754144GS-R that are sold separately must be used with the IE-75000-R.<br>By connecting with the host machine, efficient debugging can be made.<br>It contains the emulation board IE-75000-R-EM which is connected. |  |              |                            |
|            | IE-75001-R                                    | In-circuit emulator for debugging the hardware and software when developing application systems that use the 75X Series and 75XL Series. When developing a μPD754202, the emulation board IE-75300-R-EM and emulation probe EP-754144GS-R which are sold separately must be used with the IE-75001-R.<br>By connecting with the host machine, efficient debugging can be made.   |  |              |                            |
|            | IE-75300-R-EM                                 | Emulation board for evaluating the application systems that use a μPD754202.<br>It must be used with the IE-75000-R or IE-75001-R.   |  |              |                            |
|            | EP-754144GS-R<br>EV-9500GS-20<br>EV-9501GS-20 | Emulation probe for the μPD754202.<br>It must be connected to IE-75000-R (or IE-75001-R) and IE-75300-R-EM.<br>It is supplied with the 20-pin flexible boards EV-9500GS-20 (compatible with 20-pin plastic shrink SOP) and EV-9501GS-20 (compatible with 20-pin plastic SOP) which facilitate connection to a target system.   |  |              |                            |
| Software   | IE control program                            | Connects the IE-75000-R or IE-75001-R to a host machine via RS-232-C and Centronics I/F and controls the IE-75000-R or IE-75001-R on a host machine.   |  |              |                            |
|            |   | Host machine   | OS   | Supply media | Part number (product name) |
|            |   | PC-9800 Series   | MS-DOS<br>(Ver. 3.30 to Ver. 6.2 <sup>Note 2</sup> ) | 3.5-inch 2HD | μS5A13IE75X                |
|            |   |  |  | 5-inch 2HD   | μS5A10IE75X                |
|            |   | IBM PC/AT and compatible machines  | Refer to "OS for IBM PC"                             | 3.5-inch 2HC | μS7B13IE75X                |
| 5-inch 2HC | μS7B10IE75X                                   |  |  |              |                            |

**Notes 1.** Maintenance product

**2.** Ver. 5.00 or later have the task swap function, but it cannot be used for this software.

**Remark** Operation of the IE control program is guaranteed only on the above host machines and OSs.

**OS for IBM PC**

The following IBM PC OS's are supported.

| OS       | Version   |
|----------|---|
| PC DOS™  | Ver. 5.02 to Ver. 6.3<br>J6.1/V <sup>Note</sup> to J6.3/V <sup>Note</sup> |
| MS-DOS   | Ver. 5.0 to Ver. 6.22<br>5.0/V <sup>Note</sup> to J6.2/V <sup>Note</sup>  |
| IBM DOS™ | J5.02/V <sup>Note</sup>   |

**Note** Only English mode is supported.

**Caution** Ver. 5.0 or later have the task swap function, but it cannot be used for this software.

**APPENDIX C. RELATED DOCUMENTS**

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

**Device related documents**

| Document Name                   | Document Number |               |
|---------------------------------|-----------------|---------------|
|                                 | Japanese        | English       |
| μPD754202, 754202(A) Data Sheet | U12181J         | This document |
| μPD754202 User's Manual         | U11132J         | U11132E       |
| 75XL Series Selection Guide     | U10453J         | U10453E       |

**Development tool related documents**

| Document Name |                                       | Document Number |         |          |
|---------------|---------------------------------------|-----------------|---------|----------|
|               |                                       | Japanese        | English |          |
| Hardware      | IE-75000-R/IE-75001-R User's Manual   |                 | EEU-846 | EEU-1416 |
|               | IE-75300-R-EM User's Manual           |                 | U11354J | U11354E  |
|               | EP-754144GS-R User's Manual           |                 | U10695J | U10695E  |
| Software      | RA75X Assembler Package User's Manual | Operation       | EEU-731 | EEU-1346 |
|               |                                       | Language        | EEU-730 | EEU-1363 |

**Other related documents**

| Document Name   | Document Number |          |
|---|-----------------|----------|
|   | Japanese        | English  |
| IC Package Manual   | C10943X         |          |
| Semiconductor Device Mounting Technology Manual             | C10535J         | C10535E  |
| Quality Grades on NEC Semiconductor Devices                 | C11531J         | C11531E  |
| NEC Semiconductor Device Reliability/Quality Control System | C10983J         | C10983E  |
| Electrostatic Discharge (ESD) Test                          | MEM-539         | –        |
| Guide to Quality Assurance for Semiconductor Devices        | C11893J         | MEI-1202 |
| Microcomputer Product Series Guide                          | U11416J         | –        |

**Caution** These documents are subject to change without notice. Be sure to read the latest documents for designing, etc.

[MEMO]

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

**Note:** Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

**Note:** No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

**Note:** Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.



## Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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NEC devices are classified into the following three quality grades:

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Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

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Anti-radioactive design is not implemented in this product.