NEC

MOS INTEGRATED CIRCUIT

# μPD753012A, 753016A, 753017A

## 4-BIT SINGLE-CHIP MICROCONTROLLER

### DESCRIPTION

The μPD753017A is one of the 75XL series 4-bit single-chip microcontroller chips and has a data processing capability comparable to that of an 8-bit microcontroller.

It has an on-chip LCD controller/driver with a larger ROM capacity and extended CPU functions compared with the conventional μPD75316B, and can provide high-speed operation at a low supply voltage of 1.8 V. It can be supplied in a small plastic TQFP package (12 × 12 mm) and is suitable for small sets using LCD panels.

**Detailed descriptions of functions are provided in the following document. Be sure to read the document before designing.**

**μPD753017 User's Manual : U11282E**

### FEATURES

- Low voltage operation: $V_{DD}$ = 1.8 to 5.5 V
  - Can be driven by two 1.5 V batteries
- On-chip memory
  - Program memory (ROM):
    12288 × 8 bits (μPD753012A)
    16384 × 8 bits (μPD753016A)
    24576 × 8 bits (μPD753017A)
  - Data memory (RAM):
    1024 × 4 bits
- Capable of high-speed operation and variable instruction execution time for power saving
  - 0.95, 1.91, 3.81, 15.3 μs (at 4.19 MHz operation)
  - 0.67, 1.33, 2.67, 10.7 μs (at 6.0 MHz operation)
  - 122 μs (at 32.768 kHz operation)
- Internal programmable LCD controller/driver
- Small plastic TQFP (12 × 12 mm)
  - Suitable for small sets such as cameras
- One-time PROM: μPD75P3018A

### APPLICATION

Remote controllers, camera-integrated VCRs, cameras, gas meters, etc.

**In this document, unless otherwise specified, the description is made based on μPD753017A as typical product.**



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**The mark ★ shows major revised points.**

## ORDERING INFORMATION

| | Part number | Package |
|---|---|---|
| | μPD753012AGC-XXX-3B9 | 80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm) |
| ★ | μPD753012AGC-XXX-8BT | 80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm) |
| | μPD753012AGK-XXX-BE9 | 80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.05 mm) |
| ★ | μPD753012AGK-XXX-9EU | 80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.00 mm) |
| | μPD753016AGC-XXX-3B9 | 80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm) |
| ★ | μPD753016AGC-XXX-8BT | 80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm) |
| | μPD753016AGK-XXX-BE9 | 80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.05 mm) |
| ★ | μPD753016AGK-XXX-9EU | 80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.00 mm) |
| | μPD753017AGC-XXX-3B9 | 80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm) |
| ★ | μPD753017AGC-XXX-8BT | 80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm) |
| | μPD753017AGK-XXX-BE9 | 80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.05 mm) |
| ★ | μPD753017AGK-XXX-9EU | 80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.00 mm) |

**Remark** XXX indicates ROM code suffix.

## FUNCTION OUTLINE

| Parameter | | | Function |
|---|---|---|---|
| Instruction execution time | | | • 0.95, 1.91, 3.81, 15.3 μs (main system clock: at 4.19 MHz operation)<br>• 0.67, 1.33, 2.67, 10.7 μs (main system clock: at 6.0 MHz operation)<br>• 122 μs (subsystem clock: at 32.768 kHz operation) |
| Internal memory | ROM | | 12288 × 8 bits (μPD753012A) |
| | | | 16384 × 8 bits (μPD753016A) |
| | | | 24576 × 8 bits (μPD753017A) |
| | RAM | | 1024 × 4 bits |
| General purpose register | | | • 4-bit operation: 8 × 4 banks<br>• 8-bit operation: 4 × 4 banks |
| Input/output port | CMOS input | 8 | On-chip pull-up resistors can be specified by using software: 23 |
| | CMOS input/output | 16 | |
| | CMOS output | 8 | Also used for segment pins |
| | N-ch open-drain input/output | 8 | Withstands 13 V, on-chip pull-up resistors can be specified by using mask option |
| | Total | 40 | |
| LCD controller/driver | | | • Segment number selection : 24/28/32 segments (can be changed to CMOS output port in 4 time-unit; max. 8)<br>• Display mode selection : Static, 1/2 duty (1/2 bias), 1/3 duty (1/2 bias), 1/3 duty (1/3 bias), 1/4 duty (1/3 bias) |
| | | | On-chip split resistor for LCD drive can be specified by using mask option |
| Timer | | | 5 channels<br>• 8-bit timer/event counter: 3 channels (can be used for 16-bit timer/event counter, carrier generator, timer with gate)<br>• Basic interval timer/watchdog timer: 1 channel<br>• Watch timer: 1 channel |
| Serial interface | | | • 3-wire serial I/O mode ... MSB or LSB can be selected for transferring first bit<br>• 2-wire serial I/O mode<br>• SBI mode |
| Bit sequential buffer | | | 16 bits |
| Clock output (PCL) | | | • Φ, 524, 262, 65.5 kHz (main system clock: at 4.19 MHz operation)<br>• Φ, 750, 375, 93.8 kHz (main system clock: at 6.0 MHz operation) |
| Buzzer output (BUZ) | | | • 2, 4, 32 kHz (main system clock: at 4.19 MHz operation or subsystem clock: at 32.768 kHz operation)<br>• 2.93, 5.86, 46.9 kHz (main system clock: at 6.0 MHz operation) |
| Vectored interrupt | | | External: 3, Internal: 5 |
| Test input | | | External: 1, Internal: 1 |
| System clock oscillator | | | • Ceramic or crystal oscillator for main system clock oscillation<br>• Crystal oscillator for subsystem clock oscillation |
| Standby function | | | STOP/HALT mode |
| Power supply voltage | | | $V_{DD}$ = 1.8 to 5.5 V |
| Package | | | • 80-pin plastic QFP (14 × 14 mm)<br>• 80-pin plastic TQFP (fine pitch) (12 × 12 mm) |

CONTENTS

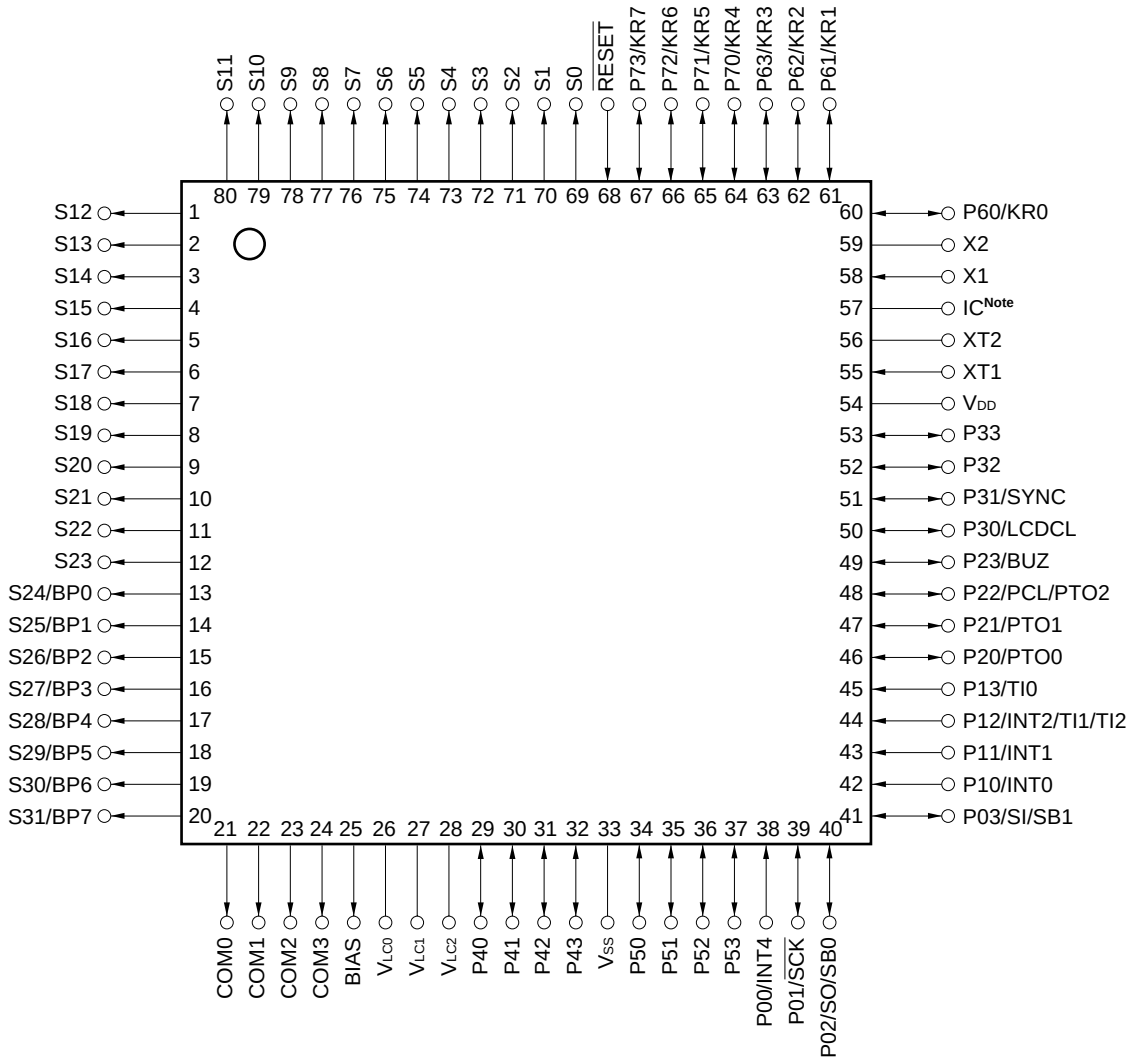
## 1. PIN CONFIGURATION (Top View)

- 80-pin plastic QFP (14 × 14 mm)

★ μPD753012AGC-XXX-3B9, 753012AGC-XXX-8BT, 753016AGC-XXX-3B9, 753016AGC-XXX-8BT
μPD753017AGC-XXX-3B9, 753017AGC-XXX-8BT

- 80-pin plastic TQFP (fine pitch) (12 × 12 mm)

★ μPD753012AGK-XXX-BE9, 753012AGK-XXX-9EU, 753016AGK-XXX-BE9, 753016AGK-XXX-9EU
μPD753017AGK-XXX-BE9, 753017AGK-XXX-9EU

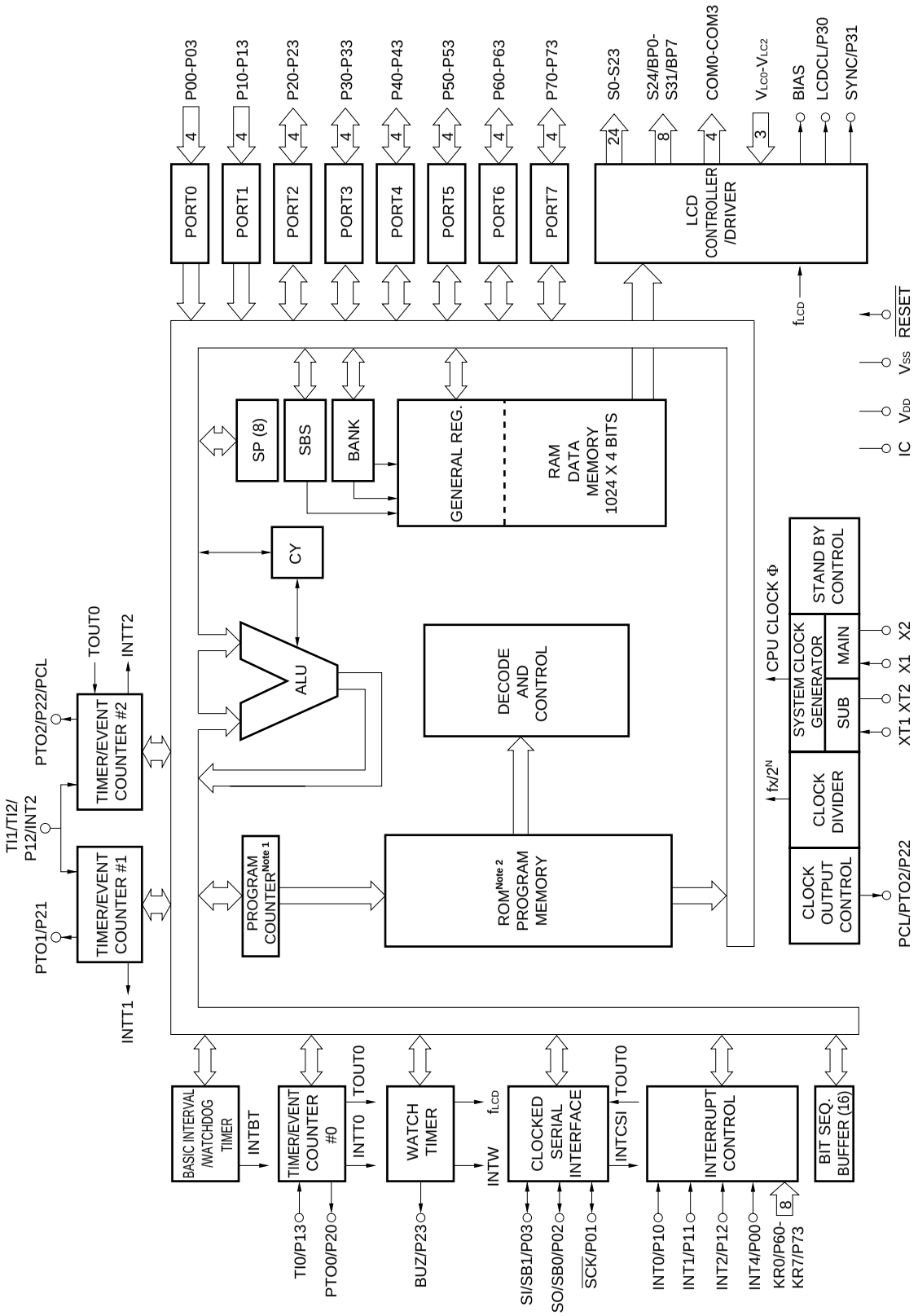



**Note** Connect the IC (Internally Connected) pin directly to $V_{DD}$.

**Pin Identification**

| | | | |
|---|---|---|---|
| BIAS | : LCD Power Supply Bias Control | PCL | : Programmable Clock |
| BP0-BP7 | : Bit Port | PTO0-PTO2 | : Programmable Timer Output 0-2 |
| BUZ | : Buzzer Clock | $\overline{\text{RESET}}$ | : Reset Input |
| COM0-COM3 | : Common Output 0-3 | S0-S31 | : Segment Output 0-31 |
| IC | : Internally Connected | SB0, SB1 | : Serial Bus 0, 1 |
| INT0, INT1, INT4 | : External Vectored Interrupt 0, 1, 4 | $\overline{\text{SCK}}$ | : Serial Clock |
| INT2 | : External Test Input 2 | SI | : Serial Input |
| KR0-KR7 | : Key Return | SO | : Serial Output |
| LCDCL | : LCD Clock | SYNC | : LCD Synchronization |
| P00-P03 | : Port 0 | TI0-TI2 | : Timer Input 0-2 |
| P10-P13 | : Port 1 | $V_{DD}$ | : Positive Power Supply |
| P20-P23 | : Port 2 | $V_{LC0}$-$V_{LC2}$ | : LCD Power Supply 0-2 |
| P30-P33 | : Port 3 | $V_{SS}$ | : Ground |
| P40-P43 | : Port 4 | X1, X2 | : Main System Clock Oscillation 1, 2 |
| P50-P53 | : Port 5 | XT1, XT2 | : Subsystem Clock Oscillation 1, 2 |
| P60-P63 | : Port 6 | | |
| P70-P73 | : Port 7 | | |

## 2. BLOCK DIAGRAM




**Notes 1.** μPD753012A and 753016A have a 14-bit configuration, and μPD753017A has a 15-bit configuration.

**2.** Capacity of the ROM depends on the product.

## 3. PIN FUNCTION

### 3.1 Port Pins (1/2)

| Pin Name | I/O | Alternate Function | Function | 8-bit I/O | After Reset | I/O Circuit Type[Note 1] |
|---|---|---|---|---|---|---|
| P00 | Input | INT4 | 4-bit input port (PORT0).<br>For P01 to P03, connection of on-chip pull-up resistors can be specified by software in 3-bit units. | No | Input | <B> |
| ★ P01 | | $\overline{SCK}$ | | | | <F>-A |
| ★ P02 | | SO/SB0 | | | | <F>-B |
| ★ P03 | | SI/SB1 | | | | <M>-C |
| P10 | Input | INT0 | 4-bit input port (PORT1).<br>Connection of on-chip pull-up resistors can be specified by software in 4-bit units.<br>Only P10/INT0 can select noise elimination circuit. | No | input | <B>-C |
| P11 | | INT1 | | | | |
| P12 | | TI1/TI2/INT2 | | | | |
| P13 | | TI0 | | | | |
| P20 | I/O | PTO0 | 4-bit input/output port (PORT2).<br>Connection of on-chip pull-up resistors can be specified by software in 4-bit units. | No | Input | E-B |
| P21 | | PTO1 | | | | |
| P22 | | PCL/PTO2 | | | | |
| P23 | | BUZ | | | | |
| P30 | I/O | LCDCL | Programmable 4-bit input/output port (PORT3).<br>This port can be specified for input/output bit-wise.<br>Connection of on-chip pull-up resistor can be specified by software in 4-bit units. | No | Input | E-B |
| P31 | | SYNC | | | | |
| P32 | | – | | | | |
| P33 | | – | | | | |
| P40-P43[Note 2] | I/O | – | N-ch open-drain 4-bit input/output port (PORT4).<br>A pull-up resistor can be contained bit-wise (mask option).<br>Withstand voltage is 13 V in open-drain mode. | Yes | High level (when pull-up resistors are provided) or high impedance | M-D |
| P50-P53[Note 2] | I/O | – | N-ch open-drain 4-bit input/output port (PORT5).<br>A pull-up resistor can be contained bit-wise (mask option).<br>Withstand voltage is 13 V in open-drain mode. | | High level (when pull-up resistors are provided) or high impedance | M-D |

**Notes 1.** Circuit types enclosed in brackets indicate the Schmitt trigger input.

**2.** If on-chip pull-up resistors are not specified by mask option (when used as N-ch open-drain input port), low level input leakage current increases when input or bit manipulation instruction is executed.

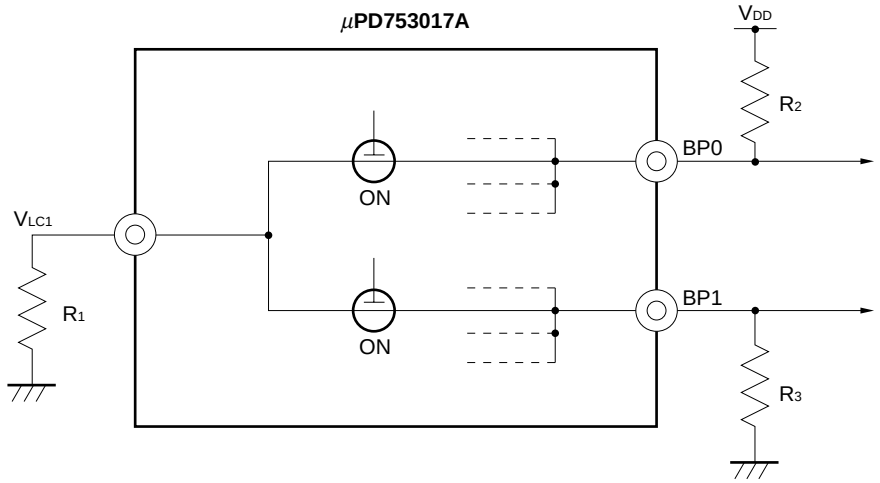
### 3.1 Port Pins (2/2)

| Pin Name | I/O | Alternate Function | Function | 8-bit I/O | After Reset | I/O Circuit Type[Note 1] |
|---|---|---|---|---|---|---|
| P60 | I/O | KR0 | Programmable 4-bit input/output port (PORT6). This port can be specified for input/output bit-wise. Connection of on-chip pull-up resistors can be specified by software in 4-bit units. | Yes | Input | <F>-A |
| P61 | | KR1 | | | | |
| P62 | | KR2 | | | | |
| P63 | | KR3 | | | | |
| P70 | I/O | KR4 | 4-bit input/output port (PORT7). Connection of on-chip pull-up resistors can be specified by software in 4-bit units. | | Input | <F>-A |
| P71 | | KR5 | | | | |
| P72 | | KR6 | | | | |
| P73 | | KR7 | | | | |
| BP0 | Output | S24 | 1-bit output port (BIT PORT). Also used for segment output pins. | No | **Note 2** | H-A |
| BP1 | | S25 | | | | |
| BP2 | | S26 | | | | |
| BP3 | | S27 | | | | |
| BP4 | Output | S28 | | | | |
| BP5 | | S29 | | | | |
| BP6 | | S30 | | | | |
| BP7 | | S31 | | | | |

**Notes 1.** Circuit types enclosed in brackets indicate the Schmitt trigger input.

**2.** BP0 through BP7 select $V_{LC1}$ as an input source.
However, the output levels change depending on the external circuit of BP0 through BP7 and $V_{LC1}$.

**Example** Because BP0 through BP7 are mutually connected inside the μPD753017A, the output levels of BP0 through BP7 are determined by $R_1$, $R_2$, and $R_3$.



### 3.2 Non-port Pins (1/2)

| Pin Name | I/O | Alternate Function | Function | | After Reset | I/O Circuit Type[Note 1] |
|---|---|---|---|---|---|---|
| TI0 | Input | P13 | Inputs external event pulses to the timer/event counter. | | Input | <B>-C |
| TI1 | | P12/INT2 | | | | |
| TI2 | | | | | | |
| PTO0 | Output | P20 | Timer/event counter output | | Input | E-B |
| PTO1 | | P21 | | | | |
| PTO2 | | P22/PCL | | | | |
| PCL | | P22/PTO2 | Clock output | | | |
| BUZ | | P23 | Optional frequency output (for buzzer output or system clock trimming) | | | |
| $\overline{SCK}$ | I/O | P01 | Serial clock input/output | | Input | <F>-A |
| SO/SB0 | | P02 | Serial data output<br>Serial data bus input/output | | | <F>-B |
| SI/SB1 | | P03 | Serial data input<br>Serial data bus input/output | | | <M>-C |
| INT4 | Input | P00 | Edge detection vectored interrupt input (both rising edge and falling edge detection) | | Input | <B> |
| INT0 | Input | P10 | Edge detection vectored interrupt input (detection edge can be selected)<br>INT0/P10 can select noise elimination circuit. | Noise elimination circuit/asynchronous selection | Input | <B>-C |
| INT1 | | P11 | | Asynchronous | | |
| INT2 | Input | P12/TI1/TI2 | Rising edge detection testable input | Asynchronous | Input | <B>-C |
| KR0-KR3 | Input | P60-P63 | Falling edge detection testable input | | Input | <F>-A |
| KR4-KR7 | Input | P70-P73 | Falling edge detection testable input | | Input | <F>-A |
| S0-S23 | Output | – | Segment signal output | | **Note 2** | G-A |
| S24-S31 | Output | BP0-BP7 | Segment signal output | | **Note 2** | H-A |
| COM0-COM3 | Output | – | Common signal output | | **Note 2** | G-B |
| $V_{LC0}$-$V_{LC2}$ | – | – | LCD drive power<br>On-chip split resistor is enable (mask option). | | – | – |
| BIAS | Output | – | Output for external split resistor disconnect | | **Note 3** | – |
| LCDCL[Note 4] | Output | P30 | Clock output for externally expanded driver | | Input | E-B |
| SYNC[Note 4] | Output | P31 | Clock output for externally expanded driver synchronization | | Input | E-B |

**Notes 1.** Circuit types enclosed in brackets indicate the Schmitt trigger input.

**2.** Each display output selects the following $V_{LCX}$ as input source.
S0-S31: $V_{LC1}$, COM0-COM2: $V_{LC2}$, COM3: $V_{LC0}$

**3.** When a split resistor is contained ..... Low level
When no split resistor is contained ..... High impedance

**4.** These pins are provided for future system expansion. At present, these pins are used only as pins P30 and P31.

### 3.2 Non-port Pins (2/2)

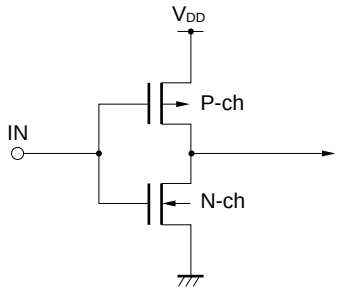
| Pin Name | I/O | Alternate Function | Function | After Reset | I/O Circuit Type[Note] |
|---|---|---|---|---|---|
| X1 | Input | – | Crystal/ceramic connection pin for the mainsystem clock oscillation. When inputting the external clock, input the external clock to pin X1, and the inverted phase of the external clock to pin X2. | – | – |
| X2 | – | – | | | |
| XT1 | Input | – | Crystal connection pin for the subsystem clock oscillation. When the external clock is used, input the external clock to pin XT1, and the inverted phase of the external clock to pin XT2. Pin XT1 can be used as a 1-bit input (test) pin. | – | – |
| XT2 | – | | | | |
| $\overline{\text{RESET}}$ | Input | – | System reset input (low level active) | – | <B> |
| IC | – | – | Internally connected. Connect directly to $V_{DD}$. | – | – |
| $V_{DD}$ | – | – | Positive power supply | – | – |
| $V_{SS}$ | – | – | GND | – | – |

**Note** Circuit types enclosed in brackets indicate the Schmitt trigger input.

### 3.3 Pin Input/Output Circuits

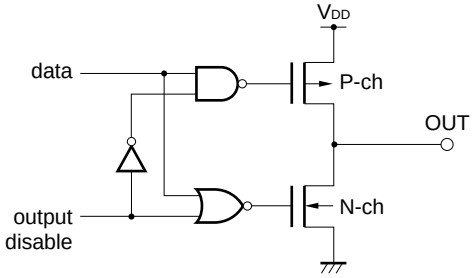
The μPD753017A pin input/output circuits are shown schematically.

TYPE A



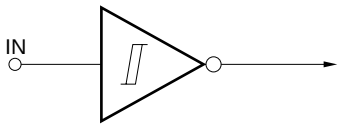

CMOS standard input buffer

TYPE D



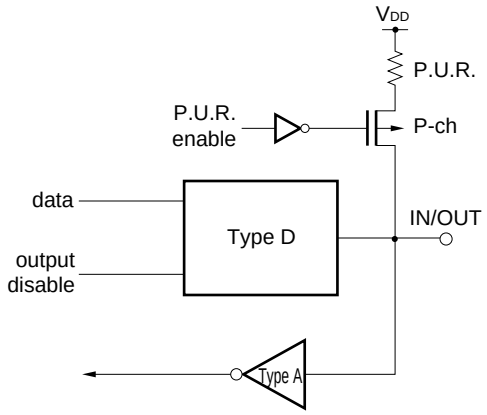

Push-pull output that can be placed in output high impedance (both P-ch and N-ch off).

TYPE B



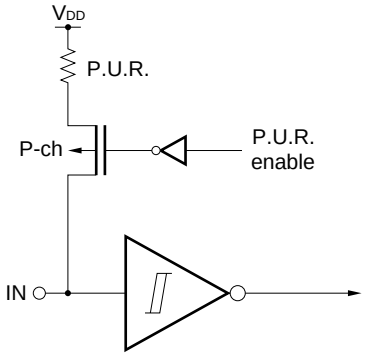

Schmitt trigger input with hysteresis characteristics

TYPE E-B



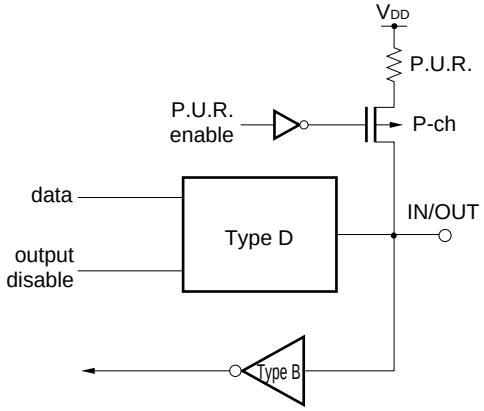

P.U.R. : Pull-Up Resistor

TYPE B-C



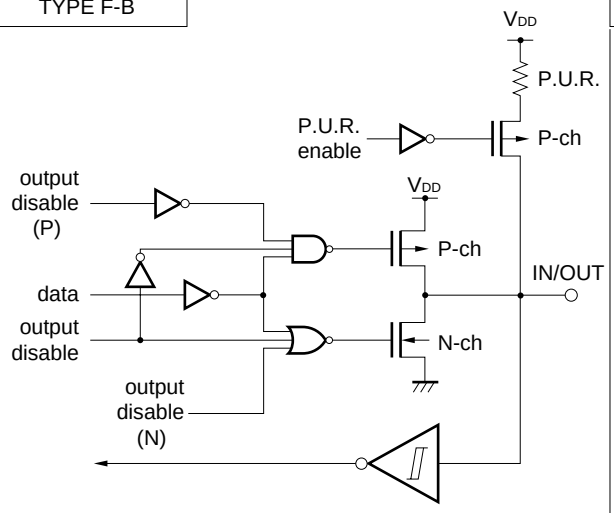

P.U.R. : Pull-Up Resistor

TYPE F-A



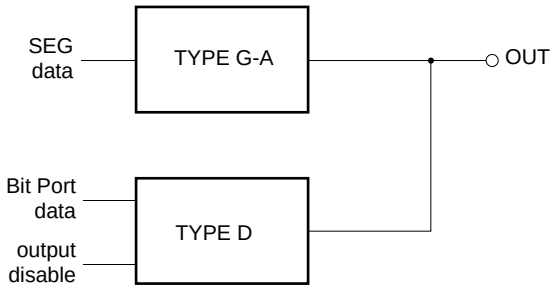

P.U.R. : Pull-Up Resistor

TYPE F-B

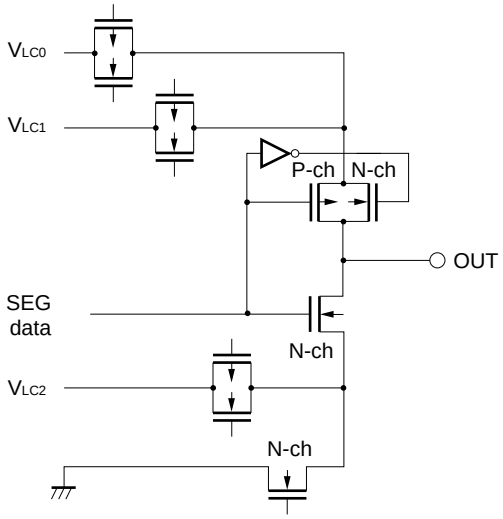



P.U.R. : Pull-Up Resistor

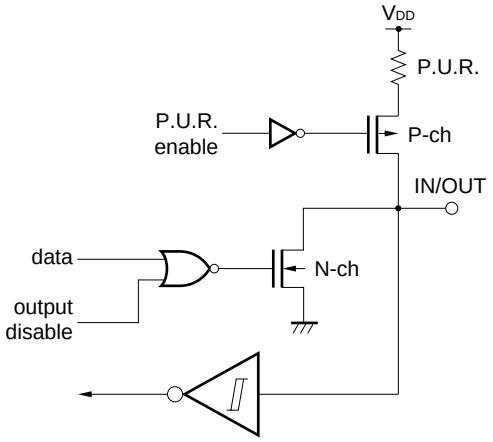
TYPE H-A★




TYPE G-A

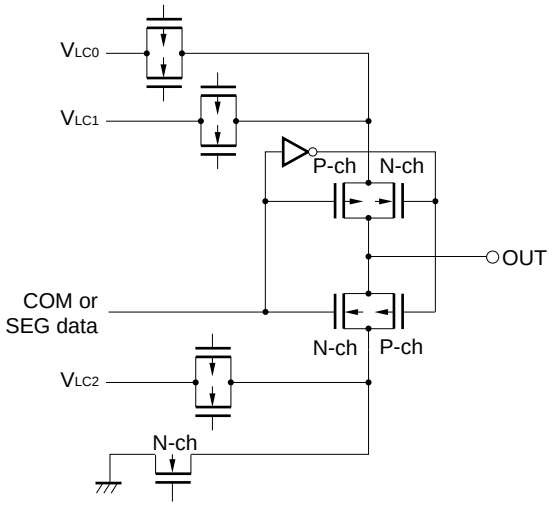



TYPE M-C

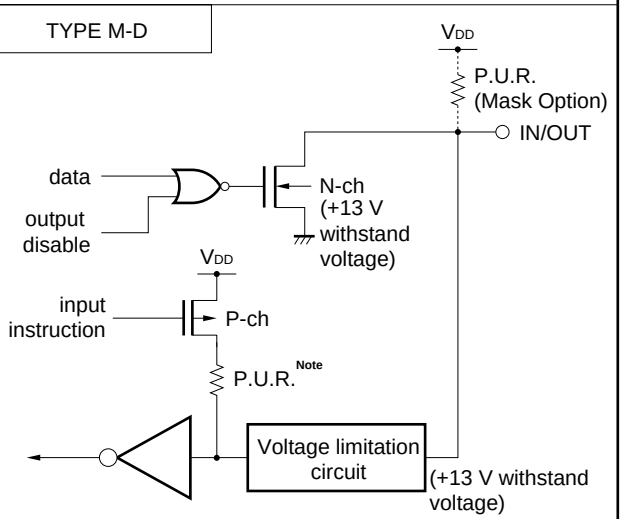



P.U.R. : Pull-Up Resistor

TYPE G-B




TYPE M-D




**Note** The pull-up resistor operates only when an input instruction is executed (current flows from $V_{DD}$ to the pin when the pin is low).

### 3.4 Recommended Connection for Unused Pins

**Table 3-1. List of Recommended Connection for Unused Pins**

| Pin | Recommended Connection |
|---|---|
| P00/INT4 | Connect to $V_{SS}$ or $V_{DD}$ |
| P01/$\overline{SCK}$ | Connect to $V_{SS}$ or $V_{DD}$ via a resistor individually |
| P02/SO/SB0 | |
| P03/SI/SB1 | Connect to $V_{SS}$ |
| P10/INT0, P11/INT1 | Connect to $V_{SS}$ or $V_{DD}$ |
| P12/TI1/TI2/INT2 | |
| P13/TI0 | |
| P20/PTO0 | Input: Connect to $V_{SS}$ or $V_{DD}$ via a resistor individually |
| P21/PTO1 | Output: Leave open |
| P22/PTO2/PCL | |
| P23/BUZ | |
| P30/LCDCL | |
| P31/SYNC | |
| P32 | |
| P33 | |
| P40-P43 | Input: Connect to $V_{SS}$ |
| P50-P53 | Output: Connect to $V_{SS}$ (do not connect a pull-up resistor of mask option) |
| P60/KR0-P63/KR3 | Input: Connect to $V_{SS}$ or $V_{DD}$ via a resistor individually |
| P70/KR4-P73/KR7 | Output: Leave open |
| S0-S23 | Leave open |
| S24/BP0-S31/BP7 | |
| COM0-COM3 | |
| $V_{LC0}$-$V_{LC2}$ | Connect to $V_{SS}$ |
| BIAS | Only if all of $V_{LC0}$-$V_{LC2}$ are unused, connect to $V_{SS}$. In other cases, leave open. |
| ★ XT1 | Connect to $V_{SS}$ |
| XT2[Note] | Leave open |
| IC | Connect to $V_{DD}$ directly |

**Note** When the subsystem clock is not used, set SOS.0 to 1 (so as not to use the internal feedback resistor).

## 4. SWITCHING FUNCTION BETWEEN Mk I MODE AND Mk II MODE

### 4.1 Differences between Mk I Mode and Mk II Mode

The CPU of μPD753017A has the following two modes: Mk I and Mk II, either of which can be selected. The mode can be switched by the bit 3 of the stack bank select register (SBS).

- Mk I mode: Upward compatible with μPD75316B.
  Can be used in the 75XL CPU with a ROM capacity of up to 16K bytes.
- Mk II mode: Incompatible with μPD75316B.
  Can be used in all the 75XL CPU's including those products whose ROM capacity is more than 16K bytes.

**Table 4-1. Differences between Mk I Mode and Mk II Mode**

| | Mk I Mode | Mk II Mode |
|---|---|---|
| Program memory (bytes) | • μPD753012A : 12288<br>• μPD753016A, 753017A : 16384 | • μPD753012A : 12288<br>• μPD753016A : 16384<br>• μPD753017A : 24576 |
| Number of stack bytes for subroutine instructions | 2 bytes | 3 bytes |
| BRA !addr1 instruction<br>CALLA !addr1 instruction | Not available | Available |
| CALL !addr instruction | 3 machine cycles | 4 machine cycles |
| CALLF !faddr instruction | 2 machine cycles | 3 machine cycles |

**Caution The Mk II mode supports a program area exceeding 16 Kbytes for the 75X and 75XL series. Therefore, this mode is effective for enhancing software compatibility with products exceeding 16 Kbytes.**
**When the Mk II mode is selected, the number of stack bytes used during execution of subroutine call instructions increases by one byte per stack compared to the Mk I mode. When the CALL !addr and CALLF !faddr instructions are used, the machine cycle becomes longer by one machine cycle. Therefore, use the Mk I mode if the RAM efficiency and processing performance are more important than software compatibility.**

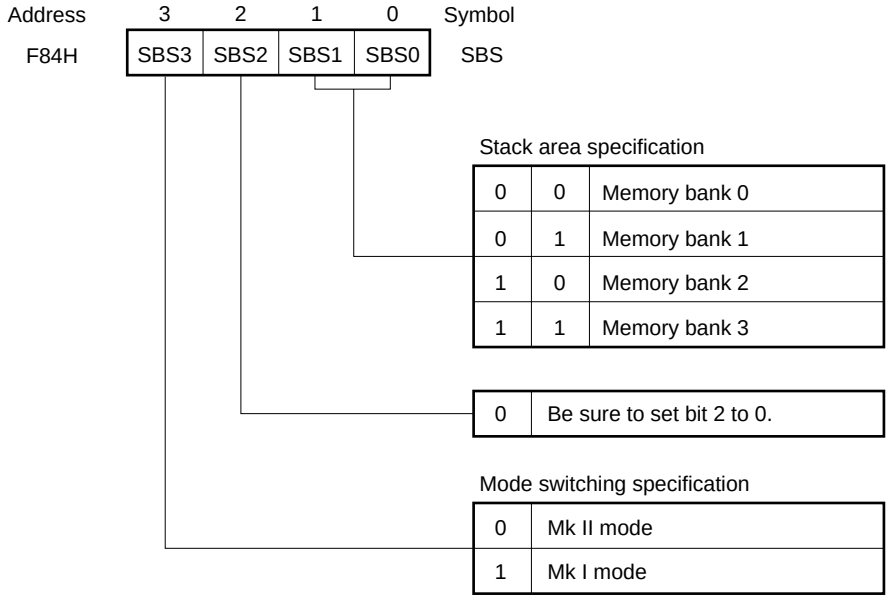
### 4.2 Setting Method of Stack Bank Select Register (SBS)

Switching between the Mk I mode and Mk II mode can be done by the stack bank select register (SBS). Figure 4-1 shows the format.

The SBS is set by a 4-bit memory manipulation instruction. When using the Mk I mode, the SBS must be initialized to 10XXB[Note] at the beginning of a program. When using the Mk II mode, it must be initialized to 00XXB[Note].

**Note** Set the desired value in the XX positions.

**Figure 4-1. Stack Bank Select Register Format**




**Caution Since SBS. 3 is set to "1" after a $\overline{\text{RESET}}$ signal is generated, the CPU operates in the Mk I mode. When executing an instruction in the Mk II mode, set SBS. 3 to "0" to select the Mk II mode.**

## 5. MEMORY CONFIGURATION

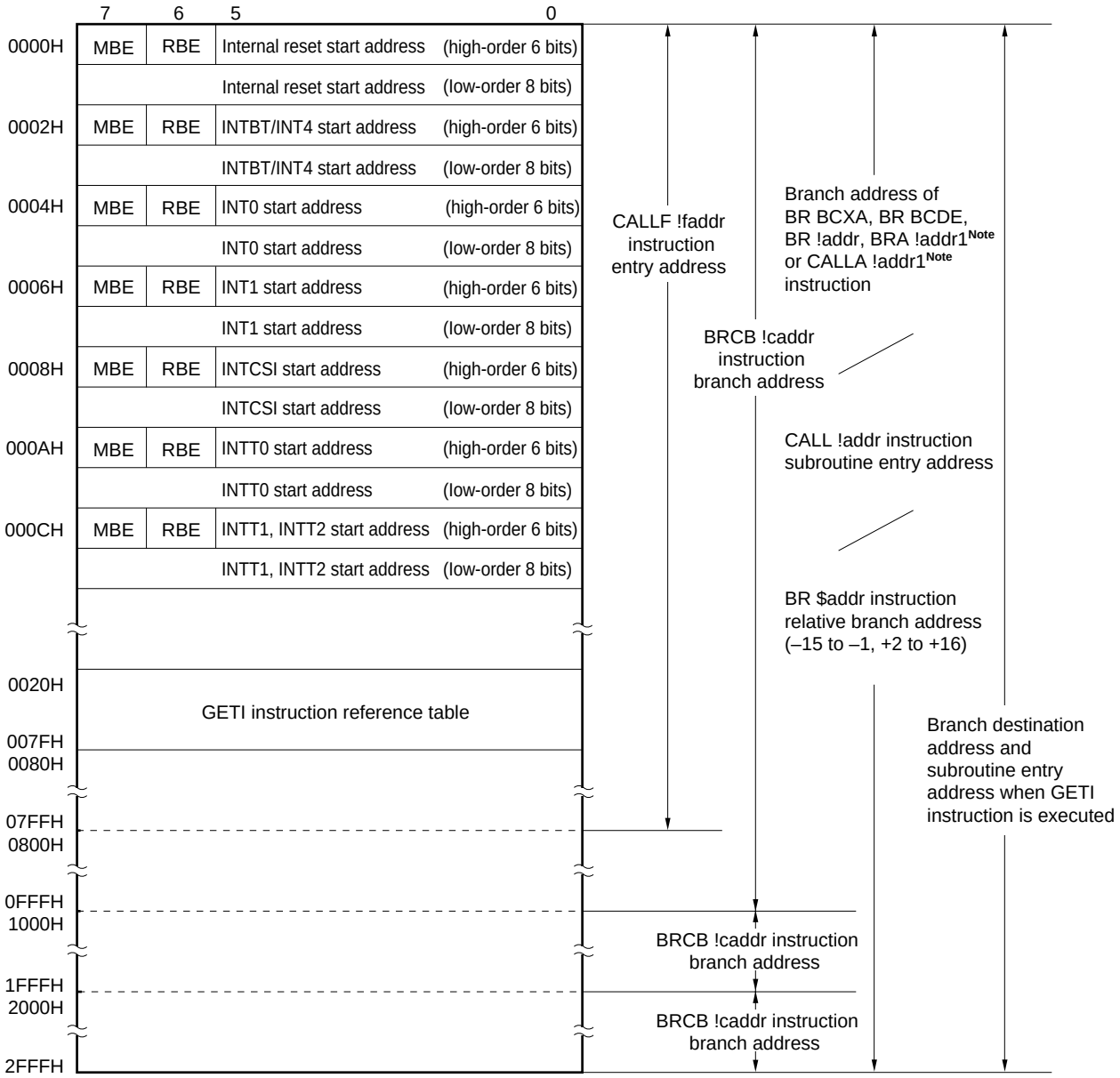
- Program memory (ROM) ..... 12288 × 8 bits (μPD753012A)
  ..... 16384 × 8 bits (μPD753016A)
  ..... 24576 × 8 bits (μPD753017A)
  - Addresses 0000H and 0001H
    Vector table wherein the program start address and the values set for the RBE and MBE at the time a $\overline{\text{RESET}}$ signal is generated are written. Reset start is possible from any address.
  - Addresses 0002H to 000DH
    Vector table wherein the program start address and the values set for the RBE and MBE by each vectored interrupt are written. Interrupt processing can start from any address.
  - Addresses 0020H to 007FH
    Table area referenced by the GETI instruction[Note].

    **Note** The GETI instruction realizes a 1-byte instruction on behalf of any 2-byte/3-byte instruction, or two 1-byte instructions. It is used to decrease the number of program steps.

- Data memory (RAM)
  - Data area ...1024 words × 4 bits (000H to 3FFH)
  - Peripheral hardware area...128 × 4 bits (F80H to FFFH)

**Figure 5-1. Program Memory Map (1/3)**

**(a) μPD753012A**

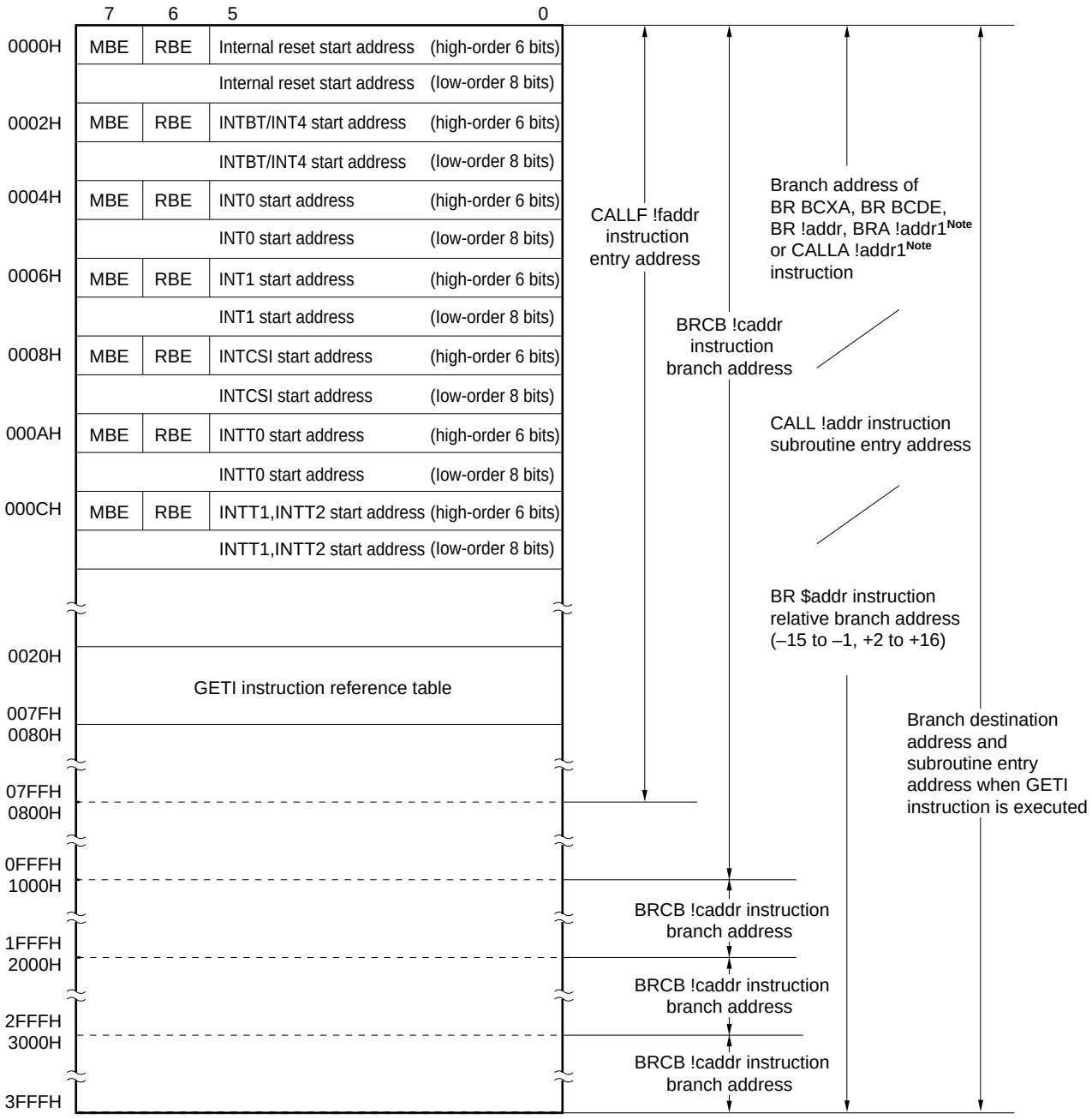



**Note** Can be used only in the Mk II mode.

**Remark** In addition to the above, a branch can be taken to the address indicated by changing only the low-order 8 bits of PC by executing the BR PCDE, BR PCXA instruction.

**Figure 5-1. Program Memory Map (2/3)**

**(b) μPD753016A**

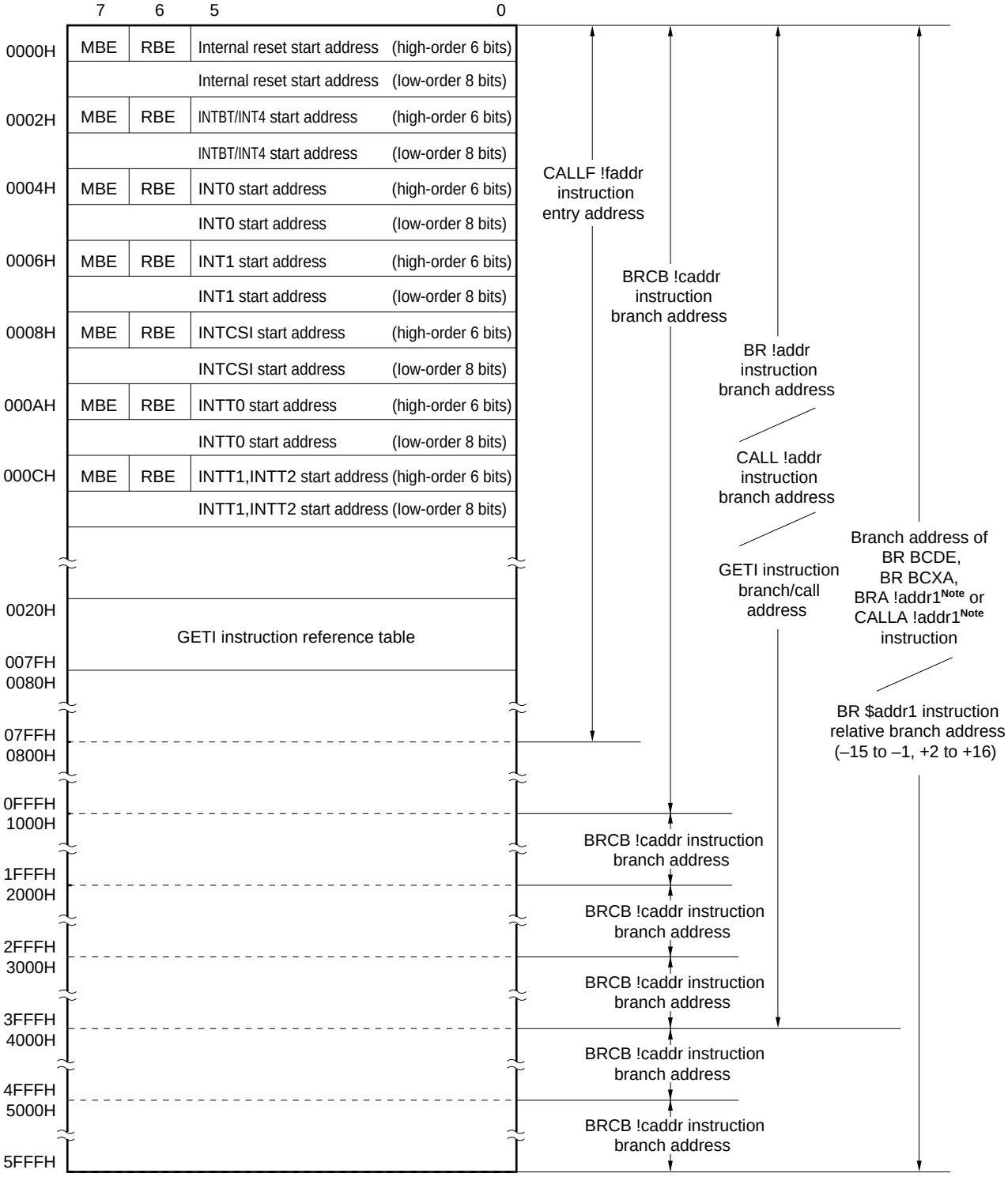



**Note** Can be used only in the Mk II mode.

**Remark** In addition to the above, a branch can be taken to the address indicated by changing only the low-order 8 bits of PC by executing the BR PCDE, BR PCXA instruction.

**Figure 5-1. Program Memory Map (3/3)**

**(c) μPD753017A**

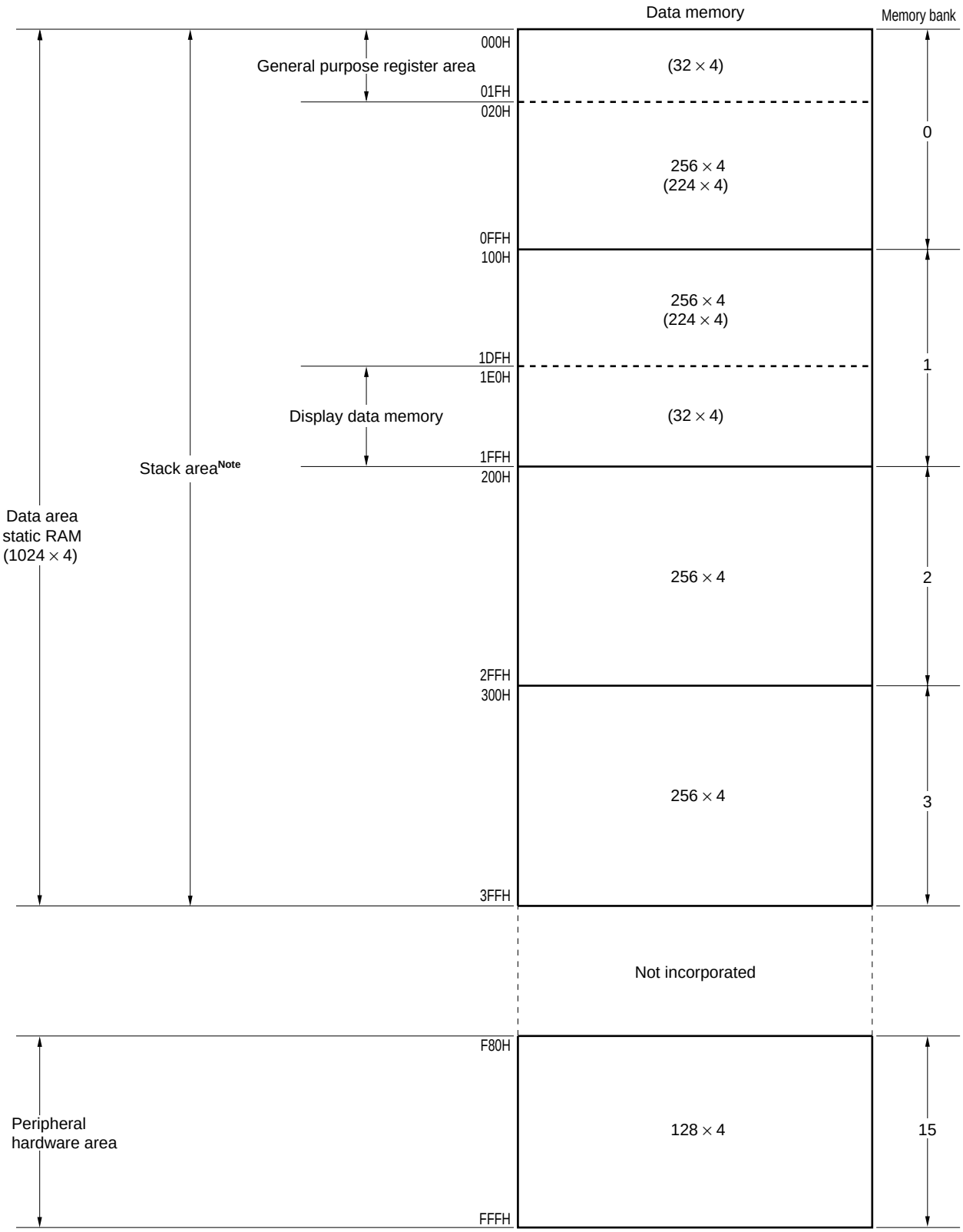



**Note** Can be used only in the Mk II mode.

**Caution The interrupt vector start address shown above consists of 14 bits. Set it in 16K space (0000H-3FFFH).**

**Remark** In addition to the above, a branch can be taken to the address indicated by changing only the low-order 8 bits of PC by executing the BR PCDE, BR PCXA instruction.

**Figure 5-2. Data Memory Map**




**Note** For stack area, one memory bank can be selected among memory banks 0 to 3.

# 6. PERIPHERAL HARDWARE FUNCTIONS

## 6.1 Digital Input/Output Ports

There are four types of I/O ports as follows.

| | |
|---|---|
| · CMOS input (PORT0, 1) | : 8 |
| · CMOS input/output (PORT2, 3, 6, 7) | : 16 |
| · N-channel open-drain input/output (PORT4, 5) | : 8 |
| · Bit port output (BP0-BP7) | : 8 |
| Total | 40 |

**Table 6-1. Types and Features of Digital Ports**

| Port (Pin Name) | Function | Operation and Features | | Remarks |
|---|---|---|---|---|
| PORT0 (P00-P03) | 4-bit input | When the serial interface function is used, the alternate function pins function as output ports depending on the operation mode. | | Also used for the INT4, SCK, SO/SB0, SI/SB1 pins. |
| PORT1 (P10-P13) | | Input-only port | | Also used for the INT0-INT2 and TI0-TI2 pins. |
| PORT2 (P20-P23) | 4-bit I/O | Can be set to input mode or output mode in 4-bit units. | | Also used for the PTO0-PTO2, PCL, BUZ pins. |
| PORT3 (P30-P33) | | Can be set to input mode or output mode in 1/4-bit units. | | Also used for the LCDCL, SYNC pins. |
| PORT4 (P40-P43) | 4-bit I/O (N-channel open-drain, 13 V withstanding) | Can be set to input mode or output mode in 4-bit units. | Ports 4 and 5 are paired and data can be input/output in 8-bit units. | On-chip pull-up resistor can be specified bit-wise by mask option. |
| PORT5 (P50-P53) | | | | |
| PORT6 (P60-P63) | 4-bit I/O | Can be set to input mode or output mode in 1/4-bit units. | Ports 6 and 7 are paired and data can be input/output in 8-bit units. | Also used for the KR0-KR3 pins. |
| PORT7 (P70-P73) | | Can be set to input mode or output mode in 4-bit units. | | Also used for the KR4-KR7 pins. |
| BP0-BP7 | 1-bit output | Outputs data bit-wise. Can be switched to LCD drive segment output S24-S31 by software. | | — |

## 6.2 Clock Generator

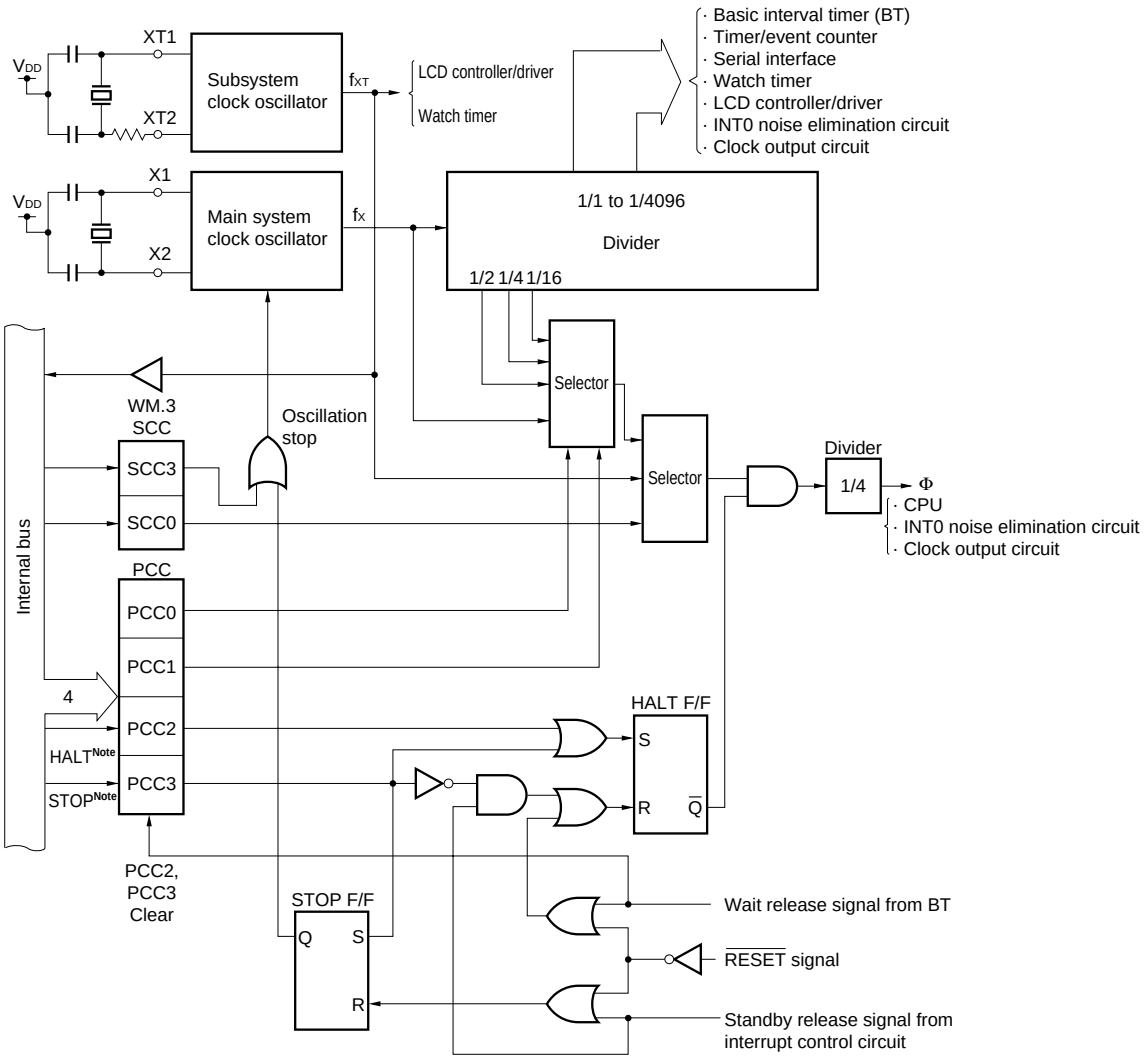
Operation of the clock generator is determined by the processor clock control register (PCC) and system clock control register (SCC).

The two clocks, the main system clock and subsystem clock, are available.

The instruction excution time can be altered.

- 0.95 μs, 1.91 μs, 3.81 μs, 15.3 μs (main system clock : at 4.19 MHz operation)
- 0.67 μs, 1.33 μs, 2.67 μs, 10.7 μs (main system clock : at 6.0 MHz operation)
- 122 μs (subsystem clock : at 32.768 kHz operation)

**Figure 6-1. Clock Generator Block Diagram**




**Note** Instruction execution

**Remarks 1.** $f_X$ = Main system clock frequency

**2.** $f_{XT}$ = Subsystem clock frequency

**3.** Φ = CPU clock

**4.** PCC: Processor Clock Control Register

**5.** SCC: System Clock Control Register

**6.** One clock cycle ($t_{CY}$) of Φ equal to one machine cycle of the instruction.

### 6.3 Subsystem Clock Oscillator Control Functions

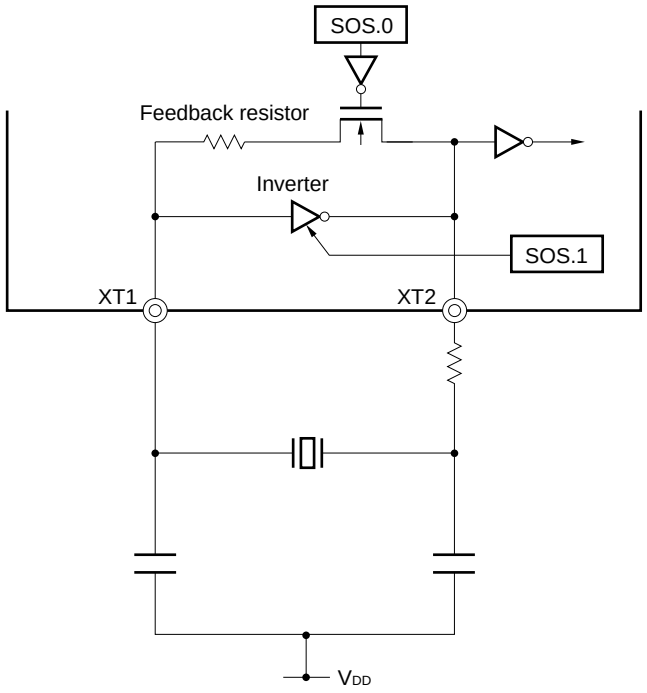
The μPD753017A subsystem clock oscillator has the following two control functions.

- Selects by software whether an internal feedback resistor is to be used or not[Note].
- Reduces current consumption by decreasing the drive current of the on-chip inverter when the supply voltage is high ($V_{DD} \geq 2.7$ V).

★ **Note** When the subsystem clock is not used, set SOS.0 to 1 (so as not to use the internal feedback resistor) by software, connect XT1 to $V_{SS}$, and open XT2. This makes it possible to reduce the current consumption in the subsystem clock oscillator.

The above functions can be used by switching the bits 0 and 1 of the sub-oscillator control register (SOS). (See Figure 6-2.)

**Figure 6-2. Subsystem Clock Oscillator**

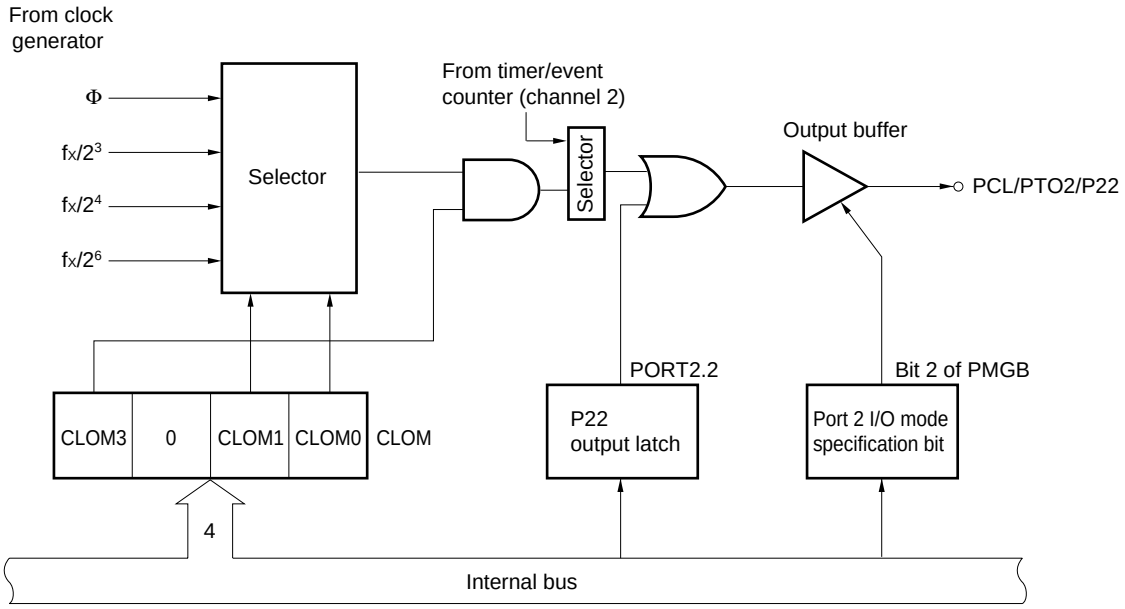


## 6.4 Clock Output Circuit

The clock output circuit is provided to output the clock pulses from the P22/PTO2/PCL pin to the application of remote control wave outputs and peripheral LSI's.

- Clock output (PCL) : Φ, 524, 262, 65.5 kHz (at 4.19 MHz operation)
  Φ, 750, 375, 93.8 kHz (at 6.0 MHz operation)

**Figure 6-3. Clock Output Circuit Block Diagram**



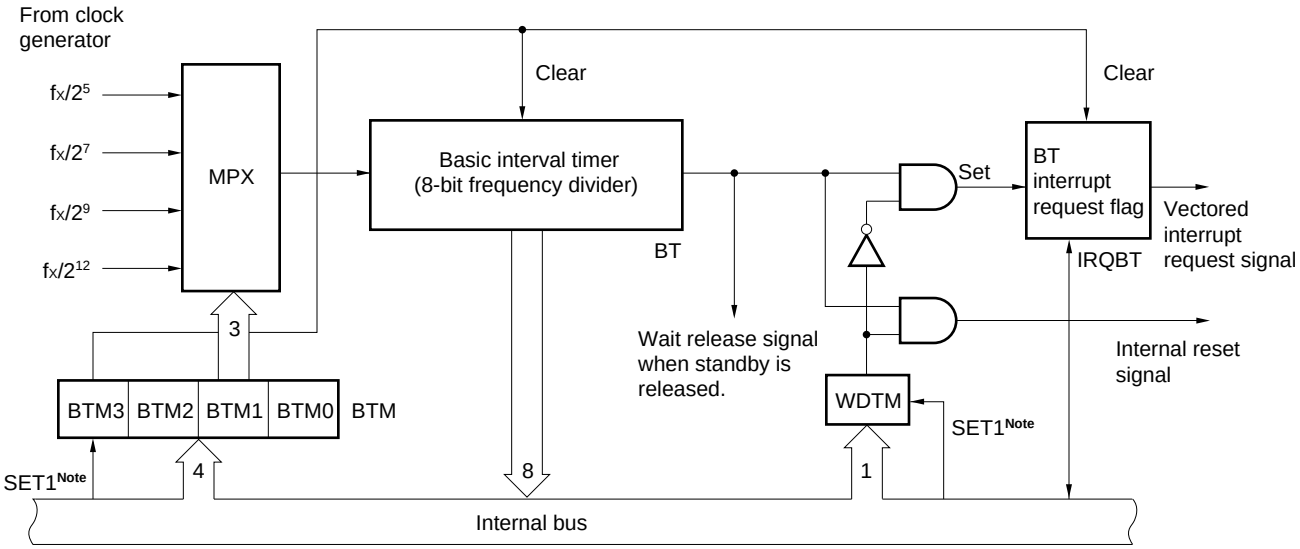

**Remark** Special care has been taken in designing the chip so that small-width pulses may not be output when switching clock output enable/disable.

## 6.5 Basic Interval Timer/Watchdog Timer

The basic interval timer/watchdog timer has the following functions.

- Interval timer operation to generate a reference time interrupt
- Watchdog timer operation to detect a runaway of program and reset the CPU
- Selects and counts the wait time when the standby mode is released
- Reads the contents of counting

**Figure 6-4. Basic Interval Timer/Watchdog Timer Block Diagram**



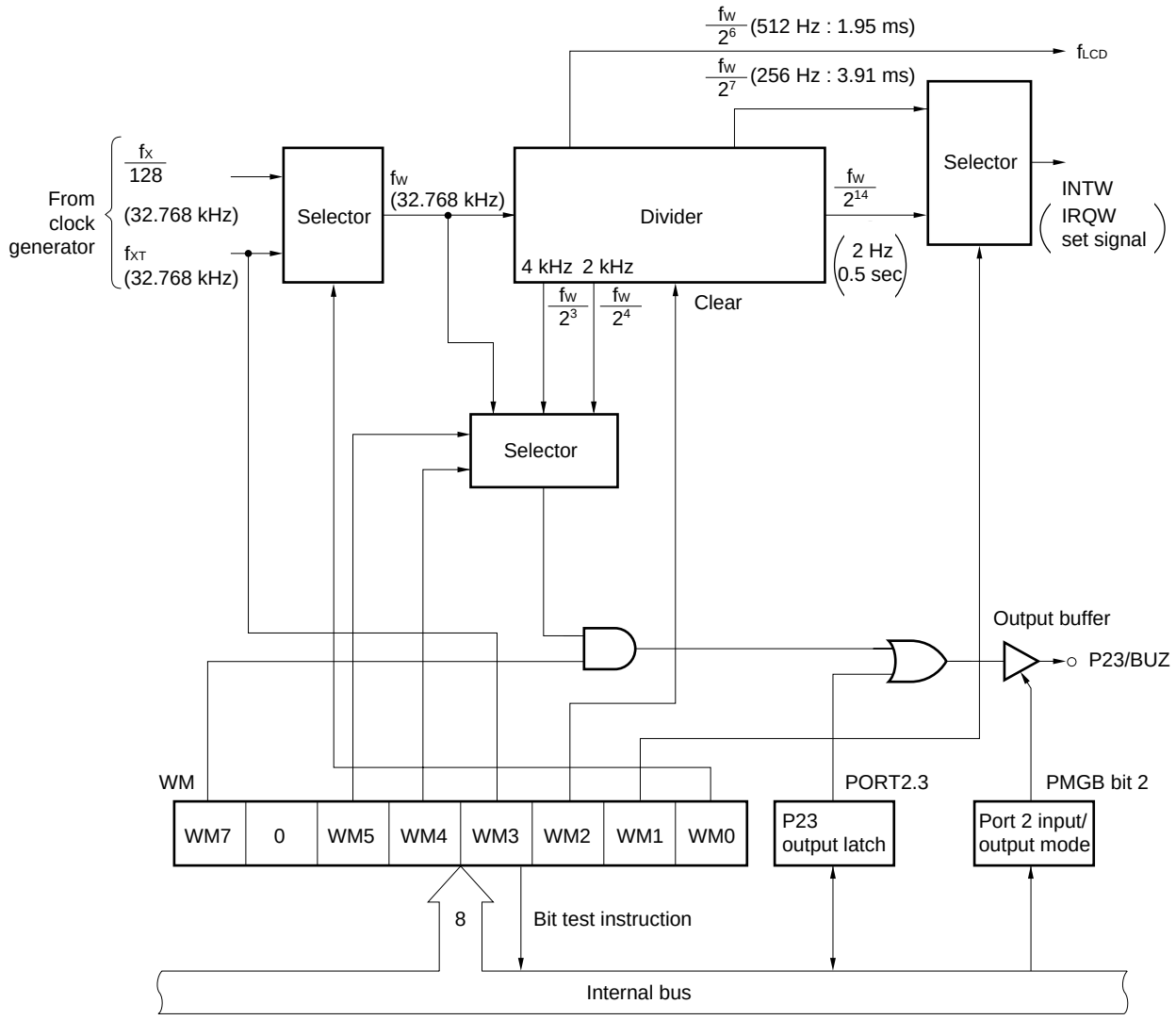

**Note** Instruction execution

## 6.6 Watch Timer

The μPD753017A has one channel of watch timer. The watch timer has the following functions.

- Sets the test flag (IRQW) with 0.5 sec interval.
  The standby mode can be released by the IRQW.
- 0.5 sec interval can be created by both the main system clock (4.19 MHz) and subsystem clock (32.768 kHz).
- Convenient for program debugging and checking as interval becomes 128 times longer (3.91 ms) with the fast feed mode.
- Outputs the frequencies (2.048, 4.096, 32.768 kHz) to the P23/BUZ pin, usable for buzzer and trimming of system clock oscillation frequencies.
- Clears the frequency divider to make the clock start with zero seconds.

**Figure 6-5. Watch Timer Block Diagram**




The values enclosed in parentheses are applied when $f_X$ = 4.19 MHz and $f_{XT}$ = 32.768 kHz.

## 6.7 Timer/Event Counter

The μPD753017A has three channels of timer/event counter. The timer/event counter has the following functions.

- Programmable interval timer operation
- Square wave output of any frequency to the PTOn pin (n = 0, 1)
- Event counter operation
- Divides the frequency of signal input via the TIn pin to 1-Nth of the original signal and outputs the divided frequency to the PTOn pin (frequency division operation).
- Supplies the shift clock to the serial interface circuit (channel 0 only).
- Calls the count value.

The timer/event counter operates in the following four modes as set by the mode register.

**Table 6-2. Operation Modes of Timer/Event Counter**

| Mode \ Channel | | Channel 0 | Channel 1 | Channel 2 |
|---|---|---|---|---|
| 8-bit timer/event counter mode | | Yes | Yes | Yes |
| | Gate control function | No[Note] | No | Yes |
| PWM pulse generator mode | | No | No | Yes |
| 16-bit timer/event counter mode | | No | Yes | |
| | Gate control function | No[Note] | Yes | |
| Carrier generator mode | | No | Yes | |

**Note** Used for gate control signal generation

**Figure 6-6. Timer/Event Counter Block Diagram (Channel 0)**

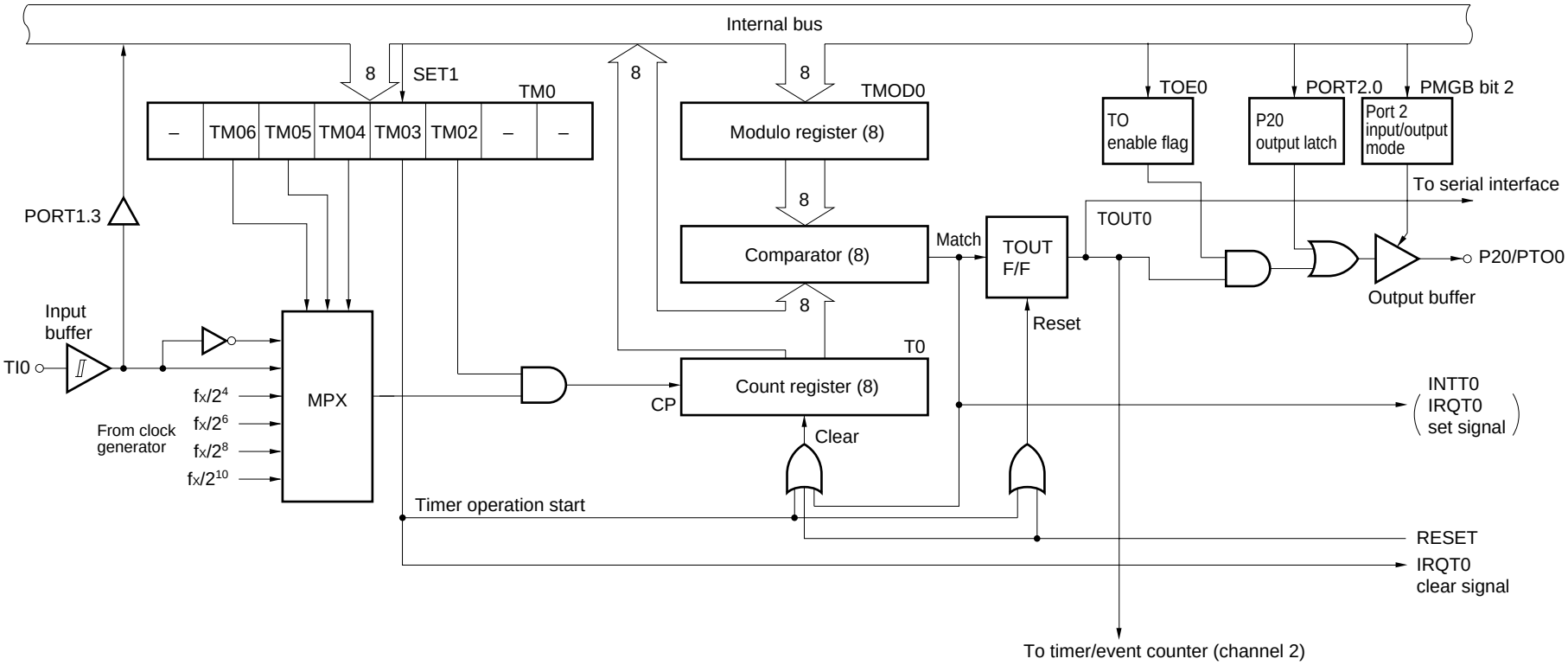


**Figure 6-7. Timer/Event Counter Block Diagram (Channel 1)**

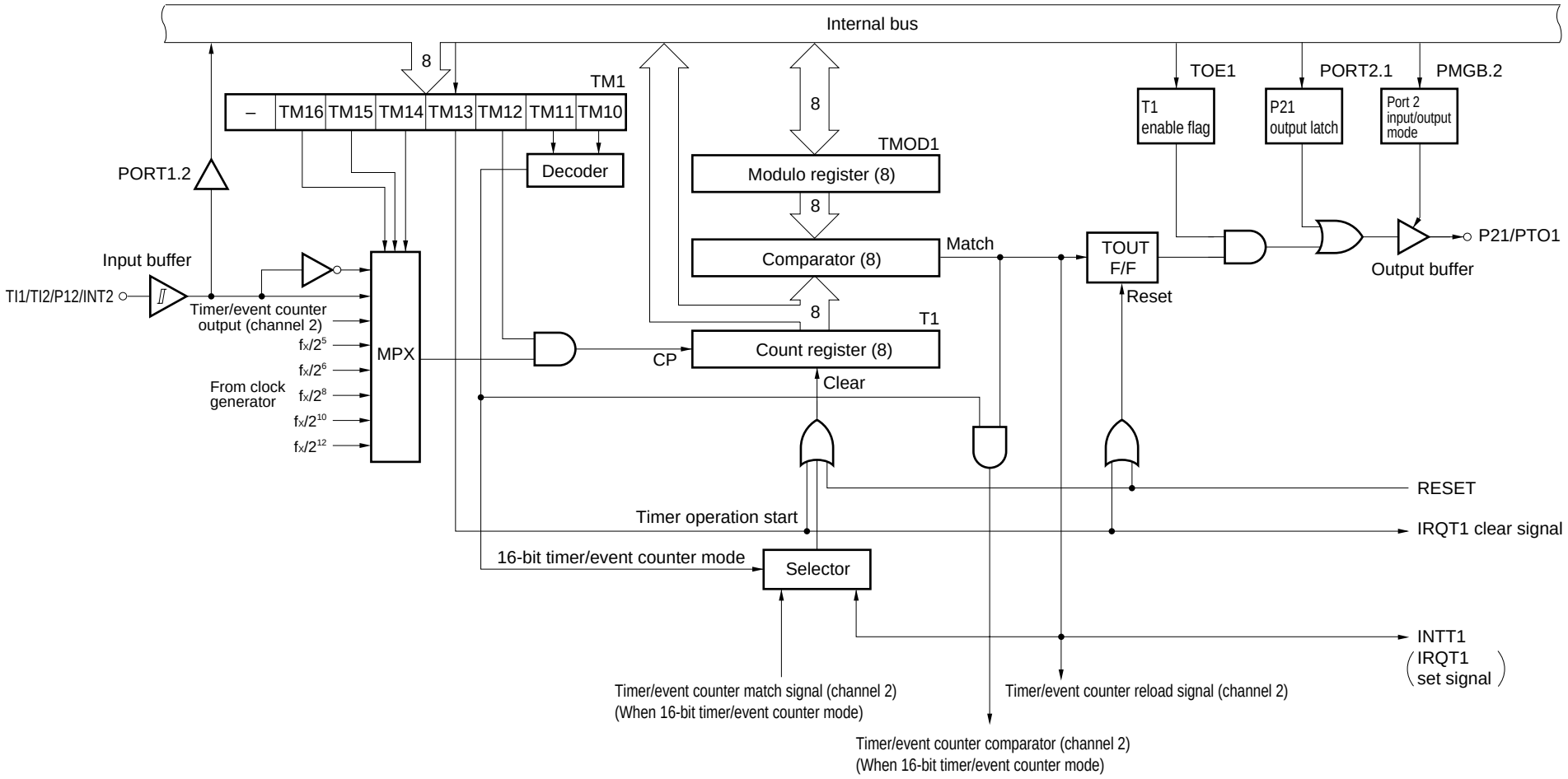
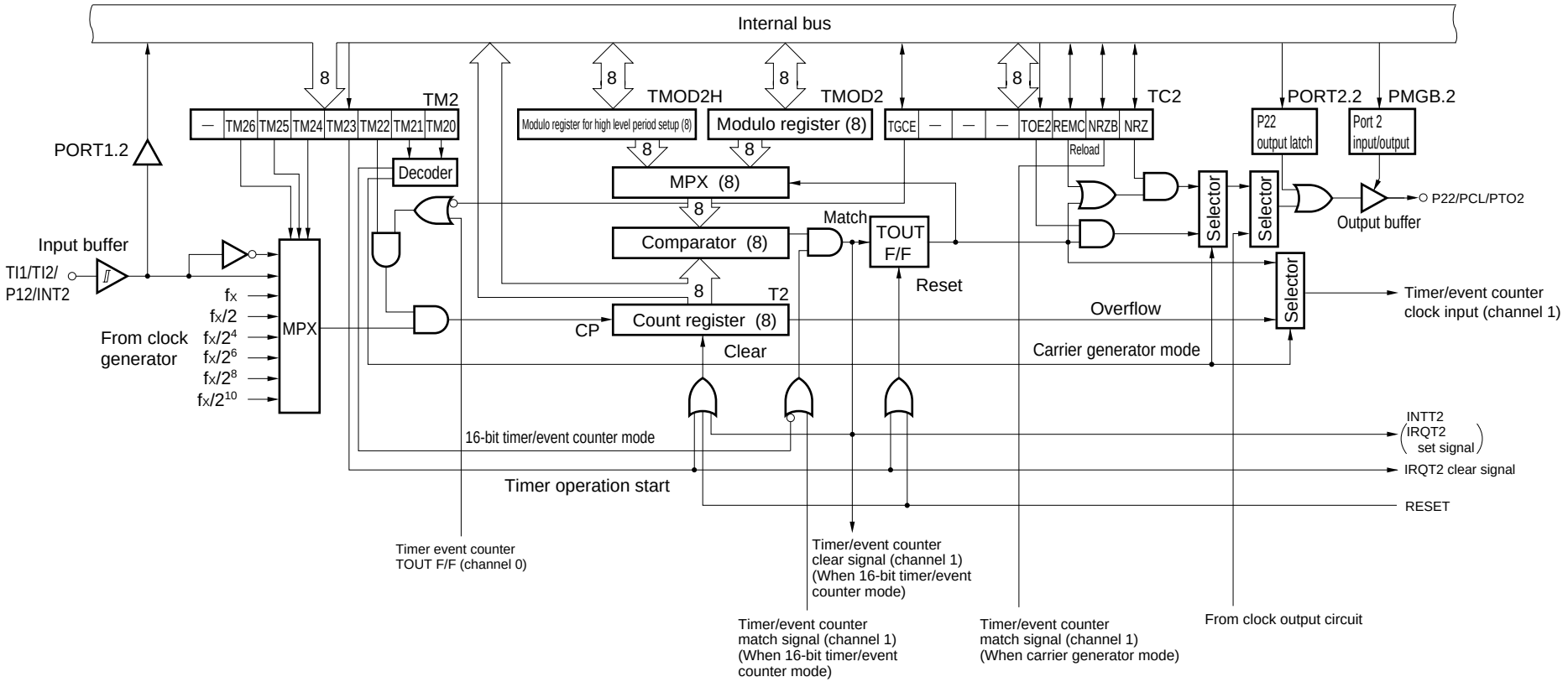


**Figure 6-8. Timer/Event Counter Block Diagram (Channel 2)**✦

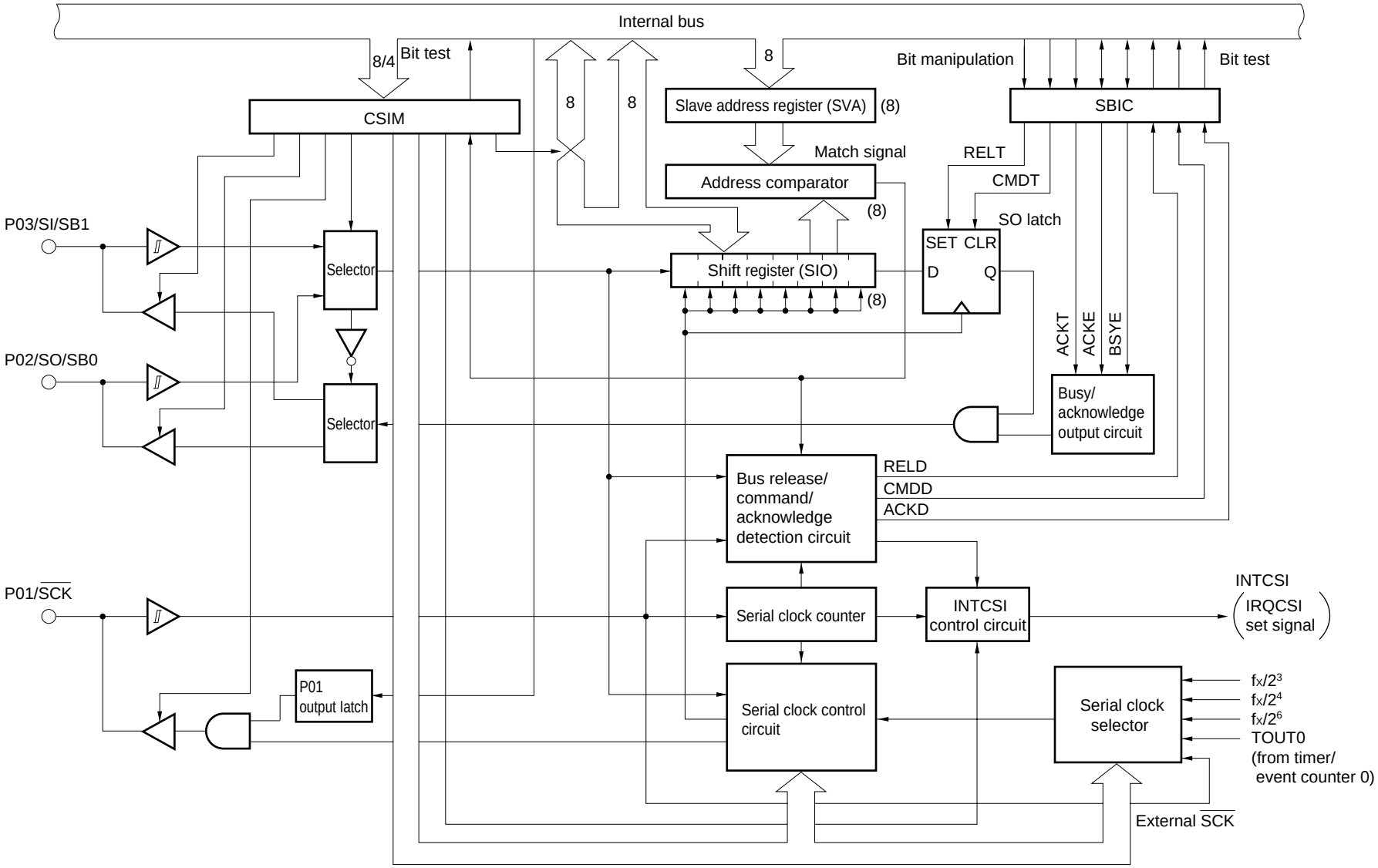


### 6.8 Serial Interface

The μPD753017A is provided with an 8-bit clocked serial interface. This serial interface operates in the following four modes:

- Operation stop mode
- 3-wire serial I/O mode
- 2-wire serial I/O mode
- SBI mode

**Figure 6-9. Serial Interface Block Diagram**



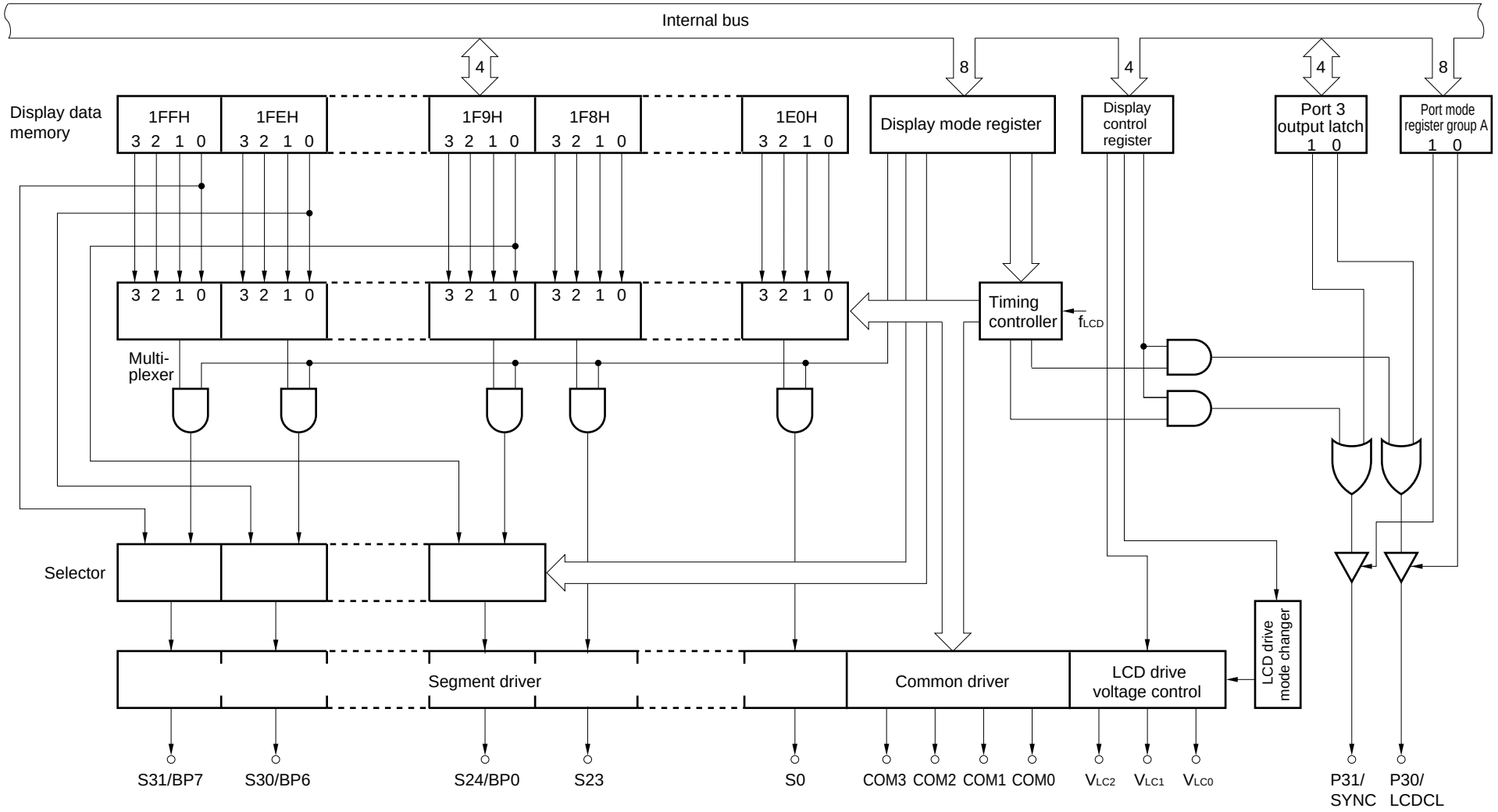
### 6.9 LCD Controller/Driver

The μPD753017A incorporates a display controller which generates segment and common signals according to the display data memory contents and incorporates segment and common drivers which can drive the LCD panel directly.

The μPD753017A LCD controller/driver functions are as follows:

- Display data memory is read automatically by DMA operation and segment and common signals are generated.
- Display mode can be selected from among the following five:
  ⟨1⟩ Static
  ⟨2⟩ 1/2 duty (time multiplexing by 2), 1/2 bias
  ⟨3⟩ 1/3 duty (time multiplexing by 3), 1/2 bias
  ⟨4⟩ 1/3 duty (time multiplexing by 3), 1/3 bias
  ⟨5⟩ 1/4 duty (time multiplexing by 4), 1/3 bias
- A frame frequency can be selected from among four in each display mode.
- A maximum of 32 segment signal output pins (S0-S31) and four common signal output pins (COM0-COM3).
- The segment signal output pins (S24-S27 and S28-S31) can be changed to the output ports in 4-pin units.
- Split-resistor can be incorporated to supply LCD drive power (mask option).
  · Various bias methods and LCD drive voltages can be applicable.
  · When display is off, current flow to the split resistor is cut.
- Display data memory not used for display can be used for normal data memory.
- It can also operate by using the subsystem clock.

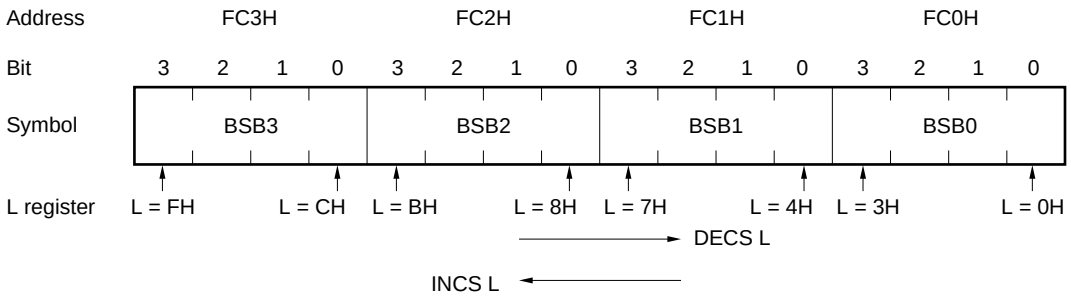
**Figure 6-10. LCD Controller/Driver Block Diagram**



## 6.10 Bit Sequential Buffer ... 16 Bits

The bit sequential buffer (BSB) is a special data memory for bit manipulation and the bit manipulation can be easily performed by changing the address specification and bit specification in sequence, therefore it is useful when processing a long data bit-wise.

**Figure 6-11. Bit Sequential Buffer Format**




**Remarks 1.** In the pmem.@L addressing, the specified bit moves corresponding to the L register.

**2.** In the pmem.@L addressing, the BSB can be manipulated regardless of MBE/MBS specification.

## 7. INTERRUPT FUNCTION AND TEST FUNCTION

μPD753017A has eight types of interrupt sources and two types of test sources. Among the test sources, INT2 is provided with two testable inputs for edge detection.

μPD753017A has the following functions in the interrupt control circuit.

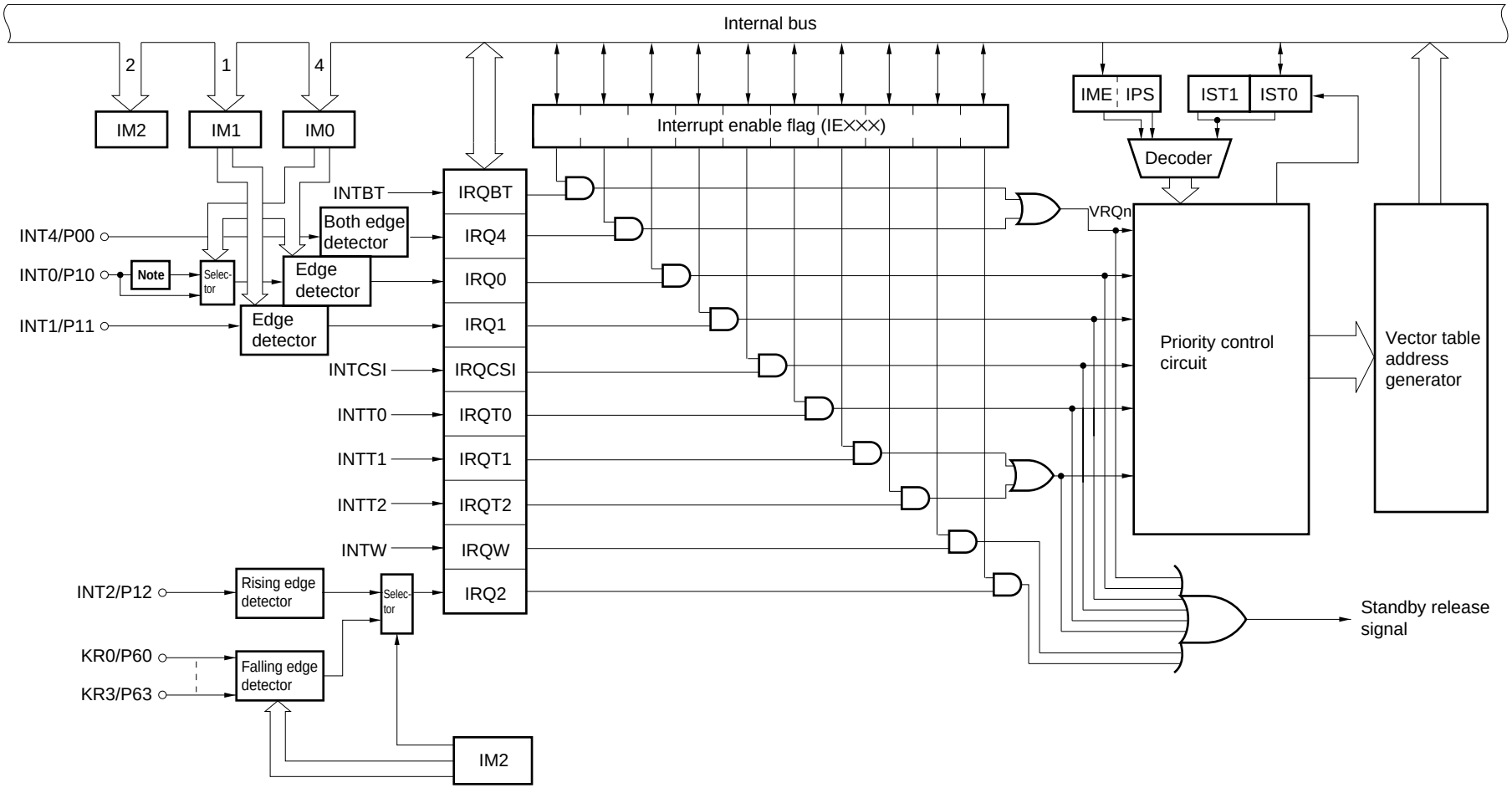
### (1) Interrupt function

- Vectored interrupt function for hardware control, enabling/disabling the interrupt acceptance by the interrupt enable flag (IEXXX) and interrupt master enable flag (IME).
- Can set any interrupt start address.
- Nesting interrupts wherein the order of priority can be specified by the interrupt priority select register (IPS).
- Test function of interrupt request flag (IRQXXX). An interrupt generated can be checked by software.
- Release the standby mode. A release interrupt can be selected by the interrupt enable flag.

### (2) Test function

- Test request flag (IRQXXX) generation can be checked by software.
- Release the standby mode. The test source to be released can be selected by the test enable flag.

**Figure 7-1. Interrupt Control Circuit Block Diagram**




**Note** Noise elimination circuit (Standby release is disabled when noise elimination circuit is selected.)

## 8. STANDBY FUNCTION

In order to save power consumption while a program is in a standby mode, two types of standby modes (STOP mode and HALT mode) are provided for the μPD753017A.

**Table 8-1. Operation Status in Standby Mode**

| | | STOP Mode | HALT Mode |
|---|---|---|---|
| Set instruction | | STOP instruction | HALT instruction |
| System clock when set | | Settable only when the main system clock is used. | Settable both by the main system clock and subsystem clock. |
| Operation status | Clock generator | Only the main system clock stops oscillation. | Only the CPU clock Φ halts (oscillation continues). |
| | Basic interval timer/ watchdog timer | Operation stops | Operation. (The IRQBT is set in the reference interval.)Note 1 |
| | Serial interface | Operable only when an external $\overline{SCK}$ input is selected as the serial clock. | OperableNote 1 |
| | Timer/event counter | Operable only when a signal input to the TI0-TI2 pins is specified as the count clock. | OperableNote 1 |
| | Watch timer | Operable when $f_{XT}$ is selected as the count clock. | Operable |
| | LCD controller/driver | Operable only when $f_{XT}$ is selected as the LCDCL. | Operable |
| | External interrupt | The INT1, 2, and 4 are operable.<br>Only the INT0 is not operated.Note 2 | |
| | CPU | The operation stops. | |
| ★ Release signals | | • Interrupt request signal sent from the operable hardware enabled by the interrupt enable flag.<br>• Test request signal sent from the test source enabled by the test enable flag.<br>• $\overline{RESET}$ input | |

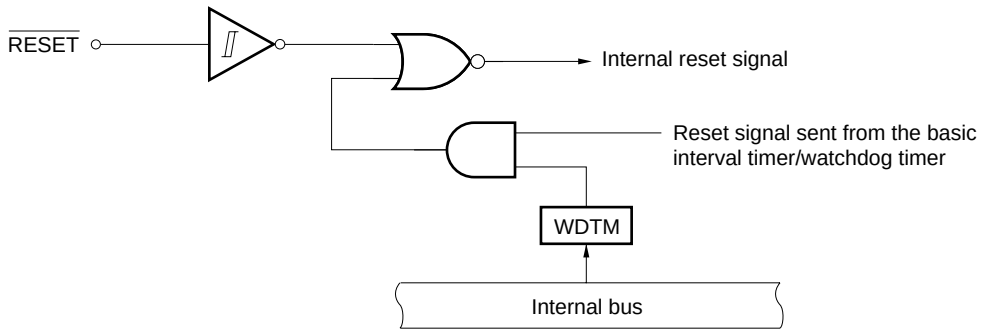
**Notes 1.** Cannot operate only when the main system clock stops.

**2.** Can operate only when the noise elimination circuit is not used (IM02 = 1) by bit 2 of the edge detection mode register (IM0).

## 9. RESET FUNCTION

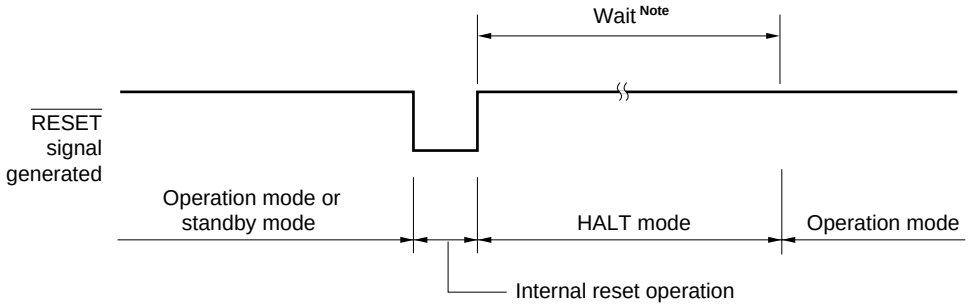
There are two reset inputs: external reset signal ($\overline{\text{RESET}}$) and reset signal sent from the basic interval timer/watchdog timer. When either one of the reset signals are input, an internal reset signal is generated. Figure 9-1 shows the circuit diagram of the above two inputs.

**Figure 9-1. Configuration of Reset Function**




The μPD753017A is set by the $\overline{\text{RESET}}$ signal generated and each hardware is initialized as listed in Table 9-1. Figure 9-2 shows the timing chart of the reset operation.

**Figure 9-2. Reset Operation by $\overline{\text{RESET}}$ Signal Generation**




**Note** The following two times can be selected by the mask option.

$2^{17}/f_X$ (21.8 ms : at 6.0 MHz operation, 31.3 ms : at 4.19 MHz operation)

$2^{15}/f_X$ (5.46 ms : at 6.0 MHz operation, 7.81 ms : at 4.19 MHz operation)

**Table 9-1. Status of Each Hardware after Reset (1/2)**

| Hardware | | $\overline{\text{RESET}}$ Signal Generation in Standby Mode | $\overline{\text{RESET}}$ Signal Generation in Operation |
|---|---|---|---|
| Program counter (PC) | | Sets the low-order 6 bits of program memory's address 0000H to the PC13-PC8 and the contents of address 0001H to the PC7-PC0. Resets the PC14 of the μPD753017A to 0. | Sets the low-order 6 bits of program memory's address 0000H to the PC13-PC8 and the contents of address 0001H to the PC7-PC0. Resets the PC14 of the μPD753017A to 0. |
| PSW | Carry flag (CY) | Held | Undefined |
| | Skip flag (SK0-SK2) | 0 | 0 |
| | Interrupt status flag (IST0) | 0 | 0 |
| | Bank enable flag (MBE, RBE) | Sets the bit 6 of program memory's address 0000H to the RBE and bit 7 to the MBE. | Sets the bit 6 of program memory's address 0000H to the RBE and bit 7 to the MBE. |
| Stack pointer (SP) | | Undefined | Undefined |
| Stack bank select register (SBS) | | 1000B | 1000B |
| Data memory (RAM) | | Held | Undefined |
| General-purpose register (X, A, H, L, D, E, B, C) | | Held | Undefined |
| Bank select register (MBS, RBS) | | 0, 0 | 0, 0 |
| Basic interval timer/ watchdog timer | Counter (BT) | Undefined | Undefined |
| | Mode register (BTM) | 0 | 0 |
| | Watchdog timer enable flag (WDTM) | 0 | 0 |
| Timer/event counter (T0) | Counter (T0) | 0 | 0 |
| | Modulo register (TMOD0) | FFH | FFH |
| | Mode register (TM0) | 0 | 0 |
| | TOE0, TOUT F/F | 0, 0 | 0, 0 |
| Timer/event counter (T1) | Counter (T1) | 0 | 0 |
| | Modulo register (TMOD1) | FFH | FFH |
| | Mode register (TM1) | 0 | 0 |
| | TOE1, TOUT F/F | 0, 0 | 0, 0 |
| Timer/event counter (T2) | Counter (T2) | 0 | 0 |
| | Modulo register (TMOD2) | FFH | FFH |
| | High level period setting modulo register (TMOD2H) | FFH | FFH |
| | Mode register (TM2) | 0 | 0 |
| | TOE2, TOUT F/F | 0, 0 | 0, 0 |
| | REMC, NRZ, NRZB | 0, 0, 0 | 0, 0, 0 |
| | TGE | 0 | 0 |
| Watch timer | Mode register (WM) | 0 | 0 |

**Table 9-1. Status of Each Hardware after Reset (2/2)**

| Hardware | | $\overline{\text{RESET}}$ Signal Generation in Standby Mode | $\overline{\text{RESET}}$ Signal Generation in Operation |
|---|---|---|---|
| Serial interface | Shift register (SIO) | Held | Undefined |
| | Operation mode register (CSIM) | 0 | 0 |
| | SBI control register (SBIC) | 0 | 0 |
| | Slave address register (SVA) | Held | Undefined |
| Clock generator, clock output circuit | Processor clock control register (PCC) | 0 | 0 |
| | System clock control register (SCC) | 0 | 0 |
| | Clock output mode register (CLOM) | 0 | 0 |
| Sub-oscillator control register (SOS) | | 0 | 0 |
| LCD controller/ driver | Display mode register (LCDM) | 0 | 0 |
| | Display control register (LCDC) | 0 | 0 |
| Interrupt function | Interrupt request flag (IRQXXX) | Reset (0) | Reset (0) |
| | Interrupt enable flag (IEXXX) | 0 | 0 |
| | Interrupt master enable flag (IME) | 0 | 0 |
| | INT0, 1, 2 mode registers (IM0, IM1, IM2) | 0, 0, 0 | 0, 0, 0 |
| | Interrupt priority selection register (IPS) | 0 | 0 |
| Digital port | Output buffer | Off | Off |
| | Output latch | Cleared (0) | Cleared (0) |
| | I/O mode registers (PMGA, PMGB) | 0 | 0 |
| | Pull-up resistor specification register (POGA) | 0 | 0 |
| Bit sequential buffer (BSB0-BSB3) | | Held | Undefined |

## 10. MASK OPTION

The μPD753017A has the following mask options.

- P40-P43, P50-P53 mask options
  On-chip pull-up resistors can be connected.
  <1> On-chip pull-up resistors are specifiable bit-wise.
  <2> On-chip pull-up resistors are not specifiable.

- $V_{LC0}$-$V_{LC2}$ pins, BIAS pin mask option
  On-chip split resistor for LCD drive can be connected.
  <1> Split resistor is not connected.
  <2> Four 10 kΩ (TYP.) split resistors are connected at the same time.
  <3> Four 100 kΩ (TYP.) split resistors are connected at the same time.

- Standby function mask option
  Wait times can be selected by a $\overline{\text{RESET}}$ signal.
  <1> $2^{17}/f_X$ (21.8 ms : at $f_X$ = 6.0 MHz, 31.3 ms : at $f_X$ = 4.19 MHz)
  <2> $2^{15}/f_X$ (5.46 ms : at $f_X$ = 6.0 MHz, 7.81 ms : at $f_X$ = 4.19 MHz)

- Subsystem clock mask option
  Use of the internal feedback resistor can be selected.
  <1> Internal feedback resistor can be used.
  (Switched ON/OFF via software)
  <2> Internal feedback resistor cannot be used.
  (Switched out in hardware)

## 11. INSTRUCTION SET

### (1) Expression formats and description methods of operands

The operand is described in the operand column of each instruction in accordance with the description method for the operand expression format of the instruction. For details, refer to **RA75X Assembler Package User's Manual——Language (U12385E)**. If there are several elements, one of them is selected. Capital letters and the + and – symbols are key words and are described as they are.

For immediate data, appropriate numbers and labels are described.

Instead of the labels such as mem, fmem, pmem, and bit, the symbols of the registers can be described. However, there are restrictions in the labels that can be described for fmem and pmem. For details, see User's Manual.

| Expression Format | Description Method |
|---|---|
| reg<br>reg1 | X, A, B, C, D, E, H, L<br>X, B, C, D, E, H, L |
| rp<br>rp1<br>rp2<br>rp'<br>rp'1 | XA, BC, DE, HL<br>BC, DE, HL<br>BC, DE<br>XA, BC, DE, HL, XA', BC', DE', HL'<br>BC, DE, HL, XA', BC', DE', HL' |
| rpa<br>rpa1 | HL, HL+, HL–, DE, DL<br>DE, DL |
| n4<br>n8 | 4-bit immediate data or label<br>8-bit immediate data or label |
| mem<br>bit | 8-bit immediate data or label[Note]<br>2-bit immediate data or label |
| fmem<br>pmem | FB0H-FBFH, FF0H-FFFH immediate data or label<br>FC0H-FFFH immediate data or label |
| addr<br><br>addr1<br>caddr<br>faddr | 0000H-2FFFH immediate data or label (μPD753012A)<br>0000H-3FFFH immediate data or label (μPD753016A, 753017A)<br>0000H-5FFFH immediate data or label<br>12-bit immediate data or label<br>11-bit immediate data or label |
| taddr | 20H-7FH immediate data (where bit0 = 0) or label |
| PORTn<br>IEXXX<br>RBn<br>MBn | PORT0-PORT7<br>IEBT, IET0-IET2, IE0-IE2, IE4, IECSI, IEW<br>RB0-RB3<br>MB0, MB1, MB2, MB3, MB15 |

**Note** mem can be only used even address in 8-bit data processing.

**(2) Legend in explanation of operation**

| | |
|---|---|
| A | : A register; 4-bit accumulator |
| B | : B register |
| C | : C register |
| D | : D register |
| E | : E register |
| H | : H register |
| L | : L register |
| X | : X register |
| XA | : XA register pair; 8-bit accumulator |
| BC | : BC register pair |
| DE | : DE register pair |
| HL | : HL register pair |
| XA' | : XA' expanded register pair |
| BC' | : BC' expanded register pair |
| DE' | : DE' expanded register pair |
| HL' | : HL' expanded register pair |
| PC | : Program counter |
| SP | : Stack pointer |
| CY | : Carry flag; bit accumulator |
| PSW | : Program status word |
| MBE | : Memory bank enable flag |
| RBE | : Register bank enable flag |
| PORTn | : Port n (n = 0-7) |
| IME | : Interrupt master enable flag |
| IPS | : Interrupt priority selection register |
| IEXXX | : Interrupt enable flag |
| RBS | : Register bank selection register |
| MBS | : Memory bank selection register |
| PCC | : Processor clock control register |
| . | : Separation between address and bit |
| (XX) | : The contents addressed by XX |
| XXH | : Hexadecimal data |

### (3) Explanation of symbols under addressing area column

| | | | |
|---|---|---|---|
| *1 | MB = MBE•MBS<br>(MBS = 0-3, 15) | | Data memory addressing |
| *2 | MB = 0 | | |
| *3 | MBE = 0 : MB = 0 (000H-07FH)<br>MB = 15 (F80H-FFFH)<br>MBE = 1 : MB = MBS (MBS = 0-3, 15) | | |
| *4 | MB = 15, fmem = FB0H-FBFH, FF0H-FFFH | | |
| *5 | MB = 15, pmem = FC0H-FFFH | | |
| *6 | μPD753012A | addr = 0000H-2FFFH | Program memory addressing |
| | μPD753016A<br>753017A | addr = 0000H-3FFFH | |
| *7 | μPD753012A<br>753016A<br>753017A<br>(In Mk I mode) | addr = (Current PC) – 15 to (Current PC) – 1<br>(Current PC) + 2 to (Current PC) + 16 | |
| | μPD753017A<br>(In Mk II mode) | addr1 = (Current PC) – 15 to (Current PC) – 1<br>(Current PC) + 2 to (Current PC) + 16 | |
| *8 | μPD753012A | caddr = 0000H-0FFFH ($PC_{13, 12}$ = 00B) or<br>1000H-1FFFH ($PC_{13, 12}$ = 01B) or<br>2000H-2FFFH ($PC_{13, 12}$ = 10B) | |
| | μPD753016A | caddr = 0000H-0FFFH ($PC_{13, 12}$ = 00B) or<br>1000H-1FFFH ($PC_{13, 12}$ = 01B) or<br>2000H-2FFFH ($PC_{13, 12}$ = 10B) or<br>3000H-3FFFH ($PC_{13, 12}$ = 11B) | |
| | μPD753017A | caddr = 0000H-0FFFH ($PC_{14, 13, 12}$ = 000B) or<br>1000H-1FFFH ($PC_{14, 13, 12}$ = 001B) or<br>2000H-2FFFH ($PC_{14, 13, 12}$ = 010B) or<br>3000H-3FFFH ($PC_{14, 13, 12}$ = 011B) or<br>4000H-4FFFH ($PC_{14, 13, 12}$ = 100B) or<br>5000H-5FFFH ($PC_{14, 13, 12}$ = 101B) | |
| *9 | faddr = 0000H-07FFH | | |
| *10 | taddr = 0020H-007FH | | |
| *11 | μPD753012A | addr1 = 0000H-2FFFH | |
| | μPD753016A | addr1 = 0000H-3FFFH | |
| | μPD753017A | addr1 = 0000H-5FFFH | |

**Remarks 1.** MB indicates memory bank that can be accessed.

**2.** In *2, MB = 0 independently of how MBE and MBS are set.

**3.** In *4 and *5, MB = 15 independently of how MBE and MBS are set.

**4.** *6 to *11 indicate the areas that can be addressed.

**(4) Explanation of number of machine cycles column**

S denotes the number of machine cycles required by skip operation when a skip instruction is executed. The value of S varies as follows.

- When no skip is made: S = 0
- When the skipped instruction is a 1- or 2-byte instruction: S = 1
- When the skipped instruction is a 3-byte instruction[Note]: S = 2

**Note** 3-byte instruction: BR !addr, BRA !addr1, CALL !addr or CALLA !addr1 instruction

**Caution The GETI instruction is skipped in one machine cycle.**

One machine cycle is equal to one cycle of CPU clock Φ (= $t_{CY}$); time can be selected from among four types by setting PCC.

| Instruction Group | Mnemonic | Operand | Number of Bytes | Number of Machine Cycles | Operation | Addressing Area | Skip Condition |
|---|---|---|---|---|---|---|---|
| Transfer | MOV | A, #n4 | 1 | 1 | A ← n4 | | String effect A |
| | | reg1, #n4 | 2 | 2 | reg1 ← n4 | | |
| | | XA, #n8 | 2 | 2 | XA ← n8 | | String effect A |
| | | HL, #n8 | 2 | 2 | HL ← n8 | | String effect B |
| | | rp2, #n8 | 2 | 2 | rp2 ← n8 | | |
| | | A, @HL | 1 | 1 | A ← (HL) | *1 | |
| | | A, @HL+ | 1 | 2+S | A ← (HL), then L ← L+1 | *1 | L = 0 |
| | | A, @HL– | 1 | 2+S | A ← (HL), then L ← L–1 | *1 | L = FH |
| | | A, @rpa1 | 1 | 1 | A ← (rpa1) | *2 | |
| | | XA, @HL | 2 | 2 | XA ← (HL) | *1 | |
| | | @HL, A | 1 | 1 | (HL) ← A | *1 | |
| | | @HL, XA | 2 | 2 | (HL) ← XA | *1 | |
| | | A, mem | 2 | 2 | A ← (mem) | *3 | |
| | | XA, mem | 2 | 2 | XA ← (mem) | *3 | |
| | | mem, A | 2 | 2 | (mem) ← A | *3 | |
| | | mem, XA | 2 | 2 | (mem) ← XA | *3 | |
| | | A, reg1 | 2 | 2 | A ← reg1 | | |
| | | XA, rp' | 2 | 2 | XA ← rp' | | |
| | | reg1, A | 2 | 2 | reg1 ← A | | |
| | | rp'1, XA | 2 | 2 | rp'1 ← XA | | |
| | XCH | A, @HL | 1 | 1 | A ↔ (HL) | *1 | |
| | | A, @HL+ | 1 | 2+S | A ↔ (HL), then L ← L+1 | *1 | L = 0 |
| | | A, @HL– | 1 | 2+S | A ↔ (HL), then L ← L–1 | *1 | L = FH |
| | | A, @rpa1 | 1 | 1 | A ↔ (rpa1) | *2 | |
| | | XA, @HL | 2 | 2 | XA ↔ (HL) | *1 | |
| | | A, mem | 2 | 2 | A ↔ (mem) | *3 | |
| | | XA, mem | 2 | 2 | XA ↔ (mem) | *3 | |
| | | A, reg1 | 1 | 1 | A ↔ reg1 | | |
| | | XA, rp' | 2 | 2 | XA ↔ rp' | | |

| Instruction Group | Mnemonic | Operand | Number of Bytes | Number of Machine Cycles | Operation | Addressing Area | Skip Condition |
|---|---|---|---|---|---|---|---|
| Table reference | MOVT[Note 1] | XA, @PCDE | 1 | 3 | XA ← $(PC_{13-8}+DE)_{ROM}$ | | |
| | | | | | ● μPD753017A<br>XA ← $(PC_{14-8}+DE)_{ROM}$ | | |
| | | XA, @PCXA | 1 | 3 | XA ← $(PC_{13-8}+XA)_{ROM}$ | | |
| | | | | | ● μPD753017A<br>XA ← $(PC_{14-8}+XA)_{ROM}$ | | |
| | | XA, @BCDE[Note 2] | 1 | 3 | XA ← $(B_{1,0}+CDE)_{ROM}$ | *6 | |
| | | | | | ● μPD753017A<br>XA ← $(B_{2-0}+CDE)_{ROM}$ | *11 | |
| | | XA, @BCXA[Note 2] | 1 | 3 | XA ← $(B_{1,0}+CXA)_{ROM}$ | *6 | |
| | | | | | ● μPD753017A<br>XA ← $(B_{2-0}+CXA)_{ROM}$ | *11 | |
| Bit transfer | MOV1 | CY, fmem.bit | 2 | 2 | CY ← (fmem.bit) | *4 | |
| | | CY, pmem.@L | 2 | 2 | CY ← $(pmem_{7-2}+L_{3-2}.bit(L_{1-0}))$ | *5 | |
| | | CY, @H+mem.bit | 2 | 2 | CY ← $(H+mem_{3-0}.bit)$ | *1 | |
| | | fmem.bit, CY | 2 | 2 | (fmem.bit) ← CY | *4 | |
| | | pmem.@L, CY | 2 | 2 | $(pmem_{7-2}+L_{3-2}.bit(L_{1-0}))$ ← CY | *5 | |
| | | @H+mem.bit, CY | 2 | 2 | $(H+mem_{3-0}.bit)$ ← CY | *1 | |
| Operation | ADDS | A, #n4 | 1 | 1+S | A ← A+n4 | | carry |
| | | XA, #n8 | 2 | 2+S | XA ← XA+n8 | | carry |
| | | A, @HL | 1 | 1+S | A ← A+(HL) | *1 | carry |
| | | XA, rp' | 2 | 2+S | XA ← XA+rp' | | carry |
| | | rp'1, XA | 2 | 2+S | rp'1 ← rp'1+XA | | carry |
| | ADDC | A, @HL | 1 | 1 | A, CY ← A+(HL)+CY | *1 | |
| | | XA, rp' | 2 | 2 | XA, CY ← XA+rp'+CY | | |
| | | rp'1, XA | 2 | 2 | rp'1, CY ← rp'1+XA+CY | | |
| | SUBS | A, @HL | 1 | 1+S | A ← A–(HL) | *1 | borrow |
| | | XA, rp' | 2 | 2+S | XA ← XA–rp' | | borrow |
| | | rp'1, XA | 2 | 2+S | rp'1 ← rp'1–XA | | borrow |
| | SUBC | A, @HL | 1 | 1 | A, CY ← A–(HL)–CY | *1 | |
| | | XA, rp' | 2 | 2 | XA, CY ← XA–rp'–CY | | |
| | | rp'1, XA | 2 | 2 | rp'1, CY ← rp'1–XA–CY | | |

**Notes 1.** The above operations in the shaded boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

**2.** Only the following bits are valid for the B register.

μPD753012A, 753016A : low-order 2 bits

μPD753017A : low-order 3 bits

**Remark** When the μPD753017A is set in the Mk I mode, $PC_{14}$ is fixed to 0.

| Instruction Group | Mnemonic | Operand | Number of Bytes | Number of Machine Cycles | Operation | Addressing Area | Skip Condition |
|---|---|---|---|---|---|---|---|
| Operation | AND | A, #n4 | 2 | 2 | A ← A ∧ n4 | | |
| | | A, @HL | 1 | 1 | A ← A ∧ (HL) | *1 | |
| | | XA, rp' | 2 | 2 | XA ← XA ∧ rp' | | |
| | | rp'1, XA | 2 | 2 | rp'1 ← rp'1 ∧ XA | | |
| | OR | A, #n4 | 2 | 2 | A ← A ∨ n4 | | |
| | | A, @HL | 1 | 1 | A ← A ∨ (HL) | *1 | |
| | | XA, rp' | 2 | 2 | XA ← XA ∨ rp' | | |
| | | rp'1, XA | 2 | 2 | rp'1 ← rp'1 ∨ XA | | |
| | XOR | A, #n4 | 2 | 2 | A ← A ∀ n4 | | |
| | | A, @HL | 1 | 1 | A ← A ∀ (HL) | *1 | |
| | | XA, rp' | 2 | 2 | XA ← XA ∀ rp' | | |
| | | rp'1, XA | 2 | 2 | rp'1 ← rp'1 ∀ XA | | |
| Accumulator manipulation | RORC | A | 1 | 1 | CY ← $A_0$, $A_3$ ← CY, $A_{n-1}$ ← $A_n$ | | |
| | NOT | A | 2 | 2 | A ← $\overline{A}$ | | |
| Increment and Decrement | INCS | reg | 1 | 1+S | reg ← reg+1 | | reg = 0 |
| | | rp1 | 1 | 1+S | rp1 ← rp1+1 | | rp1 = 00H |
| | | @HL | 2 | 2+S | (HL) ← (HL)+1 | *1 | (HL) = 0 |
| | | mem | 2 | 2+S | (mem) ← (mem)+1 | *3 | (mem) = 0 |
| | DECS | reg | 1 | 1+S | reg ← reg–1 | | reg = FH |
| | | rp' | 2 | 2+S | rp' ← rp'–1 | | rp' = FFH |
| Comparison | SKE | reg, #n4 | 2 | 2+S | Skip if reg = n4 | | reg = n4 |
| | | @HL, #n4 | 2 | 2+S | Skip if (HL) = n4 | *1 | (HL) = n4 |
| | | A, @HL | 1 | 1+S | Skip if A = (HL) | *1 | A = (HL) |
| | | XA, @HL | 2 | 2+S | Skip if XA = (HL) | *1 | XA = (HL) |
| | | A, reg | 2 | 2+S | Skip if A = reg | | A = reg |
| | | XA, rp' | 2 | 2+S | Skip if XA = rp' | | XA = rp' |
| Carry flag manipulation | SET1 | CY | 1 | 1 | CY ← 1 | | |
| | CLR1 | CY | 1 | 1 | CY ← 0 | | |
| | SKT | CY | 1 | 1+S | Skip if CY = 1 | | CY = 1 |
| | NOT1 | CY | 1 | 1 | CY ← $\overline{CY}$ | | |

| Instruction Group | Mnemonic | Operand | Number of Bytes | Number of Machine Cycles | Operation | Addressing Area | Skip Condition |
|---|---|---|---|---|---|---|---|
| Memory bit manipulation | SET1 | mem.bit | 2 | 2 | (mem.bit) ← 1 | *3 | |
| | | fmem.bit | 2 | 2 | (fmem.bit) ← 1 | *4 | |
| | | pmem.@L | 2 | 2 | (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) ← 1 | *5 | |
| | | @H+mem.bit | 2 | 2 | (H+mem$_{3-0}$.bit) ← 1 | *1 | |
| | CLR1 | mem.bit | 2 | 2 | (mem.bit) ← 0 | *3 | |
| | | fmem.bit | 2 | 2 | (fmem.bit) ← 0 | *4 | |
| | | pmem.@L | 2 | 2 | (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) ← 0 | *5 | |
| | | @H+mem.bit | 2 | 2 | (H+mem$_{3-0}$.bit) ← 0 | *1 | |
| | SKT | mem.bit | 2 | 2+S | Skip if (mem.bit)=1 | *3 | (mem.bit)=1 |
| | | fmem.bit | 2 | 2+S | Skip if (fmem.bit)=1 | *4 | (fmem.bit)=1 |
| | | pmem.@L | 2 | 2+S | Skip if (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))=1 | *5 | (pmem.@L)=1 |
| | | @H+mem.bit | 2 | 2+S | Skip if (H+mem$_{3-0}$.bit)=1 | *1 | (@H+mem.bit)=1 |
| | SKF | mem.bit | 2 | 2+S | Skip if (mem.bit)=0 | *3 | (mem.bit)=0 |
| | | fmem.bit | 2 | 2+S | Skip if (fmem.bit)=0 | *4 | (fmem.bit)=0 |
| | | pmem.@L | 2 | 2+S | Skip if (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))=0 | *5 | (pmem.@L)=0 |
| | | @H+mem.bit | 2 | 2+S | Skip if (H+mem$_{3-0}$.bit)=0 | *1 | (@H+mem.bit)=0 |
| | SKTCLR | fmem.bit | 2 | 2+S | Skip if (fmem.bit)=1 and clear | *4 | (fmem.bit)=1 |
| | | pmem.@L | 2 | 2+S | Skip if (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))=1 and clear | *5 | (pmem.@L)=1 |
| | | @H+mem.bit | 2 | 2+S | Skip if (H+mem$_{3-0}$.bit)=1 and clear | *1 | (@H+mem.bit)=1 |
| | AND1 | CY, fmem.bit | 2 | 2 | CY ← CY ∧ (fmem.bit) | *4 | |
| | | CY, pmem.@L | 2 | 2 | CY ← CY ∧ (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) | *5 | |
| | | CY, @H+mem.bit | 2 | 2 | CY ← CY ∧ (H+mem$_{3-0}$.bit) | *1 | |
| | OR1 | CY, fmem.bit | 2 | 2 | CY ← CY ∨ (fmem.bit) | *4 | |
| | | CY, pmem.@L | 2 | 2 | CY ← CY ∨ (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) | *5 | |
| | | CY, @H+mem.bit | 2 | 2 | CY ← CY ∨ (H+mem$_{3-0}$.bit) | *1 | |
| | XOR1 | CY, fmem.bit | 2 | 2 | CY ← CY ∀ (fmem.bit) | *4 | |
| | | CY, pmem.@L | 2 | 2 | CY ← CY ∀ (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) | *5 | |
| | | CY, @H+mem.bit | 2 | 2 | CY ← CY ∀ (H+mem$_{3-0}$.bit) | *1 | |

| Instruction Group | Mnemonic | Operand | Number of Bytes | Number of Machine Cycles | Operation | Addressing Area | Skip Condition |
|---|---|---|---|---|---|---|---|
| Branch | BR[Note 1] | addr | – | – | $PC_{13-0} \leftarrow$ addr<br>(Select appropriate instruction from among the following instructions according to the assembler being used.<br>BR !addr<br>BRCB !caddr<br>BR $addr) | *6 | |
| | | addr1 | – | – | ● μPD753012A, 753016A<br>$PC_{13-0} \leftarrow$ addr1<br>(Select appropriate instruction from among the following instructions according to the assembler being used.<br>BR !addr<br>BRA !addr1<br>BRCB !caddr<br>BR $addr1) | *11 | |
| | | | | | ● μPD753017A<br>$PC_{14-0} \leftarrow$ addr1<br>(Select appropriate instruction from among the following instructions according to the assembler being used.<br>BR !addr<br>BRA !addr1<br>BRCB !caddr<br>BR $addr1) | | |
| | | !addr | 3 | 3 | $PC_{13-0} \leftarrow$ addr | *6 | |
| | | | | | ● μPD753017A<br>$PC_{14} \leftarrow 0$, $PC_{13-0} \leftarrow$ addr | | |
| | | $addr | 1 | 2 | $PC_{13-0} \leftarrow$ addr | *7 | |
| | | $addr1 | 1 | 2 | ● μPD753017A<br>$PC_{14-0} \leftarrow$ addr1 | | |
| | | PCDE | 2 | 3 | $PC_{13-0} \leftarrow PC_{13-8}$+DE | | |
| | | | | | ● μPD753017A<br>$PC_{14-0} \leftarrow PC_{14-8}$+DE | | |
| | | PCXA | 2 | 3 | $PC_{13-0} \leftarrow PC_{13-8}$+XA | | |
| | | | | | ● μPD753017A<br>$PC_{14-0} \leftarrow PC_{14-8}$+XA | | |
| | | BCDE[Note 2] | 2 | 3 | $PC_{13-0} \leftarrow$ BCDE | *6 | |
| | | | | | ● μPD753017A<br>$PC_{14-0} \leftarrow$ BCDE | *11 | |
| | | BCXA[Note 2] | 2 | 3 | $PC_{13-0} \leftarrow$ BCXA | *6 | |
| | | | | | ● μPD753017A<br>$PC_{14-0} \leftarrow$ BCXA | *11 | |

**Notes 1.** The above operations in the shaded boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

**2.** Only the following bits are valid for the B register.

μPD753012A, 753016A : low-order 2 bits

μPD753017A : low-order 3 bits

**Remark** When the μPD753017A is set in the Mk I mode, $PC_{14}$ is fixed to 0.

| Instruction Group | Mnemonic | Operand | Number of Bytes | Number of Machine Cycles | Operation | Addressing Area | Skip Condition |
|---|---|---|---|---|---|---|---|
| Branch | BRA[Note] | !addr | 3 | 3 | ● μPD753012A, 753016A<br>$PC_{13-0} \leftarrow$ addr | *6 | |
| | | !addr1 | 3 | 3 | ● μPD753017A<br>$PC_{14-0} \leftarrow$ addr1 | *11 | |
| | BRCB[Note] | !caddr | 2 | 2 | $PC_{13-0} \leftarrow PC_{13,12}$+caddr$_{11-0}$ | *8 | |
| | | | | | ● μPD753017A<br>$PC_{14-0} \leftarrow PC_{14,13,12}$+caddr$_{11-0}$ | | |
| Subroutine stack control | CALLA[Note] | !addr | 3 | 3 | ● μPD753012A, 753016A<br>$(SP-6)(SP-3)(SP-4) \leftarrow PC_{11-0}$<br>$(SP-5) \leftarrow 0, 0, PC_{13, 12}$<br>$(SP-2) \leftarrow \times, \times$, MBE, RBE<br>$PC_{13-0} \leftarrow$ addr, SP ← SP–6 | *6 | |
| | | !addr1 | 3 | 3 | ● μPD753017A<br>$(SP-6)(SP-3)(SP-4) \leftarrow PC_{11-0}$<br>$(SP-5) \leftarrow 0, PC_{14, 13, 12}$<br>$(SP-2) \leftarrow \times, \times$, MBE, RBE<br>$PC_{14-0} \leftarrow$ addr1, SP ← SP–6 | *11 | |
| | CALL[Note] | !addr | 3 | 3 | $(SP-4)(SP-1)(SP-2) \leftarrow PC_{11-0}$<br>$(SP-3) \leftarrow$ MBE, RBE, $PC_{13}$, $PC_{12}$<br>$PC_{13-0} \leftarrow$ addr, SP ← SP–4 | *6 | |
| | | | | 4 | ● μPD753012A, 753016A<br>$(SP-6)(SP-3)(SP-4) \leftarrow PC_{11-0}$<br>$(SP-5) \leftarrow 0, 0, PC_{13, 12}$<br>$(SP-2) \leftarrow \times, \times$, MBE, RBE<br>$PC_{13-0} \leftarrow$ addr, SP ← SP–6 | | |
| | | | | 4 | ● μPD753017A<br>$(SP-6)(SP-3)(SP-4) \leftarrow PC_{11-0}$<br>$(SP-5) \leftarrow 0, PC_{14, 13, 12}$<br>$(SP-2) \leftarrow \times, \times$, MBE, RBE<br>$PC_{14} \leftarrow 0, PC_{13-0} \leftarrow$ addr, SP ← SP–6 | | |
| | CALLF[Note] | !faddr | 2 | 2 | $(SP-4)(SP-1)(SP-2) \leftarrow PC_{11-0}$<br>$(SP-3) \leftarrow$ MBE, RBE, $PC_{13}$, $PC_{12}$<br>$PC_{13-0} \leftarrow$ 000+faddr, SP ← SP–4 | *9 | |
| | | | | 3 | ● μPD753012A, 753016A<br>$(SP-6)(SP-3)(SP-4) \leftarrow PC_{11-0}$<br>$(SP-5) \leftarrow 0, 0, PC_{13, 12}$<br>$(SP-2) \leftarrow \times, \times$, MBE, RBE<br>$PC_{13-0} \leftarrow$ 000+faddr, SP ← SP–6 | | |
| | | | | 3 | ● μPD753017A<br>$(SP-6)(SP-3)(SP-4) \leftarrow PC_{11-0}$<br>$(SP-5) \leftarrow 0, PC_{14, 13, 12}$<br>$(SP-2) \leftarrow \times, \times$, MBE, RBE<br>$PC_{14-0} \leftarrow$ 0000+faddr, SP ← SP–6 | | |

**Note** The above operations in the shaded boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

**Remark** When the μPD753017A is set in the Mk I mode, $PC_{14}$ is fixed to 0.

| Instruction Group | Mnemonic | Operand | Number of Bytes | Number of Machine Cycles | Operation | Addressing Area | Skip Condition |
|---|---|---|---|---|---|---|---|
| Subroutine stack control | RET[Note] | | 1 | 3 | MBE, RBE, $PC_{13}$, $PC_{12}$ ← (SP+1)<br>$PC_{11-0}$ ← (SP)(SP+3)(SP+2),<br>SP ← SP+4 | | |
| | | | | | ● μPD753012A, 753016A<br>×, ×, MBE, RBE ← (SP+4)<br>0, 0, $PC_{13}$, $PC_{12}$ ← (SP+1)<br>$PC_{11-0}$ ← (SP)(SP+3)(SP+2), SP ← SP+6 | | |
| | | | | | ● μPD753017A<br>×, ×, MBE, RBE ← (SP+4)<br>0, $PC_{14}$, $PC_{13}$, $PC_{12}$ ← (SP+1)<br>$PC_{11-0}$ ← (SP)(SP+3)(SP+2), SP ← SP+6 | | |
| | RETS[Note] | | 1 | 3+S | MBE, RBE, $PC_{13}$, $PC_{12}$ ← (SP+1)<br>$PC_{11-0}$ ← (SP)(SP+3)(SP+2),<br>SP ← SP+4<br>then skip unconditionally | | Unconditional |
| | | | | | ● μPD753012A, 753016A<br>×, ×, MBE, RBE ← (SP+4)<br>0, 0, $PC_{13}$, $PC_{12}$ ← (SP+1)<br>$PC_{11-0}$ ← (SP)(SP+3)(SP+2), SP ← SP+6<br>then skip unconditionally | | |
| | | | | | ● μPD753017A<br>×, ×, MBE, RBE ← (SP+4)<br>0, $PC_{14}$, $PC_{13}$, $PC_{12}$ ← (SP+1)<br>$PC_{11-0}$ ← (SP)(SP+3)(SP+2), SP ← SP+6<br>then skip unconditionally | | |
| | RETI[Note] | !faddr | 1 | 3 | MBE, RBE, $PC_{13}$, $PC_{12}$ ← (SP+1)<br>$PC_{11-0}$ ← (SP)(SP+3)(SP+2)<br>PSW ← (SP+4)(SP+5), SP ← SP+6 | | |
| | | | | | ● μPD753012A, 753016A<br>0, 0, $PC_{13}$, $PC_{12}$ ← (SP+1)<br>$PC_{11-0}$ ← (SP)(SP+3)(SP+2)<br>PSW ← (SP+4)(SP+5), SP ← SP+6 | | |
| | | | | | ● μPD753017A<br>0, $PC_{14}$, $PC_{13}$, $PC_{12}$ ← (SP+1)<br>$PC_{11-0}$ ← (SP)(SP+3)(SP+2)<br>PSW ← (SP+4)(SP+5), SP ← SP+6 | | |

**Note** The above operations in the shaded boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

**Remark** When the μPD753017A is set in the Mk I mode, $PC_{14}$ is fixed to 0.

| Instruction Group | Mnemonic | Operand | Number of Bytes | Number of Machine Cycles | Operation | Addressing Area | Skip Condition |
|---|---|---|---|---|---|---|---|
| Subroutine stack control | PUSH | rp | 1 | 1 | (SP–1)(SP–2) ← rp, SP ← SP–2 | | |
| | | BS | 2 | 2 | (SP–1) ← MBS, (SP–2) ← RBS, SP ← SP–2 | | |
| | POP | rp | 1 | 1 | rp ← (SP+1)(SP), SP ← SP+2 | | |
| | | BS | 2 | 2 | MBS ← (SP+1), RBS ← (SP), SP ← SP+2 | | |
| Interrupt control | EI | | 2 | 2 | IME(IPS.3) ← 1 | | |
| | | IEXXX | 2 | 2 | IEXXX ← 1 | | |
| | DI | | 2 | 2 | IME(IPS.3) ← 0 | | |
| | | IEXXX | 2 | 2 | IEXXX ← 0 | | |
| Input/output | IN Note 1 | A, PORTn | 2 | 2 | A ← PORTn (n = 0-7) | | |
| | | XA, PORTn | 2 | 2 | XA ← PORTn+1, PORTn (n = 4, 6) | | |
| | OUT Note 1 | PORTn, A | 2 | 2 | PORTn ← A (n = 2-7) | | |
| | | PORTn, XA | 2 | 2 | PORTn+1, PORTn ← XA (n = 4, 6) | | |
| CPU control | HALT | | 2 | 2 | Set HALT mode (PCC.2 ← 1) | | |
| | STOP | | 2 | 2 | Set STOP mode (PCC.3 ← 1) | | |
| | NOP | | 1 | 1 | No operation | | |
| Special | SEL | RBn | 2 | 2 | RBS ← n (n = 0-3) | | |
| | | MBn | 2 | 2 | MBS ← n (n = 0-3, 15) | | |
| | GETI Notes 2, 3 | taddr | 1 | 3 | • When TBR instruction<br>$PC_{13-0}$ ← (taddr)$_{5-0}$+(taddr+1) | *10 | |
| | | | | | • When TCALL instruction<br>(SP–4)(SP–1)(SP–2) ← $PC_{11-0}$<br>(SP–3) ← MBE, RBE, $PC_{13}$, $PC_{12}$<br>$PC_{13-0}$ ← (taddr)$_{5-0}$+(taddr+1)<br>SP ← SP–4 | | |
| | | | | | • When instruction other than TBR and TCALL instructions<br>(taddr) (taddr+1) instruction is executed | | Depending on the reference instruction |
| | | | 1 | 3 | ● μPD753017A<br>• When TBR instruction<br>$PC_{13-0}$ ← (taddr)$_{5-0}$+(taddr+1)<br>$PC_{14}$ ← 0 | | |
| | | | | 4 | • When TCALL instruction<br>(SP–6)(SP–3)(SP–4) ← $PC_{11-0}$<br>(SP–5) ← 0, 0, $PC_{13, 12}$<br>(SP–2) ← ×, ×, MBE, RBE<br>$PC_{13-0}$ ← (taddr)$_{5-0}$+(taddr+1)<br>SP ← SP–6, $PC_{14}$ ← 0 | | |
| | | | | 3 | • When instruction other than TBR and TCALL instructions<br>(taddr) (taddr+1) instruction is executed | | Depending on the reference instruction |

**Notes 1.** While the IN instruction and OUT instruction are being executed, the MBE must be set to 0 or 1 and MBS must be set to 15.

**2.** The above operations in the shaded boxes can be performed only in the Mk II mode. The other operations can be performed only in the Mk I mode.

**3.** The TBR and TCALL instructions are the table definition assembler pseudo instructions of the GETI instruction.

**Remark** When the μPD753017A is set in the Mk I mode, $PC_{14}$ is fixed to 0.

## 12. ELECTRICAL SPECIFICATIONS

### Absolute Maximum Ratings ($T_A$ = 25°C)

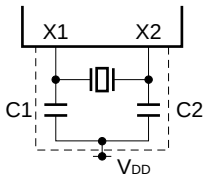
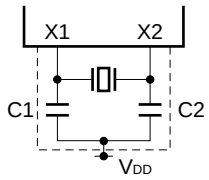
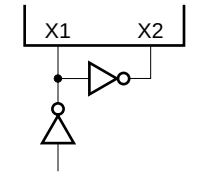
| Parameter | Symbol | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | | –0.3 to +7.0 | V |
| Input voltage | $V_{I1}$ | Other than ports 4, 5 | | –0.3 to $V_{DD}$ + 0.3 | V |
| | $V_{I2}$ | Ports | Pull-up resistor provided | –0.3 to $V_{DD}$ + 0.3 | V |
| | | 4, 5 | N-ch open-drain | –0.3 to +14 | V |
| Output voltage | $V_O$ | | | –0.3 to $V_{DD}$ + 0.3 | V |
| High-level output current | $I_{OH}$ | Per pin | | –10 | mA |
| | | Total of all pins | | –30 | mA |
| Low-level output current | $I_{OL}$ | Per pin | | 30 | mA |
| | | Total of all pins | | 220 | mA |
| Operating ambient temperature | $T_A$ | | | –40 to +85 | °C |
| Storage temperature | $T_{stg}$ | | | –65 to +150 | °C |

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

### Capacitance ($T_A$ = 25°C, $V_{DD}$ = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | f = 1 MHz | | | 15 | pF |
| Output capacitance | $C_{OUT}$ | Unmeasured pins returned to 0 V | | | 15 | pF |
| I/O capacitance | $C_{IO}$ | | | | 15 | pF |

**Main System Clock Oscillator Characteristics ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Resonator | Recommended Circuit | Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Ceramic resonator |  | Oscillation frequency ($f_X$)Note 1 | | 1.0 | | 6.0Note 2 | MHz |
| | | Oscillation stabilization timeNote 3 | After $V_{DD}$ has reached MIN. value of oscillation voltage range | | | 4 | ms |
| Crystal resonator |  | Oscillation frequency ($f_X$)Note 1 | | 1.0 | | 6.0Note 2 | MHz |
| | | Oscillation stabilization timeNote 3 | $V_{DD}$ = 4.5 to 5.5 V | | | 10 | ms |
| | | | | | | 30 | |
| External clock |  | X1 input frequency ($f_X$)Note 1 | | 1.0 | | 6.0Note 2 | MHz |
| | | X1 input high-, low-level width ($t_{XH}$, $t_{XL}$) | | 83.3 | | 500 | ns |

**Notes 1.** The oscillation frequency and X1 input frequency shown above indicate characteristics of the oscillator only. For the instruction execution time, refer to **AC Characteristics**.

**2.** If the oscillation frequency is 4.19 MHz < $f_X$ ≤ 6.0 MHz at 1.8 V ≤ $V_{DD}$ < 2.7 V, do not set the processor clock control register (PCC) to 0011. If PCC = 0011, one machine cycle time is less than 0.95 μs, falling short of the rated value of 0.95 μs.

**3.** The oscillation stabilization time is the time required for oscillation to be stabilized after $V_{DD}$ has been applied or STOP mode has been released.

**Caution When using the main system clock oscillator, wire the portion enclosed in the dotted line in the above figure as follows to prevent adverse influence due to wiring capacitance:**

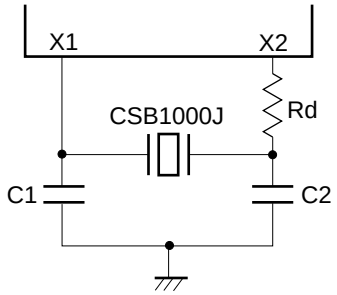
- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with other signal lines.**
- **Do not route the wiring in the vicinity of a line through which a high alternating current flows.**
- **Always keep the ground point of the capacitor of the oscillator at the same potential as $V_{DD}$.**
- **Do not ground to a power supply pattern through which a high current flows.**
- **Do not extract signals from the oscillator.**

**Recommended Oscillator Constant**

**Ceramic resonator ($T_A$ = –20 to +80°C)**

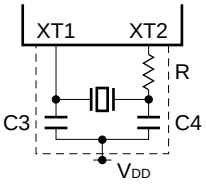
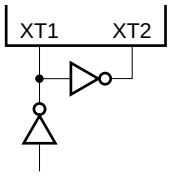
| Manufacturer | Part Number | Frequency (MHz) | Recommended Circuit Constant (pF) | | Oscillation Voltage Range (V) | | Remarks |
|---|---|---|---|---|---|---|---|
| | | | C1 | C2 | MIN. | MAX. | |
| TDK Corp. | CCR1000K2 | 1.0 | 100 | 100 | 1.8 | 5.5 | – |
| | CCR2.0MC33 | 2.0 | – | – | | | On-chip capacitor |
| | CCR4.19MC3 | 4.19 | | | | | |
| | FCR4.19MC5 | | | | | | |
| | CCR6.0MC3 | 6.0 | | | | | |
| Murata Mfg. Co., Ltd. | CSB1000J[Note] | 1.0 | 100 | 100 | 2.1 | 5.5 | Rd = 5.6 kΩ |
| | CSA2.00MG040 | 2.0 | 100 | 100 | 1.9 | | – |
| | CST2.00MG040 | | – | – | | | On-chip capacitor |
| | CSA4.19MG | 4.19 | 30 | 30 | 1.8 | | – |
| | CST4.19MGW | | – | – | | | On-chip capacitor |
| | CSA6.00MG | 6.0 | 30 | 30 | 2.3 | | – |
| | CST6.00MGW | | – | – | | | On-chip capacitor |
| Kyocera Corp. | KBR-1000F/Y | 1.0 | 100 | 100 | 1.8 | 5.5 | – |
| | KBR-2.0MS | 2.0 | 68 | 68 | | | |
| | KBR-4.0MSA/MSB | 4.0 | 33 | 33 | | | |
| | KBR-4.0MKC | | – | – | | | On-chip capacitor |
| | KBR-4.0MKD | | | | | | |
| | KBR-4.0MKS | | | | | | |
| | PBRC4.00A | 4.0 | 33 | 33 | | | – |
| | PBRC4.00B | | – | – | | | On-chip capacitor |
| | KBR-4.19MSA | 4.19 | 33 | 33 | | | – |
| | KBR-4.19MSB | | 33 | 33 | | | |
| | KBR-4.19MKC | | – | – | | | On-chip capacitor |
| | KBR-4.19MKD | | | | | | |
| | KBR-4.19MKS | | | | | | |
| | PBRC4.19A | | 33 | 33 | | | – |
| | PBRC4.19B | | – | – | | | On-chip capacitor |
| | KBR-6.0MSA/MSB | 6.0 | 33 | 33 | | | – |
| | KBR-6.0MKC | | – | – | | | On-chip capacitor |
| | KBR-6.0MKD | | | | | | |
| | KBR-6.0MKS | | | | | | |
| | PBRC6.00A | | 33 | 33 | | | – |
| | PBRC6.00B | | – | – | | | On-chip capacitor |

**Note** When using the CSB1000J (1.0 MHz) by Murata Mfg. Co., Ltd. as a ceramic resonator, a limiting resistor (Rd = 5.6 kΩ) is necessary (refer to the figure below). The resistor is not necessary when using the other recommended resonators.




**Caution The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. Oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation frequency must be adjusted on the implementation circuit. For details, please contact directly the manufacturer of the resonator you will use.**

**Subsystem Clock Oscillator Characteristics ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Resonator | Recommended Circuit | Parameter | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Crystal resonator |  | Oscillation frequency ($f_{XT}$)Note 1 | | 32 | 32.768 | 35 | kHz |
| | | Oscillation stabilization timeNote 2 | $V_{DD}$ = 4.5 to 5.5 V | | 1.0 | 2 | s |
| | | | | | | 10 | |
| External clock |  | XT1 input frequency ($f_{XT}$)Note 1 | | 32 | | 100 | kHz |
| | | XT1 input high-, low-level width ($t_{XTH}$, $t_{XTL}$) | | 5 | | 15 | μs |

**Notes 1.** The oscillation frequency shown above indicates characteristics of the oscillator only. For the instruction execution time, refer to **AC Characteristics**.

**2.** The oscillation stabilization time is the time required for oscillation to be stabilized after $V_{DD}$ has been applied.

**Caution When using the subsystem clock oscillator, wire the portion enclosed in the dotted line in the above figure as follows to prevent adverse influence due to wiring capacitance:**

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with other signal lines.**
- **Do not route the wiring in the vicinity of a line through which a high alternating current flows.**
- **Always keep the ground point of the capacitor of the oscillator at the same potential as $V_{DD}$.**
- **Do not ground to a power supply pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

**The subsystem clock oscillator has a low amplification factor to reduce current consumption and is more susceptible to noise than the main system clock oscillator. Therefore, exercise utmost care in wiring the subsystem clock oscillator.**

★ **Remark** For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

**DC Characteristics ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Low-level output current | $I_{OL}$ | Per pin | | | | | 15 | mA |
| | | Total of all pins | | | | | 150 | mA |
| High-level input voltage | $V_{IH1}$ | Ports 2, 3 | | $V_{DD}$ = 2.7 to 5.5 V | 0.7 $V_{DD}$ | | $V_{DD}$ | V |
| | | | | $V_{DD}$ = 1.8 to 2.7 V | 0.9 $V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH2}$ | Ports 0, 1, 6, 7, $\overline{RESET}$ | | $V_{DD}$ = 2.7 to 5.5 V | 0.8 $V_{DD}$ | | $V_{DD}$ | V |
| | | | | $V_{DD}$ = 1.8 to 2.7 V | 0.9 $V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH3}$ | Ports 4, 5 | Pull-up resistor provided | $V_{DD}$ = 2.7 to 5.5 V | 0.7 $V_{DD}$ | | $V_{DD}$ | V |
| | | | | $V_{DD}$ = 1.8 to 2.7 V | 0.9 $V_{DD}$ | | $V_{DD}$ | V |
| | | | N-ch open-drain | $V_{DD}$ = 2.7 to 5.5 V | 0.7 $V_{DD}$ | | 13 | V |
| | | | | $V_{DD}$ = 1.8 to 2.7 V | 0.9 $V_{DD}$ | | 13 | V |
| | $V_{IH4}$ | X1, XT1 | | | $V_{DD}$–0.1 | | $V_{DD}$ | V |
| Low-level input voltage | $V_{IL1}$ | Ports 2, 3, 4, 5 | | $V_{DD}$ = 2.7 to 5.5 V | 0 | | 0.3 $V_{DD}$ | V |
| | | | | $V_{DD}$ = 1.8 to 2.7 V | 0 | | 0.1 $V_{DD}$ | V |
| | $V_{IL2}$ | Ports 0, 1, 6, 7, $\overline{RESET}$ | | $V_{DD}$ = 2.7 to 5.5 V | 0 | | 0.2 $V_{DD}$ | V |
| | | | | $V_{DD}$ = 1.8 to 2.7 V | 0 | | 0.1 $V_{DD}$ | V |
| | $V_{IL3}$ | X1, XT1 | | | 0 | | 0.1 | V |
| High-level output voltage | $V_{OH}$ | $\overline{SCK}$, SO, Ports 2, 3, 6, 7, BP0-BP7 $I_{OH}$ = –1 mA | | | $V_{DD}$–0.5 | | | V |
| Low-level output voltage | $V_{OL1}$ | $\overline{SCK}$, SO, Ports 2-7, BP0-BP7 | | $I_{OL}$ = 15 mA, $V_{DD}$ = 5.0 V ±10% | | 0.2 | 2.0 | V |
| | | | | $I_{OL}$ = 1.6 mA | | | 0.4 | V |
| | $V_{OL2}$ | SB0, SB1 | N-ch open-drain, Pull-up resistor ≥ 1 kΩ | | | | 0.2 $V_{DD}$ | V |
| High-level input leakage current | $I_{LIH1}$ | $V_{IN}$ = $V_{DD}$ | Pins other than X1, XT1, ports 4, 5 | | | | 3 | μA |
| | $I_{LIH2}$ | | X1, XT1 | | | | 20 | μA |
| | $I_{LIH3}$ | $V_{IN}$ = 13 V | Ports 4, 5 (N-ch open-drain) | | | | 20 | μA |
| Low-level input leakage current | $I_{LIL1}$ | $V_{IN}$ = 0 V | Pins other than X1, XT1, ports 4, 5 | | | | –3 | μA |
| | $I_{LIL2}$ | | X1, XT1 | | | | –20 | μA |
| | $I_{LIL3}$ | | Ports 4, 5 (N-ch open-drain) When input instruction is not executed | | | | –3 | μA |
| | | | Ports 4, 5 (N-ch open-drain) When input instruction is executed | | | | –30 | μA |
| | | | | $V_{DD}$ = 5 V | | –10 | –27 | μA |
| | | | | $V_{DD}$ = 3 V | | –3 | –8 | μA |
| High-level output leakage current | $I_{LOH1}$ | $V_{OUT}$ = $V_{DD}$ | $\overline{SCK}$, SO/SB0, SB1, ports 2, 3, 6, 7, ports 4, 5 (pull-up resistor provided), BP0-BP7 | | | | 3 | μA |
| | $I_{LOH2}$ | $V_{OUT}$ = 13 V | Ports 4, 5 (N-ch open-drain) | | | | 20 | μA |
| Low-level output leakage current | $I_{LOL}$ | $V_{OUT}$ = 0 V | | | | | –3 | μA |
| Internal pull-up resistor ★ | $R_{L1}$ | $V_{IN}$ = 0 V | Ports 0, 1, 2, 3, 6, 7 (except P00 pin) | | 50 | 100 | 200 | kΩ |
| | $R_{L2}$ | | Ports 4, 5 (mask option selected) | | 15 | 30 | 60 | kΩ |

**DC Characteristics ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| LCD drive voltage[Note 1] | $V_{LCD}$ | VAC0 = 0 | | | 2.2 | | $V_{DD}$ | V |
| | | VAC0 = 1 | | | 1.8 | | $V_{DD}$ | V |
| VAC current[Note 2] | $I_{VAC}$ | VAC0 = 1, $V_{DD}$ = 2.0 V ±10% | | | | 1 | 4 | μA |
| LCD split resistor[Note 3] | $R_{LCD1}$ | | | | 50 | 100 | 200 | kΩ |
| | $R_{LCD2}$ | | | | 5 | 10 | 20 | kΩ |
| LCD output voltage deviation[Note 4] (common) | $V_{ODC}$ | $I_O$ = ±1.0 μA | $V_{LCD0} = V_{LCD}$<br>$V_{LCD1} = V_{LCD} \times 2/3$<br>$V_{LCD2} = V_{LCD} \times 1/3$ | | 0 | | ±0.2 | V |
| LCD output voltage deviation[Note 4] (segment) | $V_{ODS}$ | $I_O$ = ±0.5 μA | 1.8 V ≤ $V_{LCD}$ ≤ $V_{DD}$ | | 0 | | ±0.2 | V |
| Supply current[Notes 2, 5] | $I_{DD1}$ | 6.00 MHz[Note 6] crystal oscillation C1 = C2 = 22 pF | $V_{DD}$ = 5.0 V ±10%[Note 7] | | | 2.2 | 6.6 | mA |
| | | | $V_{DD}$ = 3.0 V ±10%[Note 8] | | | 0.6 | 2.0 | mA |
| | $I_{DD2}$ | | HALT mode | $V_{DD}$ = 5.0 V ±10% | | 0.72 | 2.1 | mA |
| | | | | $V_{DD}$ = 3.0 V ±10% | | 0.27 | 0.8 | mA |
| | $I_{DD1}$ | 4.19 MHz[Note 6] crystal oscillation C1 = C2 = 22 pF | $V_{DD}$ = 5.0 V ±10%[Note 7] | | | 1.7 | 5.1 | mA |
| | | | $V_{DD}$ = 3.0 V ±10%[Note 8] | | | 0.3 | 0.9 | mA |
| | $I_{DD2}$ | | HALT mode | $V_{DD}$ = 5.0 V ±10% | | 0.7 | 2.0 | mA |
| | | | | $V_{DD}$ = 3.0 V ±10% | | 0.23 | 0.7 | mA |
| | $I_{DD3}$ | 32.768 kHz[Note 9] crystal oscillation | Low voltage mode[Note 10] | $V_{DD}$ = 3.0 V ±10% | | 15 | 45 | μA |
| | | | | $V_{DD}$ = 2.0 V ±10% | | 8 | 24 | μA |
| | | | | $V_{DD}$ = 3.0 V, $T_A$ = 25°C | | 15 | 30 | μA |
| | | | Low current consumption mode[Note 11] | $V_{DD}$ = 3.0 V ±10% | | 12 | 36 | μA |
| | | | | $V_{DD}$ = 3.0 V, $T_A$ = 25°C | | 12 | 24 | μA |
| | $I_{DD4}$ | | HALT mode | Low voltage mode[Note 10] | $V_{DD}$ = 3.0 V ±10% | 8.5 | 25 | μA |
| | | | | | $V_{DD}$ = 2.0 V ±10% | 4 | 12 | μA |
| | | | | | $V_{DD}$ = 3.0 V, $T_A$ = 25°C | 8.5 | 17 | μA |
| | | | | Low current consumption mode[Note 11] | $V_{DD}$ = 3.0 V ±10% | 3.5 | 12 | μA |
| | | | | | $V_{DD}$ = 3.0 V, $T_A$ = 25°C | 3.5 | 7 | μA |
| | $I_{DD5}$ | XT1 = 0 V[Note 12] STOP mode | $V_{DD}$ = 5.0 V ±10% | | | 0.05 | 10 | μA |
| | | | $V_{DD}$ = 3.0 V ±10% | | | 0.02 | 5 | μA |
| | | | | $T_A$ = 25°C | | 0.02 | 3 | μA |

**Notes 1.** When 1.8 V ≤ $V_{DD}$ < 2.7 V, $T_A$ = –10 to +85°C.

**2.** Clear VAC0 to 0 in the low current consumption mode and STOP mode. When VAC0 is set to 1, the current increases by about 1 μA.

**3.** Either $R_{LCD1}$ or $R_{LCD2}$ can be selected by mask option.

**4.** Voltage deviation is the difference between the ideal values ($V_{LCDn}$; n = 0, 1, 2) of the segment and common outputs and the output voltage.

**5.** The current flowing through the internal pull-up resistor and the LCD divider resistor is not included.

**6.** Including the case when the subsystem clock oscillates.

**7.** When the device operates in high-speed mode with the processor clock control register (PCC) set to 0011.

**8.** When the device operates in low-speed mode with PCC set to 0000.

**9.** When the device operates on the subsystem clock, with the system clock control register (SCC) set to 1001 and oscillation of the main system clock stopped.

**10.** When the sub-oscillator control register (SOS) is set to 0000.

**11.** When SOS is set to 0010.

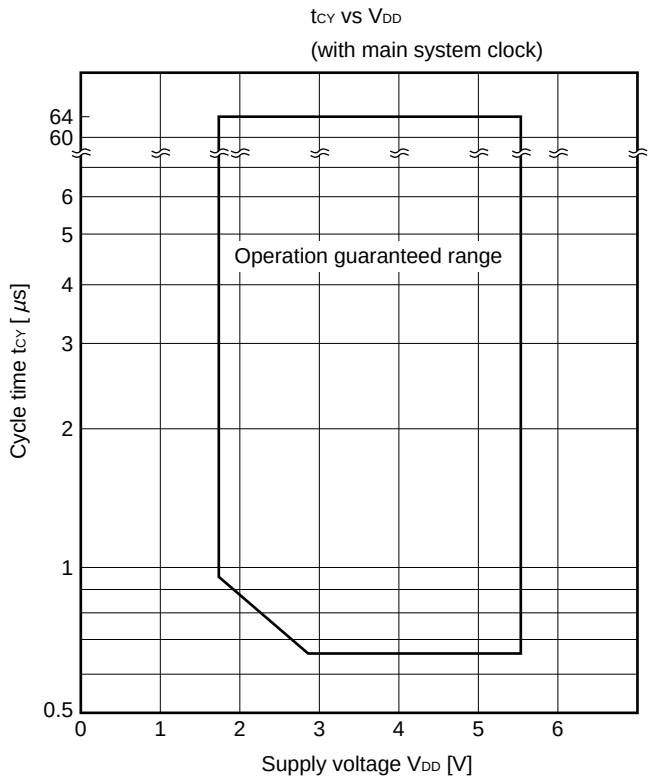
**12.** When SOS is set to 00X1, and the feedback resistor of the sub-oscillator is not used (X: don't care).

**AC Characteristics ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| CPU clock cycle time[Note 1] (minimum instruction execution time = 1 machine cycle) | $t_{CY}$ | Operates with main system clock | $V_{DD}$ = 2.7 to 5.5 V | 0.67 | | 64 | μs |
| | | | | 0.95 | | 64 | μs |
| | | Operates with subsystem clock | | 114 | 122 | 125 | μs |
| TI0, TI1, TI2 input frequency | $f_{TI}$ | $V_{DD}$ = 2.7 to 5.5 V | | 0 | | 1 | MHz |
| | | | | 0 | | 275 | kHz |
| TI0, TI1, TI2 input high-, low-level width | $t_{TIH}$, $t_{TIL}$ | $V_{DD}$ = 2.7 to 5.5 V | | 0.48 | | | μs |
| | | | | 1.8 | | | μs |
| Interrupt input high-, low-level width | $t_{INTH}$, $t_{INTL}$ | INT0 | IM02 = 0 | **Note 2** | | | μs |
| | | | IM02 = 1 | 10 | | | μs |
| | | INT1, 2, 4 | | 10 | | | μs |
| | | KR0-KR7 | | 10 | | | μs |
| $\overline{\text{RESET}}$ low-level width | $t_{RSL}$ | | | 10 | | | μs |

**Notes 1.** The cycle time of the CPU clock (Φ) is determined by the oscillation frequency of the connected resonator, the system clock control register (SCC), and processor clock control register (PCC). The figure on the right shows the supply voltage $V_{DD}$ vs. cycle time $t_{CY}$ characteristics when the device operates with the main system clock.

**2.** $2t_{CY}$ or $128/f_X$ depending on the setting of the interrupt mode register (IM0).



### Serial transfer operation

**2-wire and 3-wire serial I/O modes ($\overline{SCK}$ ··· internal clock output): ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK}$ cycle time | $t_{KCY1}$ | $V_{DD}$ = 2.7 to 5.5 V | | 1300 | | | ns |
| | | | | 3800 | | | ns |
| $\overline{SCK}$ high-, low-level width | $t_{KL1}$ | $V_{DD}$ = 2.7 to 5.5 V | | $t_{KCY1}$/2–50 | | | ns |
| | $t_{KH1}$ | | | $t_{KCY1}$/2–150 | | | ns |
| SI[Note 1] setup time | $t_{SIK1}$ | $V_{DD}$ = 2.7 to 5.5 V | | 150 | | | ns |
| (to $\overline{SCK}$ ↑) | | | | 500 | | | ns |
| SI[Note 1] hold time | $t_{KSI1}$ | $V_{DD}$ = 2.7 to 5.5 V | | 400 | | | ns |
| (from $\overline{SCK}$ ↑) | | | | 600 | | | ns |
| $\overline{SCK}$ ↓ → SO[Note 1] | $t_{KSO1}$ | $R_L$ = 1 kΩ, [Note 2] | $V_{DD}$ = 2.7 to 5.5 V | 0 | | 250 | ns |
| output delay time | | $C_L$ = 100 pF | | 0 | | 1000 | ns |

**Notes 1.** Read as SB0 or SB1 when using the 2-wire serial I/O mode.

**2.** $R_L$ and $C_L$ respectively indicate the load resistance and load capacitance of the SO output line.

**2-wire and 3-wire serial I/O modes ($\overline{SCK}$ ··· external clock input): ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK}$ cycle time | $t_{KCY2}$ | $V_{DD}$ = 2.7 to 5.5 V | | 800 | | | ns |
| | | | | 3200 | | | ns |
| $\overline{SCK}$ high-, low-level width | $t_{KL2}$ | $V_{DD}$ = 2.7 to 5.5 V | | 400 | | | ns |
| | $t_{KH2}$ | | | 1600 | | | ns |
| SI[Note 1] setup time | $t_{SIK2}$ | $V_{DD}$ = 2.7 to 5.5 V | | 100 | | | ns |
| (to $\overline{SCK}$ ↑) | | | | 150 | | | ns |
| SI[Note 1] hold time | $t_{KSI2}$ | $V_{DD}$ = 2.7 to 5.5 V | | 400 | | | ns |
| (from $\overline{SCK}$ ↑) | | | | 600 | | | ns |
| $\overline{SCK}$ ↓ → SO[Note 1] | $t_{KSO2}$ | $R_L$ = 1 kΩ, [Note 2] | $V_{DD}$ = 2.7 to 5.5 V | 0 | | 300 | ns |
| output delay time | | $C_L$ = 100 pF | | 0 | | 1000 | ns |

**Notes 1.** Read as SB0 or SB1 when using the 2-wire serial I/O mode.

**2.** $R_L$ and $C_L$ respectively indicate the load resistance and load capacitance of the SO output line.

**SBI mode ($\overline{SCK}$ ··· internal clock output (master)): ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK}$ cycle time | $t_{KCY3}$ | $V_{DD}$ = 2.7 to 5.5 V | | 1300 | | | ns |
| | | | | 3800 | | | ns |
| $\overline{SCK}$ high-, low-level width | $t_{KL3}$ | $V_{DD}$ = 2.7 to 5.5 V | | $t_{KCY3}$/2–50 | | | ns |
| | $t_{KH3}$ | | | $t_{KCY3}$/2–150 | | | ns |
| SB0, 1 setup time (to $\overline{SCK}$ ↑) | $t_{SIK3}$ | $V_{DD}$ = 2.7 to 5.5 V | | 150 | | | ns |
| | | | | 500 | | | ns |
| SB0, 1 hold time (from $\overline{SCK}$ ↑) | $t_{KSI3}$ | | | $t_{KCY3}$/2 | | | ns |
| $\overline{SCK}$ ↓ → SB0, 1 output delay time | $t_{KSO3}$ | $R_L$ = 1 kΩ, $C_L$ = 100 pF | Note $V_{DD}$ = 2.7 to 5.5 V | 0 | | 250 | ns |
| | | | | 0 | | 1000 | ns |
| $\overline{SCK}$ ↑ → SB0, 1 ↓ | $t_{KSB}$ | | | $t_{KCY3}$ | | | ns |
| SB0, 1 ↓ → $\overline{SCK}$ ↓ | $t_{SBK}$ | | | $t_{KCY3}$ | | | ns |
| SB0, 1 low-level width | $t_{SBL}$ | | | $t_{KCY3}$ | | | ns |
| SB0, 1 high-level width | $t_{SBH}$ | | | $t_{KCY3}$ | | | ns |

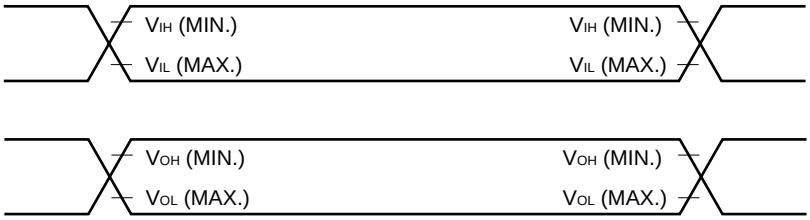
**Note** $R_L$ and $C_L$ respectively indicate the load resistance and load capacitance of the SB0, 1 output line.

**SBI mode ($\overline{SCK}$ ··· external clock input (slave)): ($T_A$ = –40 to +85°C, $V_{DD}$ = 1.8 to 5.5 V)**

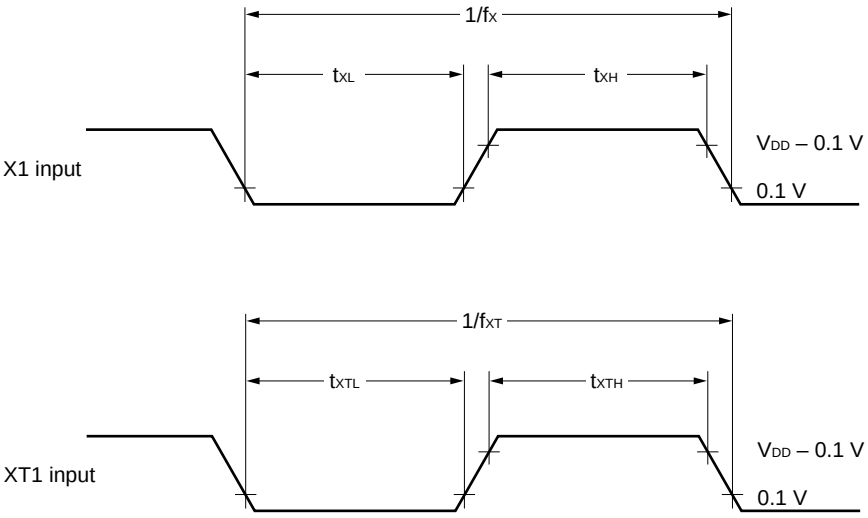
| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{SCK}$ cycle time | $t_{KCY4}$ | $V_{DD}$ = 2.7 to 5.5 V | | 800 | | | ns |
| | | | | 3200 | | | ns |
| $\overline{SCK}$ high-, low-level width | $t_{KL4}$ | $V_{DD}$ = 2.7 to 5.5 V | | 400 | | | ns |
| | $t_{KH4}$ | | | 1600 | | | ns |
| SB0, 1 setup time (to $\overline{SCK}$ ↑) | $t_{SIK4}$ | $V_{DD}$ = 2.7 to 5.5 V | | 100 | | | ns |
| | | | | 150 | | | ns |
| SB0, 1 hold time (from $\overline{SCK}$ ↑) | $t_{KSI4}$ | | | $t_{KCY4}$/2 | | | ns |
| $\overline{SCK}$ ↓ → SB0, 1 output delay time | $t_{KSO4}$ | $R_L$ = 1 kΩ, $C_L$ = 100 pF | Note $V_{DD}$ = 2.7 to 5.5 V | 0 | | 300 | ns |
| | | | | 0 | | 1000 | ns |
| $\overline{SCK}$ ↑ → SB0, 1 ↓ | $t_{KSB}$ | | | $t_{KCY4}$ | | | ns |
| SB0, 1 ↓ → $\overline{SCK}$ ↓ | $t_{SBK}$ | | | $t_{KCY4}$ | | | ns |
| SB0, 1 low-level width | $t_{SBL}$ | | | $t_{KCY4}$ | | | ns |
| SB0, 1 high-level width | $t_{SBH}$ | | | $t_{KCY4}$ | | | ns |

**Note** $R_L$ and $C_L$ respectively indicate the load resistance and load capacitance of the SB0, 1 output line.

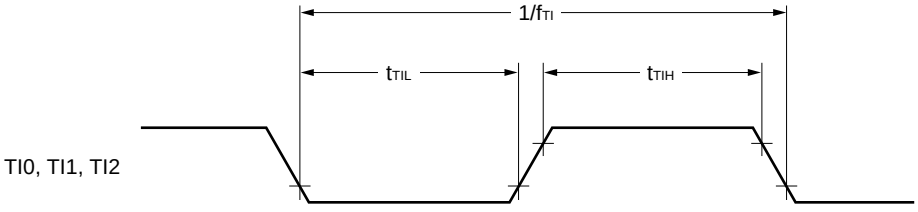
**AC timing test points (except X1 and XT1 inputs)**




**Clock timing**

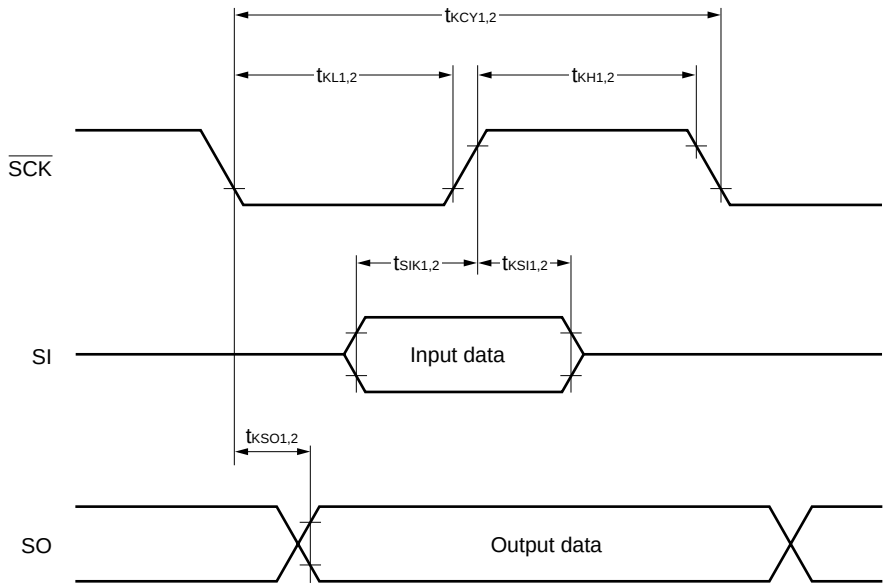



**TI0, TI1, TI2 timing**

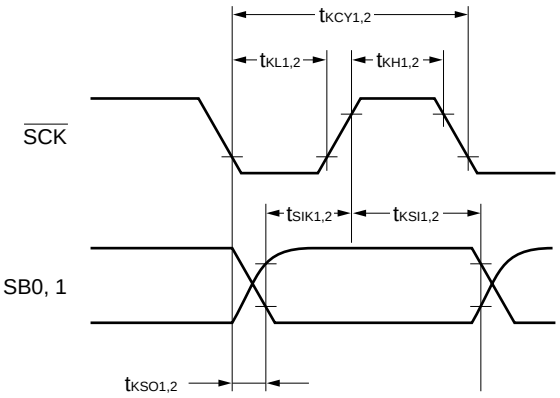


### Serial transfer timing

#### 3-wire serial I/O mode

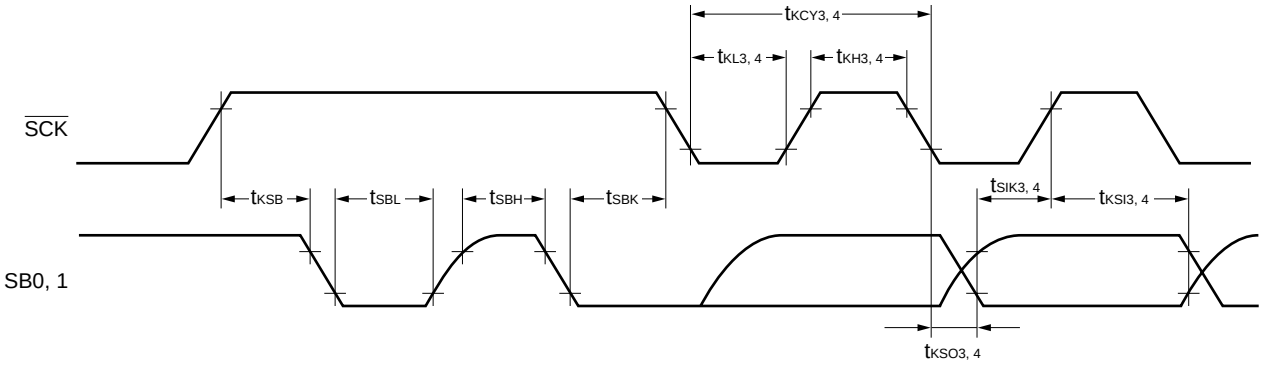



#### 2-wire serial I/O mode

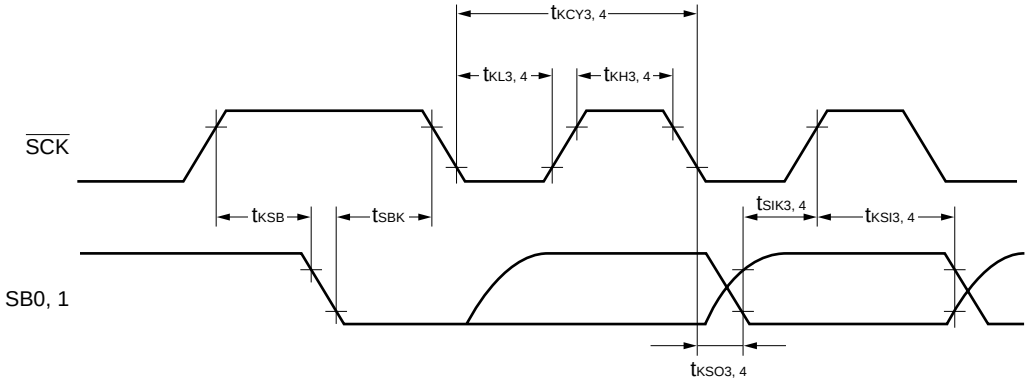


### Serial transfer timing

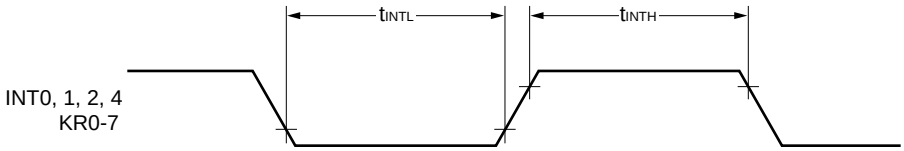
#### Bus release signal transfer



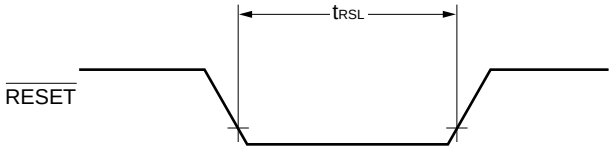

#### Command signal transfer




#### Interrupt input timing




#### RESET input timing



**Data retention characteristics of data memory in STOP mode and at low supply voltage ($T_A$ = –40 to +85°C)**

| | Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| ★ | Data retention power supply voltage | $V_{DDDR}$ | | 1.8 | | 5.5 | V |
| | Release signal setup time | $t_{SREL}$ | | 0 | | | μs |
| | Oscillation stabilization wait time[Note 1] | $t_{WAIT}$ | Released by $\overline{RESET}$ | | **Note 2** | | ms |
| | | | Released by interrupt request | | **Note 3** | | ms |

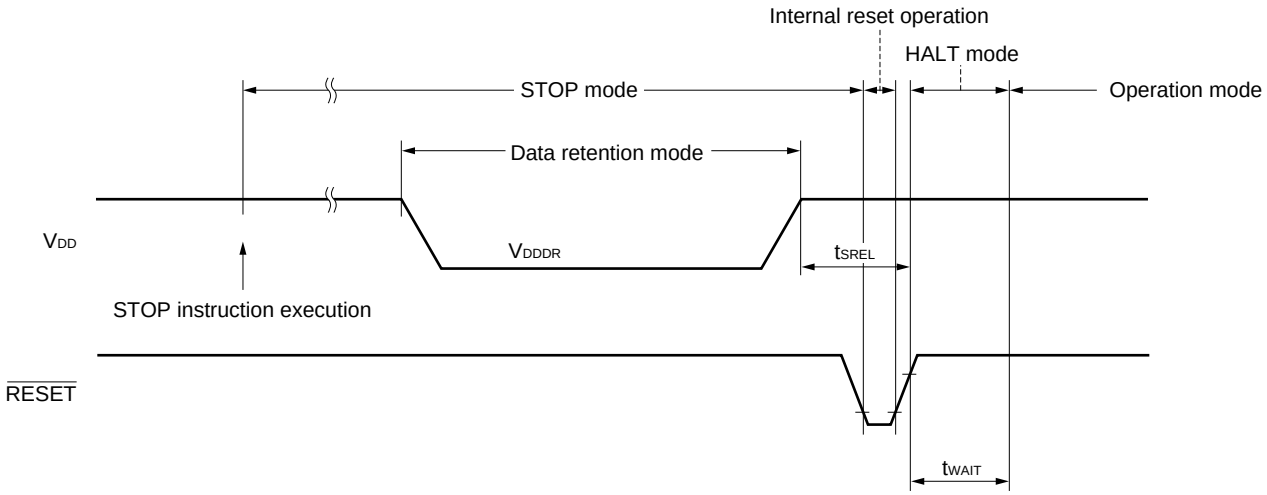
**Notes 1.** The oscillation stabilization wait time is the time during which the CPU stops operating to prevent unstable operation when oscillation is started.

**2.** Either $2^{17}/f_X$ or $2^{15}/f_X$ can be selected by mask option.

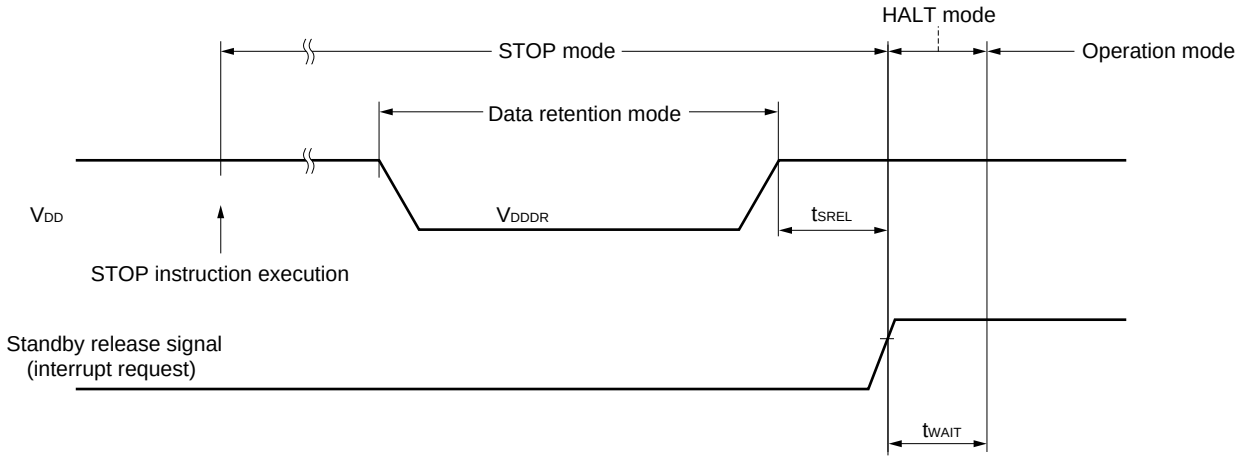
**3.** Set by the basic interval timer mode register (BTM). (Refer to the table below.)

| BTM3 | BTM2 | BTM1 | BTM0 | Wait Time | |
|---|---|---|---|---|---|
| | | | | $f_X$ = 4.19 MHz | $f_X$ = 6.0 MHz |
| – | 0 | 0 | 0 | $2^{20}/f_X$ (approx. 250 ms) | $2^{20}/f_X$ (approx. 175 ms) |
| – | 0 | 1 | 1 | $2^{17}/f_X$ (approx. 31.3 ms) | $2^{17}/f_X$ (approx. 21.8 ms) |
| – | 1 | 0 | 1 | $2^{15}/f_X$ (approx. 7.81 ms) | $2^{15}/f_X$ (approx. 5.46 ms) |
| – | 1 | 1 | 1 | $2^{13}/f_X$ (approx. 1.95 ms) | $2^{13}/f_X$ (approx. 1.37 ms) |

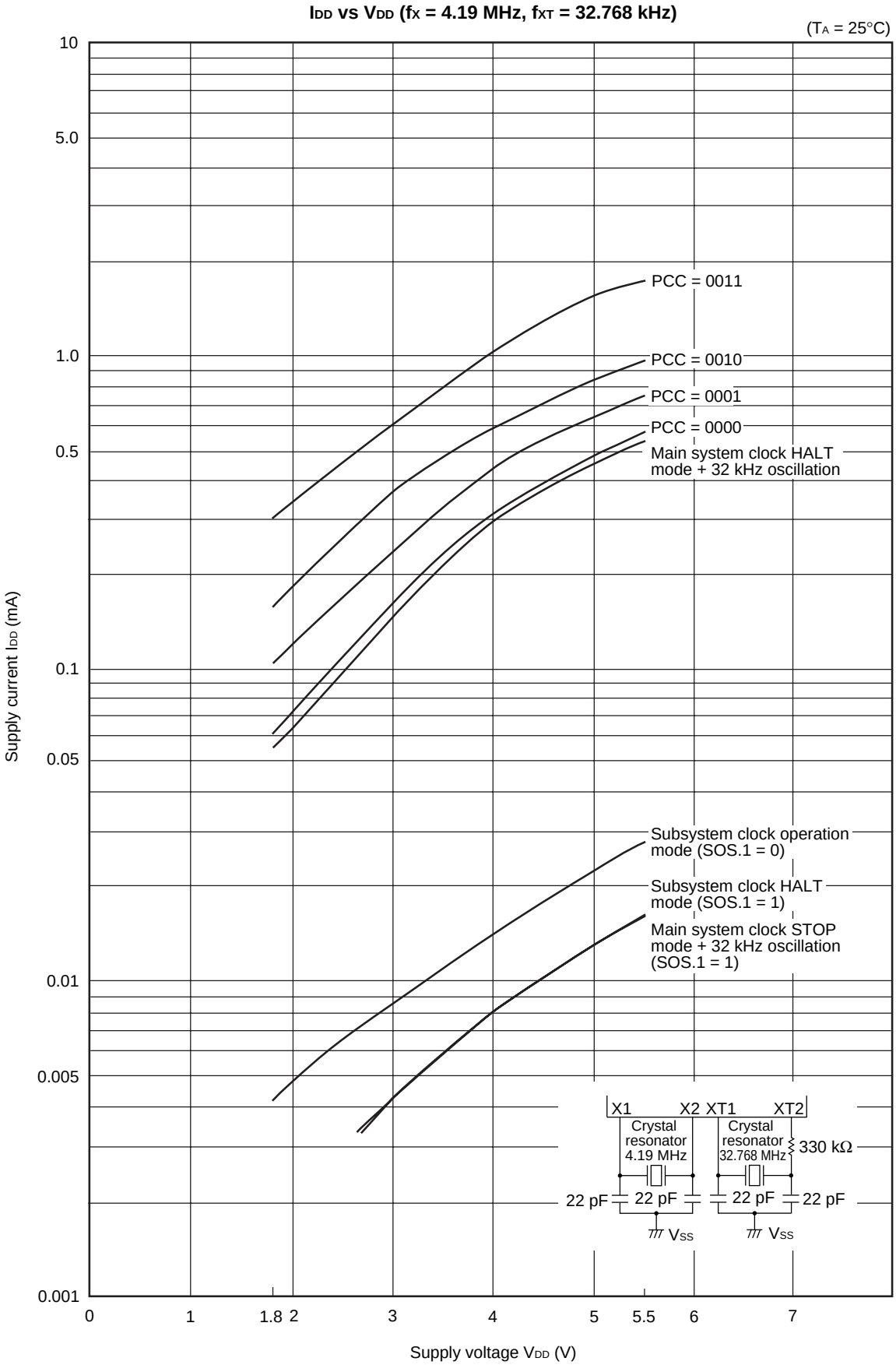
**Data retention timing (when STOP mode released by $\overline{RESET}$)**



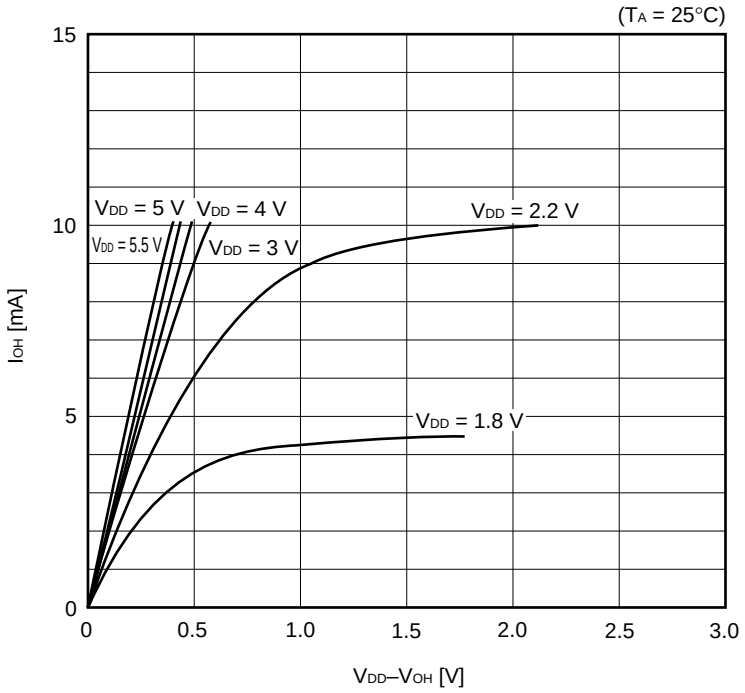

**Data retention timing (standby release signal: when STOP mode released by interrupt signal)**



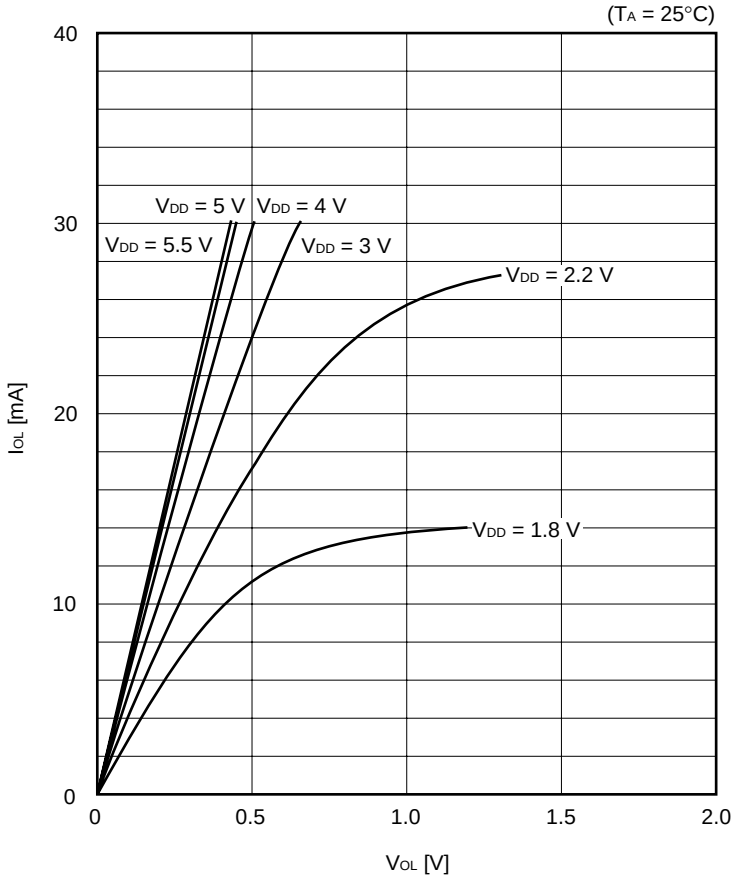
## ★ 13. CHARACTERISTICS CURVES (REFERENCE VALUES)



**$I_{OH}$ vs $V_{DD}$–$V_{OH}$ (Ports 2, 3, 6, 7)**

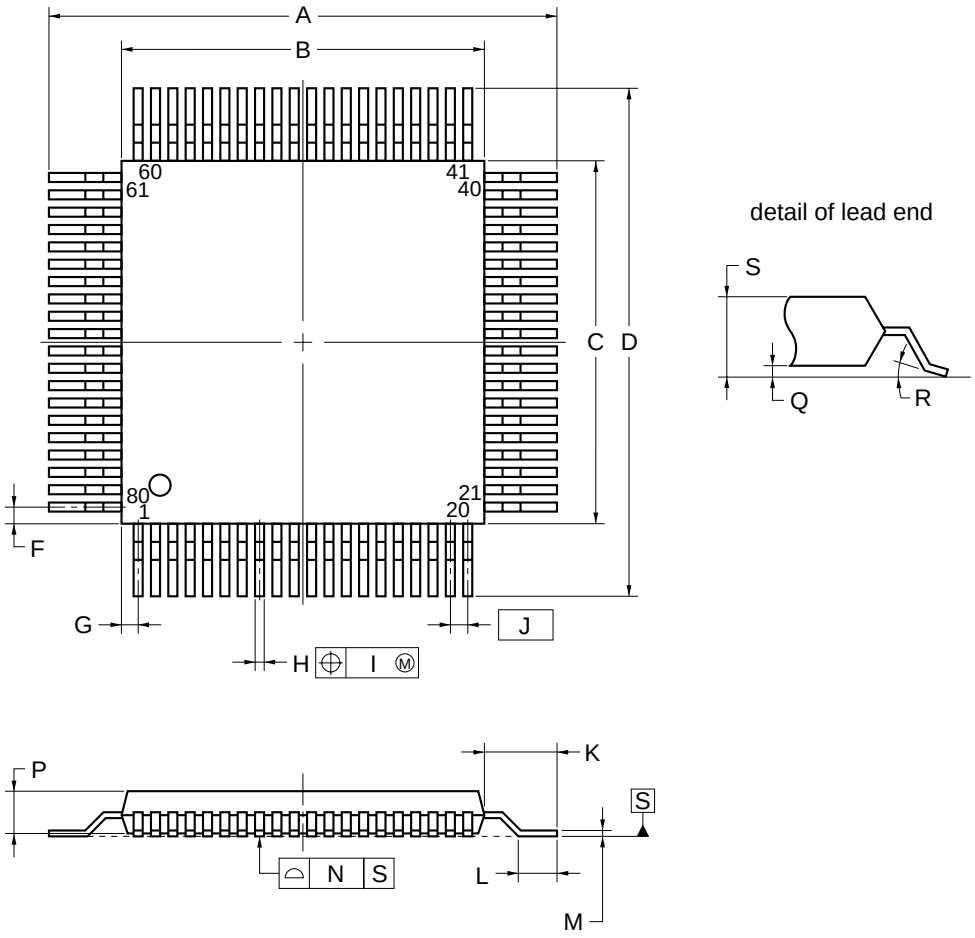



**$I_{OL}$ vs $V_{OL}$ (Ports 2, 3, 6, 7)**



## 14. PACKAGE DRAWINGS

### 80-PIN PLASTIC QFP (14x14)



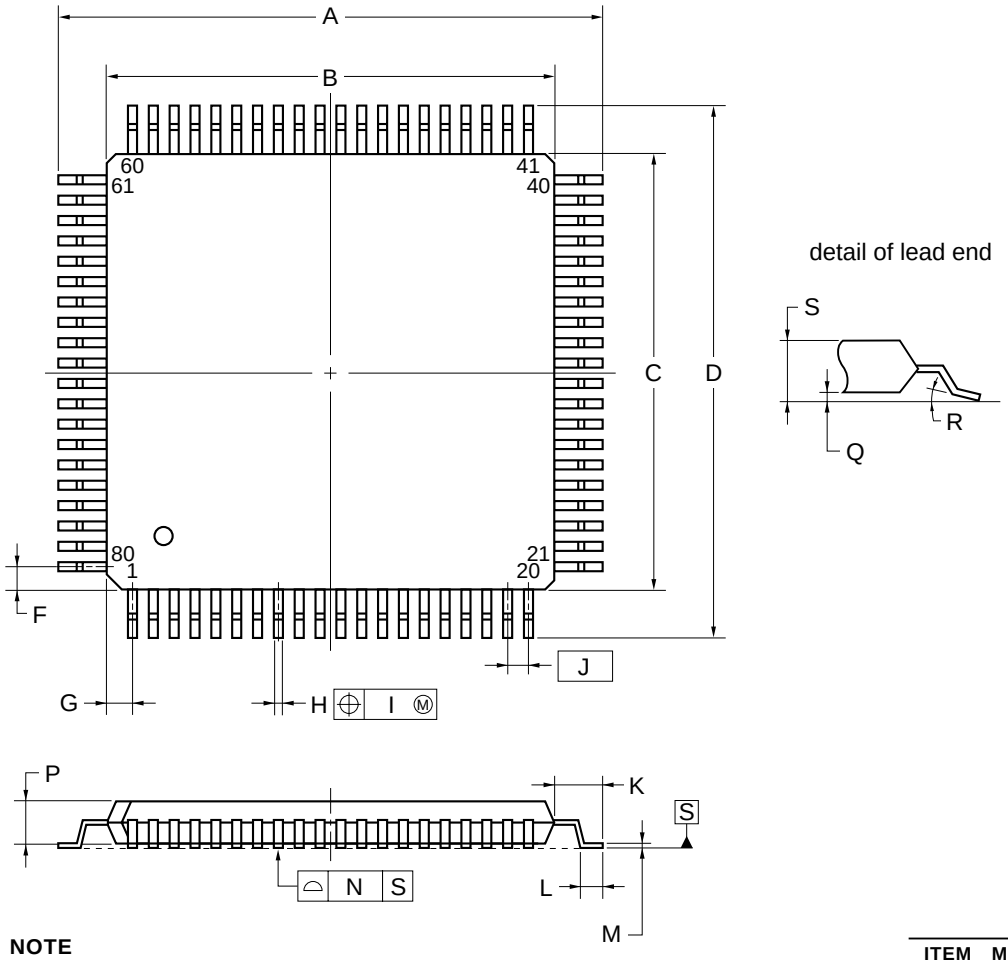

**NOTE**

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 17.2±0.4 |
| B | 14.0±0.2 |
| C | 14.0±0.2 |
| D | 17.2±0.4 |
| F | 0.825 |
| G | 0.825 |
| H | 0.30±0.10 |
| I | 0.13 |
| J | 0.65 (T.P.) |
| K | 1.6±0.2 |
| L | 0.8±0.2 |
| M | $0.15^{+0.10}_{-0.05}$ |
| N | 0.10 |
| P | 2.7±0.1 |
| Q | 0.1±0.1 |
| R | 5°±5° |
| S | 3.0 MAX. |

**S80GC-65-3B9-6**

## ★ 80-PIN PLASTIC QFP (14x14)



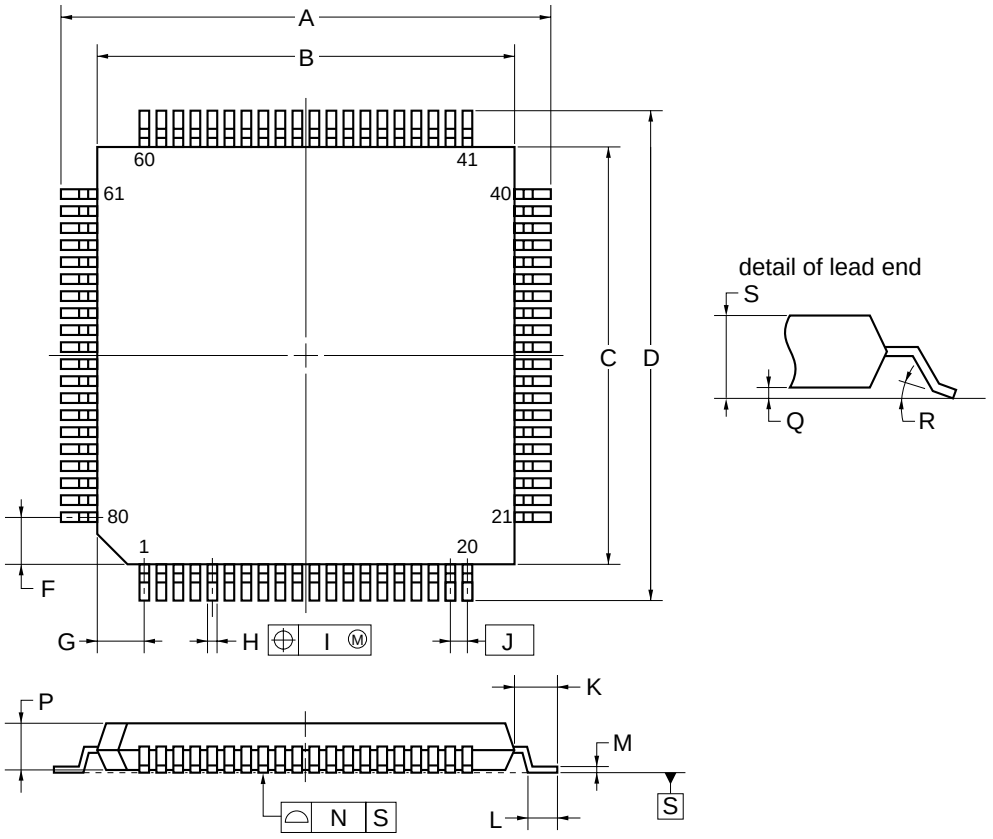

**NOTE**

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 17.20±0.20 |
| B | 14.00±0.20 |
| C | 14.00±0.20 |
| D | 17.20±0.20 |
| F | 0.825 |
| G | 0.825 |
| H | 0.32±0.06 |
| I | 0.13 |
| J | 0.65 (T.P.) |
| K | 1.60±0.20 |
| L | 0.80±0.20 |
| M | $0.17^{+0.03}_{-0.07}$ |
| N | 0.10 |
| P | 1.40±0.10 |
| Q | 0.125±0.075 |
| R | $3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$ |
| S | 1.70 MAX. |

**P80GC-65-8BT-1**

## 80 PIN PLASTIC TQFP (FINE PITCH) (12x12)



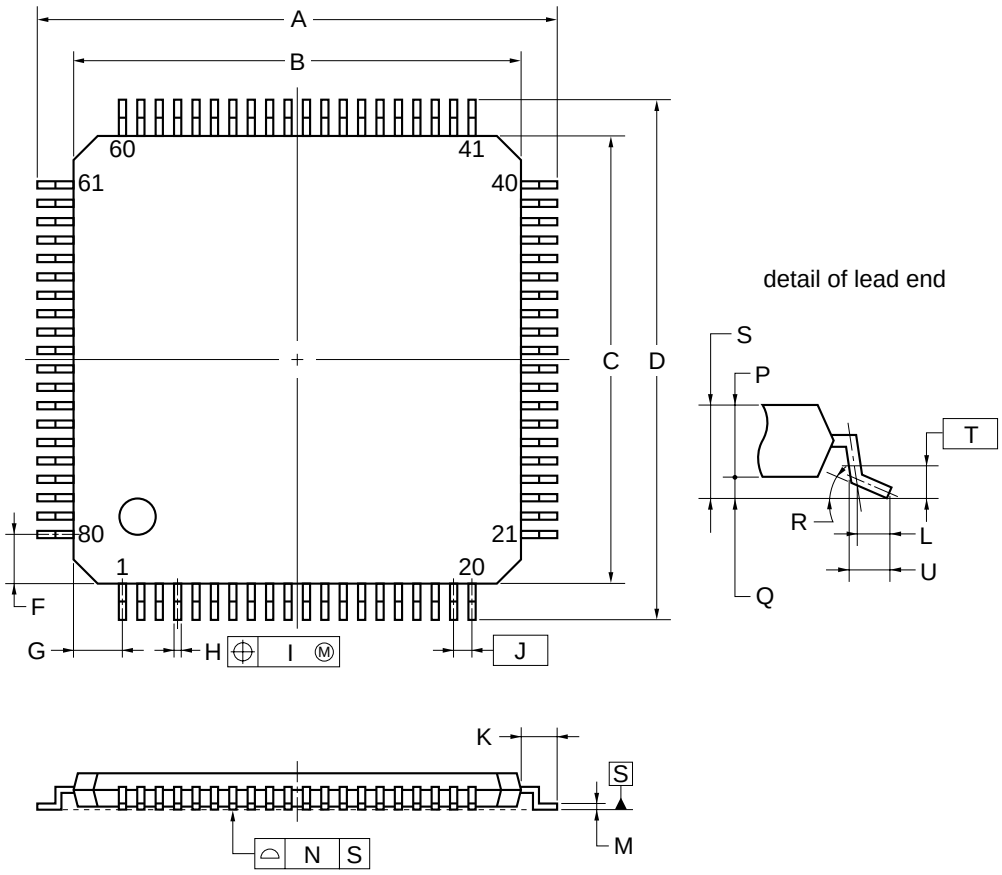

**NOTE**

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 14.00±0.20 |
| B | 12.00±0.20 |
| C | 12.00±0.20 |
| D | 14.00±0.20 |
| F | 1.25 |
| G | 1.25 |
| H | $0.22^{+0.05}_{-0.04}$ |
| I | 0.10 |
| J | 0.50 (T.P.) |
| K | 1.00±0.20 |
| L | 0.50±0.20 |
| M | $0.145^{+0.055}_{-0.045}$ |
| N | 0.10 |
| P | 1.05±0.07 |
| Q | 0.10±0.05 |
| R | 5°±5° |
| S | 1.27 MAX. |

**P80GK-50-BE9-6**

## ★ 80-PIN PLASTIC TQFP (FINE PITCH) (12x12)




**NOTE**

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 14.0±0.2 |
| B | 12.0±0.2 |
| C | 12.0±0.2 |
| D | 14.0±0.2 |
| F | 1.25 |
| G | 1.25 |
| H | 0.22±0.05 |
| I | 0.08 |
| J | 0.5 (T.P.) |
| K | 1.0±0.2 |
| L | 0.5 |
| M | 0.145±0.05 |
| N | 0.08 |
| P | 1.0 |
| Q | 0.1±0.05 |
| R | $3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$ |
| S | 1.1±0.1 |
| T | 0.25 |
| U | 0.6±0.15 |

**P80GK-50-9EU-1**

## 15. RECOMMENDED SOLDERING CONDITIONS

Solder the μPD753017A under the following recommended conditions.

For the details on the recommended soldering conditions, refer to Information Document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For the soldering methods and conditions other than those recommended, consult NEC.

**Table 15-1. Soldering Conditions of Surface Mount Type (1/2)**

**(1) μPD753012AGC-XXX-3B9: 80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm)**
**μPD753016AGC-XXX-3B9: 80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm)**
**μPD753017AGC-XXX-3B9: 80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm)**

| Soldering Method | Soldering Conditions | Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 235°C, Reflow time: 30 seconds or below (210°C or higher), Number of reflow processes: 3 max. | IR35-00-3 |
| VPS | Package peak temperature: 215°C, Reflow time: 40 seconds or below (200°C or higher), Number of reflow processes: 3 max. | VP15-00-3 |
| Wave soldering | Solder temperature: 260°C or below, Time: 10 seconds or below, Number of flow processes: 1<br>Preheating temperature: 120°C or below (package surface temperature) | WS60-00-1 |
| Partial heating | Pin temperature: 300°C or below, Time: 3 seconds or below (per side of device) | – |

★ **(2) μPD753012AGC-XXX-8BT: 80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm)**
**μPD753016AGC-XXX-8BT: 80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm)**
**μPD753017AGC-XXX-8BT: 80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm)**

| Soldering Method | Soldering Conditions | Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 235°C, Reflow time: 30 seconds or below (210°C or higher), Number of reflow processes: 2 max. | IR35-00-2 |
| VPS | Package peak temperature: 215°C, Reflow time: 40 seconds or below (200°C or higher), Number of reflow processes: 2 max. | VP15-00-2 |
| Wave soldering | Solder temperature: 260°C or below, Time: 10 seconds or below, Number of flow processes: 1<br>Preheating temperature: 120°C or below (package surface temperature) | WS60-00-1 |
| Partial heating | Pin temperature: 300°C or below, Time: 3 seconds or below (per side of device) | – |

**Caution Do not use two or more soldering methods in combination (except the partial heating method).**

**Table 15-1. Soldering Conditions of Surface Mount Type (2/2)**

**(3) μPD753012AGK-XXX-BE9: 80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.05 mm)**
**μPD753016AGK-XXX-BE9: 80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.05 mm)**
**μPD753017AGK-XXX-BE9: 80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.05 mm)**

| Soldering Method | Soldering Conditions | Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 235°C, Reflow time: 30 seconds or below (210°C or higher), Number of reflow processes: 3 max., Exposure limit: 7 days[Note] (After that, prebaking is necessary at 125°C for 10 hours.) | IR35-107-3 |
| VPS | Package peak temperature: 215°C, Reflow time: 40 seconds or below (200°C or higher), Number of reflow processes: 3 max., Exposure limit: 7 days[Note] (After that, prebaking is necessary at 125°C for 10 hours.) | VP15-107-3 |
| Partial heating | Pin temperature: 300°C or below, Time: 3 seconds or below (per side of device) | – |

**Note** The number of days for storage after the dry pack has been opened. The storage conditions are 25°C, 65% RH max.

★ **(4) μPD753012AGK-XXX-9EU: 80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.00 mm)**
**μPD753016AGK-XXX-9EU: 80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.00 mm)**
**μPD753017AGK-XXX-9EU: 80-pin plastic TQFP (fine pitch) (12 × 12 mm, resin thickness 1.00 mm)**

| Soldering Method | Soldering Conditions | Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 235°C, Reflow time: 30 seconds or below (210°C or higher), Number of reflow processes: 2 max., Exposure limit: 7 days[Note] (After that, prebaking is necessary at 125°C for 10 hours.) | IR35-107-2 |
| VPS | Package peak temperature: 215°C, Reflow time: 40 seconds or below (200°C or higher), Number of reflow processes: 2 max., Exposure limit: 7 days[Note] (After that, prebaking is necessary at 125°C for 10 hours.) | VP15-107-2 |
| Partial heating | Pin temperature: 300°C or below, Time: 3 seconds or below (per side of device) | – |

**Note** The number of days for storage after the dry pack has been opened. The storage conditions are 25°C, 65% RH max.

**Caution Do not use two or more soldering methods in combination (except the partial heating method).**

## APPENDIX A. μPD75316B, 753017A AND 75P3018A FUNCTION LIST

| Parameter | | μPD75316B | μPD753017A | μPD75P3018A |
|---|---|---|---|---|
| Program memory | | Mask ROM<br>0000H-3F7FH<br>(16256 × 8 bits) | Mask ROM<br>0000H-5FFFH<br>(24576 × 8 bits) | One-time PROM<br>0000H-7FFFH<br>(32768 × 8 bits) |
| Data memory | | 000H-3FFH<br>(1024 × 4 bits) | | |
| CPU | | 75X Standard | 75XL CPU | |
| Instruction execution time | When main system clock is selected | 0.95, 1.91, 15.3 μs<br>(at 4.19 MHz operation) | • 0.95, 1.91, 3.81, 15.3 μs (at 4.19 MHz operation)<br>• 0.67, 1.33, 2.67, 10.7 μs (at 6.0 MHz operation) | |
| | When subsystem clock is selected | 122 μs (32.768 kHz operation) | | |
| Pin connection | 44 | P12/INT2 | P12/INT2/TI1/TI2 | |
| | 47 | P21 | P21/PTO1 | |
| | 48 | P22/PCL | P22/PCL/PTO2 | |
| | 50-53 | P30-P33 | | P30/MD0-P33/MD3 |
| | 57 | IC | | $V_{PP}$ |
| Stack | SBS register | None | SBS.3 = 1: Mk I mode selection<br>SBS.3 = 0: Mk II mode selection | |
| | Stack area | 000H-0FFH | n00H-nFFH (n = 0-3) | |
| | Subroutine call instruction stack operation | 2-byte stack | Mk I mode: 2-byte stack<br>Mk II mode: 3-byte stack | |
| Instruction | BRA !addr1<br>CALLA !addr1 | Unavailable | Mk I mode: unavailable<br>Mk II mode: available | |
| | MOVT XA, @BCDE<br>MOVT XA, @BCXA<br>BR BCDE<br>BR BCXA | | Available | |
| | CALL !addr | 3 machine cycles | Mk I mode: 3 machine cycles, Mk II mode: 4 machine cycles | |
| | CALLF !faddr | 2 machine cycles | Mk I mode: 2 machine cycles, Mk II mode: 3 machine cycles | |
| Timer | | 3 channels<br>• Basic interval timer: 1 channel<br>• 8-bit timer/event counter: 1 channel<br>• Watch timer: 1 channel | 5 channels<br>• Basic interval timer/watchdog timer: 1 channel<br>• 8-bit timer/event counter: 3 channels (can be used as 16-bit timer/event counter, carrier generator, timer with gate)<br>• Watch timer: 1 channel | |

| Parameter | | μPD75316B | μPD753017A | μPD75P3018A |
|---|---|---|---|---|
| Clock output (PCL) | | Φ, 524, 262, 65.5 kHz (Main system clock: at 4.19 MHz operation) | • Φ, 524, 262, 65.5 kHz (Main system clock: at 4.19 MHz operation)<br>• Φ, 750, 375, 93.8 kHz (Main system clock: at 6.0 MHz operation) | |
| BUZ output | | 2 kHz (Main system clock: at 4.19 MHz operation) | • 2, 4, 32 kHz (Main system clock: at 4.19 MHz operation or subsystem clock: at 32.768 kHz operation)<br>• 2.93, 5.86, 46.9 kHz (Main system clock: at 6.0 MHz operation) | |
| Serial interface | | 3 modes are available<br>• 3-wire serial I/O mode ... MSB/LSB can be selected for transfer first bit<br>• 2-wire serial I/O mode<br>• SBI mode | | |
| SOS register | Feedback resistor cut flag (SOS.0) | None | Provided | |
| | Sub-oscillator current cut flag (SOS.1) | None | Provided | |
| Register bank selection register (RBS) | | None | Yes | |
| Standby release by INT0 | | Unavailable | Available | |
| Interrupt priority selection register (IPS) | | None | Yes | |
| Vectored interrupt | | External: 3, internal: 3 | External: 3, internal: 5 | |
| Supply voltage | | $V_{DD}$ = 2.0 to 6.0 V | $V_{DD}$ = 1.8 to 5.5 V | |
| Operating ambient temperature | | $T_A$ = –40 to +85°C | | |
| Package | | • 80-pin plastic TQFP (fine pitch) (12 × 12 mm)<br>• 80-pin plastic QFP (14 × 14 mm) | | |

## APPENDIX B. DEVELOPMENT TOOLS

The following development tools are provided for system development using the μPD753017A. The 75XL series uses a common relocatable assembler, in combination with a device file matching each machine.

### Language processor

| | Host Machine | | | Part Number (product name) |
|---|---|---|---|---|
| | | OS | Supply media | |
| RA75X relocatable assembler | PC-9800 series | MS-DOS™ (Ver. 3.30 to Ver. 6.2[Note]) | 3.5-inch 2HD | μS5A13RA75X |
| | IBM PC/AT™ and compatible machines | Refer to **OS for IBM PC** | 3.5-inch 2HC | μS7B13RA75X |

| | Host Machine | | | Part Number (product name) |
|---|---|---|---|---|
| | | OS | Supply media | |
| Device file | PC-9800 series | MS-DOS (Ver. 3.30 to Ver. 6.2[Note]) | 3.5-inch 2HD | μS5A13DF753017 |
| | IBM PC/AT and compatible machines | Refer to **OS for IBM PC** | 3.5-inch 2HC | μS7B13DF753017 |

**Note** Ver. 5.00 or later is provided with a task swap function, but it does not work with this software.

**Remark** The operation of the assembler and device file is guaranteed only on the above host machines and OSs.

**PROM write tools**

| | | | | | |
|---|---|---|---|---|---|
| Hardware | PG-1500 | PG-1500 is a PROM programmer which enables you to program single-chip microcontroller containing PROM by stand-alone or host machine operation by connecting an attached board and optional programmer adapter to PG-1500.<br>It also enables you to program typical PROM devices of 256K bits to 4M bits. | | | |
| | PA-75P316BGC | PROM programmer adapter common to μPD75P3018AGC-3B9. Connect the programmer adapter to PG-1500 for use. | | | |
| | PA-75P316BGK | PROM programmer adapter common to μPD75P3018AGK-BE9. Connect the programmer adapter to PG-1500 for use. | | | |
| ★ | PA-75P3018AGC-8BT | PROM programmer adapter common to μPD75P3018AGC-8BT. Connect the programmer adapter to PG-1500 for use. | | | |
| ★ | PA-75P3018AGK-9EU | PROM programmer adapter common to μPD75P3018AGK-9EU. Connect the programmer adapter to PG-1500 for use. | | | |
| Software | PG-1500 controller | PG-1500 and a host machine are connected by serial and parallel interfaces and PG-1500 is controlled on the host machine. | | | |
| | | Host machine | OS | Supply media | Part number (product name) |
| | | PC-9800 series | MS-DOS (Ver. 3.30 to Ver. 6.2[Note]) | 3.5-inch 2HD | μS5A13PG1500 |
| | | IBM PC/AT and compatible machines | Refer to **OS for IBM PC** | 3.5-inch 2HD | μS7B13PG1500 |

**Note** Ver.5.00 or later is provided with a task swap function, but it does not work with this software.

**Remark** The operation of the PG-1500 controller is guaranteed only on the above host machines and OSs.

**Debugging tool**

The in-circuit emulators (IE-75000-R and IE-75001-R) are available as the program debugging tool for the μPD753017A.

The system configurations are described as follows.

<table>
<tr><td rowspan="6">Hardware</td><td>IE-75000-R<sup>Note 1</sup></td><td colspan="3">In-circuit emulator for debugging the hardware and software when developing the application systems that use the 75X series and 75XL series. When developing a μPD753017 subseries, the emulation board IE-75300-R-EM and emulation probe that are sold separately must be used with the IE-75000-R.<br>By connecting with the host machine and the PROM programmer, efficient debugging can be made.<br>It contains the emulation board IE-75000-R-EM which is connected.</td></tr>
<tr><td>IE-75001-R</td><td colspan="3">In-circuit emulator for debugging the hardware and software when developing the application systems that use the 75X series and 75XL series. When developing a μPD753017 subseries, the emulation board IE-75300-R-EM and emulation probe which are sold separately must be used with the IE-75001-R.<br>It can debug the system efficiently by connecting the host machine and PROM programmer.</td></tr>
<tr><td>IE-75300-R-EM</td><td colspan="3">Emulation board for evaluating the application systems that use the μPD753017 subseries.<br>It must be used with the IE-75000-R or IE-75001-R.</td></tr>
<tr><td>EP-753017GC-R<br>EV-9200GC-80</td><td colspan="3">Emulation probe for the μPD753017AGC.<br>It must be connected to the IE-75000-R (or IE-75001-R) and IE-75300-R-EM.<br>It is supplied with the 80-pin conversion socket EV-9200GC-80 which facilitates connection to a target system.</td></tr>
<tr><td>EP-753017GK-R<br>TGK-080SDW<sup>Note 2</sup></td><td colspan="3">Emulation probe for the μPD753017AGK.<br>It must be connected to the IE-75000-R (or IE-75001-R) and IE-75300-R-EM.<br>It is supplied with the 80-pin conversion adapter TGK-080SDW which facilitates connection to a target system.</td></tr>
<tr><td rowspan="3">Software</td><td rowspan="3">IE control program</td><td colspan="3">Connects the IE-75000-R or IE-75001-R to a host machine via RS-232-C and Centronix I/F and controls the IE-75000-R or IE-75001-R on a host machine.</td></tr>
<tr><td rowspan="2">Host machine</td><td>OS</td><td>Supply media</td><td rowspan="2">Part number (product name)</td></tr>
<tr><td>PC-9800 series</td><td>MS-DOS<br>( Ver. 3.30 to Ver. 6.2<sup>Note 3</sup> )</td><td>3.5-inch 2HD</td><td>μS5A13IE75X</td></tr>
<tr><td>IBM PC/AT and compatible machines</td><td>Refer to OS for IBM PC</td><td>3.5-inch 2HC</td><td>μS7B13IE75X</td></tr>
</table>

**Notes 1.** Maintenance parts

**2.** This is a product of TOKYO ELETECH CORPORATION.
For further information, contact: Daimaru Kogyo, Ltd.
Tokyo Electronics Department (TEL +81-3-3820-7112)
Osaka Electronics 2nd Department (TEL +81-6-6244-6672)

**3.** Ver.5.00 or later is provided with a task swap function, but it dose not work with this software.

**Remarks 1.** The operation of the IE control program is guaranteed only on the above host machines and OSs.

**2.** The μPD753012, 753016, 753017, 75P3018, 753012A, 753016A, 753017A, and 75P3018A are commonly referred to as the μPD753017 subseries.

**OS for IBM PC**

The following IBM PC OS's are supported.

| OS | Version |
|---|---|
| PC DOS™ | Ver. 5.02 to Ver. 6.3<br>J6.1/V[Note] to J6.3/V[Note] |
| MS-DOS | Ver. 5.0 to Ver. 6.22<br>5.0/V[Note] to 6.2/V[Note] |
| IBM DOS™ | J5.02/V[Note] |

**Note** Only English version is supported.

**Caution Ver. 5.0 or later is provided with a task swap function, but it does not work with this software.**

## ★ APPENDIX C. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

### Device Related Documents

| Document Name | Document No. | |
|---|---|---|
| | Japanese | English |
| μPD753012A, 753016A, 753017A Data Sheet | U11662J | U11662E (this document) |
| μPD75P3018A Data Sheet | U11917J | U11917E |
| μPD753017 User's Manual | U11282J | U11282E |
| μPD753017 Instruction Table | IEM-5598 | — |
| 75XL Series Selection Guide | U10453J | U10453E |

### Development Tool Related Documents

| Document Name | | | Document No. | |
|---|---|---|---|---|
| | | | Japanese | English |
| Hardware | IE-75000-R/IE-75001-R User's Manual | | EEU-846 | EEU-1416 |
| | IE-75300-R-EM User's Manual | | U11354J | U11354E |
| | EP-753017GC/GK-R User's Manual | | EEU-967 | EEU-1494 |
| | PG-1500 User's Manual | | U11940J | U11940E |
| Software | RA75X Assembler Package | Operation | U12622J | U12622E |
| | User's Manual | Language | U12385J | U12385E |
| | PG-1500 Controller User's Manual | PC-9800 Series (MS-DOS) Base | EEU-704 | EEU-1291 |
| | | IBM PC Series (PC DOS) Base | EEU-5008 | U10540E |

### Other Related Documents

| Document Name | Document No. | |
|---|---|---|
| | Japanese | English |
| SEMICONDUCTOR SELECTION GUIDE Products & Package (CD-ROM) | X13769X | |
| Semiconductor Device Mounting Technology Manual | C10535J | C10535E |
| Quality Grades on NEC Semiconductor Devices | C11531J | C11531E |
| NEC Semiconductor Device Reliability/Quality Control System | C10983J | C10983E |
| Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD) | C11892J | C11892E |
| Guide to Microcontroller-Related Products by Third Parties | U11416J | – |

**Caution The above related documents are subject to change without notice. For design purpose, etc., be sure to use the latest documents.**

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

# Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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Fax: 408-588-6130
800-729-9288

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**NEC Electronics Singapore Pte. Ltd.**
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**NEC Electronics Taiwan Ltd.**
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