NEC

MOS INTEGRATED CIRCUIT

μPD75048

4-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD75408 is a 4-bit single-chip microcomputer whose data processing capability is comparative to that of an 8-bit microcomputer.

The μPD75048 employs a CPU whose minimum instruction execution time is 0.95 μs, and contains the EEPROM, A/D converter, multi-function timer, and high performance hardware to provide high cost to performance ratio.

Detailed functions are described in the following user's manual. Read this manual when designing your system.

μPD75048 User's Manual: IEU-704

FEATURES

- Built-in EEPROM: 1024 x 4 bits (data memory area)
- Built-in 8-bit resolution A/D converter (successive approximation): 8 channels
  - Capable of operating at low voltage: V_{DD} = 2.7 to 6.0 V
  - Reference voltage can be arbitrarily specified between AV_{REF+} and AV_{REF-}.
- Built-in multi-function timer which can provide the following functions:
  - 8-bit timer
  - PWM output
  - 16-bit free running timer
  - 16-bit integration type A/D converter counter
- I/O ports: 48 pins
  - Middle voltage N-ch open drain input/output ports: 12 pins
  - 43 I/O lines can be provided with internal pull-down resistors
- PROM version is available: μPD75P048 (One-time PROM)

APPLICATIONS

- Consumer electronics products, telephones, cameras, automobile audio equipment, electronics measurement equipment, etc.

ORDERING INFORMATION

Part Number	Package	Quality grade
μPD75048CW-xxx	64-pin plastic shrink DIP (750 mil)	Standard
μPD75048GC-xxx-AB8	64-pin plastic QFP (□ 14mm)	Standard

Remarks: xxx is ROM code number.

Please refer to "Quality Grade on NEC Semiconductor Devices" (Document Number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information in this document is subject to change without notice.

Document No. IC - 2518C
(O. D. No. IC - 7931C)
Date Published February 1994 P
Printed in Japan

The mark ★ shows major revised points.

FUNCTIONAL OUTLINE

Item	Function			
Instructions	41			
Instruction Execution Time	• With main system clock: 0.95, 1.91, 15.3 μs (at 4.19 MHz) • With subsystem clock: 122 μs (at 32.768 kHz)			
Internal Memory	Program memory (ROM) : 8064 x 8 bits			
	Data memory (RAM) : 512 x 4 bits Data memory (EEPROM) : 1024 x 4 bits			
EEPROM	• Retains data in case of power failure • Number of writes: 100,000 times • Write time: 10 ms • Write end, overwrite interrupt functions			
General-Purpose Register	• 4-bit manipulation: 8 (X, A, B, C, D, E, H, L) • 8-bit manipulation: 4 (XA, BC, DE, HL)			
Accumulator	• Bit accumulator (CY) • 4-bit accumulator (A) • 8-bit accumulator (XA)			
Instruction Set	• Abundant bit manipulation instructions • Efficient 4-bit data manipulation instructions • 8-bit data manipulation instructions • GETI instruction executing 2-/3-byte instruction with a single byte			
I/O Line	48	12	Input pin	Via software, w/pull-up resistor: 27 w/pull-down resistor: 4
		24	CMOS I/O pin (direct LED drive: 4)	
		12	Medium-voltage N-ch open-drain I/O (direct LED drive)	By mask option, w/pull-up resistor: 12
Timer	4 chs	• 8-bit timer/event counter • Clock source: 4 steps • Can count events		
		• 8-bit basic interval timer • Reference time generation: 1.95, 7.82, 31.3, 250 ms (at 4.19 MHz) • Can be used as watchdog timer		
		• Clock timer • Generates 0.5-second time intervals • Count clock source: main system clock or subsystem clock (selectable) • Clock fast forward mode (generates 3.9-ms time intervals) • Buzzer output (2, 4, 32 kHz)		
		• Multi-function timer Can be used as: • 8-bit timer • PWM output • 16-bit free-running timer • Counter for 16-bit integral A/D converter		
8-bit Serial Interface	• Three modes: • 3-line serial I/O mode ... MSB/LSB first (selectable) • 2-line serial I/O mode • SBI mode			
Bit Sequential Buffer	Special bit manipulation memory: 16 bits • Ideal for remote controller			
Clock Output Function	Timer/event counter output (PTO0): output of square wave at specified frequency			
	Clock output (PCL): Φ/, $f_x/2^3$, $f_x/2^4$, $f_x/2^6$			
	Buzzer output (BUZ): 2, 4, 32 kHz (with main system clock or subsystem clock)			

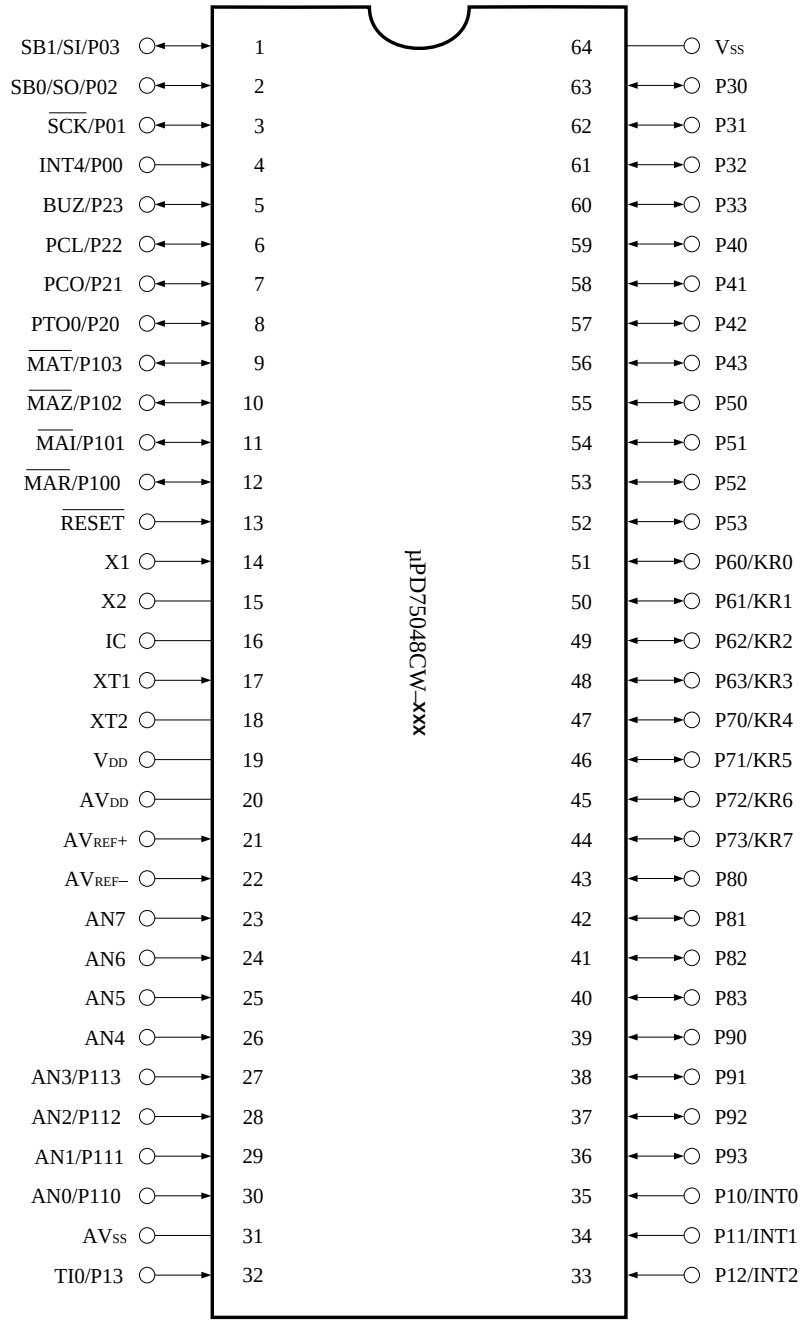
(cont'd)

Item	Function
A/D Converter	8-bit resolution A/D converter (successive approximation type): 8 channels • Low-voltage operation: V_{DD} = 2.7 – 6.0 V • Reference voltage setting range: $AV_{REF+} - AV_{REF-}$ 2.5 V ≤ (AV_{REF+}) – (AV_{REF-}) ≤ 6.0 V
Vector Interrupt	External: 3, Internal: 6
Test Input	External: 1, Internal: 1
System Clock Oscillator Circuit	• Ceramic/crystal oscillator circuit for main system clock oscillation • Crystal oscillator circuit for subsystem clock oscillation
Standby Function	• STOP mode: main system clock oscillation stops • HALT mode: system clock oscillation continues (clock supply to CPU stops)
Package	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (□ 14 mm)

CONTENTS

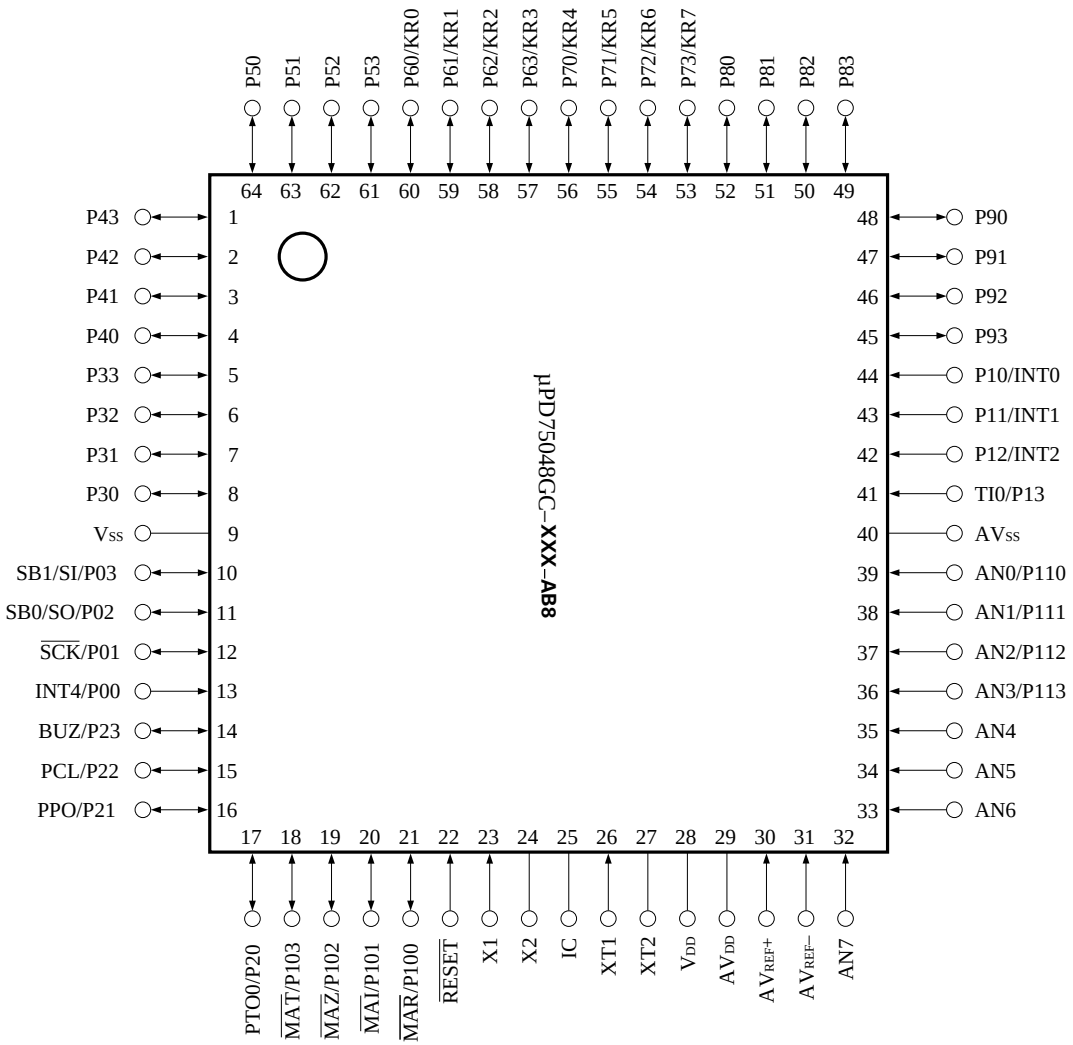
1. PIN CONFIGURATION (TOP VIEW)

• 64-PIN PLASTIC SHRINK DIP (750 mil)



IC : Internally Connected (Connect directly to V_{DD})

• **64-PIN PLASTIC QFP (□ 14 mm)**

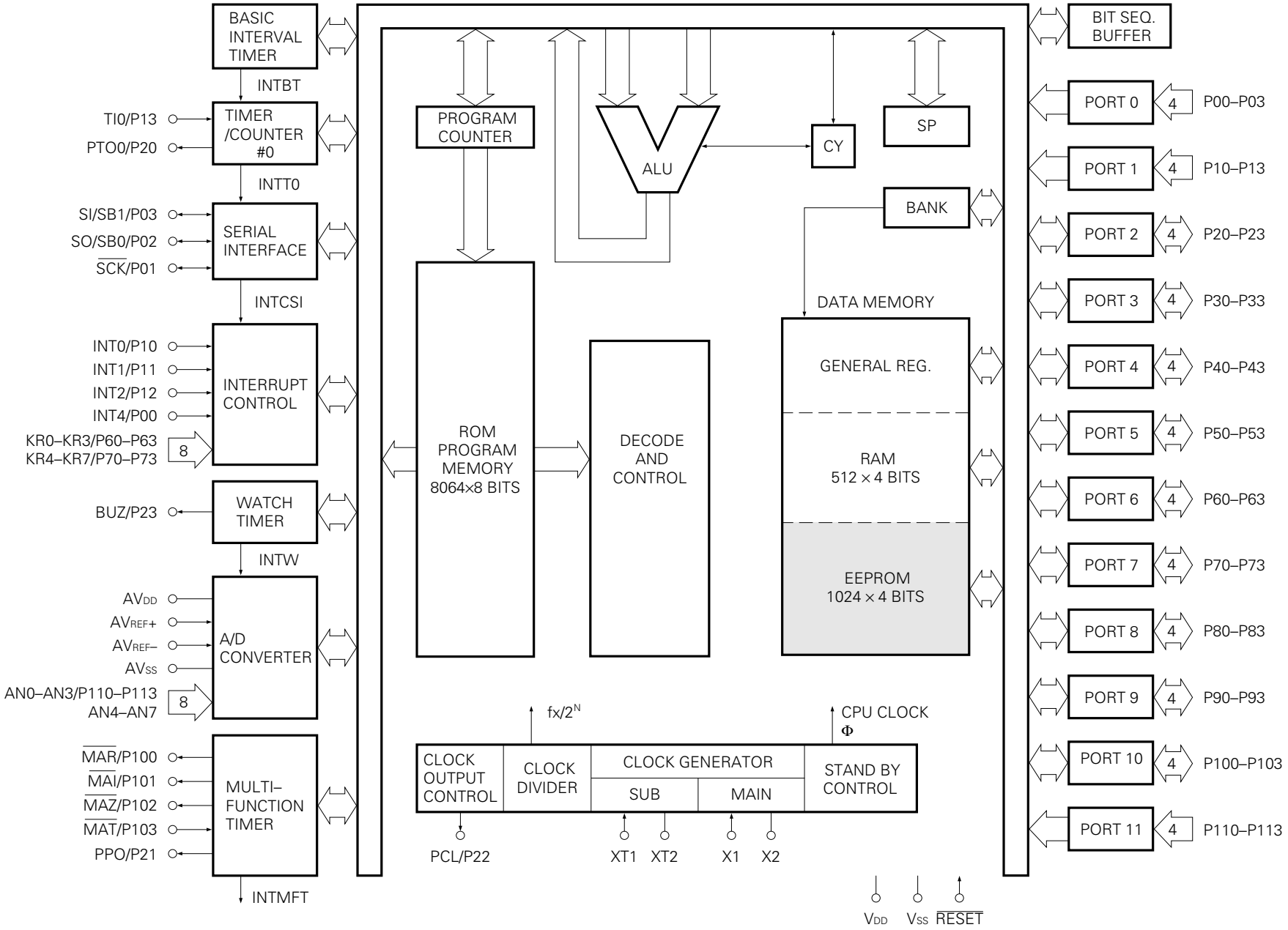


IC : Internally Connected (Connect directly to V_{DD})

PIN IDENTIFICATION

P00-03	: Port0		: Port 0	
P10-13	: Port1		: Port 1	
P20-23	: Port2		: Port 2	
P30-33	: Port3		: Port 3	
P40-43	: Port4		: Port 4	
P50-53	: Port5		: Port 5	
P60-63	: Port6		: Port 6	
P70-73	: Port7		: Port 7	
P80-83	: Port8		: Port 8	
P90-93	: Port9		: Port 9	
P100-103	: Port10		: Port 10	
P110-113	: Port11		: Port 11	
KR0-7	: Key Return		: Key interrupt input	
$\overline{SCK}$	: Serial Clock		: Serial clock input/output	
SI	: Serial Input		: Serial data input	
SO	: Serial Output		: Serial data output	
SB0, 1	: Serial Bus 0, 1		: Serial bus input/output	
$\overline{RESET}$	: Reset Input		: Reset input	
TI0	: Timer Input 0		: External event pulse input	
PTO0	: Programmable Timer Output 0		: Timer/event counter output	
BUZ	: Buzzer Clock		: Arbitrary frequency output	
PCL	: Programmable Clock		: Clock output	
INT0,1,4	: External Vectored Interrupt 0, 1, 4		: External vector interrupt input	
INT2	: External Test Input 2		: External test input	
X1, 2	: Main System Clock Oscillation 1, 2		: Main system clock oscillation pin	
XT1, 2	: Subsystem Clock Oscillation 1, 2		: Subsystem clock oscillation pin	
$\overline{MAR}$	: Reference Integration Control	MFT A/D mode	: Reference integration signal output	MFT A/D mode
$\overline{MAI}$	: Integration Control		: Integration signal output	
$\overline{MAZ}$	: Autozero Control		: Autozero signal output	
$\overline{MAT}$	: External Comparate Timing Input		: External comparator signal input	
$\overline{PPO}$	: Programmable Pulse Output ... MFT timer mode		: Pulse output ... MFT timer mode	
AN0-7	: Analog Input 0-7		: Analog input	
AV_{REF+}	: Analog Reference (+)		: Analog reference voltage (+) input (AV_{DD})	
AV_{REF-}	: Analog Reference (-)		: Analog reference voltage (-) input (AV_{SS})	
AV_{DD}	: Analog V_{DD}		: A/D converter positive power supply	
AV_{SS}	: Analog V_{SS}		: A/D converter GND	
V_{DD}	: Positive Power Supply		: Positive power supply	
V_{SS}	: Ground		: GND	

Remarks : MFT: Multi-function timer


BASIC INTERVAL TIMER
INTBT
TI0/P13
PTO0/P20
TIMER /COUNTER #0
INTT0
SI/SB1/P03
SO/SB0/P02
SCK/P01
SERIAL INTERFACE
INTCSI
INT0/P10
INT1/P11
INT2/P12
INT4/P00
KR0–KR3/P60–P63
KR4–KR7/P70–P73
8
INTERRUPT CONTROL
BUZ/P23
WATCH TIMER
INTW
AVDD
AVREF+
AVREF–
AVSS
AN0–AN3/P110–P113
AN4–AN7
8
A/D CONVERTER
MAR/P100
MAI/P101
MAZ/P102
MAT/P103
PPO/P21
MULTI–FUNCTION TIMER
INTMFT
PROGRAM COUNTER
ALU
CY
SP
BANK
DATA MEMORY
GENERAL REG.
RAM 512 × 4 BITS
EEPROM 1024 × 4 BITS
ROM PROGRAM MEMORY 8064×8 BITS
DECODE AND CONTROL
fx/2N
CPU CLOCK Φ
CLOCK OUTPUT CONTROL
CLOCK DIVIDER
CLOCK GENERATOR
SUB
MAIN
STAND BY CONTROL
PCL/P22
XT1
XT2
X1
X2
VDD
VSS
RESET
BIT SEQ. BUFFER
PORT 0
4
P00–P03
PORT 1
P10–P13
PORT 2
P20–P23
PORT 3
P30–P33
PORT 4
P40–P43
PORT 5
P50–P53
PORT 6
P60–P63
PORT 7
P70–P73
PORT 8
P80–P83
PORT 9
P90–P93
PORT 10
P100–P103
PORT 11
P110–P113

3. PIN FUNCTIONS

3.1 PORT PINS

Pin Name	Input/Output	Also Served As	Function	8-Bit I/O	When Reset	Input/ Output Circuit TYPE*1
P00	Input/ Output	INT4	4-bit input/output port(PORT0) Pull up resistros can be specified in 3-bit units for the P01 to P03 pins by software.	X	Input	Ⓑ
P01	Input/ Output	$\overline{SCK}$				Ⓕ-A
P02	Input/ Output	SO/SB0				Ⓕ-B
P03	Input/ Output	SO/SB1				Ⓜ-C
P10	Input	INT0	With noise elimination function	X	Input	Ⓑ-C
P11		INT1	4-bit input port(PORT1) Internal pull-up resistors can be specified in 4-bit units by software.			
P12		INT2				
P13		TI0				
P20	Input/ Output	PTO0	4-bit input/output port(PORT2) Internal pull-up resistors can be specified in 4-bit units by software.	X	Input	E -B
P21		PPO				
P22		PCL				
P23		BUZ				
P30*2	Input/ Output	—	Programmable 4-bit input/output port (PORT3) This port can be specified for input/ output in bit units. Internal pull-up resistors can be specified in 4-bit units by software.	X	Input	E -B
P31*2		—				
P32*2		—				
P33*2		—				
P40-43*2	Input/ Output	—	N-ch open-drain 4-bit input/output port (PORT4) Internal pull-up resistors can be specified in 4-bit units (by mask option). Resistive voltage is 10V in the open-drain mode.	○	High level (with internal pull-up register) or high imped-ance	M
P50-53*2	Input/ Output	—	N-ch open-drain 4-bit input/output port (PORT5) Internal pull-up resistors can be specified in bit units (by mask option). Resistive voltage is 10V in the open-drain mode.		High level (with internal pull-up register) or high imped-ance	M

*1: Circles indicate Schmitt trigger inputs.

2: Can directly drive LED.

(cont'd)

Pin Name	Input/Output	Also Served As	Function	8-Bit I/O	When Reset	Input/ Output Circuit TYPE*1
P60	Input/ Output	KR0	Programmable 4-bit input/output port (PORT6) This port can be specified for input/ output in bit units. Internal pull-up resistors can be specified in 4-bit units by software.	◯	Input	Ⓕ-A
P61		KR1				
P62		KR2				
P63		KR3				
P70	Input/ Output	KR4	4-bit input/output port(PORT7) Internal pull-up resistors can be specified in 4-bit units by software.		Input	Ⓕ-A
P71		KR5				
P72		KR6				
P73		KR7				
P80-83	Input/ Output	—	4-bit input/output port(PORT8) Internal pull-up resistors can be specified in 4-bit units by software.	X	Input	E-B
P90-93	Input/ Output	—	4-bit input/output port(PORT9) Internal pull-down resistors can be specified in 4-bit units by software.		Input	E-D
P100	Input/ Output	$\overline{MAR}$	N-ch open-drain 4-bit input/output port (PORT10) Internal pull-up resistors can be specified in bit units (by mask option). Resistive voltage is 10V in the open-drain mode.	X	High level (with internal pull-up resistor) or high impedance	M
P101		$\overline{MAI}$				
P102		$\overline{MAZ}$				
P103		$\overline{MAT}$				
P110	Input	AN0	4-bit input port(PORT11)		Input	Y-A
P111		AN1				
P112		AN2				
P113		AN3				

*1: Circles indicate Schmitt trigger inputs.

3.2 NON PORT PINS

Pin Name	Input/Output	Also Served As	Functon		When Reset	Input/ Output Circuit TYPE*1
TI0	Input	P13	Timer/event counter external event pulse input		Input	Ⓑ- C
PTO0	Input/ Output	P20	Timer/event counter output		Input	E - B
PCL	Input/ Output	P22	Clock output		Input	E - B
BUZ	Input/ Output	P23	Arbitrary frequency output(for buzzer or for trimming the system clock)		Input	E - B
$\overline{SCK}$	Input/ Output	P01	Serial clock input/output		Input	Ⓕ- A
SO/SB0	Input/ Output	P02	Serial data output Serial bus input/output		Input	Ⓕ- B
SI/SB1	Input/ Output	P03	Serial data input Serial bus input/output		Input	Ⓜ- C
INT4	Input	P00	Edge detection vector interrupt input (both rising and falling edge detection are effective)		Input	Ⓑ
INT0	Input	P10	Edge detection vector interrupt input (detection edge is selectable)	Clock synchronous	Input	Ⓑ- C
INT1		P11		Asynchronous		
INT2	Input	P12	Edge detection vector interrupt input (rising edge is detected.)	Asynchronous	Input	Ⓑ- C
KR0-KR3	Input/ Output	P60-63	Parallel falling edge detection testable input		Input	Ⓕ- A
KR4-KR7	Input/ Output	P70-73	Parallel falling edge detection testable input		Input	Ⓕ- A
$\overline{MAR}$	Input/ Output	P100	In the MFT integration type A/ D converter mode	Reference integration signal output	*2	M
$\overline{MAI}$	Input/ Output	P101		Integration signal output		
$\overline{MAZ}$	Input/ Output	P102		Auto zero signal output		
$\overline{MAT}$	Input/ Output	P103		Comparator input		
PPO	Input/ Output	P21	In the MFT timer mode	Timer pulse output	Input	E - B

1: Circles indicate Schmitt trigger inputs.

2: High level (with internal pull-up resistor) or high impedence

Remarks: MFT: Multi-function timer

(cont'd)

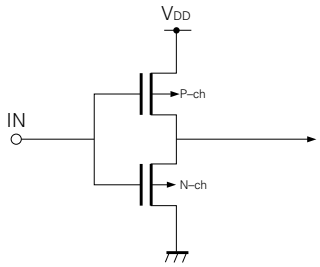
Pin Name	Input/Output	Also Served As	Function		When Reset	Input/ Output Circuit TYPE*1
AN0-AN3	Input	—	Pins only for A/D converter	8-bit analog input	Input	Y-A
AN4-AN7		—				Y
AV_{REF+}	Input	—		Reference voltage input (AV_{DD} side)	—	Z-A
AV_{REF-}	Input	—		Reference voltage input (AV_{SS} side)	—	Z-A
AV_{DD}	—	—		Positive power supply	—	—
AV_{SS}	—	—		GND	—	—
X1, X2	Input	—	A crystal/ceramic resonator for the main system clock is connected across these pins. When using the external clock, the X1 pin inputs the external clock, and the X2 pin inputs the reverse phase of the external clock signal.		—	—
XT1, XT2	Input	—	A crystal resonator for the subsystem clock is connected across these pins. When using the external clock, the XT1 pin inputs the external clock, and the XT2 pin inputs the reverse phase of the external clock signal. The XT1 pin can be used as a 1-bit input(test) pin.		—	—
$\overline{RESET}$	Input	—	System reset input		—	Ⓑ
IC	—	—	Internally Connected. Should be connected directly to V_{DD}.		—	—
V_{DD}	—	—	Positive power supply		—	—
V_{SS}	—	—	GND		—	—

*1: Circles indicate Schmitt trigger inputs.

3.3 PIN INPUT/OUTPUT CIRCUITS

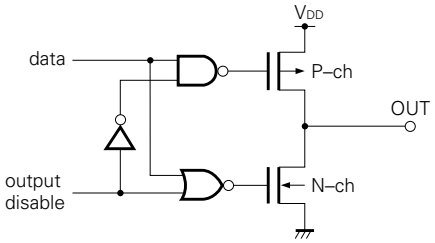
The following shows a simplified input/output circuit diagram for each pin of the μPD75048.

TYPE A (for TYPE E–B)



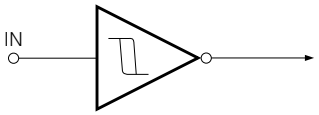
Input buffer of CMOS standard

TYPE D (for TYPE E–B, F-A)



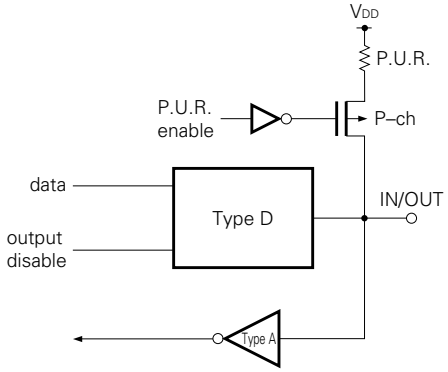
Push–pull output that can be set in the output high–impedance state (both P–ch and N–ch are off)

TYPE B



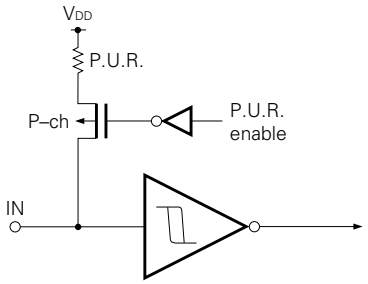
Schmitt trigger input with hysteresis characteristics

TYPE E–B



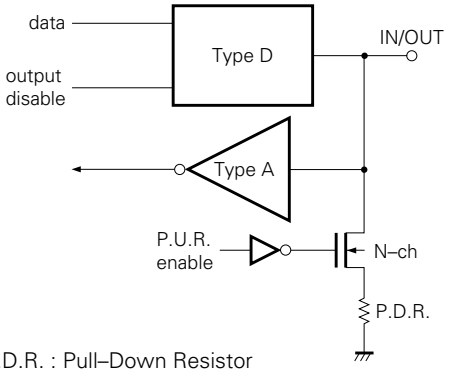
P.U.R. : Pull–Up Resistor

TYPE B–C



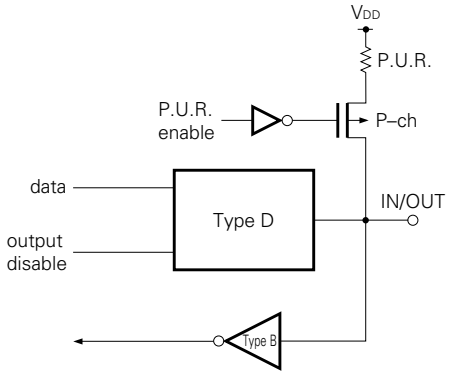
P.U.R. : Pull–Up Resistor

TYPE E–D



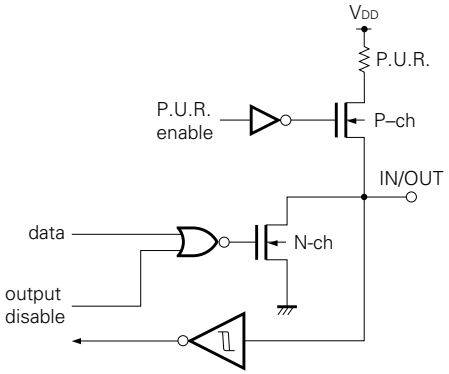
P.D.R. : Pull–Down Resistor

TYPE F–A



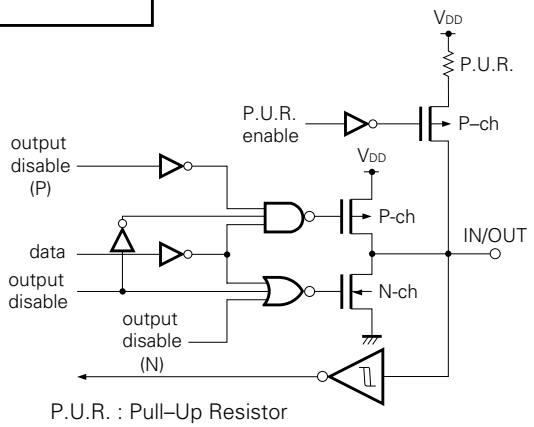
P.U.R. : Pull–Up Resistor

TYPE M–C



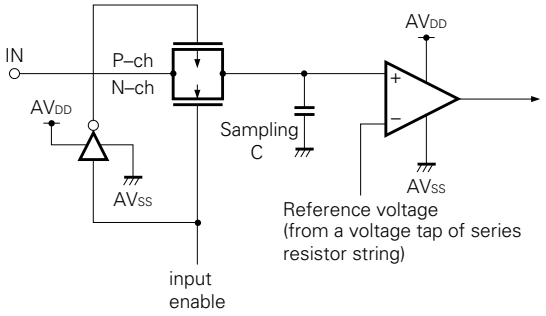
P.U.R. : Pull–Up Resistor

TYPE F–B

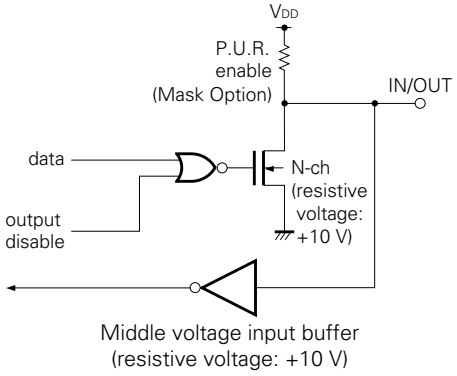


P.U.R. : Pull–Up Resistor

TYPE Y



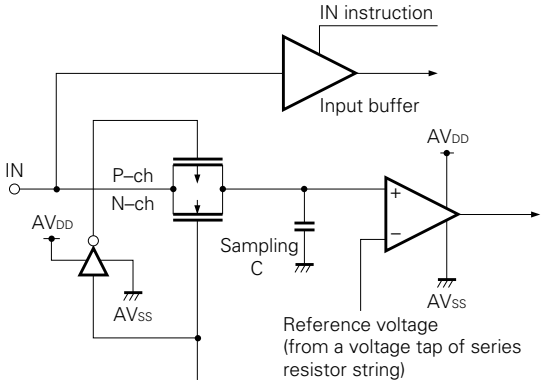
TYPE M

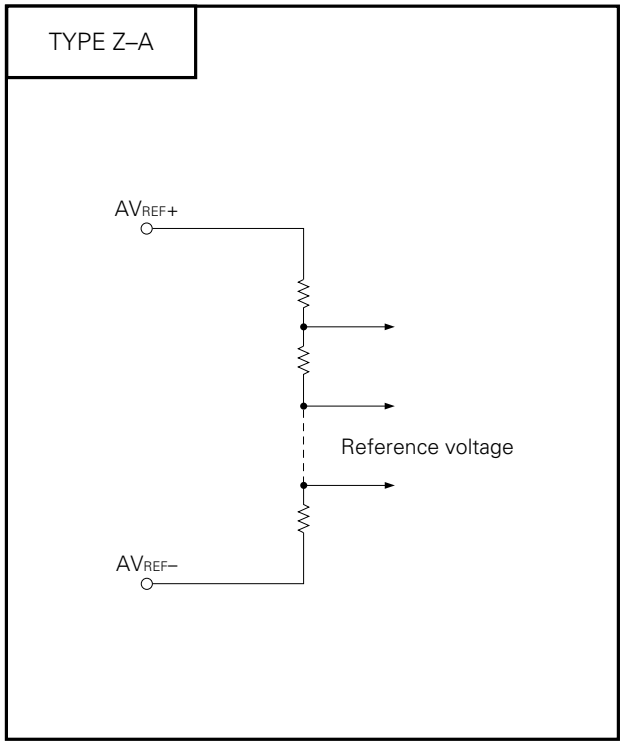


Middle voltage input buffer
(resistive voltage: +10 V)

P.U.R. : Pull–Up Resistor

TYPE Y–A





3.4 SELECTION OF MASK OPTIONS

The following mask options are available:

Pin	Mask Option	
P40 - P43, P50 - P53, P100 - P103	① w/pull-up resistor (can be specified bitwise)	② w/o pull-up resistor (can be specified bitwise)
XT1, XT2	① w/feedback resistor (with subsystem clock used)	② w/o feedback resistor (without subsystem clock used)

3.5 PROCESSING OF UNUSED PINS ★

Pin	Recommended Condition
P00/INT4	Connect to V_{SS}
P01/$\overline{SCK}$	Connect to V_{SS} or V_{DD}
P02/SO/SB0	
P03/SI/SB1	
P10/INT0-P12/INT2	Connect to V_{SS}
P13/TI0	
P20/PTO0	Input: Connect to V_{SS} or V_{DD} Output: Open
P21/PPO	
P22/PCL	
P23/BUZ	
P30-P33	
P40-P43	
P50-P53	
P60/KR0-P63/KR3	
P70/KR4-P73/KR7	
P80-P83	
P90-P93	
P100/$\overline{MAR}$	
P101/$\overline{MAI}$	
P102/$\overline{MAZ}$	
P103/$\overline{MAT}$	
P110/AN0-P113/AN3	Connect to V_{SS} or V_{DD}
AN4-AN7	
AV_{REF+}	Connect to V_{SS}
AV_{REF-}	
AV_{SS}	
AV_{DD}	Connect to V_{DD}
XT1	Connect to V_{SS} or V_{DD}
XT2	Open
IC	Connect directly to V_{DD}

4. MEMORY CONFIGURATION

- Program memory (ROM)...8064 x 8 bits (0000H-1F7FH)
  - 0000H, 0001H: Vector table to which address from which program is started is written after reset
  - 0002H-000FH: Vector table to which address from which program is started is written after interrupt
  - 0020H-007FH: Table area referenced by GETI instruction

- Data memory
  - Data area
    Static RAM....512 x 4 bits (000H-1FFH)
    EEPROM....1024 x 4 bits (400H-7FFH)
  - Peripheral hardware area....128 x 4 bits (F80H-FFFH)

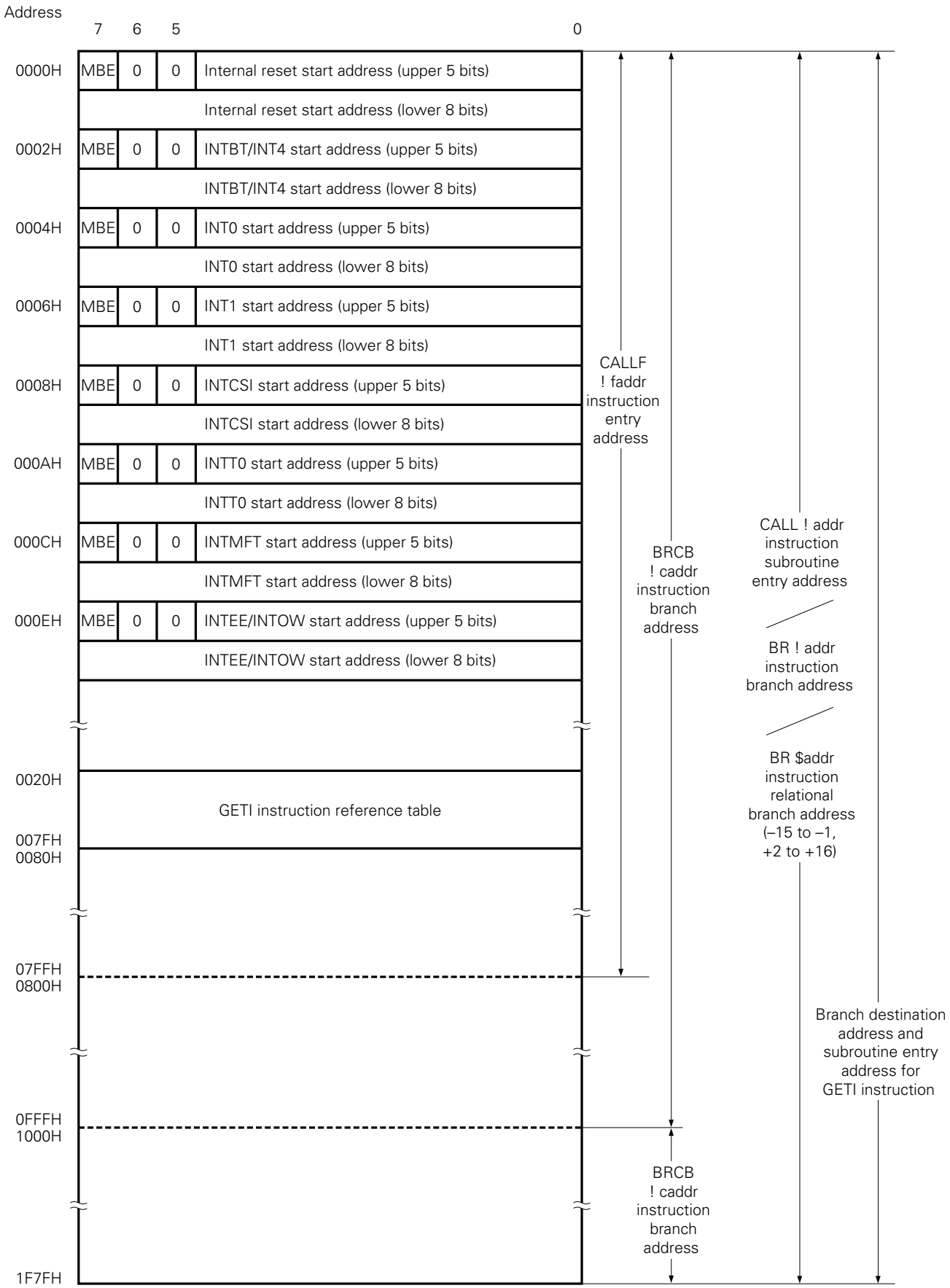


Fig. 4-1 Program Memory Map

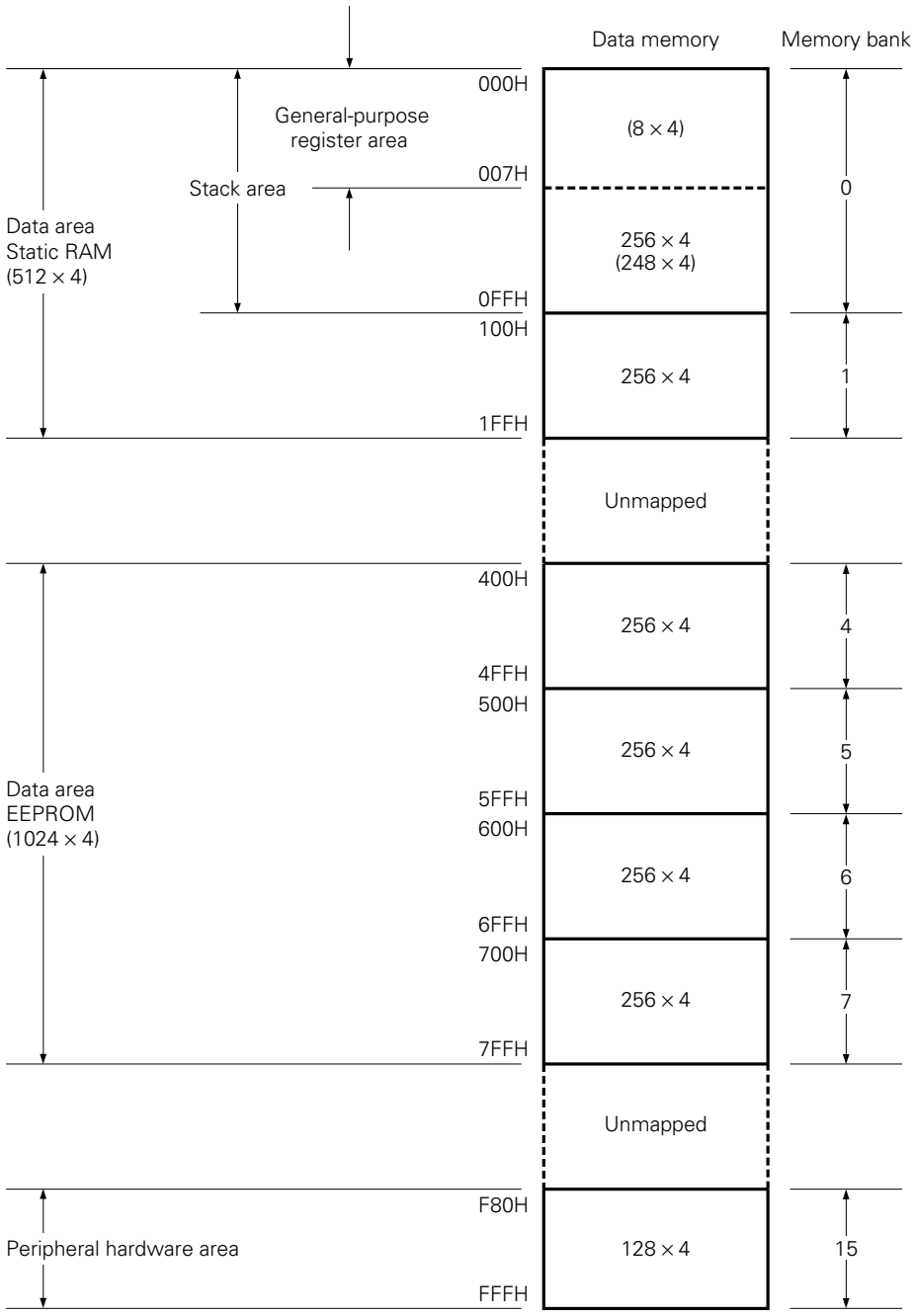


Fig. 4-2 Data Memory Map

5. EEPROM

The μPD75048 contains the 1024-word x 4-bit EEPROM (Electrically Erasable PROM).
The EEPROM of the μPD75048 has the following characteristics.

- The EEPROM can retain its contents even if the power is turned off.
- In the same manner as the static RAM, data can be manipulated (auto-erase/write/read) in 4-bit or 8-bit units by using a memory manipulation instruction
- The contens of EEPROM are automatically erased or written by hardware, so that the overhead of the software is alleviated.
  - Write time .... 10 ms.
  - Number of write operation100,000 times (guaranteed).
- Write operation can be controlled by interrupt.
  - When write operation is completed an interrupt occurs.
  - When overwrite is executed. (Write operation is executed during write operation)
- Whether or not the EEPROM is possible to be written can be checked by individually checking the write status flag.

6. PERIPHERAL HARDWARE FUNCTIONS

6.1 PORT

I/O ports are classified into the following three inds:

- CMOS input (PORT0, 1, 11) : 12
- CMOS I/O (PORT2, 3, 6, 7, 8, 9) : 24
- N-ch open-drain I/O (PORT4, 5, 10) : 12

Total 48

Table 6-1 Port Function

Port (Symbol)	Function	Operation/Feature	Remarks
PORT0 PORT1	4-bit input	Can be read or tested regardless of the operation mode of the shared pin.	Also serves as the SO/SB0, SI/SB1, SCK, INT0 to 2, INT4, and TI0 pins
PORT3* PORT6	4-bit input/output	Can be specified for input/output in 1-bit units.	Port 6 can also serve as the KR0 to KR3 pins.
PORT2 PORT7		Can be specified for input/output in 4-bit units. Ports 6 and 7 can be paired to input/ output data in 8-bit units.	Port 2 can also serve as the PTO0, PPO, PCL, and BUZ pins. Also serves as the KR4 to KR7 pins.
PORT4* PORT5* PORT10*	4-bit input/output (N-ch open-drain, can sustain with 10V)	Can be specified for input/output in 4-bit units. Ports 4 and 5 can be paired to input/output data in 8-bit units.	Whether or not the internal pull-up resistor is provided can be specified for each bit by mask option. Port 10 can also serve as the $\overline{MAR}$, $\overline{MAI}$, $\overline{MAZ}$, and $\overline{MAT}$ pins.
PORT8 PORT9	4-bit input/output	Can be specified for input/output in 4-bit units.	
PORT11	4-bit input	4-bit input-only port.	Port 11 can also serve as the AN0 to AN3 pins.

*: Can directly drive LED.

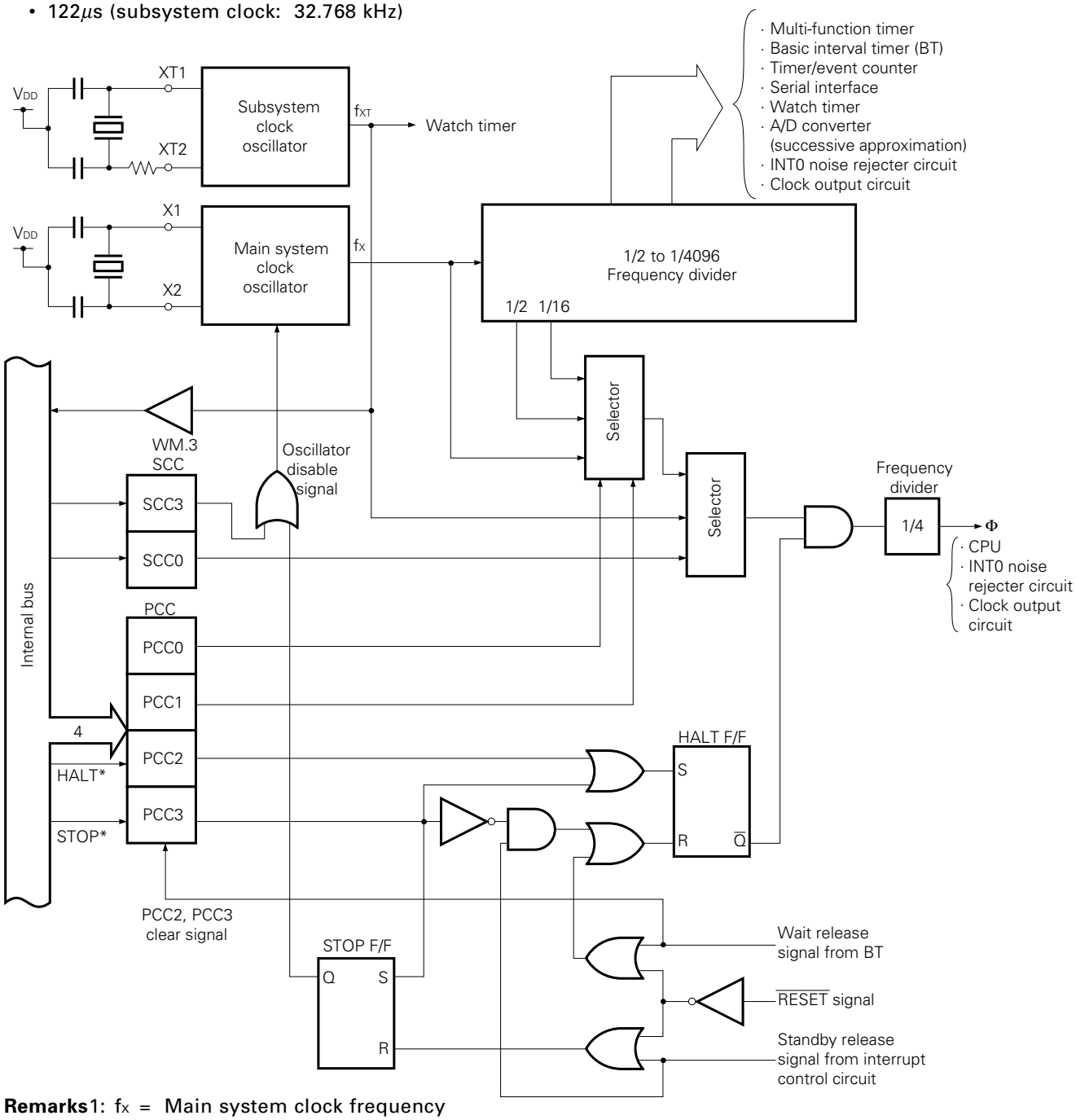
6.2 CLOCK GENERATOR CIRCUIT

The operation of the clock generator circuit is determined by the processor clock control regiser (PPC) and system clock control register (SCC).

This circuit can generate two types of clocks: main system clock and subsystem clock.

In addition, it can also change the instruction execution time.

- 0.95 μs, 1.91 μs, 15.3 μs (main system clock: 4.19 MHz)
- 122μs (subsystem clock: 32.768 kHz)



Remarks 1: f_X = Main system clock frequency
2: f_{XT} = Subsystem clock frequency
3: Φ = CPU clock
4: PCC: Processor clock control register
5: SCC: System clock control register
6: * indicates instruction execution.
7: One clock cysle (t_{CY}) of Φ is one machine cycle of an instruction. For t_{CY}, refer to AC characteristics in 11. ELECTRICAL SPECIFICATIONS.

Fig. 6-1 Clock Generator Block Diagram

6.3 CLOCK OUTPUT CIRCUIT

The clock output circuit outputs clock pulse from the P22/PCL pin. This clock pulse is used for supplying clock pulses to the remote control output, peripheral LSIs, etc.

- Clock output (PCL): Φ, 524 kHz, 65.5 kHz (at 4.19 MHz)

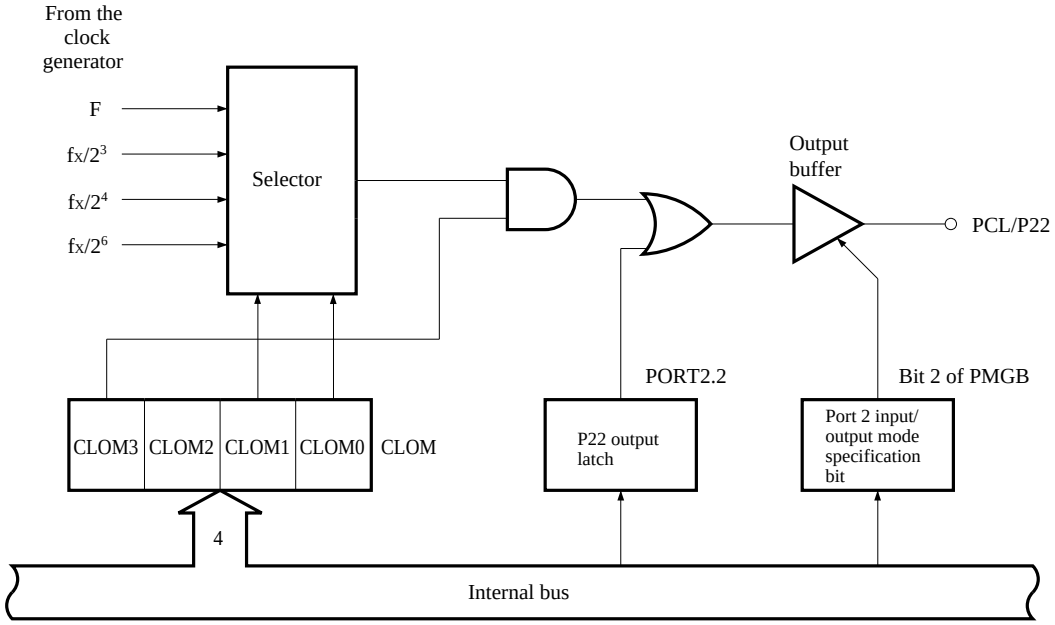


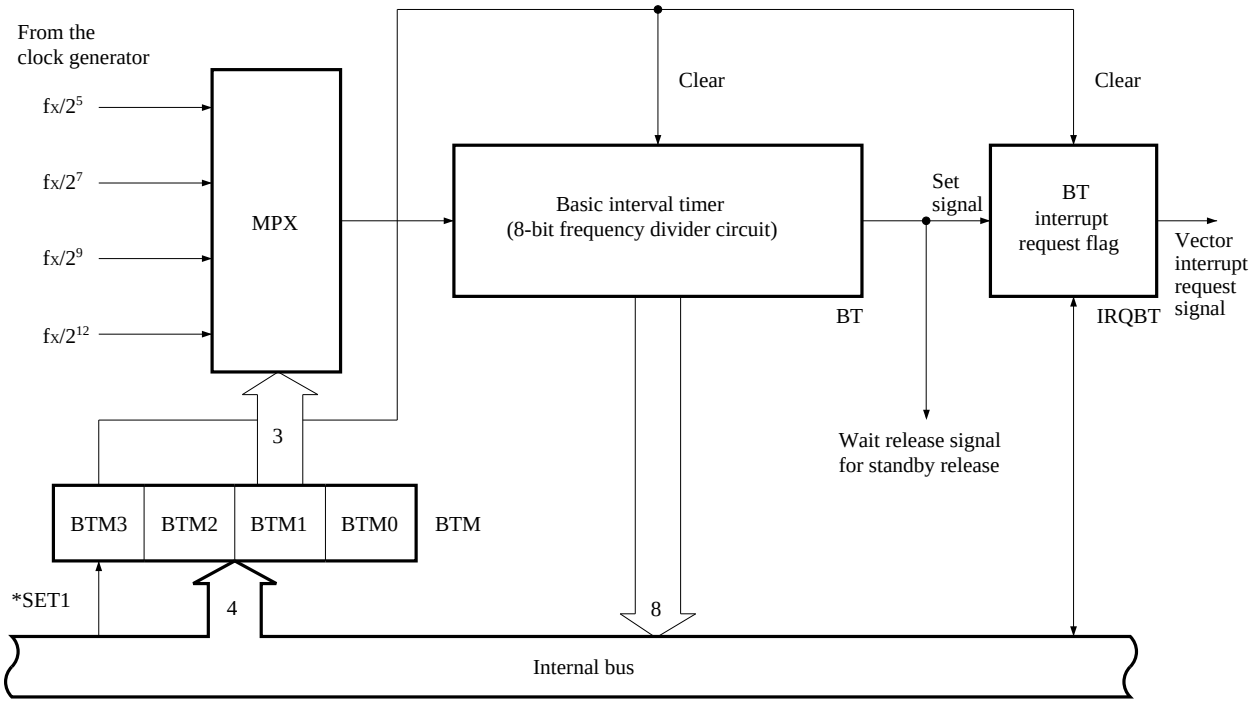
Fig. 6-2 Clock Output Circuit Configuration

Remarks: A measures to prevent outputting narrow width pulse when selecting clock output enable/disable is taken.

6.4 BASIC INTERVAL TIMER

The basic interval timer has these functions:

- Interval timer operation which generates a reference time interrupt
- Watchdog timer application which detects a program runaway
- Selects the wait time for releasing the standby mode and counts the wait time
- Reads out the count value



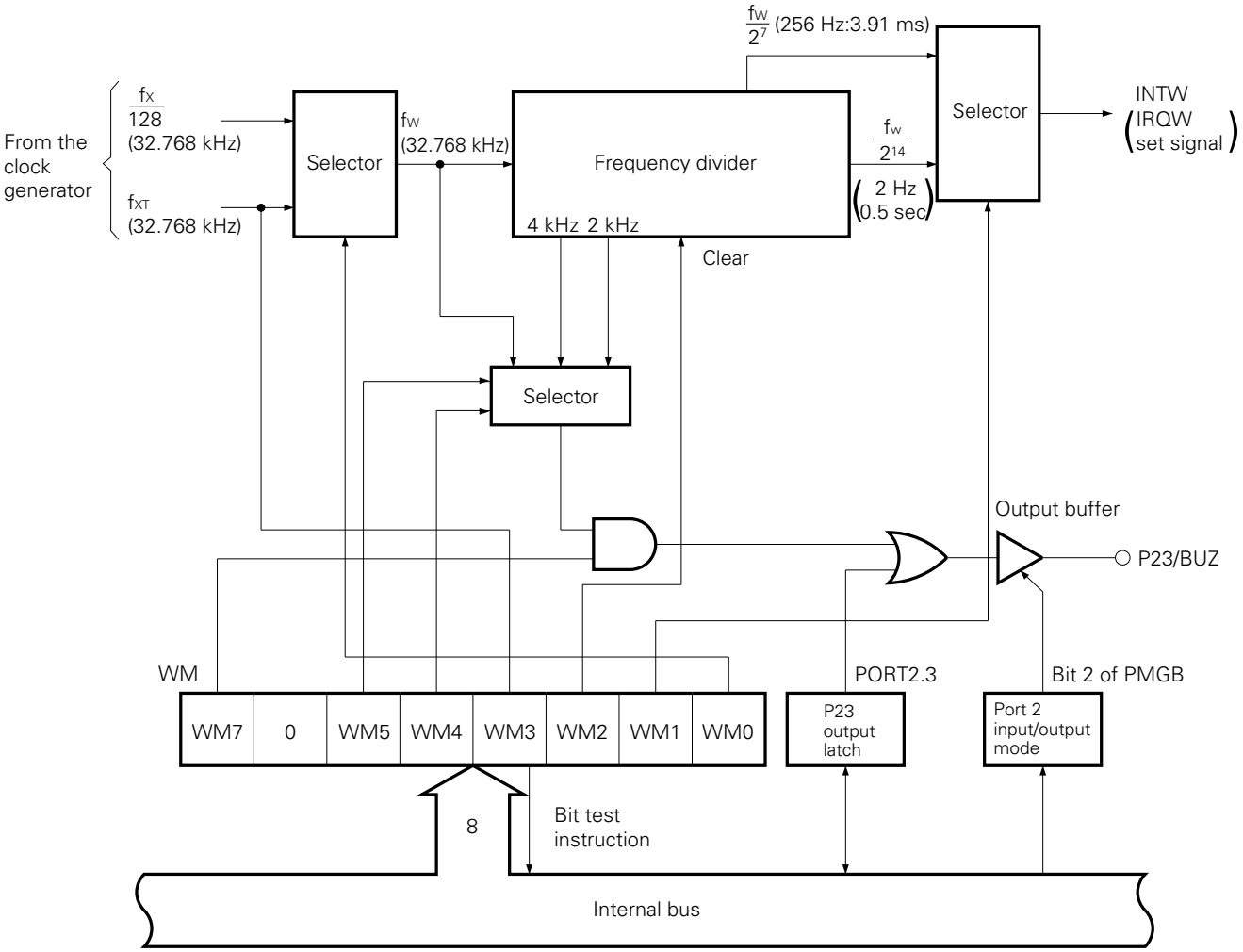
Remarks : *: Instruction execution

Fig. 6-3 Basic Interval Timer Configuration

6.5 WATCH TIMER

The μPD75048 has a built-in 1-ch watch timer. The clock timer has the following functions.

- Sets the test flag (IRQW) with 0.5sec interval.
  The standby mode can be released by IRQW.
- 0.5 second interval can be generated either from the main system clock or subsystem clock.
- Time interval can be advanced to 128 times faster (3.91 ms) by setting the fast mode. This is convenient for program debugging, test, etc.
- Arbitrary frequency (2.048kHz/4.096kHz/32.768kHz) can be output to the P23/BUZ pin. This can be used for beep and system clock frequency trimming.
- The frequency divider circuit can be cleared so that zero second clock start is possible.



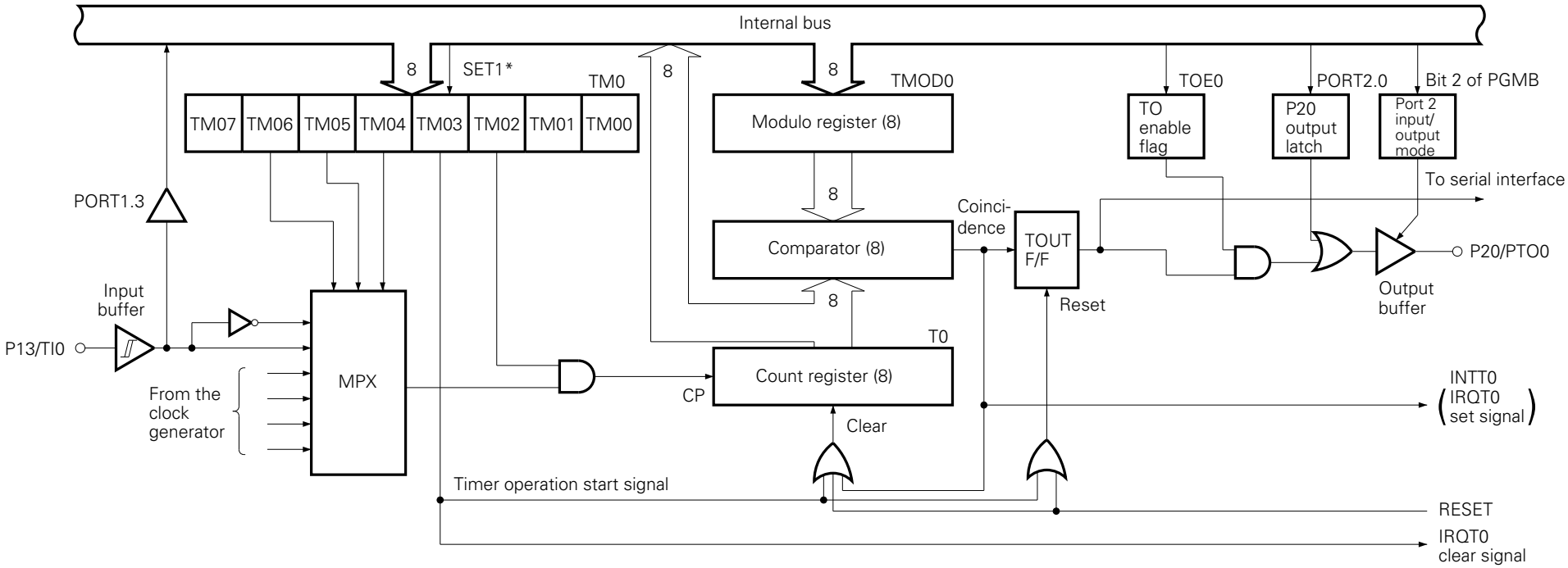
( ) is for f_X = 4.194304 MHz, f_{XT} = 32.768 KHz.

Fig. 6-4 Clock Timer Block Diagram

6.6 TIMER/EVENT COUNTER

The μPD75048 has a built-in 1-ch timer/event counter. The timer/event counter has the following functions.

- Programmable interval timer operation
- Outputs square-wave signal of an arbitrary frequency to the PTO0 pin.
- Event counter operation
- Divides the TI0 pin input in N and outputs to the PTO0 pin (frequency divider operation).
- Supplies serial shift clock to the serial interface circuit.
- Count condition read out function



*:Instruction execution

Fig. 6-5 Timer/Event Counter Block Diagram

6.7 SERIAL INTERFACE

The μPD75048 is equipped with an 8-bit clocked serial interface that operates in the following four modes:

- Operation stop mode
- Three-line serial I/O mode
- Two-line serial I/O mode
- SBI mode (serial bus interface mode)

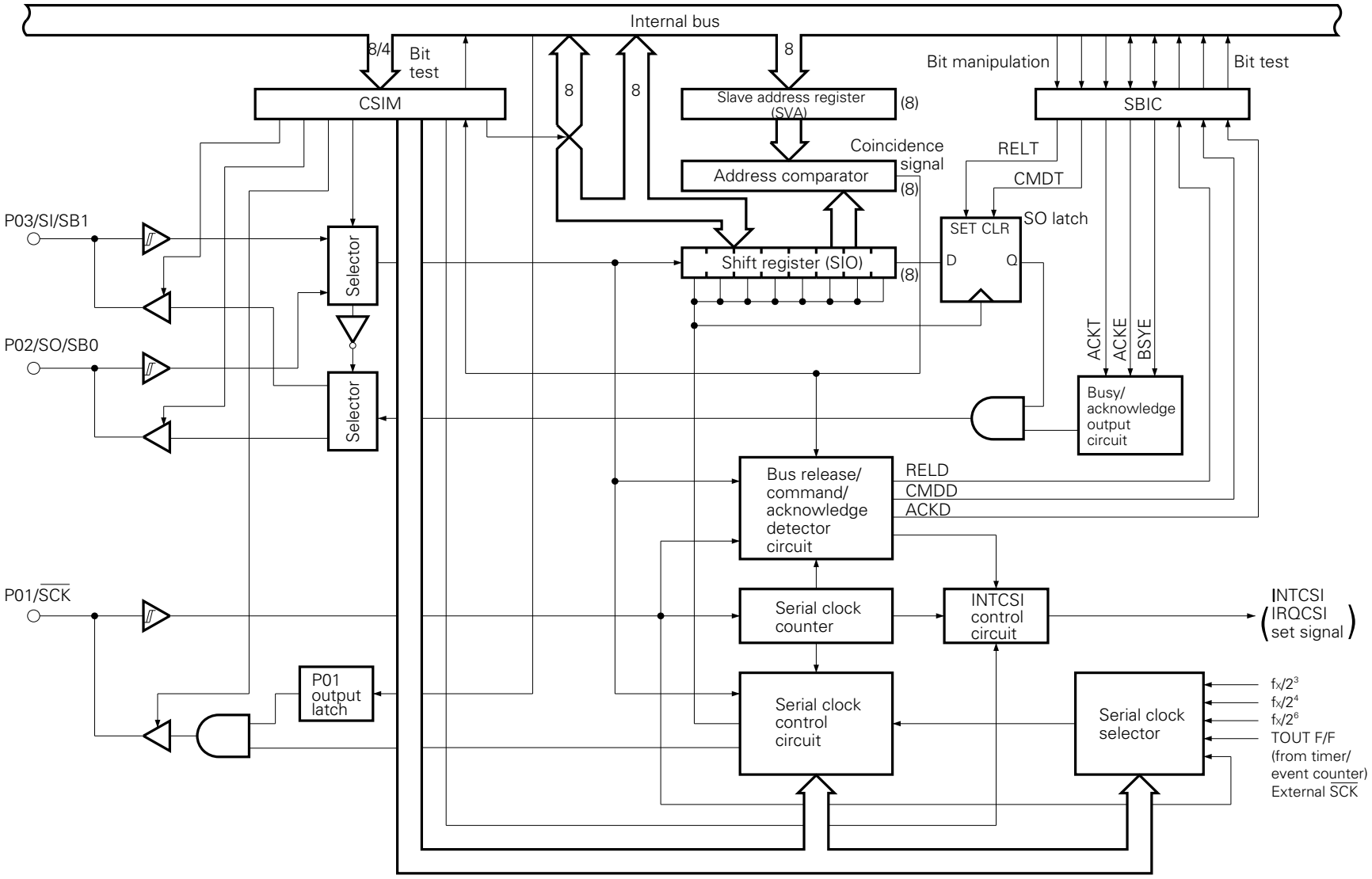


Fig. 6-6 Serial Interface Block Diagram

6.8 A/D CONVERTER

The μPD75048 has an 8-bit precision successive approximation A/D converter with 8 analog input channels (AN0 to AN7).

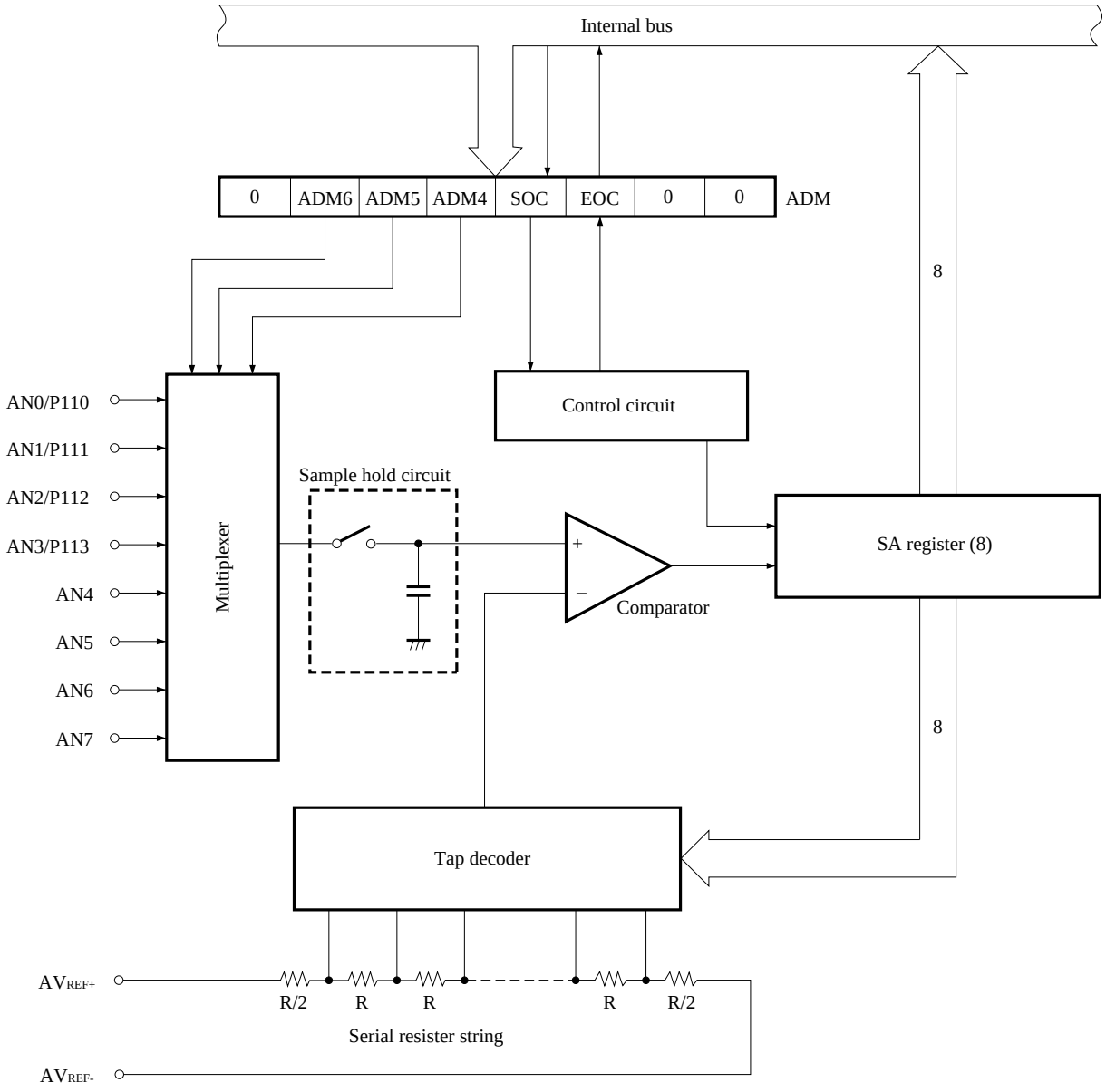


Fig. 6-7 A/D Converter Block Diagram

6.9 MULTI-FUNCTION TIMER (MFT)

The μPD75048 contains 1 channel of multi-function timer (MFT).

The MFT has the following four modes and functions:

- 8-bit timer mode
  - Functions as programmable interval timer
  - Outputs square waves of arbitrary frequency to the PPO pin
- PWM mode
  - Outputs 6/7/8-bit precision PWM signal to the PPO pin
- 16-bit free running timer mode
  - Functions as interval timer which generates an interrupt with specified interval
  - Can be used as one-shot timer
- Integration type A/D converter mode
  - Outputs 16-bit integration type A/D converter control signal
  - 13/14/15/16-bit precision selectable

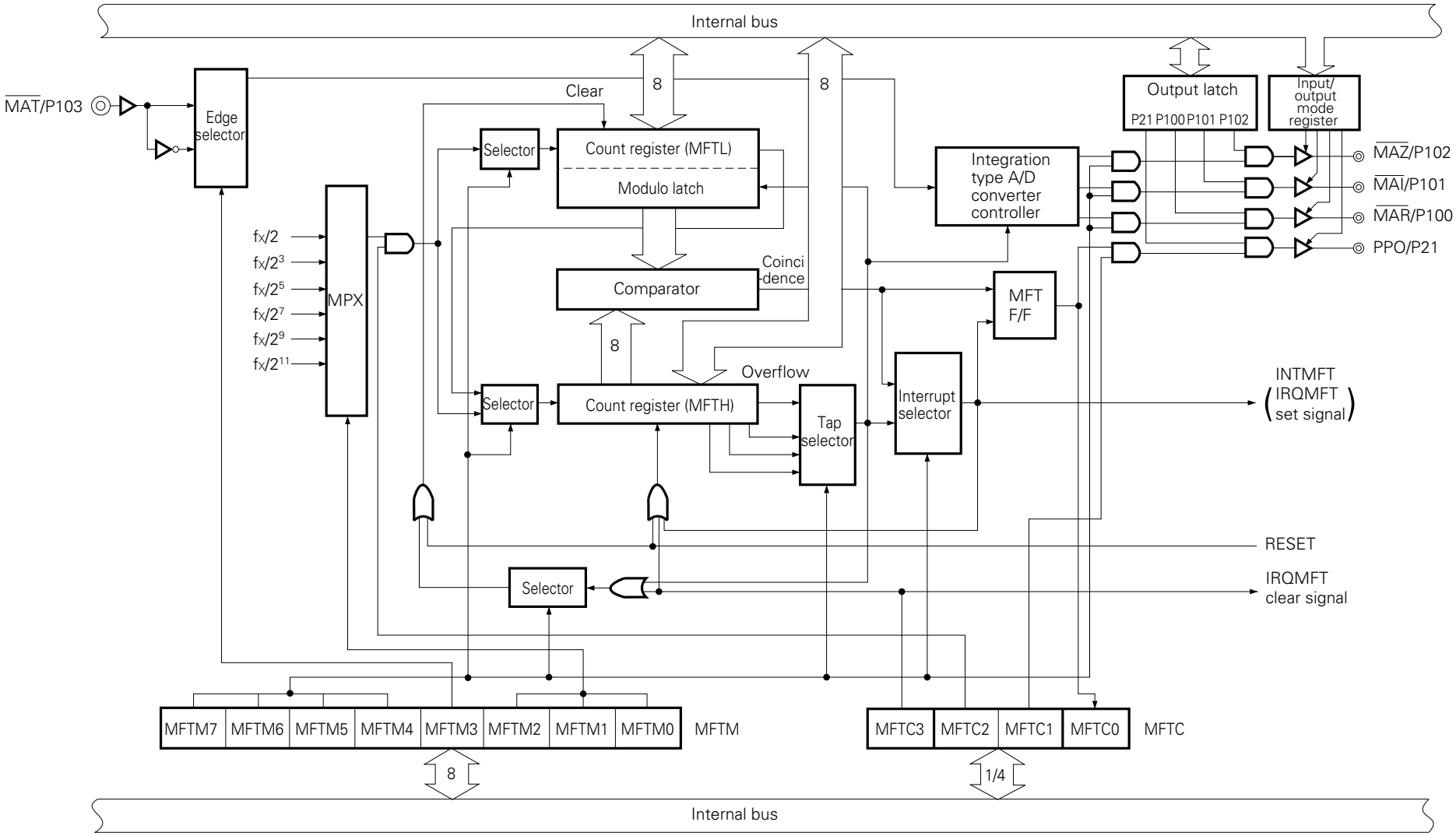
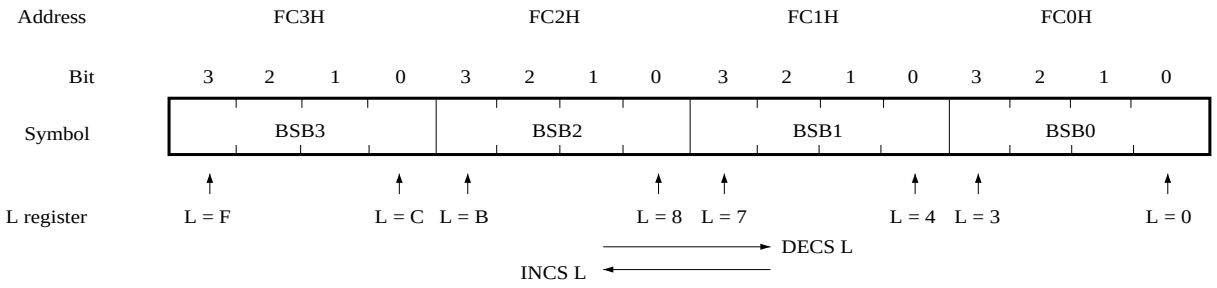


Fig. 6-8 Multi-Function Timer Block Diagram

6.10 BIT SEQUENTIAL BUFFER .... 16 BITS

The bit sequential buffer is a data memory specifically provided for bit manipulation. With this buffer, addresses and bit specifications can be sequentially up-dated in bit manipulation operation. Therefore, this buffer is very useful for processing long data in bit units.



Remarks: For the pmem.@L addressing, the specification bit is shifted according to the L register.

Fig. 6-9 Bit Sequential Buffer Format

7. INTERRUPT FUNCTIONS

The μPD75048 has 9 different interrupt sources. In addition to that, multiple interrupt by software control is also possible.

The μPD75048 is also provided with two types of test sources, of which INT2 was two types of edge detection testable inputs.

The interrupt control circuit of the μPD75048 has these functions:

- Hardware controlled vector interrupt function which can control whether or not to accept an interrupt by using the interrupt flag (IExxx) and interrupt master enable flag (IME).
- The interrupt start address can be arbitrarily set.
- Interrupt request flag (IRQxxx) test function (an interrupt generation can be confirmed by means of software).
- Standby mode release (Interrupts to be released can be selected by the interrupt enable flag).

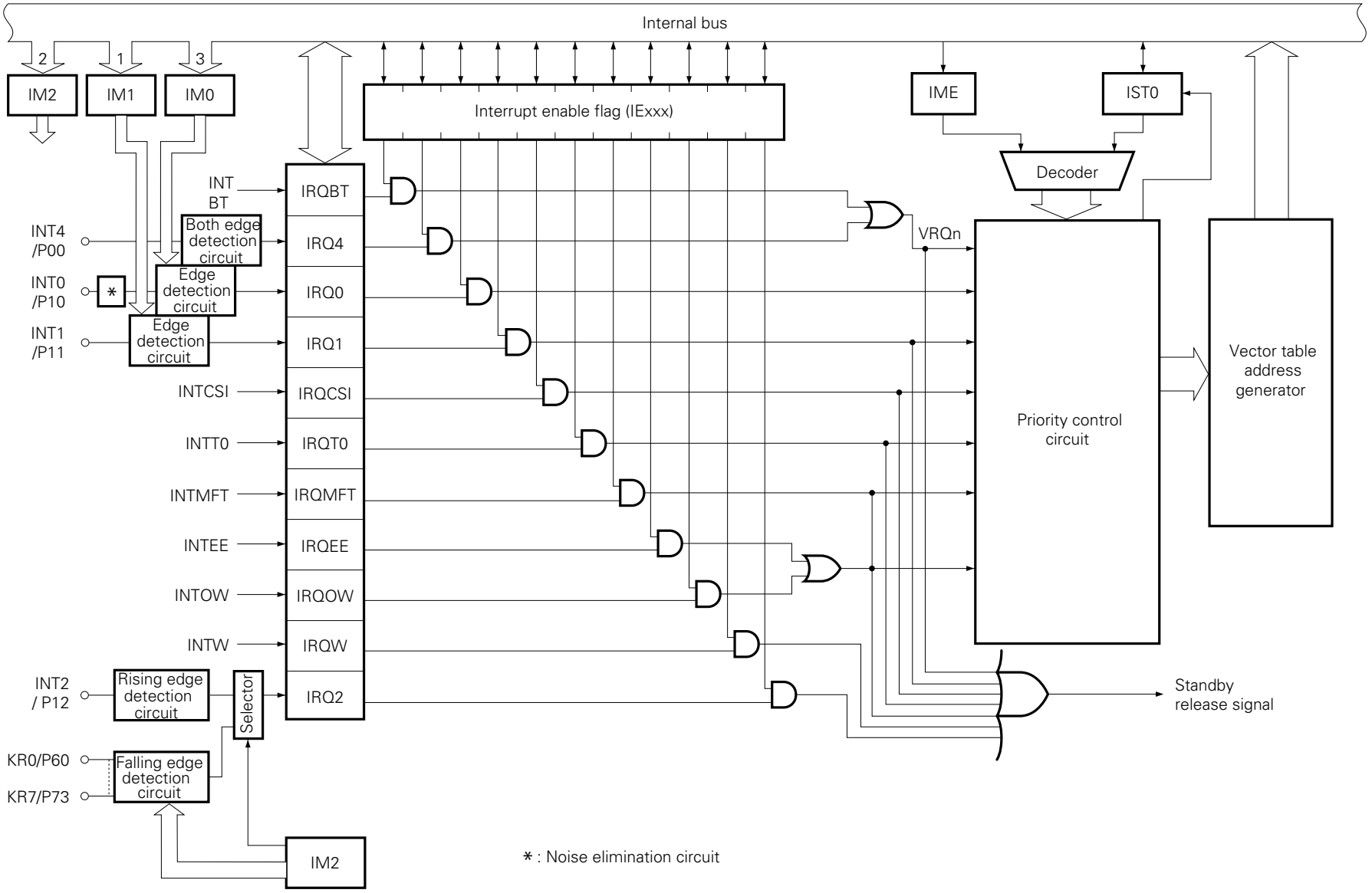


Fig. 7-1 Interrupt Control Circuit Block Diagram

8. STANDBY FUNCTIONS

The μPD75048 has two different standby modes (STOP mode and HALT mode) to reduce the power consumption while waiting for program execution.

Table 8-1 Each Status in Standby Mode

		STOP Mode	HALT Mode
Setting Instruction		STOP instrtuction	HALT Instruction
System Clock for Setting		Can be set only when operating on the main system clock	Can be set either with the main system clock or the subsystem clock
Operation Status	Clock Generator	Only the main system clock stops its operation	Only the CPU clock Φ stops its operation (oscillation continues)
	Basic Interval Timer	No operation	Operates only when main system clock oscillates (Sets IRQBT at reference time interval)
	Serial Interface	Can operate only when the external $\overline{SCK}$ input is selected for the serial clock	Operates only when external $\overline{SCK}$ input is selected as serial clock, or when main system clock oscillates
	Timer/Event Counter	Can operate only when the TI0 pin input is selected for the count clock	Operates only when TI0 pin input is selected as count clock, or when main system clock oscillates
	Watch Timer	Can operate when f_{XT} is selected as the count clock	Can operate
	A/D Convertor	No operation	Can operate *
	Multi Function Timer	No operation	Can operate *
	EEPROM	No operation	Can operate *
	External Interrupt	INT1, INT2, and INT4 can operate. Only INT0 can not operate.	
	CPU	No operation	
Release Signal		An interrupt request signal from a hardware whose operation is enabled by the interrupt enable flag or the $\overline{RESET}$ input.	An interrupt request signal from a hardware whose operation is enabled by the interrupt enable flag or the $\overline{RESET}$ input.

*: Operation is possible only when the main system clock is operating.

9. RESET FUNCTION

When the $\overline{\text{RESET}}$ signal is input, the μPD75048 is reset and each hardware is initialized as indicated in Table 9-1. Fig. 9-1 shows the reset operation timing.

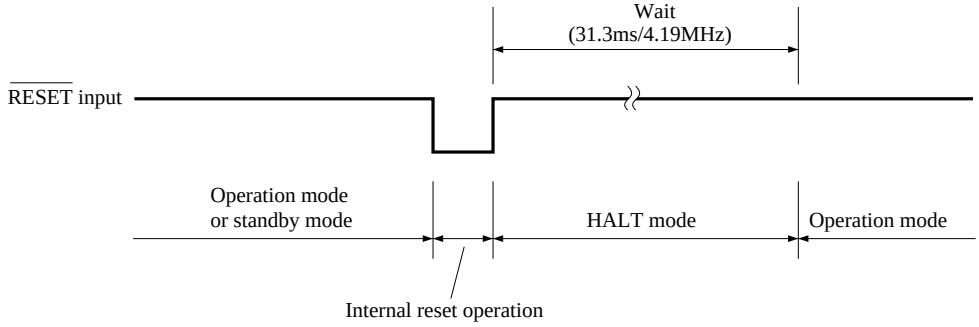


Fig. 9-1 Reset Operation by $\overline{\text{RESET}}$ Input

Table 9-1 Status of Each Hardware after Reset (1/2)

Hardware		$\overline{\text{RESET}}$ Input in Standby Mode	$\overline{\text{RESET}}$ Input During Operation
Program Counter (PC)		The contents of the lower 5 bits of address 0000H of the program memory are set to PC12-8, and the contents of address 0001H are set to PC7-0.	The contents of the lower 5 bits of address 0000H of the program memory are set to PC12-8, and the contents of address 0001H are set to PC7-0.
PSW	Carry Flag (CY)	Retained	Undefined
	Skip Flag (SK0-2)	0	0
	Interrupt Status Flag (IST0)	0	0
	Bank Enable Flag (MBE)	The contents of bit 7 of address 0000H of the program memory is set to MBE.	The contents of bit 7 of address 0000H of the program memory is set to MBE.
Stack Pointer (SP)		Undefined	Undefined
Data Memory (RAM)		Retained *	Undefined
Data Memory (EEPROM)	EEPROM	Contents of address being written is undefined.	Contents of address being written is undefined.
	EEPROM Write Control Register	0	0
General-Purpose Register (X, A, H, L, D, E, B, C)		Retained	Undefined
Bank Selection Register (MBS)		0	0
Basic Interval Timer	Counter (BT)	Undefined	Undefined
	Mode Register (BTM)	0	0
Timer/Event Counter	Counter (T0)	0	0
	Modulo Register (TMOD0)	FFH	FFH
	Mode Register (TM0)	0	0
	TOE0, TOUT F/F	0, 0	0, 0
Watch Timer	Mode Register (WM)	0	0

*: The data at the addresses 0F8H-0FDH of data memory is undefined by $\overline{\text{RESET}}$ input.

Table 9-1 Status of Each Hardware after Reset (2/2)

Hardware			$\overline{\text{RESET}}$ Input in Standby Mode	$\overline{\text{RESET}}$ Input During Operation
Serial Interface	Shift Register (SIO)		Retained	Undefined
	Operation Mode Register (CSIM)		0	0
	SBI Control Register (SBIC)		0	0
	Slave Address Register (SVA)		Retained	Undefined
Clock Generator, Clock Output Circuit	Processor Clock Control Register (PCC)		0	0
	System Clock Control Register (SCC)		0	0
	Clock Output Mode Register (CLOM)		0	0
★ Interrupt Function	Interrupt request flag (IRQxxx)	IRQ1, IRQ2, IRQ4	Undefined	Undefined
		Other than above	0	0
	Interrupt Enable Flag (IExxx)		0	0
	Interrupt Master Enable Flag (IME)		0	0
	INT0, INT1, INT2 Mode Registers (IM0, IM1, IM2)		0, 0, 0	0, 0, 0
Digital Port	Output Buffer		Off	Off
	Output Latch		Clear (0)	Clear (0)
	Input/Output Mode Register (PMGA, PMGB, PMGC)		0	0
	Pull-up Resistor Specification Register (POGA, POGB)		0	0
	Pull-down Resistor Specification Register (PDGB)		0	0
Multi-Function Timer	Counter (MFTL)		FFH	FFH
	Counter (MFTH)		0	0
	Mode Register (MFTM)		0	0
	Control Register (MFTC)		0	0
A/D Converter	Mode Register (ADM)		04H	04H
	SA Register (SA)		Retained	Undefined
Bit sequential buffer (BSB0-3)			Retained	Undefined

10. INSTRUCTION SET

(1) Operand representation and description

Describe one or more operands in the operand field of each instruction according to the operand representation and description methods of the instruction (for details, refer to RA75X Assembler Package User's Manual - Language (EEU-730). With some instructions, only one operand should be selected from several operands. The uppercase characters, +, and - are keywords and must be described as is.

Describe an appropriate numeric value or label as immediate data.

The symbols of the register flags can be described in the places of mem, fmem, pmem, and bit. (For details, refer to μPD75048 User's Manual (IEU-704). However, fmem and pmem restricts the label that can be described.

Representation	Description
reg reg1	X, A, B, C, D, E, H, L X, B, C, D, E, H, L
rp rp1 rp2	XA, BC, DE, HL BC, DE, HL BC, DE
rpa rpa1	HL, DE, DL DE, DL
n4 n8	4-bit immediate data or label 8-bit immediate data or label
mem* bit	8-bit immediate data or label 2-bit immediate data or label
fmem pmem	FB0H to FBFH, FF0H to FFFH immediate data or label FC0H to FFFH immediate data or label
addr caddr faddr	0000H to 1F7FH immediate data or label 12-bit immediate data or label 11-bit immediate data or label
taddr	20H to 7FH immediate data (where bit0=0) or label
PORTn IExxx MBn	PORT0 to PORT11 IEBT, IECSI, IET0, IE0, IE1, IE2, IE4, IEW, IEMFT, IEEE, IEOW MB0, MB1, MB4, MB5, MB6, MB7, MB15

*: Only even addresses can be described as mem for 8-bit data processing.

(2) Legend of operation field

A	:	A register; 4-bit accumulator
B	:	B register; 4-bit accumulator
C	:	C register; 4-bit accumulator
D	:	D register; 4-bit accumulator
E	:	E register; 4-bit accumulator
H	:	H register; 4-bit accumulator
L	:	L register; 4-bit accumulator
X	:	X register; 4-bit accumulator
XA	:	Register pair (XA); 8-bit accumulator
BC	:	Register pair (BC); 8-bit accumulator
DE	:	Register pair (DE); 8-bit accumulator
HL	:	Register pair (HL); 8-bit accumulator
PC	:	Program counter
SP	:	Stack pointer
CY	:	Carry flag; or bit accumulator
PSW	:	Program status word
MBE	:	Memory bank enable flag
PORTn	:	Port n (n = 0 to 11)
IME	:	Interrupt master enable flag
IExxx	:	Interrupt enable flag
MBS	:	Memory bank selector register
PCC	:	Processor clock control register
·	:	Delimiter of address and bit
(xx)	:	Contents addressed by xx
xxH	:	Hexadecimal data

(3) Symbols in addressing area field

*1	MB = MBE · MBS (MBS = 0, 1, 15)	Data memory addressing
*2	MB = 0	
*3	MBE = 0 : MB = 0 (00H-7FH) MB = 15 (80H-FFH) MBE = 1 : MB = MBS (MBS = 0, 1, 15)	
*4	MB = 15, fmem = FB0H-FBFH, FF0H-FFFH	
*5	MB = 15, pmem = FC0H-FFFH	
*6	addr = 0000H-1F7FH	Program memory addressing
*7	addr = (Current PC) -15 to (Current PC) - 1 (Current PC) +2 to (Current PC) + 16	
*8	caddr = 0000H-0FFFH (PC_{12} = 0) or 1000H-1F7FH (PC_{12} = 1)	
*9	faddr = 0000H-07FFH	
*10	taddr = 0020H-007FH	
*11	MB = MBE · MBS (MBS = 0, 1, 4, 5, 6, 7, 15)	Data memory addressing
*12	MBE = 0: MB = 0 (00H-7FH) MB = 15 (80H-FFH) MBE = 1: MB = MBS (MBS = 0, 1, 4, 5, 6, 7, 15)	

Remarks 1: MB indicates memory bank that can be accessed.

2: In *2, MB = 0 regardless of MBE and MBS.

3: In *4 and *5, MB = 15 regardless of MBE and MBS.

4: *6 to *10 indicate areas that can be addressed.

5: When MBS is 4, 5, 6 or 7, addressing area is in the EEPROM area.

(4) Machine cycle field

In this field, S indicates the number of machine cycles required when an instruction having a skip function skips. The value of S varies as follows:

- When no instruction is skipped ..... S = 0
- When 1-byte or 2-byte instruction is skipped ..... S = 1
- When 3-byte instruction (BR !addr or CALL !addr) is skipped ..... S = 2

Note : The GETI instruction is skipped in one machine cycle.

One machine cycle equals to one cycle of the CPU clock Φ, ($=t_{CY}$), and can be changed in three steps depending on the setting of the processor clock control register (PCC).

Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Transfer	MOV	A, #n4	1	1	A ← n4		String effect A
		reg1, #n4	2	2	reg1 ← n4		
		XA, #n8	2	2	XA ← n8		String effect A
		HL, #n8	2	2	HL ← n8		String effect B
		rp2, #n8	2	2	rp2 ← n8		
		A, @HL	1	1	A ← (HL)	*11	
		A, @rpa1	1	1	A ← (rpa1)	*2	
		XA, @HL	2	2	XA ← (HL)	*11	
		@HL, A	1	1	(HL) ← A	*11	
		@HL, XA	2	2	(HL) ← XA	*11	
		A,mem	2	2	A ← (mem)	*12	
		XA, mem	2	2	XA ← (mem)	*12	
		mem, A	2	2	(mem) ← A	*12	
		mem, XA	2	2	(mem) ← XA	*12	
		A, reg	2	2	A ← reg		
		XA, rp	2	2	XA ← rp		
		reg1, A	2	2	reg1 ← A		
		rp1, XA	2	2	rp1 ← XA		
	XCH	A, @HL	1	1	A ↔ (HL)	*11	
		A, @rpa1	1	1	A ↔ (rpa1)	*2	
		XA, @HL	2	2	XA ↔ (HL)	*11	
		A, mem	2	2	A ↔ (mem)	*12	
		XA, mem	2	2	XA ↔ (mem)	*12	
		A, reg1	1	1	A ↔ reg1		
		XA, rp	2	2	XA ↔ rp		
Table Reference	MOVT	XA, @PCDE	1	3	XA ← $(PC_{12-8}+DE)_{ROM}$		
		XA, @PCXA	1	3	XA ← $(PC_{12-8}+XA)_{ROM}$		
Arithmetic Operation	ADDS	A, #n4	1	1+S	A ← A+n4		carry
		A, @HL	1	1+S	A ← A+(HL)	*11	carry
	ADDC	A, @HL	1	1	A, CY ← A+(HL)+CY	*11	
	SUBS	A, @HL	1	1+S	A ← A-(HL)	*11	borrow
	SUBC	A, @HL	1	1	A, CY ← A-(HL)-CY	*11	
	AND	A, #n4	2	2	A ← A ∧ n4		
		A, @HL	1	1	A ← A ∧ (HL)	*11	
	OR	A, #n4	2	2	A ← A ∨ n4		
		A, @HL	1	1	A ← A ∨ (HL)	*11	
	XOR	A, #n4	2	2	A ← A ∨̄ n4		
		A, @HL	1	1	A ← A ∨̄ (HL)	*11	
Accumulator Manipulation	RORC	A	1	1	CY ← A_0, A_3 ← CY, A_{n-1} ← A_n		
	NOT	A	2	2	A ← $\overline{A}$		

Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Increment/ Decrement	INCS	reg	1	1+S	reg ← reg+1		reg = 0
		@HL	2	2+S	(HL) ← (HL)+1	*11	(HL) = 0
		mem	2	2+S	(mem) ← (mem)+1	*12	(mem) = 0
	DECS	reg	1	1+S	reg ← reg-1		reg = FH
Compare	SKE	reg, #n4	2	2+S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2+S	Skip if (HL) = n4	*11	(HL) = n4
		A, @HL	1	1+S	Skip if A = (HL)	*11	A = (HL)
		A, reg	2	2+S	Skip if A = reg		A = reg
Carry flag Manipulation	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1+S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	CY ← $\overline{CY}$		
Memory/ Bit Manipulation	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ← 1	*4	
		pmem.@L	2	2	($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0})) ← 1	*5	
		@H+mem.bit	2	2	(H + mem_{3-0}.bit) ← 1	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0}) ← 0	*5	
		@H+mem.bit	2	2	(H+mem_{3-0}.bit) ← 0	*1	
	SKT	mem.bit	2	2+S	Skip if(mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2+S	Skip if(fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2+S	Skip if($pmem_{7-2}$+L_{3-2}.bit (L_{1-0})) = 1	*5	(pmem.@L) = 1
		@H+mem.bit	2	2+S	Skip if(H + mem_{3-0}.bit) = 1	*1	(@H+mem.bit) = 1
	SKF	mem.bit	2	2+S	Skip if(mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2+S	Skip if(fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2+S	Skip if($pmem_{7-2}$ +L_{3-2}.bit (L_{1-0})) = 0	*5	(pmem.@L) = 0
		@H+mem.bit	2	2+S	Skip if (H + mem_{3-0}.bit) = 0	*1	(@H+mem.bit) = 0
	SKTCLR	fmem.bit	2	2+S	Skip if(fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2+S	Skip if($pmem_{7-2}$+L_{3-2}.bit (L_{1-0})) = 1 and clear	*5	(pmem.@L) = 1
		@H+mem.bit	2	2+S	Skip if (H+mem_{3-0}.bit) = 1 and clear	*1	(@H+mem.bit) = 1
	AND1	CY,fmem.bit	2	2	CY ← CY ∧ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY ∧ ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))	*5	
		CY,@H+mem.bit	2	2	CY ← CY ∧ (H+mem_{3-0}.bit)	*1	
	OR1	CY,fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY ∨ ($pmem_{7-2}$+L_{3-2}.bit (L_{1-0}))	*5	
		CY,@H+mem.bit	2	2	CY ← CY ∨ (H+mem_{3-0}.bit)	*1	
	XOR1	CY,fmem.bit	2	2	CY ← CY ⊻ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY ⊻ ($pmem_{7-2}$+L_{3-2}.bit (L_{1-0}))	*5	
		CY,@H+mem.bit	2	2	CY ← CY ⊻ (H+mem_{3-0}.bit)	*1	

Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Branch	BR	addr	—	—	$PC_{12-0} \leftarrow$ addr (The most suitable instruction is selectable from among BR !addr, BRCB !caddr, and BR $addr depending on the assembler.)	*6	
		!addr	3	3	$PC_{12-0} \leftarrow$ addr	*6	
		$addr	1	2	$PC_{12-0} \leftarrow$ addr	*7	
	BRCB	!caddr	2	2	$PC_{12-0} \leftarrow PC_{12} +$ caddr$_{11-0}$	*8	
Subroutine/ Stack Control	CALL	!addr	3	3	(SP-4)(SP-1)(SP-2) $\leftarrow PC_{11-0}$ (SP-3) $\leftarrow$ MBE,0, 0, PC_{12} $PC_{12-0} \leftarrow$ addr,SP $\leftarrow$ SP-4	*6	
	CALLF	!faddr	2	2	(SP-4)(SP-1)(SP-2) $\leftarrow PC_{11-0}$ (SP-3) $\leftarrow$ MBE,0, 0, PC_{12} $PC_{12-0} \leftarrow$ 00,faddr,SP $\leftarrow$ SP-4	*9	
	RET		1	3	MBE,x,x,$PC_{12} \leftarrow$ (SP+1) $PC_{11-0} \leftarrow$ (SP)(SP+3)(SP+2) SP $\leftarrow$ SP+4		
	RETS		1	3+S	MBE,x,x,$PC_{12} \leftarrow$ (SP+1) $PC_{11-0} \leftarrow$ (SP)(SP+3)(SP+2) SP $\leftarrow$ SP+4, then skip unconditionally		Unconditional
	RETI		1	3	MBE,x,x,$PC_{12} \leftarrow$ (SP+1) $PC_{11-0} \leftarrow$ (SP)(SP+3)(SP+2) PSW $\leftarrow$ (SP+4)(SP+5), SP $\leftarrow$ SP+6		
	PUSH	rp	1	1	(SP-1)(SP-2) $\leftarrow$ rp, SP $\leftarrow$ SP-2		
		BS	2	2	(SP-1) $\leftarrow$ MBS,(SP-2) $\leftarrow$ 0,SP $\leftarrow$ SP-2		
	POP	rp	1	1	rp $\leftarrow$ (SP+1)(SP),SP $\leftarrow$ SP+2		
		BS	2	2	MBS $\leftarrow$ (SP+1),SP $\leftarrow$ SP+2		
Interrupt Control	EI		2	2	IME $\leftarrow$ 1		
		IExxx	2	2	IExxx $\leftarrow$ 1		
	DI		2	2	IME $\leftarrow$ 0		
		IExxx	2	2	IExxx $\leftarrow$ 0		
I/O	IN	A,PORTn	2	2	A $\leftarrow PORT_n$ (n = 0-11)		
		XA,PORTn	2	2	XA $\leftarrow PORT_{n+1},PORT_n$ (n = 4, 6)		
	OUT	PORTn,A	2	2	$PORT_n \leftarrow$ A (n = 2-10)		
		PORTn,XA	2	2	$PORT_{n+1},PORT_n \leftarrow$ XA (n = 4, 6)		
CPU Control	HALT		2	2	Set HALT Mode(PCC.2 $\leftarrow$ 1)		
	STOP		2	2	Set STOP Mode (PCC.3 $\leftarrow$ 1)		
	NOP		1	1	No Operation		
Special	SEL	MBn	2	2	MBS $\leftarrow$ n(n=0, 1, 4, 5, 6, 7, 15)		
	GETI	taddr	1	3	· Where TBR instruction, $PC_{12-0} \leftarrow$ (taddr)$_{4-0}$+(taddr+1)	*10	
					· Where TCALL instruction, (SP-4)(SP-1)(SP-2) $\leftarrow PC_{11-0}$ (SP-3) $\leftarrow$ MBE, 0, 0, PC_{12} $PC_{12-0} \leftarrow$ (taddr)$_{4-0}$+(taddr+1) SP $\leftarrow$ SP-4		
					· Except for TBR and TCALL instructions, Instruction execution of (taddr)(taddr+1)		Depends on referenced instruction

Note : When executing the IN/OUT instruction, MBE = 0, or MBE = 1, and MBS = 15.

★ *Remarks* : TBR and TCALL instructions are assembler seudo-instructions for the table definition of GETI instruction.

11. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply Voltage	V_{DD}			-0.3 to +7.0	V
Input Voltage	V_{I1}	Other than ports 4, 5, 10		-0.3 to V_{DD}+0.3	V
	V_{I2}	Ports 4, 5, 10	w/pull-up resistor	-0.3 to V_{DD}+0.3	V
			Open drain	-0.3 to +11	V
Output Voltage	V_O			-0.3 to V_{DD}+0.3	V
High-Level Output Current	I_{OH}	1 pin		-10	mA
		All pins		-30	mA
Low-Level Output Current	I_{OL}*	Ports 0, 3, 4, 5 1 pin	Peak	30	mA
			rms	15	mA
		Other than ports 0, 3, 4, 5 1 pin	Peak	20	mA
			rms	5	mA
		Total of ports 0, 3 - 9, 11	Peak	170	mA
			rms	120	mA
		Total of ports 0, 2, 10	Peak	30	mA
			rms	20	mA
Operating Temperature	T_{opt}			-10 to +70	°C
Storage Temperature	T_{stg}			-65 to +150	°C

*: rms = Peak value x $\sqrt{Duty}$

Note: Even if one of the parameters exceeds its absolute maximum rating even momentarily, the quality of the product may be degraded. The absolute maximum rating therefore specifies the upper or lower limit of the value at which the product can be used without physical damages. Be sure not to exceed or fall below this value when using the product. ★

EEPROM RATINGS (T_a = -10 to +70°C, V_{DD} = 2.7 to 6.0 V)

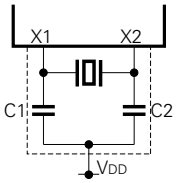
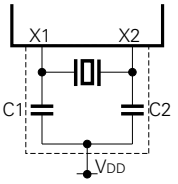
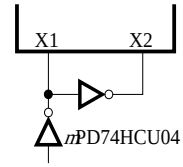
Parameter	Symbol	Conditions	μ	
Write Times	—		100,000	times
Data Retention Time	—		10	years

CAPACITANCE (T_a = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_I	f = 1 MHz			15	pF
Output Capacitance	C_O	Pins other than thosemeasured are at 0 V			15	pF
Input/Output	C_{IO}				15	pF

MAIN SYSTEM CLOCK OSCILLATOR CIRCUIT CHARACTERISTICS

(T_a = -10 to +70°C, V_{DD} = 2.7 to 6.0 V)

Oscillator	Recommended Constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic		Oscillation frequency(f_X)*1	V_{DD} = oscillation voltage range	2.0		5.0*3	MHz
		Oscillation stabilization time*2	After V_{DD} come to MIN. value of oscillation voltage range			4	ms
Crystal		Oscillation frequency (f_X)*1		2.0	4.19	5.0*3	MHz
		Oscillation stabilization time*2	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External Clock		X1 input frequency (f_X)*1		2.0		5.0*3	MHz
		X1 input high-, low-level widths (t_{XH}, t_{XL})		100		250	ns

*1: Only to express the characteristics of the oscillator circuit. For instruction execution time, refer to AC Characteristics.

2: Time required for oscillation to stabilize after V_{DD} has reached the minimum volue of the oscillation voltage range or the STOP mode has been released.

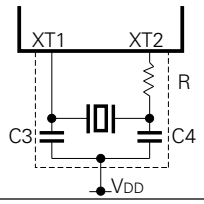
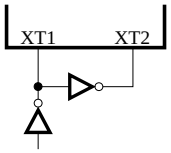
3: When the oscillation frequency is 4.19 MHz < fx ≤ 5.0 MHz, do not select PCC = 0011 as the instruction execution time: otherwise, one machine cycle is set to less than 0.95 μs, falling short of the rated minimum value of 0.95 μs.

★ **Note**: When using the oscillation circuit of the main system clock, wire the portion enclosed in dotted line in the figures as follows to avoid adverse influences on the wiring capacity:

- Keep the wiring length as short as possible.
- Do not cross the wiring over the other signal lines.
- Do not route the wiring in the vicinity of lines through which a high alternating current flows.
- Always keep the ground point of the capacitor of the oscillator circuit at the same potential as V_{DD}. Do not connect the ground pattern through which a high curent flows.
- Do not extract signals from the oscillation circuit.

SUBSYSTEM CLOCK OSCILLATOR CIRCUIT CHARACTERISTICS

(T_a = -10 to +70°C, V_{DD} = 2.7 to 6.0 V)

Oscillator	Recommended Constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
Crystal		Oscillation frequency (f_{XT})*1		32	32.768	35	kHz
		Oscillation stabilization time*2	V_{DD} = 4.5 to 6.0 V		1.0	2	ms
						10	ms
External Clock		XT1 input frequency (f_{XT})*1		32		100	kHz
		XT1 input high-, low-level widths (t_{XTH}, t_{XTL})		5		15	μs

*1: Indicates only the characteristics of the oscillator circuit. For instruction execution time, refer to AC Characteristics.

2: Time required for oscillation to stabilize after V_{DD} has reached the minimum value of the oscillation voltage range.

Note: When using the oscillation circuit of the subsystem clock, wire the portion enclosed in dotted line in the figures as follows to avoid adverse influences on the wiring capacity: ★

- Keep the wiring length as short as possible.
- Do not cross the wiring over the other signal lines.
- Do not route the wiring in the vicinity of lines through which a high alternating current flows.
- Always keep the ground point of the capacitor of the oscillator circuit at the same potential as V_{DD}. Do not connect the ground pattern through which a high current flows.
- Do not extract signals from the oscillation circuit.

The amplification factor of the subsystem clock oscillation circuit is designed to be low to reduce the current dissipation and therefore, the subsystem clock oscillation circuit is influenced by noise more easily than the main system clock oscillation circuit. When using the subsystem clock, therefore, exercise utmost care in wiring the circuit.

DC CHARACTERISTICS (T_a = -10 to +70°C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-Level Input Voltage	V_{IH1}	Ports 2,3,8,9,11		0.7V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0,1,6,7, $\overline{RESET}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4,5,10	w/pull-up resistor	0.7V_{DD}		V_{DD}	V
			Open-drain	0.7V_{DD}		10	V
	V_{IH4}	X1, X2, XT1, XT2		V_{DD}-0.5		V_{DD}	V
Low-level Input Voltage	V_{IL1}	Ports 2-5, 8-11		0		0.3V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7, $\overline{RESET}$		0		0.2V_{DD}	V
	V_{IL3}	X1, X2, XT1, XT2		0		0.4	V
High-Level Output Voltage	V_{OH}	V_{DD} = 4.5 to 6.0V, I_{OH} = -1 mA		V_{DD}-1.0			V
		I_{OH} = -100 μA		V_{DD}-0.5			V
Low-Level Output Voltage	V_{OL}	Ports 3,4,5	V_{DD} = 4.5 to 6.0V, I_{OL} = 15mA		0.4	2.0	V
		V_{DD} = 4.5 to 6.0V, I_{OL} = 1.6 mA				0.4	V
		I_{OL} = 400 μA				0.5	V
		SB0, 1	Open-drain pull-up resistor ≥ 1 kΩ			0.2V_{DD}	V
High-Level Input Leakage Current	I_{LIH1}	V_I = V_{DD}	Other than below			3	μA
	I_{LIH2}		X1,X2,XT1			20	μA
	I_{LIH3}	V_I = 9V	Ports 4,5,10 (open-drain)			20	μA
Low-Level Input Leakage Current	I_{LIL1}	V_I = 0V	Other than below			-3	μA
	I_{LIL2}		X1,X2,XT1			-20	μA
High-Level Output Leakage Current	I_{LOH1}	V_O = V_{DD}	Other than below			3	μA
	I_{LOH2}	V_O = 9V	Ports 4,5,10 (open-drain)			20	μA
Low-Level Output Leakage Current	I_{LOL}	V_O = 0V				-3	μA
Internal Pull-Up Resistor	R_{U1}	Ports 0,1,2,3,6,7,8 (except P00) V_I = 0V	V_{DD} = 5.0V±10%	15	40	80	kΩ
			V_{DD} = 3.0V±10%	30		300	kΩ
	R_{U2}	Ports 4,5,10 V_O = V_{DD}-2.0 V	V_{DD} = 5.0V±10%	15	40	70	kΩ
			V_{DD} = 3.0V±10%	10		60	kΩ
Internal Pull-Down Resistor	R_D	Port 9 V_{IN} = V_{DD}	V_{DD} = 5.0V±10%	15	40	70	kΩ
			V_{DD} = 3.0V±10%	10		60	kΩ

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply Current *1	I_{DD1}	4.19MHz crystal oscillator C1 = C2 = 22pF	V_{DD} = 5V±10%*2			3.5	10	mA
			V_{DD} = 3V±10%*3			0.65	1.8	mA
	I_{DD2}		HALT mode	V_{DD} = 5V±10%		800	2400	μA
				V_{DD} = 3V±10%		350	1000	μA
	I_{DD3}	32.768kHz*4 crystal oscillator	Operation mode	V_{DD} = 3V±10%		70	210	μA
	I_{DD4}		HALT mode	V_{DD} = 3V±10%		20	60	μA
	I_{DD5}	XT1 = 0V STOP mode	V_{DD} = 5V±10%			0.5	20	μA
			V_{DD} = 3V±10%			0.3	10	μA
				T_a = 25°C			5	μA
	I_{DD6}	32.768kHz oscillator STOP mode	V_{DD} = 3V±10%*5			6	20	μA

*1: Current flowing through internal pull-up resistor. Current flowing when EEPROM is accessed is not included.

2: When μPD75048 operates in high-speed mode with processor clock control register (PCC) set to 0011.

3: When μPD75048 operates in low-speed mode with PCC set to 0000.

4: When the system clock control register (SCC) is set to 1001, the oscillation of the main system clock is stopped, and the subsystem clock is used.

5: When STOP instruction is executed with SCC set to 0000.

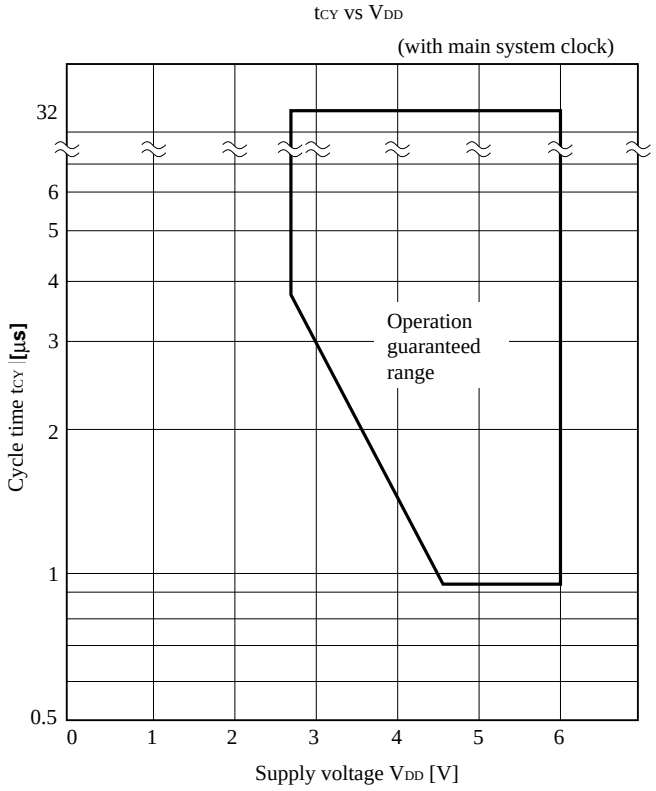
Note: Supply current when EEPROM is accessed is shown in EEPROM Characteristics.

AC CHARACTERISTICS (T_a = -10 to +70°C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU Clock Cycle Time (Minimum Instruction Execution Time = 1 Machine Cycle)*1	t_{CY}	w/main system clock	V_{DD} = 4.5-6.0V	0.95		32	μs
				3.8		32	μs
		w/subsystem clock		114	122	125	μs
TI0 Input Frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		1	MHz
				0		275	kHz
TI0 Input High-, Low-Level Widths	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.48			μs
				1.8			μs
Interrupt Input High-, Low-Level Widths	t_{INTH}, t_{INTL}	INT0		*2			μs
		INT1, 2, 4		10			μs
		KR0-7		10			μs
$\overline{RESET}$ Low-Level Width	t_{RSL}			10			μs

*1: The CPU clock (Φ) cycle time is determined by the oscillation frequency of the connected oscillator, system clock control register (SCC), and processor clock control register (PCC).
The figure on the right is cycle time t_{CY} vs. supply voltage V_{DD} characteristics at the main system clock.

*2: $2t_{CY}$ or $128/f_X$ depending on the setting of the interrupt mode register (IM0).



SERIAL TRANSFER OPERATION

Two-Line and Three-Line Serial I/O Modes ($\overline{SCK}$: internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL1}	V_{DD} = 4.5 to 6.0 V		t_{KCY1}/2-50			ns
	t_{KH1}			t_{KCY1}/2-150			ns
SI Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK1}			150			ns
SI Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI1}			400			ns
$\overline{SCK}$ ↓→ SO Output Delay Time	t_{KSO1}	R_L = 1kΩ, C_L = 100pF*	V_{DD} = 4.5 to 6.0V			250	ns
						1000	ns

TWO-LINE AND THREE-LINE SERIAL I/O MODES ($\overline{SCK}$: external clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY2}	V_{DD} = 4.5 to 6.0V		800			ns
				3200			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL2}	V_{DD} = 4.5 to 6.0V		400			ns
	t_{KH2}			1600			ns
SI Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK2}			100			ns
SI Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI2}			400			ns
$\overline{SCK}$ ↓→ SO Output Delay Time	t_{KSO2}	R_L = 1kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0V			300	ns
						1000	ns

*: R_L and C_L are load resistance and load capacitance of the SO output line.

SBI MODE ($\overline{SCK}$: internal clock output (master))

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL3} t_{KH3}	V_{DD} = 4.5 to 6.0 V		t_{KCY3}/2-50			ns
				t_{KCY3}/2-150			ns
SB0, 1 Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK3}			150			ns
SB0, 1 Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI3}			t_{KCY3}/2			ns
$\overline{SCK}$ ↓→ SB0, 1 Output Delay Time	t_{KSO3}	R_L = 1kΩ, C_L = 100pF*	V_{DD} = 4.5 to 6.0V	0		250	ns
				0		1000	ns
$\overline{SCK}$ ↑→ SB0, 1 ↓	t_{KSB}			t_{KCY3}			ns
SB0,1 ↓→ $\overline{SCK}$	t_{SBK}			t_{KCY3}			ns
SB0, 1 Low-Level Width	t_{SBL}			t_{KCY3}			ns
SB0, 1 High-Level Width	t_{SBH}			t_{KCY3}			ns

SBI MODE ($\overline{SCK}$: external clock input (slave))

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ Ligh-, Low-Level Widths	t_{KL4} t_{KH4}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SB0, 1 Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK4}			100			ns
SB0, 1 Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI4}			$t_{KCY4/2}$			ns
$\overline{SCK}$ ↓→ SB0, 1 Output Delay Time	t_{KSO4}	R_L = 1kΩ, C_L = 100pF*	V_{DD} = 4.5 to 6.0V	0		300	ns
				0		1000	ns
$\overline{SCK}$ ↑→ SB0, 1 ↓	t_{KSB}			t_{KCY4}			ns
SB0,1 ↓→ $\overline{SCK}$ ↓	t_{SBK}			t_{KCY4}			ns
SB0, 1 Low-Level Width	t_{SBL}			t_{KCY4}			ns
SB0, 1 High-Level Width	t_{SBH}			t_{KCY4}			ns

*: R_L and C_L are load resistance and load capacitance of the SB0 and SB1 output lines.

A/D CONVERTER (T_a = -10 to +70°C, V_{DD} = 2.7 to 6.0V, AV_{SS} = V_{SS} = 0V)

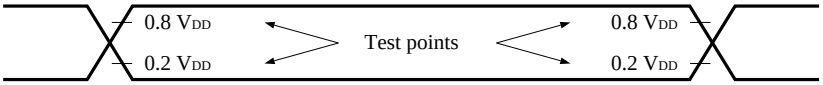
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Absolute Accuracy*1		2.5V ≤ AV_{REF} ≤ V_{DD}			±1.5	LSB
Conversion Time*2	t_{CONV}				168/f_X	μs
Sampling Time*3	t_{SAMP}				44/f_X	μs
Analog Input Voltage	V_{IAN}		AV_{REF-}		AV_{REF+}	V
Analog Supply Voltage	AV_{DD}		2.5		V_{DD}	V
Reference Input Voltage	AV_{REF+}	2.5V ≤ (AV_{ref+}) – (AV_{ref-})	2.5		AV_{DD}	V
Reference Input Voltage	AV_{REF-}	2.5V ≤ (AV_{ref+}) – (AV_{ref-})	0		1.0	V
Analog Input Impedance	R_{AN}			1000		MΩ
AV_{REF} Current	AI_{REF}			0.25	2.0	mA

*1: Absolute accuracy excluding quantization error ($\pm\frac{1}{2}$LSB)

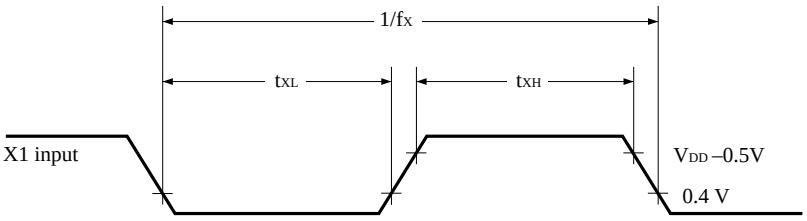
2: Time since execution of conversion start instruction until end of conversion (EOC = 1) (40.1 μs: f_X = 4.19 MHz)

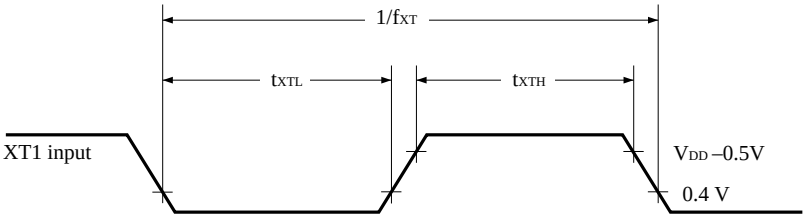
3: Time since execution of conversion start instruction until end of sampling (10.5 μs: f_X = 4.19 MHz)

AC TIMING TEST POINT (excluding X1 and XT1 inputs)

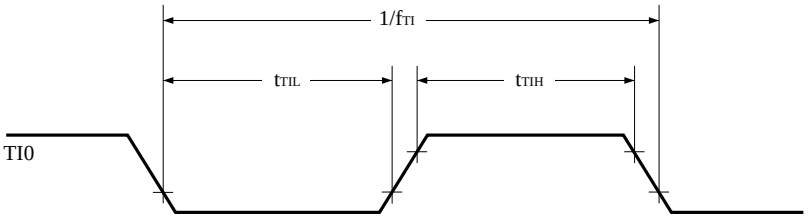


CLOCK TIMING



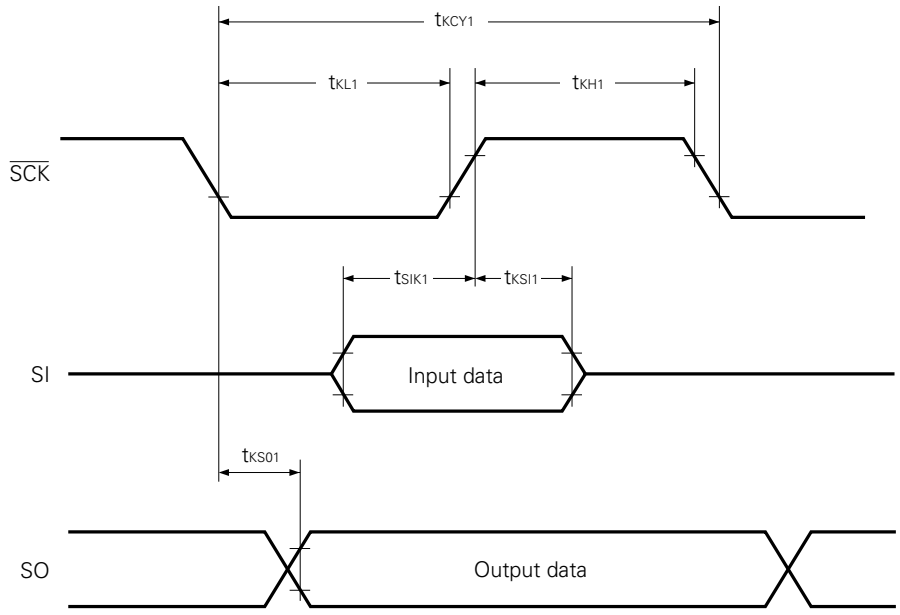


TI0 TIMING

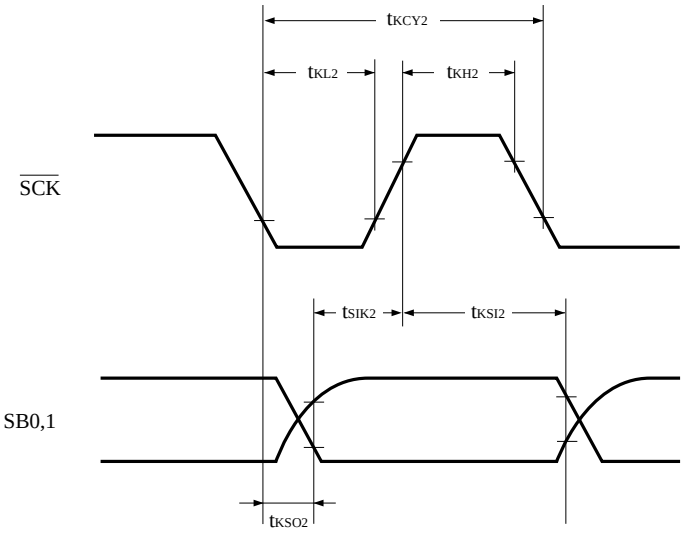


SERIAL TRANSFER TIMING

THREE-LINE SERIAL I/O MODE:

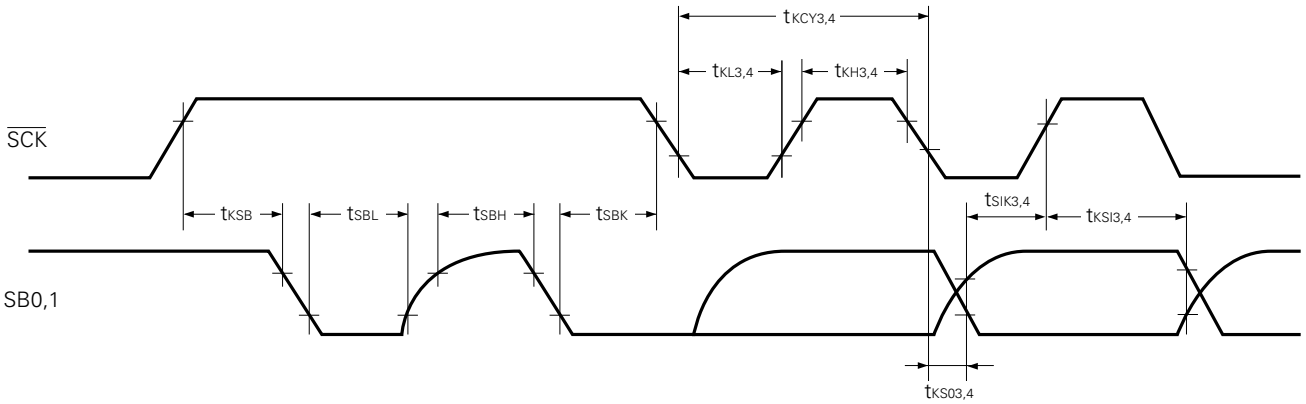


TWO-LINE SERIAL I/O MODE:

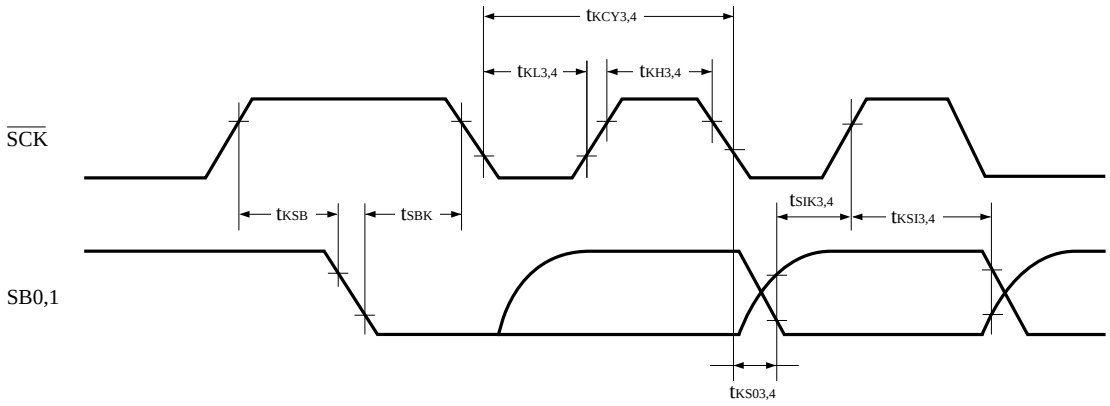


SERIAL TRANSFER TIMING

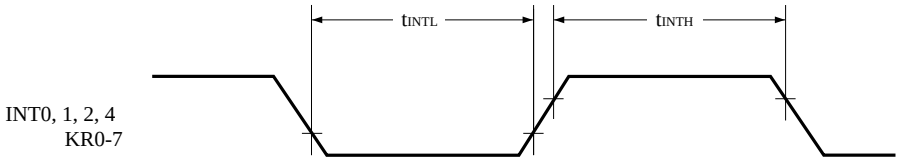
BUS RELEASE SIGNAL TRANSFER:



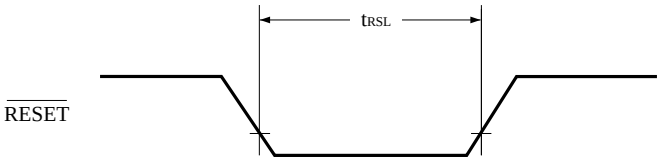
COMMAND SIGNAL TRANSFER:



INTERRUPT INPUT TIMING



RESET INPUT TIMING



EEPROM CHARACTERISTICS

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current for EEPROM access*1	I_{DD7}	4.19MHz crystal oscillator C1 = C = 22pF	V_{DD} = 5V+10%*2		6.5	20	mA
			V_{DD} = 3V+10%*3		2	6	mA

*1: Current flowing through the internal pull-up resistor is not included.

2: When the processor clock control register (PCC) is set to 0011 and the high-speed mode is used.

3: When PCC is set to 0000 and the low-speed mode is used.

EEPROM WRITE TIME

Select the write time of the EEPROM in accordance with the oscillation frequency of the main system clock as follows:

Oscillation Frequency of Main System Clock (f_X)	Setting of EEPROM Control Register		Write time
	EWTC1	EWTC0	
f_X = 2.0 to 5.0 MHz	0	0	2^{12} x 18/f_X (17.6 ms)
f_X = 2.0 to 4.2 MHz	0	1	2^{11} x 18/f_X (8.8 ms)
f_X = 2.0 MHz	1	0	2^{10} x 18/f_X

Remarks: ( ): f_X = 4.19 MHz

LOW-VOLTAGE DATA RETENTION CHARACTERISTICS OF DATA MEMORY IN STOP MODE

(T_a = –10 to +70°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data Retention Supply Voltage	V_{DDDR}		2.0		6.0	V
Data Retention Supply Current*1	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release Signal Set Time	t_{SREL}		0			μs
Oscillation Stabilization Wait Time*2	t_{WAIT}	Released by $\overline{\text{RESET}}$		$2^{17}/f_X$		ms
		Released by interrupt request		*3		ms

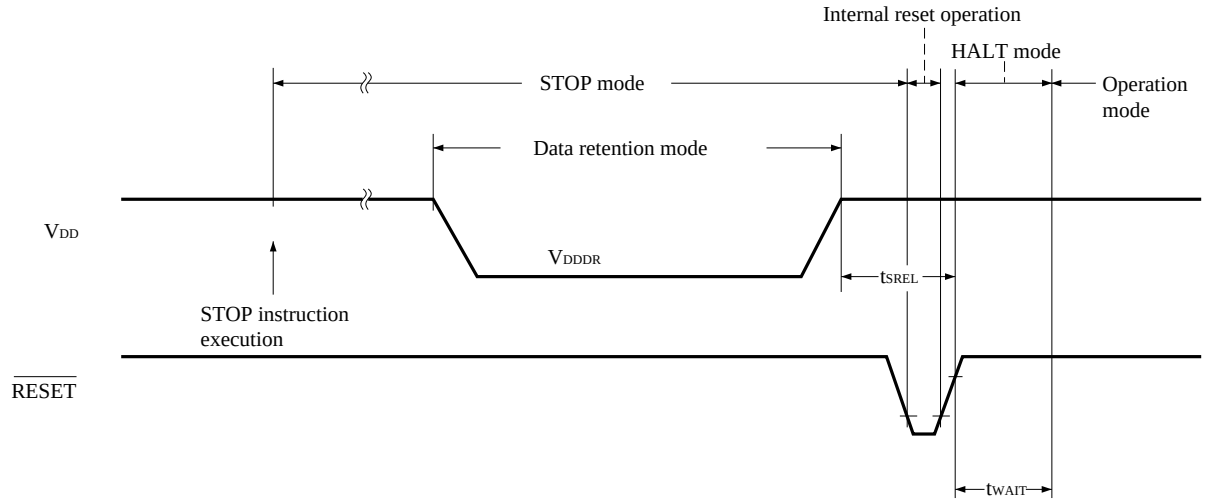
*1: Does not include current flowing through internal pull-up resistor

2: The oscillation stabilization wait time is the time during which the CPU is stopped to prevent unstable operation when oscillation is started.

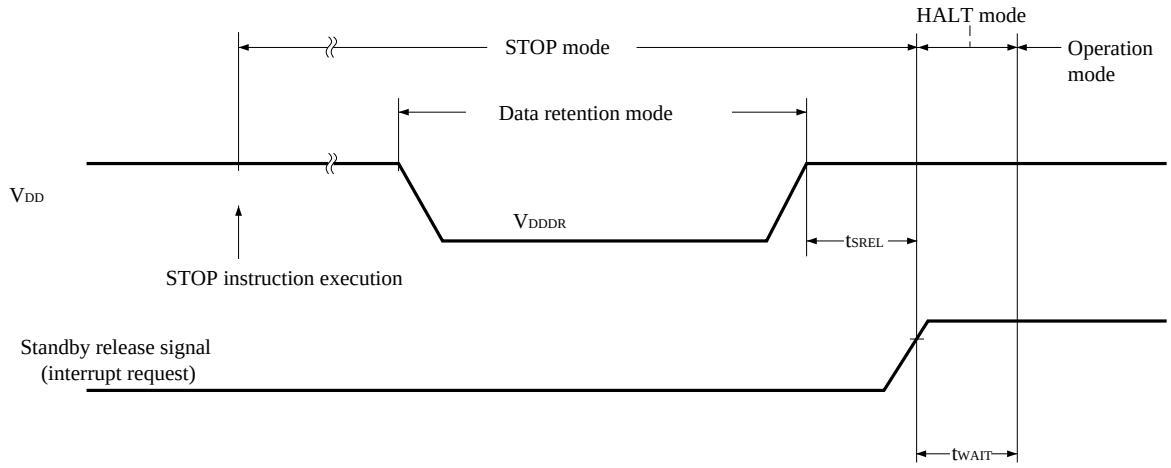
3: Depends on the setting of the basic interval timer mode register (BTM) as follows:

BTM3	BTM2	BTM1	BTM0	WAIT time ( ): f_X = 4.19 MHz
–	0	0	0	$2^{20}/f_X$ (approx. 250 ms)
–	0	1	1	$2^{17}/f_X$ (approx. 31.3 ms)
–	1	0	1	$2^{15}/f_X$ (approx. 7.82 ms)
–	1	1	1	$2^{13}/f_X$ (approx. 1.95 ms)

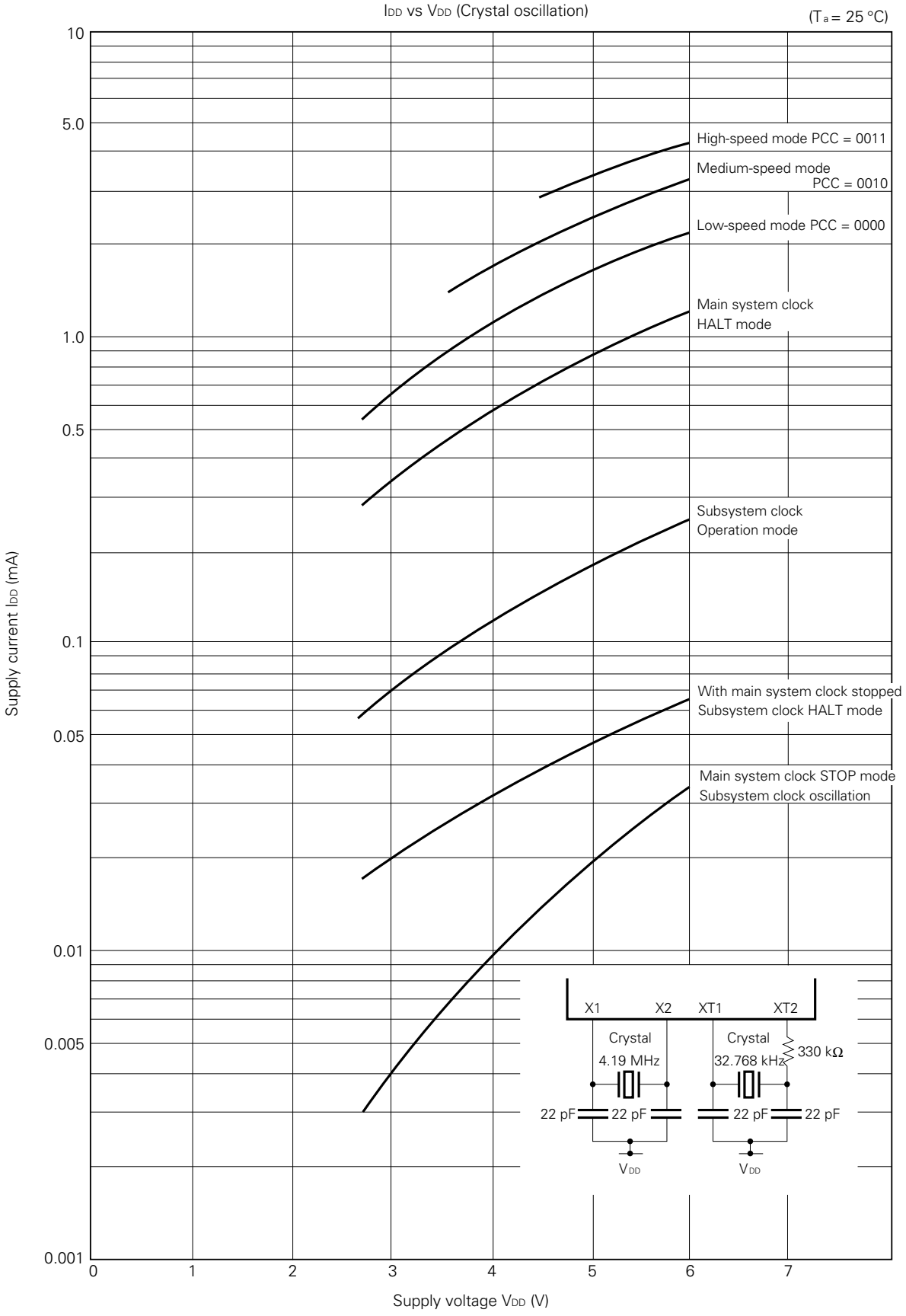
DATA RETENTION TIMING (releasing STOP mode by $\overline{\text{RESET}}$)

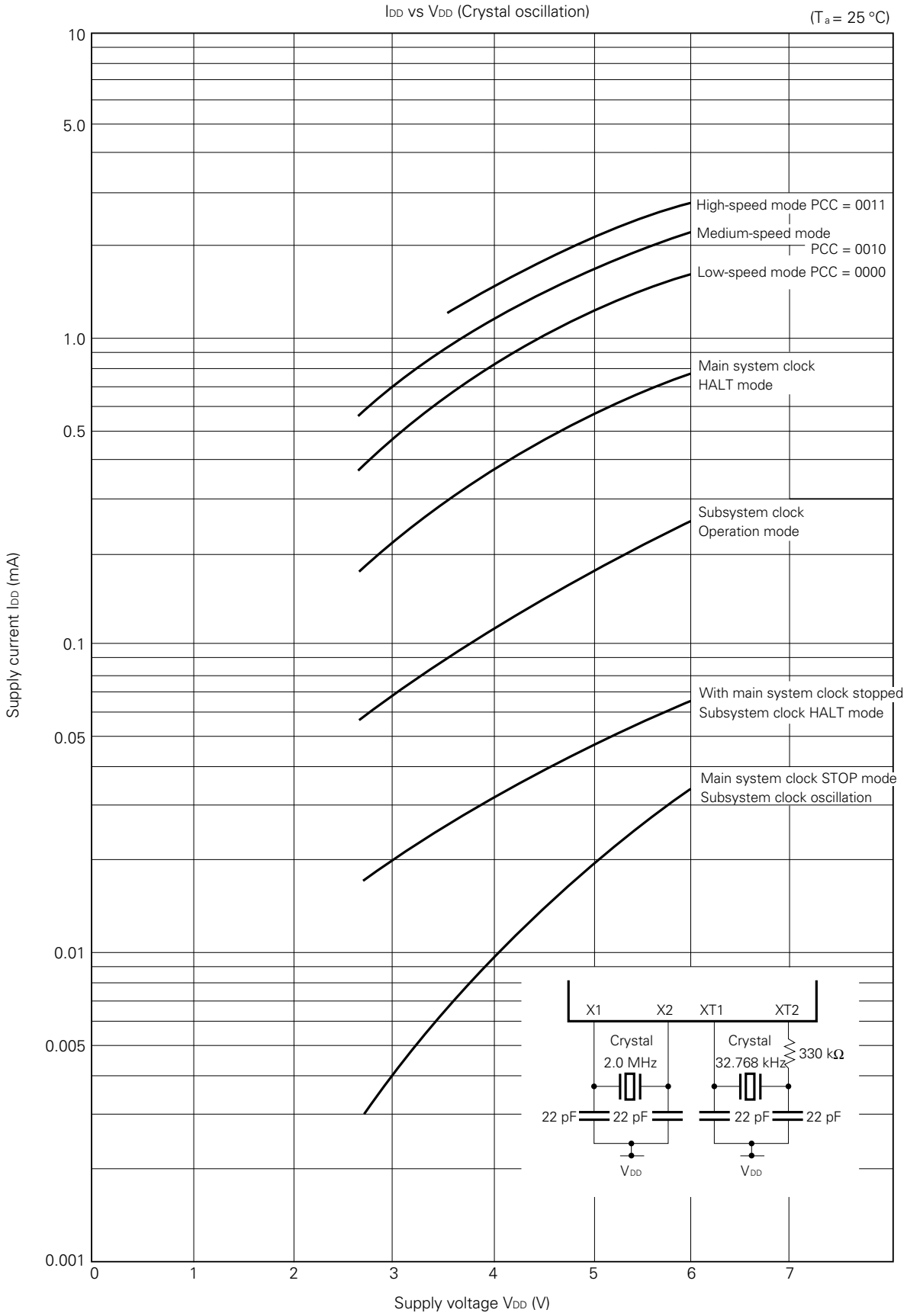


DATA RETENTION TIMING (standby release signal: releasing STOP mode by interrupt)



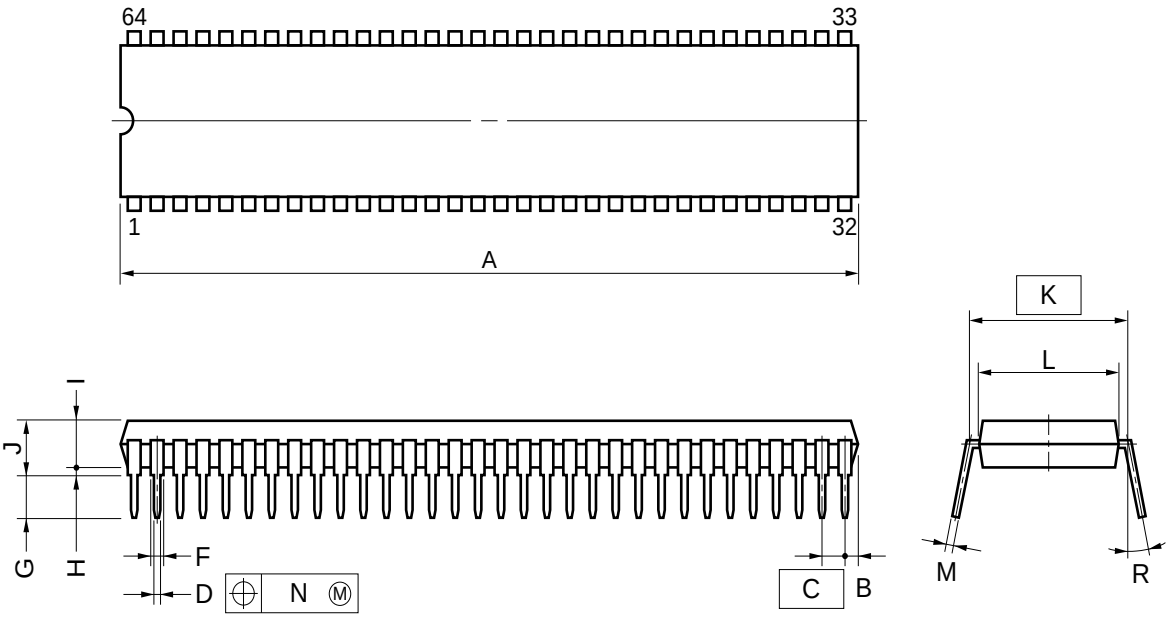
12. PERFORMANCE CURVE




IDD vs VDD (Crystal oscillation)
(Ta = 25 °C)
Supply current IDD (mA)
Supply voltage VDD (V)
10
5.0
1.0
0.5
0.1
0.05
0.01
0.005
0.001
0
1
2
3
4
5
6
7
High-speed mode PCC = 0011
Medium-speed mode
PCC = 0010
Low-speed mode PCC = 0000
Main system clock
HALT mode
Subsystem clock
Operation mode
With main system clock stopped
Subsystem clock HALT mode
Main system clock STOP mode
Subsystem clock oscillation
X1
X2
XT1
XT2
Crystal
2.0 MHz
Crystal
32.768 kHz
330 kΩ
22 pF
22 pF
22 pF
22 pF
VDD
VDD

13. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



NOTE

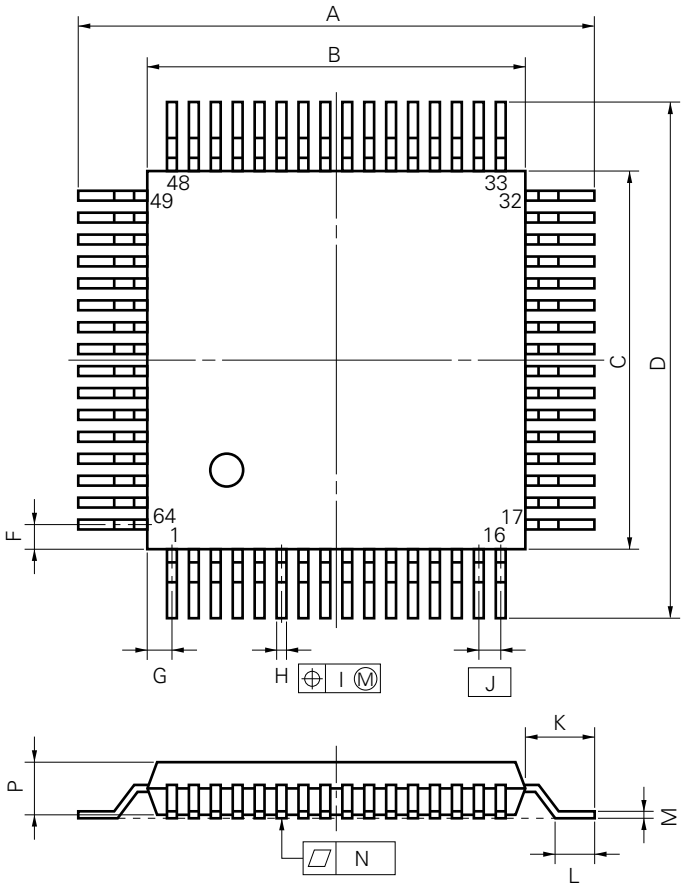
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

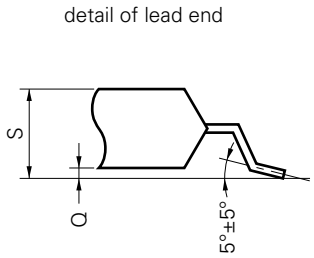
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

64 PIN PLASTIC QFP (□14)





P64GC-80-AB8-3

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

14. RECOMMENDED SOLDERING CONDITIONS

It is recommended that μPD75048 be soldered under the following conditions. For details on the recommended soldering conditions, refer to Information Document "Semiconductor Devices Mounting Manual" (IEI-616). For other soldering methods and conditions, consult NEC.

Table 14-1 Soldering Conditions of Surface Mount Type

μPD75048GC - xxx - AB8: 64-pin plastic QFP (□ 14 mm)

Soldering Method	Soldering Conditions	Symbol for Recommended Condition
Ware Soldering	Soldering bath temperature: 260°C max., time: 10 seconds max., number of times: 1, maximum number of days: 2 days*, (beyond this period, 16 hours of pre-baking is required at 125°C), Pre-heating temperature: 120°C max.	WS60-162-1
Infrared Reflow	Package peak temperature: 230°C, time: 30 seconds max. (210°C min.), number of times: 1, maximum number of days: 2 days* (beyond this period, 16 hours of pre-baking is required at 125°C)	IR30-162-1
VPS	Package peak temperature: 215°C, time: 40 seconds max. (200°C min.), number of times: 1, maximum number of days: 2 days* (beyond this period, 16 hours of pre-baking is required at 125°C)	VP15-162-1
Pin Partial Heating	Pin temperature: 300°C max., time: 3 seconds max. (per side)	—

**:* Number of days after unpacking the dry pack. Storage conditions are 25°C and 65%RH max.

Note: Do not use two or more soldering methods in combination (except the pin partial heating method).

Table 14-2 Soldering Conditions of Through-Hole Type

μPD75048CW - xxx: 64-pin plastic shrink DIP (750 mil)

Soldering Method	Soldering Conditions
Wave soldering (lead parts only)	Soldering bath temperature: 260°C max., time: 10 seconds max.,
Pin Partial Heating	Pin temperature: 260°C max., time: 10 seconds max.

Caution: The wave soldering must be performed at the lead part only. Note that the soldering must not be directly contacted to the board.

Notice

A model that can be soldered under the more stringent conditions (infrared reflow peak temperature: 235°C, numbver of times:2, and an extended number of days) is also available.
For details, consult NEC.

APPENDIX A. DIFFERENCES BETWEEN μPD75048 AND 75028/75008 FUNCTIONS

Item		μPD75048	μPD75028	μPD75008
ROM (bytes)		8064		
RAM (x4 bits)		512		
EEPROM (x4 bits)		1024	None	
Instruction Cycle	Main System Clock	0.95 μs, 1.91 μs, 15.3 μs (4.19 MHz)		
	Subsystem Clock	122μs (32.768 kHz)		
I/O Port	CMOS Input	48 (12 + 24 + 12)		34 (8 + 18 + 8)
	CMOS I/O	12 • Pull-up via software: 27 (except P00) 24 • Pull-down via software: 4		8 Pull-up via software 18 (except P00)
	N-ch Open-Drain I/O	12 (10 V, pull-up by mask option)		8 (10 V, pull-up by mask option)
A/D Converter		• 8-bit resolution x 8 channels • Low-voltage operation: V_{DD} = 2.7 - 6.0		None
16-bit Multifunction Timer		1 ch • 8-bit timer mode • PWM output mode • 16-bit free running timer mode • 16-bit integral A/D converter mode		None
Vector Interrupt		External: 3, Internal: 6	External: 3, Internal: 4	External: 3, Internal: 3
Test Input		External: 1, Internal: 1		
Buzzer Output (BUZ)		2 kHz, 4 kHz, 32 kHz (at 4.19 MHz, 32.768 kHz operation)		2 kHz (at 4.19 MHz, 32.768 kHz operation)
Package		• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (□ 14 mm)		• 42-pin plastic shrink DIP (600 mil) • 44-pin plastic QFP (□ 10 mm)
Supply Voltage		V_{DD} = 2.7 - 6.0 V		
Operating Temperature		-10 to +70°C	-40 to +70°C	-40 to +85°C ★
PROM Model		μPD75P048	μPD75P036	μPD75P008

APPENDIX B. DEVELOPMENT TOOLS

The following development tools are readily available to support development of systems using μPD75048:

Hardware	IE-75000-R[*1] IE-75001-R	In-circuit emulator for 75X series
	IE-75000-R-EM[*2]	Emulation board for IE-75000-R and IE-75001-R
	EP-75028CW-R	Emulation prove for μPD75048
	EP-75028GC-R EV-9200GC-64	Emulation prove for μPD75048, provided with EV-9200GC-64, 64-pin conversion socket
	PG-1500	PROM programmer
	PA-75P036GC	PROM programmer adapter solely used for μPD75P048GC. It is connected to PG-1500.
	PA-75P036CW	PROM programmer adapter solely used for μPD75P048CW. It is connected to PG-1500.
Software	IE Control Program PG-1500 Controller RA75X Relocatable Assembler	Host machine PC-9800 series (MS-DOS™ Ver. 3.30 to Ver. 5.00A[*3]) IBM PC/AT™ (PC DOS™ Ver. 3.1)

*1: Maintenance product
2: Not provided with IE-75001-R.
3: Ver. 5.00/5.00A has a task swap function, but this function cannot be used with this software.

Remarks : For development tools from other companies, refer to 75X Series Selection Guide (IF-151).

[MEMO]

GENERAL NOTES ON CMOS DEVICES

① STATIC ELECTRICITY (ALL MOS DEVICES)

Exercise care so that MOS devices are not adversely influenced by static electricity while being handled.

The insulation of the gates of the MOS device may be destroyed by a strong static charge. Therefore, when transporting or storing the MOS device, use a conductive tray, magazine case, or conductive buffer materials, or the metal case NEC uses for packaging and shipment, and use grounding when assembling the MOS device system. Do not leave the MOS device on a plastic plate and do not touch the pins of the device.

Handle boards on which MOS devices are mounted similarly .

② PROCESSING OF UNUSED PINS (CMOS DEVICES ONLY)

Fix the input level of CMOS devices.

Unlike bipolar or NMOS devices, if a CMOS device is operated with nothing connected to its input pin, intermediate level input may be generated due to noise, and an inrush current may flow through the device, causing the device to malfunction. Therefore, fix the input level of the device by using a pull-down or pull-up resistor. If there is a possibility that an unused pin serves as an output pin (whose timing is not specified), each pin should be connected to V_{DD} or GND through a resistor.

Refer to "Processing of Unused Pins" in the documents of each devices.

③ STATUS BEFORE INITIALIZATION (ALL MOS DEVICES)

The initial status of MOS devices is undefined upon power application.

Since the characteristics of an MOS device are determined by the quantity of injection at the molecular level, the initial status of the device is not controlled during the production process. The output status of pins, I/O setting, and register contents upon power application are not guaranteed. However, the items defined for reset operation and mode setting are subject to guarantee after the respective operations have been executed.

When using a device with a reset function, be sure to reset the device after power application.

[MEMO]

NEC is manufacturing and selling the products under microcomputer (with on-chip EEPROM) patent license with the BULL CP8.
This product should not be used for IC cards (SMART CARD).

M4 92.6