NEC

MOS INTEGRATED CIRCUIT

μPD72103A

HDLC CONTROLLER

DESCRIPTION

The μPD72103A HDLCC (High-Level Data Link Control Procedure Controller) is a communication control LSI which supports HDLC.

Since the HDLCC has an on-chip DMA (Direct Memory Access) function, the host system can perform serial communication by HDLC frame easily by providing commands and data on memory.

The details of functions are described in the following user's manual. Be sure to read this manual before designing.

μPD72103A User's Manual : S10766E

FEATURES

- HDLC frame control
- Address field recognition function : 1 byte/2 bytes
- Full duplex communication: × 1 channel
- Baud rate: 8 Mbps max. (2 Mbps max. when DPLL is used) Note
- Maximum transmit/receive data length : 16 Kbytes
- Level 2 header and I field or level 2 and 3 headers and user data can be separated on external memory
- Various statistical information
- DPLL (Digital Phase-Locked Loop) function
- On-chip DMA controller: 8/16 bits data, 24 bits address
- General-purpose input/output pins : Input pin × 2
  Output pin × 2
- On-chip transmission control function (LAP-D mode)
- Data format : NRZ, NRZI decode/encode
- Command chain function
- FCS (Frame Check Sequence) : 16 bits/32 bits
- System clock : 1 MHz to 16 MHz
- CMOS
- 5-V single power supply

Note Transfer rate is restricted depending on the system clock frequency and operating environment. For details, refer to **5. CAUTIONS ON OVERRUN ERRORS**.

The information in this document is subject to change without notice.

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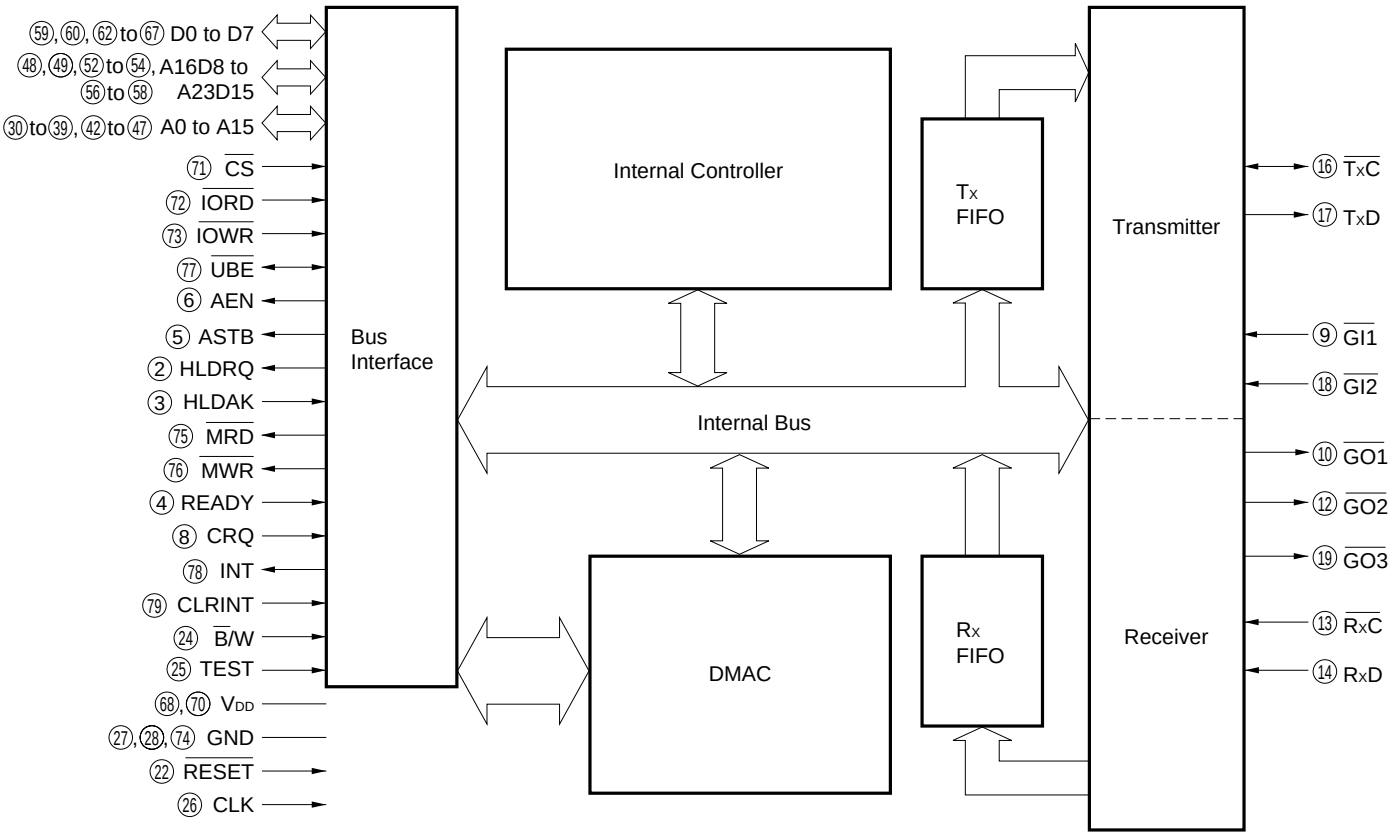
The mark ★ shows major revised points.

ORDERING INFORMATION

Part Number	Package
μPD72103AGC-3B9	80-pin plastic QFP (14 × 14 mm)
μPD72103ALP	68-pin plastic QFJ (950 × 950 mil)

BLOCK DIAGRAM

Numbers next to the pin names are the pin numbers on the μPD72103AGC-3B9 (80-pin plastic QFP).



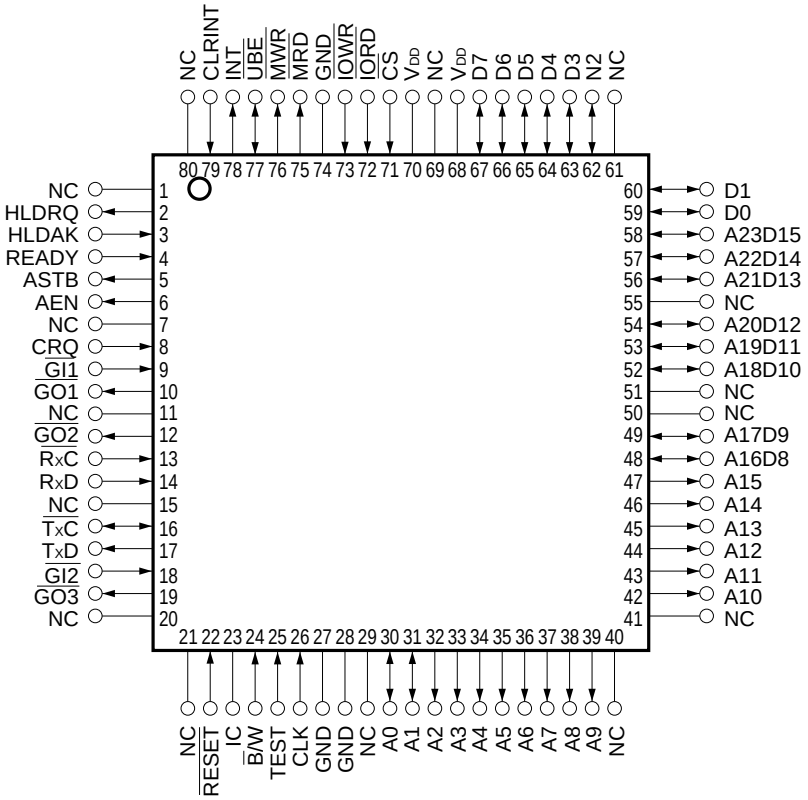
INTERNAL BLOCK FUNCTION

Name	Function
Bus interface	μPD72103A and external memory or external host processor interface.
Internal controller	Controls HDLC framing, including the DMAC, transmitter, and receiver.
DMAC (Direct Memory Access Controller)	Controls transfer of data on external memory to internal controller and transmitter or controls writing of internal controller and receiver data to external memory.
T_X FIFO	32-byte buffer used when sending transmit data from DMAC to transmitter.
R_X FIFO	128-byte buffer used when sending receive data from receiver to DMAC.
Transmitter	Converts contents of T_X FIFO to HDLC frame and transmits it as serial data.
Receiver	Receives HDLC frame and writes the data to R_X FIFO.
Internal bus	Bus which connects the internal controller, DMAC, FIFO, serial block, and bus interface. It consists of an 24-bit address bus and 8/16-bit data bus.

PIN CONFIGURATIONS (TOP VIEW)

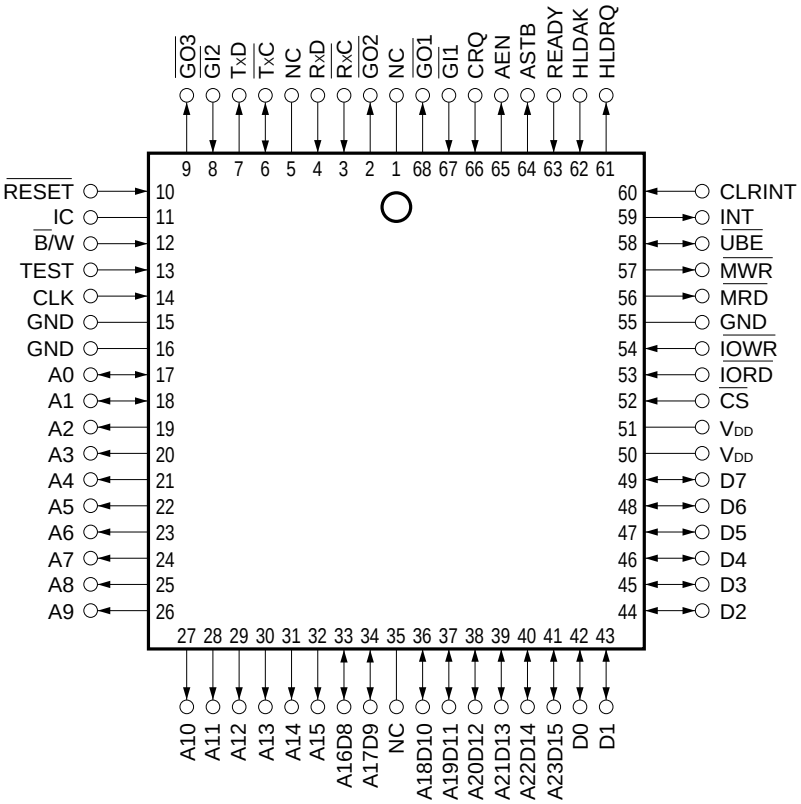
80-Pin Plastic QFP (14 × 14 mm)

μPD72103AGC-3B9



68-Pin Plastic QFJ (950 × 950 mil)

μPD72103ALP



CONTENTS

1. PINS

1.1 Pin Functions

Pin No.		Pin Name	I/O	Active Level	Function
80-Pin QFP	68-Pin QFJ				
1, 7, 11, 15, 20, 21, 29, 40, 41, 50, 51, 55, 61, 69, 80	1, 5, 35	NC (No Connection)	—	—	Leave open.
2	61	HLDRQ (Hold Request)	O	H	Hold request signal to external host processor. This signal is activated to change from bus slave to bus master when DMA operation is to be performed in μPD72103A.
3	62	HLDAK (Hold Acknowledge)	I	H	Hold acknowledge signal from external host processor. When μPD72103A detects that this signal is active, it changes from bus slave to bus master, and starts DMA operation.
4	63	READY (Ready)	I	H	Input signal used to extend $\overline{MRD}$ & $\overline{MWR}$ signal width. While READY signal is low, $\overline{MRD}$ & $\overline{MWR}$ signals maintain low level. READY signal should be changed at setup/hold times within specification.
5	64	ASTB (Address Strobe)	O	H	Used to externally latch address output from μPD72103A.
6	65	AEN (Address Enable)	O	H	When bus master, this signal enables latched upper address and outputs it to system address bus. Also used to disable other system bus drivers.
8	66	CRQ (Command Request)	I	H	Signal by which external host processor requests μPD72103A to execute command. μPD72103A fetches command in external memory on rising edge of this signal.
9	67	$\overline{GI1}$	I	—	General-purpose input pin. Issues "general-purpose input pin change detection LSW" Note 1 when change of input level is detected.
10	68	$\overline{GO1}$	O	—	General-purpose output pin. Output level is changed when "general-purpose output pin write LCW" Note 2 is executed.

Notes 1. LSW : Link Status Word

2. LCW : Link Command Word

Pin No.		Pin Name	I/O	Active Level	Function
80-Pin QFP	68-Pin QFJ				
12	2	$\overline{GO2}$	O	—	General-purpose output pin. Output level is changed when "general-purpose output pin write LCW" is executed.
13	3	$\overline{RxC}$ (Receive Clock)	I	—	In on-chip DPLL mode: μPD72103A on-chip DPLL transmit/receive clock input.
					In external DPLL mode: Receive clock input.
14	4	RxD (Receive Data)	I	—	Serial receive data input.
16	6	$\overline{TxC}$ (Transmit Clock)	I/O	—	In on-chip DPLL mode: Outputs clock obtained by division-by-16 of $\overline{RxC}$ pin input signal created in μPD72103A.
					In external DPLL mode: Inputs transmit clock from off-chip.
17	7	TxD (Transmit Data)	O	—	Serial transmit data output.
18	8	$\overline{GI2}$	I	L	In LAP-D mode: Enable signal for frame transmission from outside.
					When not in LAP-D mode: General-purpose input. When a change in the input level is detected, a "general-purpose input change detection LSW" is reported.
19	9	$\overline{GO3}$	O	L	In LAP-D mode: Request signal for frame transmission to outside.
					When not in LAP-D mode: This pin does not function. Leave open.
22	10	$\overline{RESET}$ (Reset)	I	L	Performs internal initialization of μPD72103A. 7 or more CLK clock cycles are required. After reset, bus slave mode is set.
23	11	IC (Internally Connected)	—	—	No connection should be made to this pin.
24	12	$\overline{B}$/W (Byte/Word)	I	L/H	Specifies data bus for access to external memory. $\overline{B}$/W = 0 : byte unit (8 bits) $\overline{B}$/W = 1 : word unit (16 bits) After powering on, $\overline{B}$/W pin status should be fixed. In a word access, lower half of data bus comprises even address data contents.
25	13	TEST (Test)	I	—	Should be pulled high during operation.

Pin No.		Pin Name	I/O	Active Level	Function	
80-Pin QFP	68-Pin QFJ					
26	14	CLK (Clock)	I	—	System clock input 1 MHz to 16 MHz clock should be input.	
27, 28, 74	15, 16, 55	GND	—	—	Ground pin.	
30, 31	17, 18	A0, A1	I/O 3-state	—	Bidirectional 3-state address lines	When bus master : (output) Output low-order 2 bits of memory access address.
						When bus slave : (input) Input address when external host processor accesses μPD72103A internal register.
32 to 39, 42 to 47	19 to 32	A2 to A15	O 3-state	—	When bus master : Output bits 2 to 15 of memory address.	
					When bus slave : High impedance.	
48, 49, 52 to 54, 56 to 58	33, 34 36 to 41	A16D8 to A23D15	I/O 3-state	—	Bidirectional 3-state address/data bus. Multiplex pins for 16 to 23 bits of high-order of address and 8 to15 bits of high-order of data.	
59, 60 62 to 67	42 to 49	D0 to D7	I/O 3-state	—	Bidirectional 3-state data bus	When bus master : Output when write to external memory performed. Input when read is performed.
						When bus slave : Usually high impedance. Output internal register data when external host processor reads μPD72103A internal data.
68, 70	50, 51	V_{DD}	—	—	+5 power supply.	
71	52	$\overline{CS}$ (Chip Select)	I	L	When bus master: Set to disabled state. When bus slave: When low-level, read/write operation from host processor is possible.	
72	53	$\overline{IORD}$ (I/O Read)	I	L	Used to enable external host processor to read contents of μPD72103A internal register. When bus master : Set to disabled state.	
73	54	$\overline{IOWR}$ (I/O Write)	I	L	Used to enable external host processor to write data to μPD72103A internal register. When bus master : Set to disabled state.	

<table>
<tr><th colspan="2">Pin No.</th><th rowspan="2">Pin Name</th><th rowspan="2">I/O</th><th rowspan="2">Active Level</th><th rowspan="2">Function</th></tr>
<tr><th>80-Pin QFP</th><th>68-Pin QFJ</th></tr>
<tr><td>75</td><td>56</td><td>$\overline{\text{MRD}}$
(Memory Read)</td><td>O
3-state</td><td>L</td><td>When bus master:
When low-level, external memory data is read.

When bus slave:
High impedance.</td></tr>
<tr><td>76</td><td>57</td><td>$\overline{\text{MWR}}$
(Memory Write)</td><td>O
3-state</td><td>L</td><td>When bus master:
When low-level, data is written to external memory.

When bus slave:
High impedance</td></tr>
<tr><td>77</td><td>58</td><td>$\overline{\text{UBE}}$
(Upper Byte Enable)</td><td>I/O
3-state</td><td>L/H</td><td>When bus master:
Signal output from this pin depends on $\overline{\text{B}}$/W pin input value.
• Byte transfer mode ($\overline{\text{B}}$/W = 0)
$\overline{\text{UBE}}$ is always high impedance.
• Word transfer mode ($\overline{\text{B}}$/W = 1)
Indicates whether valid data is on pins D0 to D7 or pins A16D8 to A23D15 (or both).
<table>
<tr><th>$\overline{\text{UBE}}$</th><th>A0</th><th>D0 to D7</th><th>A16D8 to A23D15</th></tr>
<tr><td>0</td><td>0</td><td>√</td><td>√</td></tr>
<tr><td>0</td><td>1</td><td>–</td><td>√</td></tr>
<tr><td>1</td><td>0</td><td>√</td><td>–</td></tr>
<tr><td>1</td><td>1</td><td>–</td><td>–</td></tr>
</table>
When bus slave:
$\overline{\text{UBE}}$ is input, and indicates whether valid data is on pins D0 to D7 or pins A16D8 to A23D15.
<table>
<tr><th>$\overline{\text{UBE}}$</th><th>A0</th><th>D0 to D7</th><th>A16D8 to A23D15</th></tr>
<tr><td>0</td><td>0</td><td>√</td><td>–</td></tr>
<tr><td>0</td><td>1</td><td>–</td><td>√</td></tr>
<tr><td>1</td><td>0</td><td>√</td><td>–</td></tr>
<tr><td>1</td><td>1</td><td>√</td><td>–</td></tr>
</table></td></tr>
<tr><td>78</td><td>59</td><td>INT
(Interrupt)</td><td>O</td><td>H</td><td>Interrupt signal from μPD72103A to external host processor.</td></tr>
<tr><td>79</td><td>60</td><td>CLRINT
(Clear interrupt)</td><td>I</td><td>H</td><td>Signal which deactivates INT signal output by μPD72103A.
μPD72103A drives INT signal low on rising edge of this signal.</td></tr>
</table>

1.2 Pin Status after Reset

When a μPD72103A reset is performed, the output pin and input/output pin statuses are as shown below. As the reset signal is latched by the CLK signal, 4 CLK clocks are required until the status shown under "During Reset" in the table below is attained.

Pin No.		Pin Name	I/O	During Reset (This state continues after reset)
80-Pin QFP	68-Pin QFJ			
12	2	$\overline{GO2}$	O	H
16	6	$\overline{TxC}$	I/O	Hi-Z
17	7	$\overline{TxD}$	O	H
19	9	GO3	O	H
30, 31	17, 18	A0, A1	I/O 3-state	Hi-Z
32 to 39 42 to 47	19 to 26, 27 to 32	A2 to A15	O 3-state	Hi-Z
48, 49, 52 to 54, 56 to 58	33, 34, 36 to 41	A16/D8 to A23/D15	I/O 3-state	Hi-Z
59, 60, 62 to 67	42 to 49	D0 to D7	I/O 3-state	Hi-Z
75	56	$\overline{MRD}$	O 3-state	Hi-Z
76	57	$\overline{MWR}$	O 3-state	Hi-Z
77	58	$\overline{UBE}$	I/O 3-state	Hi-Z
78	59	INT	O	L
2	61	HLDRQ	O	L
5	64	ASTB	O	L
6	65	AEN	O	L
10	68	$\overline{GO1}$	O	H

2. INTERNAL REGISTERS

The μPD72103A has 4 internal registers. These registers are controlled by 6 pins: $\overline{IORD}$, $\overline{IOWR}$, A1, A0, $\overline{UBE}$ and $\overline{CS}$. The host processor can only access μPD72103A internal registers when it is the bus slave.

Table 2-1 shows the internal register map (for $\overline{UBE}$, see the $\overline{UBE}$ entry in "Pin Functions").

Table 2-1. I/O Port Map

$\overline{CS}$	$\overline{IORD}$	$\overline{IOWR}$	A1	A0	Internal Register	Function
1	×	×	×	×	——	Does not function
0	1	0	0	0	Control register	Write
0	0	1	0	0	Internal status register	Read
0	1	0	0	1	Internal FIFO active register	When 5 is written to this register, MSET command[Note] can be written to internal FIFO.
0	1	0	1	0	——	Setting prohibited
0	1	0	1	1	Internal FIFO register	Writes MSET command to internal FIFO.
0	0	1	1	1	——	Setting prohibited

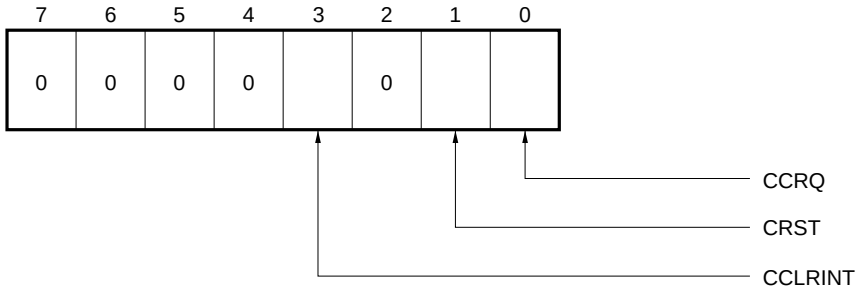
× : don't care

Note The MSET command is a memory area setting command. It determines the host interface (memory space used) between the host processor and the μPD72103A. For details, see **the User's Manual** (**S10766E**).

2.1 Control Register

The control register is used when the host processor accesses the μPD72103A.

Figure 2-1. Control Register



Caution 0 must be written to bit 2, 4, 5, 6 and 7.

Table 2-2. Control Register

Bit Name	Name	Function
CCRQ	Control Command Request	When 1 is written to this bit, a command is executed. This operation is the same as command execution by means of the CRQ pin. It does not matter to the host processor which is selected. This bit is automatically cleared to 0 internally, and therefore the host processor does not have to write 0 to this bit after writing 1 to it.
CRST	Control Reset	When 1 is written to this bit, an internal reset of the μPD72103A is performed automatically. This reset is the same as a reset performed by means of the $\overline{\text{RESET}}$ pin. This bit is automatically cleared to 0 internally, and therefore the host processor does not have to write 0 to this bit after writing 1 to it.
CCLRINT	Control Clear INT	When 1 is written to this bit, the INT pin is reset automatically. This function is the same as resetting the INT pin by means of the CLRINT pin. It does not matter to the host processor which is selected. This bit is automatically cleared to 0 internally, and therefore the host processor does not have to write 0 to this bit after writing 1 to it.

2.2 Internal Status Register

The internal status register is used to indicate the internal status of the μPD72103A.

Figure 2-2. Internal Status Register

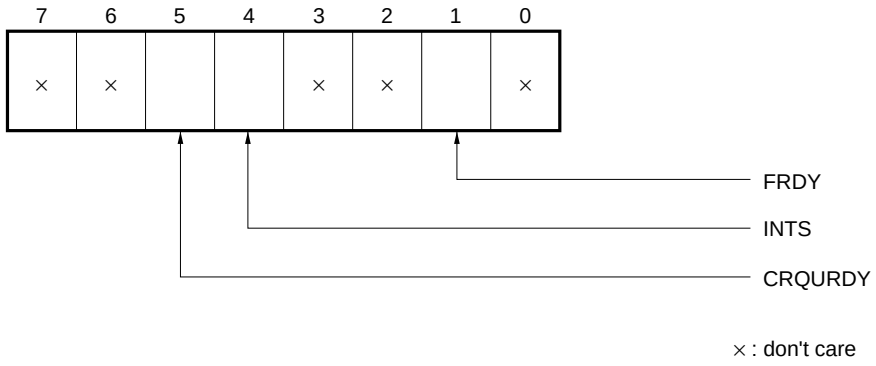


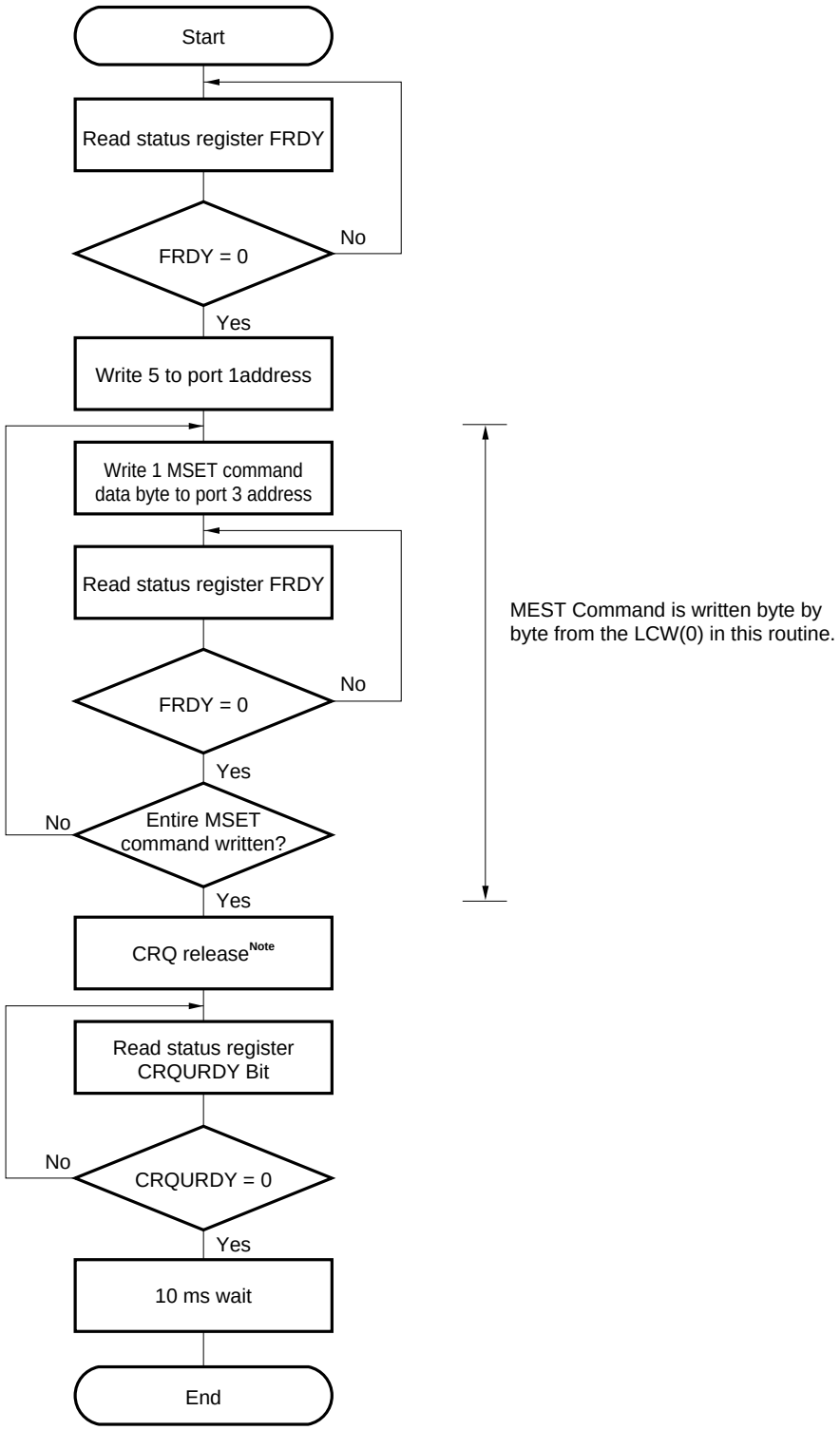
Table 2-3. Internal Status Register

Bit Name	Name	Function
FRDY	FIFO Ready	When the MSET command is written to the internal FIFO, this bit is referenced. If this bit is 0 the write can be performed. If this bit is 1 it is necessary to wait until it becomes 0 before writing to the FIFO. This bit is 0 immediately after RESET.
INTS	INT Status	The same signal as the INT pin. The host processor can ascertain the status report timing from the μPD72103A by polling this bit as well as by means of an interrupt via the INT pin. This bit is 0 immediately after RESET.
CRQURDY	Command Request Unready	After an MSET command is issued, this bit is set to 0 and the next command should be issued after the elapse of 10 ms (in case of 8 MHz system clock). This bit is 0 immediately after RESET.

2.3 Writing MSET Command to Internal FIFO

Only an MSET command can be written to the internal FIFO in the μPD72103A immediately after a reset. This command should be written the following procedure in the flowchart below.

Figure 2-3. Flowchart for Writing MSET Command to Internal FIFO



★ **Note** Pulse input to CRQ pin, or set 1 to CCRQ bit in command reigster

3. DMAC (DIRECT MEMORY ACCESS CONTROLLER) FUNCTIONS

When the μPD72103A is the bus master, it can perform reading of commands and transmit data in external memory and writing of the internal status and receive data to external memory by means of the on-chip DMAC.

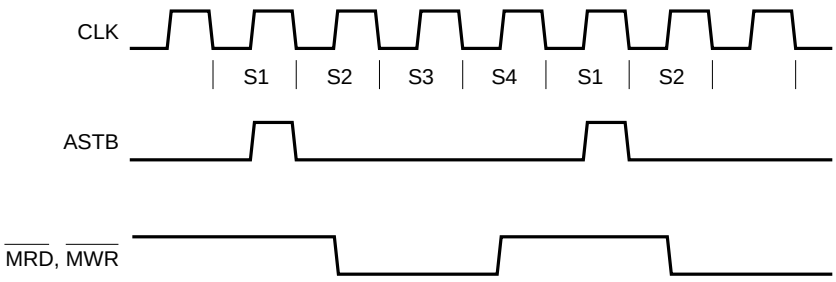
The DMA address is 24 bits in length, and data is selected by means of the $\overline{B}$/W pin so that either 8-bit or 16-bit memory can be handled.

3.1 Block Transfers

For the transfer of long data, the μPD72103A uses DMA with the data divided into 4-byte blocks. The HLDRQ pin is activated (driven high) once for a one block DMA. The basic DMA bus cycle is 4 clock cycles. One byte (8 bits) or 2 bytes (16 bits) can be transferred in one such bus cycle. When 4 bytes are transferred as a block, 4 bus cycles are needed in byte transfer mode. In word transfer mode, the number of cycles depends on the address. In the case of 4 bytes from an odd address, 3 bus cycles are required, while only 2 bus cycles are required from an even address.

The basic clock of one bus cycle is shown in **Figure 3-1**.

Figure 3-1. Basic Clock of One Bus Cycle in Block Transfer

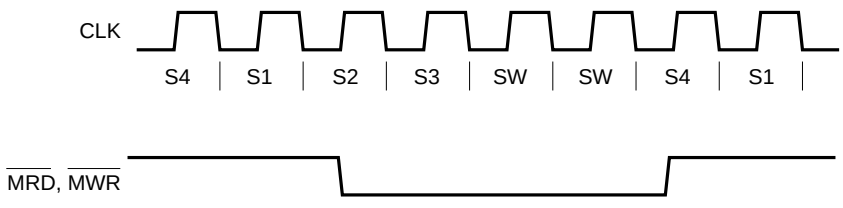


3.2 Programmable Wait

In a μPD72103A DMA, there are basically 4 clock cycles in one bus cycle, and in this case $\overline{MRD}$ and $\overline{MWR}$ are 2 clock cycles in width. There are two methods for memory for which this 2 clock cycle width is insufficient. The first is a programmable wait function whereby the μPD72103A increases the active width by automatically inserting wait cycles in $\overline{MRD}$ and $\overline{MWR}$ internally. The programmable wait value can be set by means of "operating mode setting LCW" DMAW. **Figure 3-2** shows an example in which programmable waits = 2.

The other method is to extend the width of $\overline{MRD}$ and $\overline{MWR}$ by driving the READY signal low. This method is effective for setting a longer wait than the set value of DMAW.

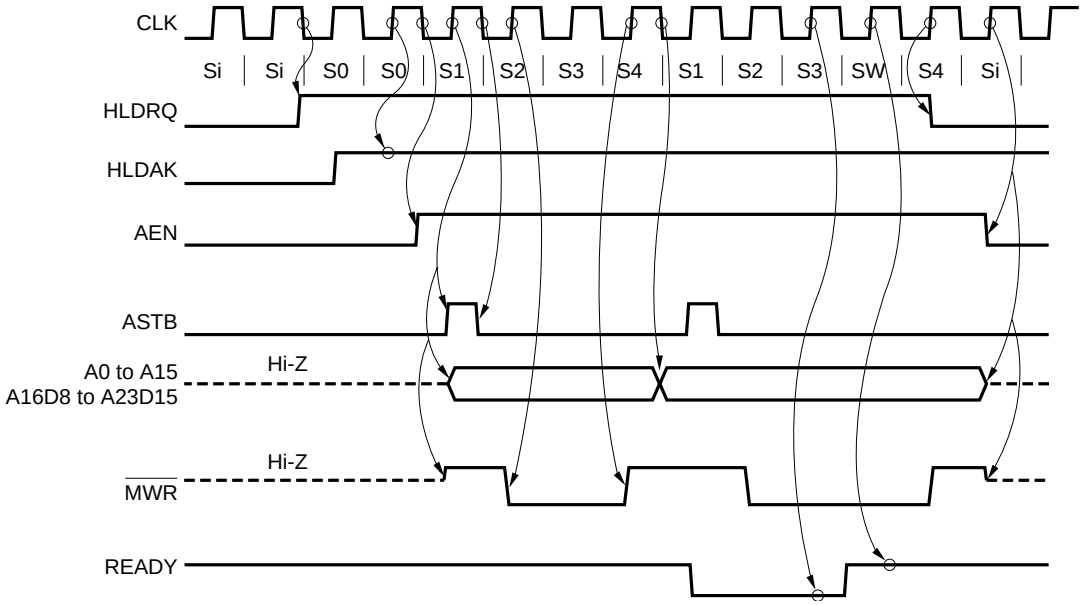
Figure 3-2. Example with Programmable Waits = 2



3.3 Basic DMA Timing

Figure 3-3. Memory Write Timing

(1) When $\overline{B}$/W is 0



(2) When $\overline{B}$/W is 1

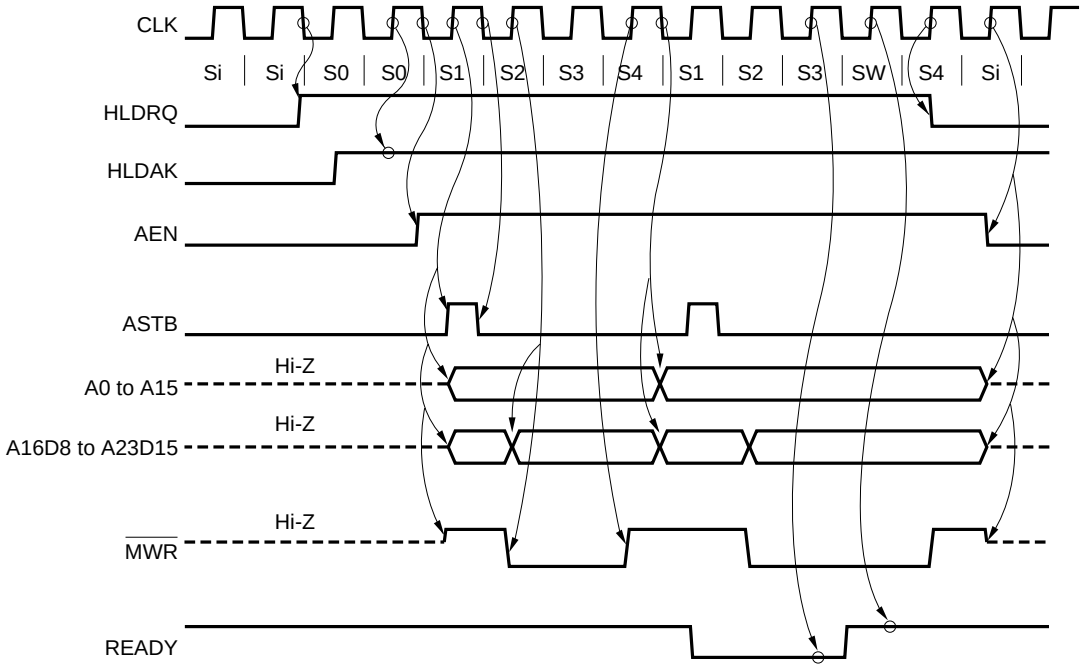
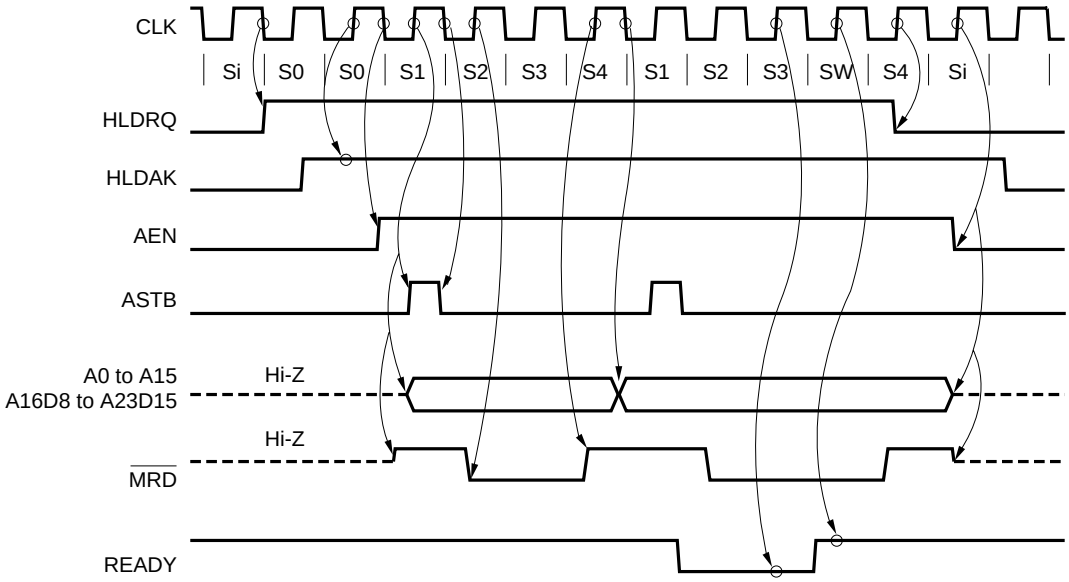
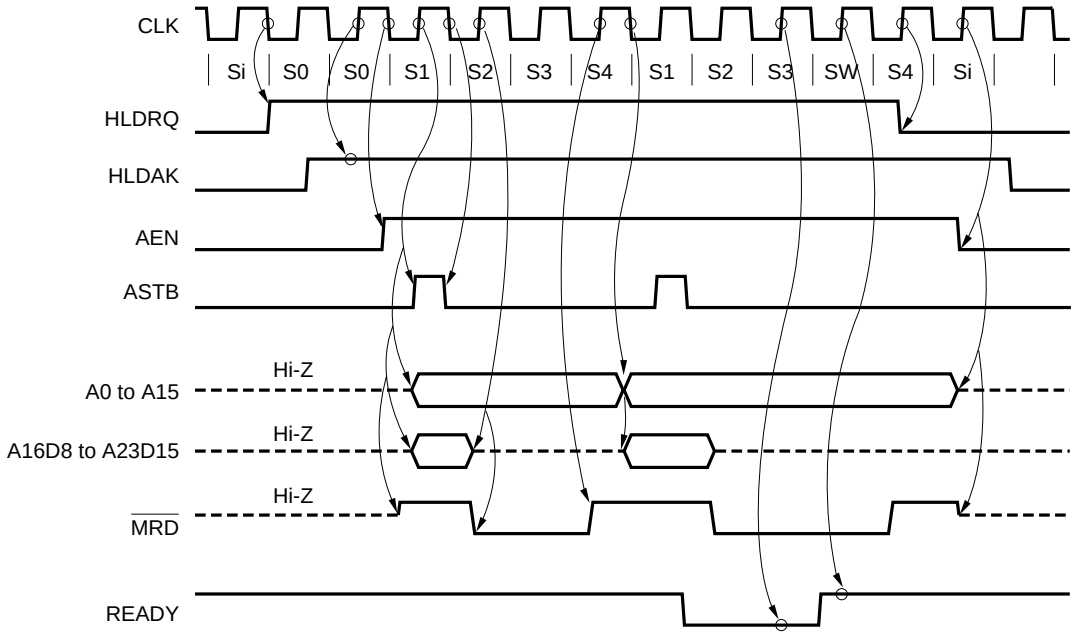


Figure 3-4. Memory Read Timing

(1) When $\overline{B}$/W is 0



(2) When $\overline{B}$/W is 1



3.4 Address/Data Multiplexing

The 24 address pins and 16 data pins are multiplexed as shown below.

Pins	Address	Data
A0 to A15	0 to 15	
A16D8 to A23D15	16 to 23	8 to 15
D0 to D7		0 to 7

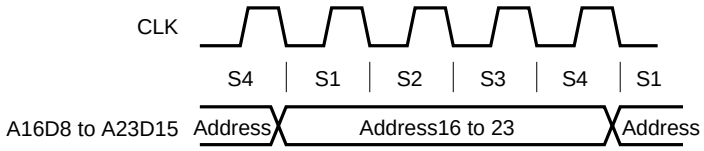
The purpose of this multiplexing is to reduce external address latching.

When external memory is configured in byte mode ($\overline{B}$/W = 0), external address latching is not necessary. When memory is configured in word mode ($\overline{B}$/W = 1), external address latching is not necessary if the memory capacity is 64K bytes or less (the number of address pins needed is 16 or fewer). If the memory is larger than 64K bytes, an external address latch is required for pins A16D8 to A23D15.

To make this kind of external circuit possible, the operation of pins A16D8 to A23D15 on which addresses and data are multiplexed depends on the input value of the $\overline{B}$/W pin.

Figure 3-5. Byte Mode ($\overline{B}$/W = 0)

(1) Memory Read



(2) Memory Write

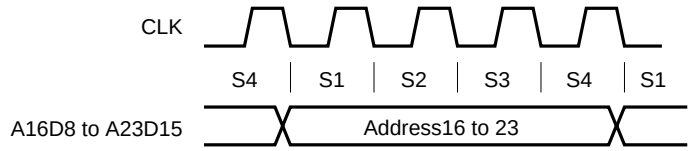
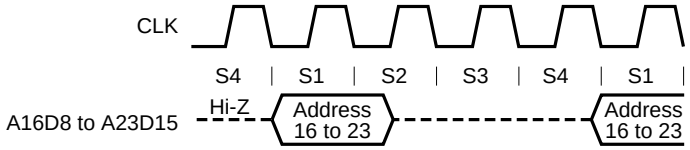
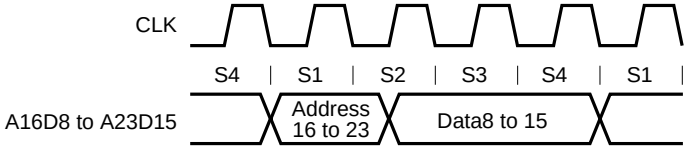


Figure 3-6. Word Mode ($\overline{B}$/W = 1)

(1) Memory Read



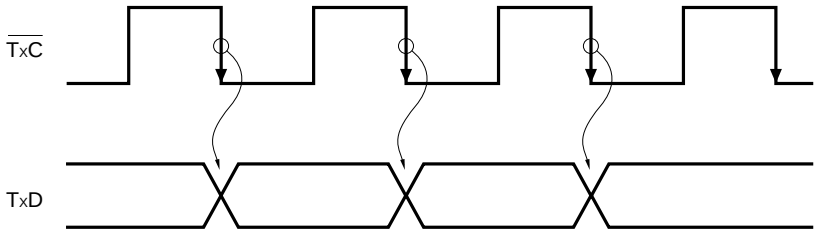
(2) Memory Write



4. SERIAL TIMINGS

4.1 Transmission Timing

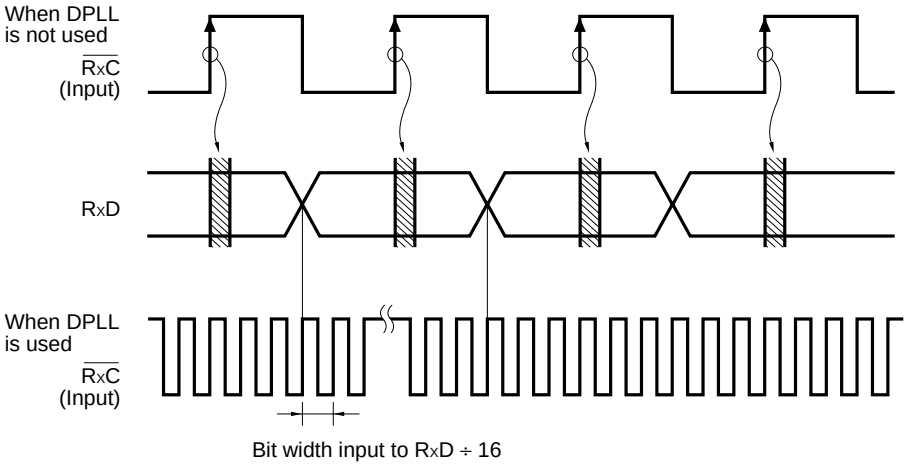
Transmit data from the TxD pin is output as one bit from the fall of $\overline{\text{TxC}}$ to the next fall of $\overline{\text{TxC}}$.



Remark The $\overline{\text{TxC}}$ pin is an output pin when DPLL is used, and an input pin when DPLL is not used.

4.2 Reception Timing

Receive data from the RxD pin is sampled on the rise of $\overline{\text{RxC}}$.



4.3 Transmission Control Function (LAP-D MODE)

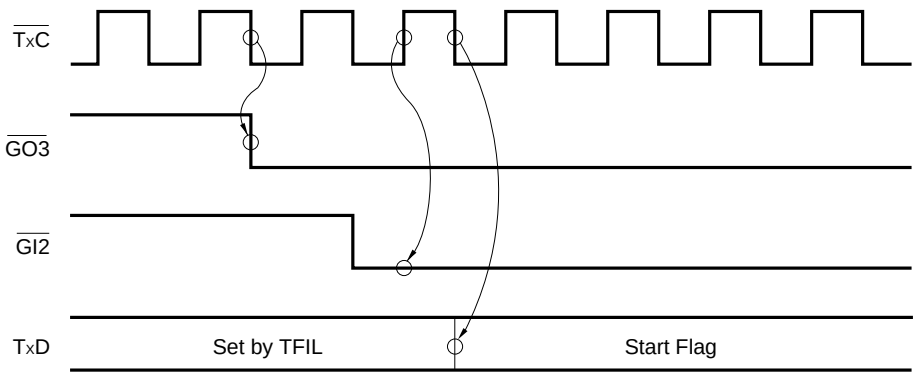
When the LAP-D mode is selected, the $\overline{\text{GO3}}$ pin is used for the frame transmission request signal and the $\overline{\text{GI2}}$ pin is used for the frame transmission enable signal. The operation of the $\overline{\text{GI2}}$ and $\overline{\text{GO3}}$ pins in the LAP-D mode is shown below.

$\overline{\text{GO3}}$ pin	When a transmit command is fetched and transmit data is written into the TxFIFO, the μPD72103A drives this pin low and issues a transmission request to the external circuitry. When the $\overline{\text{GI2}}$ pin is driven low by the external circuitry, the μPD72103A starts frame transmission, and drives this pin high after the end flag is transmitted.
$\overline{\text{GI2}}$ pin	When the $\overline{\text{GO3}}$ pin is driven low, the μPD72103A samples this pin, and if it is low, starts frame transmission. When this pin is driven high by the external circuitry during frame transmission, the μPD72103A suspends frame transmission and sets the TxD pin to the status set by TFIL.

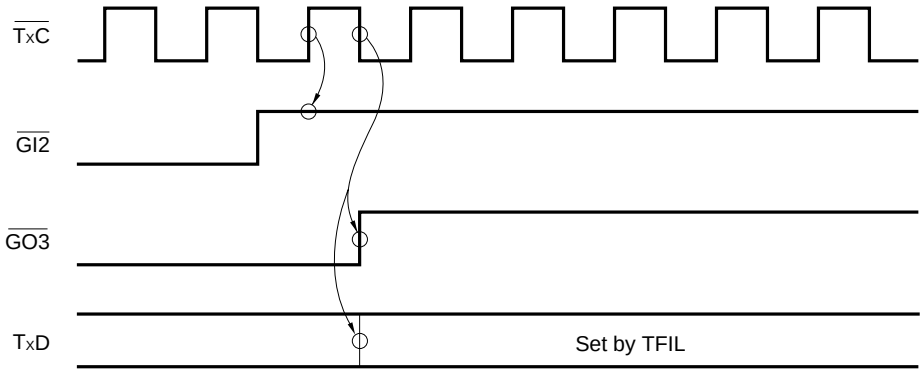
The operation timing of the $\overline{\text{GI2}}$ and $\overline{\text{GO3}}$ pins is shown in **Figure 4-1**.

Figure 4-1. Pin $\overline{GI2}$/$\overline{GO3}$ Operation Timing (in DPLL Mode)

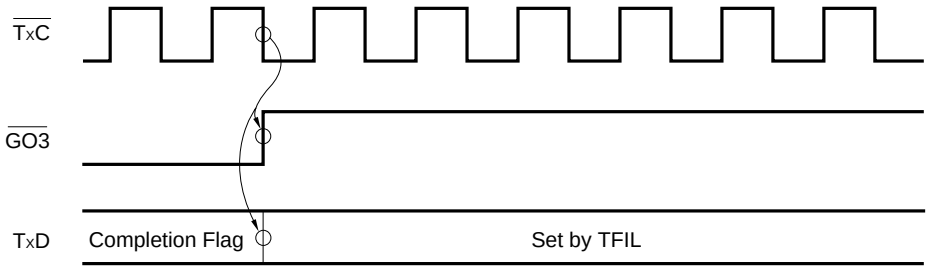
(a) Frame transmission operation



(b) Frame transmission abort operation



(c) Frame transmission completion operation



5. CAUTIONS ON OVERRUN ERRORS

When μPD72103A reception processing is performed, time is taken in performing receive DMA processing for the reasons given below, and during this period there may be an overrun of received frames, with frames being discarded internally.

The main causes of overrun are described below.

[Causes]

a. Address search processing

If AUTO ≠ 00H is set and address identification is performed, there is a long interval between frame reception and receive DMA initiation, and an overrun error may occur. With receive DMA, the address table set by AFST and the receive address field are compared sequentially, and the receive DMA is initiated after they match. Therefore, the nearer the matching address is to the end of the address table, the greater the probability of an overrun error occurring.

b. Status report processing

While a status report is being executed, DMA transfer initiation processing for the received data (receive buffer address setting for the internal DMAC and receive DMA channel initiation) is disabled. Consequently, if the status report execution timing and frame reception initiation timing coincide, the receive DMA does not start until the status report processing ends. As a result, data accumulates in the receive FIFO, and in some cases 128 bytes of data or more may be received, causing an overrun.

c. Reception end interrupt servicing

During frame reception end processing, the reception interrupt generated by the next frame is masked, and therefore data received during this time is accumulated in the receive FIFO, and eventually causes an overrun.

d. Receive buffer chain processing

If the receive buffer is small, the high the transfer speed compared with the time taken to initiate a receive buffer DMA, the greater the amount of data that will be left in the receive FIFO, eventually resulting in an overrun error. Especially in a short frame reception, the reception start processing of packets is immediately followed by the reception complete processing. Thus, the processing time takes longer than the normal frame reception and the next frame to be received has highly possibility for overrun errors.

The following measures should be taken to prevent overrun errors.

[Preventive measures]

- Reduce the transfer rate
- Perform retransmission processing by means of the higher-layer software
- Increase the system clock rate (MAX. 16 MHz)
- Increase the reception interval
- When using the receive buffer chain, increase the receive buffer size as large as possible.

(1) and **(2)** show data relating to overrun error causes.

The receive DMA processing disabled time for each cause depends on the set parameters, etc.

(1) Receive DMA processing disabled time for each setting with causes a, b and c

Cause	Condition	Set Value & Receive DMA Processing Item	Disabled Time [μs]
a	1	AUTO = 00H, STBC = 0	Approx. 16
	2	AUTO = 00H, STBC = 4	Approx. 27
	3	AUTO = 00H, STBC = 8	Approx. 38
	4	AUTO = 01H, STBC = 4, BC = 3 of AFST	Approx. 27
	5	AUTO = 01H, STBC = 4, BC = 12 of AFST	Approx. 40
	6	AUTO = 01H, STBC = 8, BC = 3 of AFST	Approx. 39
	7	AUTO = 01H, STBC = 8, BC = 12 of AFST	Approx. 52
b	1	When there is no status report	Approx. 17
	2	When there is an SIAK status report	Approx. 70
	3	When there is an SIAF status report	Approx. 31
c	1	When STBC = 0 and there is no receive buffer chain	Approx. 65
	2	When STBC = 4 and there is no receive buffer chain	Approx. 70
	3	When STBC = 8 and there is no receive buffer chain	Approx. 81
	4	When there is a receive buffer chain in conditions c1 to c3 (number of receive buffers used = N)	(Condition c1 to c3) + approx. 13 μs × N

Remarks 1. As regards the MDAK and GPAE statuses, the time is virtually the same as for condition b1.

2. The above data assumes the use of 16 MHz system clock.

3. Transmit operations are not affected.

(2) Upper limit of transfer rate at which overrun error does not occur in case of multiplicity of causes a, b and c

Cause			Upper limit of transfer rate at which overrun error is not caused [Mbps]
a	b	c	
1	1	1	8.0
	2		6.8
	3		8.0
2	1	2	8.0
	2		6.1
	3		7.9
4	1		8.0
	2		6.1
	3		7.9
5	1		8.0
	2		5.6
	3		7.2
3	1	3	7.5
	2		5.4
	3		6.8
6	1		7.4
	2		5.4
	3		6.7
7	1		6.8
	2		5.0
	3		6.2

Remark The above data assumes the use of 16 MHz system clock and HLDRQ response time of 1 μs.

6. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Test Conditions	Rating	Unit
Power supply voltage	V_{DD}		–0.5 to +7.0	V
Input voltage	V_I		–0.5 to V_{DD} + 0.3	V
Output voltage	V_O		–0.5 to V_{DD} + 0.3	V
Ambient frequency temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–40 to +125	°C

Caution If any of the above parameters exceeds the absolute maximum ratings, even momentarily, device reliability may be imposed. The absolute maximum ratings are values that may physically damage the product. Be sure to use the product within the ratings.

DC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 5 V ±10%)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage low	V_{ILC}	CLK pin	–0.5		+0.8	V
	V_{ILR}	$\overline{R_XC}$ pin (in DPLL Mode)	–0.5		+0.4	V
	V_{IL}	Other pins	–0.5		+0.8	V
Input voltage high	V_{IHC}	CLK, TEST pins	+3.3		V_{DD} + 0.3	V
	V_{IHR}	$\overline{R_XC}$ pin (in DPLL Mode)	+3.3		V_{DD} + 0.3	V
	V_{IH}	Other pins	+2.2		V_{DD} + 0.3	V
Output voltage low	V_{OL}	I_{OL} = 2.5 mA			+0.4	V
Output voltage high	V_{OH}	I_{OH} = –400 μA	0.7 × V_{DD}			V
Supply current	I_{DD}	Operating		25	50	mA
Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ V_{DD}			±10	μA
Output leakage current	I_{LO}	0 V ≤ V_{OUT} ≤ V_{DD}			±10	μA

CAPACITANCE (T_A = +25°C, V_{DD} = 0 V)

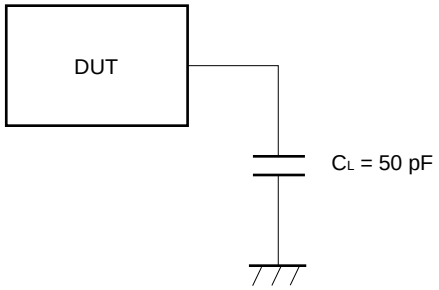
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz	—	8	15	pF
Output capacitance	C_O		—	8	15	pF
Input/output capacitance	C_{IO}		—	8	20	pF

AC CHARACTERISTICS (T_A = –40 to +85°C, V_{DD} = 5 V ±10%)

Bus Master (1)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Clock cycle time	t_{CYK}		62	1000	ns
Clock low-level time	t_{KKL}		25		ns
Clock high-level time	t_{KKH}		25		ns
Clock rise time	t_{KR}	1.5 to 3.0 V		6	ns
Clock fall time	t_{KF}	3.0 to 1.5 V		6	ns

Load Condition

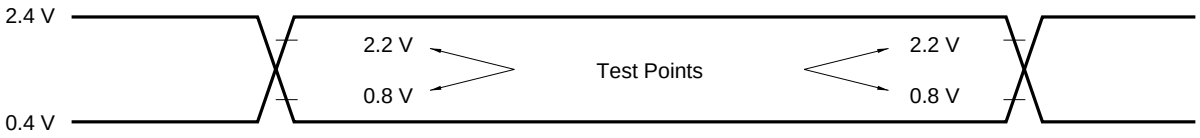


C_L includes the jig capacity.

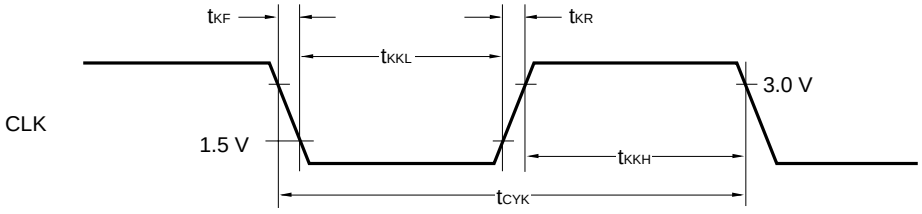
Caution When the load capacity exceeds 50 pF due to the unit configuration, set the load capacity of this device to less than 50 pF by placing a buffer, etc.

Remark DUT: non-test device

AC Test Input/Output Waveforms (Excluding Clock)

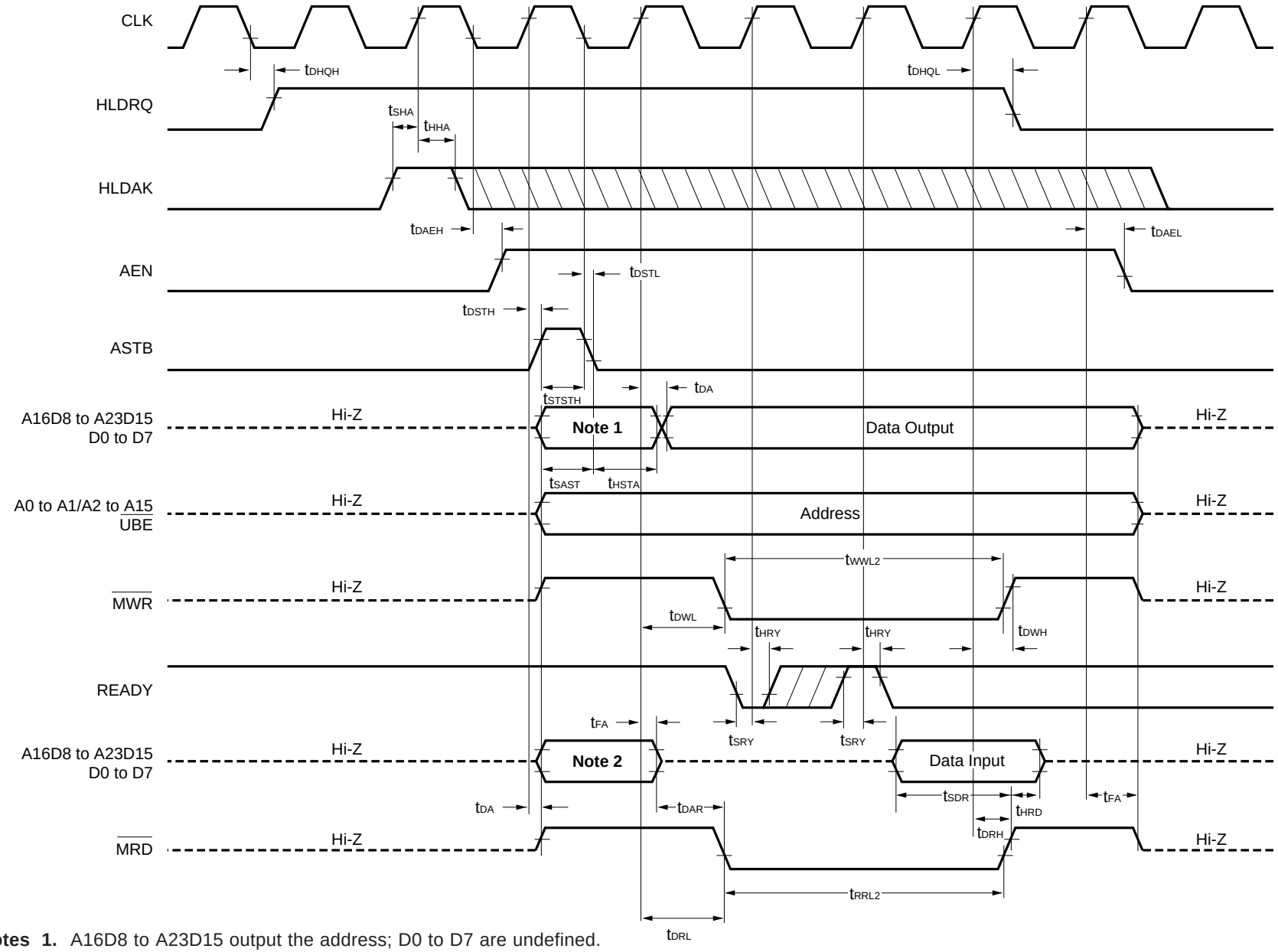


System Clock



Bus Master (2)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
HLDRQ high delay time (from CLK low)	t_{DHQH}			50	ns
HLDRQ low delay time (from CLK high)	t_{DHQL}			50	ns
HLDAK setup time (to CLK high)	t_{SHA}		20		ns
HLDAK hold time (from CLK high)	t_{HHA}		10		ns
AEN high delay time (from CLK low)	t_{DAEH}			50	ns
AEN low delay time (from CLK high)	t_{DAEL}			50	ns
ASTB high delay time (from CLK high)	t_{DSTH}			35	ns
ASTB high level width	t_{STSTH}		t_{KKH}–10		ns
ASTB low delay time (from CLK low)	t_{DSTL}			50	ns
ADR/$\overline{UBE}$/$\overline{MRD}$/$\overline{MWR}$ delay time (from CLK high)	t_{DA}			50	ns
ADR/$\overline{UBE}$/$\overline{MRD}$/$\overline{MWR}$ float time (from CLK high)	t_{FA}			35	ns
ADR setup time (to ASTB low)	t_{SAST}		t_{KKH}–17		ns
ADR hold time (from ASTB low)	t_{HSTA}		t_{KKL}–17		ns
$\overline{MRD}$ low delay time (from ADR float)	t_{DAR}		0		ns
$\overline{MRD}$ low delay time (from CLK high)	t_{DRL}			35	ns
$\overline{MRD}$ low level width	t_{RRL2}		$2t_{CYK}$–25		ns
$\overline{MRD}$ high delay time (from CLK high)	t_{DRH}			35	ns
DATA setup time (to $\overline{MRD}$ high)	t_{SDR}		50		ns
DATA hold time (from $\overline{MRD}$ high)	t_{HRD}		0		ns
$\overline{MWR}$ low delay time (from CLK high)	t_{DWL}			35	ns
$\overline{MWR}$ low level width	t_{WWL2}		$2t_{CYK}$–25		ns
$\overline{MWR}$ high delay time (from CLK high)	t_{DWH}			35	ns
READY setup time (to CLK high)	t_{SRY}		20		ns
READY hold time (from CLK high)	t_{HRY}		10		ns



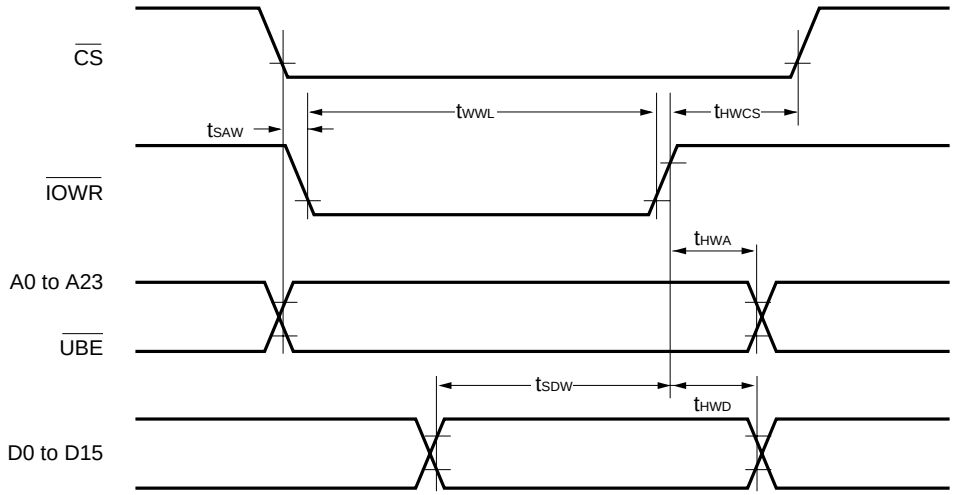
Notes 1. A16D8 to A23D15 output the address; D0 to D7 are undefined.

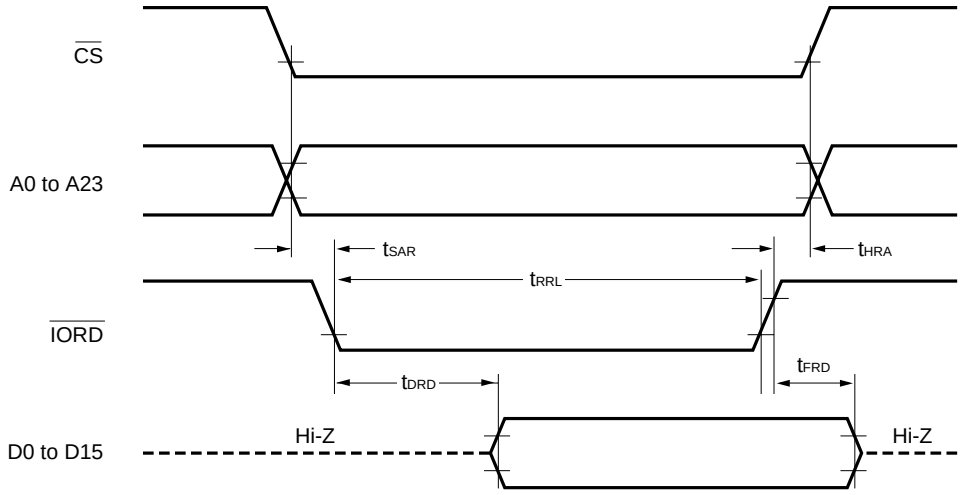
2. A16D8 to A23D15 output the address; D0 to D7 are Hi-Z.

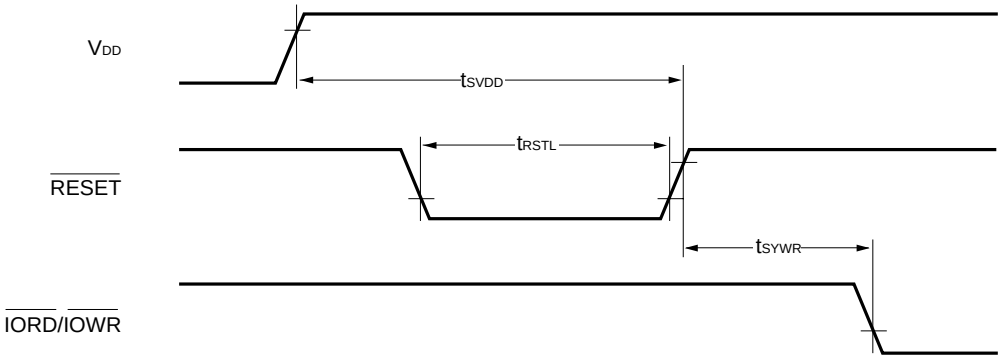
Bus Slave (1)

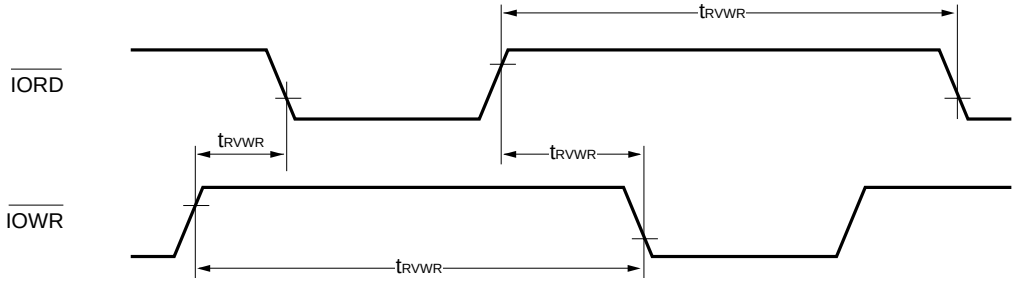
Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{IOWR}$ low level width	t_{WWL}		50		ns
$\overline{CS}$ low hold time (from $\overline{IOWR}$ high)	t_{HWCS}		0		ns
ADR/$\overline{UBE}$/$\overline{CS}$ low setup time (to $\overline{IOWR}$ low)	t_{SAW}		0		ns
ADR/$\overline{UBE}$ hold time (from $\overline{IOWR}$ high)	t_{HWA}		0		ns
DATA setup time (to $\overline{IOWR}$ high)	t_{SDW}		50		ns
DATA hold time (from $\overline{IOWR}$ high)	t_{HWD}		0		ns
$\overline{IORD}$ low level width	t_{RRL}		75		ns
ADR/$\overline{CS}$ low setup time (to $\overline{IORD}$ low)	t_{SAR}		20		ns
ADR/$\overline{CS}$ low hold time (from $\overline{IORD}$ high)	t_{HRA}		0		ns
DATA delay time (from $\overline{IORD}$ low)	t_{DRD}			60	ns
DATA float time (from $\overline{IORD}$ high)	t_{FRD}		10	50	ns
$\overline{RESET}$ low level width	t_{RSTL}		$7t_{CYK}$		ns
V_{DD} setup time (to $\overline{RESET}$ high)	t_{SVDD}		1000		ns
$\overline{RESET}$ high - 1st $\overline{IOWR}$/$\overline{IORD}$	t_{SYWR}		$2t_{CYK}$		ns
$\overline{IOWR}$/$\overline{IORD}$ recovery time	t_{RVWR}		100		ns

Bus Slave


CS
tSAW
tWWL
tHWCS
IOWR
tHWA
A0 to A23
UBE
tSDW
tHWD
D0 to D15

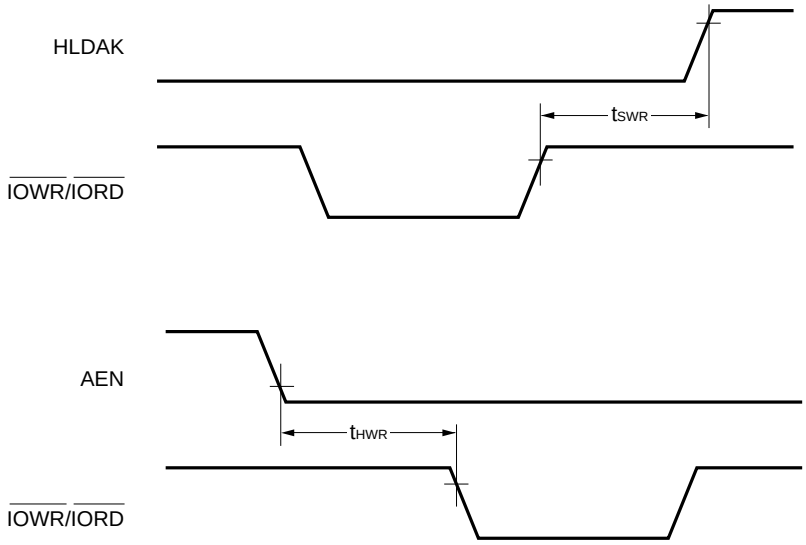

CS
A0 to A23
tSAR
tHRA
tRRL
IORD
tFRD
tDRD
D0 to D15
Hi-Z
Hi-Z


VDD
tSVDD
tRSTL
RESET
tSYWR
IORD/IOWR


tRVWR
IORD
tRVWR
tRVWR
IOWR
tRVWR

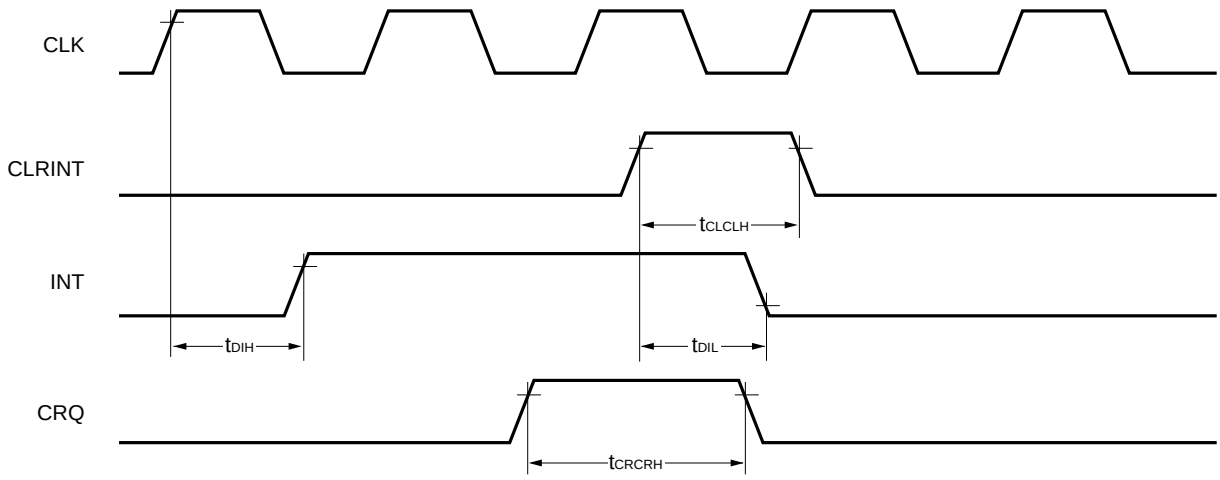
Bus Slave (2)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{IOWR}$/$\overline{IORD}$ high setup time (to HLDAK high)	t_{SWR}		–10		ns
$\overline{IOWR}$/$\overline{IORD}$ high hold time (from AEN low)	t_{HWR}		50		ns



Bus Slave (3)

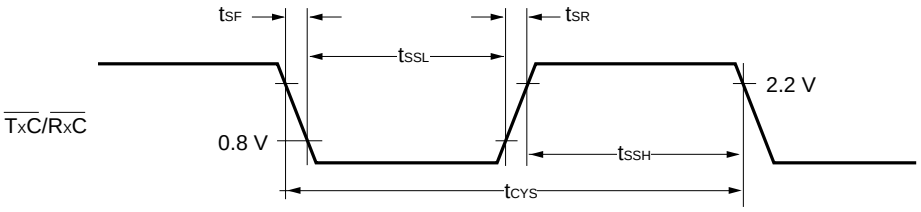
Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
CLRINT high level width	t_{CLCLH}		50		ns
INT delay time (from CLK high)	t_{DIH}			50	ns
INT low delay time (from CLRINT high)	t_{DIL}			50	ns
CRQ high level width	t_{CRCRH}		50		ns

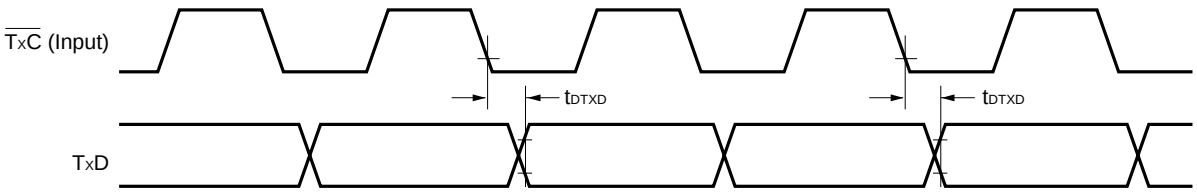


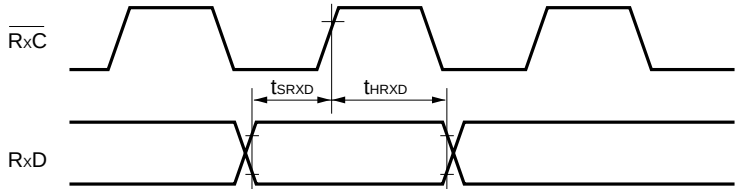
Serial Section (1)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{T_xC}/\overline{R_xC}$ cycle time	t_{CYS}	When on-chip DPLL is not used	125	DC	ns
$\overline{T_xC}/\overline{R_xC}$ low time	t_{SSL}		55		ns
$\overline{T_xC}/\overline{R_xC}$ high time	t_{SSH}		55		ns
$\overline{T_xC}/\overline{R_xC}$ rise time	t_{SR}			7	ns
$\overline{T_xC}/\overline{R_xC}$ fall time	t_{SF}			7	ns
T_xD delay time (from $\overline{T_xC}$ low)	t_{DTXD}			40	ns
R_xD setup time (to $\overline{R_xC}$ high)	t_{SRXD}		20		ns
R_xD hold time (from $\overline{R_xC}$ high)	t_{HRXD}		35		ns

Serial Clock

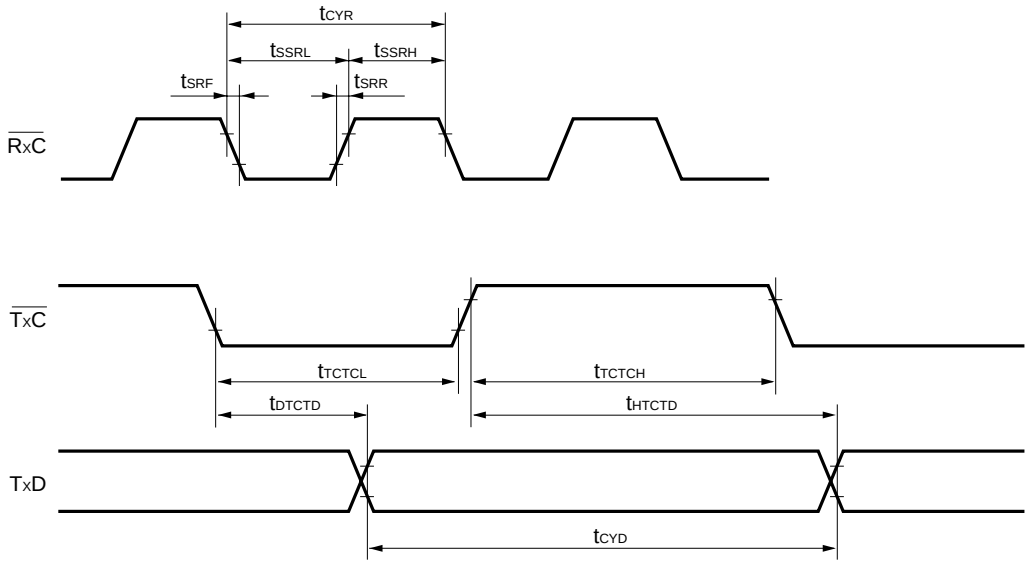






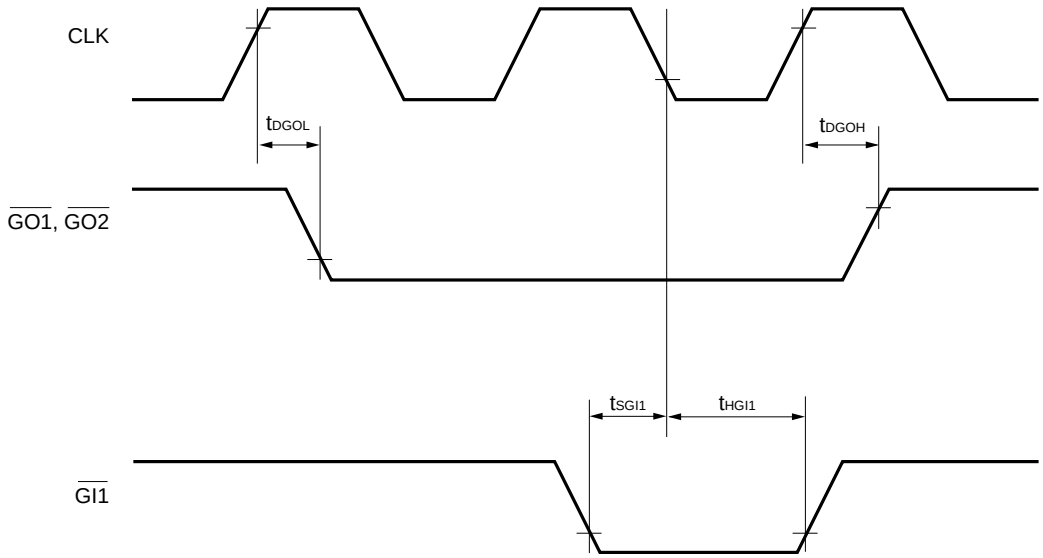
Serial Section (2)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{R_XC}$ cycle time	t_{CYR}	When on-chip DPLL is used	30		ns
$\overline{R_XC}$ low time	t_{SSRL}		10		ns
$\overline{R_XC}$ high time	t_{SSRH}		10		ns
$\overline{R_XC}$ rise time	t_{SRR}			5	ns
$\overline{R_XC}$ fall time	t_{SRF}			5	ns
Transmission/reception data cycle	t_{CYD}		480		ns
$\overline{T_XC}$ low time	t_{TCTCL}		$0.5t_{CYD}$–25		ns
$\overline{T_XC}$ high time	t_{TCTCH}		$0.5t_{CYD}$–25		ns
T_XD delay time (from $\overline{T_XC}$ low)	t_{DTCTD}			50	ns
T_XD hold time (from $\overline{T_XC}$ high)	t_{HTCTD}		$0.5t_{CYD}$–25		ns



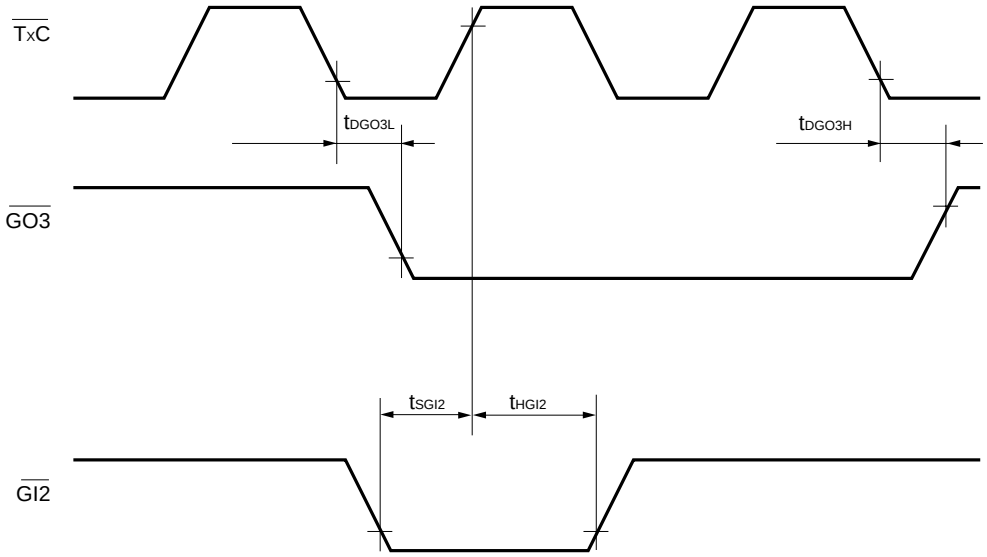
General-Purpose Input/Output Pins (1)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{GO1}$, $\overline{GO2}$ high delay time (from CLK high)	t_{DGOH}			50	ns
$\overline{GO1}$, $\overline{GO2}$ low delay time (from CLK high)	t_{DGOL}			50	ns
$\overline{GI1}$ setup time (to CLK low)	t_{SGI1}		20		ns
$\overline{GI1}$ hold time (from CLK low)	t_{HGI1}		10		ns



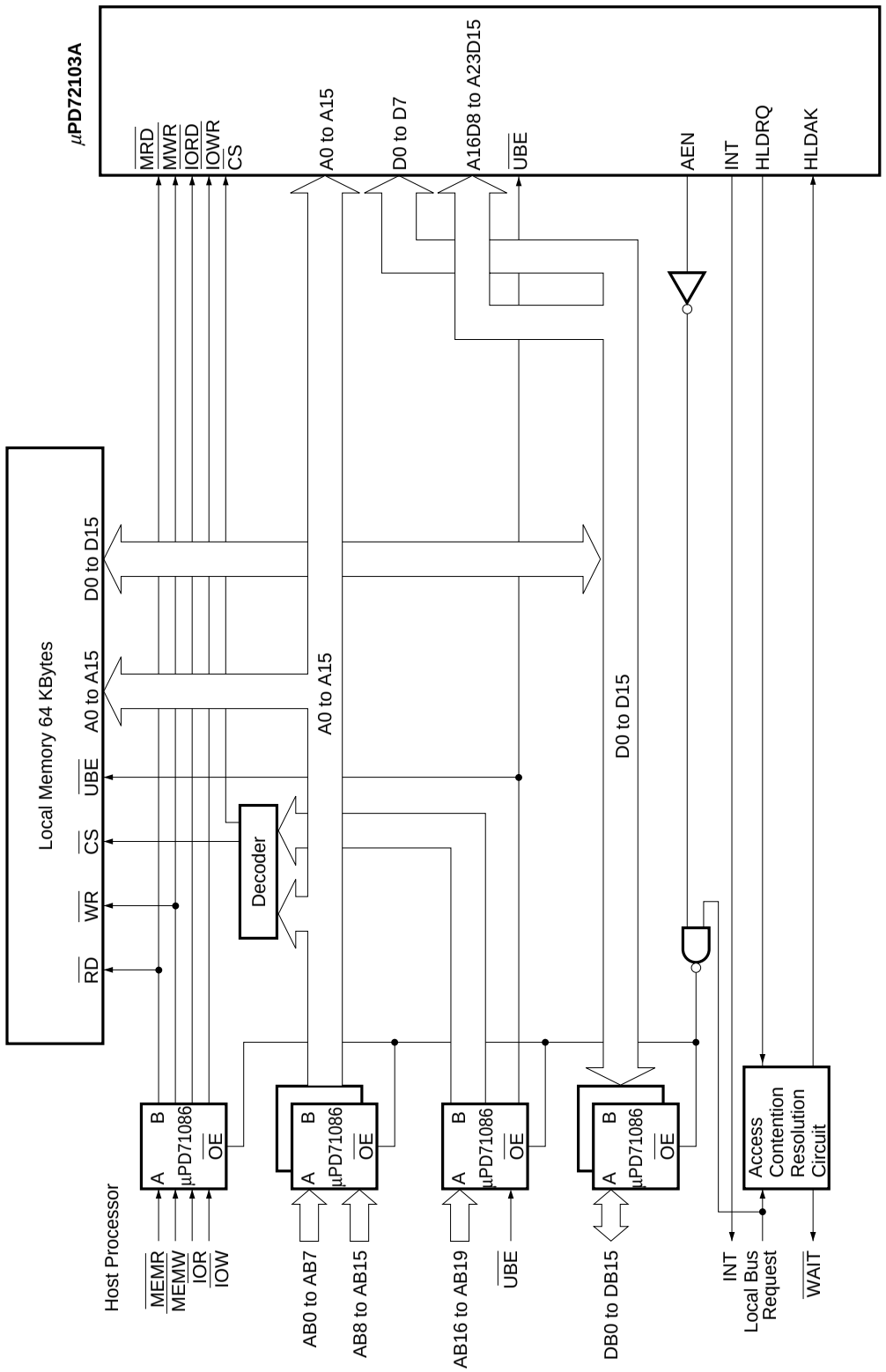
General-Purpose Input/Output Pins (2)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{GO3}$ high delay time (from $\overline{TxC}$ low)	t_{DGO3H}	At the use of LAP-D mode		50	ns
$\overline{GO3}$ low delay time (from $\overline{TxC}$ low)	t_{DGO3L}			50	ns
$\overline{GI2}$ setup time (to $\overline{TxC}$ high)	t_{SGI2}		20		ns
$\overline{GI2}$ hold time (from $\overline{TxC}$ high)	t_{HGI2}		20		ns

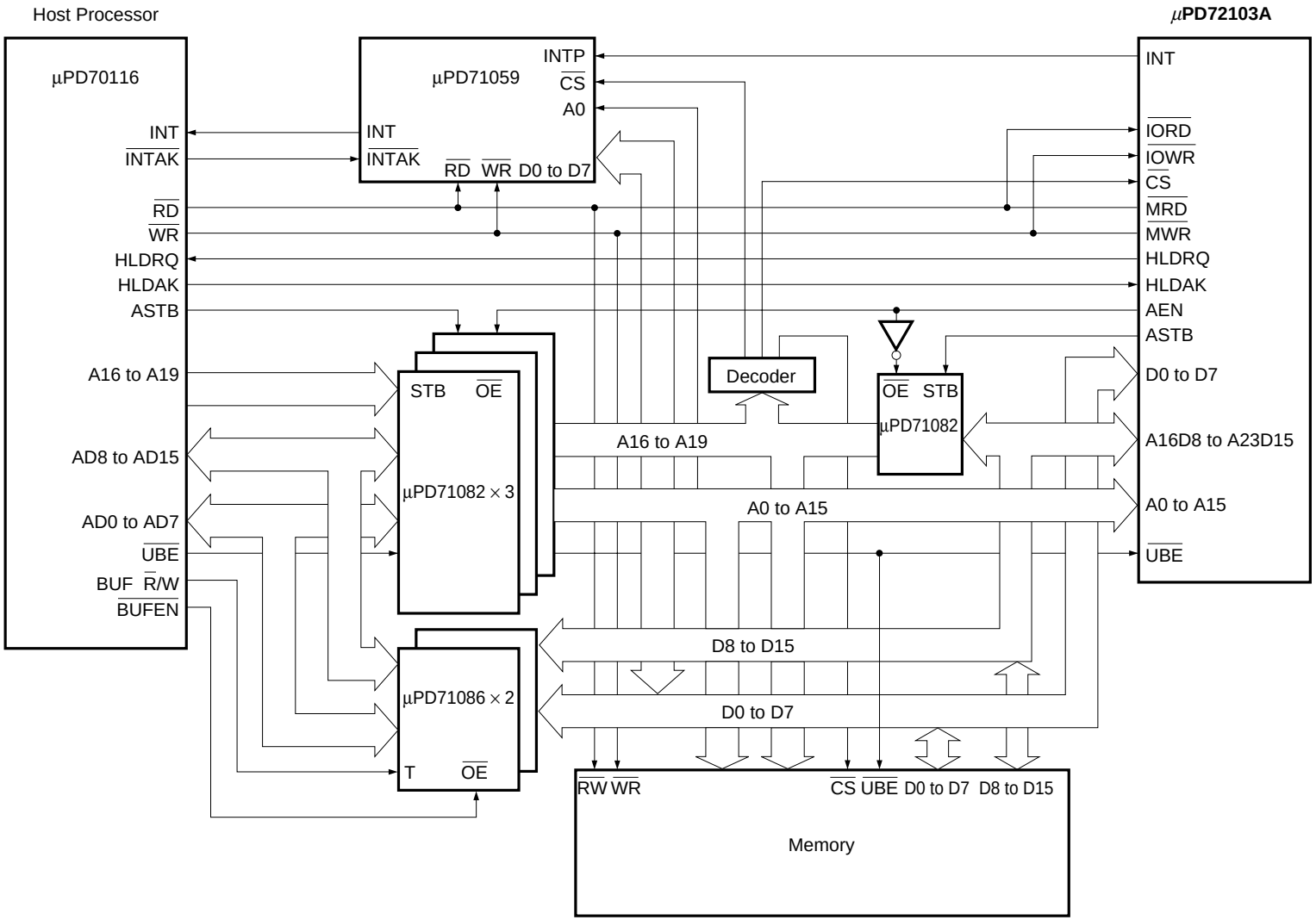


7. SYSTEM CONFIGURATION EXAMPLE

μPD72103A System Configuration Example (Local Memory Type)

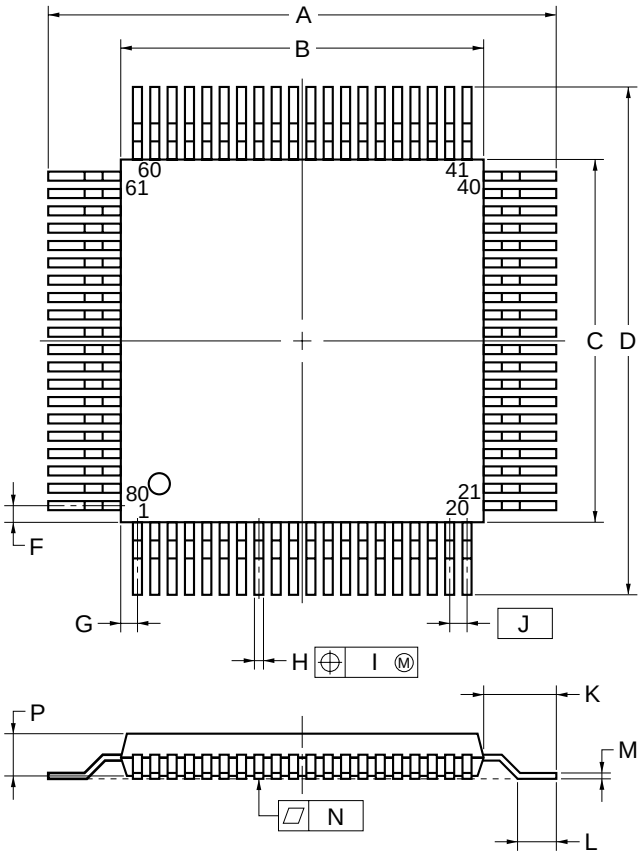


μPD72103A System Configuration Example (Main Memory Shared Type)

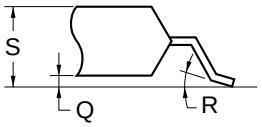


8. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14×14)



detail of lead end



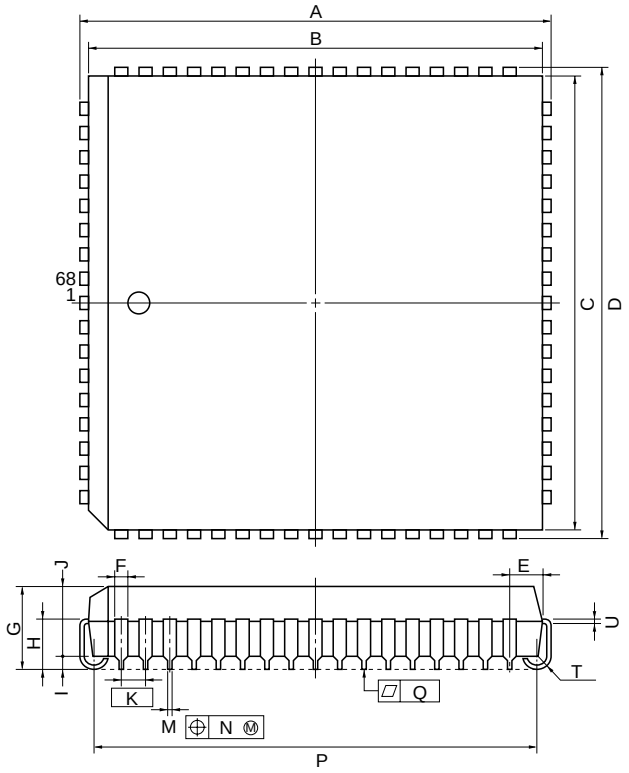
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.825	0.032
G	0.825	0.032
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

S80GC-65-3B9-4

68 PIN PLASTIC QFJ (□ 950 mil)



P68L-50A1-2

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	25.2±0.2	0.992±0.008
B	24.20	0.953
C	24.20	0.953
D	25.2±0.2	0.992±0.008
E	1.94±0.15	$0.076^{+0.007}_{-0.006}$
F	0.6	0.024
G	4.4±0.2	$0.173^{+0.009}_{-0.008}$
H	2.8±0.2	$0.110^{+0.009}_{-0.008}$
I	0.9 MIN.	0.035 MIN.
J	3.4	0.134
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±1.0	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	23.12±0.20	$0.910^{+0.009}_{-0.008}$
Q	0.15	0.006
T	R 0.8	R 0.031
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

★ 9. RECOMMEDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended below.

For details of recommended soldering conditions for the surface mounting type, refer to the document **"Semiconductor Device Mounting Technology Manual"** (**C10535E**).

For soldering methods and conditions other than those recommended below, contact your NEC sales representatives.

Surface Mounting Type

- **μPD72103AGC-3B9 : 80-pin plastic QFP (14 × 14 mm)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C Reflow time: 30 seconds max. (210°C min.) Number of reflow process: 3 max.	IR35-00-3
VPS	Package peak temperature: 215°C Reflow time 40 seconds max. (200°C min.) Number of reflow process: 3 max.	VP15-00-3
Wave soldering	Solder bath temperature: 260°C Reflow time: 10 seconds max., Number of reflow process: 1 Preheating temperature:120°C max. (package surface temperature)	WS60-00-1
Pin part heating	Pin temperature: 300°C max., Time: 3 seconds max. (per side of device)	———

Caution Use more than one soldering method should be avoided (except in the case of pin part heating).

- **μPD72103ALP : 68-pin plastic QFJ (950 × 950 mil)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
VPS	Package peak temperature: 215°C Reflow time: 40 seconds max., Number of reflow process: 1	VP15-00-1
Pin part heating	Pin temperature: 300°C max., Time: 3 seconds max. (per side of side)	———

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

The export of this product from Japan is prohibited without governmental license. To export or re-export this product from a country other than Japan may also be prohibited without a license from that country. Please call an NEC sales representative.

The application circuits and their parameters are for reference only and are not intended for use in actual design-in's.

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