PRELIMINARY DATA SHEET

NEC

MOS INTEGRATED CIRCUIT
µPD70F3224, µPD70F3226

V850ES/GB1™ VENUS
32-/16-bit Single-Chip Microcontroller with CAN Interface

DESCRIPTION

The V850ES/GB1 VENUS single chip microcontroller is a member of NEC's V850 32-bit RISC family, which match the performance gains attainable with RISC-based controllers to the needs of embedded control applications. The V850 CPU offers easy pipeline handling and programming, resulting in compact code size comparable to 16-bit CISC CPUs.

The V850ES/GB1 offers an excellent combination of general purpose peripheral functions, like serial communication interfaces (UART, clocked SI), timers and measurement inputs (A/D converter), with dedicated CAN network support. The device offers power-saving modes to manage the power consumption effectively under varying conditions. Thus equipped, the V850ES/GB1 VENUS is ideally suited for automotive applications.

FEATURES

- 32-bit RISC CPU with Harvard Architecture
- Internal Flash EEPROM: 128 KB
- Internal RAM: 6 KB
- CAN Interface: 1 channel (DCAN)
- Serial Interfaces: 4 channels
  - 3-wire mode: 2 channels
  - UART mode: 2 channels (LIN compatible)
- Timers: 7 channels
  - 16-bit dual time-base timer: 1 channel
  - 16-bit capture/compare timer: 1 channel
  - 8-bit multi purpose timer: 3 channels
  - Watch timer: 1 channel
  - Watchdog timer: 1 channel
- 10-bit resolution A/D Converter: 12 channels
- I/O lines: 84
- Power supply voltage range: +4.0 V to +5.5 V
- Frequency range:
  - Main: 8 to 16 MHz
  - Crystal Sub clock: 32.768 KHz (µPD70F3224)
  - RC sub clock: 40 to 100 KHz (µPD70F3226)
- Built-in low power saving mode:
  - Halt, Watch, Stop
- Temperature range:
  - -40°C to +85°C (µPD70F3224(A), µPD70F3226(A))
  - -40°C to +105°C (µPD70F3224(A1), µPD70F3226(A1))
- Package:
  - 100 LQFP, 0.5 mm pin-pitch (14 × 14 mm)

ORDERING INFORMATION

Device	Part Number	Package	Flash EEPROM	RAM	Sub Clock	Operating Temperature (T_A)
V850ES/GB1	µPD70F3224GC(A)-8EU	LQFP100 14 × 14 mm	128 KB	6 KB	Crystal	-40°C ~ +85°C
	PD70F3224GC(A1)-8EU					-40°C ~ +105°C
	µPD70F3226GC(A)-8EU				RC	-40°C ~ +85°C
	µPD70F3226GC(A1)-8EU					-40°C ~ +105°C

The information contained in this document is released in advance of the production cycle for the device. The parameters for the device may change before final production, or NEC Corporation may, at its own discretion, withdraw the device prior to production.

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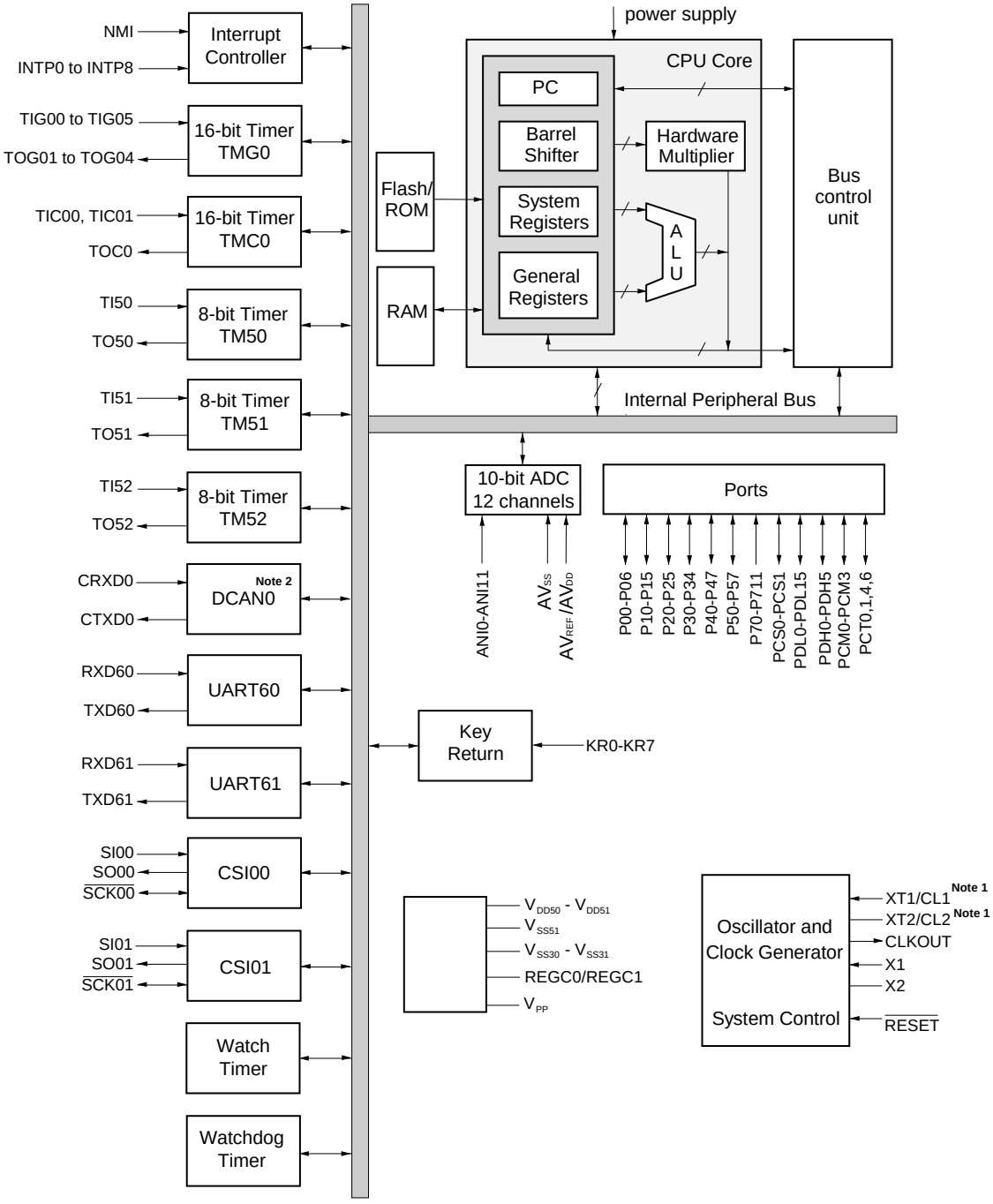
INTERNAL BLOCK DIAGRAM



Notes: 1. μPD78F3224: XT1,XT2,
μPD78F3226: CL1,CL2

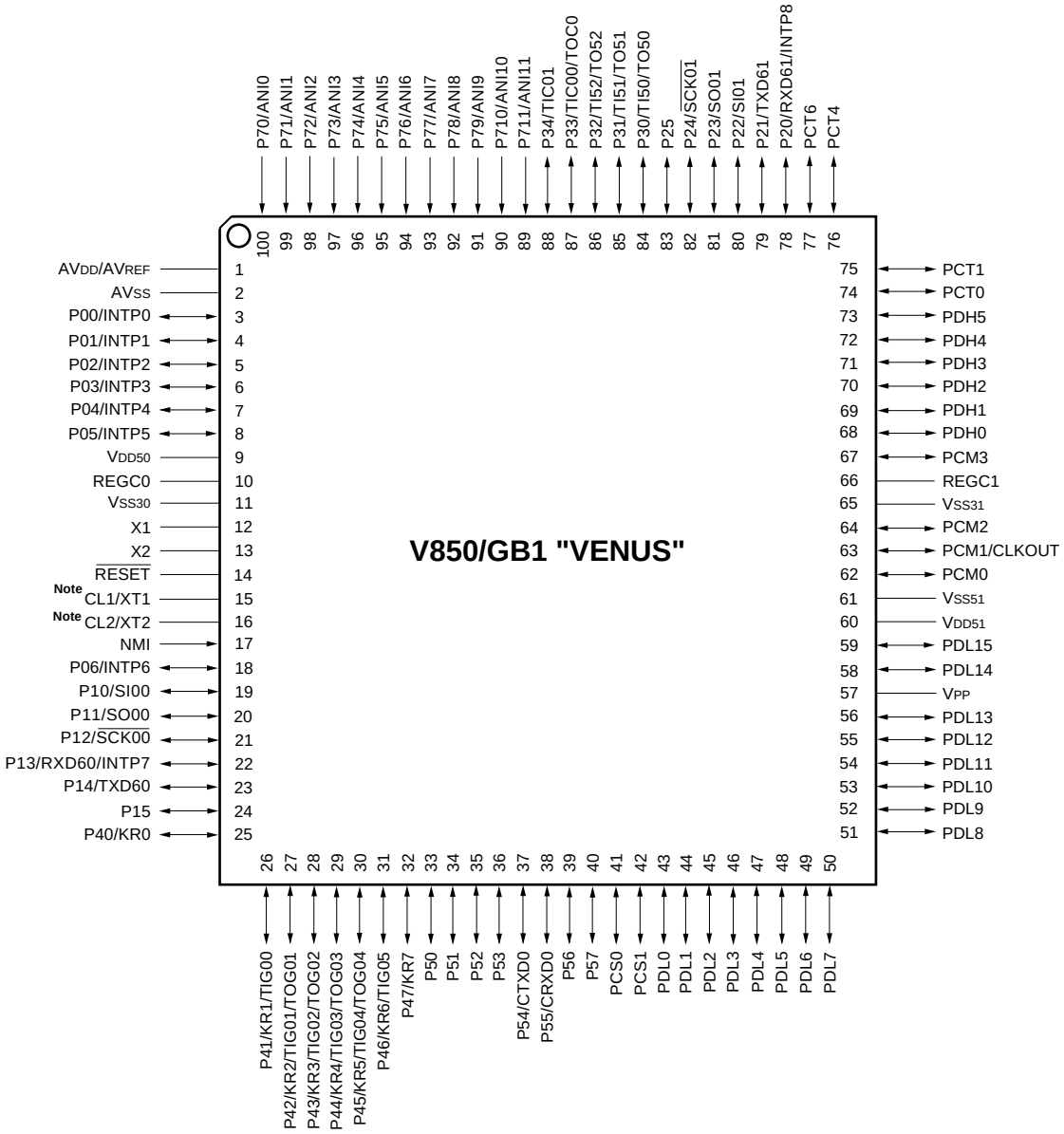
2. The CAN macro of this device fulfils the requirements according ISO 11898. Additionally the CAN macro was tested according to the test procedures required by ISO 16845. The CAN macro successfully passed all test patterns. Beyond these test patterns, other tests like robustness tests and processor interface tests as recommended by C&S/FH Wolfenbuettel have successfully been issued.

PIN IDENTIFICATION

ANI0 to ANI11	Analog Input
AV_{DD}/AV_{REF}	Analog Power Supply
AV_{SS}	Analog Ground
CLKOUT	Processor Clock Output
CRXD0	CAN Receive Data
CTXD0	CAN Transmit Data
INTP0 to INTP8	External Interrupt Input
NMI	Non-Maskable Interrupt Input
P00 to P06	Port 0
P10 to P15	Port 1
P20 to P25	Port 2
P30 to P34	Port 3
P40 to P47	Port 4
P50 to P57	Port 5
P70 to P711	Port 7
PCS0 to PCS1	Port CS
PCT0, PCT1, PCT4, PCT6	Port CT
PDH0 to PDH5	Port DH
PCM0 to PCM3	Port CM
PDL0 to PDL15	Port DL
KR0 to KR7	Key Return Inputs
$\overline{RESET}$	Reset Input
RXD60, RXD61	UART Receive Data
$\overline{SCK00}$, $\overline{SCK01}$	Synchronous Interface Clock
SI00, SI01	Synchronous Interface Input
SO00, SO01	Synchronous Interface Output
TI50, TI51, TI52	Timer 5 Count Input
TIC00, TIC01	Timer C0 Capture Input
TIG00 to TIG05	Timer G0 Capture Input
TO50, TO51, TO52	Timer 5 Compare Output
TOC0	Timer C0 Compare Output
TOG01 to TOG04	Timer G0 Compare Output
TXD60, TXD61	UART Transmit Data
X1, X2	Main System Clock
XT1, XT2 (CL1,CL2)	Crystal (RC) Sub Clock
REGC0, REGC1	3.3 V Regulator Output
V_{SS30}, V_{SS31}	Ground
V_{SS51}	Ground for I/O Buffers
V_{DD50}	Digital Power Supply
V_{DD51}	Power Supply for I/O Buffers
V_{PP}	Programming Voltage

PIN CONFIGURATION

- 100-Pin Plastic LQFP (fine pitch) (14 mm × 14 mm) (Top View)



Note: μPD78F3224: XT1,XT2,
μPD78F3226: CL1,CL2

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1.1 Pin Functions

Table 1-1: Pin Functions (1/4)

Pin		Function		I/O	Driver Type	Software Pull Up
No.	Name	Default	Alternate			
1	AV_{DD}/AV_{REF}	Analog Supply	-	-	-	-
2	AV_{SS}	Analog Ground	-	-	-	-
3	P00/INTP0	Port 0: 7-bit input/output port	External interrupt input INTP0	I/O	5-W	X
4	P01/INTP1		External interrupt input INTP1			
5	P02/INTP2		External interrupt input INTP2			
6	P03/INTP3		External interrupt input INTP3			
7	P04/INTP4		External interrupt input INTP4			
8	P05/INTP5		External interrupt input INTP5			
9	V_{DD50}	Digital Supply	-	-	-	-
10	REGC0	Internal Voltage Regulator Output	-	-	-	-
11	V_{SS30}	Digital Ground	-	-	-	-
12	X1	Main Oscillator Input	-	I	16	-
13	X2	Main Oscillator Output	-	O	16	-
14	$\overline{RESET}$	Reset Input	-	I	2	-
15	CL1/XT1	Sub Oscillator Input	-	I	16	-
16	CL2/XT2	Sub Oscillator Output	-	O	16	-
17	NMI	Non-Maskable Interrupt Input	-	I	2	-
18	P06/INTP6	Port 0: 7-bit input/output port	External interrupt input INTP6	I/O	5-W	X
19	P10/SI00	Port 1: 6-bit input/output port	3-wire Serial Link 0 Data Input	I/O	5-W	X
20	P11/SO00		3-wire Serial Link 0 Data Output	I/O	5-A	X
21	P12/$\overline{SCK00}$		3-wire Serial Link 0 Clock I/O	I/O	5-W	X
22	P13/RXD60/ INTP7		UART0 Data Input External interrupt input INTP7	I/O	5-W	X
23	P14/TXD60		UART0 Data Output	I/O	5-A	X
24	P15**Note**		-	I/O	5-A	X

Note: Usage of P15 is restricted: P15 has to be connected to V_{DD51} via a pull-up resistor before $\overline{RESET}$ release and the period of counting the oscillation stabilization time.

Table 1-1: Pin Functions (2/4)

Pin		Function		I/O	Driver Type	Software Pull Up
No.	Name	Default	Alternate			
25	P40/KR0	Port 4: 8-bit input/output port	Key Return Input 0	I/O	5-W	X
26	P41/KR1/ TIG00		Key Return Input 1 TimerG0 Capture Trigger 0 TimerG0 Compare Output 0	I/O	5-W	X
27	P42/KR2/ TIG01/TOG01		Key Return Input 2 TimerG0 Capture Trigger 1 TimerG0 Compare Output 1			
28	P43/KR3/ TIG02/TOG02		Key Return Input 3 TimerG0 Capture Trigger 2 TimerG0 Compare Output 2			
29	P44/KR4/ TIG03/TOG03		Key Return Input 4 TimerG0 Capture Trigger 3 TimerG0 Compare Output 3			
30	P45/KR5/ TIG04/TOG04		Key Return Input 5 TimerG0 Capture Trigger 4 TimerG0 Compare Output 4	I/O	5-W	X
31	P46/KR6/ TIG05		Key Return Input 6 TimerG0 Capture Trigger 5			
32	P47/KR7		Key Return Input 7			
33	P50	Port 5: 8-bit input/output port	-	I/O	5-A	X
34	P51		-		5-A	
35	P52		-		5-A	
36	P53		-		5-A	
37	P54/CTXD0		DCAN0 Transmit Data		5-A	
38	P55/CRXD0		DCAN0 Receive Data		5-W	
39	P56		-		5-A	
40	P57		-		5-A	
41	PCS0	Port CS: 2-bit input/output port	-	I/O	5-K	-
42	PCS1		-			
43	PDL0	Port DL: 16-bit input/output port	-	I/O	5-K	-
44	PDL1		-			
45	PDL2		-			
46	PDL3		-			
47	PDL4		-			
48	PDL5		-			
49	PDL6		-			
50	PDL7		-			
51	PDL8		-			
52	PDL9		-			
53	PDL10		-			
54	PDL11		-			
55	PDL12		-			
56	PDL13		-			
57	V_{PP}	Programming Voltage Input	-	-	-	-

Table 1-1: Pin Functions (3/4)

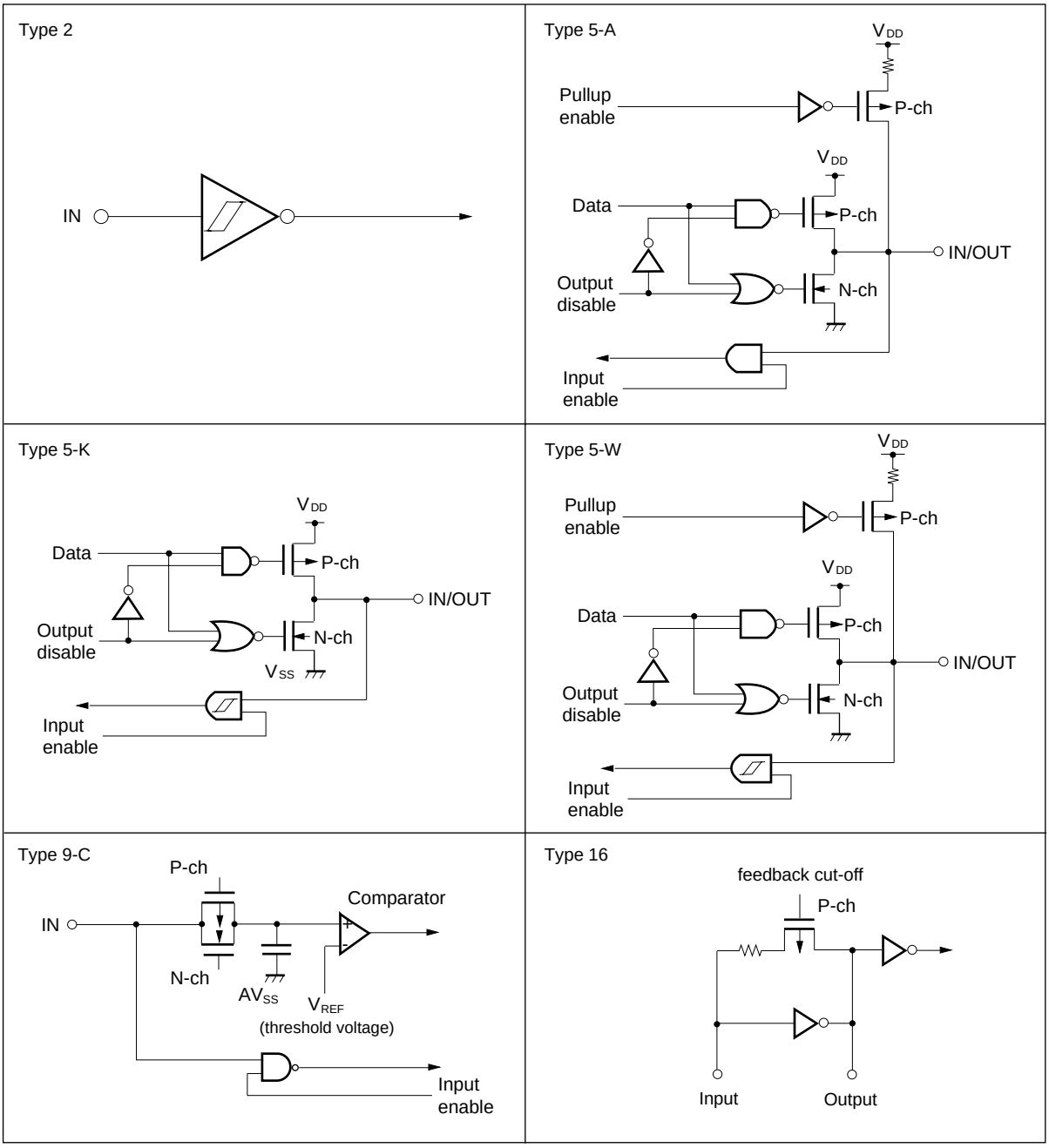
Pin		Function		I/O	Driver Type	Software Pull Up
No.	Name	Default	Alternate			
58	PDL14	Port DL: 16-bit input/output port	-	I/O	5-K	-
59	PDL15		-			
60	V_{DD51}	Power Supply I/O Buffers	-	-	-	-
61	V_{SS51}	I/O Buffers Ground	-	-	-	-
62	PCM0	Port CM: 4-bit input/output port	-	I/O	5-K	-
63	PCM1/ CLKOUT		CPU Clock Output			
64	PCM2		-			
65	V_{SS31}	Digital Ground	-	-	-	-
66	REGC1	Internal Voltage Regulator Output	-	-	-	-
67	PCM3	Port CM: 4-bit input/output port	-	I/O	5-K	-
68	PDH0	Port DH: 6-bit input/output port	-			
69	PDH1		-			
70	PDH2		-			
71	PDH3		-			
72	PDH4		-			
73	PDH5		-			
74	PCT0	Port CT: 4-bit input/output port	-	I/O	5-K	-
75	PCT1		-			
76	PCT4		-			
77	PCT6		-			
78	P20/RXD61/ INTP8	Port 2: 6-bit input/output port	UART1 Data Input External interrupt input INTP8	I/O	5-W	X
79	P21/TXD61		UART1 Data Output		5-A	
80	P22/SI01		3-wire Serial Link 1 Data Input		5-W	
81	P23/SO01		3-wire Serial Link 1 Data Output		5-A	
82	P24/$\overline{SCK01}$		3-wire Serial Link 1 Clock I/O		5-W	
83	P25		-		5-A	
84	P30/TI50/ TO50	Port 3: 5-bit input/output port	8-bit Timer 50 External Clock Input / PWM Output	I/O	5-W	X
85	P31/TI51/ TO51		8-bit Timer 51 External Clock Input / PWM Output			
86	P32/TI52/ TO52		8-bit Timer 52 External Clock Input / PWM Output			
87	P33/TIC00/ TOC0		16 bits TimerC0 Capture Trigger 0 / Compare Output 0			
88	P34/TIC01		16 bits TimerC0 Capture Trigger 1			

Table 1-1: Pin Functions (4/4)

Pin		Function		I/O	Driver Type	Software Pull Up
No.	Name	Default	Alternate			
89	P711/ANI11	Port 7: 12-bit input port	ANI11	I	9-C	–
90	P710/ANI10		ANI12			
91	P79/ANI9		ANI9			
92	P78/ANI8		ANI8			
93	P77/ANI7		ANI7			
94	P76/ANI6		ANI7			
95	P75/ANI5		ANI6			
96	P74/ANI4		ANI5			
97	P73/ANI3		ANI3			
98	P72/ANI2		ANI2			
99	P71/ANI1		ANI1			
100	P70/ANI0		ANI0			

1.2 I/O Circuits

Figure 1-1: Input / Output Circuits



1.3 Port Pin

Table 1-2: Mode of Port Pin After Reset (1/3)

Port Name	Pin Name	Pin Function after Reset Single Chip Mode	If not used
PNMI	NMI	NMI	Independently connect to V_{SS51} or V_{DD51} via resistor
P0	P00/INTP0	Port Mode (input mode)	Input: Independently connect to V_{SS51} or V_{DD51} via resistor Output: leave open
	P01/INTP1		
	P02/INTP2		
	P03/INTP3		
	P04/INPT4		
	P05/INPT5		
	P06/INPT6		
P1	P10/SI00	Port Mode (input mode)	Input: Independently connect to V_{SS51} or V_{DD51} via resistor Output: leave open
	P11/SO00		
	P12/$\overline{SCK00}$		
	P13/INTP7/RXD60		
	P14/TXD60		
	P15 **Note**		
P2	P20/INTP8/RXD61	Port Mode (input mode)	Input: Independently connect to V_{SS51} or V_{DD51} via resistor Output: leave open
	P21/TXD61		
	P22/SIO01		
	P23/SO01		
	P24/$\overline{SCK01}$		
	P25		
P3	P30/TI50/TO50	Port Mode (input mode)	Input: Independently connect to V_{SS51} or V_{DD51} via resistor Output: leave open
	P31/TI51/TO51		
	P32/TI52/TO52		
	P33/TIC00/TOC0		
	P34/TIC01		
P4	P40/KR0	Port Mode (input mode)	Input: Independently connect to V_{SS51} or V_{DD51} via resistor Output: leave open
	P41/KR1/TIG00		
	P42/KR2/TIG01/TOG01		
	P43/KR3/TIG02/TOG02		
	P44/KR4/TIG03/TOG03		
	P45/KR5/TIG04/TOG04		
	P46/KR6/TIG05		
	P47/KR7		

Note: Usage of P15 is restricted: P15 has to be connected to V_{DD51} via a pull-up resistor before $\overline{RESET}$ release and the period of counting the oscillation stabilization time.

Table 1-2: Mode of Port Pin After Reset (2/3)

Port Name	Pin Name	Pin Function after Reset Single Chip Mode	If not used
P5	P50	Port Mode (input mode)	Input: Independently connect to V_{SS51} or V_{DD51} via resistor Output: leave open
	P51		
	P52		
	P53		
	P54/CTXD0		
	P55/CRCD0		
	P56		
	P57		
P7	P70/ANI0	Port Mode (input mode)	Independently connect to AV_{SS} or AV_{DD} via resistor
	P71/ANI1		
	P72/ANI2		
	P73/ANI3		
	P74/ANI4		
	P75/ANI5		
	P76/ANI6		
	P77/ANI7		
	P78/ANI8		
	P79/ANI9		
	P710/ANI10		
	P711/ANI11		
PCS	PCS0	Port Mode (input mode)	Input: Independently connect to V_{SS51} or V_{DD51} via resistor Output: leave open
	PCS1		
PCT	PC0	Port Mode (input mode)	Input: Independently connect to V_{SS51} or V_{DD51} via resistor Output: leave open
	PC1		
	PC4		
	PC6		
PDH	PDH0	Port Mode (input mode)	Input: Independently connect to V_{SS51} or V_{DD51} via resistor Output: leave open
	PDH1		
	PDH2		
	PDH3		
	PDH4		
	PDH5		
PCM	PCM0	Port Mode (input mode)	Input: Independently connect to V_{SS51} or V_{DD51} via resistor Output: leave open
	PCM1		
	PCM2		
	PCM3		

Table 1-2: Mode of Port Pin After Reset (3/3)

Port Name	Pin Name	Pin Function after Reset Single Chip Mode	If not used
PDL	PDL0	Port Mode (input mode)	Input: Independently connect to V_{SS51} or V_{DD51} via resistor Output: leave open
	PDL1		
	PDL2		
	PDL3		
	PDL4		
	PDL5		
	PDL6		
	PDL7		
	PDL8		
	PDL9		
	PDL10		
	PDL11		
	PDL12		
	PDL13		
	PDL14		
	PDL15		

1.4 Non-Port Pin

Table 1-3: Non-Port Pin Recommended Connections

Pin Number	Pin name	Connection for normal operation	if not used
1	AV_{DD}	Analog power supply	Connect to V_{DD51}
2	AV_{SS}	Analog Ground	Connect to V_{SS51}
9	V_{DD50}	5.0 V Power supply	-
10	REGC0	Connect an 1 μF capacitor between this pin and Ground	-
11	V_{SS30}	Digital Ground	-
12	X1	Refer to 2.4.3 for recommended circuit	-
13	X2		-
14	$\overline{RESET}$	Reset input	-
15	XT1	Refer to 2.4.3 for recommended circuit	Connect to V_{SS30} or V_{SS31} via resistor
16	XT2		Leave open
57	V_{PP}	Connect to Ground for normal operation	-
60	V_{DD51}	I/O Buffers power supply	
61	V_{SS51}	I/O Buffers Ground	
65	V_{SS31}	Digital ground	
66	REGC1	Connect an 1 μF capacitor between this pin and Ground	

2. Electrical Specifications

2.1 Absolute Maximum Ratings

μPD70F3224(A), μPD70F3226(A),
μPD70F3224(A1), μPD70F3226(A1)

T_A = 25°C

Table 2-1: Absolute Maximum Ratings

Parameter		Symbol	Test Conditions	Ratings	Unit
Supply voltage		V_{DD50}, V_{DD51}		-0.5 ~ +6.0	V
		AV_{DD}	$AV_{DD} \le V_{DD5x}$ + 0.5 V	-0.5 ~ +6.0	
		V_{SS3x}, V_{SS51}		-0.5 ~ +0.5	
		AV_{SS}		-0.5 ~ +0.5	
		V_{PP}		-0,5 ~ +8.5	
Input voltage	All port pins[Note 1], NMI, $\overline{RESET}$	V_I	$V_I < V_{DD5x}$ + 0.5 V	-0.5 ~ +6.0	
Analog Input Voltage	P7	V_{AN}	$V_{AN} < AV_{DD}$ + 0.5 V	-0.5 ~ +6.0	
Output current low	1 pin	I_{OL}		4.0	mA
	All pins			50	
Output current high	1 pin	I_{OH}		-4.0	
	All pins			-50	
Output voltage	All port pins[Note 1] except P7	V_{O1}	$V_{O1} < V_{DD5x}$ + 0.5 V	-0.5 ~ +6.0	V
Operating temperature		T_A	Normal operating mode	-40 ~ +85 [Note 2]	°C
				-40 ~ +105 [Note 3]	
			Flash programming mode	-20 ~ +70	
Storage temperature		T_{STGA}	Before programming	-55 ~ +150	
		T_{STGB}	After programming	-55 ~ +125	

Remark: x = 0, 1

Notes: 1. All Ports pins are P0, P1, P2, P3, P4, P5, P7, PCS, PCT, PDH, PCM, PDL.

2. μPD70F3224(A), μPD70F3226(A)

3. μPD70F3224(A1), μPD70F3226(A1)

2.2 General Characteristics

2.2.1 Main Oscillator Characteristics

T_A= -40 ~ +85°C: μPD70F3224 (A), μPD70F3226 (A),
T_A= -40 ~ +105°C: μPD70F3224 (A1), μPD70F3226 (A1)

$V_{DD50} = V_{DD51} = AV_{DD}$ = 4.0 V ~ 5.5 V, $V_{SS30} = V_{SS31} = V_{SS51} = AV_{SS}$ = 0 V

Table 2-2: Main Oscillator Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Main oscillator frequency	f_{XX}		8		16	MHz
Oscillation stabilization time **Note 1**	T_{OST}	After Reset		$2^{17}/f_{XX}$		ms
		After Stop mode **Note 2**	2	**Note 3**		ms
		After Watch mode **Note 4**	100	**Note 3**		μs

Notes: 1. Minimum time, which is required for internal stabilization. The OSTS register has to be set to a time, which is longer than above defined values, before entering either WATCH or STOP mode.

2. Start-up time of external resonator is not included and must be checked with resonator supplier.

3. Typical value differs depending on settings of the Oscillation Stabilization Time Selection register (OSTS)

4. To release watch mode, minimum 11-clock cycles time is required. If sub clock is used to recover from watch mode, minimum time for watch mode release is determined by this 11-clock cycles.

2.2.2 Sub Oscillator Characteristics

(1) Crystal sub oscillator

T_A= -40 ~ +85°C: μPD70F3224 (A)
T_A= -40 ~ +105°C: μPD70F3224 (A1)

$V_{DD50} = V_{DD51} = AV_{DD}$ = 4.0 V ~ 5.5 V, $V_{SS30} = V_{SS31} = V_{SS51} = AV_{SS}$ = 0 V

Table 2-3: Crystal Sub Oscillator Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Sub oscillator frequency	f_{XT}			32.768		KHz
Oscillation stabilization time	T_{SOST}			10		s

(2) RC sub oscillator

T_A= -40 ~ +85°C: μPD70F3226 (A)
T_A= -40 ~ +105°C: μPD70F3226 (A1)

$V_{DD50} = V_{DD51} = AV_{DD}$ = 4.0 V ~ 5.5 V, $V_{SS30} = V_{SS31} = V_{SS51} = AV_{SS}$ = 0 V)

Table 2-4: RC Sub Oscillator Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Sub oscillator frequency	f_{XT}	R = 510 ± 5% KΩ, C = 33 ± 10% pF **Note**		40	100	KHz

Note: These values of R and C are typical values for f_{XT} = 40 KHz

2.2.3 I/O Capacitance

T_A= -40 ~ +85°C: μPD70F3224 (A), μPD70F3226 (A),
T_A= -40 ~ +105°C: μPD70F3224 (A1), μPD70F3226 (A1)

T_A = 25°C, $V_{DD50} = V_{DD51} = V_{SS51} = V_{SS30} = V_{SS31} = AV_{DD} = AV_{SS}$ = 0 V

Table 2-5: I/O Capacitance

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz Unmeasured pins returned to 0 V			15	pF
Input/output capacitance	C_{IO}				15	pF
Output capacitance	C_O				15	pF

2.3 DC Characteristics

μPD70F3224 (A), μPD70F3226 (A)

T_A= -40 ~ +85°C
$V_{DD50} = V_{DD51} = AV_{DD}$ = 4.0 V ~ 5.5 V, $V_{SS30} = V_{SS31} = V_{SS51} = AV_{SS}$ = 0 V

Table 2-6: DC Characteristics

Parameter		Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
High level Input Voltage	P11, P14-P15, P21, P23, P25, P50-P54, P56-P57	V_{IH1}		0.7 V_{DD51}		V_{DD51}	V
	P00-P06, P10, P12-P13, P20, P22, P24, P30-P34, PDL0-PDL15, PCM0-PCM3, PDH0-PDH5, PCT0, PCT1, PCT4, PCT6, NMI	V_{IH2}		0.8 V_{DD51}		V_{DD51}	
	P70-P711**Note**	V_{IH3}		0.7 V_{DD51}		AV_{DD}	
	$\overline{RESET}$	V_{IH4}		0.8 V_{DD51}		V_{DD51}	
Low level Input voltage	P11, P14-P15, P21, P23, P25, P50-P54, P56-P57	V_{IL1}		V_{SS51}		0.3 V_{DD51}	
	P00-P06, P10, P12-P13, P20, P22, P24, P30-P34, PDL0-PDL15, PCM0-PCM3, PDH0-PDH5, PCT0, PCT1, PCT4, PCT6, NMI	V_{IL2}		V_{SS51}		0.2 V_{DD51}	
	P70-P711**Note**	V_{IL3}		0		0.3 AV_{DD}	
	$\overline{RESET}$	V_{IL4}		V_{SS51}		0.2 V_{DD51}	
High Level Output Voltage		V_{OH1}	I_{OH} = -2.0 mA	V_{DD51} - 1.0 V		V_{DD51}	
			I_{OH} = -100 μA	V_{DD5x} - 0.5 V		V_{DD51}	
Low Level Output Voltage		V_{OL1}	I_{OL} = 2.0 mA			0.4	
			I_{OL} = 100 μA			0.2	
Input leakage current, high	except for X1, X2, XT1, XT2	I_{LIH1}	$V_I = V_{DD5}$		0.3	3	μA
Input leakage current, low	except for X1, X2, XT1, XT2	I_{LIL1}	V_I = 0 V		-0.3	-3	
Software Pull-up resistor	P0, P1, P2, P3, P4, P5	R1		10	30	100	KΩ

Note: Can only be used as digital input port when $AV_{DD} = V_{DD}$

μPD70F3224 (A1), μPD70F3226 (A1)

T_A= -40 ~ +105°C
$V_{DD50} = V_{DD51} = AV_{DD}$ = 4.0 V ~ 5.5 V, $V_{SS51} = V_{SS30} = V_{SS31} = AV_{SS}$ = 0 V

Table 2-7: DC Characteristics

Parameter		Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
High level Input Voltage	P11, P14-P15, P21, P23, P25, P50-P54, P56-P57	V_{IH1}		0.7 V_{DD51}		V_{DD51}	V
	P00-P06, P10, P12-P13, P20, P22, P24, P30-P34, PDL0-PDL15, PCM0-PCM3, PDH0-PDH5, PCT0, PCT1, PCT4, PCT6, NMI	V_{IH2}		0.8 V_{DD51}		V_{DD51}	
	P70-P711**Note**	V_{IH3}		0.7 V_{DD51}		AV_{DD}	
	$\overline{\text{RESET}}$	V_{IH4}		0.8 V_{DD51}		V_{DD51}	
Low level Input voltage	P11, P14-P15, P21, P23, P25, P50-P54, P56-P57	V_{IL1}		V_{SS51}		0.3 V_{DD51}	
	P00-P06, P10, P12-P13, P20, P22, P24, P30-P34, PDL0-PDL15, PCM0-PCM3, PDH0-PDH5, PCT0, PCT1, PCT4, PCT6, NMI	V_{IL2}		V_{SS51}		0.2 V_{DD51}	
	P70-P711**Note**	V_{IL3}		0		0.3 V_{DD51}	
	$\overline{\text{RESET}}$	V_{IL4}		V_{SS51}		0.2 V_{DD51}	
High Level Output Voltage		V_{OH1}	I_{OH} = -2.0 mA	V_{DD51} - 1.0 V		V_{DD51}	
			I_{OH} = -100 μA	V_{DD5x} - 0.5 V		V_{DD51}	
Low Level Output Voltage		V_{OL1}	I_{OL} = 2.0 mA			0.4	
			I_{OL} = 100 μA			0.2	
Input leakage current, high	except for X1, X2, XT1, XT2	I_{LIH1}	$V_I = V_{DD5}$			15	μA
Input leakage current, low	except for X1, X2, XT1, XT2	I_{LIL1}	V_I = 0 V			-15	
Software Pull-up resistor	P0, P1, P2, P3, P4, P5	R1		10	30	100	KΩ

Note: Can only be used as digital input port when $AV_{DD} = V_{DD}$

μPD70F3224 (A)

T_A= -40 ~ +85°C:
V_{DD50} = V_{DD51} = AV_{DD} = 4.0 V ~ 5.5 V, V_{SS51} = V_{SS30} = V_{SS31} = AV_{SS} = 0 V
f_{XX} = 16 MHz, f_{XT} = 32.768 KHz

Table 2-8: Power Supply Current

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Power Supply Current **Note 1** μPD70F3224(A)	I_{DD1}	Operating **Note 2**		35	50	mA
	I_{DD2}	HALT mode **Note 3**		10	20	
	I_{DD3}	WATCH mode **Note 4**		1.3	2	
	I_{DD4}	STOP mode **Note 5**		30	60	μA
	I_{DD5}	Sub Operating **Note 6**		360	600	
	I_{DD6}	Sub HALT mode **Note 7**		250	400	
	I_{DD7}	Sub WATCH mode **Note 8**		150	300	

Notes: 1. AV_{DD}/AV_{REF} current, port current (including a current flowing through the on-chip pull-up resistors) are not included.

2. CPU operating at maximum frequency (PCC = 0x00H), peripheral functions operating at maximum frequency (excepted DCAN0).

3. CPU stopped, peripheral functions operating at maximum frequency (excepted DCAN0).

4. CPU stopped, all peripheral functions stopped (Watch timer and Watchdog timer operating on subclock).

5. Subclock not connected.

6. CPU operating on subclock, main system clock oscillator stopped, all peripheral functions stopped, (Watch timer and Watchdog timer operating on subclock).

7. CPU stopped, main system clock oscillator stopped, all peripheral functions stopped (Watch timer and Watchdog timer operating on subclock).

8. CPU stopped, main system clock oscillator stopped, all peripheral functions stopped (Watch timer and Watchdog timer operating on subclock).

μPD70F3224 (A1)

T_A= -40 ~ +105°C:
$V_{DD50} = V_{DD51} = AV_{DD}$ = 4.0 V ~ 5.5 V, $V_{SS51} = V_{SS30} = V_{SS31} = AV_{SS}$ = 0 V
f_{XX} = 16 MHz, f_{XT} = 32.768 KHz

Table 2-9: Power supply current

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Power Supply Current Note 1 μPD70F3224(A1)	I_{DD1}	Operating Note 2		35	50	mA
	I_{DD2}	HALT mode Note 3		10	20	
	I_{DD3}	WATCH mode Note 4		1.3	3.5	
	I_{DD4}	STOP mode Note 5		30	1500	μA
	I_{DD5}	Sub Operating Note 6		360	2500	
	I_{DD6}	Sub HALT mode Note 7		250	2000	
	I_{DD7}	Sub WATCH mode Note 8		150	1800	

Notes: 1. AV_{DD}/AV_{REF} current, port current (including a current flowing through the on-chip pull-up resistors) are not included.

2. CPU operating at maximum frequency (PCC = 0x00H), peripheral functions operating at maximum frequency (excepted DCAN0).

3. CPU stopped, peripheral functions operating at maximum frequency (excepted DCAN0).

4. CPU stopped, all peripheral functions stopped (Watch timer and Watchdog timer operating on subclock).

5. Subclock not connected.

6. CPU operating on subclock, main system clock oscillator stopped, all peripheral functions stopped, (Watch timer and Watchdog timer operating on subclock).

7. CPU stopped, main system clock oscillator stopped, all peripheral functions stopped (Watch timer and Watchdog timer operating on subclock).

8. CPU stopped, main system clock oscillator stopped, all peripheral functions stopped (Watch timer and Watchdog timer operating on subclock).

μPD70F3224 (A), μPD70F3226 (A),
μPD70F3224 (A1), μPD70F3226 (A1)

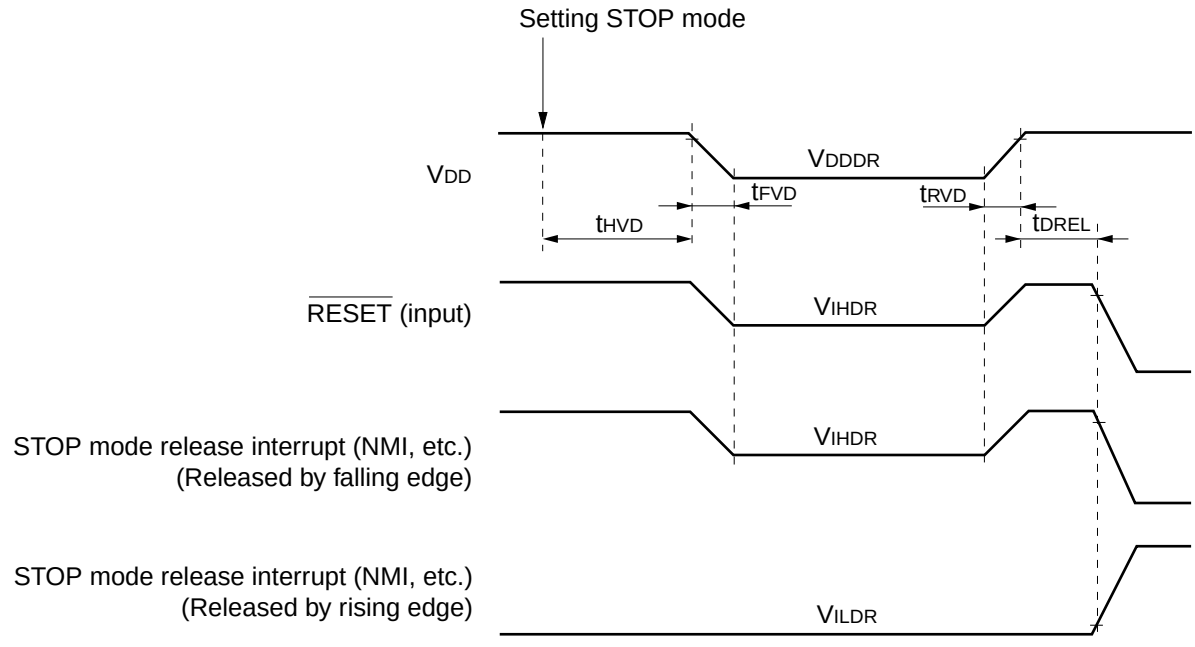
T_A= -40 ~ +85°C:

Table 2-10: Data Retention Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode **Note** (no functions operating)	3.0		5.5	V
Supply Voltage rise time	t_{RVD}		200			μs
Supply Voltage fall time	t_{FVD}		200			μs
Supply voltage hold time	t_{HVD}		0			ms
STOP release signal input time	t_{DREL}		0			ns
Data retention High-level input voltage	V_{IHDR}	All input ports	$0.9V_{DDDR}$		V_{DDDR}	V
Data retention High-level input voltage	V_{ILDR}	All input ports	0		$0.1V_{DDDR}$	V

Note: Subclock stopped

Figure 2-1: Data Retention Timing



2.4 AC Characteristics

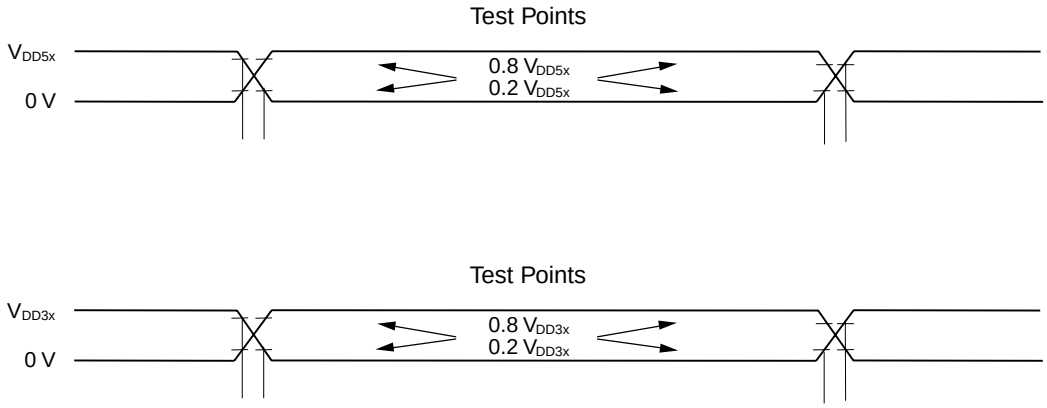
2.4.1 General

T_A= -40 ~ +85°C: μPD70F3224 (A), μPD70F3226 (A)
T_A= -40 ~ +105°C: μPD70F3224 (A1), μPD70F3226 (A1)

$V_{DD50} = V_{DD51} = AV_{DD}$ = 4.0 V ~ 5.5 V, $V_{SS51} = V_{SS30} = V_{SS31} = AV_{SS}$ = 0 V

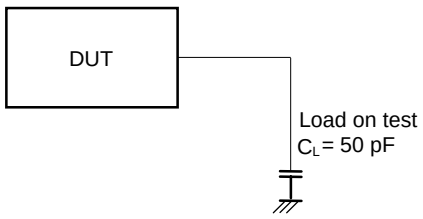
Output pin load capacitance: C_L= 50 pF

Figure 2-2: AC Test Input Waveform, AC Test Load Condition



2.4.2 AC Test Load Condition

Figure 2-3: AC Test Load Condition



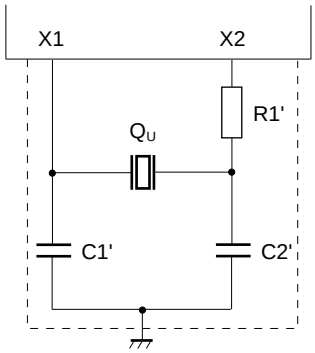
2.4.3 Recommended Oscillator Circuit

(1) Main system clock oscillator

(a) Ceramic resonator or crystal resonator connection

T_A= -40 ~ +85°C: μPD70F3224 (A), μPD70F3226 (A)
T_A= -40 ~ +105°C: μPD70F3224 (A1), μPD70F3226 (A1)

Figure 2-4: Main Oscillator Recommendations



Remark: Values of capacitors C1', C2' and R1' depend on used resonator and must be specified in cooperation with the manufacturer.

Cautions: 1. External clock input is prohibited.

2. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

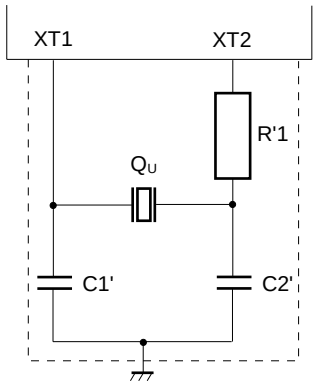
- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

(2) Recommended Subsystem clock oscillator circuit

(a) Ceramic resonator or crystal resonator connection

T_A= -40 ~ +85°C: μPD70F3224 (A)
T_A= -40 ~ +105°C: μPD70F3224 (A1)

Figure 2-5: Sub Oscillator Recommendations



Remark: Values of capacitors C1', C2' and resistors R'1 depend on used resonator and must be specified in cooperation with the manufacturer.

Cautions: 1. External clock input is prohibited.

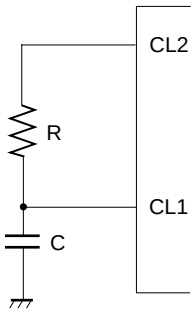
2. When using the sub system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

(b) RC Oscillator connection

T_A= -40 ~ +85°C: μPD70F3226 (A)
T_A= -40 ~ +105°C: μPD70F3226 (A1)

Figure 2-6: RC Oscillator Connection



2.4.4 Voltage regulator

T_A= -40 ~ +85°C: μPD70F3224 (A), μPD70F3226 (A)
T_A= -40 ~ +105°C: μPD70F3224 (A1), μPD70F3226 (A1)

V_{DD50} =V_{DD51} = AV_{DD} = 4.0 V ~ 5.5 V, V_{SS51} = V_{SS30} = V_{SS31} = AV_{SS} = 0 V

Table 2-11: Voltage regulator

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Output voltage stabilization time	t_{REG}	Time starts when V_{DD50} reaches minimum value of 4.0 V (C_{REGC0} = C_{REGC1} = 1 μF) **Note**		2	ms

Note: C_{REGC0} & C_{REGC1} are respectively connected to REGC0 and REGC1 pins. They must have the same value.

Remark: To improve EMI and noise filtering, it might be necessary to connect small size capacitances in parallel with C_{REGC0} & C_{REGC1}.

2.4.5 Reset

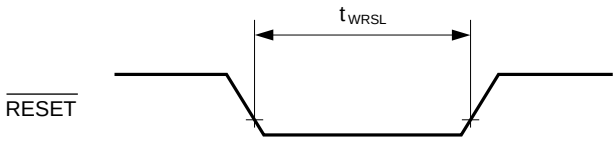
T_A= -40 ~ +85°C: μPD70F3224 (A), μPD70F3226 (A)
T_A= -40 ~ +105°C: μPD70F3224 (A1), μPD70F3226 (A1)

$V_{DD50} = V_{DD51} = AV_{DD}$ = 4.0 V ~ 5.5 V, $V_{SS51} = V_{SS30} = V_{SS31} = AV_{SS}$ = 0 V

Table 2-12: Reset Timing

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ low-level width	t_{WRSL}		500		ns

Figure 2-7: $\overline{\text{RESET}}$ Timing



2.4.6 Peripheral Function Characteristics

(1) Key return timing

T_A= -40 ~ +85°C: μPD70F3224 (A), μPD70F3226 (A)
T_A= -40 ~ +105°C: μPD70F3224 (A1), μPD70F3226 (A1)

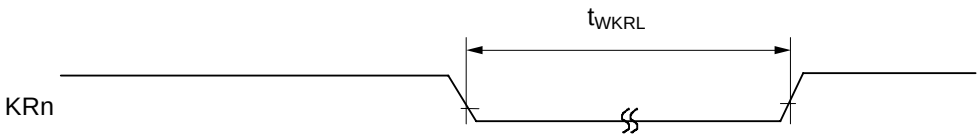
$V_{DD50} = V_{DD51} = AV_{DD}$ = 4.0 V ~ 5.5 V, $V_{SS51} = V_{SS30} = V_{SS31} = AV_{SS}$ = 0 V

Table 2-13: Key Return Timing

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
KRn input low level width **Note**	t_{WKRL}		500		ns

Note: n = 0 to 7

Figure 2-8: Key Return Timing



(2) Interrupt Timing

T_A= -40 ~ +85°C: μPD70F3224 (A), μPD70F3226 (A)
T_A= -40 ~ +105°C: μPD70F3224 (A1), μPD70F3226 (A1)

$V_{DD50} = V_{DD51} = AV_{DD}$ = 4.0 V ~ 5.5 V, $V_{SS51} = V_{SS30} = V_{SS31} = AV_{SS}$ = 0 V

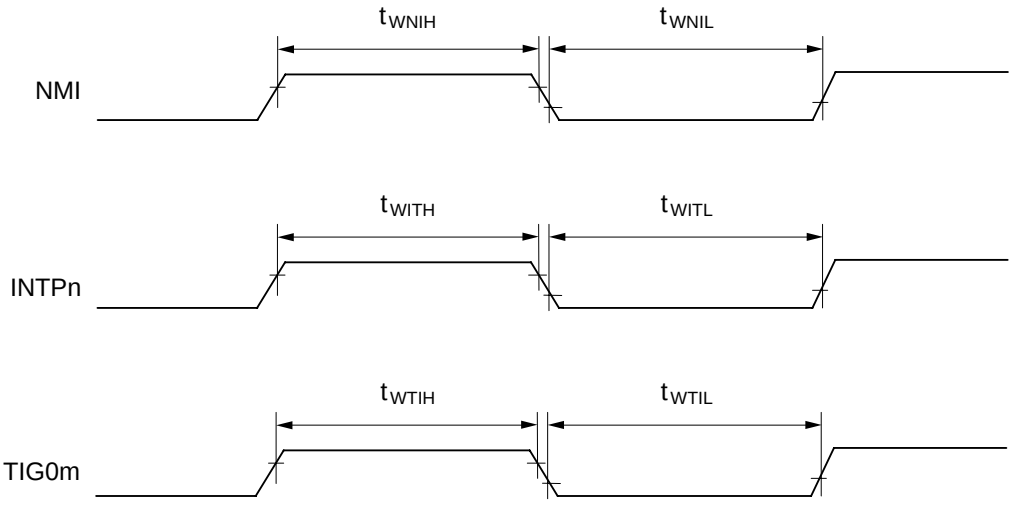
Table 2-14: Interrupt Timing

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
NMI high-level width	t_{WNIH}		500		ns
NMI low-level width	t_{WNIL}		500		ns
INTPn**Note 1** high-level width	t_{WITH}		500		ns
INTPn**Note 1** low-level width	t_{WITL}		500		ns
TIG0m, TIC0n**Note 2** high-level width	t_{WTIH}		500		ns
TIG0m, TIC0n**Note 2** low-level width	t_{WTIL}		500		ns

Notes: 1. n = 0 to 8

2. n = 0 to 1, m = 0 to 5

Figure 2-9: Interrupt Timing



Remarks: 1. n = 0 to 8

2. m = 0 to 5

(3) Timer G0 / Timer C0 /Timer 5n

T_A= -40 ~ +85°C: μPD70F3224 (A), μPD70F3226 (A)
T_A= -40 ~ +105°C: μPD70F3224 (A1), μPD70F3226 (A1)

$V_{DD50} = V_{DD51} = AV_{DD}$ = 4.0 V ~ 5.5 V, $V_{SS51} = V_{SS30} = V_{SS31} = AV_{SS}$ = 0 V

Table 2-15: Timer G0 / Timer C0 / Timer 5n Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
TIG0m high-level width**Note 1**	t_{WTIGH}		T_T x 2 + 20**Note 2**		ns
TIG0m low-level width**Note 1**	t_{WTIGL}		T_T x 2 + 20**Note 2**		ns
TIC0m high-level width**Note 3**	t_{WTICH}		T_T x 2 + 20**Note 2**		ns
TIC0m low-level width**Note 3**	t_{WTICL}		T_T x 2 + 20**Note 2**		ns
TI5n input cycle time**Note 4**	T_{WTI5CY}		120		ns
TI5n input high level with**Note 4**	T_{WTI5CH}		48		ns
TI5n low level width**Note 4**	T_{WTI5CL}		48		ns

Notes: 1. n = 0 to 1, m = 0 to 5

2. T_T: Depends on selected clock source for the peripheral clock supply and the setup of the respective timer macro clock and timer channel setup

3. m = 0 to 1

4. n = 0 to 2

Figure 2-10: Timer G0 Characteristics

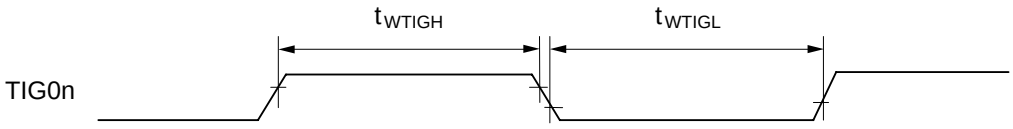


Figure 2-11: Timer C0 Characteristics

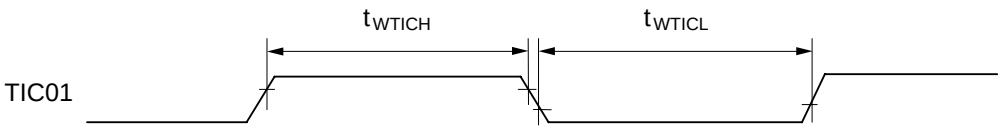
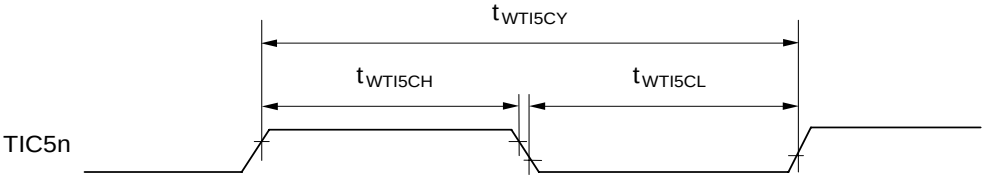


Figure 2-12: Timer 5n Characteristics



(4) CSI

T_A= -40 ~ +85°C: μPD70F3224 (A), μPD70F3226 (A)
T_A= -40 ~ +105°C: μPD70F3224 (A1), μPD70F3226 (A1)

V_{DD50} =V_{DD51} = AV_{DD} = 4.0 V ~ 5.5 V, V_{SS51} = V_{SS30} = V_{SS31} = AV_{SS} = 0

Table 2-16: CSI Master Mode Characteristics

Parameter Note	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{SCK0n}$ cycle time	t_{CYSKM}	Output	200		ns
$\overline{SCK0n}$ high level width	t_{WSKHM}	Output	0.5 t_{CYSK} - 10		ns
$\overline{SCK0n}$ low level width	t_{WSKLM}	Output	0.5 t_{CYSK} - 10		ns
SI0n set up time (to $\overline{SCK0n}$ ↑)	t_{SSISKM}		30		ns
SI0n hold time (from $\overline{SCK0n}$ ↑)	t_{HSKSIM}		30		ns
SO0n output delay time (from $\overline{SCK0n}$ ↓)	t_{DSKSOM}			30	ns
SO0n output hold time (from $\overline{SCK0n}$ ↑)	t_{HSKSOM}		0.5 t_{CYSK} - tbd		ns

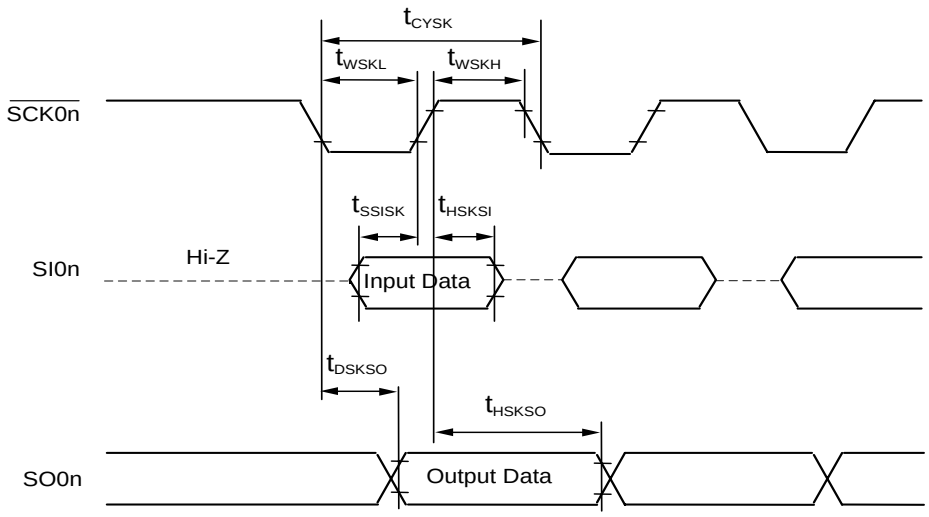
Note: n = 0, 1

Table 2-17: CSI Slave Mode Characteristics

Parameter Note	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{SCK0n}$ cycle time	t_{CYSKS}	Input	200		ns
$\overline{SCK0n}$ high level width	t_{WSKHS}	Input	0.5 t_{CYSKS} -10		ns
$\overline{SCK0n}$ low level width	t_{WSKLS}	Input	0.5 t_{CYSKS} -10		ns
SI0n set up time (to $\overline{SCK0n}$ ↑)	t_{SSISKS}		50		ns
SI0n hold time (from $\overline{SCK0n}$ ↑)	t_{HSKSIS}		50		ns
SO0n output delay time (from $\overline{SCK0n}$ ↓)	t_{DSKSOS}			50	ns
SO0n output hold time (from $\overline{SCK0n}$ ↑)	t_{HSKSOS}		t_{WSKH}		ns

Note: n = 0, 1

Figure 2-13: CSI Slave Mode Characteristics



(5) UART

T_A= -40 ~ +85°C: μPD70F3224 (A), μPD70F3226 (A)
T_A= -40 ~ +105°C: μPD70F3224 (A1), μPD70F3226 (A1)

$V_{DD50} = V_{DD51} = AV_{DD}$ = 4.0 V ~ 5.5 V, $V_{SS51} = V_{SS30} = V_{SS31} = AV_{SS}$ = 0 V

Table 2-18: UART Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Transfer rate	T_{UART}	$f_{Peripheral} \geq 5$ MHz		312500	bps

(6) DCAN

T_A= -40 ~ +85°C: μPD70F3224 (A), μPD70F3226 (A)
T_A= -40 ~ +105°C: μPD70F3224 (A1), μPD70F3226 (A1)

$V_{DD50} = V_{DD51} = AV_{DD}$ = 4.0 V ~ 5.5 V, $V_{SS51} = V_{SS30} = V_{SS31} = AV_{SS}$ = 0 V

Table 2-19: DCAN Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Transfer rate	T_{DCAN}	f_{XX} = 16 MHz		1	Mbps

2.5 A/D Converter

T_A= -40 ~ +85°C: μPD70F3224 (A), μPD70F3226 (A)

$V_{DD50} = V_{DD51} = AV_{DD}$ = 4.5 V ~ 5.5 V, $V_{SS51} = V_{SS30} = V_{SS31} = AV_{SS}$ = 0 V

Table 2-20: A/D Converter Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution	-			10		Bit
Overall Error[Note 1]	-				±3	LSB
Conversion time[Note 2]	T_{CONV}		5		12	μs
Sampling time[Note 3]	T_{SAM}			T_{CONV}/6		μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{DD}	V
Analog supply current	I_{AVDD}	A/D converter is operating		4.0	8.0	mA.
	I_{LAVDD}	A/D converter is stopped		1	5	μA

Notes: 1. The quantization error is not included

2. The conversion time T_{CONV} depends on the setting of the ADM register

3. The sampling time T_{SAM} depends on the setting of the ADM register

T_A= -40 ~ +105°C: μPD70F3224 (A1), μPD70F3226 (A1)

$V_{DD50} = V_{DD51} = AV_{DD}$ = 4.5 V ~ 5.5 V, $V_{SS51} = V_{SS30} = V_{SS31} = AV_{SS}$ = 0 V

Table 2-21: A/D Converter Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution	-			10		Bit
Overall Error[Note 1]	-				±6	LSB
Conversion time[Note 2]	T_{CONV}		5		12	μs
Sampling time[Note 3]	T_{SAM}			T_{CONV}/6		μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{DD}	V
Analog supply current	I_{AVDD}	A/D converter is operating		4.0	8.0	mA
	I_{LAVDD}	A/D converter is stopped		2	10	μA

Notes: 1. The quantization error is not included

2. The conversion time T_{CONV} depends on the setting of the ADM register

3. The sampling time T_{SAM} depends on the setting of the ADM register

2.6 Flash EEPROM Characteristics

T_A= -40 ~ +85°C: μPD70F3224 (A), μPD70F3226 (A)
T_A= -40 ~ +105°C: μPD70F3224 (A1), μPD70F3226 (A1)

$V_{DD50} = V_{DD51} = AV_{DD}$ = 4.0 V ~ 5.5 V, $V_{SS51} = V_{SS30} = V_{SS31} = AV_{SS}$ = 0 V

(1) Basic specification

Table 2-22: Flash EEPROM Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		4.0		5.5	V
	V_{PP}		0.8 V_{DD}		1.2 V_{DD}	V
	V_{PPH}		7.5	7.8	8.1	V
	V_{PPL}		0		0.5	V
V_{PP} Supply current	I_{PP}			40	80	mA
Maximum times of reprogramming	C_{WRT}		100			times
Write time	T_{WRT}	Byte		20	200	μs
Erase time	t_{ERASEB}	Block (64 KBytes)		0.2	20	s
	t_{ERASEA}	Block (128 KBytes)		0.4	40	s
Programming temperature	T_{PRG}		- 20		+70	°C

(2) Serial programming operation characteristics

Table 2-23: Serial Programming Operation Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
V_{DD5X} ↑ setup time to V_{PP} ↑	t_{VDD5SU}		1.0			ms
V_{DD5X} ↑ hold time to V_{PP} ↑	t_{VDD5HD}		1.0			ms
V_{DD5X} ↑ setup time to $\overline{RESET}$ ↑	t_{DRRR}		10			μs
V_{PP}↑ setup time to $\overline{RESET}$ ↑	t_{PSRRF}		1			μs
$\overline{RESET}$ ↑ count start setup time (to V_{PPH} level)	t_{RFOF}	$V_{PP} = V_{PPH}$,T = $1/f_{XX}$	5T + 500			μs
Times of V_{PP} counting	t_{COUNT}				10	ms
V_{PP} count High level width	t_{CH}		1			μs
V_{PP} count low level width	t_{CL}		1			μs
V_{PP} count rise time	t_R				tbd	μs
V_{PP} count fall time	t_F				tbd	μs

Figure 2-14: V_{DD5X} Setup/Hold Time for V_{PP} Terminal

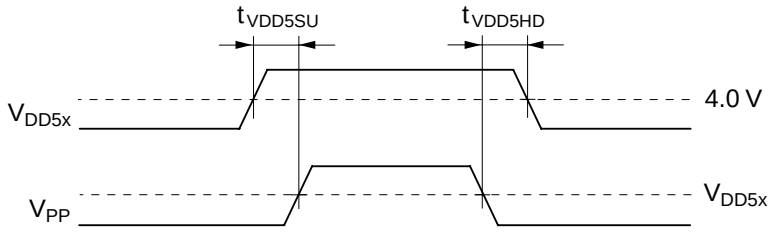
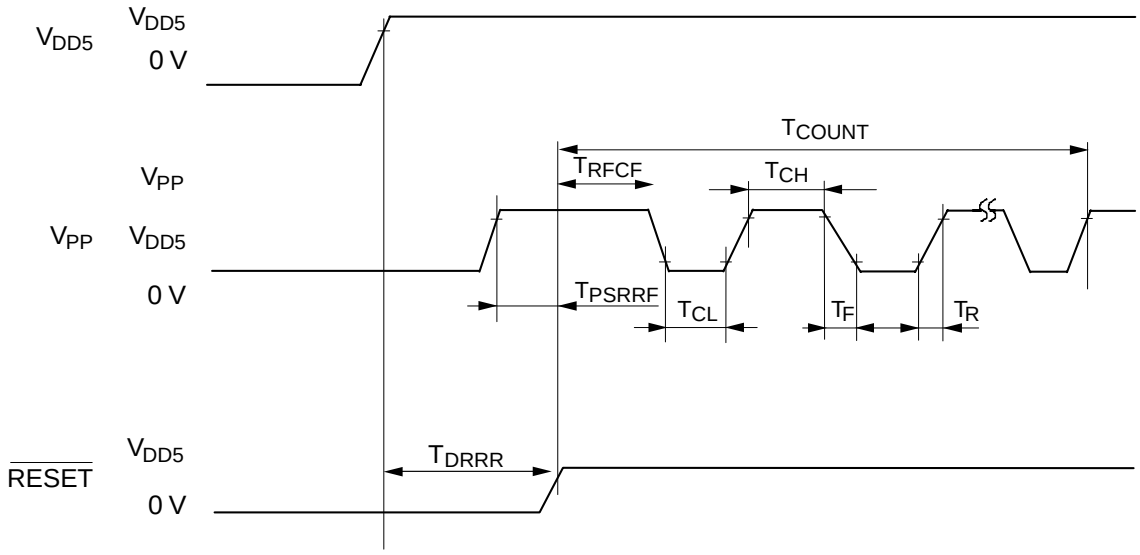


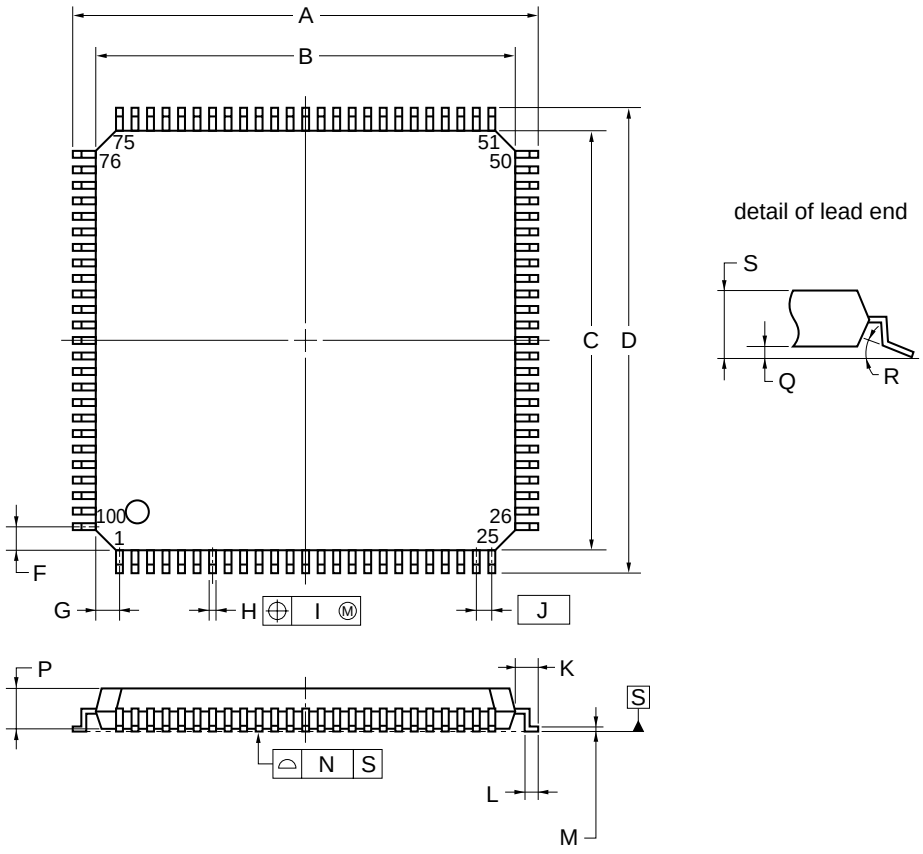
Figure 2-15: Flash EEPROM Programming Timings



3. Package Drawing

Figure 3-1: Package Drawing

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	$0.22^{+0.05}_{-0.04}$
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.60 MAX.

S100GC-50-8EU, 8EA-2

4. Recommended Soldering Conditions

Solder this product under the following recommended conditions.
For details of the recommended soldering conditions, refer to information document Semiconductor Device:
Mounting Technology Manual (C10535E).

For soldering methods and conditions other than those recommended please consult NEC.

Table 4-1: Soldering Conditions

Soldering Method	Soldering Condition	Symbol of Recommended Soldering Condition
Infrared reflow	Package peak temperature: 245°C, Time: 30 seconds max. (210°C min.), Number of times: 2 max., Number of days: 7 **Note**	IR45-207-2
VPS	Package peak temperature: 215°C, Time: 30 seconds max. (210°C min.), Number of times: 2 max., Number of days: 7 **Note**	VP15-207-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per side of device)	-

Note: After that, prebaking is necessary at tbd °C for tbd hours.
The number of days refers to storage at 25°C, 65% RH MAX after the dry pack has been opened.

Caution: Do not use two or more soldering methods in combination (except partial heating method).

5. Revision History

Version	Date	Author	Remarks
U15871EE1V1DS00	April 2003	ABU-SE	§2.5: A/D converter voltage range specification. Rework of document layout. Text and typing mistakes corrections.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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