

V850E/MA1™

## 32-BIT SINGLE-CHIP MICROCONTROLLERS

**DESCRIPTION**

The  $\mu$ PD70F3107A and 70F3107A(A) are products of the V850 Series™ of 32-bit single-chip microcontrollers for real-time control applications. This microcontroller integrates a 32-bit CPU, ROM, RAM, an interrupt controller, a real-time pulse unit, a serial interface, an A/D converter, a DMA controller, and other functions on a single chip.

The  $\mu$ PD70F3107A and 70F3107A(A) are products that substitute flash memory for the internal mask ROM of the  $\mu$ PD703107A and 703107A(A). This enables users to perform on-board program writing and erasure, making this product effective for evaluation during system development, small-lot production of multiple devices, and rapid production start.

**Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.**

**V850E/MA1 Hardware User's Manual: U14359E**  
**V850E1 Architecture User's Manual: U14559E**

**FEATURES**

- Number of instructions: 83
- Minimum instruction execution time: 20 ns (50 MHz internal operation)
- General-purpose registers: 32 bits  $\times$  32 registers
- Instruction set optimized for control applications
- Internal memory  
Flash memory: 256 KB  
RAM: 10 KB
- Memory access control (supporting EDO DRAM, SDRAM, and page ROM)
- Advanced internal interrupt controller
- Real-time pulse unit suitable for control operations
- Powerful serial interface (with dedicated internal baud rate generator)
- On-chip clock generator
- 10-bit resolution A/D converter: 8 channels
- DMA controller: 4 channels
- Power saving functions
- Can be replaced with mask ROM-incorporated  $\mu$ PD703105A, 703106A, 703106A(A), 703107A, or 703107A(A) for mass production

**APPLICATIONS**

- Office machines (such as ink jet printers, facsimiles, and PPCs)
- Multimedia systems (such as digital still cameras, DVD players, and video printers)

**The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.  
 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.**

**ORDERING INFORMATION**

Part Number	Package	Quality Grade
μPD70F3107AGJ-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Standard
μPD70F3107AF1-EN4	161-pin plastic FBGA (13 × 13)	Standard
μPD70F3107AGJ(A)-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Special

The μPD70F3107A and μPD70F3107A(A) differ in the quality grade only.

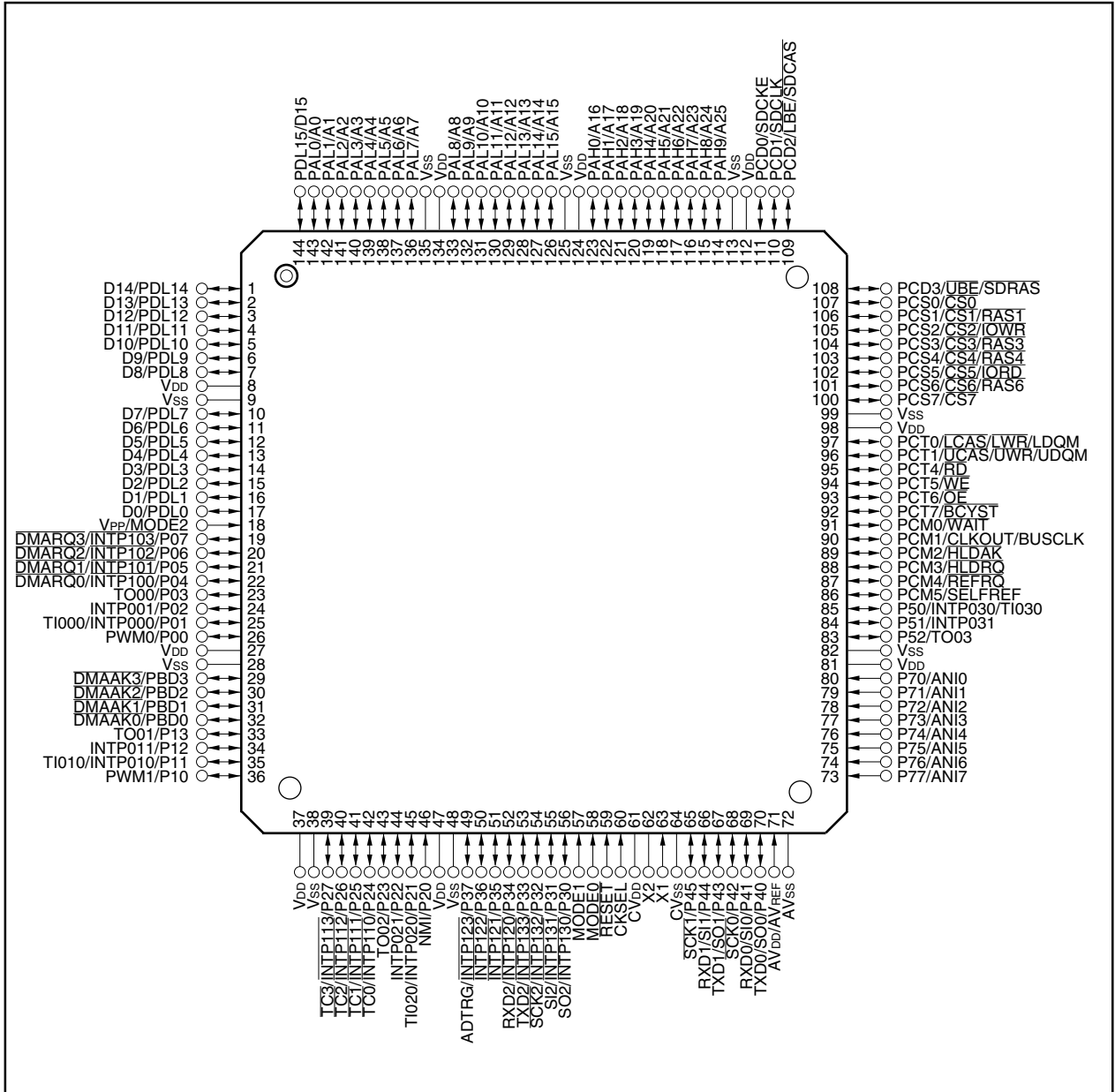
Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

PIN CONFIGURATION (TOP VIEW)

- 144-pin plastic LQFP (fine pitch) (20 × 20)

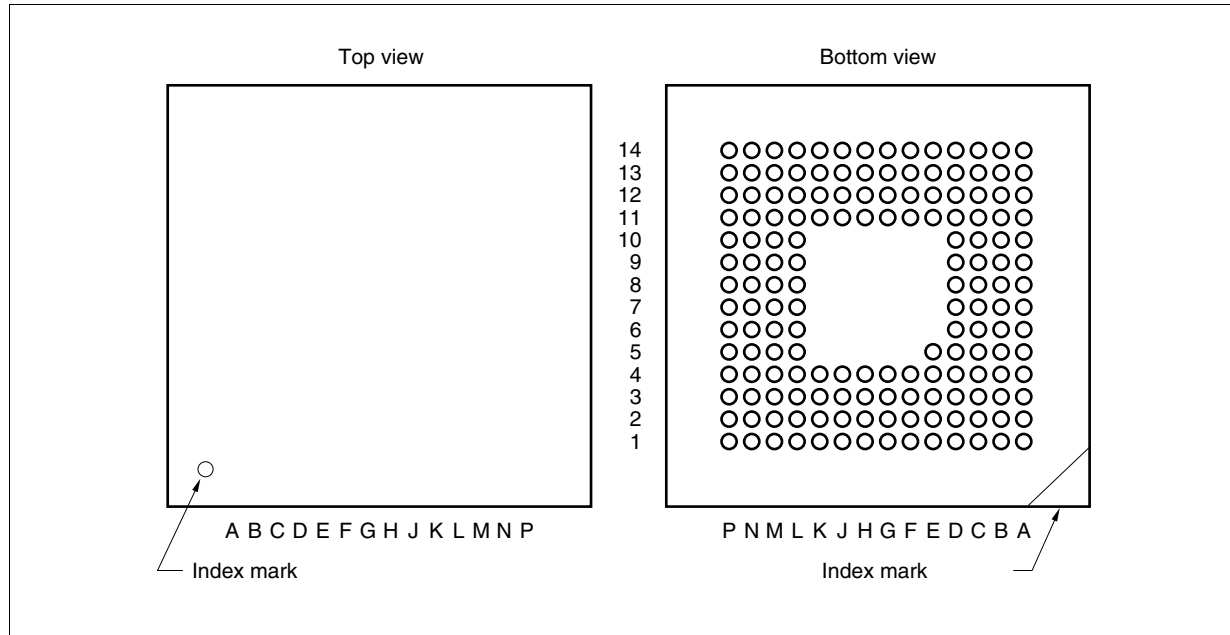
μPD70F3107AGJ-UEN

μPD70F3107AGJ(A)-UEN



• 161-pin plastic FBGA (13 × 13)

μPD70F3107AF1-EN4



(1/2)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A1	–	B10	A21/PAH5	D5	A6/PAL6
A2	D15/PDL15	B11	A25/PAH9	D6	A10/PAL10
A3	A2/PAL2	B12	SDCLK/PCD1	D7	A14/PAL14
A4	A5/PAL5	B13	CS1/RAS1/PCS1	D8	A16/PAH0
A5	–	B14	–	D9	A20/PAH4
A6	A9/PAL9	C1	–	D10	A23/PAH7
A7	A12/PAL12	C2	D9/PDL9	D11	SDCKE/PCD0
A8	A15/PAL15	C3	D13/PDL13	D12	CS0/PCS0
A9	A17/PAH1	C4	A1/PAL1	D13	CS5/IORD/PCS5
A10	–	C5	A7/PAL7	D14	–
A11	A24/PAH8	C6	V <sub>DD</sub>	E1	D5/PDL5
A12	V <sub>DD</sub>	C7	A11/PAL11	E2	D7/PDL7
A13	LBE/SDCAS/PCD2	C8	V <sub>DD</sub>	E3	D8/PDL8
A14	UBE/SDRAS/PCD3	C9	A19/PAH3	E4	D11/PDL11
B1	–	C10	A22/PAH6	E5	–
B2	D12/PDL12	C11	V <sub>SS</sub>	E11	CS6/RAS6/PCS6
B3	A0/PAL0	C12	CS3/RAS3/PCS3	E12	CS4/RAS4/PCS4
B4	A4/PAL4	C13	CS2/IOWR/PCS2	E13	CS7/PCS7
B5	V <sub>SS</sub>	C14	–	E14	V <sub>SS</sub>
B6	A8/PAL8	D1	V <sub>SS</sub>	F1	D2/PDL2
B7	A13/PAL13	D2	D10/PDL10	F2	D3/PDL3
B8	V <sub>SS</sub>	D3	D14/PDL14	F3	D4/PDL4
B9	A18/PAH2	D4	A3/PAL3	F4	V <sub>DD</sub>

(2/2)

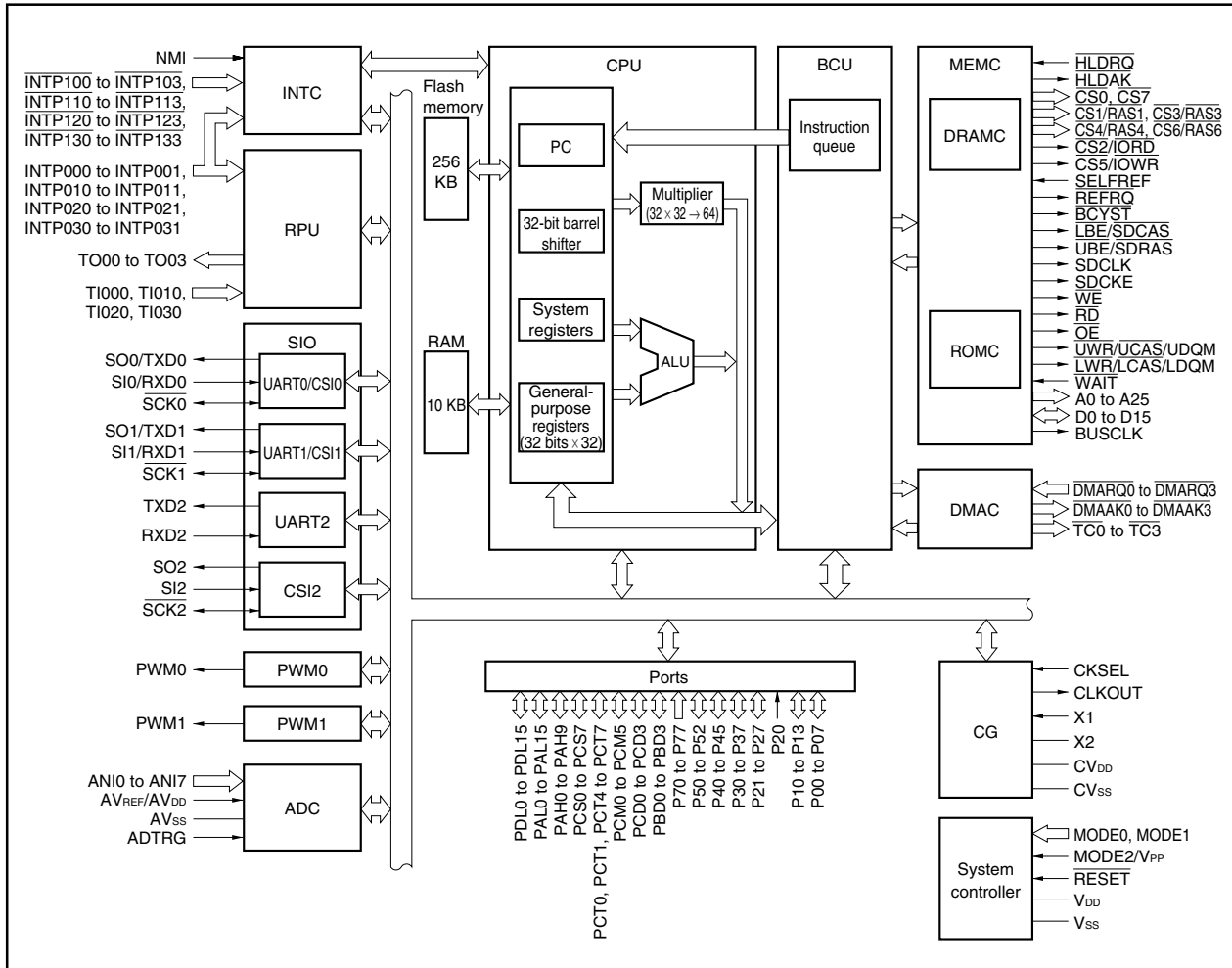
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
F11	RD/PCT4	L6	V <sub>DD</sub>	P5	–
F12	V <sub>DD</sub>	L7	INTP122/P36	P6	INTP121/P35
F13	LCAS/LWR/LDQM/PCT0	L8	SI2/INTP131/P31	P7	SCK2/INTP132/P32
F14	UCAS/UWR/UDQM/PCT1	L9	RESET	P8	MODE1
G1	V <sub>PP</sub> /MODE2	L10	TXD1/SO1/P43	P9	CV <sub>DD</sub>
G2	DMARQ3/INTP103/P07	L11	ANI7/P77	P10	X1
G3	D0/PDL0	L12	ANI4/P74	P11	–
G4	D6/PDL6	L13	ANI3/P73	P12	RXD1/SI1/P44
G11	WAIT/PCM0	L14	ANI2/P72	P13	RXD0/SI0/P41
G12	WE/PCT5	M1	–	P14	–
G13	BCYST/PCT7	M2	INTP011/P12		
G14	OE/PCT6	M3	TO01/P13		
H1	DMARQ2/INTP102/P06	M4	TC2/INTP112/P26		
H2	DMARQ1/INTP101/P05	M5	TI020/INTP020/P21		
H3	DMARQ0/INTP100/P04	M6	V <sub>SS</sub>		
H4	D1/PDL1	M7	RXD2/INTP120/P34		
H11	REFRQ/PCM4	M8	MODE0		
H12	HLDRQ/PCM3	M9	CKSEL		
H13	HLDK/PCM2	M10	SCK1/P45		
H14	CLKOUT/BUSCLK/PCM1	M11	TXD0/SO0/P40		
J1	TO00/P03	M12	ANI6/P76		
J2	TI000/INTP000/P01	M13	ANI5/P75		
J3	V <sub>DD</sub>	M14	–		
J4	INTP001/P02	N1	–		
J11	TO03/P52	N2	PWM1/P10		
J12	TI030/INTP030/P50	N3	TC3/INTP113/P27		
J13	SELFREF/PCM5	N4	TC0/INTP110/P24		
J14	INTP031/P51	N5	NMI/P20		
K1	PWM0/P00	N6	ADTRG/INTP123/P37		
K2	V <sub>SS</sub>	N7	TXD2/INTP133/P33		
K3	DMAAK1/PBD1	N8	SO2/INTP130/P30		
K4	DMAAK3/PBD3	N9	X2		
K11	ANI1/P71	N10	CV <sub>SS</sub>		
K12	ANI0/P70	N11	SCK0/P42		
K13	V <sub>SS</sub>	N12	AV <sub>DD</sub> /AV <sub>REF</sub>		
K14	V <sub>DD</sub>	N13	AV <sub>SS</sub>		
L1	–	N14	–		
L2	DMAAK2/PBD2	P1	V <sub>DD</sub>		
L3	TI010/INTP010/P11	P2	V <sub>SS</sub>		
L4	DMAAK0/PBD0	P3	TC1/INTP111/P25		
L5	TO02/P23	P4	INTP021/P22		

**Remark** Leave the A1, A5, A10, B1, B14, C1, C14, D14, E5, L1, M1, M14, N1, N14, P5, P11, and P14 pins open.

**PIN IDENTIFICATION**

A0 to A25:	Address bus	P70 to P77:	Port 7
ADTRG:	A/D trigger input	PAH0 to PAH9:	Port AH
ANI0 to ANI7:	Analog input	PAL0 to PAL15:	Port AL
AV <sub>DD</sub> :	Analog power supply	PBD0 to PBD3:	Port BD
AV <sub>REF</sub> :	Analog reference voltage	PCD0 to PCD3:	Port CD
AV <sub>SS</sub> :	Analog ground	PCM0 to PCM5:	Port CM
BCYST:	Bus cycle start timing	PCS0 to PCS7:	Port CS
BUSCLK:	Bus clock output	PCT0, PCT1,	
CKSEL:	Clock generator operating mode select	PCT4 to PCT7:	Port CT
CLKOUT:	Clock output	PDL0 to PDL15:	Port DL
CS <sub>0</sub> to CS <sub>7</sub> :	Chip select	PWM0, PWM1:	Pulse width modulation
CV <sub>DD</sub> :	Clock generator power supply	RAS <sub>1</sub> , RAS <sub>3</sub> ,	
CV <sub>SS</sub> :	Clock generator ground	RAS <sub>4</sub> , RAS <sub>6</sub> :	Row address strobe
D0 to D15:	Data bus	RD:	Read
DMAAK0 to DMAAK3:	DMA acknowledge	REFRQ:	Refresh request
DMARQ0 to DMARQ3:	DMA request	RESET:	Reset
HLD <sub>AK</sub> :	Hold acknowledge	RXD0 to RXD2:	Receive data
HLD <sub>RQ</sub> :	Hold request	SCK0 to SCK2:	Serial clock
INTP000, INTP001,		SDCAS:	SDRAM column address strobe
INTP010, INTP011,		SDCKE:	SDRAM clock enable
INTP020, INTP021,		SDCLK:	SDRAM clock output
INTP030, INTP031,		SDRAS:	SDRAM row address strobe
INTP100 to INTP103,		SELFREF:	Self-refresh request
INTP110 to INTP113,		SI0 to SI2:	Serial input
INTP120 to INTP123,		SO0 to SO2:	Serial output
INTP130 to INTP133:	Interrupt request from peripherals	TC0 to TC3:	Terminal count signal
IORD:	I/O read strobe	TI000, TI010,	
IOWR:	I/O write strobe	TI020, TI030:	Timer input
LBE:	Lower byte enable	TO00 to TO03:	Timer output
LCAS:	Lower column address strobe	TXD0 to TXD2:	Transmit data
LDQM:	Lower DQ mask enable	UBE:	Upper byte enable
LWR:	Lower write strobe	UCAS:	Upper column address strobe
MODE0 to MODE2:	Mode	UDQM:	Upper DQ mask enable
NMI:	Non-maskable interrupt request	UWR:	Upper write strobe
OE:	Output enable	V <sub>DD</sub> :	Power supply
P00 to P07:	Port 0	V <sub>PP</sub> :	Programming power supply
P10 to P13:	Port 1	V <sub>SS</sub> :	Ground
P20 to P27:	Port 2	WAIT:	Wait
P30 to P37:	Port 3	WE:	Write enable
P40 to P45:	Port 4	X1, X2:	Crystal
P50 to P52:	Port 5		

INTERNAL BLOCK DIAGRAM



**CONTENTS**

- 1. CHANGES FROM μPD70F3107 DATA SHEET (U14618E) ..... 9**
- 2. DIFFERENCES BETWEEN PRODUCTS ..... 9**
- 3. PIN FUNCTIONS..... 10**
  - 3.1 Port Pins..... 10**
  - 3.2 Non-Port Pins ..... 12**
  - 3.3 Pin I/O Circuits and Recommended Connection of Unused Pins..... 15**
- 4. ELECTRICAL SPECIFICATIONS..... 18**
  - 4.1 Normal Operation Mode ..... 18**
  - 4.2 Flash Memory Programming Mode ..... 72**
- 5. PACKAGE DRAWING ..... 75**
- 6. RECOMMENDED SOLDERING CONDITIONS..... 77**
- APPENDIX NOTES ON TARGET SYSTEM DESIGN..... 78**



**1. CHANGES FROM μPD70F3107 DATA SHEET (U14618E)**

Page	Description
Throughout	Addition of 161-pin plastic FBGA (13 × 13) package
p. 4	Addition of 161-pin plastic FBGA (13 × 13) pin configuration diagram
p. 18	Addition of storage temperature (T <sub>stg</sub> ) specification for FBGA package
p. 20	Deletion of TDK recommended oscillator constant
p. 24	Addition of PLL mode specifications (other than x10) to X1 input cycle (<1> t <sub>cyx</sub> )
pp.28, 30, 32, 34, 36	Addition of description on $\overline{UBE}$ , $\overline{LBE}$ signals in timing chart
p. 29	Relaxing of data input setup time (to address) (<39> t <sub>SAID</sub> ) and data input setup time (to $\overline{RD}$ ) (<40> t <sub>SRDID</sub> ) specifications
p. 31	Change of data output setup time (to $\overline{UWR}$ , $\overline{LWR}$ , $\overline{IOWR}$ ↑) (<56> t <sub>SODWR</sub> ) specifications
pp.37 to 41	Addition of <b>(5) SRAM, external ROM, and external I/O access timing (vis-à-vis BUSCLK signal) (when BCP bit of BCP register = 1)</b>
p. 68	Addition of SIn setup time (to $\overline{SCKn}$ ↓) (<167> t <sub>SSISK</sub> ), SIn hold time (from $\overline{SCKn}$ ↓) (<168> t <sub>HSKSI</sub> ), SOn output delay time (from $\overline{SCKn}$ ↑) (<169> t <sub>DSKSO</sub> ), and SOn output hold time (from $\overline{SCKn}$ ↓) (<170> t <sub>HSKSO</sub> ) specifications
pp.69, 70	Addition of <b>(d) Timing when CKPn, DAPn bits of CSICn register = 01, (e) Timing when CKPn, DAPn bits of CSICn register = 10, and (f) Timing when CKPn, DAPn bits of CSICn register = 11</b>
p. 71	Change of specification unit for overall error, zero-scale error, and full-scale error Addition of integral linearity error and differential linearity error specifications
p. 76	Addition of 161-pin plastic FBGA (13 × 13) package drawing
p. 77	Addition of <b>6. RECOMMENDED SOLDERING CONDITIONS</b>
p. 78	Addition of <b>APPENDIX NOTES ON TARGET SYSTEM DESIGN</b>

**2. DIFFERENCES BETWEEN PRODUCTS**

Product	ROM		RAM Size	Flash Memory Programming Pin	Package	Quality Grade		
	Type	Size						
μPD703103A	Mask ROM	None	4 KB	None	144-pin LQFP	Standard		
μPD703105A		128 KB						
μPD703106A		256 KB	10 KB		144-pin LQFP 161-pin FBGA			
μPD703107A								
μPD703106A(A)					128 KB		144-pin LQFP	Special
μPD703107A(A)					256 KB			
μPD70F3107A	Flash memory	256 KB	Provided (V <sub>PP</sub> )	144-pin LQFP	Standard			
μPD70F3107A(A)				161-pin FBGA				
				144-pin LQFP	Special			

- Cautions**
1. There are differences in noise immunity and noise radiation between the flash memory version and mask ROM version. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluation for commercial samples (not engineering samples) of the mask ROM version.
  2. When switching from the flash memory version to the mask ROM version, write the same code to the free area of the internal ROM.

3. PIN FUNCTIONS

3.1 Port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function
P00	I/O	Port 0 8-bit I/O port Input/output can be specified in 1-bit units.	PWM0
P01			TI000/INTP000
P02			INTP001
P03			TO00
P04			DMARQ0/INTP100
P05			DMARQ1/INTP101
P06			DMARQ2/INTP102
P07			DMARQ3/INTP103
P10	I/O	Port 1 4-bit I/O port Input/output can be specified in 1-bit units.	PWM1
P11			INTP010/TI010
P12			INTP011
P13			TO01
P20	Input	Port 2 P20 is an input-only port. If a valid edge is input, it operates as an NMI input. Also, the status of the NMI input is shown by bit 0 of the P2 register. P21 to P27 is a 7-bit I/O port. Input/output can be specified in 1-bit units.	NMI
P21	I/O		INTP020/TI020
P22			INTP021
P23			TO02
P24			TC0/INTP110
P25			TC1/INTP111
P26			TC2/INTP112
P27			TC3/INTP113
P30	I/O	Port 3 8-bit I/O port Input/output can be specified in 1-bit units.	SO2/INTP130
P31			SI2/INTP131
P32			SCK2/INTP132
P33			TXD2/INTP133
P34			RXD2/INTP120
P35			INTP121
P36			INTP122
P37			ADTRG/INTP123
P40	I/O	Port 4 6-bit I/O port Input/output can be specified in 1-bit units.	TXD0/SO0
P41			RXD0/SI0
P42			SCK0
P43			TXD1/SO1
P44			RXD1/SI1
P45			SCK1
P50	I/O	Port 5 3-bit I/O port Input/output can be specified in 1-bit units.	INTP030/TI030
P51			INTP031
P52			TO03

(2/2)

Pin Name	I/O	Function	Alternate Function
P70 to P77	Input	Port 7 8-bit input-only port	ANI0 to ANI7
PBD0 to PBD3	I/O	Port BD 4-bit I/O port Input/output can be specified in 1-bit units.	$\overline{\text{DMAAK0}}$ to $\overline{\text{DMAAK3}}$
PCM0	I/O	Port CM 6-bit I/O port Input/output can be specified in 1-bit units.	$\overline{\text{WAIT}}$
PCM1			$\overline{\text{CLKOUT/BUSCLK}}$
PCM2			$\overline{\text{HLDAK}}$
PCM3			$\overline{\text{HLDRQ}}$
PCM4			$\overline{\text{REFRQ}}$
PCM5			$\overline{\text{SELFREF}}$
PCT0	I/O	Port CT 6-bit I/O port Input/output can be specified in 1-bit units.	$\overline{\text{LCAS/LWR/LDQM}}$
PCT1			$\overline{\text{UCAS/UWR/UDQM}}$
PCT4			$\overline{\text{RD}}$
PCT5			$\overline{\text{WE}}$
PCT6			$\overline{\text{OE}}$
PCT7			$\overline{\text{BCYST}}$
PCS0			I/O
PCS1	$\overline{\text{CS1/RAS1}}$		
PCS2	$\overline{\text{CS2/IOWR}}$		
PCS3	$\overline{\text{CS3/RAS3}}$		
PCS4	$\overline{\text{CS4/RAS4}}$		
PCS5	$\overline{\text{CS5/IORD}}$		
PCS6	$\overline{\text{CS6/RAS6}}$		
PCS7	$\overline{\text{CS7}}$		
PCD0	I/O	Port CD 4-bit I/O port Input/output can be specified in 1-bit units.	
PCD1			$\overline{\text{SDCLK}}$
PCD2			$\overline{\text{LBE/SDCAS}}$
PCD3			$\overline{\text{UBE/SDRAS}}$
PAH0 to PAH9	I/O	Port AH 8-/10-bit I/O port Input/output can be specified in 1-bit units.	A16 to A25
PAL0 to PAL15	I/O	Port AL 8-/16-bit I/O port Input/output can be specified in 1-bit units.	A0 to A15
PDL0 to PDL15	I/O	Port DL 8-/16-bit I/O port Input/output can be specified in 1-bit units.	D0 to D15

3.2 Non-Port Pins

(1/3)

Pin Name	I/O	Function	Alternate Function
TO00	Output	Pulse signal output of timer C0 to C3	P03
TO01			P13
TO02			P23
TO03			P52
TI000	Input	External count clock input of timer C0 to C3	P01/INTP000
TI010			P11/INTP010
TI020			P21/INTP020
TI030			P50/INTP030
INTP000	Input	External maskable interrupt request input, or timer C0 external capture trigger input	P01/TI000
INTP001			P02
INTP010	Input	External maskable interrupt request input, or timer C1 external capture trigger input	P11/TI010
INTP011			P12
INTP020	Input	External maskable interrupt request input, or timer C2 external capture trigger input	P21/TI020
INTP021			P22
INTP030	Input	External maskable interrupt request input, or timer C3 external capture trigger input	P50/TI030
INTP031			P51
$\overline{\text{INTP100}}$	Input	External maskable interrupt request input	P04/ $\overline{\text{DMARQ0}}$
$\overline{\text{INTP101}}$			P05/ $\overline{\text{DMARQ1}}$
$\overline{\text{INTP102}}$			P06/ $\overline{\text{DMARQ2}}$
$\overline{\text{INTP103}}$			P07/ $\overline{\text{DMARQ3}}$
$\overline{\text{INTP110}}$			P24/ $\overline{\text{TC0}}$
$\overline{\text{INTP111}}$			P25/ $\overline{\text{TC1}}$
$\overline{\text{INTP112}}$			P26/ $\overline{\text{TC2}}$
$\overline{\text{INTP113}}$			P27/ $\overline{\text{TC3}}$
$\overline{\text{INTP120}}$			P34/RXD2
$\overline{\text{INTP121}}$			P35
$\overline{\text{INTP122}}$			P36
$\overline{\text{INTP123}}$			P37/ADTRG
$\overline{\text{INTP130}}$			P30/SO2
$\overline{\text{INTP131}}$			P31/SI2
$\overline{\text{INTP132}}$			P32/SCK2
$\overline{\text{INTP133}}$			P33/TXD2
SO0	Output	CSI0 to CSI2 serial transmission data output (3-wire)	P40/TXD0
SO1			P43/TXD1
SO2			P30/INTP130
SI0	Input	CSI0 to CSI2 serial reception data input (3-wire)	P41/RXD0
SI1			P44/RXD1
SI2			P31/INTP131

(2/3)

Pin Name	I/O	Function	Alternate Function
$\overline{\text{SCK0}}$	I/O	CSI0 to CSI2 serial clock I/O (3-wire)	P42
$\overline{\text{SCK1}}$			P45
$\overline{\text{SCK2}}$			P32/ $\overline{\text{INTP132}}$
TXD0	Output	UART0 to UART2 serial transmission data output	P40/SO0
TXD1			P43/SO1
TXD2			P33/ $\overline{\text{INTP133}}$
RXD0	Input	UART0 to UART2 serial reception data input	P41/SI0
RXD1			P44/SI1
RXD2			P34/ $\overline{\text{INTP120}}$
PWM0	Output	PWM pulse signal output	P00
PWM1			P10
ANI0 to ANI7	Input	Analog inputs to the A/D converter	P70 to P77
ADTRG	Input	A/D converter external trigger input	P37/ $\overline{\text{INTP123}}$
$\overline{\text{DMARQ0}}$	Input	DMA request signal input	P04/ $\overline{\text{INTP100}}$
$\overline{\text{DMARQ1}}$			P05/ $\overline{\text{INTP101}}$
$\overline{\text{DMARQ2}}$			P06/ $\overline{\text{INTP102}}$
$\overline{\text{DMARQ3}}$			P07/ $\overline{\text{INTP103}}$
$\overline{\text{DMAAK0}}$	Output	DMA acknowledge signal output	PBD0
$\overline{\text{DMAAK1}}$			PBD1
$\overline{\text{DMAAK2}}$			PBD2
$\overline{\text{DMAAK3}}$			PBD3
$\overline{\text{TC0}}$	Output	DMA transfer termination (terminal count) signal output	P24/ $\overline{\text{INTP110}}$
$\overline{\text{TC1}}$			P25/ $\overline{\text{INTP111}}$
$\overline{\text{TC2}}$			P26/ $\overline{\text{INTP112}}$
$\overline{\text{TC3}}$			P27/ $\overline{\text{INTP113}}$
NMI	Input	Non-maskable interrupt request signal input	P20
MODE0	Input	V850E/MA1 operating mode specification	-
MODE1			-
MODE2			V <sub>PP</sub>
V <sub>PP</sub>	Input	Flash memory programming power-supply application pin	MODE2
$\overline{\text{WAIT}}$	Input	Control signal input that inserts a wait in the bus cycle	PCM0
$\overline{\text{HLDK}}$	Output	Bus hold acknowledge output	PCM2
$\overline{\text{HLDRQ}}$	Input	Bus hold request input	PCM3
$\overline{\text{REFRQ}}$	Output	Refresh request signal output for DRAM	PCM4
SELFREF	Input	Self refresh request input for DRAM	PCM5
$\overline{\text{LCAS}}$	Output	Column address strobe signal output for DRAM lower data	PCT0/ $\overline{\text{LWR/LDQM}}$
$\overline{\text{UCAS}}$	Output	Column address strobe signal output for DRAM higher data	PCT1/ $\overline{\text{UWR/UDQM}}$
$\overline{\text{LWR}}$	Output	External data lower byte write strobe signal output	PCT0/ $\overline{\text{LCAS/LDQM}}$
$\overline{\text{UWR}}$	Output	External data higher byte write strobe signal output	PCT1/ $\overline{\text{UCAS/UDQM}}$

Pin Name	I/O	Function	Alternate Function
LDQM	Output	Output disable/write mask signal output for SDRAM lower data	PCT0/LCAS/LWR
UDQM	Output	Output disable/write mask signal output for SDRAM higher data	PCT1/UCAS/UWR
RD	Output	External data bus read strobe signal output	PCT4
WE	Output	Write enable signal output for DRAM	PCT5
OE	Output	Output enable signal output for DRAM	PCT6
BCYST	Output	Strobe signal output that shows the start of the bus cycle	PCT7
CS0	Output	Chip select signal output	PCS0
CS1			PCS1/RAS1
CS2			PCS2/IOWR
CS3			PCS3/RAS3
CS4			PCS4/RAS4
CS5			PCS5/IORD
CS6			PCS6/RAS6
CS7			PCS7
RAS1	Output	Row address strobe signal output for DRAM	PCS1/CS1
RAS3			PCS3/CS3
RAS4			PCS4/CS4
RAS6			PCS6/CS6
IOWR	Output	DMA write strobe signal output	PCS2/CS2
IORD	Output	DMA read strobe signal output	PCS5/CS5
SDCKE	Output	SDRAM clock enable signal output	PCD0
SDCLK	Output	SDRAM clock signal output	PCD1
SDCAS	Output	Column address strobe signal output for SDRAM	PCD2/LBE
SDRAS	Output	Row address strobe signal output for SDRAM	PCD3/UBE
LBE	Output	External data bus lower byte enable signal output	PCD2/SDCAS
UBE	Output	External data bus higher byte enable signal output	PCD3/SDRAS
D0 to D15	I/O	16-bit data bus for external memory	PDL0 to PDL15
A0 to A15	Output	26-bit address bus for external memory	PAL0 to PAL15
A16 to A25			PAH0 to PAH9
RESET	Input	System reset input	-
X1	Input	Connects the crystal resonator for system clock oscillation. In the case of an external source supplying the clock, it is input to X1.	-
X2	-		-
CLKOUT	Output	System clock output	PCM1/BUSCLK
BUSCLK	Output	Bus clock output	PCM1/CLKOUT
CKSEL	Input	Input which specifies the clock generator's operating mode	-
AVREF	Input	Reference voltage applied to A/D converter	AVDD
AVDD	-	Positive power supply for A/D converter	AVREF
AVSS	-	Ground potential for A/D converter	-
CVDD	-	Positive power supply for the dedicated clock generator	-
CVSS	-	Ground potential for the dedicated clock generator	-
VDD	-	Positive power supply	-
VSS	-	Ground potential	-

**3.3 Pin I/O Circuits and Recommended Connection of Unused Pins**

The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.

The I/O circuit configuration of each type is schematically shown in Figure 3-1.

It is recommended that 1 to 10 kΩ resistors be used when connecting to V<sub>DD</sub> or V<sub>SS</sub> via a resistor.

**Table 3-1. Types of Pin I/O Circuits and Recommended Connection of Unused Pins (1/2)**

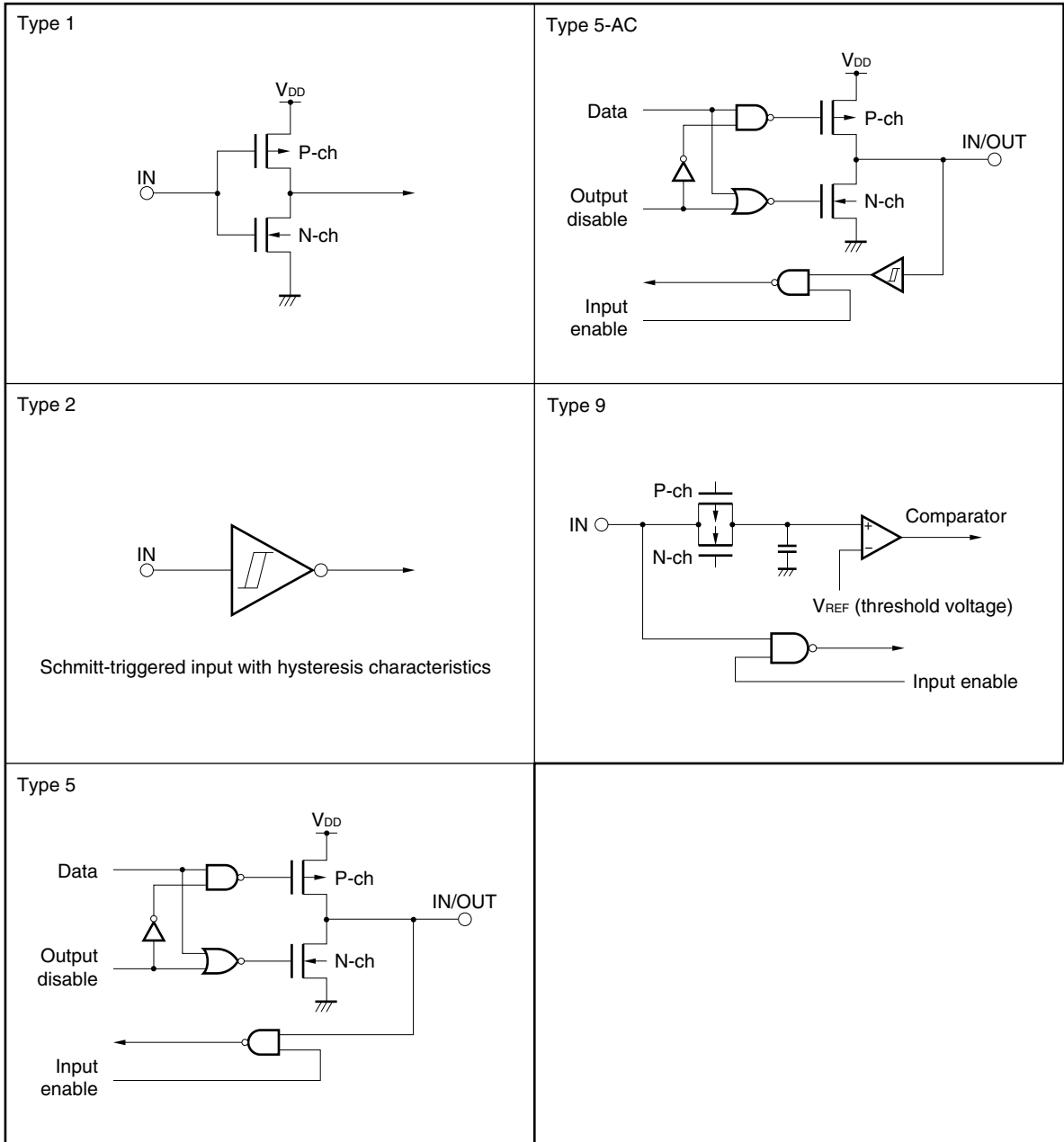
Pin Name	I/O Circuit Type	Recommended Connection
P00/PWM0	5	Input: Independently connect to V <sub>DD</sub> or V <sub>SS</sub> via a resistor. Output: Leave open.
P01/INTP000/TI000	5-AC	
P02/INTP001		
P03/TO00	5	
P04/DMARQ0/INTP100 to P07/DMARQ3/INTP103	5-AC	
P10/PWM1	5	
P11/INTP010/TI010	5-AC	
P12/INTP011		
P13/TO01	5	
P20/NMI	2	
P21/INTP020/TI020	5-AC	Input: Independently connect to V <sub>DD</sub> or V <sub>SS</sub> via a resistor. Output: Leave open.
P22/INTP021		
P23/TO02	5	
P24/TC0/INTP110 to P27/TC3/INTP113	5-AC	
P30/SO2/INTP130		
P31/SI2/INTP131		
P32/SCK2/INTP132		
P33/TXD2/INTP133		
P34/RXD2/INTP120		
P35/INTP121		
P36/INTP122		
P37/ADTRG/INTP123		
P40/TXD0/SO0		5
P41/RXD0/SI0	5-AC	
P42/SCK0		
P43/TXD1/SO1	5	
P44/RXD1/SI1	5-AC	
P45/SCK1		
P50/INTP030/TI030		
P51/INTP031	5	
P52/TO03		
P70/ANI0 to P77/ANI7	9	Connect to V <sub>SS</sub> directly.
PBD0/DMAAK0 to PBD3/DMAAK3	5	Input: Independently connect to V <sub>DD</sub> or V <sub>SS</sub> via a resistor. Output: Leave open.

Table 3-1. Types of Pin I/O Circuits and Recommended Connection of Unused Pins (2/2)

Pin Name	I/O Circuit Type	Recommended Connection
PCM0/WAIT	5	Input: Independently connect to V <sub>DD</sub> via a resistor.
PCM1/CLKOUT/BUSCLK	5	Input: Independently connect to V <sub>DD</sub> or V <sub>SS</sub> via a resistor.
PCM2/HLDAK		Output: Leave open.
PCM3/HLDRQ	5	Input: Independently connect to V <sub>DD</sub> via a resistor.
PCM4/REFRQ	5	Input: Independently connect to V <sub>DD</sub> or V <sub>SS</sub> via a resistor. Output: Leave open.
PCM5/SELFREF	5	Input: Independently connect to V <sub>SS</sub> via a resistor.
PCT0/LCAS/LWR/LDQM	5	Input: Independently connect to V <sub>DD</sub> or V <sub>SS</sub> via a resistor. Output: Leave open.
PCT1/UCAS/UWR/UDQM		
PCT4/RD		
PCT5/WE		
PCT6/OE		
PCT7/BCYST		
PCS0/CS0		
PCS1/CS1/RAS1		
PCS2/CS2/IOWR		
PCS3/CS3/RAS3		
PCS4/CS4/RAS4		
PCS5/CS5/IORD		
PCS6/CS6/RAS6		
PCS7/CS7		
PCD0/SDCKE		
PCD1/SDCLK		
PCD2/LBE/SDCAS		
PCD3/UBE/SDRAS		
PAH0/A16 to PAH9/A25		
PAL0/A0 to PAL15/A15		
PDL0/D0 to PDL15/D15		
MODE0, MODE1	2	-
MODE2/V <sub>PP</sub>		
RESET		
CKSEL	1	
AV <sub>SS</sub>	-	Connect to V <sub>SS</sub> .
AV <sub>DD</sub> /AV <sub>REF</sub>	-	Connect to V <sub>DD</sub> .



Figure 3-1. Pin I/O Circuits



4. ELECTRICAL SPECIFICATIONS

4.1 Normal Operation Mode

Absolute Maximum Ratings (T<sub>A</sub> = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V <sub>DD</sub>	V <sub>DD</sub> pin	-0.5 to +4.6	V
	CV <sub>DD</sub>	CV <sub>DD</sub> pin	-0.5 to +4.6	V
	CV <sub>SS</sub>	CV <sub>SS</sub> pin	-0.5 to +0.5	V
	AV <sub>DD</sub>	AV <sub>DD</sub> pin	-0.5 to +4.6	V
	AV <sub>SS</sub>	AV <sub>SS</sub> pin	-0.5 to +0.5	V
Input voltage	V <sub>I</sub>	X1 pin, except MODE2/V <sub>PP</sub> pin	-0.5 to +6.0	V
		MODE2/V <sub>PP</sub> pin	-0.5 to +8.5	V
Clock input voltage	V <sub>K</sub>	X1, V <sub>DD</sub> = 3.3 V ±0.3 V	-0.5 to V <sub>DD</sub> + 1.0	V
Output current, low	I <sub>OL</sub>	Per pin	4.0	mA
		Total of all pins	100	mA
Output current, high	I <sub>OH</sub>	Per pin	-4.0	mA
		Total of all pins	-100	mA
Output voltage	V <sub>O</sub>	V <sub>DD</sub> = 3.3 V ±0.3 V	-0.5 to V <sub>DD</sub> + 0.5	V
Analog input voltage	V <sub>WASN</sub>	ANI0 to ANI7, V <sub>DD</sub> = 3.3 V ±0.3 V	-0.3 to AV <sub>DD</sub> + 0.3	V
Operating ambient temperature	T <sub>A</sub>		-40 to +85	°C
Storage temperature	T <sub>stg</sub>	LQFP package	-60 to +150	°C
		FBGA package	-40 to +125	°C

- Cautions**
1. Avoid direct connections among the IC device output (or I/O) pins and between V<sub>DD</sub> or V<sub>CC</sub> and GND. However, direct connections among open-drain and open-collector pins are possible, as are direct connections to external circuits that have timing designed to prevent output conflict with pins that become high-impedance.
  2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions shown below for DC characteristics and AC characteristics are within the range for normal operation and quality assurance.

Capacitance (T<sub>A</sub> = 25°C, V<sub>DD</sub> = V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>I</sub>	f <sub>C</sub> = 1 MHz			15	pF
I/O capacitance	C <sub>IO</sub>	Unmeasured pins returned to 0 V.			15	pF
Output capacitance	C <sub>O</sub>				15	pF

**Operating Conditions**

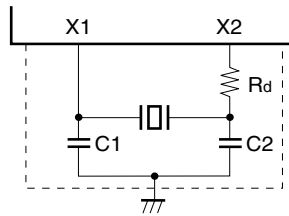
Operation Mode	Internal Operation Clock Frequency (f <sub>xx</sub> )	Operating Ambient Temperature (T <sub>A</sub> )	Power Supply Voltage (V <sub>DD</sub> )
Direct mode	4 to 25 MHz	-40 to +85°C	V <sub>DD</sub> = 3.3 V ±0.3 V
PLL mode	4 to 50 MHz	-40 to +85°C	V <sub>DD</sub> = 3.3 V ±0.3 V

**Recommended Oscillator**

**Caution** For the resonator selection and oscillator constant of the μPD70F3107A(A), customers are requested to apply to the resonator manufacturer for evaluation.

(a) Ceramic resonator

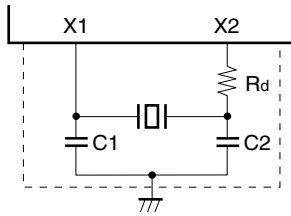
(i) Murata Mfg. Co., Ltd. (T<sub>A</sub> = -40 to +85°C)



Type	Product	Oscillation Frequency f <sub>x</sub> (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.)
			C1 (pF)	C2 (pF)	R <sub>d</sub> (kΩ)	MIN. (V)	MAX. (V)	T <sub>OST</sub> (ms)
Surface mount	CSTCC4.00MG0H6	4.0	On-chip	On-chip	0	3.0	3.6	0.09
	CSTCC5.00MG0H6	5.0	On-chip	On-chip	0	3.0	3.6	0.09
Lead	CSA4.00MG	4.0	30	30	0	3.0	3.6	0.05
	CST4.00MGW	4.0	On-chip	On-chip	0	3.0	3.6	0.05
	CSTS0400MG06	4.0	On-chip	On-chip	0	3.0	3.6	0.11
	CSA5.00MG	5.0	30	30	0	3.0	3.6	0.05
	CST5.00MGW	5.0	On-chip	On-chip	0	3.0	3.6	0.05
	CSTS0500MG06	5.0	On-chip	On-chip	0	3.0	3.6	0.11

- Cautions**
1. Connect the oscillator as closely to the X1 and X2 pins as possible.
  2. Do not wire any other signal lines in the area indicated by the broken lines.
  3. Thoroughly evaluate the matching between the μPD70F3107A and the resonator.

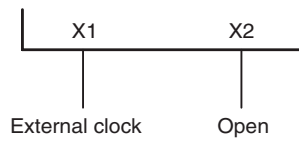
(ii) Kyocera Corporation ( $T_A = -20$  to  $+80^\circ\text{C}$ )



Type	Product	Oscillation Frequency $f_x$ (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) $T_{OST}$ (ms)
			C1 (pF)	C2 (pF)	$R_d$ (k $\Omega$ )	MIN. (V)	MAX. (V)	
Surface mount	PBRC4.00AR-A	4.0	33	33	0	3.0	3.6	0.11
	PBRC4.00BR-A	4.0	On-chip	On-chip	0	3.0	3.6	0.11
	PBRC5.00AR-A	5.0	33	33	0	3.0	3.6	0.08
	PBRC5.00BR-A	5.0	On-chip	On-chip	0	3.0	3.6	0.08
Lead	KBR-4.0MSB	4.0	33	33	0	3.0	3.6	0.11
	KBR-4.0MKC	4.0	On-chip	On-chip	0	3.0	3.6	0.11
	KBR-5.0MSB	5.0	33	33	0	3.0	3.6	0.08
	KBR-5.0MKC	5.0	On-chip	On-chip	0	3.0	3.6	0.08

- Cautions**
1. Connect the oscillator as closely to the X1 and X2 pins as possible.
  2. Do not wire any other signal lines in the area indicated by the broken lines.
  3. Thoroughly evaluate the matching between the  $\mu$ PD70F3107A and the resonator.

(b) External clock input ( $T_A = -40$  to  $+85^\circ\text{C}$ )



**DC Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 3.3 V ±0.3 V, V<sub>SS</sub> = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage, high	V <sub>IH</sub>	Except for <b>Note 1</b>	2.0		5.5	V	
		<b>Note 1</b>	0.75V <sub>DD</sub>		5.5	V	
Input voltage, low	V <sub>IL</sub>	Except for <b>Note 1</b>	-0.5		0.8	V	
		<b>Note 1</b>	-0.5		0.2V <sub>DD</sub>	V	
Clock input voltage, high	V <sub>XH</sub>	X1 pin	Direct mode	0.8V <sub>DD</sub>		V <sub>DD</sub> + 0.3	V
			PLL mode	0.8V <sub>DD</sub>		V <sub>DD</sub> + 0.3	V
Clock input voltage, low	V <sub>XL</sub>	X1 pin	Direct mode	-0.5		0.15V <sub>DD</sub>	V
			PLL mode	-0.5		0.15V <sub>DD</sub>	V
Schmitt-triggered input threshold voltage	V <sub>T</sub> <sup>+</sup>	<b>Note 1</b> , rising edge		2.0		V	
	V <sub>T</sub> <sup>-</sup>	<b>Note 1</b> , falling edge		1.0		V	
Schmitt-triggered input hysteresis width	V <sub>T</sub> <sup>+</sup> - V <sub>T</sub> <sup>-</sup>	<b>Note 1</b>	0.3			V	
Output voltage, high	V <sub>OH</sub>	I <sub>OH</sub> = -2.5 mA	0.8V <sub>DD</sub>			V	
		I <sub>OH</sub> = -100 μA	V <sub>DD</sub> - 0.4			V	
Output voltage, low	V <sub>OL</sub>	I <sub>OL</sub> = 2.5 mA			0.45	V	
Input leakage current, high	I <sub>LIH</sub>	V <sub>I</sub> = V <sub>DD</sub> , except for <b>Note 2</b>			10	μA	
Input leakage current, low	I <sub>LIL</sub>	V <sub>I</sub> = 0 V, except for <b>Note 2</b>			-10	μA	
Output leakage current, high	I <sub>LOH</sub>	V <sub>O</sub> = V <sub>DD</sub>			10	μA	
Output leakage current, low	I <sub>LOL</sub>	V <sub>O</sub> = 0 V			-10	μA	
Analog pin input leakage current	I <sub>LWASN</sub>	<b>Note 2</b>			±10	μA	
V <sub>PP</sub> supply voltage	V <sub>PP0</sub>	During normal operation	0		0.2V <sub>DD</sub>	V	
Power supply current	During normal operation	I <sub>DD1</sub>	Direct mode		3.2 × f <sub>xx</sub> + 30	4.8 × f <sub>xx</sub> + 45	mA
			PLL mode		3.2 × f <sub>xx</sub> + 30	4.8 × f <sub>xx</sub> + 45	mA
	In HALT mode	I <sub>DD2</sub>	Direct mode		1.6 × f <sub>xx</sub> + 20	2.4 × f <sub>xx</sub> + 30	mA
			PLL mode		1.6 × f <sub>xx</sub> + 20	2.4 × f <sub>xx</sub> + 30	mA
	In IDLE mode	I <sub>DD3</sub>	Direct mode		10	30	mA
			PLL mode		10	30	mA
	In STOP mode	I <sub>DD4</sub>	-40°C ≤ T <sub>A</sub> ≤ +40°C		10	60	μA
			40°C < T <sub>A</sub> ≤ 85°C			600	μA

**Notes 1.** P01/TI000/INTP000, P02/INTP001, P04/DMARQ0/INTP100 to P07/DMARQ3/INTP103, P11/TI010/INTP010, P12/INTP011, P21/TI020/INTP020, P22/INTP021, P24/TC0/INTP110 to P27/TC3/INTP113, P30/SO2/INTP130, P31/SI2/INTP131, P32/SCK2/INTP132, P33/TXD2/INTP133, P34/RXD2/INTP120, P35/INTP121, P36/INTP122, P37/ADTRG/INTP123, P41/RXD0/SI0, P42/SCK0, P44/RXD1/SI1, P45/SCK1, P50/TI030/INTP030, P51/INTP031

**2.** P70/ANI0 to P77/ANI7

**Remarks 1.** TYP. values are reference values for when T<sub>A</sub> = 25°C and V<sub>DD</sub> = 3.3 V. The current does not include the current flowing through pull-up resistors.

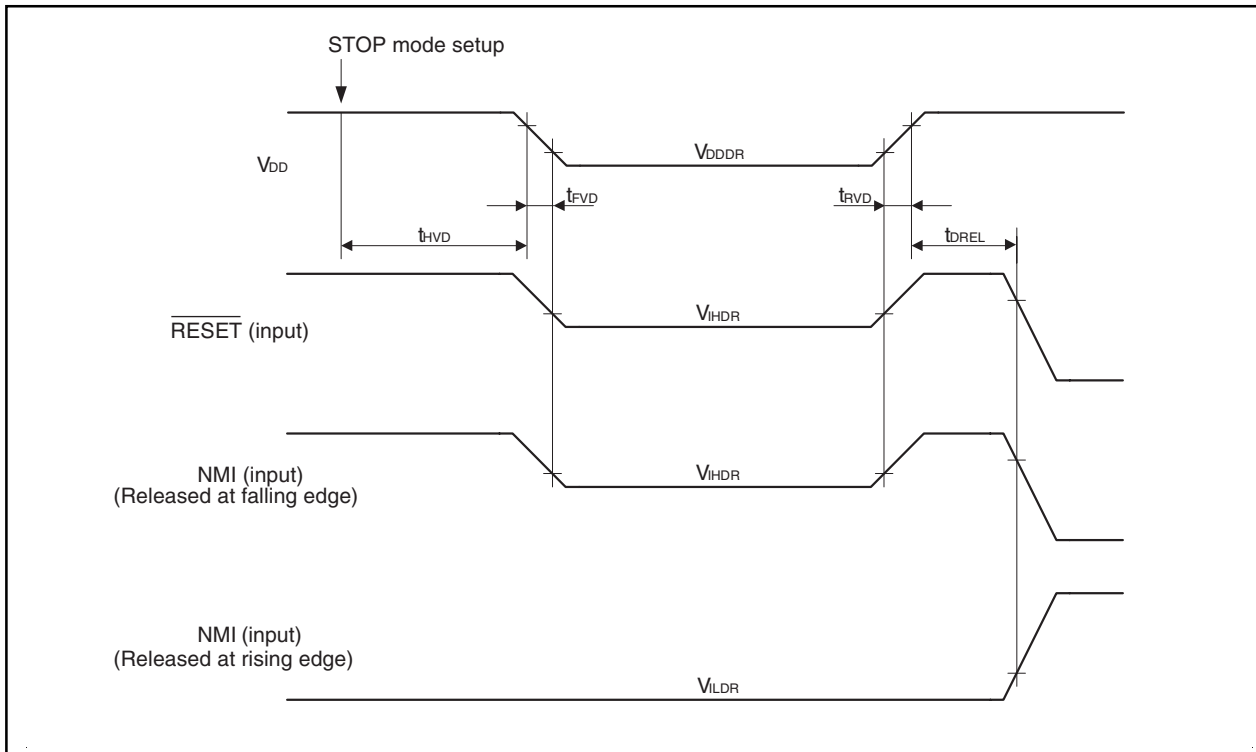
**2.** f<sub>xx</sub>: CPU operation frequency

**Data Retention Characteristics (T<sub>A</sub> = -40 to +85°C)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V <sub>DDDR</sub>	STOP mode and V <sub>DD</sub> = V <sub>DDDR</sub>	1.5		3.6	V
Data retention current	I <sub>DDDR</sub>	V <sub>DD</sub> = V <sub>DDDR</sub> -40°C ≤ T <sub>A</sub> ≤ +40°C		10	60	μA
		40°C < T <sub>A</sub> ≤ 85°C			600	μA
Power supply voltage rise time	t <sub>RV</sub>		200			μs
Power supply voltage fall time	t <sub>FV</sub>		200			μs
Power supply voltage hold time (from STOP mode setting)	t <sub>HV</sub>		0			ms
STOP release signal input time	t <sub>DREL</sub>		0			ns
Data retention high-level input voltage	V <sub>IHDR</sub>	<b>Note</b>	0.8V <sub>DDDR</sub>		V <sub>DDDR</sub>	V
Data retention low-level input voltage	V <sub>ILDR</sub>	<b>Note</b>	-0.5		0.2V <sub>DDDR</sub>	V

**Note** P01/TI000/INTP000, P02/INTP001, P04/DMARQ0/INTP100 to P07/DMARQ3/INTP103, P11/TI010/INTP010, P12/INTP011, P21/TI020/INTP020, P22/INTP021, P24/TC0/INTP110 to P27/TC3/INTP113, P30/SO2/INTP130, P31/SI2/INTP131, P32/SCK2/INTP132, P33/TXD2/INTP133, P34/RXD2/INTP120, P35/INTP121, P36/INTP122, P37/ADTRG/INTP123, P41/RXD0/SI0, P42/SCK0, P44/RXD1/SI1, P45/SCK1, P50/TI030/INTP030, P51/INTP031

**Remark** TYP. values are reference values for when T<sub>A</sub> = 25°C.

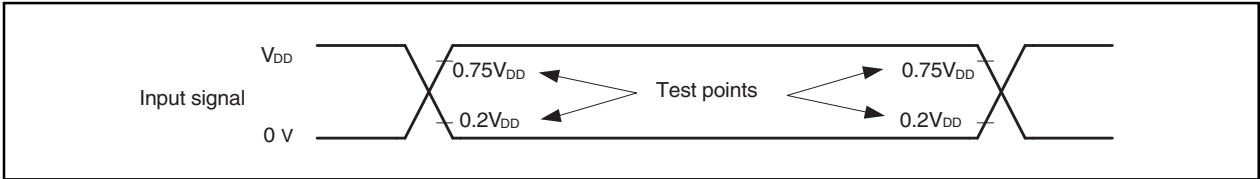


**AC Characteristics**

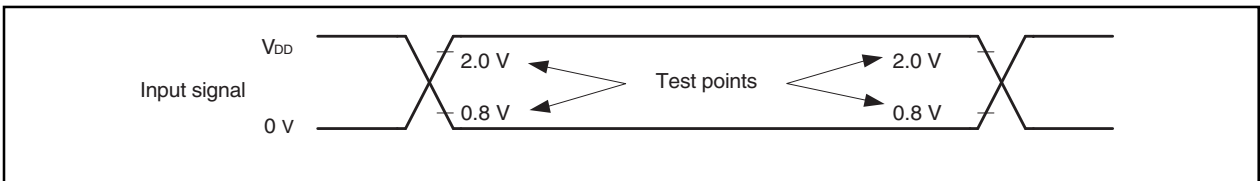
( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , output pin load capacitance:  $C_L = 50\text{ pF}$ )

**AC test input points**

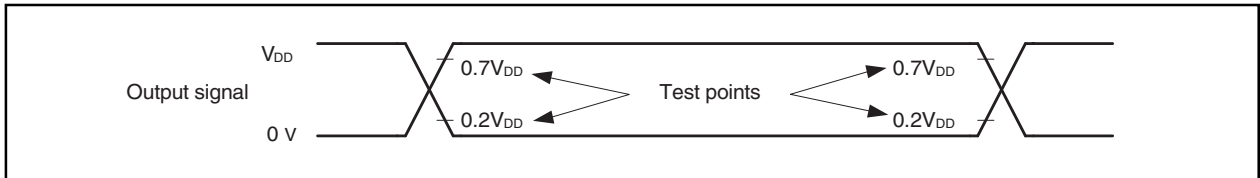
- (a) P01/TI000/INTP000, P02/INTP001, P04/DMARQ0/INTP100 to P07/DMARQ3/INTP103, P11/TI010/INTP010, P12/INTP011, P21/TI020/INTP020, P22/INTP021, P24/TC0/INTP110 to P27/TC3/INTP113, P30/SO2/INTP130, P31/SI2/INTP131, P32/SCK2/INTP132, P33/TXD2/INTP133, P34/RXD2/INTP120, P35/INTP121, P36/INTP122, P37/ADTRG/INTP123, P41/RXD0/SI0, P42/SCK0, P44/RXD1/SI1, P45/SCK1, P50/TI030/INTP030, P51/INTP031



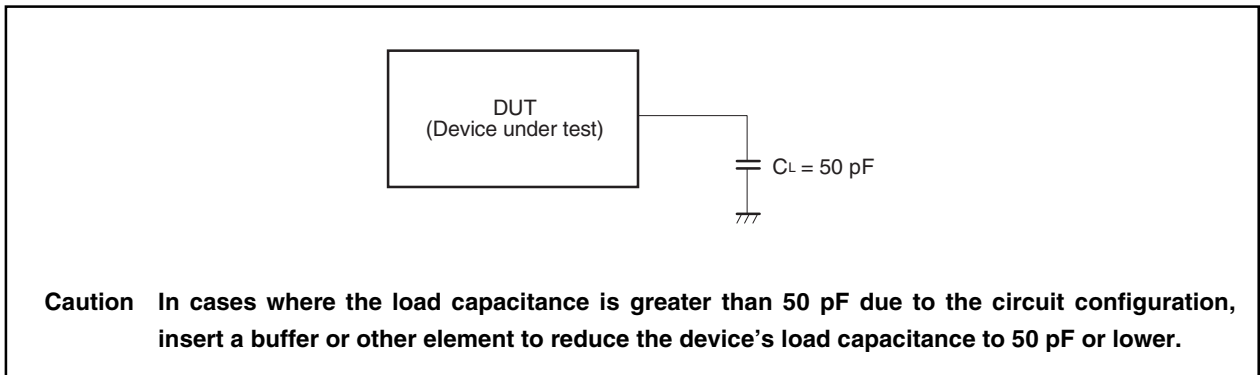
- (b) Other than (a) above



**AC test output test points**



**Load condition**



(1) Clock timing (1/2)

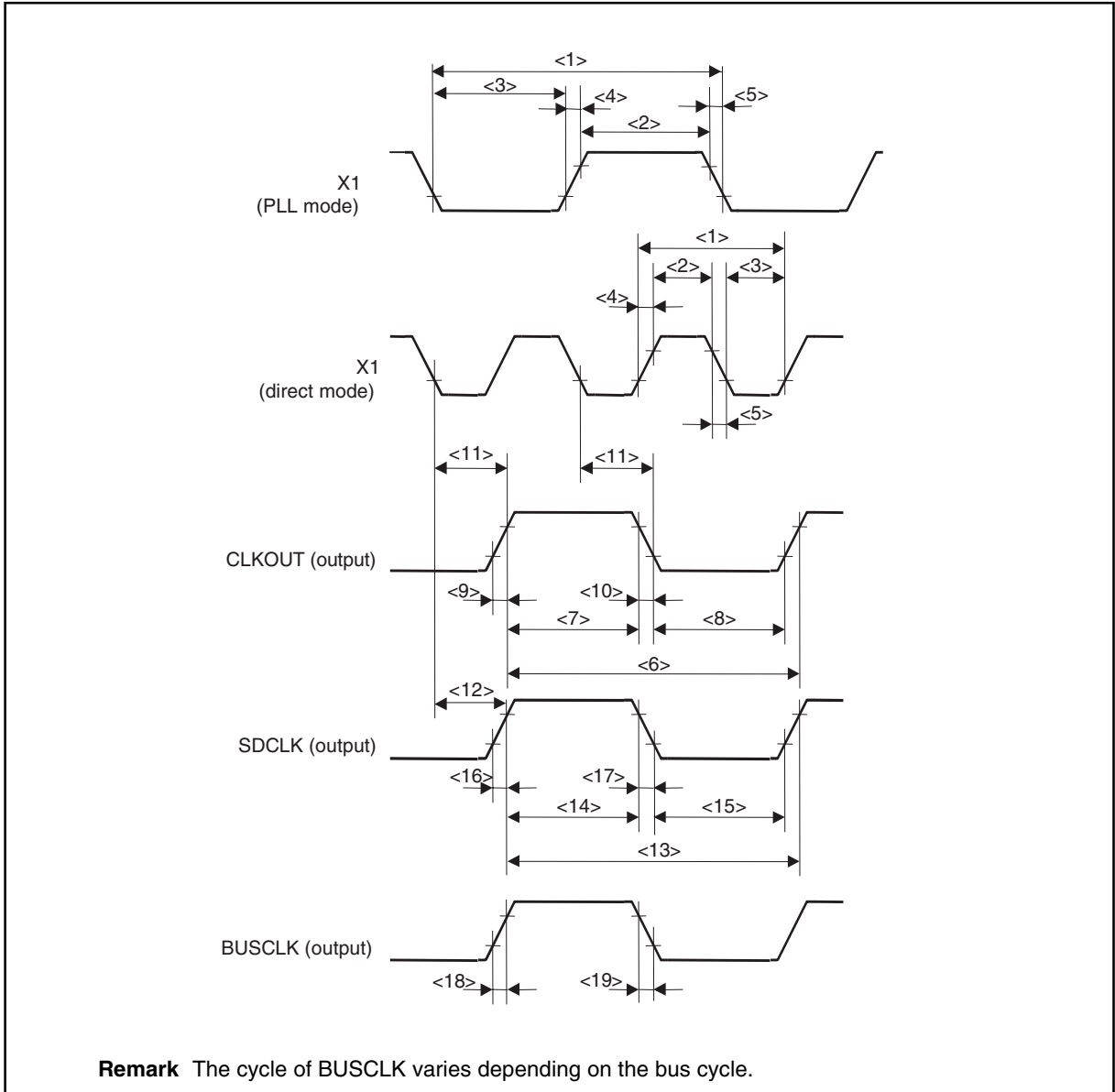
Parameter	Symbol		Conditions	MIN.	MAX.	Unit	
X1 input cycle	<1>	t <sub>cyx</sub>	Direct mode	20	125	ns	
			PLL mode	×10	200	250	ns
				Other than ×10	150	250	ns
X1 input high-level width	<2>	t <sub>wxH</sub>	Direct mode	5		ns	
			PLL mode	50		ns	
X1 input low-level width	<3>	t <sub>wxL</sub>	Direct mode	5		ns	
			PLL mode	50		ns	
X1 input rise time	<4>	t <sub>xR</sub>	Direct mode		4	ns	
			PLL mode		10	ns	
X1 input fall time	<5>	t <sub>xF</sub>	Direct mode		4	ns	
			PLL mode		10	ns	
CLKOUT output cycle	<6>	t <sub>cyK1</sub>		20	250	ns	
CLKOUT high-level width	<7>	t <sub>wKH1</sub>		0.5T – 5		ns	
CLKOUT low-level width	<8>	t <sub>wKL1</sub>		0.5T – 6		ns	
CLKOUT rise time	<9>	t <sub>KR1</sub>			5	ns	
CLKOUT fall time	<10>	t <sub>KF1</sub>			4	ns	
Delay time from X1↓ to CLKOUT	<11>	t <sub>DKX</sub>			40	ns	
Delay time from X1↓ to SDCLK	<12>	t <sub>DSX</sub>			40	ns	
SDCLK output cycle	<13>	t <sub>cyK2</sub>		20	250	ns	
SDCLK high-level width	<14>	t <sub>wKH2</sub>		0.5T – 5		ns	
SDCLK low-level width	<15>	t <sub>wKL2</sub>		0.5T – 6		ns	
SDCLK rise time	<16>	t <sub>KR2</sub>			5	ns	
SDCLK fall time	<17>	t <sub>KF2</sub>			4	ns	
BUSCLK rise time	<18>	t <sub>KR3</sub>			5	ns	
BUSCLK fall time	<19>	t <sub>KF3</sub>			4	ns	

Remarks 1. T = t<sub>cyK</sub>

2. The phase difference between CLKOUT and SDCLK, and between CLKOUT and BUSCLK cannot be defined.

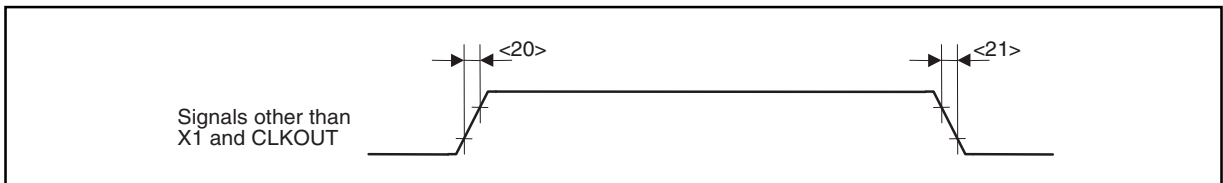


(1) Clock timing (2/2)



(2) Output waveform (other than X1 and CLKOUT)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output rise time	<20> $t_{oR}$			5	ns
Output fall time	<21> $t_{oF}$			4	ns

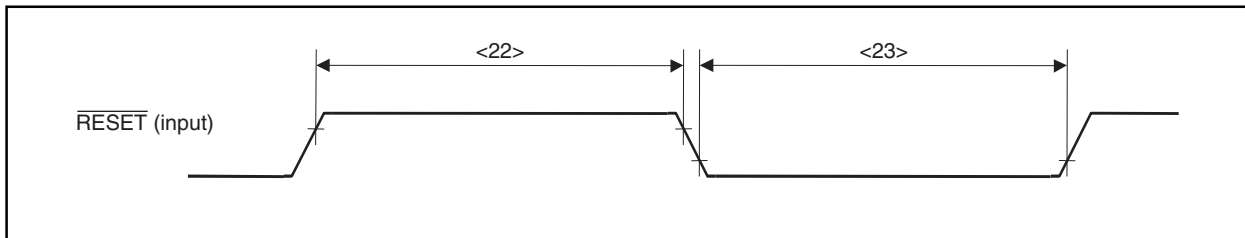


(3) Reset timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
RESET pin high-level width	<22>	t <sub>WRSH</sub>		500		ns
RESET pin low-level width	<23>	t <sub>WRSL</sub>	At power-on and at STOP mode release	500 + T <sub>OS</sub>		ns
			Other than at power-on and at STOP mode release	500		ns

**Remark** T<sub>OS</sub>: Oscillation stabilization time

**Caution** Thoroughly evaluate the oscillation stabilization time.



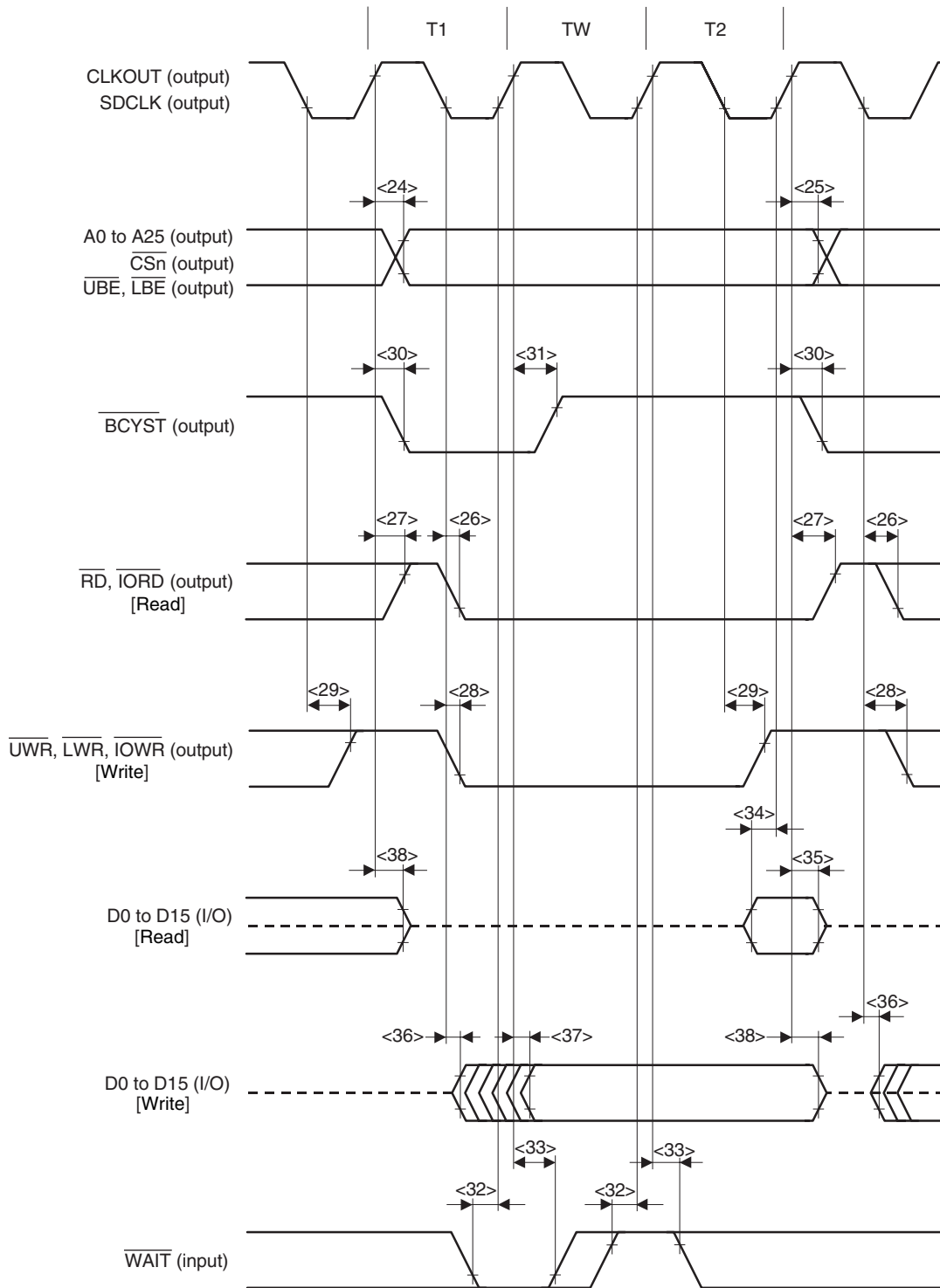
(4) SRAM, external ROM, and external I/O access timing (when BCP bit of BCP register = 0)

(a) Access timing (SRAM, external ROM, external I/O) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Address, $\overline{CS}_n$ output delay time (from CLKOUT↑)	<24> tDKA		2	13	ns
Address, $\overline{CS}_n$ output delay time (from SDCLK↑)			0	13	ns
Address, $\overline{CS}_n$ output hold time (from CLKOUT↑)	<25> tHKA		2	13	ns
Address, $\overline{CS}_n$ output hold time (from SDCLK↑)			0	13	ns
$\overline{RD}$ , $\overline{IORD}$ ↓ delay time (from CLKOUT↓)	<26> tDKRDL		2	13	ns
$\overline{RD}$ , $\overline{IORD}$ ↓ delay time (from SDCLK↓)			0	13	ns
$\overline{RD}$ , $\overline{IORD}$ ↑ delay time (from CLKOUT↑)	<27> tHKRDH		2	13	ns
$\overline{RD}$ , $\overline{IORD}$ ↑ delay time (from SDCLK↑)			0	13	ns
$\overline{UWR}$ , $\overline{LWR}$ , $\overline{IOWR}$ ↓ delay time (from CLKOUT↓)	<28> tDKWRL		2	13	ns
$\overline{UWR}$ , $\overline{LWR}$ , $\overline{IOWR}$ ↓ delay time (from SDCLK↓)			0	13	ns
$\overline{UWR}$ , $\overline{LWR}$ , $\overline{IOWR}$ ↑ delay time (from CLKOUT↓)	<29> tHKWRH		2	13	ns
$\overline{UWR}$ , $\overline{LWR}$ , $\overline{IOWR}$ ↑ delay time (from SDCLK↓)			0	13	ns
$\overline{BCYST}$ ↓ delay time (from CLKOUT↑)	<30> tDKBSL		2	13	ns
$\overline{BCYST}$ ↓ delay time (from SDCLK↑)			0	13	ns
$\overline{BCYST}$ ↑ delay time (from CLKOUT↑)	<31> tHKBSH		2	13	ns
$\overline{BCYST}$ ↑ delay time (from SDCLK↑)			0	13	ns
$\overline{WAIT}$ setup time (to CLKOUT↑)	<32> tSWK		8		ns
$\overline{WAIT}$ setup time (to SDCLK↑)			10		ns
$\overline{WAIT}$ hold time (from CLKOUT↑)	<33> tHKW		2		ns
$\overline{WAIT}$ hold time (from SDCLK↑)			2		ns
Data input setup time (to CLKOUT↑)	<34> tSKID		8		ns
Data input setup time (to SDCLK↑)			10		ns
Data input hold time (from CLKOUT↑)	<35> tHKID		2		ns
Data input hold time (from SDCLK↑)			2		ns
Data output delay time (from CLKOUT↓)	<36> tDKOD1		2	13	ns
Data output delay time (from SDCLK↓)			0	13	ns
Data output delay time (from CLKOUT↑)	<37> tDKOD2		2	13	ns
Data output delay time (from SDCLK↑)			0	13	ns
Data float delay time (from CLKOUT↑)	<38> tHKOD		2	13	ns
Data float delay time (from SDCLK↑)			0	13	ns

- Remarks**
- Maintain at least one of the data input hold times, tHRDID or tHKID.
  - n = 0 to 7

(a) Access timing (SRAM, external ROM, external I/O) (2/2)



- Remarks**
1. This is the timing when the number of waits based on the DWC0 and DWC1 registers is zero.
  2. Broken lines indicate high impedance.
  3. n = 0 to 7

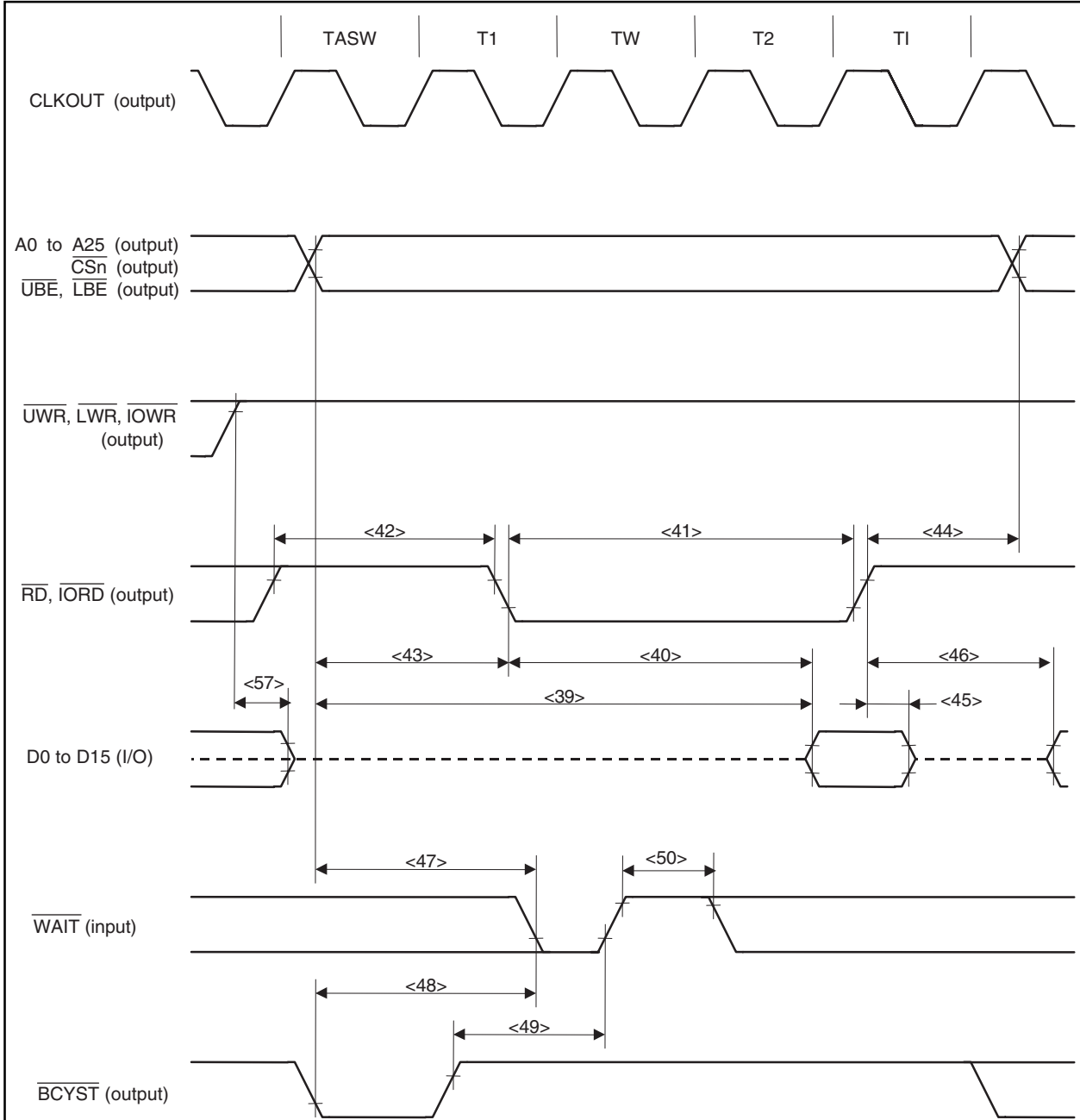
(b) Read timing (SRAM, external ROM, external I/O) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Data input setup time (from address)	<39>	t <sub>SAID</sub>		$(2 + w + w_D + w_{AS})T - 19$	ns
Data input setup time (from RD)	<40>	t <sub>SRDID</sub>		$(1.5 + w + w_D)T - 19$	ns
$\overline{RD}$ , $\overline{IORD}$ low-level width	<41>	t <sub>WRDL</sub>	$(1.5 + w + w_D)T - 10$		ns
$\overline{RD}$ , $\overline{IORD}$ high-level width	<42>	t <sub>WRDH</sub>	$(0.5 + w_{AS} + i)T - 10$		ns
Delay time from address, $\overline{CS}_n$ , to $\overline{RD}$ , $\overline{IORD}$ ↓	<43>	t <sub>DARD</sub>	$(0.5 + w_{AS})T - 10$		ns
Delay time from $\overline{RD}$ , $\overline{IORD}$ ↑ to address	<44>	t <sub>DRDA</sub>	iT		ns
Data input hold time (from $\overline{RD}$ , $\overline{IORD}$ ↑)	<45>	t <sub>HRDID</sub>	0		ns
Delay time from $\overline{RD}$ , $\overline{IORD}$ ↑ to data output	<46>	t <sub>DRDOD</sub>	$(0.5 + i)T - 10$		ns
$\overline{WAIT}$ setup time (from address)	<47>	t <sub>SAW</sub>	<b>Note</b>	$(1 + w_{AS})T - 21$	ns
$\overline{WAIT}$ setup time (from $\overline{BCYST}$ ↓)	<48>	t <sub>SBSW</sub>	<b>Note</b>	$(1 + w_{AS})T - 21$	ns
$\overline{WAIT}$ hold time (from $\overline{BCYST}$ ↑)	<49>	t <sub>HBSW</sub>	<b>Note</b>	T - 10	ns
$\overline{WAIT}$ high-level width	<50>	t <sub>WWH</sub>		T - 10	ns
Data output hold time (from $\overline{UWR}$ , $\overline{LWR}$ , $\overline{IOWR}$ ↑)	<57>	t <sub>HWROD</sub>		$(0.5 + i)T - 8$	ns

**Note** For the first  $\overline{WAIT}$  sampling when the wait count based on the DWC0 and DWC1 registers is zero.

- Remarks**
1. T = t<sub>cyk</sub>
  2. w: Wait count based on  $\overline{WAIT}$
  3. w<sub>D</sub>: Wait count based on the DWC0 and DWC1 registers
  4. Maintain at least one of the data input hold times t<sub>HRDID</sub> or t<sub>HKID</sub>
  5. n = 0 to 7
  6. i: Idle state count
  7. w<sub>AS</sub>: Address setup wait count based on the ASC register

(b) Read timing (SRAM, external ROM, external I/O) (2/2)



- Remarks**
1. This is the timing when the wait count based on the DWC0 and DWC1 registers is zero, the idle state count based on the BCC register is 1, and the wait count based on the ASC register is 1.
  2. Broken lines indicate high impedance.
  3. n = 0 to 7

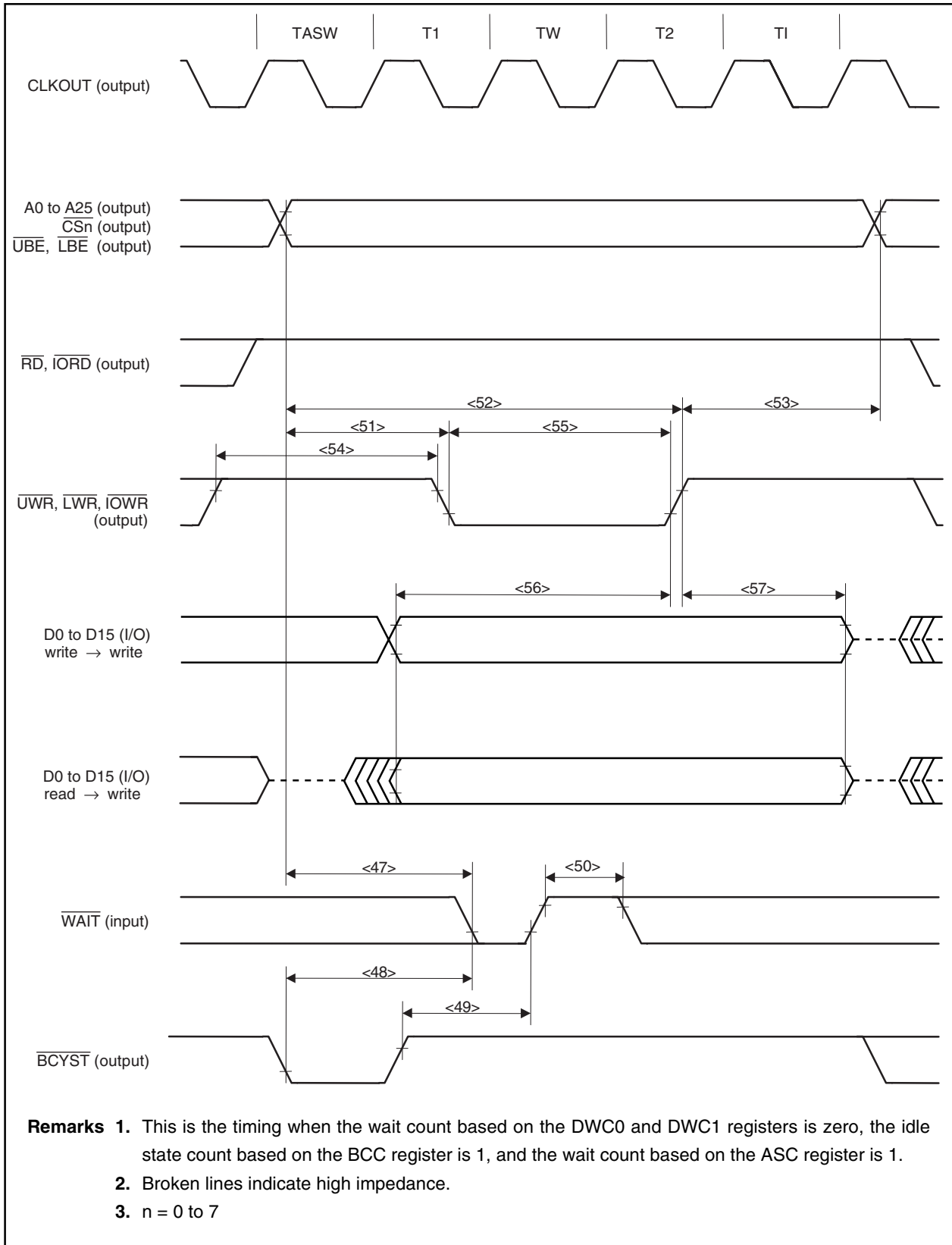
(c) Write timing (SRAM, external ROM, external I/O) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (from address)	<47> $t_{\text{SAW}}$	<b>Note</b>		$(1 + w_{\text{AS}})T - 21$	ns
$\overline{\text{WAIT}}$ setup time (from $\overline{\text{BCYST}}\downarrow$ )	<48> $t_{\text{SBSW}}$	<b>Note</b>		$(1 + w_{\text{AS}})T - 21$	ns
$\overline{\text{WAIT}}$ hold time (from $\overline{\text{BCYST}}\uparrow$ )	<49> $t_{\text{HBSW}}$	<b>Note</b>	$T - 10$		ns
$\overline{\text{WAIT}}$ high-level width	<50> $t_{\text{WWH}}$		$T - 10$		ns
Delay time from address, $\overline{\text{CS}}_n$ to $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}\downarrow$	<51> $t_{\text{DAWR}}$		$(0.5 + w_{\text{AS}})T - 10$		ns
Address setup time (to $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}\uparrow$ )	<52> $t_{\text{SAWR}}$		$(1.5 + w + w_{\text{D}} + w_{\text{AS}})T - 10$		ns
Delay time from $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}\uparrow$ to address	<53> $t_{\text{DWRA}}$		$(0.5 + i)T - 10$		ns
$\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}$ high-level width	<54> $t_{\text{WWRH}}$		$(0.5 + i + w_{\text{AS}})T - 10$		ns
$\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}$ low-level width	<55> $t_{\text{WWRL}}$		$(1 + w + w_{\text{D}})T - 10$		ns
Data output setup time (to $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}\uparrow$ )	<56> $t_{\text{SODWR}}$		$(0.5 + w + w_{\text{D}})T - 10$		ns
Data output hold time (from $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}\uparrow$ )	<57> $t_{\text{HWROD}}$		$(0.5 + i)T - 8$		ns

**Note** For the first  $\overline{\text{WAIT}}$  sampling when the wait count based on the DWC0 and DWC1 registers is zero.

- Remarks**
1.  $T = t_{\text{CYK}}$
  2.  $w$ : Wait count based on  $\overline{\text{WAIT}}$
  3.  $w_{\text{D}}$ : Wait count based on the DWC0 and DWC1 registers
  4.  $n = 0$  to 7
  5.  $i$ : Idle state count
  6.  $w_{\text{AS}}$ : Address setup wait count based on the ASC register

(c) Write timing (SRAM, external ROM, external I/O) (2/2)





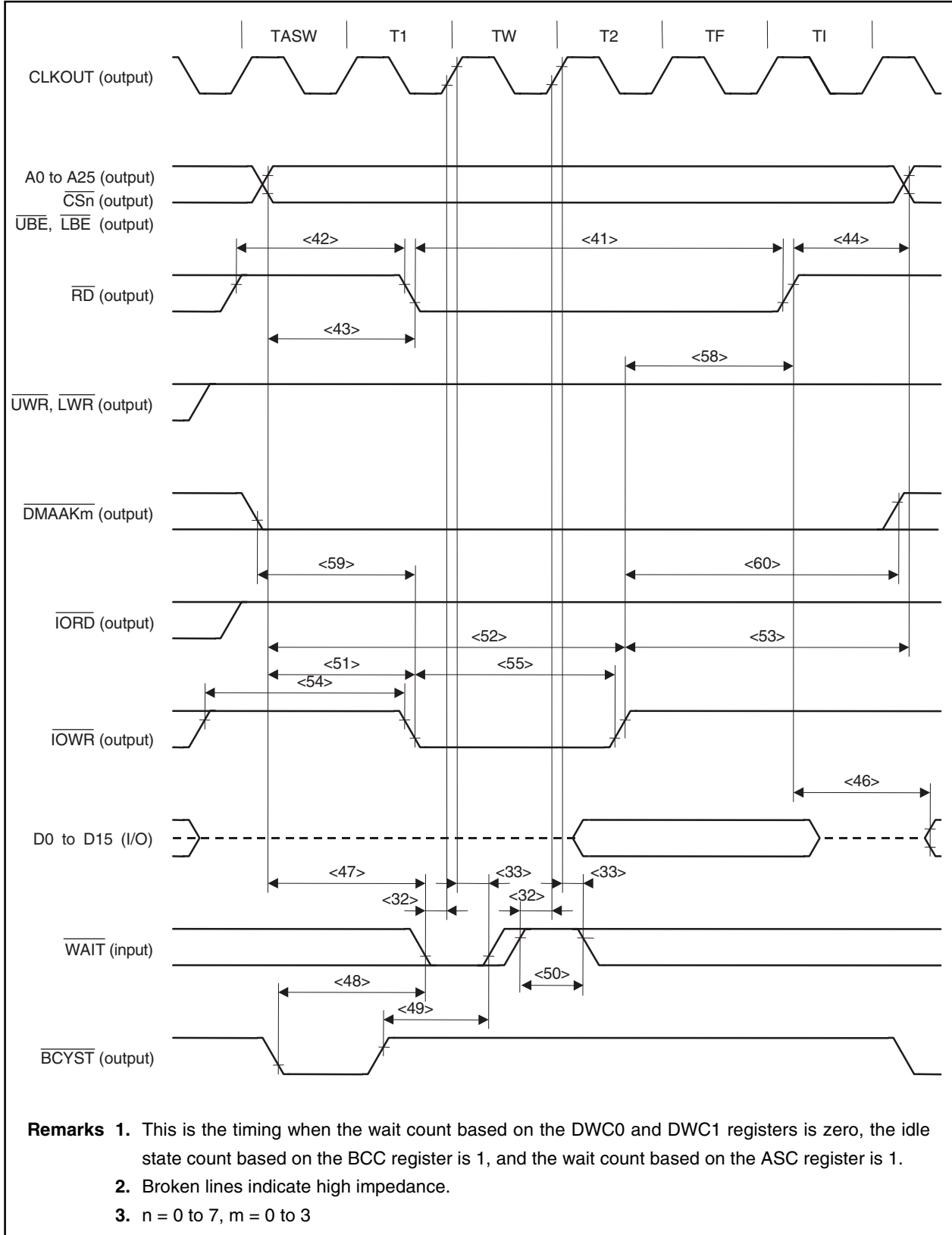
(d) DMA flyby transfer timing (SRAM → external I/O transfer) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT↑)	<32> t <sub>SWK</sub>		8		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT↑)	<33> t <sub>HKW</sub>		0		ns
$\overline{\text{RD}}$ low-level width	<41> t <sub>WRDL</sub>		$(1.5 + w + w_D)T - 10$		ns
$\overline{\text{RD}}$ high-level width	<42> t <sub>WRDH</sub>		$(0.5 + w_{AS} + i)T - 10$		ns
Delay time from address, $\overline{\text{CS}}_n$ to $\overline{\text{RD}}\downarrow$	<43> t <sub>DARD</sub>		$(0.5 + w_{AS})T - 10$		ns
Delay time from $\overline{\text{RD}}\uparrow$ to address	<44> t <sub>DRDA</sub>		iT		ns
Delay time from $\overline{\text{RD}}\uparrow$ to data output	<46> t <sub>DRDOD</sub>		$(0.5 + i)T - 10$		ns
$\overline{\text{WAIT}}$ setup time (from address)	<47> t <sub>SAW</sub>	Note		$(1 + w_{AS})T - 21$	ns
$\overline{\text{WAIT}}$ setup time (from $\overline{\text{BCYST}}\downarrow$ )	<48> t <sub>SBSW</sub>	Note		$(1 + w_{AS})T - 21$	ns
$\overline{\text{WAIT}}$ hold time (from $\overline{\text{BCYST}}\uparrow$ )	<49> t <sub>HBSW</sub>	Note	T - 10		ns
$\overline{\text{WAIT}}$ high-level width	<50> t <sub>WWH</sub>		T - 10		ns
Delay time from address to $\overline{\text{IOWR}}\downarrow$	<51> t <sub>DAWR</sub>		$(0.5 + w_{AS})T - 10$		ns
Address setup time (to $\overline{\text{IOWR}}\uparrow$ )	<52> t <sub>SAWR</sub>		$(1.5 + w + w_D + w_{AS})T - 10$		ns
Delay time from $\overline{\text{IOWR}}\uparrow$ to address	<53> t <sub>DWRA</sub>		$(1.5 + i)T - 10$		ns
$\overline{\text{IOWR}}$ high-level width	<54> t <sub>WWRH</sub>		$(0.5 + i + w_{AS})T - 10$		ns
$\overline{\text{IOWR}}$ low-level width	<55> t <sub>WWRL</sub>		$(1 + w + w_D)T - 10$		ns
Delay time from $\overline{\text{IOWR}}\uparrow$ to $\overline{\text{RD}}\uparrow$	<58> t <sub>DIWRRD</sub>		1.5T - 10		ns
Delay time from $\overline{\text{DMAAK}}_m\downarrow$ to $\overline{\text{IOWR}}\downarrow$	<59> t <sub>DDAWR</sub>		$(0.5 + w_{AS})T - 10$		ns
Delay time from $\overline{\text{IOWR}}\uparrow$ to $\overline{\text{DMAAK}}_m\uparrow$	<60> t <sub>DWRDA</sub>		$(1.5 + i)T - 10$		ns

**Note** For the first  $\overline{\text{WAIT}}$  sampling when the number of waits based on the DWC0 and DWC1 registers is zero.

- Remarks**
1. T = t<sub>cyk</sub>
  2. w: Wait count based on  $\overline{\text{WAIT}}$
  3. w<sub>D</sub>: Wait count based on the DWC0 and DWC1 registers
  4. n = 0 to 7, m = 0 to 3
  5. i: Idle state count
  6. w<sub>AS</sub>: Address setup wait count based on the ASC register

(d) DMA flyby transfer timing (SRAM → external I/O transfer) (2/2)



(e) DMA flyby transfer timing (external I/O → SRAM transfer) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT↑)	<32> $t_{\text{SWK}}$		8		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT↑)	<33> $t_{\text{HKW}}$		0		ns
$\overline{\text{IORD}}$ low-level width	<41> $t_{\text{WRDL}}$		$(2 + w + w_D)T - 10$		ns
$\overline{\text{IORD}}$ high-level width	<42> $t_{\text{WRDH}}$		$(1 + i + w_{AS})T - 10$		ns
Delay time from address, $\overline{\text{CS}}_n$ to $\overline{\text{IORD}}\downarrow$	<43> $t_{\text{DARD}}$		$(0.5 + w_{AS})T - 10$		ns
Delay time from $\overline{\text{IORD}}\uparrow$ to address	<44> $t_{\text{DRDA}}$		$(0.5 + i)T - 10$		ns
Delay time from $\overline{\text{IORD}}\uparrow$ to data output	<46> $t_{\text{DRDOD}}$		$(1 + i)T - 10$		ns
$\overline{\text{WAIT}}$ setup time (from address)	<47> $t_{\text{SAW}}$	<b>Note</b>		$(1 + w_{AS})T - 21$	ns
$\overline{\text{WAIT}}$ setup time (from $\overline{\text{BCYST}}\downarrow$ )	<48> $t_{\text{SBSW}}$	<b>Note</b>		$(1 + w_{AS})T - 21$	ns
$\overline{\text{WAIT}}$ hold time (from $\overline{\text{BCYST}}\uparrow$ )	<49> $t_{\text{HBSW}}$	<b>Note</b>	$T - 10$		ns
$\overline{\text{WAIT}}$ high-level width	<50> $t_{\text{WWH}}$		$T - 10$		ns
Delay time from address to $\overline{\text{UWR}}, \overline{\text{LWR}}\downarrow$	<51> $t_{\text{DAWR}}$		$(0.5 + w_{AS})T - 10$		ns
Address setup time (to $\overline{\text{UWR}}, \overline{\text{LWR}}\uparrow$ )	<52> $t_{\text{SAWR}}$		$(1.5 + w + w_D + w_{AS})T - 10$		ns
Delay time from $\overline{\text{UWR}}, \overline{\text{LWR}}\uparrow$ to address	<53> $t_{\text{DWRA}}$		$(0.5 + i)T - 10$		ns
$\overline{\text{UWR}}, \overline{\text{LWR}}$ high-level width	<54> $t_{\text{WWRH}}$		$(0.5 + i + w_{AS})T - 10$		ns
$\overline{\text{UWR}}, \overline{\text{LWR}}$ low-level width	<55> $t_{\text{WWRL}}$		$(1 + w + w_D)T - 10$		ns
Delay time from $\overline{\text{UWR}}, \overline{\text{LWR}}\uparrow$ to $\overline{\text{IORD}}\uparrow$	<61> $t_{\text{DWIRID}}$		$T - 10$		ns
Delay time from $\overline{\text{DMAAK}}_m\downarrow$ to $\overline{\text{IORD}}\downarrow$	<62> $t_{\text{DDARD}}$		$(0.5 + w_{AS})T - 10$		ns
Delay time from $\overline{\text{IORD}}\uparrow$ to $\overline{\text{DMAAK}}_m\uparrow$	<63> $t_{\text{DRDDA}}$		$(0.5 + i)T - 10$		ns

**Note** For first  $\overline{\text{WAIT}}$  sampling when wait count based on the  $\overline{\text{DWC}}_0$  and  $\overline{\text{DWC}}_1$  registers is zero.

**Remarks** 1.  $T = t_{\text{CYK}}$

2.  $w$ : Wait count based on  $\overline{\text{WAIT}}$

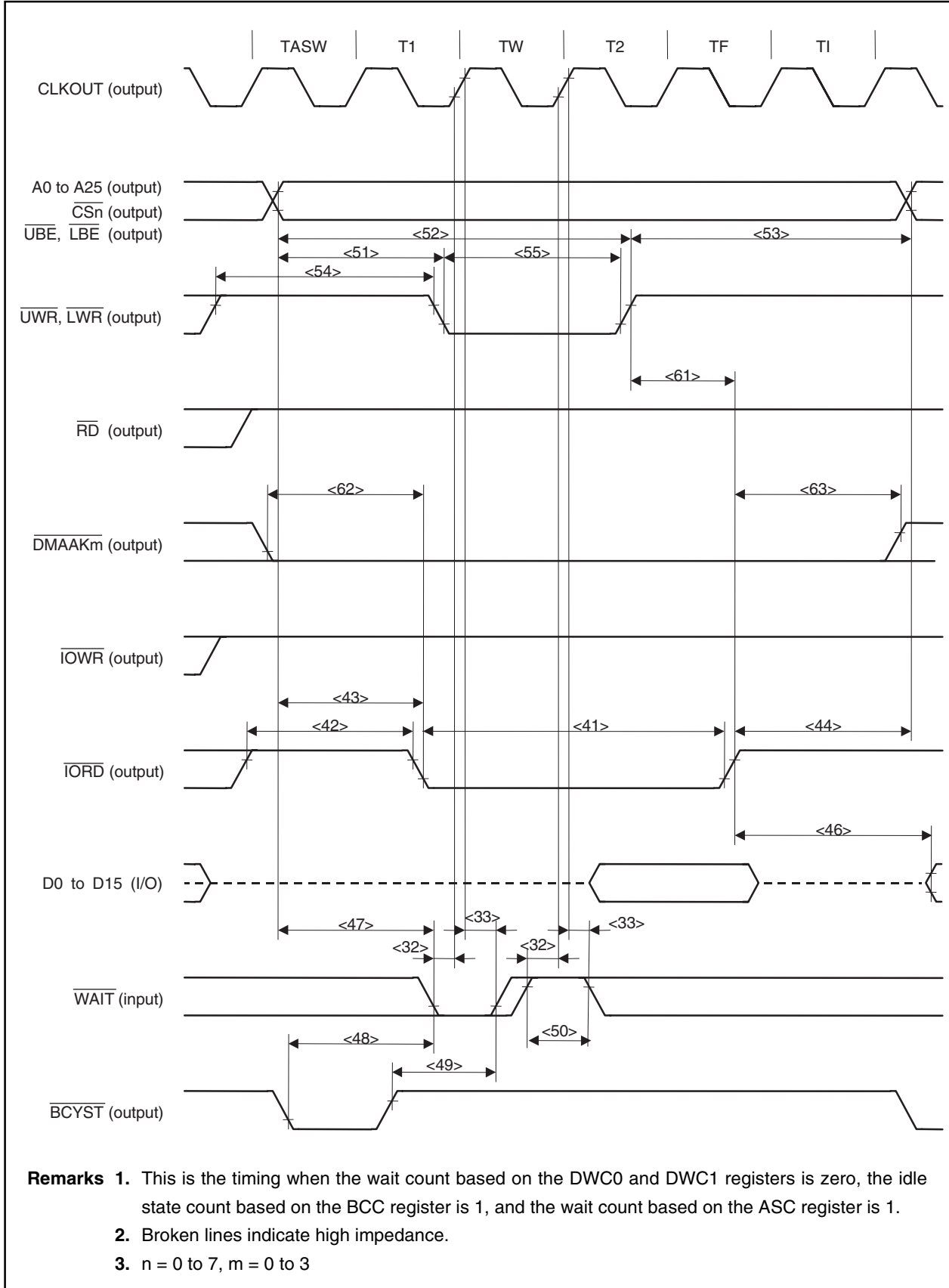
3.  $w_D$ : Wait count based on the  $\overline{\text{DWC}}_0$  and  $\overline{\text{DWC}}_1$  registers

4.  $n = 0$  to 7,  $m = 0$  to 3

5.  $i$ : Count of idle states inserted when a write cycle follows a read cycle

6.  $w_{AS}$ : Address setup wait count based on the  $\overline{\text{ASC}}$  register

(e) DMA flyby transfer timing (external I/O → SRAM transfer) (2/2)

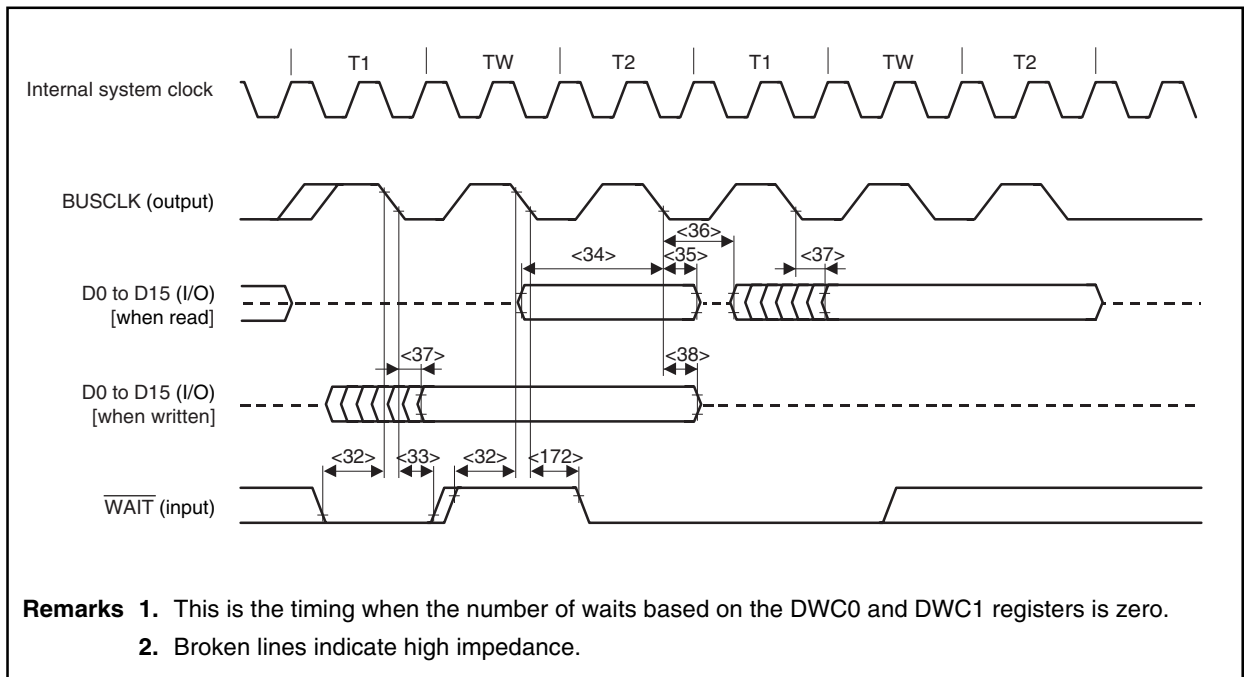


(5) SRAM, external ROM, and external I/O access timing (vis-à-vis BUSCLK signal) (when BCP bit of BCP register = 1)

(a) Access timing (SRAM, external ROM, external I/O)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
WAIT setup time (to BUSCLK ↓)	<32>	t <sub>SWK</sub>	8		ns
WAIT hold time (from BUSCLK ↓)	<33>	t <sub>HKW</sub>	0.5T - 4		ns
WAIT hold time (from BUSCLK ↓)	<172>	t <sub>HKW1</sub>	T + 2		ns
Data input setup time (to BUSCLK ↓)	<34>	t <sub>SKID</sub>	8		ns
Data input hold time (from BUSCLK ↓)	<35>	t <sub>HKID</sub>	0.5T - 4		ns
Data output delay time (from BUSCLK ↓)	<36>	t <sub>DKOD1</sub>	T - 5	T + 8	ns
Data output delay time (from BUSCLK ↓)	<37>	t <sub>DKOD2</sub>	-5	+8	ns
Data float delay time (from BUSCLK ↓)	<38>	t <sub>HKOD</sub>	0.5T - 4	0.5T + 8	ns

- Remarks**
1. Maintain at least one of the data input hold times, t<sub>HRDID</sub> or t<sub>HKID</sub>.
  2. T = Internal system clock cycle (this does not mean x2 bus cycle).



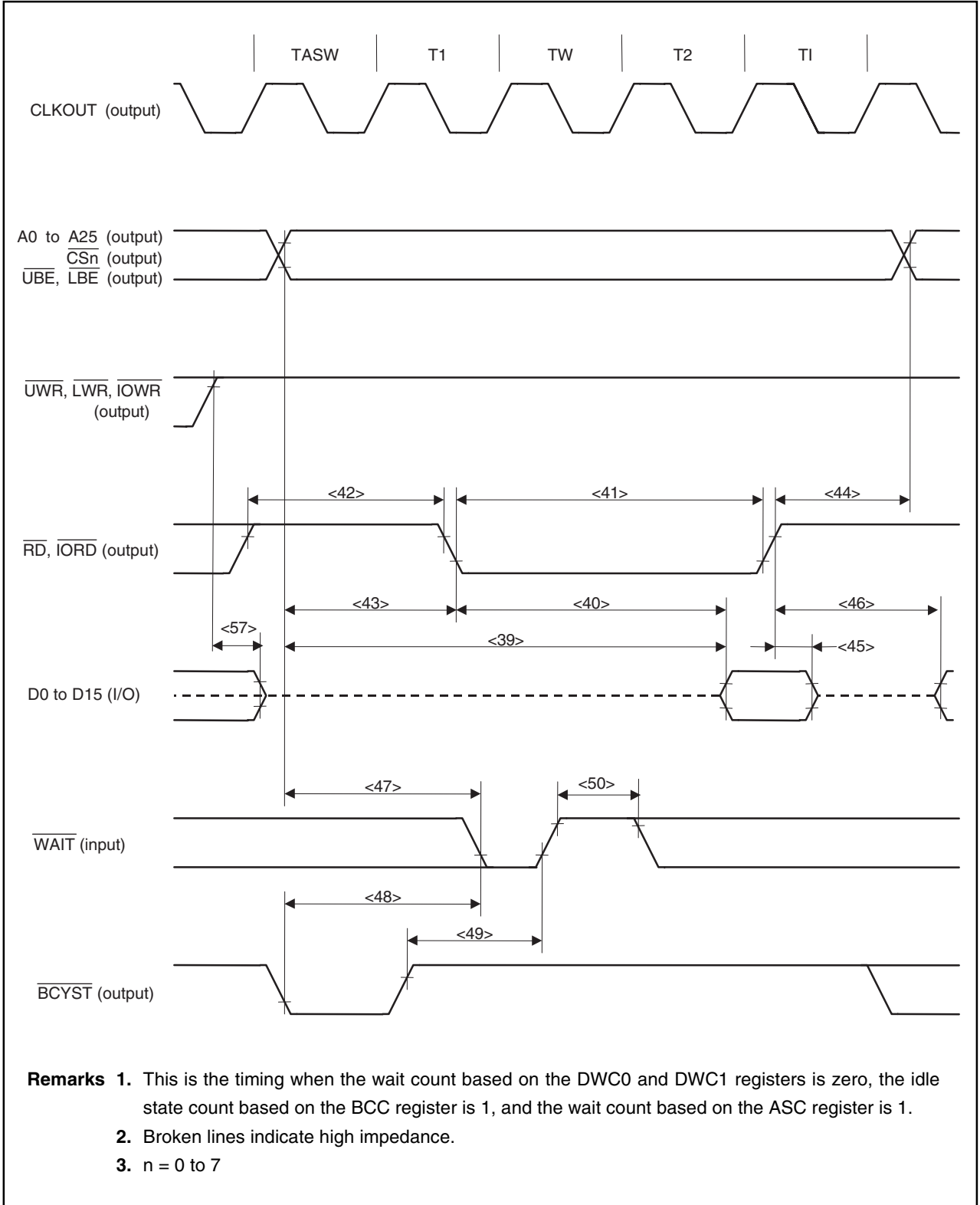
(b) Read timing (SRAM, external ROM, external I/O) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Data input setup time (to address)	<39>	t <sub>SAID</sub>		$(2 + w + w_D + w_{AS})T - 19$	ns
Data input setup time (to $\overline{RD}$ )	<40>	t <sub>SRDID</sub>		$(1.5 + w + w_D)T - 19$	ns
$\overline{RD}$ , $\overline{IORD}$ low-level width	<41>	t <sub>WRDL</sub>	$(1.25 + w + w_D)T - 10$		ns
$\overline{RD}$ , $\overline{IORD}$ high-level width	<42>	t <sub>WRDH</sub>	$(0.75 + w_{AS} + i)T - 10$		ns
Delay time from address, $\overline{CS}_n$ , to $\overline{RD}$ , $\overline{IORD}\downarrow$	<43>	t <sub>DARD</sub>	$(0.75 + w_{AS})T - 10$		ns
Delay time from $\overline{RD}$ , $\overline{IORD}\uparrow$ to address	<44>	t <sub>DRDA</sub>	iT		ns
Data input hold time (from $\overline{RD}$ , $\overline{IORD}\uparrow$ )	<45>	t <sub>HRDID</sub>	0		ns
Delay time from $\overline{RD}$ , $\overline{IORD}\uparrow$ to data output	<46>	t <sub>DRDOD</sub>	$(0.25 + i)T - 10$		ns
$\overline{WAIT}$ setup time (to address)	<47>	t <sub>SAW</sub>	<b>Note</b>	$(1 + w_{AS})T - 21$	ns
$\overline{WAIT}$ setup time (to $\overline{BCYST}\downarrow$ )	<48>	t <sub>SBSW</sub>	<b>Note</b>	$(1 + w_{AS})T - 21$	ns
$\overline{WAIT}$ hold time (from $\overline{BCYST}\uparrow$ )	<49>	t <sub>HBSW</sub>	<b>Note</b>	$0.5T - 10$	ns
$\overline{WAIT}$ high-level width	<50>	t <sub>WWH</sub>	$T - 10$		ns
Data output hold time (from $\overline{UWR}$ , $\overline{LWR}$ , $\overline{IOWR}\uparrow$ )	<57>	t <sub>HWROD</sub>	$(0.25 + i)T - 8$		ns

**Note** For the first  $\overline{WAIT}$  sampling when the wait count based on the DWC0 and DWC1 registers is zero.

- Remarks**
1. T = BUSCLK cycle (internal system clock/2)
  2. w: Wait count based on  $\overline{WAIT}$
  3. w<sub>D</sub>: Wait count based on the DWC0 and DWC1 registers
  4. Maintain at least one of the data input hold times t<sub>HRDID</sub> or t<sub>HKID</sub>
  5. n = 0 to 7
  6. i: Idle state count
  7. w<sub>AS</sub>: Address setup wait count based on the ASC register

(b) Read timing (SRAM, external ROM, external I/O) (2/2)



(c) Write timing (SRAM, external ROM, external I/O) (1/2)

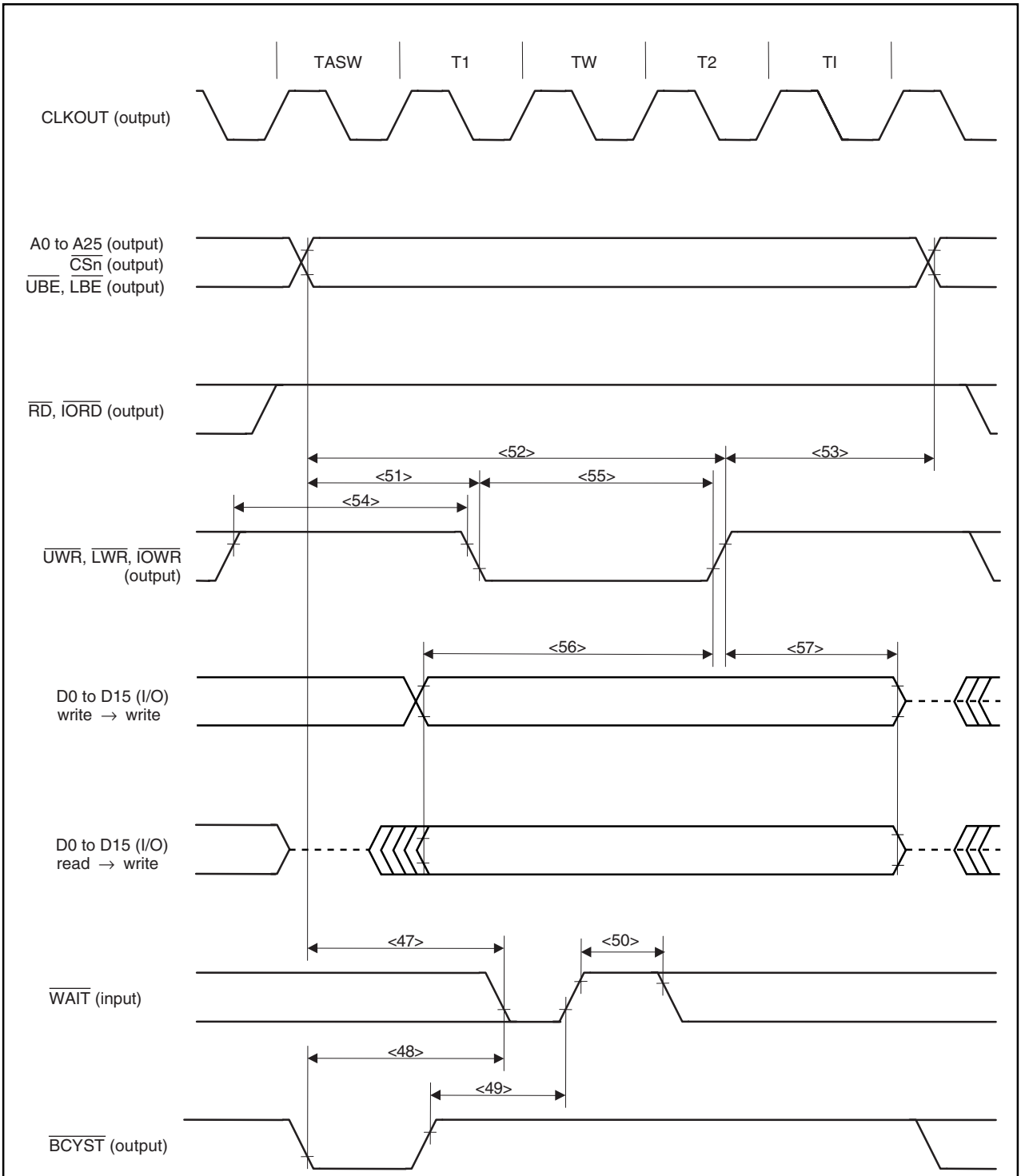
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to address)	<47> $t_{\text{SAW}}$	<b>Note</b>		$(1 + w_{\text{AS}})T - 21$	ns
$\overline{\text{WAIT}}$ setup time (to $\overline{\text{BCYST}}\downarrow$ )	<48> $t_{\text{SBSW}}$	<b>Note</b>		$(1 + w_{\text{AS}})T - 21$	ns
$\overline{\text{WAIT}}$ hold time (from $\overline{\text{BCYST}}\uparrow$ )	<49> $t_{\text{HBSW}}$	<b>Note</b>	$0.5T - 10$		ns
$\overline{\text{WAIT}}$ high-level width	<50> $t_{\text{WWH}}$		$T - 10$		ns
Delay time from address, $\overline{\text{CSn}}$ to $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}\downarrow$	<51> $t_{\text{DAWR}}$		$(0.75 + w_{\text{AS}})T - 10$		ns
Address setup time (to $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}\uparrow$ )	<52> $t_{\text{SAWR}}$		$(1.75 + w + w_{\text{D}} + w_{\text{AS}})T - 10$		ns
Delay time from $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}\uparrow$ to address	<53> $t_{\text{DWRA}}$		$(0.25 + i)T - 10$		ns
$\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}$ high-level width	<54> $t_{\text{WWRH}}$		$(1 + i + w_{\text{AS}})T - 10$		ns
$\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}$ low-level width	<55> $t_{\text{WWRL}}$		$(1 + w + w_{\text{D}})T - 10$		ns
Data output setup time (to $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}\uparrow$ )	<56> $t_{\text{SODWR}}$		$(1.25 + w + w_{\text{D}})T - 10$		ns
Data output hold time (from $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}\uparrow$ )	<57> $t_{\text{HWROD}}$		$(0.25 + i)T - 8$		ns

**Note** For the first  $\overline{\text{WAIT}}$  sampling when the wait count based on the  $\text{DWC0}$  and  $\text{DWC1}$  registers is zero.

- Remarks**
1.  $T$  = BUSCLK cycle (internal system clock/2)
  2.  $w$ : Wait count based on  $\overline{\text{WAIT}}$
  3.  $w_{\text{D}}$ : Wait count based on the  $\text{DWC0}$  and  $\text{DWC1}$  registers
  4.  $n$  = 0 to 7
  5.  $i$ : Idle state count
  6.  $w_{\text{AS}}$ : Address setup wait count based on the  $\text{ASC}$  register



(c) Write timing (SRAM, external ROM, external I/O) (2/2)



- Remarks**
1. This is the timing when the wait count based on the DWC0 and DWC1 registers is zero, the idle state count based on the BCC register is 1, and the wait count based on the ASC register is 1.
  2. Broken lines indicate high impedance.
  3. n = 0 to 7

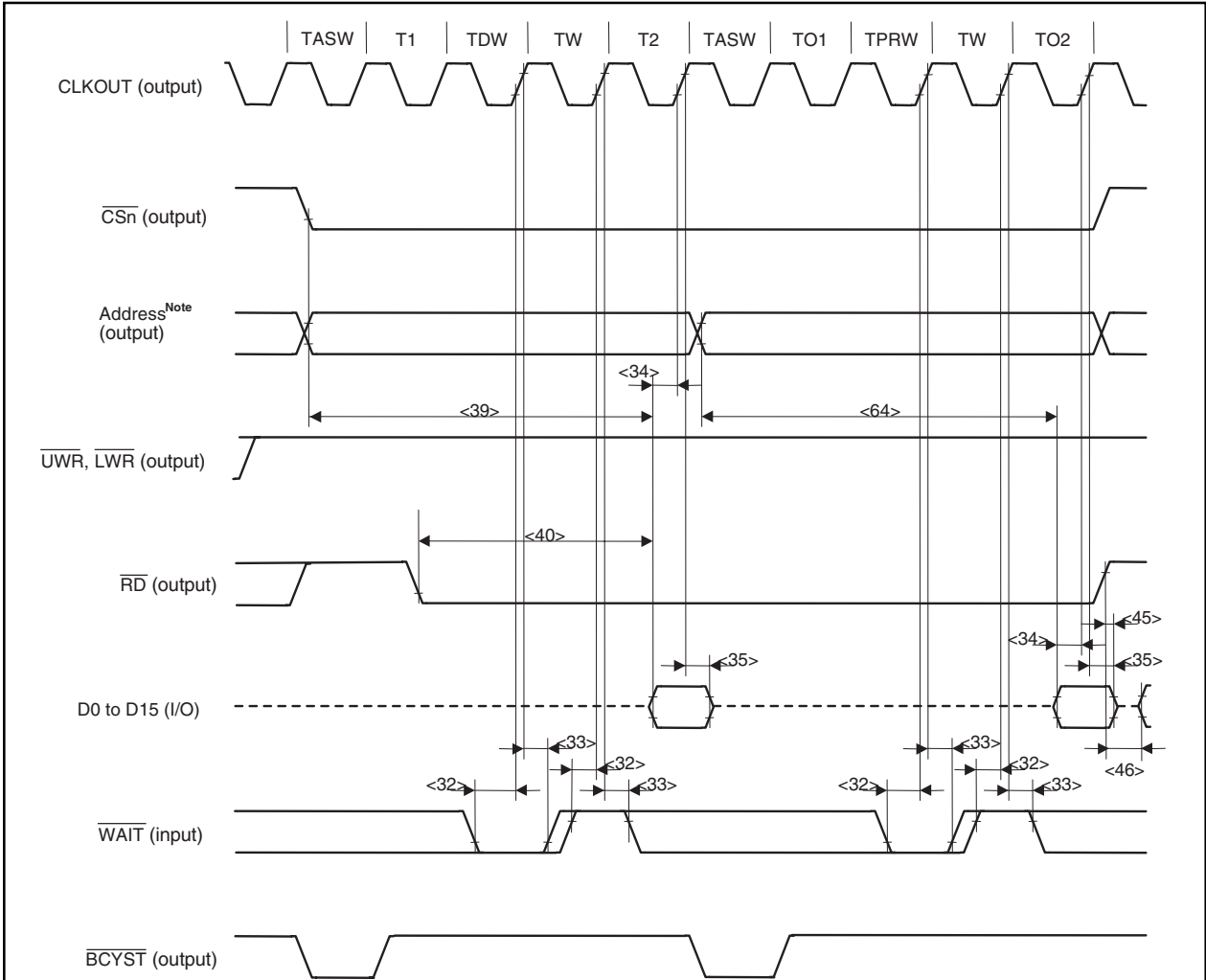
(6) Page ROM access timing

(a) 8-bit bus width (half-word/word access) and 16-bit bus width (word access) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT↑)	<32> $t_{\text{SWK}}$		8		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT↑)	<33> $t_{\text{HKW}}$		0		ns
Data input setup time (to CLKOUT↑)	<34> $t_{\text{SKID}}$		8		ns
Data input hold time (from CLKOUT↑)	<35> $t_{\text{HKID}}$		0		ns
Off-page data input setup time (to address)	<39> $t_{\text{SAID}}$			$(2 + w + w_D + w_{AS})T - 21$	ns
Off-page data input setup time (from $\overline{\text{RD}}$ )	<40> $t_{\text{SRDID}}$			$(1.5 + w + w_D)T - 21$	ns
Data input hold time (from $\overline{\text{RD}}$ ↑)	<45> $t_{\text{HRDID}}$		0		ns
Delay time from $\overline{\text{RD}}$ ↑ to data output	<46> $t_{\text{DRDOD}}$		$(0.5 + i)T - 10$		ns
On-page data input setup time (from address)	<64> $t_{\text{SOAID}}$			$(2 + w + w_{PR} + w_{AS})T - 21$	ns

- Remarks**
1.  $T = t_{\text{CYK}}$
  2.  $w$ : Wait count based on  $\overline{\text{WAIT}}$
  3.  $w_D$ : Wait count based on the DWC0 and DWC1 registers
  4.  $w_{PR}$ : Wait count based on the PRC register
  5.  $i$ : Count of idle states inserted when a write cycle follows a read cycle
  6.  $w_{AS}$ : Address setup wait count based on the ASC register
  7. Maintain at least one of the data input hold times  $t_{\text{HKID}}$  or  $t_{\text{HRDID}}$

(a) 8-bit bus width (half-word/word access) and 16-bit bus width (word access) (2/2)



**Note** On-page and off-page addresses are as follows.

PRC Register				On-Page Address	Off-Page Address
MA6	MA5	MA4	MA3		
0	0	0	0	A0 to A2	A3 to A25
0	0	0	1	A0 to A3	A4 to A25
0	0	1	1	A0 to A4	A5 to A25
0	1	1	1	A0 to A5	A6 to A25
1	1	1	1	A0 to A6	A7 to A25

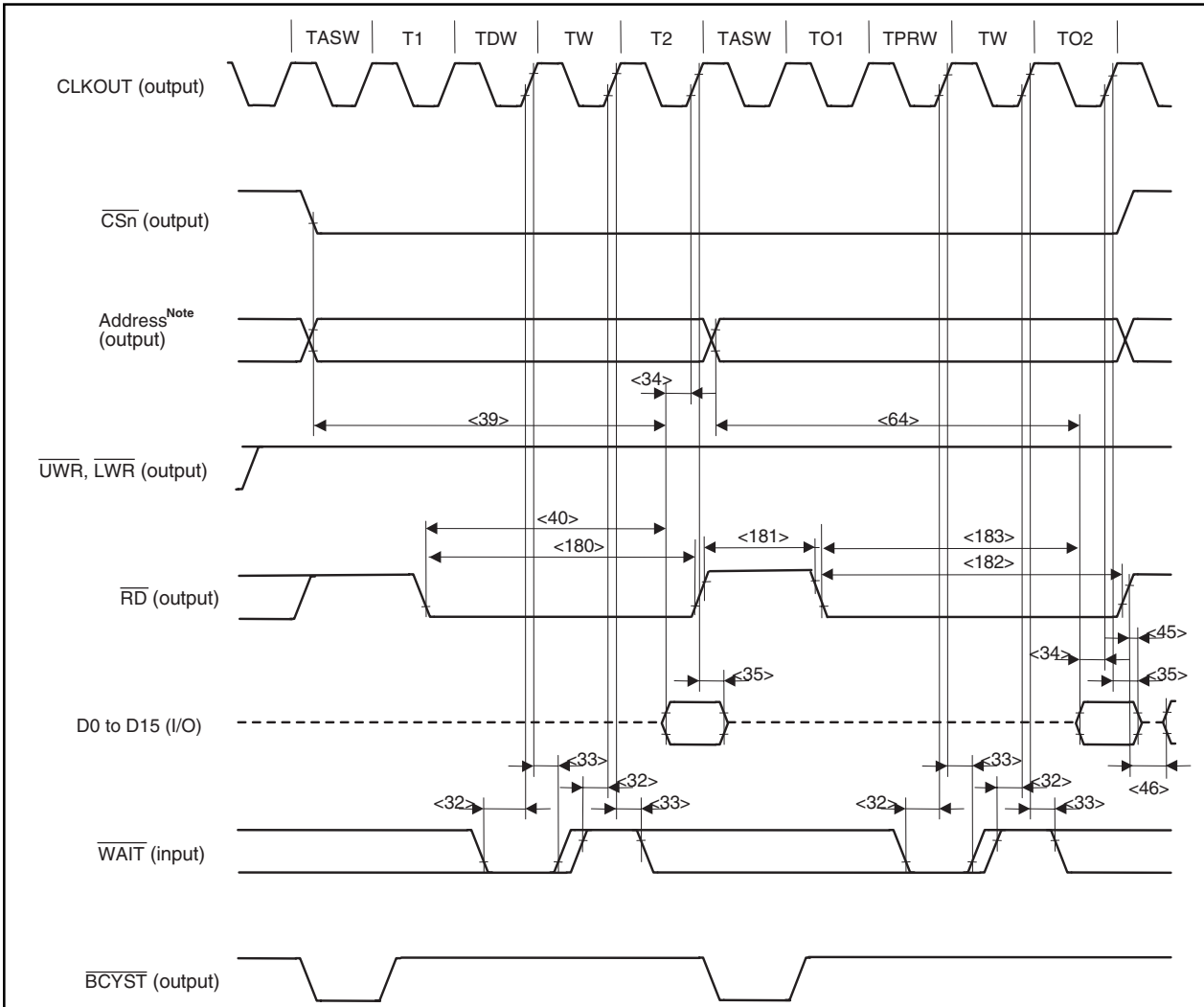
- Remarks**
- This is the timing for the following case.  
 Wait count based on the DWC0 and DWC1 registers (TDW): 1  
 Wait count based on the PRC register (TPRW): 1  
 Wait count based on the ASC register (TASW): 1
  - Broken lines indicate high impedance.
  - n = 0 to 7

(b) 8-bit bus width (byte access) and 16-bit bus width (byte/half-word access) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT↑)	<32> t <sub>SWK</sub>		8		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT↑)	<33> t <sub>HKW</sub>		0		ns
Data input setup time (to CLKOUT↑)	<34> t <sub>SKID</sub>		8		ns
Data input hold time (from CLKOUT↑)	<35> t <sub>HKID</sub>		0		ns
Off-page data input setup time (to address)	<39> t <sub>SAID</sub>			$(2 + w + w_D + w_{AS})T - 21$	ns
Off-page data input setup time (from $\overline{\text{RD}}$ )	<40> t <sub>SRDID</sub>			$(1.5 + w + w_D)T - 21$	ns
Off-page $\overline{\text{RD}}$ low-level width	<180> t <sub>WRDL</sub>		$(1.5 + w + w_D)T - 10$		ns
$\overline{\text{RD}}$ high-level width	<181> t <sub>WRDH</sub>		$(0.5 + w_{AS})T - 10$		ns
Data input hold time (from $\overline{\text{RD}}$ ↑)	<45> t <sub>HRDID</sub>		0		ns
Delay time from $\overline{\text{RD}}$ ↑ to data output	<46> t <sub>DRDOD</sub>		$(0.5 + i)T - 10$		ns
On-page $\overline{\text{RD}}$ low-level width	<182> t <sub>WORDL</sub>		$(1.5 + w + w_{PR})T - 10$		ns
On-page data input setup time (from address)	<64> t <sub>SOAID</sub>			$(2 + w + w_{PR} + w_{AS})T - 21$	ns
On-page data input setup time (from $\overline{\text{RD}}$ )	<183> t <sub>SORDID</sub>			$(1.5 + w + w_{PR})T - 21$	ns

- Remarks**
1. T = t<sub>CYK</sub>
  2. w: Wait count based on  $\overline{\text{WAIT}}$
  3. w<sub>D</sub>: Wait count based on the DWC0 and DWC1 registers
  4. w<sub>PR</sub>: Wait count based on the PRC register
  5. i: Count of idle states inserted when a write cycle follows a read cycle
  6. w<sub>AS</sub>: Address setup wait count based on the ASC register
  7. Maintain at least one of the data input hold times t<sub>HKID</sub> or t<sub>HRDID</sub>

(b) 8-bit bus width (byte access) and 16-bit bus width (byte/half-word access) (2/2)



**Note** On-page and off-page addresses are as follows.

PRC Register				On-Page Address	Off-Page Address
MA6	MA5	MA4	MA3		
0	0	0	0	A0 to A2	A3 to A25
0	0	0	1	A0 to A3	A4 to A25
0	0	1	1	A0 to A4	A5 to A25
0	1	1	1	A0 to A5	A6 to A25
1	1	1	1	A0 to A6	A7 to A25

- Remarks**
- This is the timing for the following case.  
 Wait count based on the DWC0 and DWC1 registers (TDW): 1  
 Wait count based on the PRC register (TPRW): 1  
 Wait count based on the ASC register (TASW): 1
  - Broken lines indicate high impedance.
  - n = 0 to 7

(7) DRAM access timing

(a) Read timing (EDO DRAM) (1/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Data input setup time (to CLKOUT↓)	<34> t <sub>SKID</sub>		8		ns
Data input hold time (from CLKOUT↓)	<35> t <sub>HKID</sub>		0		ns
Delay time from $\overline{OE}\uparrow$ to data output	<46> t <sub>DRDOD</sub>		$(1 + i)T - 10$		ns
Read/write cycle time	<65> t <sub>HPC</sub>		$(1 + W_{DA} + W_{CP})T - 10$		ns
Row address setup time	<66> t <sub>ASR</sub>		$0.5T - 10$		ns
Row address hold time	<67> t <sub>RAH</sub>		$(0.5 + W_{RH})T - 10$		ns
Column address setup time	<68> t <sub>ASC</sub>		$0.5T - 10$		ns
Column address hold time	<69> t <sub>CAH</sub>		$(0.5 + W_{DA})T - 10$		ns
RAS precharge time	<70> t <sub>RP</sub>	WRP = 0	T - 10		ns
		WRP ≥ 1	WRP T - 10		ns
Column address read time (to $\overline{RAS}\uparrow$ )	<71> t <sub>RAL</sub>		$(1.5 + W_{CP} + W_{DA})T - 10$		ns
$\overline{CAS}$ hold time	<72> t <sub>CSH</sub>		$(1.5 + W_{RH} + W_{DA})T - 10$		ns
Delay time from $\overline{RAS}$ to column address	<73> t <sub>RAD</sub>		$(0.5 + W_{RH})T - 10$		ns
Delay time from $\overline{RAS}$ to $\overline{CAS}$	<74> t <sub>RCD</sub>		$(1 + W_{RH})T - 10$		ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	<75> t <sub>CRP</sub>	WRP = 0	1.5T - 10		ns
		WRP ≥ 1	$(0.5 + W_{RP})T - 10$		ns
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	<76> t <sub>RHCP</sub>		$(1.5 + W_{CP} + W_{DA})T - 10$		ns
$\overline{WE}$ setup time (to $\overline{CAS}\downarrow$ )	<77> t <sub>RCS</sub>	WRP = 0	$(3 + W_{RH})T - 10$		ns
		WRP ≥ 1	$(2 + W_{RP} + W_{RH})T - 10$		ns
$\overline{WE}$ hold time (from $\overline{RAS}\uparrow$ )	<78> t <sub>RRH</sub>		$(1 + i)T - 10$		ns
$\overline{WE}$ hold time (from $\overline{CAS}\uparrow$ )	<79> t <sub>RCH</sub>		$(1.5 + i)T - 10$		ns
RAS pulse width      Off-page	<80> t <sub>RASP</sub>		$(2 + W_{RH} + W_{DA})T - 10$		ns
$\overline{CAS}$ pulse width	<81> t <sub>HCAS</sub>		$(0.5 + W_{DA})T - 10$		ns
$\overline{CAS}$ precharge time	<82> t <sub>CP</sub>		$(0.5 + W_{CP})T - 10$		ns
$\overline{CAS}$ hold time from $\overline{OE}$	Off-page	<83> t <sub>CH1</sub>	WRP = 0	$(2.5 + W_{RH} + W_{DA})T - 10$	ns
			WRP ≥ 1	$(1.5 + W_{RP} + W_{RH} + W_{DA})T - 10$	ns
	On-page	<84> t <sub>CH2</sub>		$(0.5 + W_{CP} + W_{DA})T - 10$	ns
Access time to $\overline{CAS}$ precharge	<85> t <sub>ACP</sub>			$(1.5 + W_{CP} + W_{DA})T - 21$	ns
Data input hold time (from $\overline{CAS}\downarrow$ )	<86> t <sub>DHC</sub>		0		ns
$\overline{CAS}$ access time	<87> t <sub>CAC</sub>			$(1 + W_{DA})T - 21$	ns
Access time from column address	<88> t <sub>AA</sub>			$(1.5 + W_{DA})T - 21$	ns

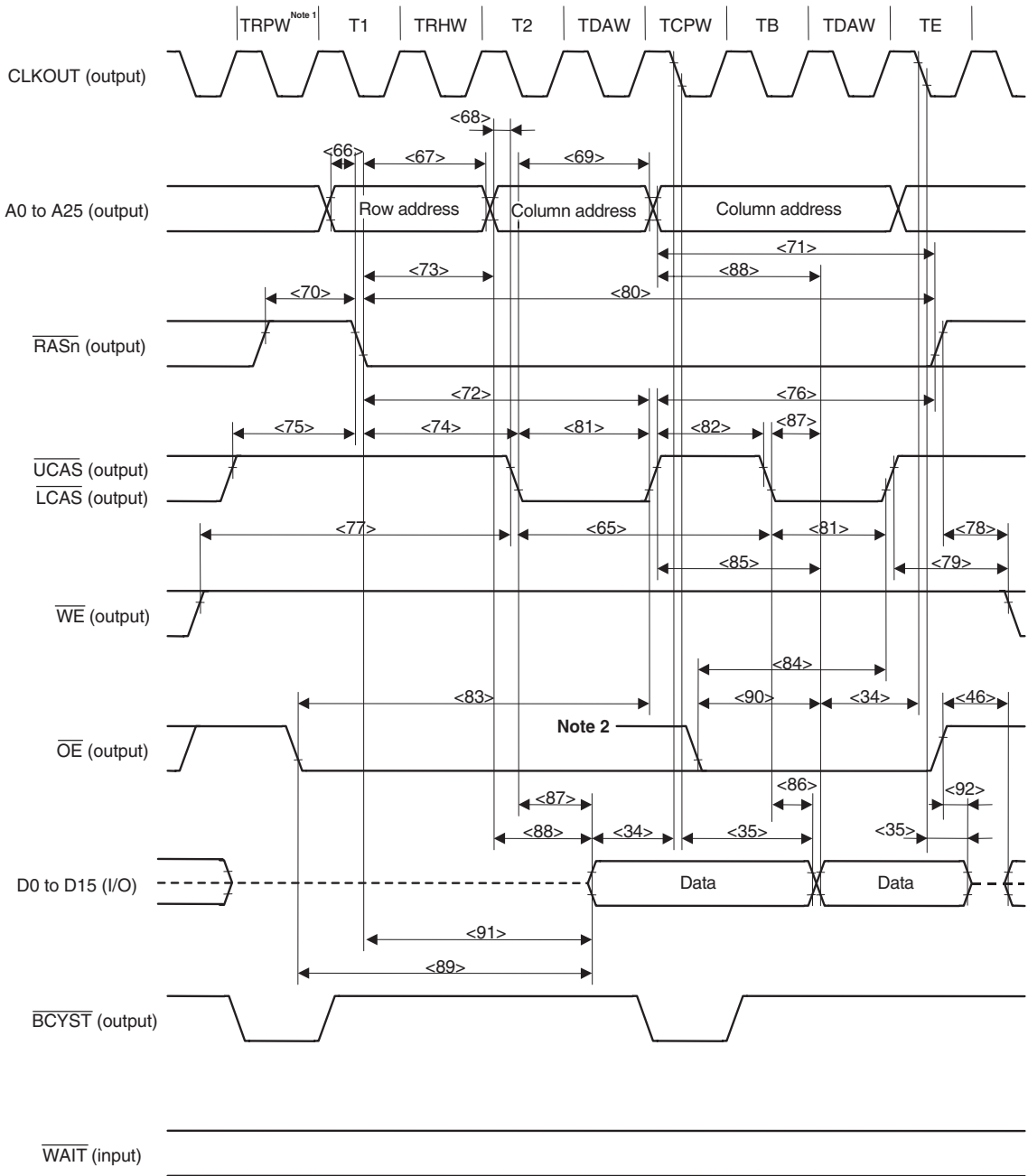
(a) Read Timing (EDO DRAM) (2/3)

Parameter		Symbol		Conditions	MIN.	MAX.	Unit
Output enable access time	Off-page	<89>	t <sub>OE1</sub>	W <sub>RP</sub> = 0		(3 + W <sub>RP</sub> + W <sub>RH</sub> + W <sub>DA</sub> )T - 21	ns
				W <sub>RP</sub> ≥ 1		(2 + W <sub>RP</sub> + W <sub>RH</sub> + W <sub>DA</sub> )T - 21	ns
	On-page	<90>	t <sub>OE2</sub>			(1 + W <sub>CP</sub> + W <sub>DA</sub> )T - 21	ns
R <sub>AS</sub> access time		<91>	t <sub>RAC</sub>			(2 + W <sub>RH</sub> + W <sub>DA</sub> ) T - 21	ns
Output buffer turn-off delay time (from $\overline{OE}$ )		<92>	t <sub>OEZ</sub>		0		ns

- Cautions**
1. At least one clock is inserted in W<sub>RP</sub> by default regardless of the setting of the RPC1n and RPC0n bits in the SCRn register (n = 1, 3, 4, or 6)
  2. The  $\overline{WAIT}$  signal cannot be controlled using the  $\overline{BCYST}$  signal when using EDO DRAM.

- Remarks**
1. T = t<sub>CYK</sub>
  2. W<sub>DA</sub>: Wait count based on the DAC1n and DAC0n bits of the SCRn register (n = 1, 3, 4, 6)
  3. W<sub>CP</sub>: Wait count based on the CPC1n and CPC0n bits of the SCRn register (n = 1, 3, 4, 6)
  4. W<sub>RP</sub>: Wait count based on the RPC1n and RPC0n bits of the SCRn register (n = 1, 3, 4, 6)
  5. W<sub>RH</sub>: Wait count based on the RHC1n and RHC0n bits of the SCRn register (n = 1, 3, 4, 6)
  6. i: Idle state count

(a) Read timing (EDO DRAM) (3/3)



- Notes**
1. At least one clock is inserted in TRPW.
  2. During on-page access from other cycles while RAS is low level.

- Remarks**
1. This is the timing for the following case.
    - Wait count based on the RPC1n and RPC0n bits of the SCRn register (TRPW): 1
    - Wait count based on the RHC1n and RHC0n bits of the SCRn register (TRHW): 1
    - Wait count based on the DAC1n and DAC0n bits of the SCRn register (TDAW): 1
    - Wait count based on the CPC1n and CPC0n bits of the SCRn register (TCPW): 1
  2. Broken lines indicate high impedance.
  3. n = 1, 3, 4, 6



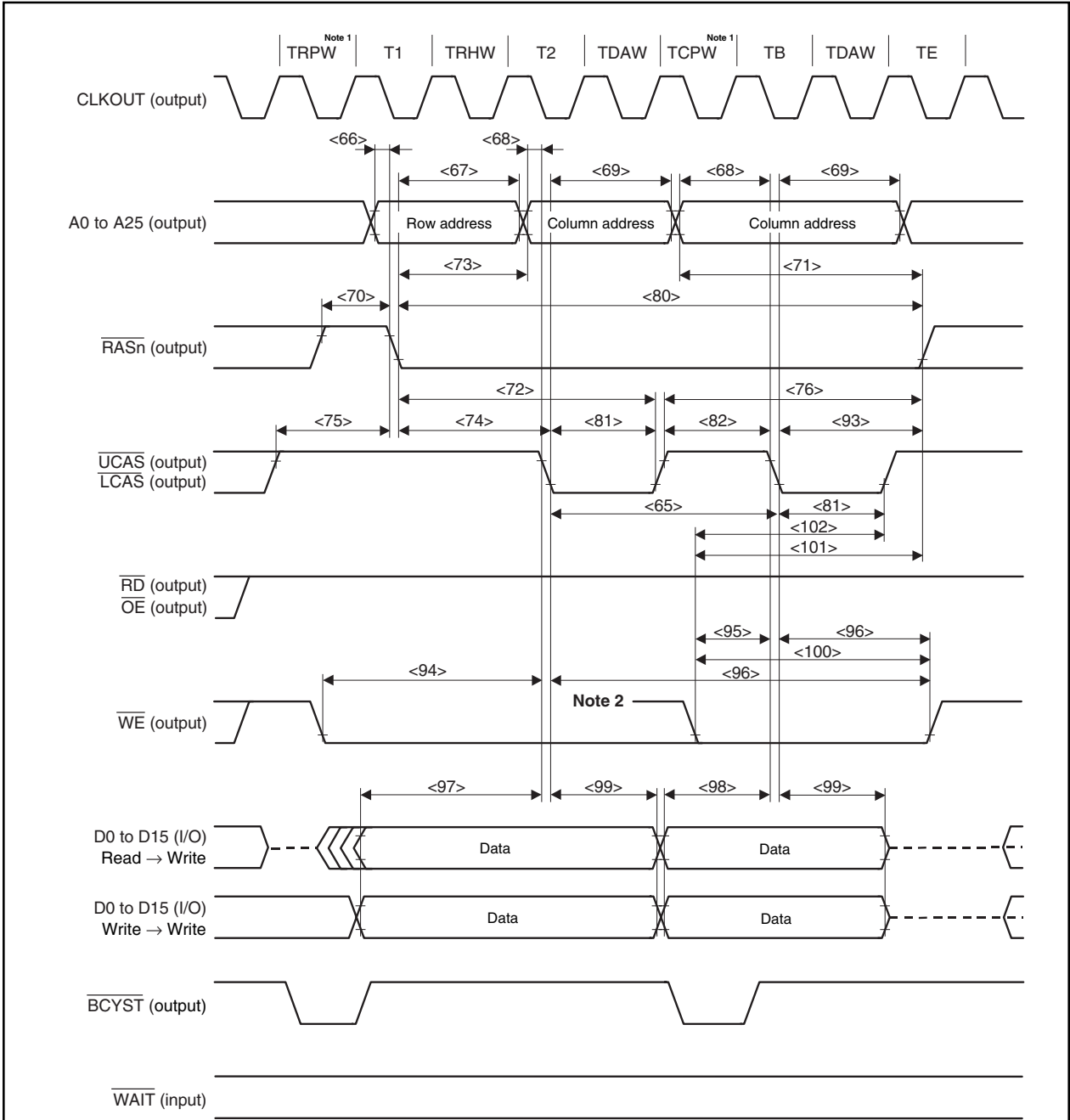
(b) Write timing (EDO DRAM) (1/2)

Parameter		Symbol	Conditions	MIN.	MAX.	Unit
Read/write cycle time		<65>	t <sub>HPC</sub>	WCP = 0	(2 + WDA)T - 10	ns
				WCP ≥ 1	(1 + WDA + WCP)T - 10	ns
Row address setup time		<66>	t <sub>ASR</sub>		0.5T - 10	ns
Row address hold time		<67>	t <sub>RAH</sub>		(0.5 + W <sub>RH</sub> )T - 10	ns
Column address setup time		<68>	t <sub>ASC</sub>		0.5T - 10	ns
Column address hold time		<69>	t <sub>CAH</sub>		(0.5 + WDA)T - 10	ns
R <sub>AS</sub> precharge time		<70>	t <sub>RP</sub>	WRP = 0	T - 10	ns
				WRP ≥ 1	W <sub>RP</sub> T - 10	ns
Column address read time (to R <sub>AS</sub> ↓)		<71>	t <sub>RAL</sub>	WCP = 0	(2.5 + WDA)T - 10	ns
				WCP ≥ 1	(1.5 + WCP + WDA)T - 10	ns
C <sub>AS</sub> hold time		<72>	t <sub>CSH</sub>		(1.5 + W <sub>RH</sub> + WDA)T - 10	ns
Delay time from R <sub>AS</sub> to column address		<73>	t <sub>RAD</sub>		(0.5 + W <sub>RH</sub> )T - 10	ns
Delay time from R <sub>AS</sub> to C <sub>AS</sub>		<74>	t <sub>RCD</sub>		(1 + W <sub>RH</sub> )T - 10	ns
C <sub>AS</sub> to R <sub>AS</sub> precharge time		<75>	t <sub>CRP</sub>	WRP = 0	1.5T - 10	ns
				WRP ≥ 1	(0.5 + W <sub>RP</sub> )T - 10	ns
R <sub>AS</sub> hold time from C <sub>AS</sub> precharge		<76>	t <sub>RHCP</sub>	WCP = 0	(2.5 + WDA)T - 10	ns
				WCP ≥ 1	(1.5 + WCP + WDA)T - 10	ns
R <sub>AS</sub> pulse width	Off-page	<80>	t <sub>RASP</sub>		(2 + W <sub>RH</sub> + WDA)T - 10	ns
C <sub>AS</sub> pulse width		<81>	t <sub>HCAS</sub>		(0.5 + WDA)T - 10	ns
C <sub>AS</sub> precharge time		<82>	t <sub>CP</sub>	WCP = 0	1.5T - 10	ns
				WCP ≥ 1	(0.5 + WCP)T - 10	ns
R <sub>AS</sub> hold time		<93>	t <sub>RSH</sub>		(1 + WDA)T - 10	ns
W <sub>E</sub> setup time (to C <sub>AS</sub> ↓)	Off-page	<94>	t <sub>WCS1</sub>	WRP = 0	(2 + W <sub>RH</sub> )T - 10	ns
				WRP ≥ 1	(1 + W <sub>RP</sub> + W <sub>RH</sub> )T - 10	ns
	On-page	<95>	t <sub>WCS2</sub>	WCP = 0	T - 10	ns
				WCP ≥ 1	W <sub>CP</sub> T - 10	ns
W <sub>E</sub> hold time (from C <sub>AS</sub> ↓)		<96>	t <sub>WCH</sub>		(1 + WDA)T - 10	ns
Data setup time (to C <sub>AS</sub> ↓)	Off-page	<97>	t <sub>DS1</sub>		(1.5 + W <sub>RH</sub> )T - 10	ns
	On-page	<98>	t <sub>DS2</sub>	WCP = 0	1.5T - 10	ns
WCP ≥ 1				(0.5 + WCP)T - 10	ns	
Data hold time (from C <sub>AS</sub> ↓)		<99>	t <sub>DH</sub>		(0.5 + WDA)T - 10	ns
W <sub>E</sub> pulse width	On-page	<100>	t <sub>WP</sub>	WCP = 0	(2 + WDA)T - 10	ns
				WCP ≥ 1	(1 + WDA + WCP)T - 10	ns
W <sub>E</sub> read time (to R <sub>AS</sub> ↑)	On-page	<101>	t <sub>RWL</sub>	WCP = 0	(2 + WDA)T - 10	ns
				WCP ≥ 1	(1 + WDA + WCP)T - 10	ns
W <sub>E</sub> read time (to C <sub>AS</sub> ↑)	On-page	<102>	t <sub>CWL</sub>	WCP = 0	(1.5 + WDA)T - 10	ns
				WCP ≥ 1	(0.5 + WDA + WCP)T - 10	ns

- Cautions**
1. At least one clock is inserted in  $w_{RP}$  by default regardless of the setting of the  $RPC1n$  and  $RPC0n$  bits in the  $SCRn$  register ( $n = 1, 3, 4, 6$ ).
  2. At least one clock is inserted in  $w_{CP}$  by default regardless of the setting of the  $CPC1n$  and  $CPC0n$  bits in the  $SCRn$  register ( $n = 1, 3, 4, 6$ ).
  3. The  $\overline{WAIT}$  signal cannot be controlled using the  $\overline{BCYST}$  signal when using EDO DRAM.

- Remarks**
1.  $T = t_{CYK}$
  2.  $w_{DA}$ : Wait count based on the  $DAC1n$  and  $DAC0n$  bits of the  $SCRn$  register ( $n = 1, 3, 4, 6$ )
  3.  $w_{CP}$ : Wait count based on the  $CPC1n$  and  $CPC0n$  bits of the  $SCRn$  register ( $n = 1, 3, 4, 6$ )
  4.  $w_{RP}$ : Wait count based on the  $RPC1n$  and  $RPC0n$  bits of the  $SCRn$  register ( $n = 1, 3, 4, 6$ )
  5.  $w_{RH}$ : Wait count based on the  $RHC1n$  and  $RHC0n$  bits of the  $SCRn$  register ( $n = 1, 3, 4, 6$ )

(b) Write timing (EDO DRAM) (2/2)



- Notes**
1. At least one clock is inserted in TRPW and TCPW.
  2. During on-page access from other cycles while  $\overline{\text{RAS}}$  is low level.

- Remarks**
1. This is the timing for the following case.
    - Wait count based on the RPC1n and RPC0n bits of the SCRn register (TRPW): 1
    - Wait count based on the RHC1n and RHC0n bits of the SCRn register (TRHW): 1
    - Wait count based on the DAC1n and DAC0n bits of the SCRn register (TDAW): 1
    - Wait count based on the CPC1n and CPC0n bits of the SCRn register (TCPW): 1
  2. Broken lines indicate high impedance.
  3. n = 1, 3, 4, 6

(c) DMA flyby transfer timing (EDO DRAM → external I/O transfer) (1/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	
$\overline{\text{WAIT}}$ setup time (to $\text{CLKOUT}\uparrow$ )	<32>	t <sub>SWK</sub>	8		ns	
$\overline{\text{WAIT}}$ hold time (from $\text{CLKOUT}\uparrow$ )	<33>	t <sub>HKW</sub>	0		ns	
Delay time from $\overline{\text{OE}}\uparrow$ to data output	<46>	t <sub>DRDOD</sub>	$(1 + i)T - 10$		ns	
Delay time from $\overline{\text{IOWR}}\uparrow$ to address	<53>	t <sub>DWRA</sub>	$1.5T - 10$		ns	
$\overline{\text{IOWR}}$ low-level width	<55>	t <sub>WWRL</sub>	WRP = 0	$(3 + \text{WRH} + \text{WDA} + w)T - 10$	ns	
			WRP ≥ 1	$(2 + \text{WRP} + \text{WDA} + \text{WRH} + w)T - 10$	ns	
Delay time from $\overline{\text{IOWR}}\uparrow$ to $\overline{\text{OE}}\uparrow$	<58>	t <sub>DWRRD</sub>	$T - 10$		ns	
Row address setup time	<66>	t <sub>ASR</sub>	$0.5T - 10$		ns	
Row address hold time	<67>	t <sub>RAH</sub>	$(0.5 + \text{WRH})T - 10$		ns	
Column address setup time	<68>	t <sub>ASC</sub>	$0.5T - 10$		ns	
Column address hold time	<69>	t <sub>CAH</sub>	$(2.5 + \text{WDA} + w)T - 10$		ns	
$\overline{\text{RAS}}$ precharge time	<70>	t <sub>RP</sub>	WRP = 0	$T - 10$	ns	
			WRP ≥ 1	$\text{WRP}T - 10$	ns	
Column address read time (to $\overline{\text{RAS}}$ )	<71>	t <sub>RAL</sub>	$(3.5 + \text{WCP} + \text{WDA} + w)T - 10$		ns	
$\overline{\text{CAS}}$ hold time	<72>	t <sub>CSH</sub>	$(3 + \text{WRH} + \text{WDA} + w)T - 10$		ns	
Delay time from $\overline{\text{RAS}}$ to column address	<73>	t <sub>RAD</sub>	$(0.5 + \text{WRH})T - 10$		ns	
Delay time from $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$	<74>	t <sub>RCD</sub>	$(1 + \text{WRH})T - 10$		ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	<75>	t <sub>CRP</sub>	WRP = 0	$2T - 10$	ns	
			WRP ≥ 1	$(1 + \text{WRP})T - 10$	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	<76>	t <sub>RHCP</sub>	$(4 + \text{WCP} + \text{WDA} + w)T - 10$		ns	
$\overline{\text{WE}}$ setup time (to $\overline{\text{CAS}}\downarrow$ )	<77>	t <sub>RCS</sub>	WRP = 0	$(3 + \text{WRH})T - 10$	ns	
			WRP ≥ 1	$(2 + \text{WRP} + \text{WRH})T - 10$	ns	
$\overline{\text{WE}}$ hold time (from $\overline{\text{RAS}}\uparrow$ )	<78>	t <sub>RRH</sub>	0		ns	
$\overline{\text{WE}}$ hold time (from $\overline{\text{CAS}}\uparrow$ )	<79>	t <sub>RCH</sub>	$T - 10$		ns	
$\overline{\text{RAS}}$ pulse width	Off-page	<80>	t <sub>RASP</sub>	$(4 + \text{WRH} + \text{WDA} + w)T - 10$	ns	
$\overline{\text{CAS}}$ precharge time		<82>	t <sub>CP</sub>	$(1 + \text{WCP})T - 10$	ns	
$\overline{\text{OE}}$ to $\overline{\text{CAS}}$ hold time	Off-page	<83>	t <sub>OCH1</sub>	WRP = 0	$(4 + \text{WRH} + \text{WDA} + w)T - 10$	ns
				WRP ≥ 1	$(3 + \text{WRP} + \text{WRH} + \text{WDA} + w)T - 10$	ns
	On-page	<84>	t <sub>OCH2</sub>	$(2 + \text{WCP} + \text{WDA} + w)T - 10$	ns	
Output buffer turn-off delay time (from $\overline{\text{OE}}\uparrow$ )		<92>	t <sub>OEZ</sub>	0	ns	
$\overline{\text{RAS}}$ hold time		<93>	t <sub>RSH</sub>	$(3 + \text{WDA} + w)T - 10$	ns	
Read/write cycle time		<103>	t <sub>RC</sub>	WRP = 0	$(5.5 + \text{WRH} + \text{WDA} + w)T - 10$	ns
				WRP ≥ 1	$(4.5 + \text{WRP} + \text{WRH} + \text{WDA} + w)T - 10$	ns
$\overline{\text{CAS}}$ pulse width		<104>	t <sub>CAS</sub>	$(2 + \text{WDA} + w)T - 10$	ns	
$\overline{\text{CAS}}$ precharge time		<105>	t <sub>CPN</sub>	WRP = 0	$(3 + \text{WRH})T - 10$	ns
				WRP ≥ 1	$(2 + \text{WRP} + \text{WRH})T - 10$	ns
High-speed page mode cycle time		<106>	t <sub>PC</sub>	$(3 + \text{WCP} + \text{WDA} + w)T - 10$	ns	

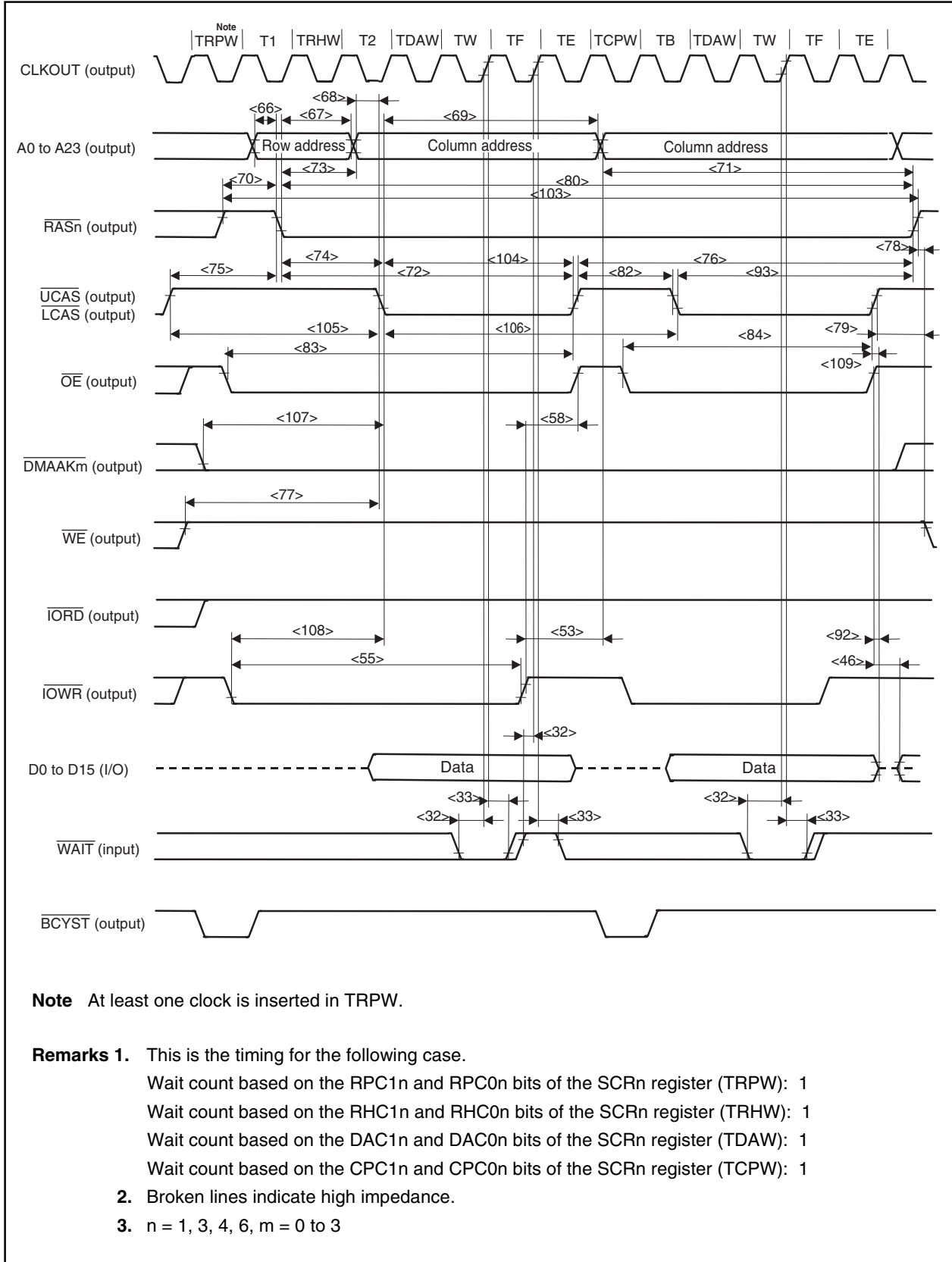
(c) DMA flyby transfer timing (EDO DRAM → external I/O transfer) (2/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Delay time from $\overline{\text{DMAAK}}_m\downarrow$ to $\overline{\text{CAS}}\downarrow$	<107>	$t_{\text{DDACS}}$	$\text{WRP} = 0$	$(2.5 + \text{WRH})T - 10$	ns
			$\text{WRP} \geq 1$	$(1.5 + \text{WRP} + \text{WRH})T - 10$	ns
Delay time from $\overline{\text{IOWR}}\downarrow$ to $\overline{\text{CAS}}\downarrow$	<108>	$t_{\text{DRDCS}}$	$\text{WRP} = 0$	$(2 + \text{WRH})T - 10$	ns
			$\text{WRP} \geq 1$	$(1 + \text{WRP} + \text{WRH})T - 10$	ns
Output buffer turn-off delay time (from $\overline{\text{CAS}}\uparrow$ )	<109>	$t_{\text{OFF}}$	0		ns

- Cautions**
1. At least one clock is inserted in  $\text{WRP}$  by default regardless of the setting of the  $\text{RPC1n}$  and  $\text{RPC0n}$  bits in the  $\text{SCRn}$  register ( $n = 1, 3, 4, 6$ ).
  2. The  $\overline{\text{WAIT}}$  signal cannot be controlled using the  $\overline{\text{BCYST}}$  signal when using EDO DRAM.

- Remarks**
1.  $T = t_{\text{CYK}}$
  2.  $w$ : Wait count based on  $\overline{\text{WAIT}}$
  3.  $w_{\text{DA}}$ : Wait count based on the  $\text{DAC1n}$  and  $\text{DAC0n}$  bits of the  $\text{SCRn}$  register ( $n = 1, 3, 4, 6$ )
  4.  $w_{\text{CP}}$ : Wait count based on the  $\text{CPC1n}$  and  $\text{CPC0n}$  bits of the  $\text{SCRn}$  register ( $n = 1, 3, 4, 6$ )
  5.  $\text{WRP}$ : Wait count based on the  $\text{RPC1n}$  and  $\text{RPC0n}$  bits of the  $\text{SCRn}$  register ( $n = 1, 3, 4, 6$ )
  6.  $\text{WRH}$ : Wait count based on the  $\text{RHC1n}$  and  $\text{RHC0n}$  bits of the  $\text{SCRn}$  register ( $n = 1, 3, 4, 6$ )
  7.  $i$ : Idle state count
  8.  $m = 0$  to 3

(c) DMA flyby transfer timing (EDO DRAM → external I/O transfer) (3/3)



(d) DMA flyby transfer timing (external I/O → EDO DRAM transfer) (1/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT↑)	<32>	t <sub>SWK</sub>	8		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT↑)	<33>	t <sub>HKW</sub>	0		ns
$\overline{\text{IORD}}$ low-level width	<41>	t <sub>WRDL</sub>	$(2 + W_{RH} + W_{DA} + w)T - 10$		ns
$\overline{\text{IORD}}$ high-level width	<42>	t <sub>WRDH</sub>	$T - 10$		ns
Delay time from $\overline{\text{IORD}}$ ↑ to address	<44>	t <sub>DRDA</sub>	$(0.5 + i)T - 10$		ns
Row address setup time	<66>	t <sub>ASR</sub>	$0.5T - 10$		ns
Row address hold time	<67>	t <sub>RAH</sub>	$(0.5 + W_{RH})T - 10$		ns
Column address setup time	<68>	t <sub>ASC</sub>	$0.5T - 10$		ns
Column address hold time	<69>	t <sub>CAH</sub>	$(1.5 + W_{DA})T - 10$		ns
$\overline{\text{RAS}}$ precharge time	<70>	t <sub>RP</sub>	WRP = 0	$T - 10$	ns
			WRP ≥ 1	$WRP T - 10$	ns
Column address read time (to $\overline{\text{RAS}}$ )	<71>	t <sub>RAL</sub>	$(2.5 + W_{CP} + W_{DA} + w)T - 10$		ns
$\overline{\text{CAS}}$ hold time	<72>	t <sub>CSH</sub>	$(2 + W_{RH} + W_{DA} + w)T - 10$		ns
Delay time from $\overline{\text{RAS}}$ to column address	<73>	t <sub>RAD</sub>	$(0.5 + W_{RH})T - 10$		ns
Delay time from $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$	<74>	t <sub>RCD</sub>	$(1 + W_{RH} + w)T - 10$		ns
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	<75>	t <sub>CRP</sub>	WRP = 0	$2T - 10$	ns
			WRP ≥ 1	$(1 + W_{RP})T - 10$	ns
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	<76>	t <sub>RHCP</sub>	$(4 + W_{CP} + W_{DA} + w)T - 10$		ns
$\overline{\text{RAS}}$ pulse width	Off-page	<80>	t <sub>RASP</sub>	$(3 + W_{RH} + W_{DA} + w)T - 10$	ns
$\overline{\text{CAS}}$ precharge time	<82>	t <sub>CP</sub>	$(1 + W_{CP} + w)T - 10$		ns
$\overline{\text{RAS}}$ hold time	<93>	t <sub>RSH</sub>	$(2 + W_{DA})T - 10$		ns
Read/write cycle time	<103>	t <sub>RC</sub>	WRP = 0	$(4.5 + W_{RH} + W_{DA} + w)T - 10$	ns
			WRP ≥ 1	$(3.5 + W_{RP} + W_{RH} + W_{DA} + w)T - 10$	ns
$\overline{\text{CAS}}$ pulse width	<104>	t <sub>CAS</sub>	$(1 + W_{DA})T - 10$		ns
$\overline{\text{CAS}}$ precharge time	<105>	t <sub>CPN</sub>	WRP = 0	$(3 + W_{RH} + w)T - 10$	ns
			WRP ≥ 1	$(2 + W_{RP} + W_{RH} + w)T - 10$	ns
High-speed page mode cycle	<106>	t <sub>PC</sub>	$(2 + W_{CP} + W_{DA} + w)T - 10$		ns
Delay time from $\overline{\text{DMAAKm}}$ ↓ to $\overline{\text{CAS}}$ ↓	<107>	t <sub>DDACS</sub>	WRP = 0	$(2.5 + W_{RH} + w)T - 10$	ns
			WRP ≥ 1	$(1.5 + W_{RP} + W_{RH} + w)T - 10$	ns
Delay time from $\overline{\text{IORD}}$ ↓ to $\overline{\text{CAS}}$ ↓	<108>	t <sub>DRDCS</sub>	WRP = 0	$(2 + W_{RH} + w)T - 10$	ns
			WRP ≥ 1	$(1 + W_{RP} + W_{RH} + w)T - 10$	ns
$\overline{\text{WE}}$ read time (to $\overline{\text{RAS}}$ ↑)	<110>	t <sub>RWL</sub>	$(3 + W_{DA} + w)T - 10$		ns
$\overline{\text{WE}}$ read time (to $\overline{\text{CAS}}$ ↑)	<111>	t <sub>CWL</sub>	$(2 + W_{DA} + w)T - 10$		ns
$\overline{\text{WE}}$ pulse width	<112>	t <sub>WP</sub>	$(2 + W_{DA} + w)T - 10$		ns
$\overline{\text{WE}}$ setup time (to $\overline{\text{CAS}}$ ↓)	Off-page	<113>	t <sub>WCS1</sub>	$(2 + W_{RH} + w)T - 10$	ns
	On-page	<114>	t <sub>WCS2</sub>	$T - 10$	ns

(d) DMA flyby transfer timing (external I/O → EDO DRAM transfer) (2/3)

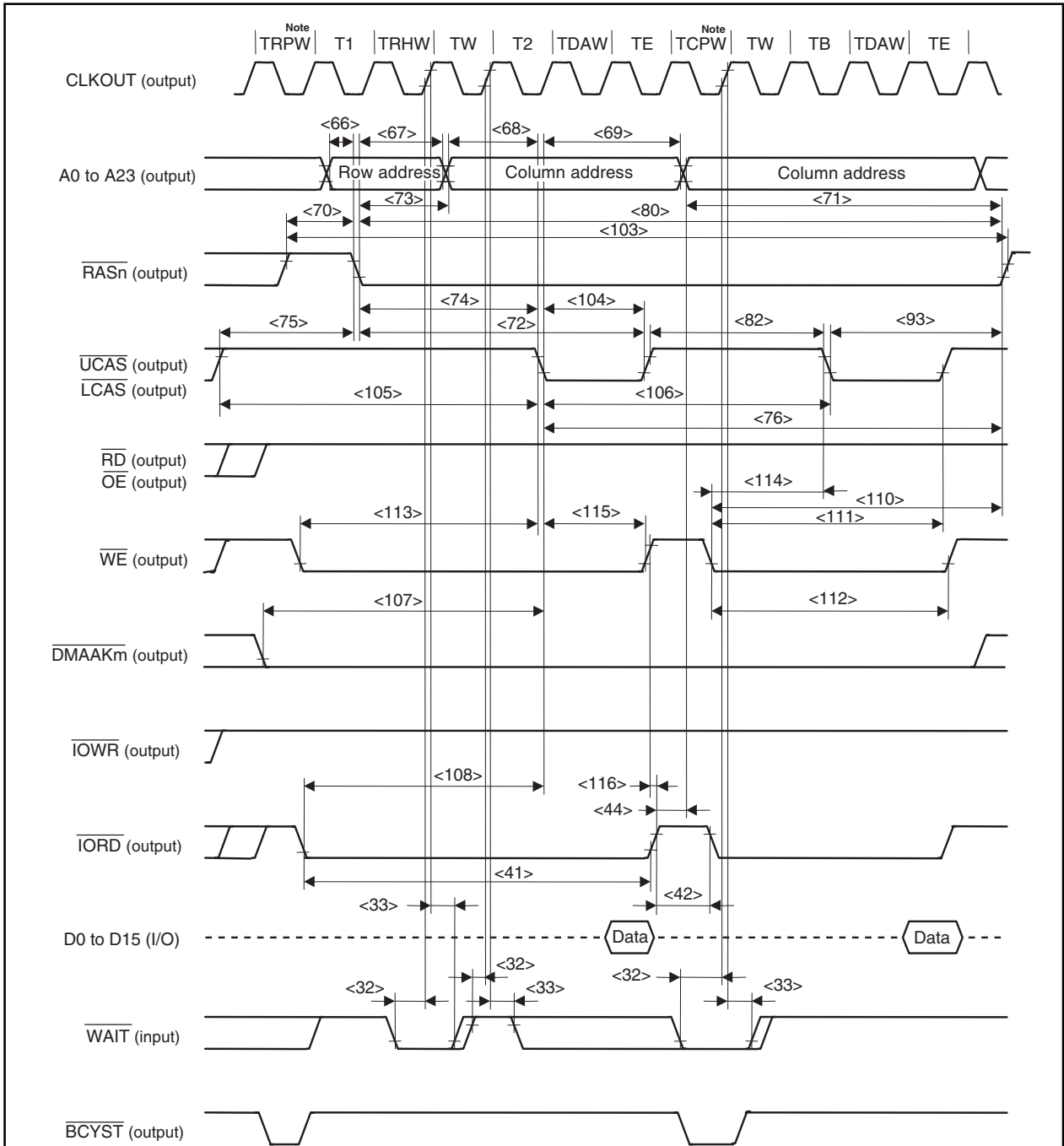
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{WE}}$ hold time (from $\overline{\text{CAS}} \downarrow$ )	<115>	$t_{\text{WCH}}$		$(1 + w_{\text{DA}})T - 10$		ns
Delay time from $\overline{\text{WE}} \uparrow$ to $\overline{\text{IORD}} \uparrow$	<116>	$t_{\text{DWERD}}$		0		ns

- Cautions**
- At least one clock is inserted in  $w_{\text{RP}}$  by default regardless of the setting of the  $\text{RPC1n}$  and  $\text{RPC0n}$  bits in the  $\text{SCRn}$  register ( $n = 1, 3, 4, 6$ ).
  - At least one clock is inserted in  $w_{\text{CP}}$  by default regardless of the setting of the  $\text{CPC1n}$  and  $\text{CPC0n}$  bits in the  $\text{SCRn}$  register ( $n = 1, 3, 4, 6$ ).
  - The  $\overline{\text{WAIT}}$  signal cannot be controlled using the  $\overline{\text{BCYST}}$  signal when using EDO DRAM.

- Remarks**
- $T = t_{\text{CYK}}$
  - $w$ : Wait counts based on  $\overline{\text{WAIT}}$
  - $w_{\text{DA}}$ : Wait count based on the  $\text{DAC1n}$  and  $\text{DAC0n}$  bits of the  $\text{SCRn}$  register ( $n = 1, 3, 4, 6$ )
  - $w_{\text{CP}}$ : Wait count based on the  $\text{CPC1n}$  and  $\text{CPC0n}$  bits of the  $\text{SCRn}$  register ( $n = 1, 3, 4, 6$ )
  - $w_{\text{RP}}$ : Wait count based on the  $\text{RPC1n}$  and  $\text{RPC0n}$  bits of the  $\text{SCRn}$  register ( $n = 1, 3, 4, 6$ )
  - $w_{\text{RH}}$ : Wait count based on the  $\text{RHC1n}$  and  $\text{RHC0n}$  bits of the  $\text{SCRn}$  register ( $n = 1, 3, 4, 6$ )
  - $i$ : Idle state count
  - $m = 0$  to 3



(d) DMA flyby transfer timing (external I/O → EDO DRAM transfer) (3/3)



**Note** At least one clock is inserted in TRPW and TCPW.

**Remarks 1.** This is the timing for the following case.

- Wait count based on the RPC1n and RPC0n bits of the SCRn register (TRPW): 1
- Wait count based on the RHC1n and RHC0n bits of the SCRn register (TRHW): 1
- Wait count based on the DAC1n and DAC0n bits of the SCRn register (TDAW): 1
- Wait count based on the CPC1n and CPC0n bits of the SCRn register (TCPW): 1

**2.** Broken lines indicate high impedance.

**3.** n = 1, 3, 4, 6, m = 0 to 3

(e) CBR refresh timing

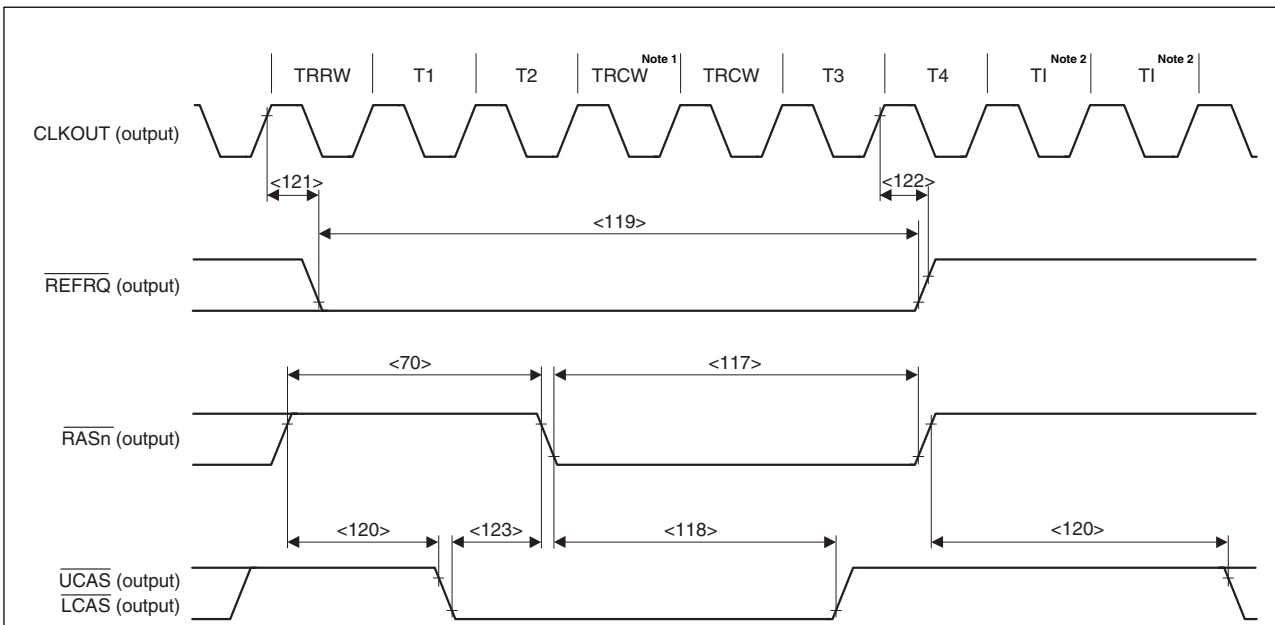
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{RAS}}$ precharge time	<70>	$t_{RP}$	$(1.5 + W_{RRW})T - 10$		ns
$\overline{\text{RAS}}$ pulse width	<117>	$t_{RAS}$	$(1.5 + W_{RCW}^{\text{Note 1}})T - 10$		ns
$\overline{\text{CAS}}$ hold time	<118>	$t_{CHR}$	$(0.5 + W_{RCW}^{\text{Note 1}})T - 10$		ns
$\overline{\text{REFRQ}}$ pulse width	<119>	$t_{WRFL}$	$(3 + W_{RRW} + W_{RCW}^{\text{Note 1}})T - 10$		ns
$\overline{\text{RAS}}$ precharge $\overline{\text{CAS}}$ hold time	<120>	$t_{RPC}$	$(2.5 + W_{RRW})T - 10$		ns
$\overline{\text{REFRQ}}$ active delay time (from CLKOUT↑)	<121>	$t_{DKRF}$	2	13	ns
$\overline{\text{REFRQ}}$ inactive delay time (from CLKOUT↑)	<122>	$t_{HKRF}$	2	13	ns
$\overline{\text{CAS}}$ setup time	<123>	$t_{CSR}$	$T - 10$		ns

**Note** At least one clock is inserted in  $W_{RCW}$  by default, regardless of the settings of the RCW0 to RCW2 bits of the RWC register.

**Remarks 1.**  $T = t_{CYK}$

**2.**  $W_{RRW}$ : Wait count based on the RRW0 and RRW1 bits of the RWC register

**3.**  $W_{RCW}$ : Wait count based on the RCW0 to RCW2 bits of the RWC register



**Notes 1.** At least one clock is inserted in TRCW, regardless of the settings of the RCW0 to RCW2 bits of the RWC register.

**2.** Idle state (TI) independent of the setting of the BCC register

**Remarks 1.** This is the timing for the following case.

Wait count based on the RRW0 and RRW1 bits of the RWC register ( $W_{RRW}$ ): 1

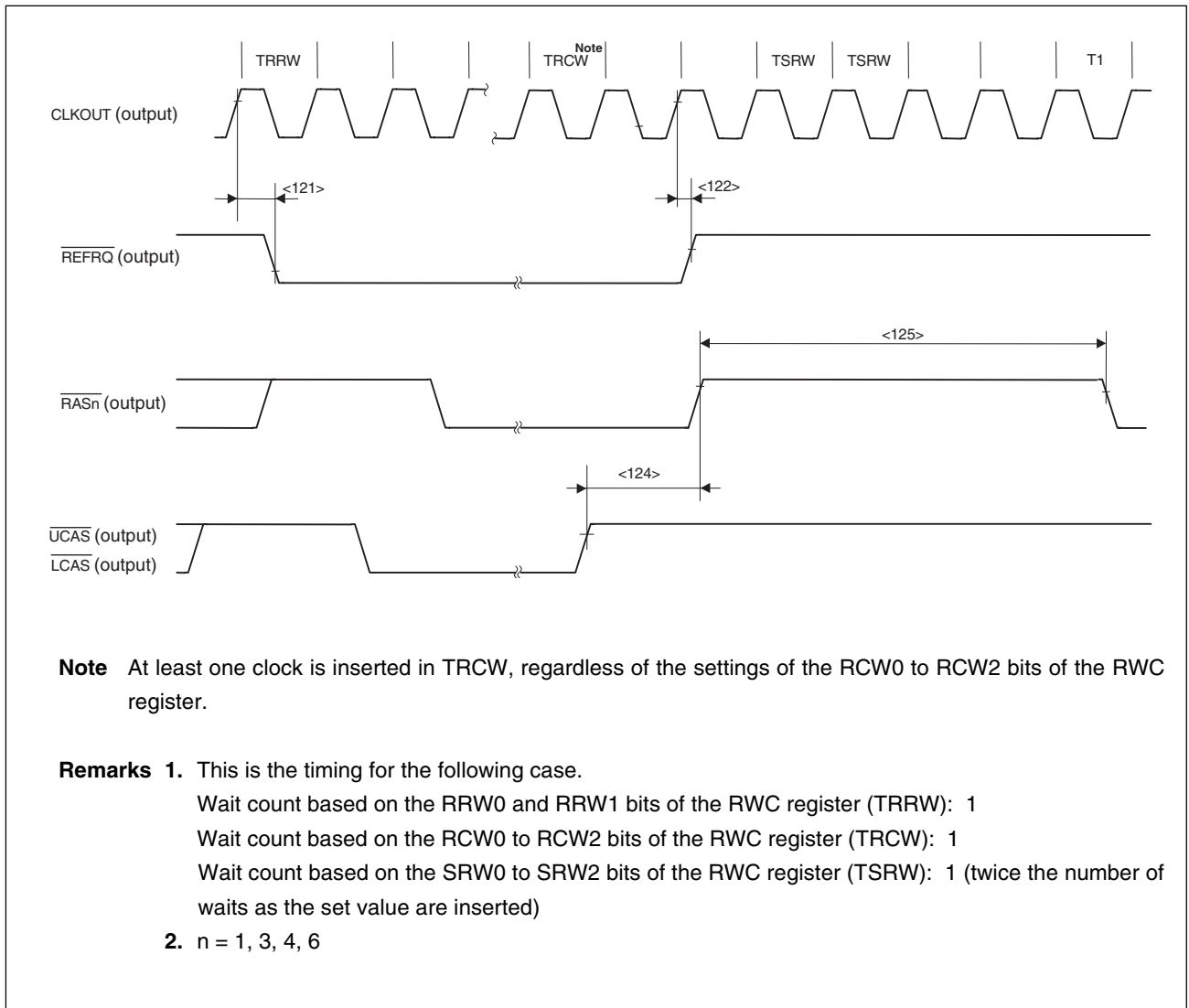
Wait count based on the RCW0 to RCW2 bits of the RWC register ( $W_{RCW}$ ): 2

**2.**  $n = 0$  to  $7$

(f) CBR self-refresh timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{REFRQ}}$ active delay time (from CLKOUT↑)	<121>	$t_{DKRF}$	2	13	ns
$\overline{\text{REFRQ}}$ inactive delay time (from CLKOUT↑)	<122>	$t_{HKRF}$	2	13	ns
$\overline{\text{CAS}}$ hold time	<124>	$t_{CHS}$	$-(WRCW \cdot T - 10)$		ns
$\overline{\text{RAS}}$ precharge time	<125>	$t_{RPS}$	$WRP = 0$	$(3 + 2W_{SRW})T - 10$	ns
			$WRP \geq 1$	$(2 + 2W_{SRW} + W_{RPW})T - 10$	ns

- Remarks**
1.  $T = t_{CYK}$
  2.  $W_{SRW}$ : Wait count based on the SRW0 to SRW2 bits of the RWC register
  3.  $W_{RCW}$ : Wait count based on the RCW0 to RCW2 bits of the RWC register
  4.  $W_{RPW}$ : Wait count based on the RRW0 and RRW1 bits of the RWC register



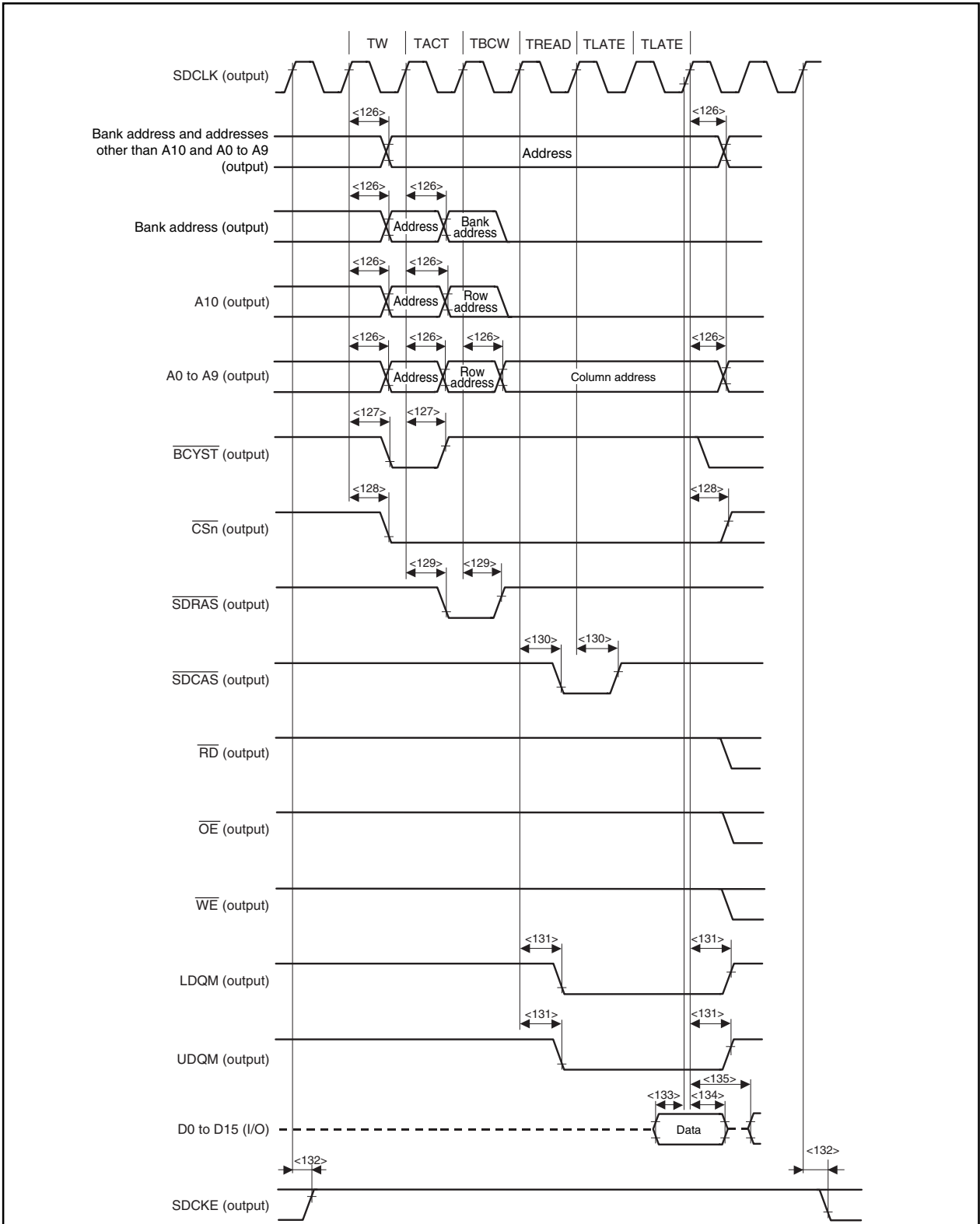
**(8) SDRAM access timing**

**(a) Read timing (SDRAM access) (1/2)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Address delay time (from SDCLK↑)	<126> t <sub>DKA</sub>		2	13	ns
BCYST delay time (from SDCLK↑)	<127> t <sub>DKBC</sub>		2	13	ns
C <sub>S</sub> n delay time (from SDCLK↑)	<128> t <sub>DKCS</sub>		2	13	ns
SDRAS delay time (from SDCLK↑)	<129> t <sub>DKRAS</sub>		2	13	ns
SDCAS delay time (from SDCLK↑)	<130> t <sub>DKCAS</sub>		2	13	ns
UDQM, LDQM delay time (from SDCLK↑)	<131> t <sub>DKDQM</sub>		2	13	ns
SDCKE delay time (from SDCLK↑)	<132> t <sub>DKCKE</sub>		2	13	ns
Data input setup time (at SDRAM read, to SDCLK↑)	<133> t <sub>SDRMK</sub>		8		ns
Data input hold time (at SDRAM read, from SDCLK↑)	<134> t <sub>HKDRM</sub>		0		ns
Delay time from SDCLK↑ to data output	<135> t <sub>DSOD</sub>			(1 + i) T - 5	ns

- Remarks**
1. T = t<sub>CYK2</sub>
  2. i = Idle state count
  3. n = 1, 3, 4, 6

(a) Read timing (SDRAM access) (2/2)



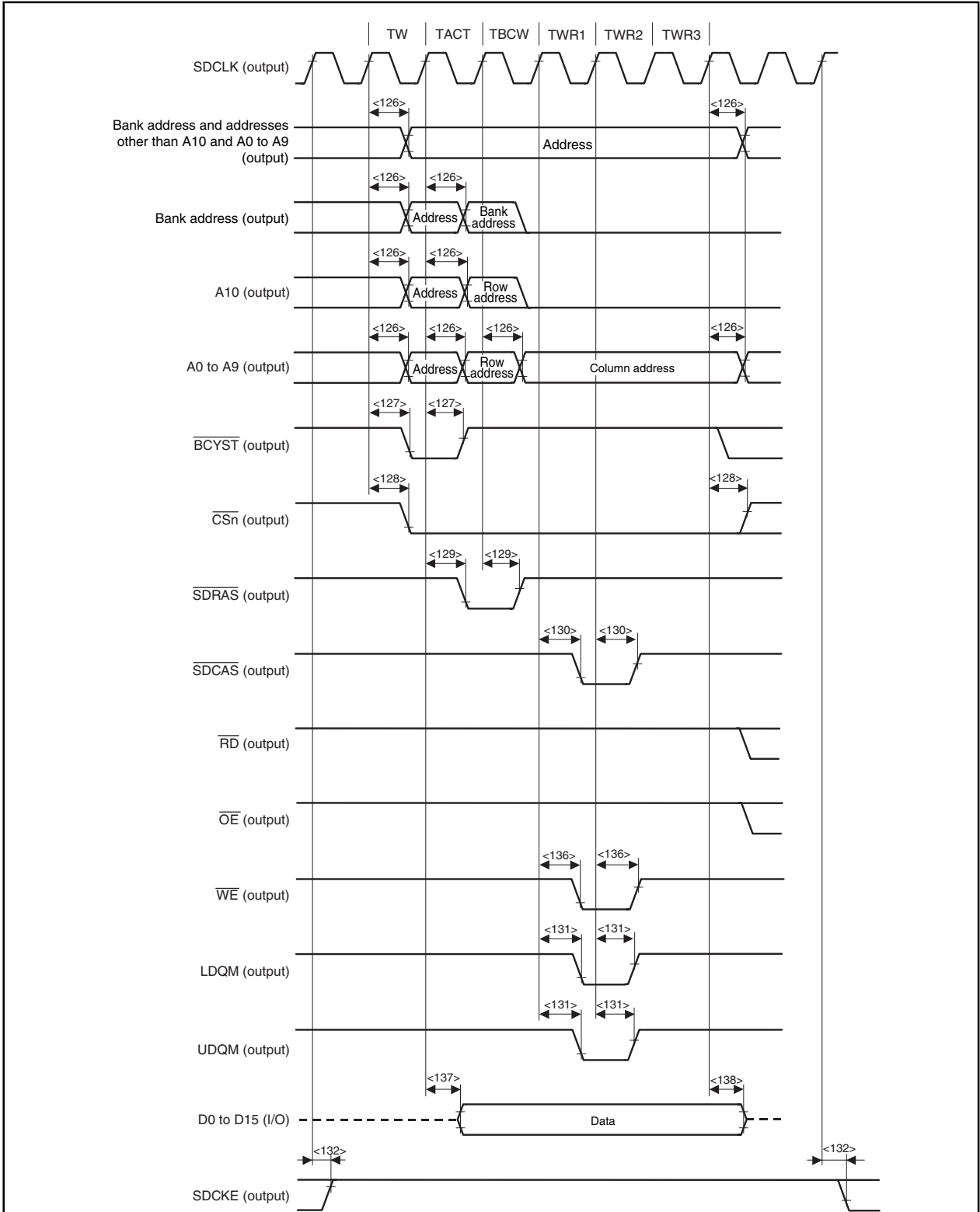
- Remarks**
1. Wait count based on the BCW1n and BCW0n bits of the SCRn register (TBCW): 2
  2. Broken lines indicate high impedance.
  3. n = 1, 3, 4, 6

(b) Write timing (SDRAM access) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Address delay time (from SDCLK↑)	<126> t <sub>DKA</sub>		2	13	ns
BCYST delay time (from SDCLK↑)	<127> t <sub>DKBC</sub>		2	13	ns
CSn delay time (from SDCLK↑)	<128> t <sub>DKCS</sub>		2	13	ns
SDRAS delay time (from SDCLK↑)	<129> t <sub>DKRAS</sub>		2	13	ns
SDCAS delay time (from SDCLK↑)	<130> t <sub>DKCAS</sub>		2	13	ns
UDQM, LDQM delay time (from SDCLK↑)	<131> t <sub>DKDQM</sub>		2	13	ns
SDCKE delay time (from SDCLK↑)	<132> t <sub>DKCKE</sub>		2	13	ns
WE delay time (from SDCLK↑)	<136> t <sub>DKWE</sub>		2	13	ns
Data output delay time (from SDCLK↑)	<137> t <sub>DKDT</sub>		2	13	ns
Data float delay time (from SDCLK↑)	<138> t <sub>HZKDT</sub>		2	13	ns

**Remark** n = 1, 3, 4, 6

(b) Write timing (SDRAM access) (2/2)

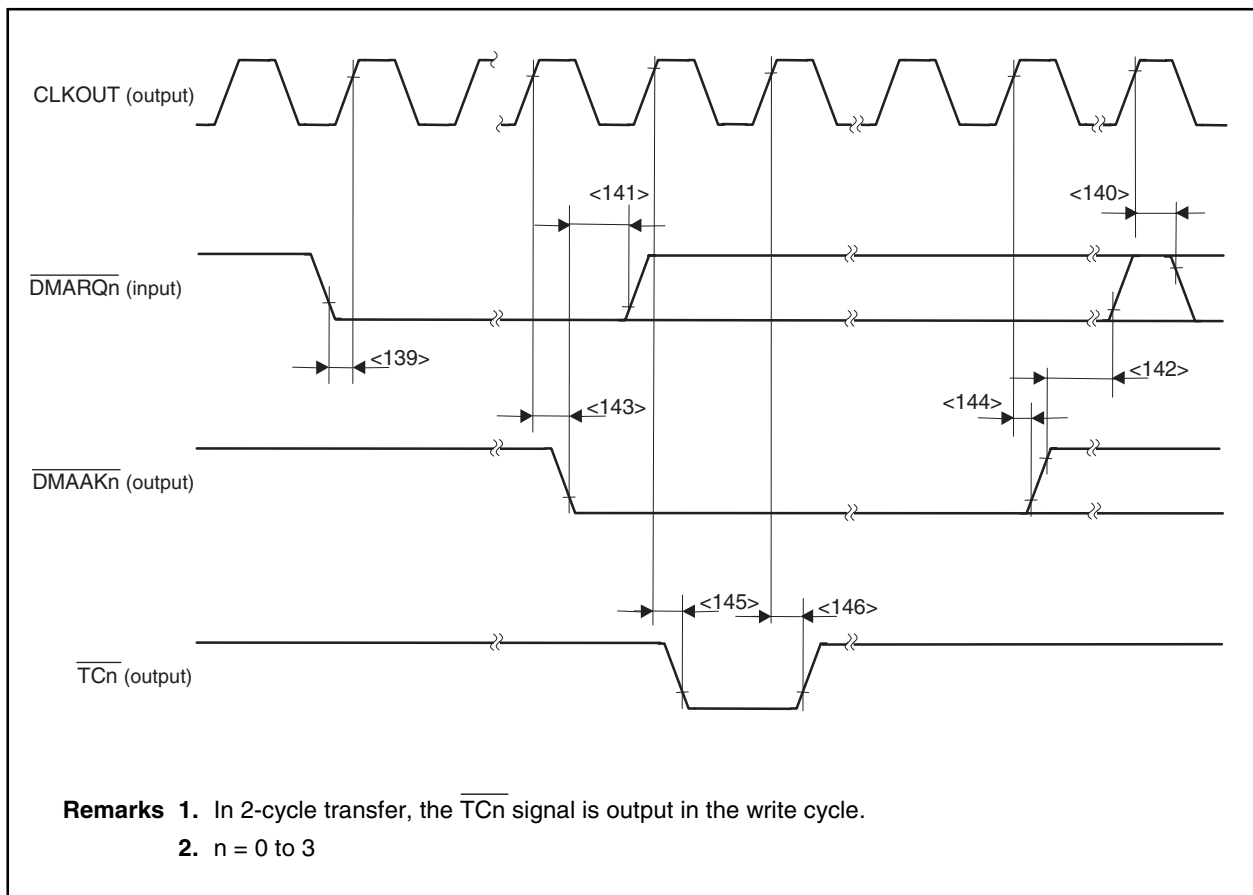


- Remarks**
1. Wait count based on the BCW1n and BCW0n bits of the SCRn register (TBCW): 2
  2. Broken lines indicate high impedance.
  3. n = 1, 3, 4, 6

(9) DMAC timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
DMARQn setup time (to CLKOUT↑)	<139> $t_{SDRK}$		8		ns
DMARQn hold time	<140> $t_{HKDR1}$	After inactive (from CLKOUT↑)	3		ns
	<141> $t_{HKDR2}$			Until DMAAKn↓	ns
Second DMA request disable timing in single transfer	<142> $t_{AKDR}$			3T	ns
DMAAKn output delay time (from CLKOUT↑)	<143> $t_{DKDA}$		2	13	ns
DMAAKn output hold time (from CLKOUT↑)	<144> $t_{HKDA}$		2	13	ns
TCn output delay time (from CLKOUT↑)	<145> $t_{HKTC}$		2	13	ns
TCn output hold time (from CLKOUT↑)	<146> $t_{HKTC}$		2	13	ns

- Remarks**
1.  $T = t_{CYK}$
  2.  $n = 0$  to 3



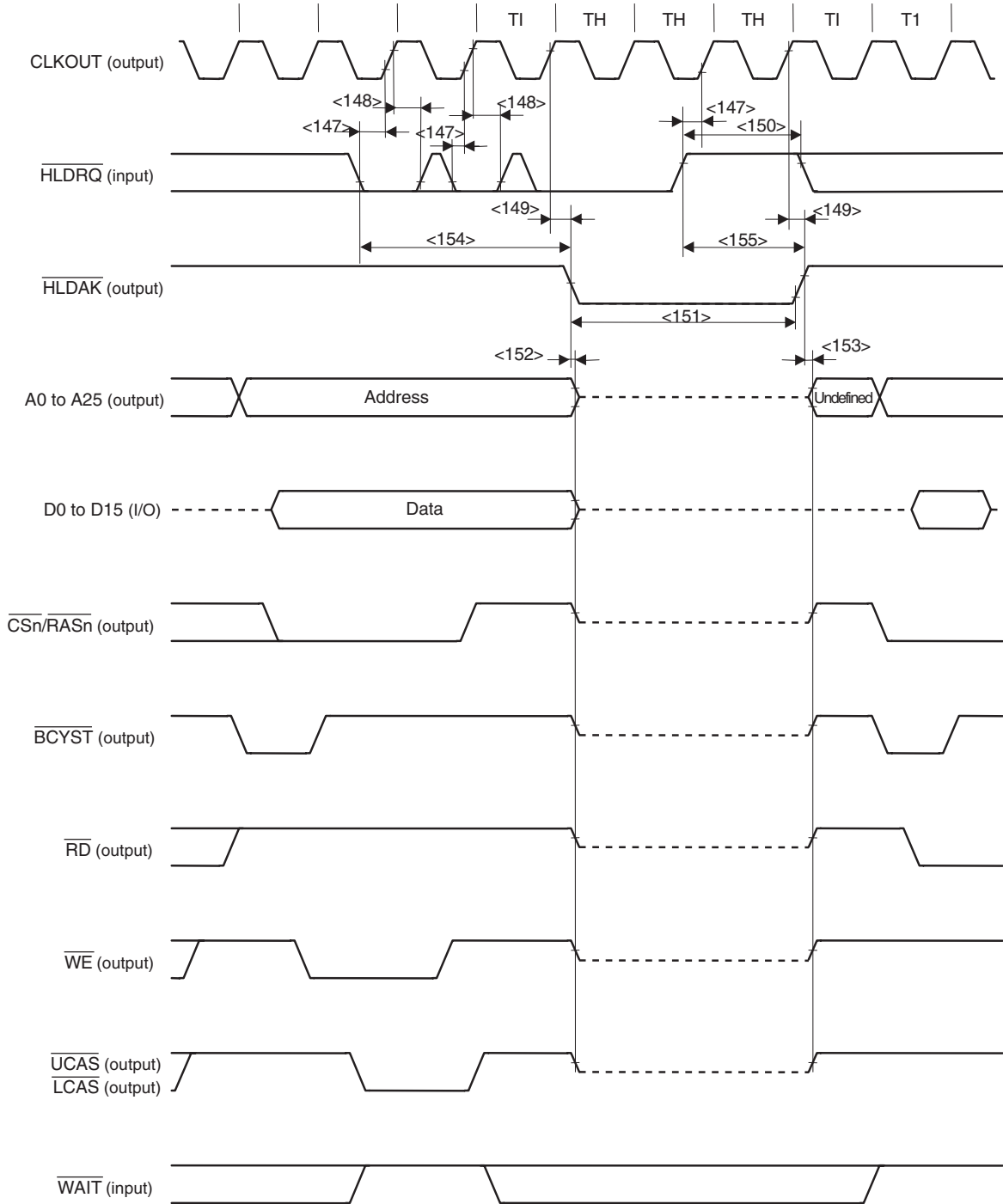


(10) Bus hold timing (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{HLDRQ}}$ setup time (to $\text{CLKOUT}\uparrow$ )	<147>	$t_{\text{SHRK}}$		8		ns
$\overline{\text{HLDRQ}}$ hold time (from $\text{CLKOUT}\uparrow$ )	<148>	$t_{\text{HKHR}}$		3		ns
Delay time from $\text{CLKOUT}\uparrow$ to $\overline{\text{HLDAK}}$	<149>	$t_{\text{DKHA}}$		2	13	ns
$\overline{\text{HLDRQ}}$ high-level width	<150>	$t_{\text{WHQH}}$		$T + 3$		ns
$\overline{\text{HLDAK}}$ low-level width	<151>	$t_{\text{WHAL}}$		$T - 11$		ns
Delay time from $\overline{\text{HLDAK}}\downarrow$ to bus float	<152>	$t_{\text{DKCF}}$		0		ns
Delay time from $\overline{\text{HLDAK}}\uparrow$ to bus output	<153>	$t_{\text{DHAC}}$		2	13	ns
Delay time from $\overline{\text{HLDRQ}}\downarrow$ to $\overline{\text{HLDAK}}\downarrow$	<154>	$t_{\text{DHQA1}}$		2T		ns
Delay time from $\overline{\text{HLDRQ}}\uparrow$ to $\overline{\text{HLDAK}}\uparrow$	<155>	$t_{\text{DHQA2}}$		T	2T + 10	ns

**Remark** T =  $t_{\text{CYK}}$

(10) Bus hold timing (2/2)

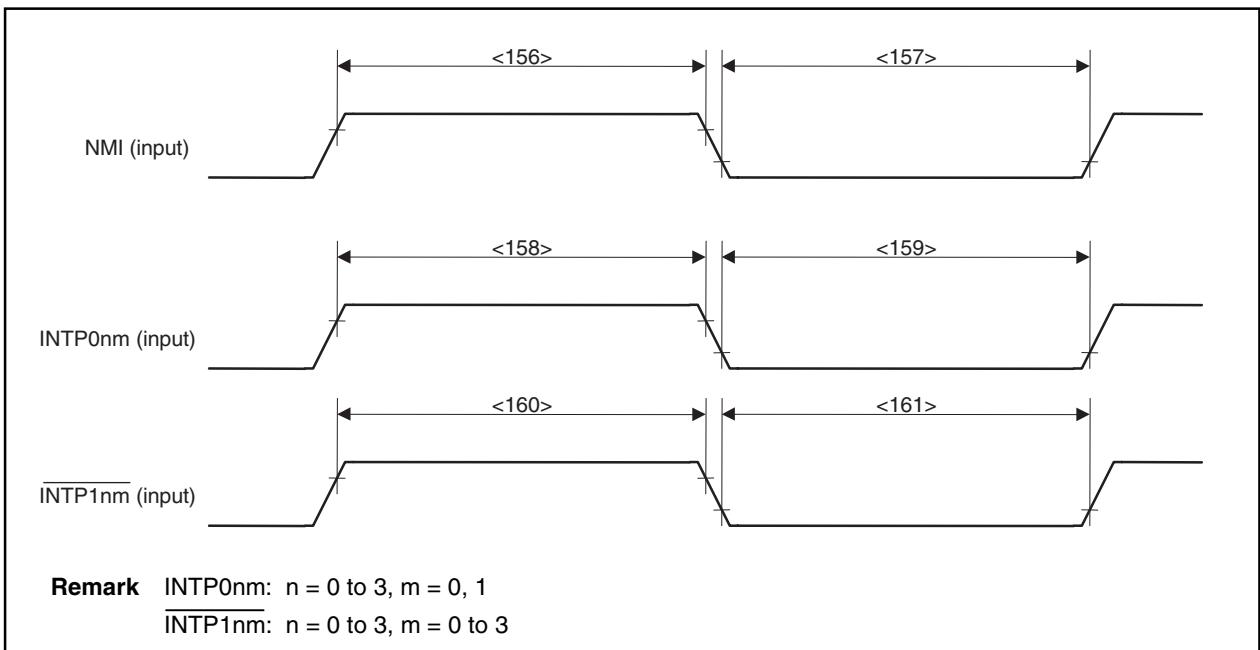


- Remarks**
1. Broken lines indicate high impedance.
  2. n = 0 to 7

(11) Interrupt timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
NMI high-level width	<156> $t_{WNIH}$		500		ns
NMI low-level width	<157> $t_{WNIL}$		500		ns
INTP0nm high-level width	<158> $t_{WIT0H}$		$3T + 500$		ns
INTP0nm low-level width	<159> $t_{WIT0L}$		$3T + 500$		ns
$\overline{\text{INTP1nm}}$ high-level width	<160> $t_{WIT1H}$		500		ns
$\overline{\text{INTP1nm}}$ low-level width	<161> $t_{WIT1L}$		500		ns

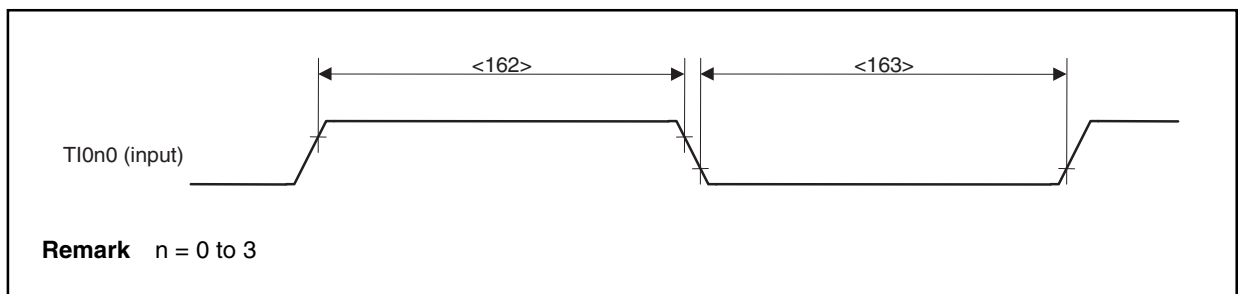
- Remarks** 1. INTP0nm:  $n = 0$  to 3,  $m = 0, 1$   
 $\overline{\text{INTP1nm}}$ :  $n = 0$  to 3,  $m = 0$  to 3  
 2.  $T = t_{CYK}$



(12) RPU timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Tl0n0 high-level width	<162> $t_{WTIH}$		$3T + 500$		ns
Tl0n0 low-level width	<163> $t_{WTIL}$		$3T + 500$		ns

- Remarks** 1.  $n = 0$  to 3  
 2.  $T = t_{CYK}$



(13) CS10 to CS12 timing (1/3)

(a) Master mode

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<164> $t_{CYSK1}$	Output	320		ns
$\overline{SCKn}$ high-level width	<165> $t_{WSK1H}$	Output	$0.5t_{CYSK1} - 20$		ns
$\overline{SCKn}$ low-level width	<166> $t_{WSK1L}$	Output	$0.5t_{CYSK1} - 20$		ns
SIn setup time (to $\overline{SCKn}\uparrow$ )	<167> $t_{SSISK}$		30		ns
SIn setup time (to $\overline{SCKn}\downarrow$ )			30		ns
SIn hold time (from $\overline{SCKn}\uparrow$ )	<168> $t_{HSKSI}$		30		ns
SIn hold time (from $\overline{SCKn}\downarrow$ )			30		ns
SOn output delay time (from $\overline{SCKn}\downarrow$ )	<169> $t_{DSKSO}$			30	ns
SOn output delay time (from $\overline{SCKn}\uparrow$ )				30	ns
SOn output hold time (from $\overline{SCKn}\uparrow$ )	<170> $t_{HSKSO}$		$0.5t_{CYSK1} - 5$		ns
SOn output hold time (from $\overline{SCKn}\downarrow$ )				$0.5t_{CYSK1} - 5$	

Remark n = 0 to 2

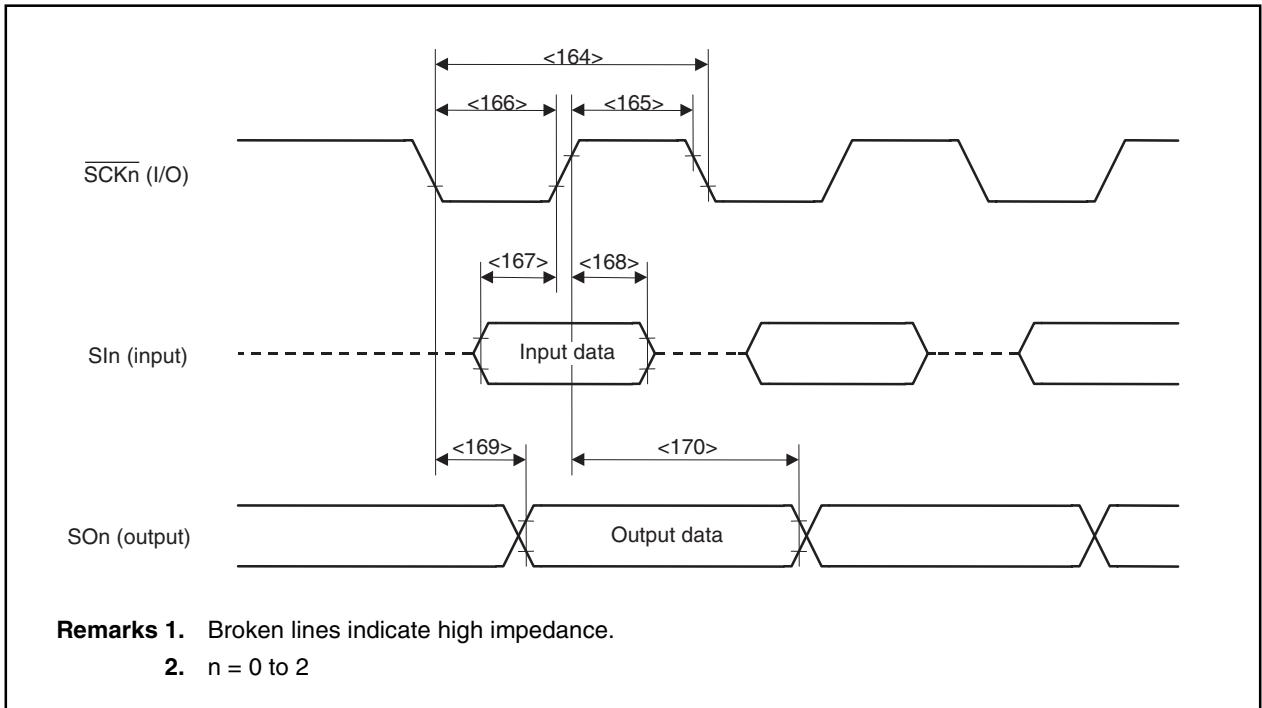
(b) Slave mode

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<164> $t_{CYSK1}$	Input	200		ns
$\overline{SCKn}$ high-level width	<165> $t_{WSK1H}$	Input	90		ns
$\overline{SCKn}$ low-level width	<166> $t_{WSK1L}$	Input	90		ns
SIn setup time (to $\overline{SCKn}\uparrow$ )	<167> $t_{SSISK}$		50		ns
SIn setup time (to $\overline{SCKn}\downarrow$ )			50		ns
SIn hold time (from $\overline{SCKn}\uparrow$ )	<168> $t_{HSKSI}$		50		ns
SIn hold time (from $\overline{SCKn}\downarrow$ )			50		ns
SOn output delay time (from $\overline{SCKn}\downarrow$ )	<169> $t_{DSKSO}$			50	ns
SOn output delay time (from $\overline{SCKn}\uparrow$ )				50	ns
SOn output hold time (from $\overline{SCKn}\uparrow$ )	<170> $t_{HSKSO}$		$t_{WSK1H}$		ns
SOn output hold time (from $\overline{SCKn}\downarrow$ )				$t_{WSK1H}$	

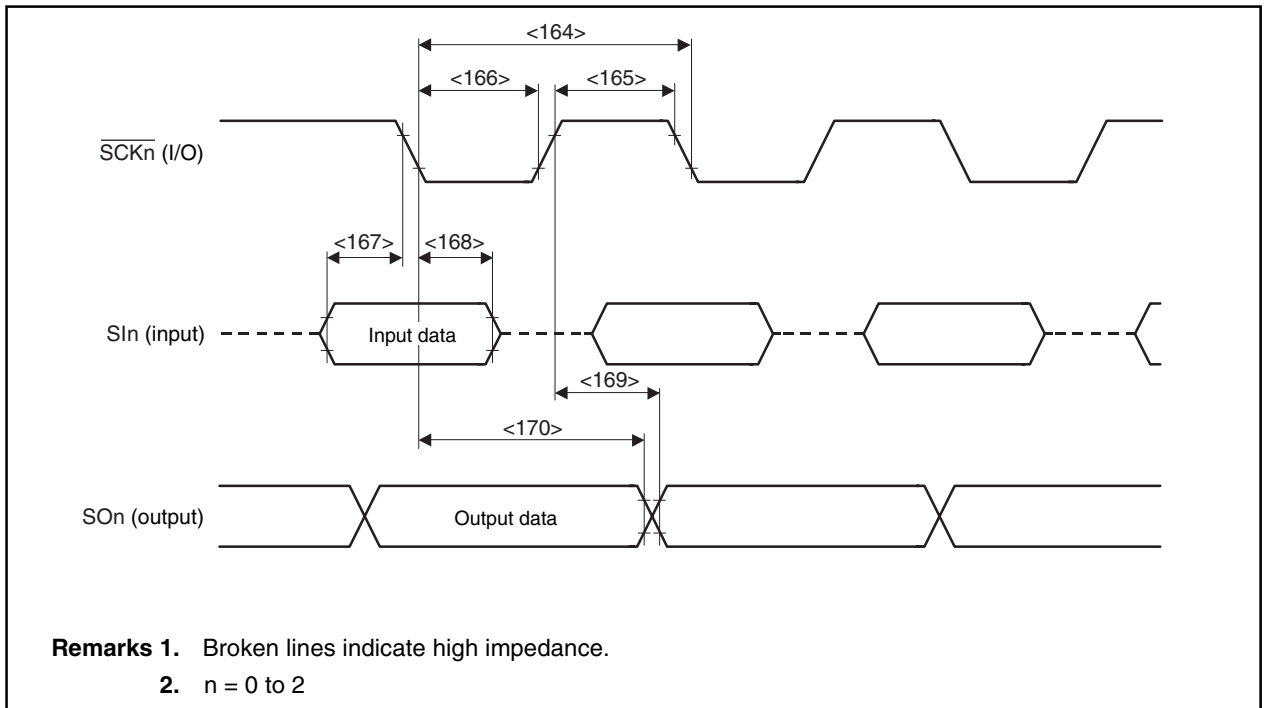
Remark n = 0 to 2

(13) CSI0 to CSI2 timing (2/3)

(c) Timing when CKPn, DAPn bits of CSICn register = 00

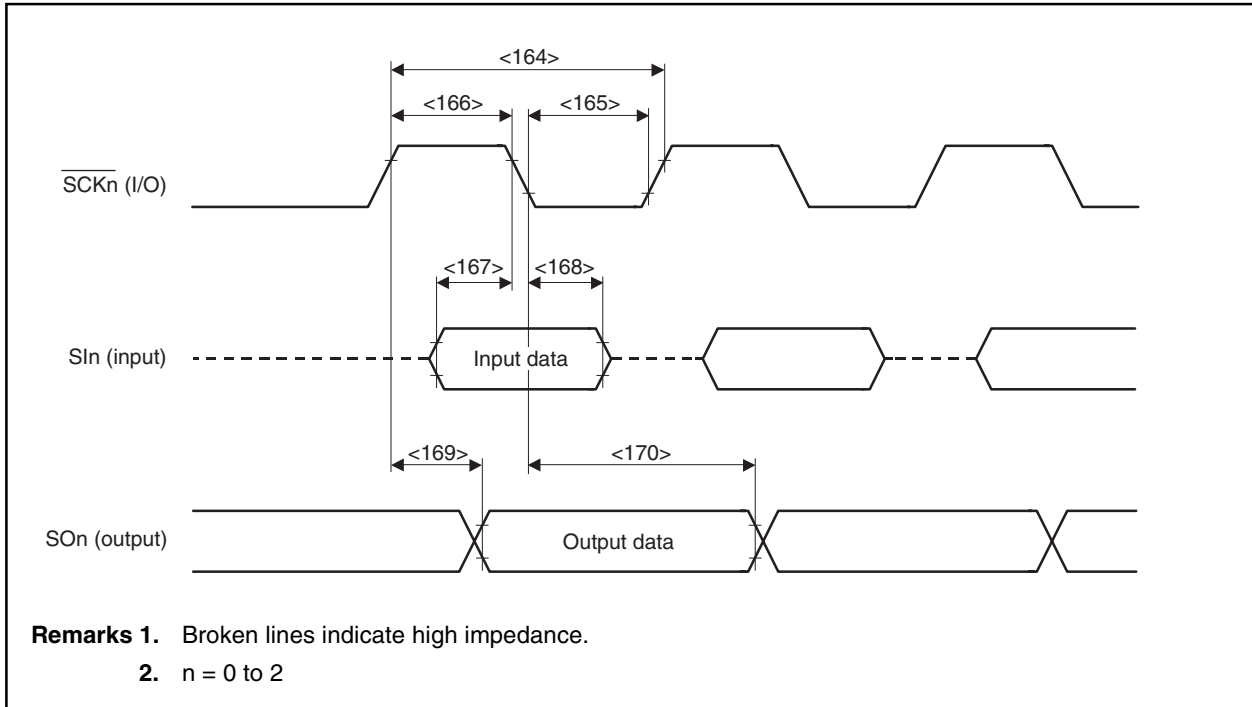


(d) Timing when CKPn, DAPn bits of CSICn register = 01

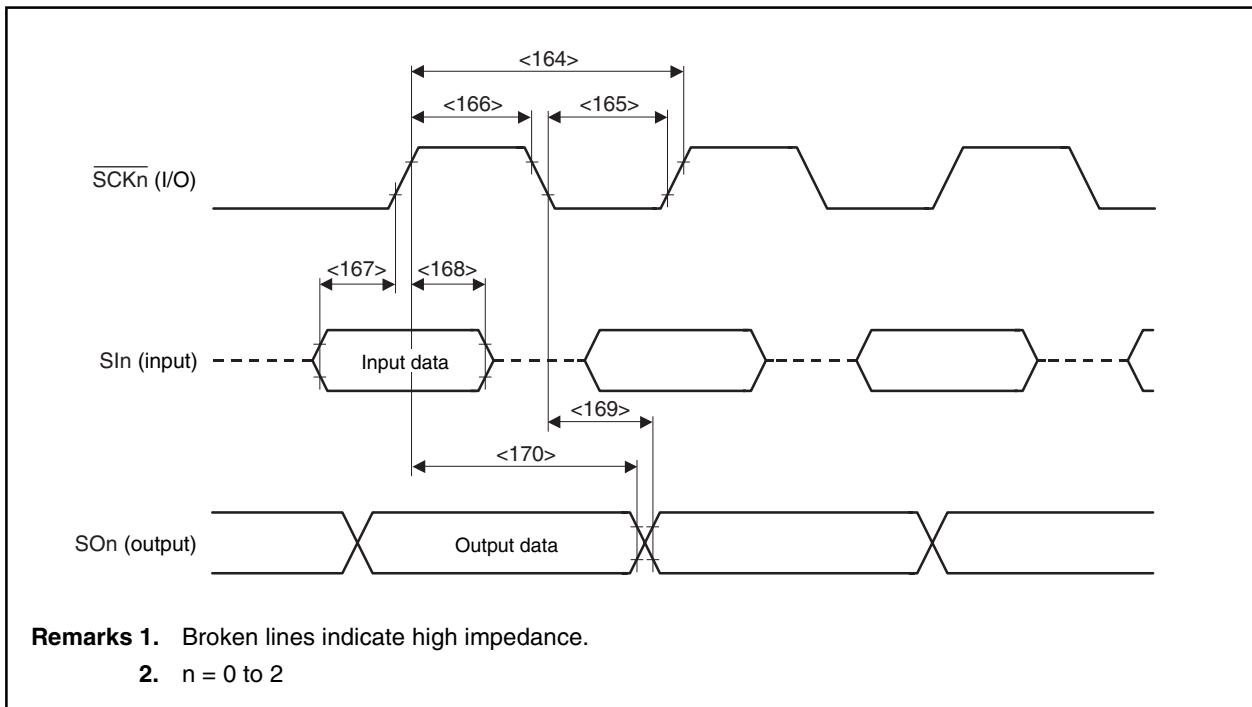


(13) CSI0 to CSI2 timing (3/3)

(e) Timing when CKPn, DAPn bits of CSICn register = 10



(f) Timing when CKPn, DAPn bits of CSICn register = 11



**A/D Converter Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = AV<sub>DD</sub> = 3.0 to 3.6 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	–		10			bit
Overall error <sup>Note 1</sup>	–				±0.49	%FSR
Quantization error	–				±1/2	%FSR
Conversion time	t <sub>CONV</sub>		5		10	μs
Sampling time	t <sub>SAMP</sub>		Conversion clock <sup>Note 2</sup> /6			ns
Zero-scale error <sup>Note 1</sup>	–				±0.49	%FSR
Full-scale error <sup>Note 3</sup>	–				±0.49	%FSR
Integral linearity error <sup>Note 3</sup>	–				±4	LSB
Differential linearity error <sup>Note 3</sup>	–				±4	LSB
Analog input voltage	V <sub>WASN</sub>		-0.3		AV <sub>REF</sub> + 0.3	V
AV <sub>REF</sub> input voltage	AV <sub>REF</sub>	AV <sub>REF</sub> = AV <sub>DD</sub>	3.0		3.6	V
AV <sub>DD</sub> supply current	AI <sub>DD</sub>				10	mA

- Notes**
1. Excluding quantization error (±0.05 %FSR)
  2. Conversion clock is the number of clocks set by the ADM1 resistor.
  3. Excluding quantization error (±0.5 LSB)

**Remark** LSB: Least Significant Bit  
 FSR: Full Scale Range  
 %FSR is the ratio to the full-scale value.

4.2 Flash Memory Programming Mode

Basic Characteristics (T<sub>A</sub> = 10 to 40°C (during rewrite), T<sub>A</sub> = -40 to +85°C (except during rewrite), V<sub>DD</sub> = AV<sub>DD</sub> = 3.0 to 3.6 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V) (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f <sub>XX</sub>		4		50	MHz
V <sub>PP</sub> supply voltage	V <sub>PP1</sub>	During flash memory programming	7.5	7.8	8.1	V
	V <sub>PPL</sub>	V <sub>PP</sub> low-level detection	-0.5		0.2V <sub>DD</sub>	V
	V <sub>PPM</sub>	V <sub>PP</sub> , V <sub>DD</sub> level detection	0.65V <sub>DD</sub>		V <sub>DD</sub> + 0.3	V
	V <sub>PPH</sub>	V <sub>PP</sub> high-voltage level detection	7.5	7.8	8.1	V
V <sub>DD</sub> supply current	I <sub>DD</sub>	V <sub>PP</sub> = V <sub>PP1</sub>			4.8f <sub>XX</sub> + 45	mA
V <sub>PP</sub> supply current	I <sub>PP</sub>	V <sub>PP</sub> = 7.8 V			100	mA
Step erase time	t <sub>ER</sub>	<b>Note 1</b>	0.398	0.4	0.402	s
Overall erase time per area	t <sub>ERA</sub>	When the step erase time = 0.4 s <b>Note 2</b>			40	s/area
Write-back time	t <sub>WB</sub>	<b>Note 3</b>	0.99	1	1.01	ms
Number of write-backs per write-back command	C <sub>WB</sub>	When the write-back time = 1 ms <b>Note 4</b>			300	Count/write-back command
Number of erase/write-backs	C <sub>ERWB</sub>				16	Count
Step writing time	t <sub>WT</sub>	<b>Note 5</b>	18	20	22	μs
Overall writing time per word	t <sub>WTW</sub>	When the step writing time = 20 μs (1 word = 4 bytes) <b>Note 6</b>	20		200	μs/word

- Notes**
1. The recommended setting value of the step erase time is 0.4 s.
  2. The prewrite time prior to erasure and the erase verify time (write-back time) are not included.
  3. The recommended setting value of the write-back time is 1 ms.
  4. Write-back is executed once by the issuance of the write-back command. Therefore, the retry count must be the maximum value minus the number of commands issued.
  5. The recommended setting value of the step writing time is 20 μs.
  6. 100 μs is added to the actual writing time per word. The internal verify time during and after the writing is not included.

- Remarks**
1. When the PG-FP3 is used, a time parameter required for writing/erasing by downloading parameter files is automatically set. Do not change the settings otherwise specified.
  2. Area 0 = 00000H to 1FFFFH, area 1 = 20000H to 3FFFFH



**Basic Characteristics** (T<sub>A</sub> = 10 to 40°C (during rewrite), T<sub>A</sub> = -40 to +85°C (except during rewrite), V<sub>DD</sub> = AV<sub>DD</sub> = 3.0 to 3.6 V, V<sub>SS</sub> = AV<sub>SS</sub> = 0 V) (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Number of rewrites per area	C <sub>ERWR</sub>	1 erase + 1 write after erase = 1 rewrite <b>Note 1</b>	<b>Note 2</b>	20		Count/area
			<b>Note 3</b>	100		

**Notes 1.** When writing initially to shipped products, it is counted as one rewrite for both “erase to write” and “write only”.

**Example** (P: Write, E: Erase)

Shipped product → P → E → P → E → P: 3 rewrites

Shipped product → E → P → E → P → E → P: 3 rewrites

- 2. LQFP package: Lot number 0124Pxxxx or earlier  
FBGA package: Lot number 0123Pxxxx or earlier
- 3. LQFP package: Lot number 0125Pxxxx or later  
FBGA package: Lot number 0124Pxxxx or later

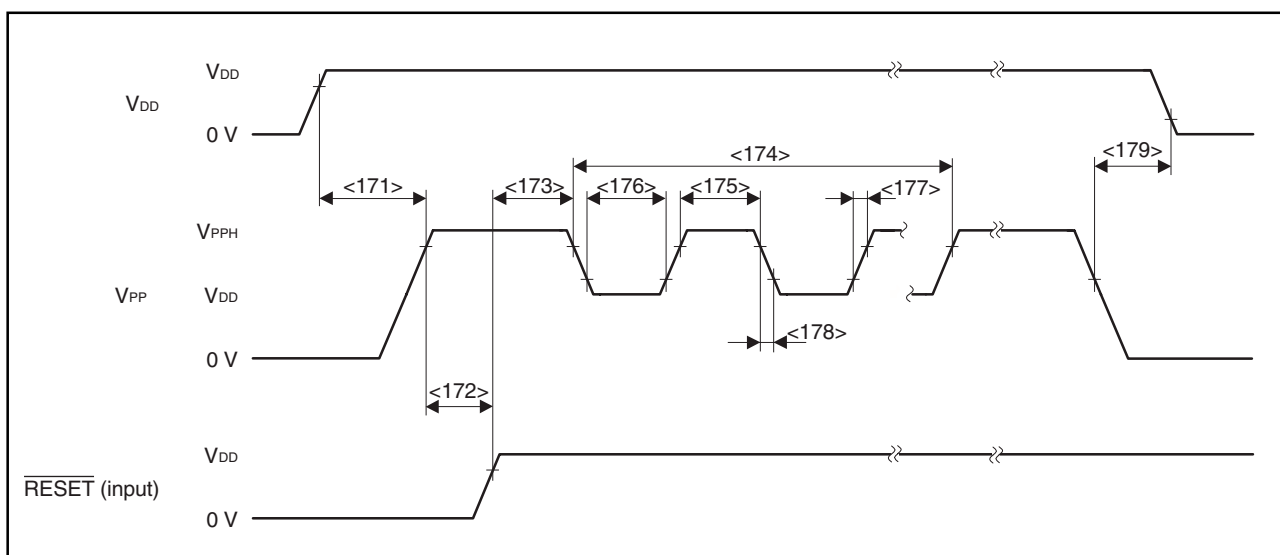
**Remarks 1.** When the PG-FP3 is used, a time parameter required for writing/erasing by downloading parameter files is automatically set. Do not change the settings otherwise specified.

- 2. Area 0 = 00000H to 1FFFFH, area 1 = 20000H to 3FFFFH
- 3. 01 indicates the year of manufacture and 23, 24, 25 indicate the week of manufacture.  
The products that are guaranteed for 100 rewrites are as follows.  
LQFP package: Products manufactured in 25th week or later (25, 26, 27...)  
FBGA package: Products manufactured in 24th week or later (24, 25, 26...)

**Serial Write Operation Characteristics**

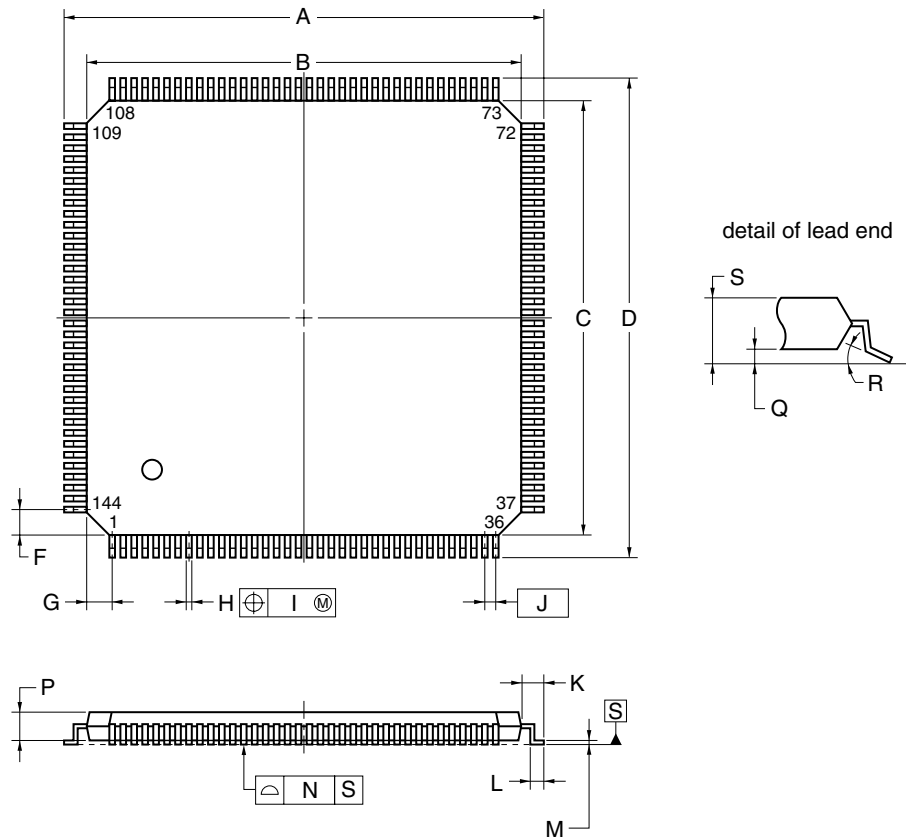
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V <sub>DD</sub> ↑ to V <sub>PP</sub> ↑ set time	<171>	t <sub>DRPSR</sub>	10			μs
V <sub>PP</sub> ↑ to $\overline{\text{RESET}}$ ↑ set time	<172>	t <sub>PSRRF</sub>	1			μs
$\overline{\text{RESET}}$ ↑ to V <sub>PP</sub> count start time	<173>	t <sub>RFOF</sub>	V <sub>PP</sub> = 7.8 V	10T + 1500		ns
Count execution time	<174>	t <sub>COUNT</sub>			15	ms
V <sub>PP</sub> counter high-level width	<175>	t <sub>CH</sub>	1			μs
V <sub>PP</sub> counter low-level width	<176>	t <sub>CL</sub>	1			μs
V <sub>PP</sub> counter rise time	<177>	t <sub>R</sub>			1	μs
V <sub>PP</sub> counter fall time	<178>	t <sub>F</sub>			1	μs
V <sub>PP</sub> ↓ to V <sub>DD</sub> ↓ reset time	<179>	t <sub>PFDR</sub>	10			μs

**Remark** T = t<sub>cyk</sub>



5. PACKAGE DRAWING

144-PIN PLASTIC LQFP (FINE PITCH) (20x20)



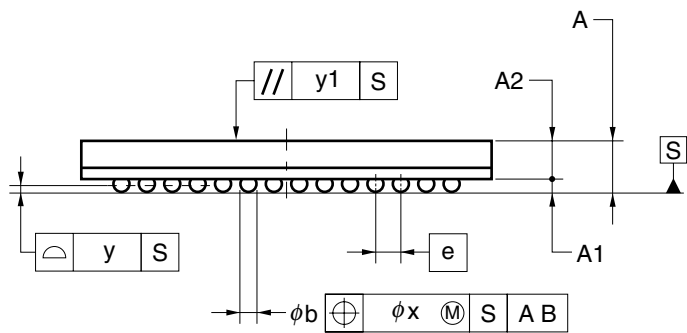
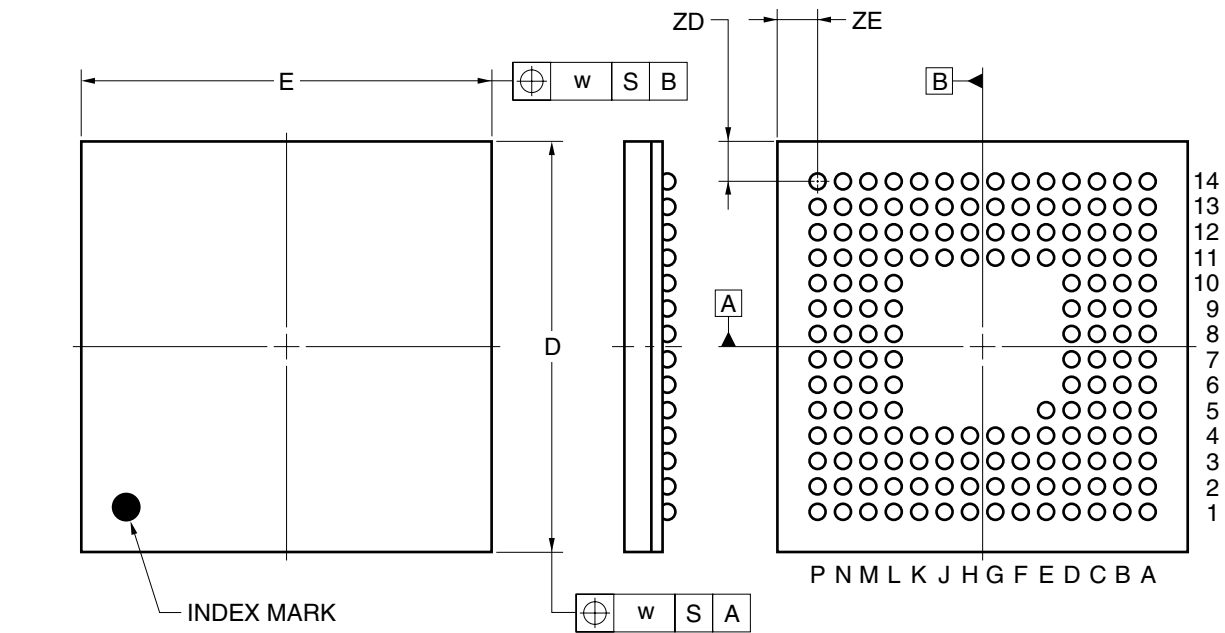
NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	22.0±0.2
B	20.0±0.2
C	20.0±0.2
D	22.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	0.17 <sup>+0.03</sup> <sub>-0.07</sub>
N	0.08
P	1.4
Q	0.10±0.05
R	3° <sup>+4°</sup> <sub>-3°</sub>
S	1.5±0.1

S144GJ-50-UEN

161-PIN PLASTIC FBGA (13x13)



ITEM	MILLIMETERS
D	13.00±0.10
E	13.00±0.10
w	0.20
A	1.48±0.10
A1	0.35±0.06
A2	1.13
e	0.80
b	0.50 <sup>+0.05</sup> <sub>-0.10</sub>
x	0.08
y	0.10
y1	0.20
ZD	1.30
ZE	1.30

P161F1-80-EN4-1

**6. RECOMMENDED SOLDERING CONDITIONS**

The μPD70F3107A and 70F3107A(A) should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

**Table 6-1. Surface Mounting Type Soldering Conditions**

**(1) μPD70F3107AGJ-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 3 days <sup>Note</sup> (after that, prebake at 125°C for 10 to 72 hours)	IR35-103-2
VPS	Package peak temperature: 215°C, Time: 25 to 40 seconds (at 200°C or higher), Count: Two times or less, Exposure limit: 3 days <sup>Note</sup> (after that, prebake at 125°C for 10 to 72 hours)	VP15-103-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

**(2) μPD70F3107AF1-EN4: 161-pin plastic FBGA (13 × 13)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less Exposure limit: 7 days <sup>Note</sup> (after that, prebake at 125°C for 10 to 72 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 25 to 40 seconds (at 200°C or higher), Count: Two times or less, Exposure limit: 7 days <sup>Note</sup> (after that, prebake at 125°C for 10 to 72 hours)	VP15-107-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

**Note** After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

**Caution** Do not use different soldering methods together (except for partial heating).

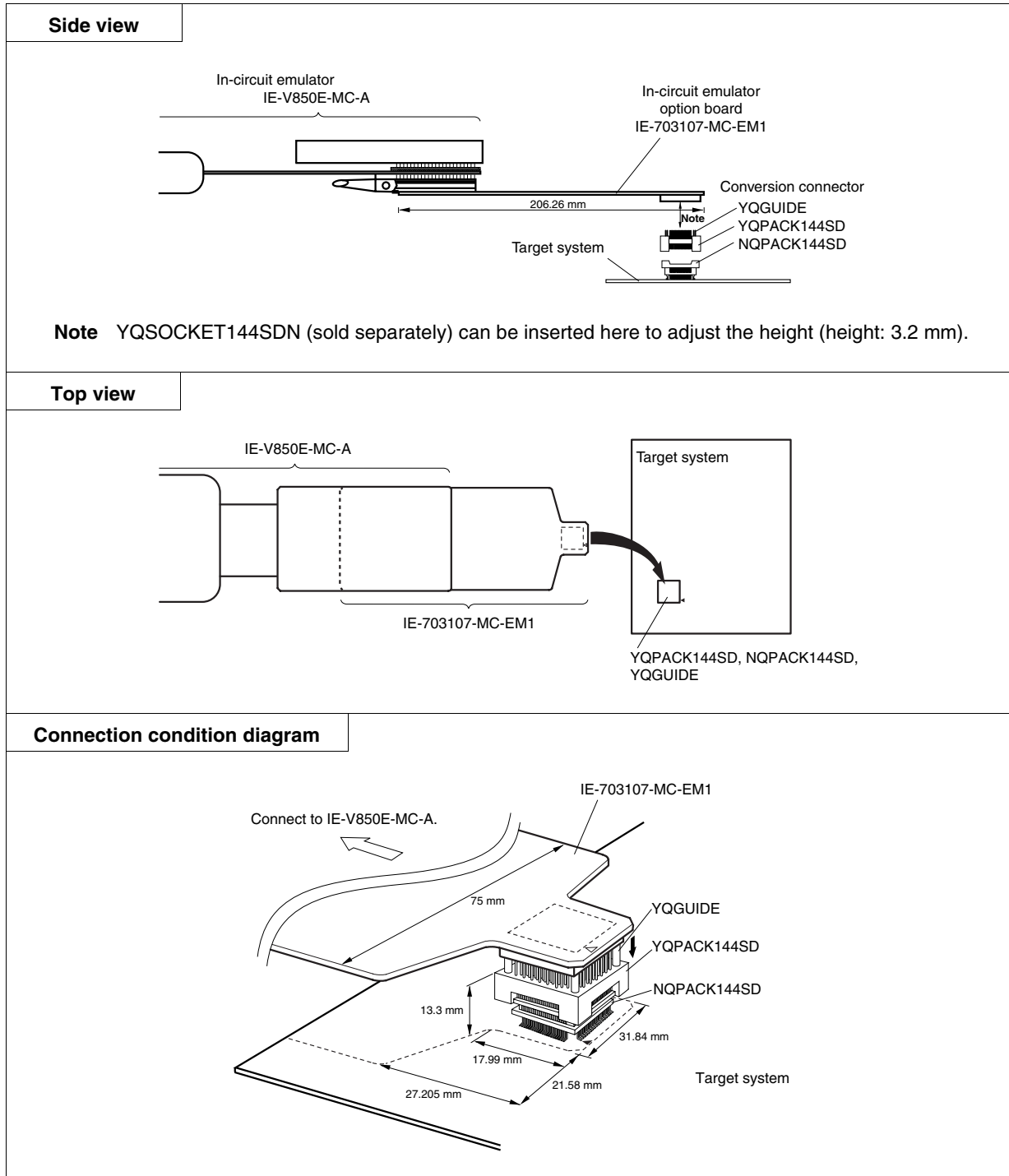
**Remark** The soldering conditions for the following product is undetermined.

- μPD70F3107AGJ(A)-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)

**APPENDIX NOTES ON TARGET SYSTEM DESIGN**

The following shows a diagram of the connection conditions between the in-circuit emulator option board and conversion connector. Design your system making allowances for conditions such as the form of parts mounted on the target system as shown below.

**Appendix-1. 144-pin Plastic LQFP (Fine Pitch) (20 × 20)**



**Remark** The connector for the 161-pin plastic FBGA package is under development.

[MEMO]

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Related document:  $\mu$ PD703103A, 703105A, 703106A, 703106A(A), 703107A, 703107A(A) Data Sheet (U15578E)

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- Availability of related technical literature
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