NEC

MOS INTEGRATED CIRCUIT

μPD70F3107

V850E/MA1™
32-/16-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD70F3107 is a product of the V850 Family™ of 32-bit single-chip microcontrollers for real-time control applications. This microcontroller integrates a 32-bit CPU, ROM, RAM, an interrupt controller, a real-time pulse unit, a serial interface, an A/D converter, a DMA controller, and other functions on a single chip.

The μPD70F3107 is a product that substitutes flash memory for the internal mask ROM of the μPD703107. This enables users to perform on-board program writing and erasure, making this product effective for evaluation during system development, small-lot production of multiple devices, and rapid production start.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

V850E/MA1 User's Manual Hardware: U14359E
V850E1 User's Manual Architecture: U14559E

FEATURES

- Number of instructions: 83
- Minimum instruction execution time: 20 ns (with a 50 MHz internal clock)
- General-purpose registers: 32 bits × 32 registers
- Instruction set suitable for control applications
- Internal memory
  Flash memory: 256 KB
  RAM: 10 KB
- Memory access control (supporting EDO DRAM, SDRAM, and page ROM)
- Sophisticated internal interrupt controller
- Real-time pulse unit suitable for control applications
- Powerful serial interface (with dedicated internal baud rate generator)
- Clock generator
- 10-bit resolution A/D converter: 8 channels
- DMA controller: 4 channels
- Power-saving functions
- Can be replaced with mask ROM-incorporated μPD703105, 703106, or 703107 for mass production

APPLICATIONS

- Office machines (such as ink jet printers, facsimiles, and PPCs)
- Multimedia systems (such as digital still cameras, DVD players, and video printers)

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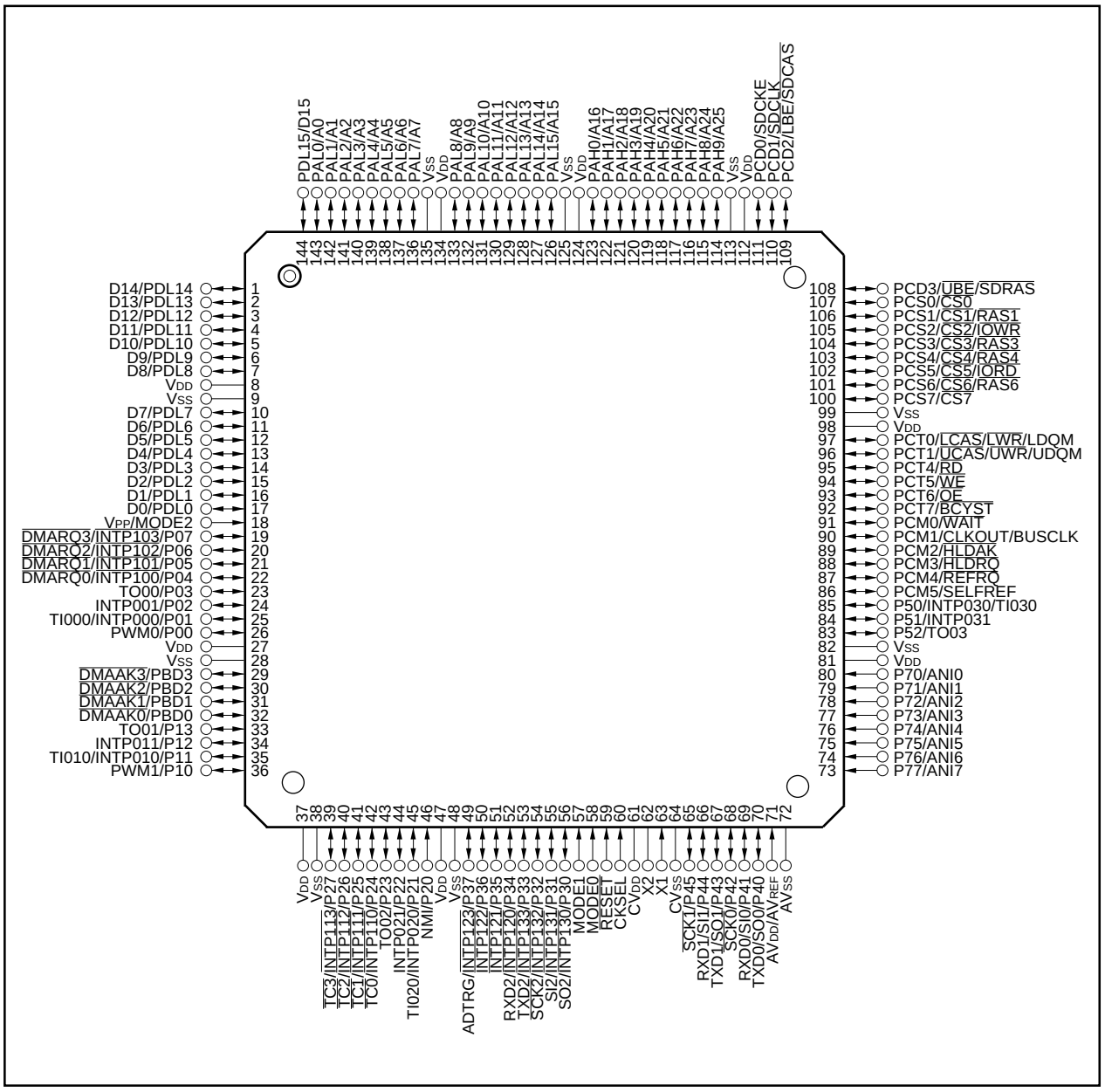
The mark ★ shows major revised points.

ORDERING INFORMATION

Part Number	Package
μPD70F3107GJ-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)

PIN CONFIGURATION (TOP VIEW)

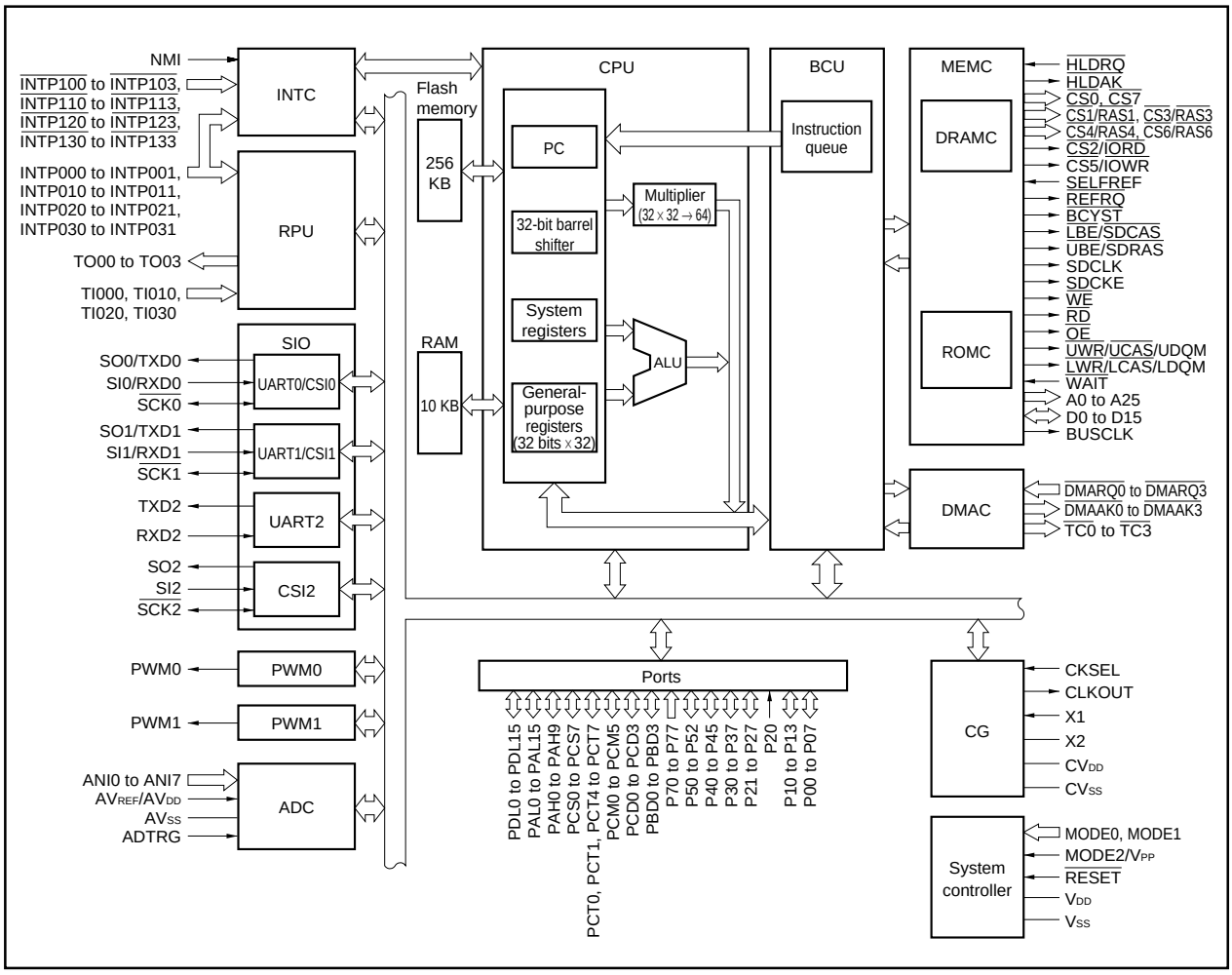
- **144-pin plastic LQFP (fine pitch) (20 × 20)**
  μPD70F3107GJ-UEN



PIN IDENTIFICATION

A0 to A25:	Address Bus	P70 to P77:	Port 7
ADTRG:	AD Trigger Input	PAH0 to PAH9:	Port AH
ANI0 to ANI7:	Analog Input	PAL0 to PAL15:	Port AL
AV_{DD}:	Analog Power Supply	PBD0 to PBD3:	Port BD
AV_{REF}:	Analog Reference Voltage	PCD0 to PCD3:	Port CD
AV_{SS}:	Analog Ground	PCM0 to PCM5:	Port CM
$\overline{BCYST}$:	Bus Cycle Start Timing	PCS0 to PCS7:	Port CS
BUSCLK:	Bus Clock Output	PCT0, PCT1,	
CKSEL:	Clock Generator Operating Mode Select	PCT4 to PCT7:	Port CT
CLKOUT:	Clock Output	PDL0 to PDL15:	Port DL
$\overline{CS0}$ to $\overline{CS7}$:	Chip Select	PWM0, PWM1:	Pulse Width Modulation
CV_{DD}:	Clock Generator Power Supply	$\overline{RAS1}$, $\overline{RAS3}$,	
CV_{SS}:	Clock Generator Ground	$\overline{RAS4}$, $\overline{RAS6}$:	Row Address Strobe
D0 to D15:	Data Bus	$\overline{RD}$:	Read
$\overline{DMAAK0}$ to $\overline{DMAAK3}$:	DMA Acknowledge	$\overline{REFRQ}$:	Refresh Request
$\overline{DMARQ0}$ to $\overline{DMARQ3}$:	DMA Request	$\overline{RESET}$:	Reset
$\overline{HLDAK}$:	Hold Acknowledge	RXD0 to RXD2:	Receive Data
$\overline{HLDRQ}$:	Hold Request	$\overline{SCK0}$ to $\overline{SCK2}$:	Serial Clock
INTP000, INTP001,		$\overline{SDCAS}$:	SDRAM Column Address Strobe
INTP010, INTP011,		SDCKE:	SDRAM Clock Enable
INTP020, INTP021,		SDCLK:	SDRAM Clock Output
INTP030, INTP031,		$\overline{SDRAS}$:	SDRAM Row Address Strobe
★ $\overline{INTP100}$ to $\overline{INTP103}$,		SELFREF:	Self-refresh Request
★ $\overline{INTP110}$ to $\overline{INTP113}$,		SI0 to SI2:	Serial Input
★ $\overline{INTP120}$ to $\overline{INTP123}$,		SO0 to SO2:	Serial Output
★ $\overline{INTP130}$ to $\overline{INTP133}$:	Interrupt Request from Peripherals	$\overline{TC0}$ to $\overline{TC3}$:	Terminal Count Signal
$\overline{IORD}$:	I/O Read Strobe	TI000, TI010,	
$\overline{IOWR}$:	I/O Write Strobe	TI020, TI030:	Timer Input
$\overline{LBE}$:	Lower Byte Enable	TO00 to TO03:	Timer Output
$\overline{LCAS}$:	Lower Column Address Strobe	TXD0 to TXD2:	Transmit Data
LDQM:	Lower DQ Mask Enable	$\overline{UBE}$:	Upper Byte Enable
$\overline{LWR}$:	Lower Write Strobe	$\overline{UCAS}$:	Upper Column Address Strobe
MODE0 to MODE2:	Mode	UDQM:	Upper DQ Mask Enable
NMI:	Non-Maskable Interrupt Request	$\overline{UWR}$:	Upper Write Strobe
$\overline{OE}$:	Output Enable	V_{DD}:	Power Supply for Internal Units
P00 to P07:	Port 0	V_{PP}:	Programming Power Supply
P10 to P13:	Port 1	V_{SS}:	Ground
P20 to P27:	Port 2	$\overline{WAIT}$:	Wait
P30 to P37:	Port 3	$\overline{WE}$:	Write Enable
P40 to P45:	Port 4	X1, X2:	Crystal
P50 to P52:	Port 5		

INTERNAL BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES AMONG PRODUCTS

1.1 Differences Between μPD70F3107 and μPD703105, 703106, 703107

Item \ Product	μPD70F3107	μPD703105	μPD703106	μPD703107
Internal ROM	Flash memory (256 KB)	Mask ROM (128 KB)	Mask ROM (128 KB)	Mask ROM (256 KB)
Internal RAM	10 KB	4 KB	10 KB	10 KB
Flash memory programming pin	Provided (V_{PP})	None		
Flash memory programming mode	Provided (MODE0 = H/L, MODE1 = H, MODE2/V_{PP} = 7.8 V)	None		
Electrical specifications	Current consumption etc. differs (see individual data sheets).			
Other	Circuit scale and mask layout differ, thus noise immunity, noise radiation, etc. differ.			

Cautions 1. There are differences in noise immunity and noise radiation between the flash memory version and mask ROM version. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluation for commercial samples (not engineering samples) of the mask ROM version.

2. When switching from the flash memory version to the mask ROM version, write the same code to the free area of the internal ROM.

2. PIN FUNCTIONS

2.1 Port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function
P00	I/O	Port 0 8-bit I/O port Input/output mode can be specified in 1-bit units.	PWM0
P01			TI000/INTP000
P02			INTP001
P03			TO00
P04			$\overline{\text{DMARQ0}}$/$\overline{\text{INTP100}}$
P05			$\overline{\text{DMARQ1}}$/$\overline{\text{INTP101}}$
P06			$\overline{\text{DMARQ2}}$/$\overline{\text{INTP102}}$
P07			$\overline{\text{DMARQ3}}$/$\overline{\text{INTP103}}$
P10	I/O	Port 1 4-bit I/O port Input/output mode can be specified in 1-bit units.	PWM1
P11			INTP010/TI010
P12			INTP011
P13			TO01
P20	Input	Port 2 P20 is an input-only port. If a valid edge is input, it operates as an NMI input. Also, the status of the NMI input is shown by bit 0 of the P2 register. P21 to P27 is a 7-bit I/O port. Input/output mode can be specified in 1-bit units.	NMI
P21	I/O		INTP020/TI020
P22			INTP021
P23			TO02
P24			$\overline{\text{TC0}}$/$\overline{\text{INTP110}}$
P25			$\overline{\text{TC1}}$/$\overline{\text{INTP111}}$
P26			$\overline{\text{TC2}}$/$\overline{\text{INTP112}}$
P27			$\overline{\text{TC3}}$/$\overline{\text{INTP113}}$
P30	I/O	Port 3 8-bit I/O port Input/output mode can be specified in 1-bit units.	SO2/$\overline{\text{INTP130}}$
P31			SI2/$\overline{\text{INTP131}}$
P32			$\overline{\text{SCK2}}$/$\overline{\text{INTP132}}$
P33			TXD2/$\overline{\text{INTP133}}$
P34			RXD2/$\overline{\text{INTP120}}$
P35			$\overline{\text{INTP121}}$
P36			$\overline{\text{INTP122}}$
P37			ADTRG/$\overline{\text{INTP123}}$
P40	I/O	Port 4 6-bit I/O port Input/output mode can be specified in 1-bit units.	TXD0/SO0
P41			RXD0/SI0
P42			$\overline{\text{SCK0}}$
P43			TXD1/SO1
P44			RXD1/SI1
P45			$\overline{\text{SCK1}}$
P50	I/O	Port 5 3-bit I/O port Input/output mode can be specified in 1-bit units.	INTP030/TI030
P51			INTP031
P52			TO03

(2/2)

Pin Name	I/O	Function	Alternate Function
P70 to P77	Input	Port 7 8-bit input-only port	ANI0 to ANI7
PBD0 to PBD3	I/O	Port BD 4-bit I/O port Input/output mode can be specified in 1-bit units.	$\overline{\text{DMAAK0}}$ to $\overline{\text{DMAAK3}}$
PCM0	I/O	Port CM 6-bit I/O port Input/output mode can be specified in 1-bit units.	$\overline{\text{WAIT}}$
PCM1			CLKOUT/BUSCLK
PCM2			$\overline{\text{HLDAK}}$
PCM3			$\overline{\text{HLDRQ}}$
PCM4			$\overline{\text{REFRQ}}$
PCM5			SELFREF
PCT0	I/O	Port CT 6-bit I/O port Input/output mode can be specified in 1-bit units.	$\overline{\text{LCAS}}$/$\overline{\text{LWR}}$/LDQM
PCT1			$\overline{\text{UCAS}}$/$\overline{\text{UWR}}$/UDQM
PCT4			$\overline{\text{RD}}$
PCT5			$\overline{\text{WE}}$
PCT6			$\overline{\text{OE}}$
PCT7			$\overline{\text{BCYST}}$
PCS0	I/O	Port CS 8-bit I/O port Input/output mode can be specified in 1-bit units.	$\overline{\text{CS0}}$
PCS1			$\overline{\text{CS1}}$/$\overline{\text{RAS1}}$
PCS2			$\overline{\text{CS2}}$/IOWR
PCS3			$\overline{\text{CS3}}$/$\overline{\text{RAS3}}$
PCS4			$\overline{\text{CS4}}$/$\overline{\text{RAS4}}$
PCS5			$\overline{\text{CS5}}$/IORD
PCS6			$\overline{\text{CS6}}$/$\overline{\text{RAS6}}$
PCS7			$\overline{\text{CS7}}$
PCD0	I/O	Port CD 4-bit I/O port Input/output mode can be specified in 1-bit units.	SDCKE
PCD1			SDCLK
PCD2			$\overline{\text{LBE}}$/$\overline{\text{SDCAS}}$
PCD3			$\overline{\text{UBE}}$/$\overline{\text{SDRAS}}$
PAH0 to PAH9	I/O	Port AH 8-/10-bit I/O port Input/output mode can be specified in 1-bit units.	A16 to A25
PAL0 to PAL15	I/O	Port AL 8-/16-bit I/O port Input/output mode can be specified in 1-bit units.	A0 to A15
PDL0 to PDL15	I/O	Port DL 8-/16-bit I/O port Input/output mode can be specified in 1-bit units.	D0 to D15

2.2 Non-Port Pins

(1/3)

Pin Name	I/O	Function	Alternate Function
TO00	Output	Pulse signal output of timer C0 to C3	P03
TO01			P13
TO02			P23
TO03			P52
TI000	Input	External count input of timer C0 to C3	P01/INTP000
TI010			P11/INTP010
TI020			P21/INTP020
TI030			P50/INTP030
INTP000	Input	External maskable interrupt request input, or timer C0 external capture trigger input	P01/TI000
INTP001			P02
INTP010	Input	External maskable interrupt request input, or timer C1 external capture trigger input	P11/TI010
INTP011			P12
INTP020	Input	External maskable interrupt request input, or timer C2 external capture trigger input	P21/TI020
INTP021			P22
INTP030	Input	External maskable interrupt request input, or timer C3 external capture trigger input	P50/TI030
INTP031			P51
★ $\overline{\text{INTP100}}$	Input	External maskable interrupt request input	P04/$\overline{\text{DMARQ0}}$
★ $\overline{\text{INTP101}}$			P05/$\overline{\text{DMARQ1}}$
★ $\overline{\text{INTP102}}$			P06/$\overline{\text{DMARQ2}}$
★ $\overline{\text{INTP103}}$			P07/$\overline{\text{DMARQ3}}$
★ $\overline{\text{INTP110}}$			P24/$\overline{\text{TC0}}$
★ $\overline{\text{INTP111}}$			P25/$\overline{\text{TC1}}$
★ $\overline{\text{INTP112}}$			P26/$\overline{\text{TC2}}$
★ $\overline{\text{INTP113}}$			P27/$\overline{\text{TC3}}$
★ $\overline{\text{INTP120}}$			P34/RXD2
★ $\overline{\text{INTP121}}$			P35
★ $\overline{\text{INTP122}}$			P36
★ $\overline{\text{INTP123}}$			P37/ADTRG
★ $\overline{\text{INTP130}}$			P30/SO2
★ $\overline{\text{INTP131}}$			P31/SI2
★ $\overline{\text{INTP132}}$			P32/$\overline{\text{SCK2}}$
★ $\overline{\text{INTP133}}$			P33/TXD2
SO0	Output	CSI0 to CSI2 serial transmission data output (3-wire)	P40/TXD0
SO1			P43/TXD1
SO2			P30/$\overline{\text{INTP130}}$
SI0	Input	CSI0 to CSI2 serial reception data input (3-wire)	P41/RXD0
SI1			P44/RXD1
SI2			P31/$\overline{\text{INTP131}}$

(2/3)

Pin Name	I/O	Function	Alternate Function
$\overline{SCK0}$	I/O	CSI0 to CSI2 serial clock I/O (3-wire)	P42
$\overline{SCK1}$			P45
$\overline{SCK2}$			P32/$\overline{INTP132}$
TXD0	Output	UART0 to UART2 serial transmission data output	P40/SO0
TXD1			P43/SO1
TXD2			P33/$\overline{INTP133}$
RXD0	Input	UART0 to UART2 serial reception data input	P41/SI0
RXD1			P44/SI1
RXD2			P34/$\overline{INTP120}$
PWM0	Output	PWM pulse signal output	P00
PWM1			P10
ANI0 to ANI7	Input	Analog inputs to the A/D converter	P70 to P77
ADTRG	Input	A/D converter external trigger input	P37/$\overline{INTP123}$
$\overline{DMARQ0}$	Input	DMA request signal input	P04/$\overline{INTP100}$
$\overline{DMARQ1}$			P05/$\overline{INTP101}$
$\overline{DMARQ2}$			P06/$\overline{INTP102}$
$\overline{DMARQ3}$			P07/$\overline{INTP103}$
$\overline{DMAAK0}$	Output	DMA acknowledge signal output	PBD0
$\overline{DMAAK1}$			PBD1
$\overline{DMAAK2}$			PBD2
$\overline{DMAAK3}$			PBD3
$\overline{TC0}$	Output	DMA transfer termination (terminal count) signal output	P24/$\overline{INTP110}$
$\overline{TC1}$			P25/$\overline{INTP111}$
$\overline{TC2}$			P26/$\overline{INTP112}$
$\overline{TC3}$			P27/$\overline{INTP113}$
NMI	Input	Non-maskable interrupt request signal input	P20
MODE0	Input	V850E/MA1 operating mode specification	–
MODE1			–
MODE2			V_{PP}
V_{PP}	Input	Flash memory programming power-supply application pin	MODE2
$\overline{WAIT}$	Input	Control signal input that inserts a wait in the bus cycle	PCM0
$\overline{HLDAK}$	Output	Bus hold acknowledge output	PCM2
$\overline{HLDRQ}$	Input	Bus hold request input	PCM3
$\overline{REFRQ}$	Output	Refresh request signal output for DRAM	PCM4
SELFREF	Input	Self refresh request input for DRAM	PCM5
$\overline{LCAS}$	Output	Column address strobe signal output for DRAM lower data	PCT0/$\overline{LWR}$/LDQM
$\overline{UCAS}$	Output	Column address strobe signal output for DRAM higher data	PCT1/$\overline{UWR}$/UDQM
$\overline{LWR}$	Output	External data lower byte write enable signal output	PCT0/$\overline{LCAS}$/LDQM
$\overline{UWR}$	Output	External data higher byte write enable signal output	PCT1/$\overline{UCAS}$/UDQM

(3/3)

Pin Name	I/O	Function	Alternate Function
LDQM	Output	Output disable/write mask signal output for SDRAM lower data	PCT0/$\overline{\text{LCAS}}$/$\overline{\text{LWR}}$
UDQM	Output	Output disable/write mask signal output for SDRAM higher data	PCT1/$\overline{\text{UCAS}}$/$\overline{\text{UWR}}$
$\overline{\text{RD}}$	Output	External data bus read strobe signal output	PCT4
$\overline{\text{WE}}$	Output	Write enable signal output for DRAM	PCT5
$\overline{\text{OE}}$	Output	Output enable signal output for DRAM	PCT6
$\overline{\text{BCYST}}$	Output	Strobe signal output that shows the start of the bus cycle	PCT7
$\overline{\text{CS0}}$	Output	Chip select signal output	PCS0
$\overline{\text{CS1}}$			PCS1/$\overline{\text{RAS1}}$
$\overline{\text{CS2}}$			PCS2/$\overline{\text{IOWR}}$
$\overline{\text{CS3}}$			PCS3/$\overline{\text{RAS3}}$
$\overline{\text{CS4}}$			PCS4/$\overline{\text{RAS4}}$
$\overline{\text{CS5}}$			PCS5/$\overline{\text{IORD}}$
$\overline{\text{CS6}}$			PCS6/$\overline{\text{RAS6}}$
$\overline{\text{CS7}}$			PCS7
$\overline{\text{RAS1}}$	Output	Row address strobe signal output for DRAM	PCS1/$\overline{\text{CS1}}$
$\overline{\text{RAS3}}$			PCS3/$\overline{\text{CS3}}$
$\overline{\text{RAS4}}$			PCS4/$\overline{\text{CS4}}$
$\overline{\text{RAS6}}$			PCS6/$\overline{\text{CS6}}$
$\overline{\text{IOWR}}$	Output	DMA write strobe signal output	PCS2/$\overline{\text{CS2}}$
$\overline{\text{IORD}}$	Output	DMA read strobe signal output	PCS5/$\overline{\text{CS5}}$
SDCKE	Output	SDRAM clock enable signal output	PCD0
SDCLK	Output	SDRAM clock signal output	PCD1
$\overline{\text{SDCAS}}$	Output	Column address strobe signal output for SDRAM	PCD2/$\overline{\text{LBE}}$
$\overline{\text{SDRAS}}$	Output	Row address strobe signal output for SDRAM	PCD3/$\overline{\text{UBE}}$
$\overline{\text{LBE}}$	Output	External data bus lower byte enable signal output	PCD2/$\overline{\text{SDCAS}}$
$\overline{\text{UBE}}$	Output	External data bus higher byte enable signal output	PCD3/$\overline{\text{SDRAS}}$
D0 to D15	I/O	16-bit data bus for external memory	PDL0 to PDL15
A0 to A15	Output	26-bit address bus for external memory	PAL0 to PAL15
A16 to A25			PAH0 to PAH9
$\overline{\text{RESET}}$	Input	System reset input	–
X1	Input	Connects the crystal resonator for system clock oscillation. In the case of an external source supplying the clock, it is input to X1.	–
X2	–		–
CLKOUT	Output	System clock output	PCM1/BUSCLK
BUSCLK	Output	Bus clock output	PCM1/CLKOUT
CKSEL	Input	Input which specifies the clock generator's operating mode	–
AV_{REF}	Input	Reference voltage applied to A/D converter	AV_{DD}
AV_{DD}	–	Positive power supply for A/D converter	AV_{REF}
AV_{SS}	–	Ground potential for A/D converter	–
CV_{DD}	–	Positive power supply for the dedicated clock generator	–
CV_{SS}	–	Ground potential for the dedicated clock generator	–
V_{DD}	–	Positive power supply	–
V_{SS}	–	Ground potential	–

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 2-1.

The input/output circuit configuration of each type is schematically shown in Figure 2-1.

It is recommended that 1 to 10 kΩ resistors be used when connecting to V_{DD} or V_{SS} via a resistor.

Table 2-1. Types of Pin I/O Circuits and Recommended Connection (1/2)

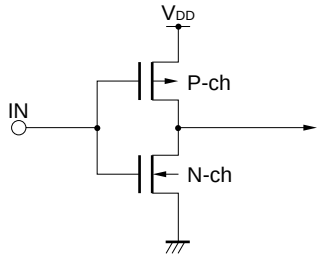
Pin Name	I/O Circuit Type	Recommended Connection
P00/PWM0	5	Input: Independently connect to V_{DD} or V_{SS} via a resistor Output: Leave open
P01/INTP000/TI000	5-AC	
P02/INTP001		
P03/TO00	5	
P04/$\overline{\text{DMARQ0}}$/$\overline{\text{INTP100}}$ to P07/$\overline{\text{DMARQ3}}$/$\overline{\text{INTP103}}$	5-AC	
P10/PWM1	5	
P11/INTP010/TI010	5-AC	
P12/INTP011		
P13/TO01	5	
P20/NMI	2	Connect to V_{SS} directly.
P21/INTP020/TI020	5-AC	Input: Independently connect to V_{DD} or V_{SS} via a resistor Output: Leave open
P22/INTP021		
P23/TO02	5	
P24/$\overline{\text{TC0}}$/$\overline{\text{INTP110}}$ to P27/$\overline{\text{TC3}}$/$\overline{\text{INTP113}}$	5-AC	
P30/SO2/$\overline{\text{INTP130}}$		
P31/SI2/$\overline{\text{INTP131}}$		
P32/$\overline{\text{SCK2}}$/$\overline{\text{INTP132}}$		
P33/TXD2/$\overline{\text{INTP133}}$		
P34/RXD2/$\overline{\text{INTP120}}$		
P35/$\overline{\text{INTP121}}$		
P36/$\overline{\text{INTP122}}$		
P37/ADTRG/$\overline{\text{INTP123}}$		
P40/TXD0/SO0	5	
P41/RXD0/SI0	5-AC	
P42/$\overline{\text{SCK0}}$		
P43/TXD1/SO1	5	
P44/RXD1/SI1	5-AC	
P45/$\overline{\text{SCK1}}$		
P50/INTP030/TI030		
P51/INTP031		
P52/TO03	5	
P70/ANI0 to P77/ANI7	9	Connect to V_{SS} directly.
PBD0/$\overline{\text{DMAAK0}}$ to PBD3/$\overline{\text{DMAAK3}}$	5	Input: Independently connect to V_{DD} or V_{SS} via a resistor Output: Leave open

Table 2-1. Types of Pin I/O Circuits and Recommended Connection (2/2)

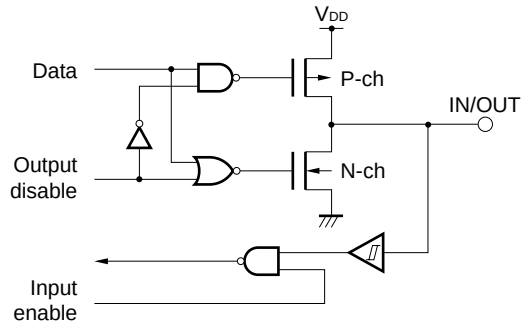
Pin Name	I/O Circuit Type	Recommended Connection
PCM0/$\overline{\text{WAIT}}$	5	Input: Independently connect to V_{DD} via a resistor
PCM1/CLKOUT/BUSCLK	5	Input: Independently connect to V_{DD} or V_{SS} via a resistor Output: Leave open
PCM2/$\overline{\text{HLDAK}}$		
PCM3/$\overline{\text{HLDRQ}}$	5	Input: Independently connect to V_{DD} via a resistor
PCM4/$\overline{\text{REFRQ}}$	5	Input: Independently connect to V_{DD} or V_{SS} via a resistor Output: Leave open
PCM5/SELFREF	5	Input: Independently connect to V_{SS} via a resistor
PCT0/$\overline{\text{LCAS}}$/$\overline{\text{LWR}}$/LDQM	5	Input: Independently connect to V_{DD} or V_{SS} via a resistor Output: Leave open
PCT1/$\overline{\text{UCAS}}$/$\overline{\text{UWR}}$/UDQM		
PCT4/$\overline{\text{RD}}$		
PCT5/$\overline{\text{WE}}$		
PCT6/$\overline{\text{OE}}$		
PCT7/$\overline{\text{BCYST}}$		
PCS0/$\overline{\text{CS0}}$		
PCS1/$\overline{\text{CS1}}$/$\overline{\text{RAS1}}$		
PCS2/$\overline{\text{CS2}}$/$\overline{\text{IOWR}}$		
PCS3/$\overline{\text{CS3}}$/$\overline{\text{RAS3}}$		
PCS4/$\overline{\text{CS4}}$/$\overline{\text{RAS4}}$		
PCS5/$\overline{\text{CS5}}$/$\overline{\text{IORD}}$		
PCS6/$\overline{\text{CS6}}$/$\overline{\text{RAS6}}$		
PCS7/$\overline{\text{CS7}}$		
PCD0/SDCKE		
PCD1/SDCLK		
PCD2/$\overline{\text{LBE}}$/$\overline{\text{SDCAS}}$		
PCD3/$\overline{\text{UBE}}$/$\overline{\text{SDRAS}}$		
PAH0/A16 to PAH9/A25		
PAL0/A0 to PAL15/A15		
PDL0/D0 to PDL15/D15		
MODE0, MODE1	2	–
MODE2/V_{PP}		
$\overline{\text{RESET}}$	2	Connect to V_{SS}.
CKSEL	1	Connect to V_{DD}.
AV_{SS}	–	Connect to V_{SS}.
AV_{DD}/AV_{REF}	–	Connect to V_{DD}.

Figure 2-1. Pin I/O Circuits

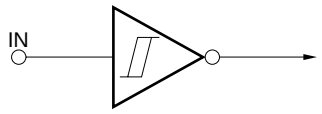
Type 1



Type 5-AC

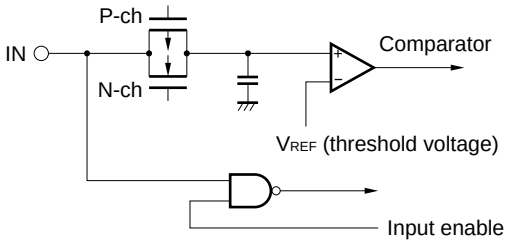


Type 2

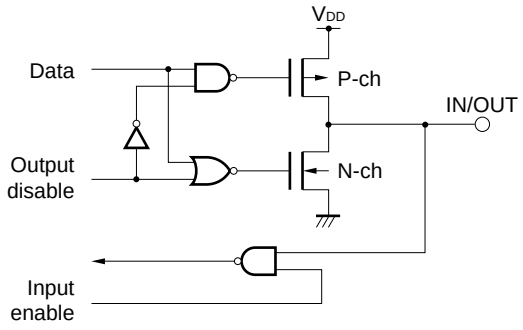


Schmitt-triggered input with hysteresis characteristics

Type 9



Type 5



3. FLASH MEMORY PROGRAMMING

The following two flash memory programming methods are available.

(1) On-board programming

The program is written to the flash memory using the dedicated flash programmer after the μPD70F3107 is mounted on the target board. Install the connectors, etc., required for communication with the dedicated flash programmer, on the target board.

(2) Off-board programming

The program is written to the flash memory using the dedicated adapter before the μPD70F3107 is mounted on the target board.

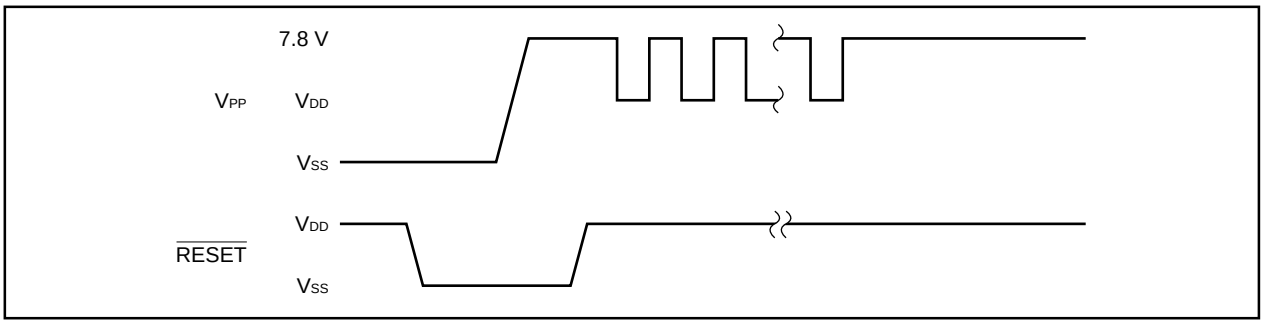
3.1 Selection of Communication Mode

Writing to the flash memory is done via serial communication using the dedicated flash programmer. Select one of the communication modes listed in Table 3-1. Base selection of the communication mode on the selection format shown in Figure 3-1. Refer to the number of V_{PP} pulses shown in Table 3-1 when selecting the communication mode.

Table 3-1. Communication Modes

Communication Mode	Pins Used	Number of V_{PP} Pulses
CSI0	SO0 (serial data output) SI0 (serial data input) $\overline{SCK0}$ (serial clock input)	0
Handshake-supporting CSI	SO0 (serial data output) SI0 (serial data input) $\overline{SCK0}$ (serial clock input) PAL0 (signal for handshake)	3

Figure 3-1. Communication Mode Selection Format



3.2 Flash Memory Programming Functions

Flash memory programming is performed by sending and receiving commands and data according to the selected communication mode. Table 3-2 shows the main flash memory programming functions.

Table 3-2. Main Flash Memory Programming Functions

Function	Description
Batch erase	Erases the contents of the entire memory.
Area erase	Erases memory contents 128 KB at a time.
Batch blank check	Checks whether the entire memory has been erased.
Data write	Writes data to flash memory based on the write start address and the number of bytes to be written.
Batch verify	Compares the contents of the entire memory with the input data.

3.3 Connecting Dedicated Flash Programmer

The connection of the dedicated flash programmer to the μPD70F3107 differs depending on the communication mode.

Figure 3-2. Connection of Dedicated Flash Programmer for CSI0 Mode

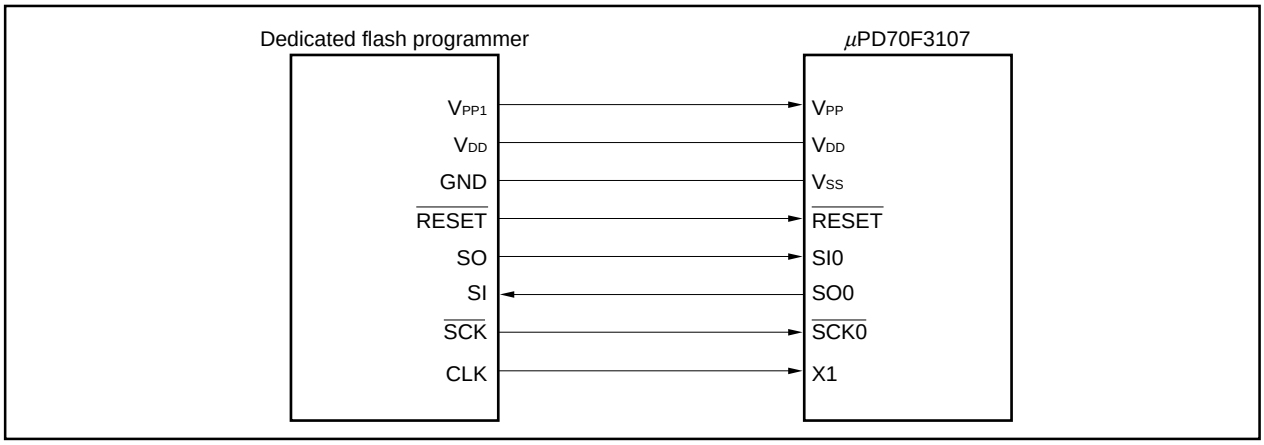
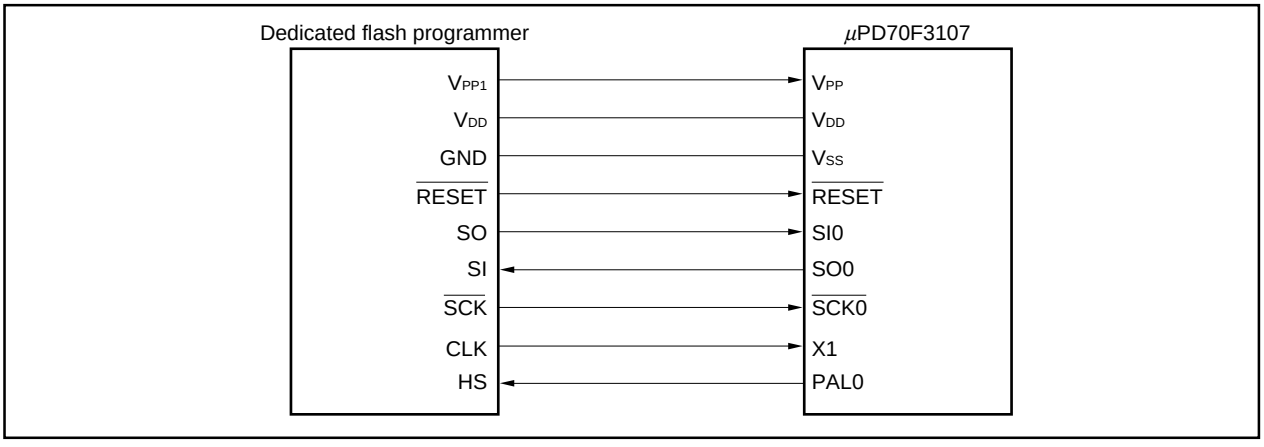


Figure 3-3. Connection of Dedicated Flash Programmer for Handshake-Supporting CSI Mode



4. ELECTRICAL SPECIFICATIONS

4.1 Normal Operation Mode

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}	V_{DD} pin	–0.5 to +4.6	V
	CV_{DD}	CV_{DD} pin	–0.5 to +4.6	V
	CV_{SS}	CV_{SS} pin	–0.5 to +0.5	V
	AV_{DD}	AV_{DD} pin	–0.5 to +4.6	V
	AV_{SS}	AV_{SS} pin	–0.5 to +0.5	V
Input voltage	V_I	X1 pin, except MODE2/V_{PP} pin	–0.5 to +6.0	V
		MODE2/V_{PP} pin	–0.5 to +8.5	V
		MODE2/V_{PP} pin in flash memory programming mode	–0.5 to +11.0	V
Clock input voltage	V_K	X1, V_{DD} = 3.3 V ±0.3 V	–0.5 to V_{DD} + 1.0	V
Output current, low	I_{OL}	Per pin	4.0	mA
		Total of all pins	100	mA
Output current, high	I_{OH}	Per pin	–4.0	mA
		Total of all pins	–100	mA
Output voltage	V_O	V_{DD} = 3.3 V ±0.3 V	–0.5 to V_{DD} + 0.5	V
Analog input voltage	V_{WASN}	ANI0 to ANI7, V_{DD} = 3.3 V ±0.3 V	–0.3 to AV_{DD} + 0.3	V
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–60 to +150	°C

Cautions 1. Do not directly connect output (or I/O) pins of IC products to each other, or to V_{DD}, V_{CC}, and GND. Open drain pins or open collector pins, however, can be directly connected to each other. Direct connection of the output pins between an IC product and an external circuit is possible, if the output pins can be set to the high-impedance state and the output timing of the external circuit is designed to avoid output conflict.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions shown below for DC characteristics and AC characteristics are within the range for normal operation and quality assurance.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz			15	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V.			15	pF
Output capacitance	C_O				15	pF

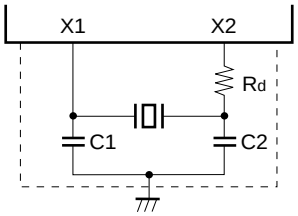
Operating Conditions

Operation Mode	Internal Operation Clock Frequency (ϕ)	Operating Ambient Temperature (T_A)	Power Supply Voltage (V_{DD})
Direct mode	4 to 25 MHz	–40 to +85°C	V_{DD} = 3.3 V ±0.3 V
PLL mode	4 to 50 MHz	–40 to +85°C	V_{DD} = 3.3 V ±0.3 V

Recommended Oscillator

(a) Ceramic resonator

(i) Murata Mfg. Co., Ltd. (T_A = –40 to +85°C)



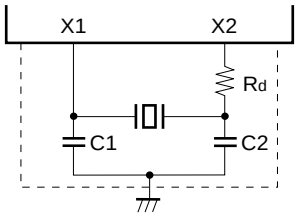
Type	Product	Oscillation Frequency	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.)
		f_{XX} (MHz)	C1 (pF)	C2 (pF)	R_d (kΩ)	MIN. (V)	MAX. (V)	T_{OST} (ms)
Surface mount	CSTCC4.00MG0H6	4.0	On-chip	On-chip	0	3.0	3.6	0.09
	CSTCC5.00MG0H6	5.0	On-chip	On-chip	0	3.0	3.6	0.09
Lead	CSA4.00MG	4.0	30	30	0	3.0	3.6	0.05
	CST4.00MGW	4.0	On-chip	On-chip	0	3.0	3.6	0.05
	CSTS0400MG06	4.0	On-chip	On-chip	0	3.0	3.6	0.11
	CSA5.00MG	5.0	30	30	0	3.0	3.6	0.05
	CST5.00MGW	5.0	On-chip	On-chip	0	3.0	3.6	0.05
	CSTS0500MG06	5.0	On-chip	On-chip	0	3.0	3.6	0.11

Cautions 1. Connect the oscillator as closely to the X1 and X2 pins as possible.

2. Do not wire any other signal lines in the area indicated by the broken lines.

3. Thoroughly evaluate the matching between the μPD70F3107 and the resonator.

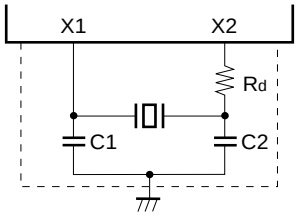
(ii) TDK (T_A = –40 to +85°C)



Type	Product	Oscillation Frequency	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.)
		f_{XX} (MHz)	C1 (pF)	C2 (pF)	R_d (kΩ)	MIN. (V)	MAX. (V)	T_{OST} (ms)
Surface mount	CCR4.0MC3	4.0	On-chip	On-chip	0	3.0	3.6	0.3
	CCR5.0MC3	5.0	On-chip	On-chip	0	3.0	3.6	0.3

Cautions 1. Connect the oscillator as closely to the X1 and X2 pins as possible.
2. Do not wire any other signal lines in the area indicated by the broken lines.
3. Thoroughly evaluate the matching between the μPD70F3107 and the resonator.

(iii) Kyocera Corporation (T_A = –20 to +80°C)

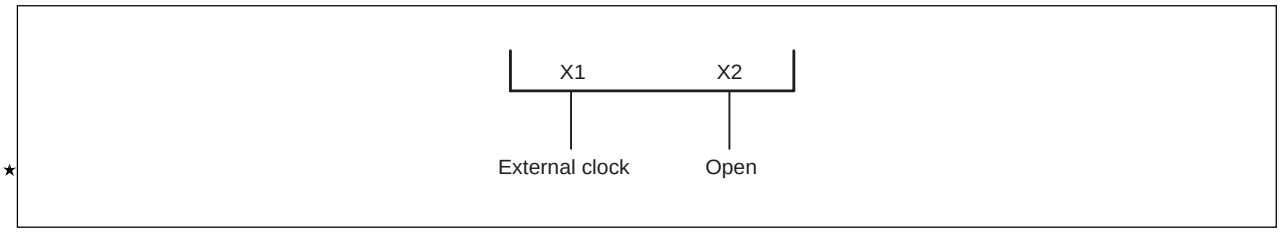


Type	Product	Oscillation Frequency	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.)
		f_{XX} (MHz)	C1 (pF)	C2 (pF)	R_d (kΩ)	MIN. (V)	MAX. (V)	T_{OST} (ms)
Surface mount	PBRC4.00AR-A	4.0	33	33	0	3.0	3.6	0.11
	PBRC4.00BR-A	4.0	On-chip	On-chip	0	3.0	3.6	0.11
	PBRC5.00AR-A	5.0	33	33	0	3.0	3.6	0.08
	PBRC5.00BR-A	5.0	On-chip	On-chip	0	3.0	3.6	0.08
Lead	KBR-4.0MSB	4.0	33	33	0	3.0	3.6	0.11
	KBR-4.0MKC	4.0	On-chip	On-chip	0	3.0	3.6	0.11
	KBR-5.0MSB	5.0	33	33	0	3.0	3.6	0.08
	KBR-5.0MKC	5.0	On-chip	On-chip	0	3.0	3.6	0.08

Cautions 1. Connect the oscillator as closely to the X1 and X2 pins as possible.
2. Do not wire any other signal lines in the area indicated by the broken lines.
3. Thoroughly evaluate the matching between the μPD70F3107 and the resonator.

(b) External clock input (T_A = –40 to +85°C)

★



DC Characteristics (T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V, V_{SS} = 0 V)

	Parameter		Symbol	Conditions		MIN.	TYP.	MAX.	Unit
★	Input voltage, high		V_{IH}	Except for **Note 1**		2.0		5.5	V
★				**Note 1**		0.75V_{DD}		5.5	V
	Input voltage, low		V_{IL}	Except for **Note 1**		–0.5		0.8	V
				Note 1		–0.5		0.2V_{DD}	V
	Clock input voltage, high		V_{XH}	X1 pin	Direct mode	0.8V_{DD}		V_{DD} + 0.3	V
					PLL mode	0.8V_{DD}		V_{DD} + 0.3	V
	Clock input voltage, low		V_{XL}	X1 pin	Direct mode	–0.5		0.15V_{DD}	V
					PLL mode	–0.5		0.15V_{DD}	V
	Schmitt-triggered input threshold voltage		V_T^+	**Note 1**, rising edge			2.0		V
			V_T^-	**Note 1**, falling edge			1.0		V
	Schmitt-triggered input hysteresis width		$V_T^+ - V_T^-$	**Note 1**		0.3			V
	Output voltage, high		V_{OH}	I_{OH} = –2.5 mA		0.8V_{DD}			V
				I_{OH} = –100 μA		V_{DD} – 0.4			V
	Output voltage, low		V_{OL}	I_{OL} = 2.5 mA				0.45	V
	Input leakage current, high		I_{LIH}	$V_I = V_{DD}$, except for **Note 2**				10	μA
	Input leakage current, low		I_{LIL}	V_I = 0 V, except for **Note 2**				–10	μA
	Output leakage current, high		I_{LOH}	$V_O = V_{DD}$				10	μA
	Output leakage current, low		I_{LOL}	V_O = 0 V				–10	μA
	Analog pin input leakage current		I_{LWASN}	**Note 2**				±10	μA
★	V_{PP} supply voltage		V_{PP0}	During normal operation		0		0.2V_{DD}	V
★	Power supply current	During normal operation	I_{DD1}	Direct mode			3.2 × f_X + 30	4.8 × f_X + 45	mA
★				PLL mode			3.2 × f_X + 30	4.8 × f_X + 45	mA
★		In HALT mode	I_{DD2}	Direct mode			1.6 × f_X + 20	2.4 × f_X + 30	mA
★				PLL mode			1.6 × f_X + 20	2.4 × f_X + 30	mA
★		In IDLE mode	I_{DD3}	Direct mode			10	30	mA
★				PLL mode			10	30	mA
		In STOP mode	I_{DD4}	–40°C ≤ T_A ≤ +40°C			10	60	μA
★				40°C < T_A ≤ 85°C				600	μA

Notes 1. P01/TI000/INTP000, P02/INTP001, P04/DMARQ0/INTP100 to P07/DMARQ3/INTP103, P11/TI010/INTP010, P12/INTP011, P21/TI020/INTP020, P22/INTP021, P24/TC0/INTP110 to P27/TC3/INTP113, P30/SO2/INTP130, P31/SI2/INTP131, P32/SCK2/INTP132, P33/TXD2/INTP133, P34/RXD2/INTP120, P35/INTP121, P36/INTP122, P37/ADTRG/INTP123, P41/RXD0/SI0, P42/SCK0, P44/RXD1/SI1, P45/SCK1, P50/TI030/INTP030, P51/INTP031

2. P70/ANI0 to P77/ANI7

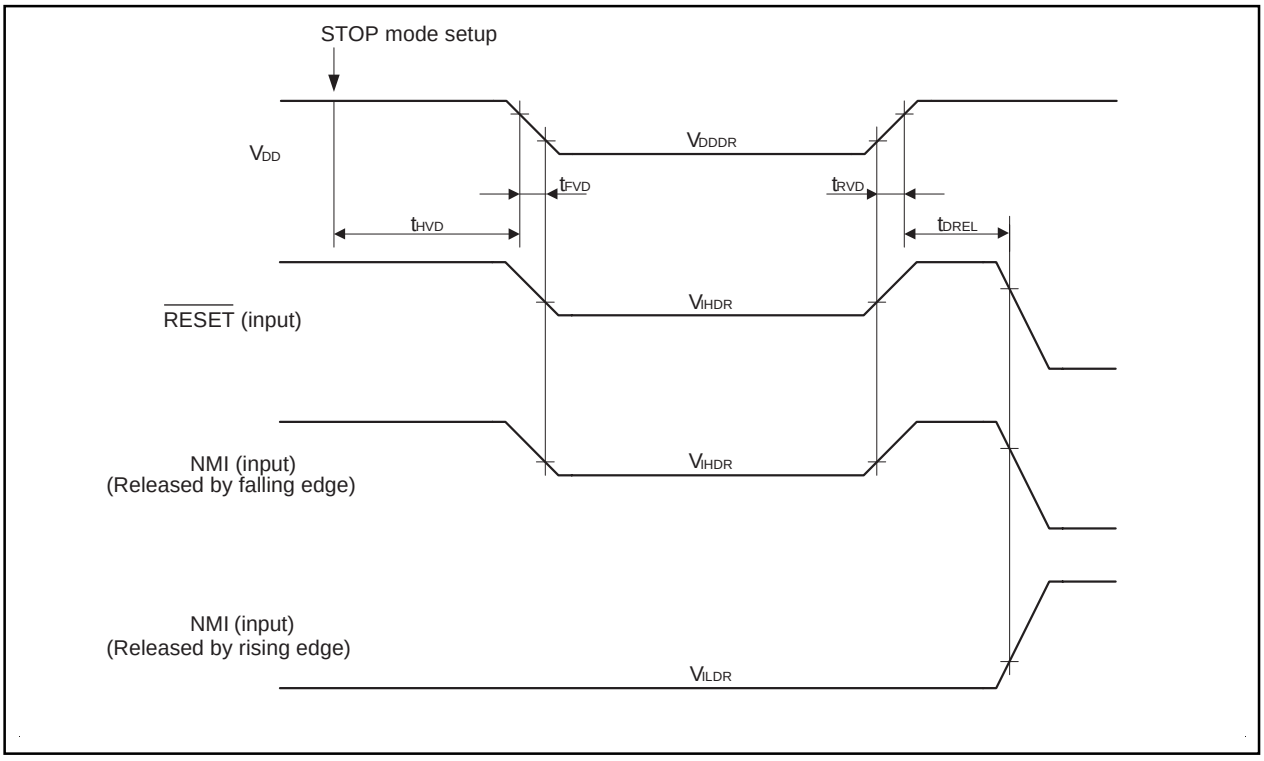
Remark The TYP. value is a reference value for when T_A = 25°C and V_{DD} = 3.3 V. The current does not include the current flowing through pull-up resistors.

Data Hold Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Data hold voltage	V_{DDDR}	STOP mode and $V_{DD} = V_{DDDR}$		1.5		3.6	V
Data hold current	I_{DDDR}	$V_{DD} = V_{DDDR}$	–40°C ≤ T_A ≤ +40°C		10	60	μA
★			40°C < T_A ≤ 85°C			600	μA
Power supply voltage rise time	t_{RVD}			200			μs
Power supply voltage fall time	t_{FVD}			200			μs
Power supply voltage hold time (from STOP mode setting)	t_{HVD}			0			ms
STOP release signal input time	t_{DREL}			0			ns
Data hold high-level input voltage	V_{IHDR}	**Note**		$0.8V_{DDDR}$		V_{DDDR}	V
Data hold low-level input voltage	V_{ILDR}	**Note**		–0.5		$0.2V_{DDDR}$	V

Note P01/TI000/INTP000, P02/INTP001, P04/DMARQ0/INTP100 to P07/DMARQ3/INTP103, P11/TI010/INTP010, P12/INTP011, P21/TI020/INTP020, P22/INTP021, P24/TC0/INTP110 to P27/TC3/INTP113, P30/SO2/INTP130, P31/SI2/INTP131, P32/SCK2/INTP132, P33/TXD2/INTP133, P34/RXD2/INTP120, P35/INTP121, P36/INTP122, P37/ADTRG/INTP123, P41/RXD0/SI0, P42/SCK0, P44/RXD1/SI1, P45/SCK1, P50/TI030/INTP030, P51/INTP031

Remark The TYP. value is a reference value for when T_A = 25°C.



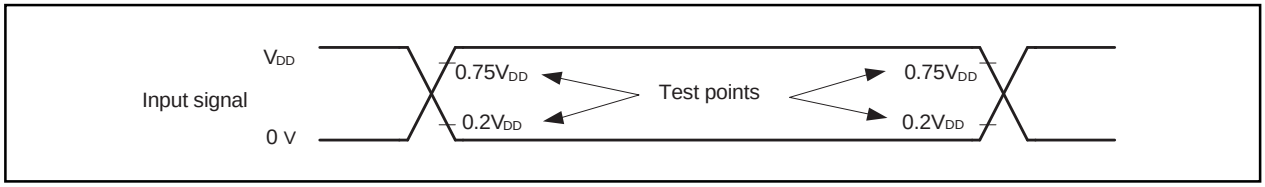
AC Characteristics

(T_A = –40 to +85°C, V_{DD} = 3.3 V ±0.3 V, V_{SS} = 0 V, output pin load capacitance: C_L = 50 pF)

AC test input waveform

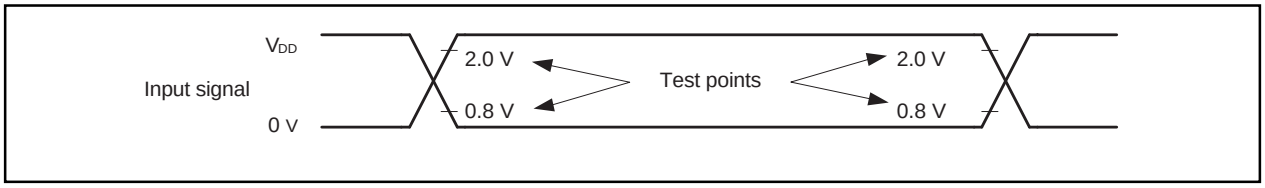
(a) P01/TI000/INTP000, P02/INTP001, P04/$\overline{\text{DMARQ0}}$/$\overline{\text{INTP100}}$ to P07/$\overline{\text{DMARQ3}}$/$\overline{\text{INTP103}}$, P11/TI010/INTP010, P12/INTP011, P21/TI020/INTP020, P22/INTP021, P24/$\overline{\text{TC0}}$/$\overline{\text{INTP110}}$ to P27/$\overline{\text{TC3}}$/$\overline{\text{INTP113}}$, P30/SO2/$\overline{\text{INTP130}}$, P31/SI2/$\overline{\text{INTP131}}$, P32/$\overline{\text{SCK2}}$/$\overline{\text{INTP132}}$, P33/TXD2/$\overline{\text{INTP133}}$, P34/RXD2/$\overline{\text{INTP120}}$, P35/$\overline{\text{INTP121}}$, P36/$\overline{\text{INTP122}}$, P37/ADTRG/$\overline{\text{INTP123}}$, P41/RXD0/SI0, P42/$\overline{\text{SCK0}}$, P44/RXD1/SI1, P45/$\overline{\text{SCK1}}$, P50/TI030/INTP030, P51/INTP031

★

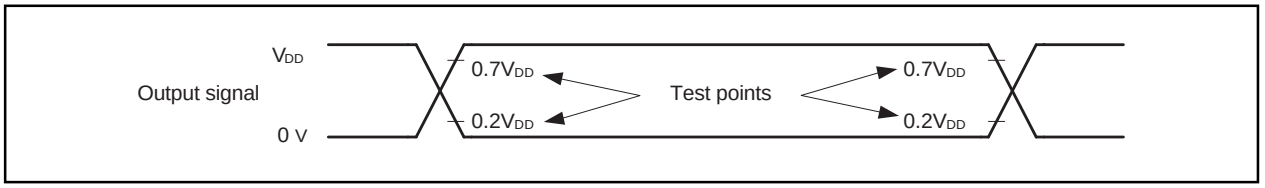


(b) Other than (a) above

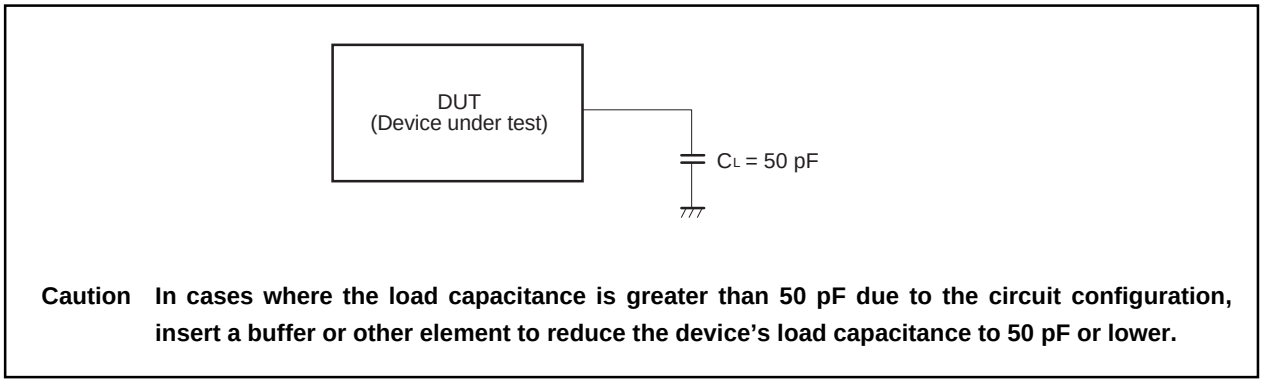
★



AC test output test points



Load condition



Caution In cases where the load capacitance is greater than 50 pF due to the circuit configuration, insert a buffer or other element to reduce the device's load capacitance to 50 pF or lower.

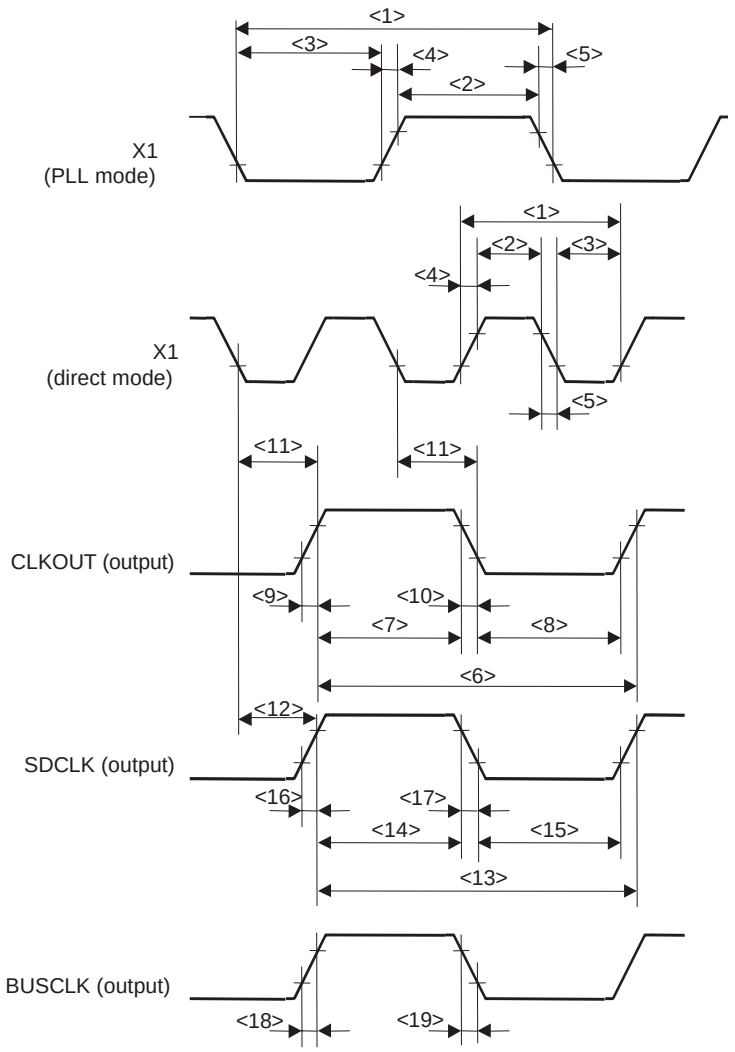
(1) Clock timing (1/2)

	Parameter	Symbol		Conditions	MIN.	MAX.	Unit
★	X1 input cycle	<1>	t_{CYX}	Direct mode	20	125	ns
				PLL mode	200	250	ns
	X1 input high-level width	<2>	t_{WXH}	Direct mode	5		ns
				PLL mode	50		ns
	X1 input low-level width	<3>	t_{WXL}	Direct mode	5		ns
				PLL mode	50		ns
	X1 input rise time	<4>	t_{XR}	Direct mode		4	ns
				PLL mode		10	ns
	X1 input fall time	<5>	t_{XF}	Direct mode		4	ns
				PLL mode		10	ns
	CPU operation frequency	–	ϕ		4	50	MHz
	CLKOUT output cycle	<6>	t_{CYK1}		20	250	ns
	CLKOUT high-level width	<7>	t_{WKH1}		0.5T – 5		ns
	CLKOUT low-level width	<8>	t_{WKL1}		0.5T – 6		ns
	CLKOUT rise time	<9>	t_{KR1}			5	ns
	CLKOUT fall time	<10>	t_{KF1}			4	ns
	Delay time from X1↓ to CLKOUT	<11>	t_{DKX}			40	ns
	Delay time from X1↓ to SDCLK	<12>	t_{DSX}			40	ns
	SDCLK output cycle	<13>	t_{CYK2}		20	250	ns
	SDCLK high-level width	<14>	t_{WKH2}		0.5T – 5		ns
	SDCLK low-level width	<15>	t_{WKL2}		0.5T – 6		ns
	SDCLK rise time	<16>	t_{KR2}			5	ns
	SDCLK fall time	<17>	t_{KF2}			4	ns
	BUSCLK rise time	<18>	t_{KR3}			5	ns
	BUSCLK fall time	<19>	t_{KF3}			4	ns

Remarks 1. $T = t_{CYK}$

2. The phase difference between CLKOUT and SDCLK, and between CLKOUT and BUSCLK cannot be defined.

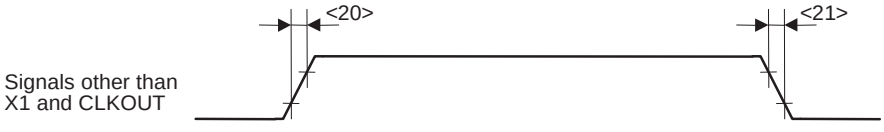
(1) Clock timing (2/2)



Caution The cycle of BUSCLK varies depending on the bus cycle.

(2) Output waveform (except for X1 and CLKOUT)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Output rise time	<20>	t_{OR}			5	ns
Output fall time	<21>	t_{OF}			4	ns

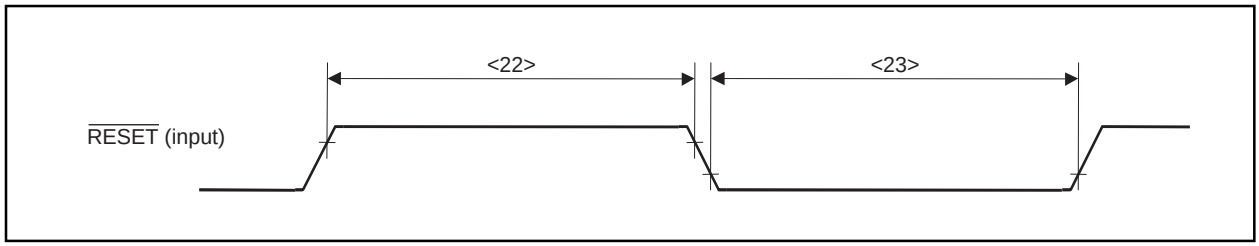


(3) Reset timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ pin high-level width	<22>	t_{WRSH}		500		ns
$\overline{\text{RESET}}$ pin low-level width	<23>	t_{WRSL}	At power-on and at STOP mode release	500 + T_{OS}		ns
			Other than at power-on and at STOP mode release	500		ns

Caution Thoroughly evaluate the oscillation stabilization time.

Remark T_{OS}: Oscillation stabilization time



(4) SRAM, external ROM, and external I/O access timing

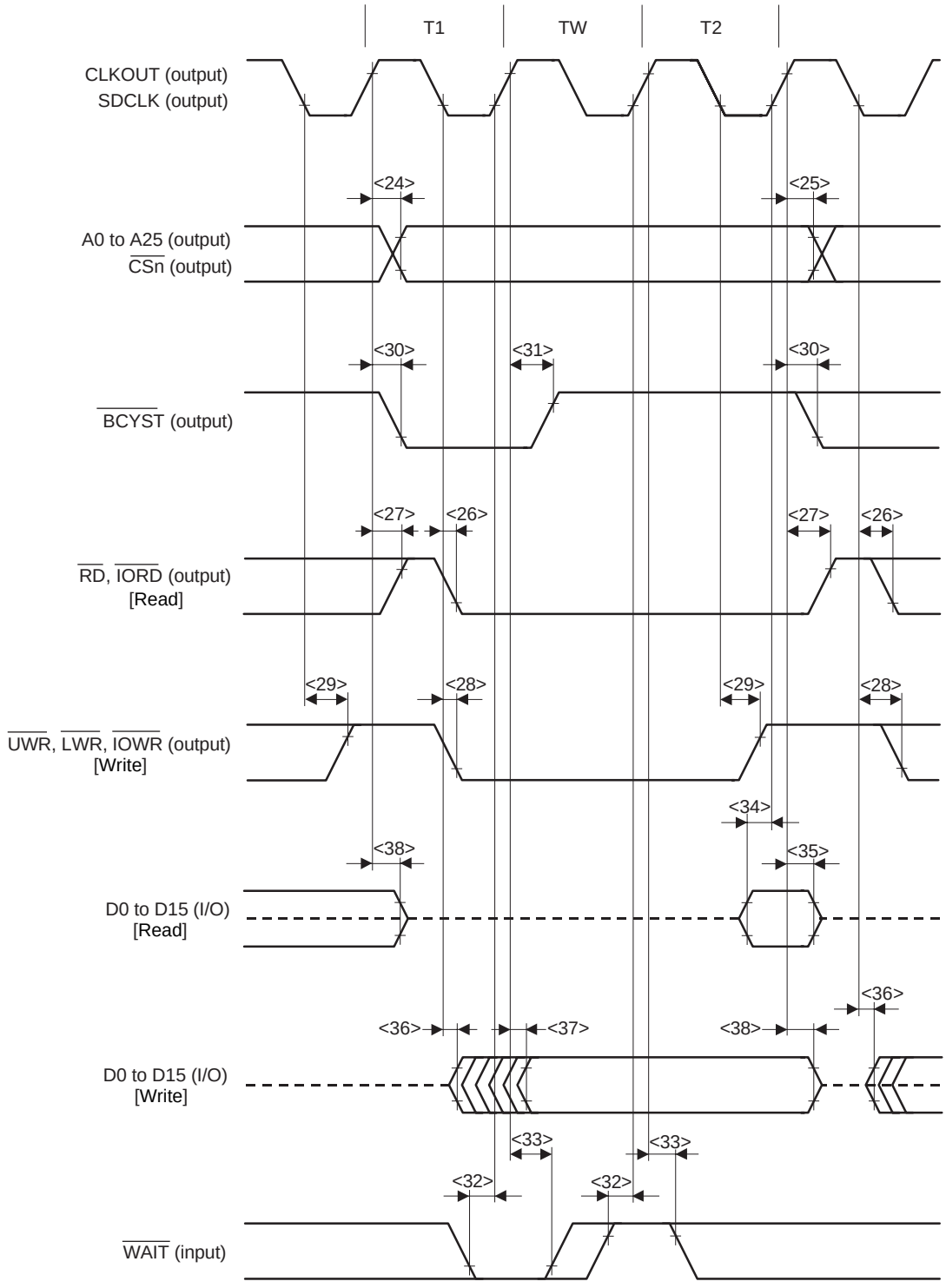
(a) Access timing (SRAM, external ROM, external I/O) (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address, $\overline{CSn}$ output delay time (from CLKOUT↑)	<24>	t_{DKA}		2	13	ns
Address, $\overline{CSn}$ output delay time (from SDCLK↑)				0	13	ns
Address, $\overline{CSn}$ output hold time (from CLKOUT↑)	<25>	t_{HKA}		2	13	ns
Address, $\overline{CSn}$ output hold time (from SDCLK↑)				0	13	ns
$\overline{RD}$, $\overline{IORD}$↓ delay time (from CLKOUT↓)	<26>	t_{DKRDL}		2	13	ns
$\overline{RD}$, $\overline{IORD}$↓ delay time (from SDCLK↓)				0	13	ns
$\overline{RD}$, $\overline{IORD}$↑ delay time (from CLKOUT↑)	<27>	t_{HKRDH}		2	13	ns
$\overline{RD}$, $\overline{IORD}$↑ delay time (from SDCLK↑)				0	13	ns
$\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$↓ delay time (from CLKOUT↓)	<28>	t_{DKWRL}		2	13	ns
$\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$↓ delay time (from SDCLK↓)				0	13	ns
$\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$↑ delay time (from CLKOUT↓)	<29>	t_{HKWRH}		2	13	ns
$\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$↑ delay time (from SDCLK↓)				0	13	ns
$\overline{BCYST}$↓ delay time (from CLKOUT↑)	<30>	t_{DKBSL}		2	13	ns
$\overline{BCYST}$↓ delay time (from SDCLK↑)				0	13	ns
$\overline{BCYST}$↑ delay time (from CLKOUT↑)	<31>	t_{HKBSH}		2	13	ns
$\overline{BCYST}$↑ delay time (from SDCLK↑)				0	13	ns
$\overline{WAIT}$ setup time (to CLKOUT↑)	<32>	t_{SWK}		8		ns
$\overline{WAIT}$ setup time (to SDCLK↑)				10		ns
$\overline{WAIT}$ hold time (from CLKOUT↑)	<33>	t_{HKW}		2		ns
$\overline{WAIT}$ hold time (from SDCLK↑)				2		ns
Data input setup time (to CLKOUT↑)	<34>	t_{SKID}		8		ns
Data input setup time (to SDCLK↑)				10		ns
Data input hold time (from CLKOUT↑)	<35>	t_{HKID}		2		ns
Data input hold time (from SDCLK↑)				2		ns
Data output delay time (from CLKOUT↓)	<36>	t_{DKOD1}		2	13	ns
Data output delay time (from SDCLK↓)				0	13	ns
Data output delay time (from CLKOUT↑)	<37>	t_{DKOD2}		2	13	ns
Data output delay time (from SDCLK↑)				0	13	ns
Data float delay time (from CLKOUT↑)	<38>	t_{HKOD}		2	13	ns
Data float delay time (from SDCLK↑)				0	13	ns

Remarks 1. Maintain at least one of the data input hold times, t_{HRDID} or t_{HKID}.

2. n = 0 to 7

(a) Access timing (SRAM, external ROM, external I/O) (2/2)



Remarks 1. This is the timing when the number of waits based on the DWC1 and DWC2 registers is zero.

2. The broken lines indicate high impedance.

3. n = 0 to 7

(b) Read timing (SRAM, external ROM, external I/O) (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Data input setup time (from address)	<39>	t_{SAID}			$(2 + w + w_D + w_{AS})T - 21$	ns
Data input setup time (from $\overline{RD}$)	<40>	t_{SRDID}			$(1.5 + w + w_D)T - 21$	ns
$\overline{RD}$, $\overline{IORD}$ low-level width	<41>	t_{WRDL}		$(1.5 + w + w_D)T - 10$		ns
$\overline{RD}$, $\overline{IORD}$ high-level width	<42>	t_{WRDH}		$(0.5 + w_{AS} + i)T - 10$		ns
Delay time from address, $\overline{CSn}$, to $\overline{RD}$, $\overline{IORD}\downarrow$	<43>	t_{DARD}		$(0.5 + w_{AS})T - 10$		ns
Delay time from $\overline{RD}$, $\overline{IORD}\uparrow$ to address	<44>	t_{DRDA}		iT		ns
Data input hold time (from $\overline{RD}$, $\overline{IORD}\uparrow$)	<45>	t_{HRDID}		0		ns
Delay time from $\overline{RD}$, $\overline{IORD}\uparrow$ to data output	<46>	t_{DRDOD}		$(0.5 + i)T - 10$		ns
$\overline{WAIT}$ setup time (from address)	<47>	t_{SAW}	**Note**		$(1 + w_{AS})T - 21$	ns
$\overline{WAIT}$ setup time (from $\overline{BCYST}\downarrow$)	<48>	t_{SBSW}	**Note**		$(1 + w_{AS})T - 21$	ns
$\overline{WAIT}$ hold time (from $\overline{BCYST}\uparrow$)	<49>	t_{HBSW}	**Note**	$T - 10$		ns
$\overline{WAIT}$ high-level width	<50>	t_{WWH}		$T - 10$		ns
★ Data output hold time (from $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}\uparrow$)	<57>	t_{HWROD}		$(0.5 + i)T - 8$		ns

Note For the first $\overline{WAIT}$ sampling when the wait count based on the DWC1 and DWC2 registers is zero.

Remarks 1. $T = t_{CYK}$

2. w: Wait count based on $\overline{WAIT}$

3. w_D: Wait count based on the DWC1 and DWC2 registers

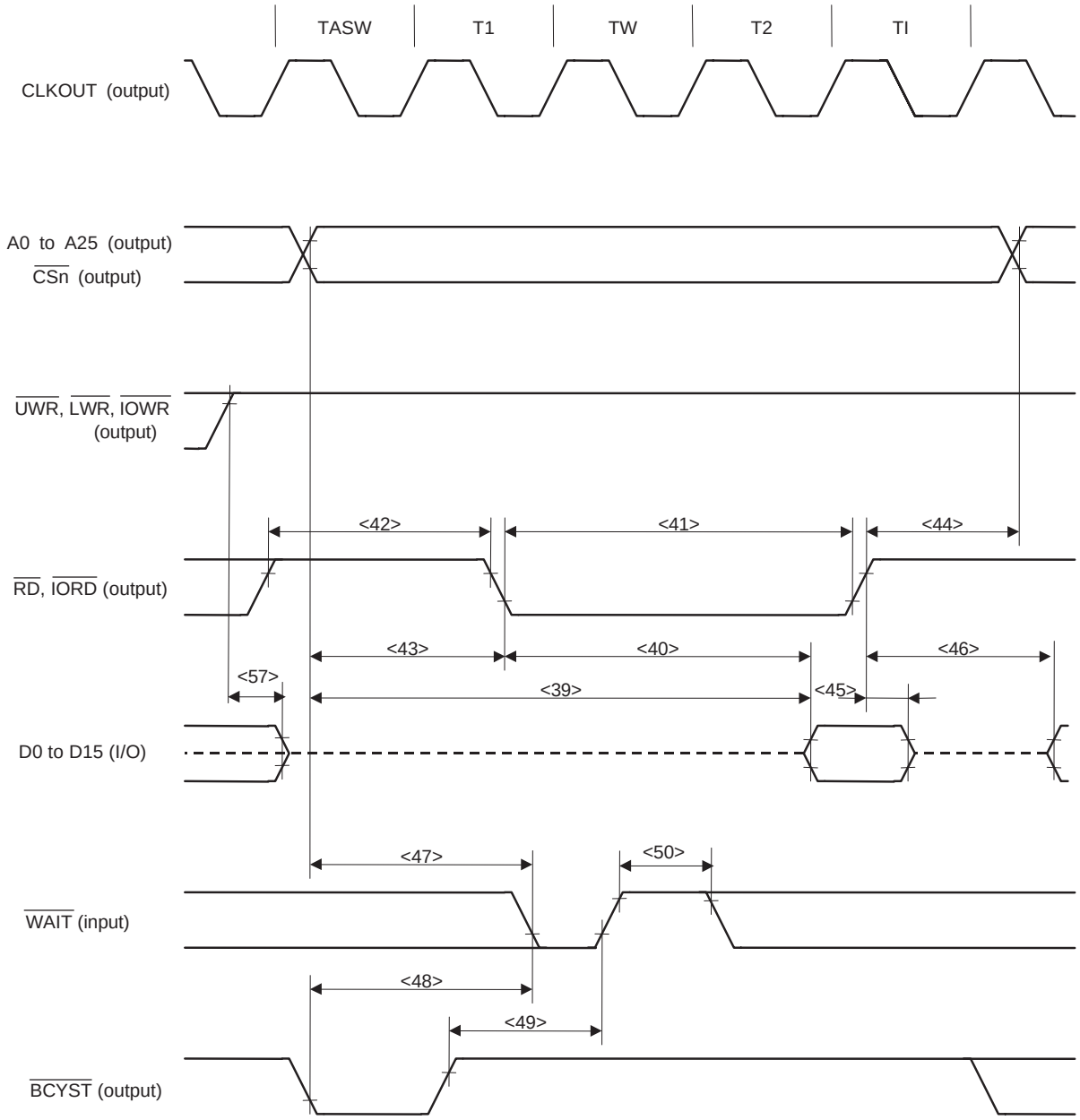
4. Maintain at least one of the data input hold times t_{HRDID} or t_{HKID}

5. n = 0 to 7

6. i: Idle state count

7. w_{AS}: Address setup wait count based on the ASC register

(b) Read timing (SRAM, external ROM, external I/O) (2/2)



Remarks 1. This is the timing when the wait count based on the DWC1 and DWC2 registers is zero, the idle state count based on the BCC register is 1, and the wait count based on the ASC register is 1.

2. The broken lines indicate high impedance.

3. n = 0 to 7

(c) Write timing (SRAM, external ROM, external I/O) (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (from address)	<47>	t_{SAW}	**Note**		$(1 + w_{AS})T - 21$	ns
$\overline{WAIT}$ setup time (from $\overline{BCYST}\downarrow$)	<48>	t_{SBSW}	**Note**		$(1 + w_{AS})T - 21$	ns
$\overline{WAIT}$ hold time (from $\overline{BCYST}\uparrow$)	<49>	t_{HBSW}	**Note**	T – 10		ns
$\overline{WAIT}$ high-level width	<50>	t_{WWH}		T – 10		ns
Delay time from address, $\overline{CSn}$ to $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}\downarrow$	<51>	t_{DAWR}		$(0.5 + w_{AS})T - 10$		ns
Address setup time (to $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}\uparrow$)	<52>	t_{SAWR}		$(1.5 + w + w_D + w_{AS})T - 10$		ns
Delay time from $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}\uparrow$ to address	<53>	t_{DWRA}		$(0.5 + i)T - 10$		ns
$\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ high-level width	<54>	t_{WWRH}		$(0.5 + i + w_{AS})T - 10$		ns
$\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ low-level width	<55>	t_{WWRL}		$(1 + w + w_D)T - 10$		ns
Data output setup time (to $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}\uparrow$)	<56>	t_{SODWR}		$(0.5 + w_{AS} + w + w_D)T - 10$		ns
★ Data output hold time (from $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}\uparrow$)	<57>	t_{HWROD}		$(0.5 + i)T - 8$		ns

Note For the first $\overline{WAIT}$ sampling when the wait count based on the DWC1 and DWC2 registers is zero.

Remarks 1. $T = t_{CYK}$

2. w: Wait count based on $\overline{WAIT}$

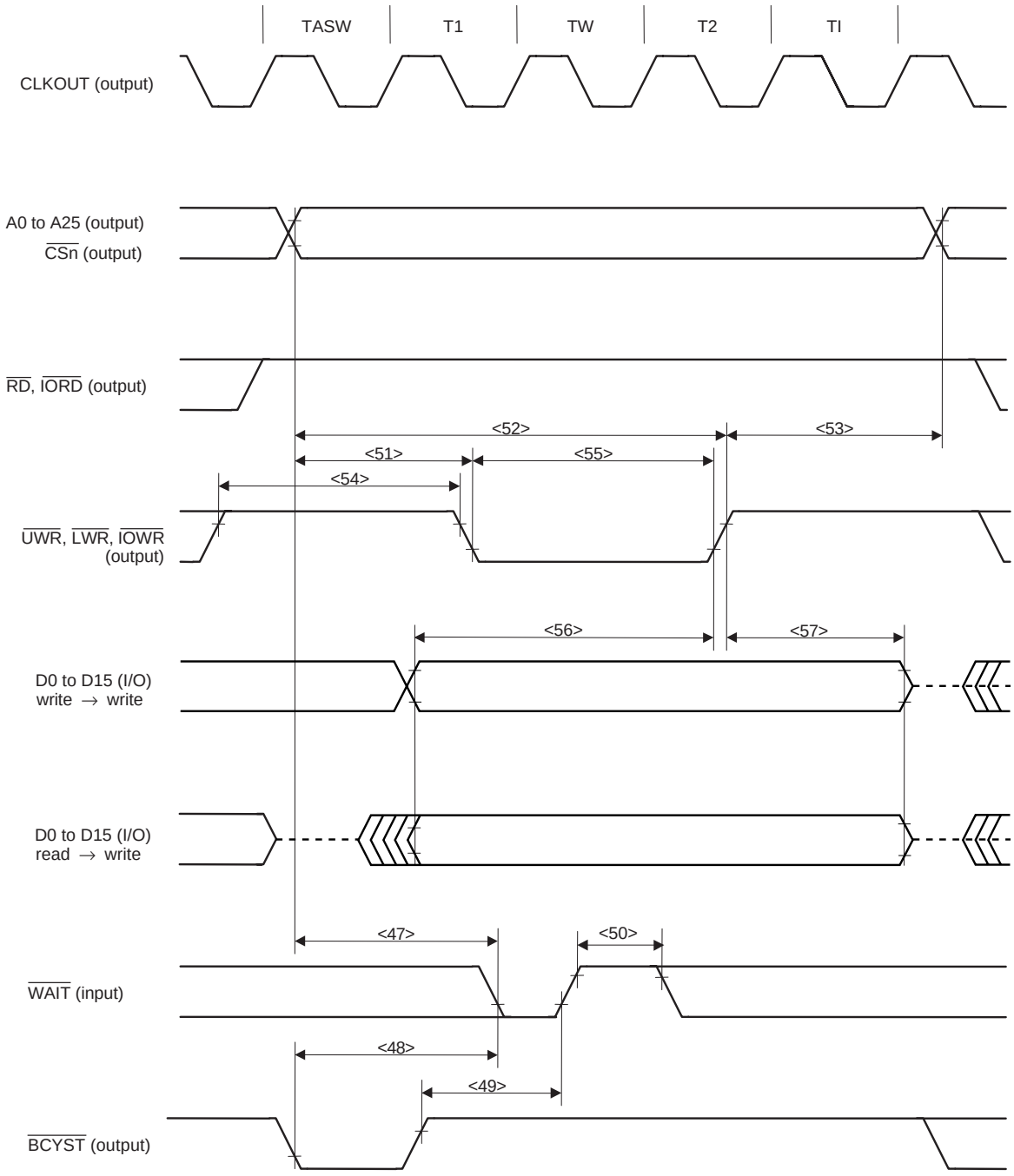
3. w_D: Wait count based on the DWC1 and DWC2 registers

4. n = 0 to 7

5. i: Idle state count

6. w_{AS}: Address setup wait count based on the ASC register

(c) Write timing (SRAM, external ROM, external I/O) (2/2)



Remarks 1. This is the timing when the wait count based on the DWC1 and DWC2 registers is zero, the idle state count based on the BCC register is 1, and the wait count based on the ASC register is 1.

2. The broken lines indicate high impedance.

3. n = 0 to 7

(d) DMA flyby transfer timing (SRAM → external I/O transfer) (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to CLKOUT↑)	<32>	t_{SWK}		8		ns
$\overline{WAIT}$ hold time (from CLKOUT↑)	<33>	t_{HKW}		0		ns
$\overline{RD}$ low-level width	<41>	t_{WRDL}		$(1.5 + w + w_D)T - 10$		ns
$\overline{RD}$ high-level width	<42>	t_{WRDH}		$(0.5 + w_{AS} + i)T - 10$		ns
Delay time from address, $\overline{CSn}$ to $\overline{RD}$↓	<43>	t_{DARD}		$(0.5 + w_{AS})T - 10$		ns
Delay time from $\overline{RD}$↑ to address	<44>	t_{DRDA}		iT		ns
Delay time from $\overline{RD}$↑ to data output	<46>	t_{DRDOD}		$(0.5 + i)T - 10$		ns
$\overline{WAIT}$ setup time (from address)	<47>	t_{SAW}	**Note**		$(1 + w_{AS})T - 21$	ns
$\overline{WAIT}$ setup time (from $\overline{BCYST}$↓)	<48>	t_{SBSW}	**Note**		$(1 + w_{AS})T - 21$	ns
$\overline{WAIT}$ hold time (from $\overline{BCYST}$↑)	<49>	t_{HBSW}	**Note**	T – 10		ns
$\overline{WAIT}$ high-level width	<50>	t_{WWH}		T – 10		ns
Delay time from address to $\overline{IOWR}$↓	<51>	t_{DAWR}		$(0.5 + w_{AS})T - 10$		ns
Address setup time (to $\overline{IOWR}$↑)	<52>	t_{SAWR}		$(1.5 + w + w_D + w_{AS})T - 10$		ns
Delay time from $\overline{IOWR}$↑ to address	<53>	t_{DWRA}		$(1.5 + i)T - 10$		ns
$\overline{IOWR}$ high-level width	<54>	t_{WWRH}		$(0.5 + i + w_{AS})T - 10$		ns
$\overline{IOWR}$ low-level width	<55>	t_{WWRL}		$(1 + w + w_D)T - 10$		ns
Delay time from $\overline{IOWR}$↑ to $\overline{RD}$↑	<58>	t_{DIWRRD}		1.5T – 10		ns
Delay time from $\overline{DMAAKm}$↓ to $\overline{IOWR}$↓	<59>	t_{DDAWR}		$(0.5 + w_{AS})T - 10$		ns
Delay time from $\overline{IOWR}$↑ to $\overline{DMAAKm}$↑	<60>	t_{DWRDA}		$(1.5 + i)T - 10$		ns

Note For the first $\overline{WAIT}$ sampling when the number of waits based on the DWC1 and DWC2 registers is zero.

Remarks 1. $T = t_{CYK}$

2. w: Wait count based on $\overline{WAIT}$

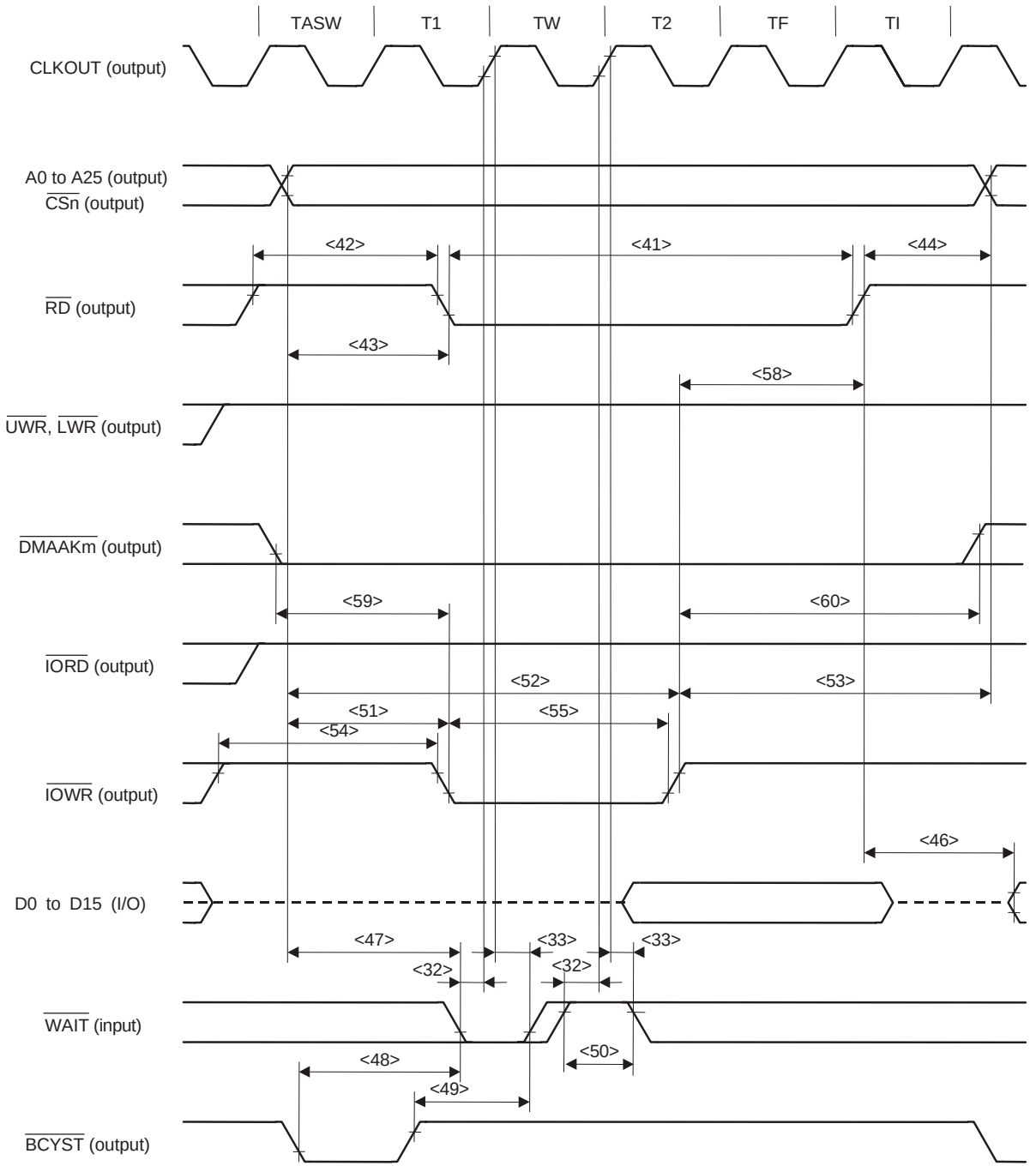
3. w_D: Wait count based on the DWC1 and DWC2 registers

4. n = 0 to 7, m = 0 to 3

5. i: Idle state count

6. w_{AS}: Address setup wait count based on the ASC register

(d) DMA flyby transfer timing (SRAM → external I/O transfer) (2/2)



Remarks 1. This is the timing when the wait count based on the DWC1 and DWC2 registers is zero, the idle state count based on the BCC register is 1, and the wait count based on the ASC register is 1.

2. The broken lines indicate high impedance.

3. n = 0 to 7, m = 0 to 3

(e) DMA flyby transfer timing (external I/O → SRAM transfer) (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to CLKOUT↑)	<32>	t_{SWK}		8		ns
$\overline{WAIT}$ hold time (from CLKOUT↑)	<33>	t_{HKW}		0		ns
$\overline{IORD}$ low-level width	<41>	t_{WRDL}		$(2 + w + w_D)T - 10$		ns
$\overline{IORD}$ high-level width	<42>	t_{WRDH}		$(1 + i + w_{AS})T - 10$		ns
Delay time from address, $\overline{CSn}$ to $\overline{IORD}$↓	<43>	t_{DARD}		$(0.5 + w_{AS})T - 10$		ns
Delay time from $\overline{IORD}$↑ to address	<44>	t_{DRDA}		$(0.5 + i)\ T - 10$		ns
Delay time from $\overline{IORD}$↑ to data output	<46>	t_{DRDOD}		$(1 + i)T - 10$		ns
$\overline{WAIT}$ setup time (from address)	<47>	t_{SAW}	**Note**		$(1 + w_{AS})T - 21$	ns
$\overline{WAIT}$ setup time (from $\overline{BCYST}$↓)	<48>	t_{SBSW}	**Note**		$(1 + w_{AS})T - 21$	ns
$\overline{WAIT}$ hold time (from $\overline{BCYST}$↑)	<49>	t_{HBSW}	**Note**	$T - 10$		ns
$\overline{WAIT}$ high-level width	<50>	t_{WWH}		$T - 10$		ns
Delay time from address to $\overline{UWR}$, $\overline{LWR}$↓	<51>	t_{DAWR}		$(0.5 + w_{AS})T - 10$		ns
Address setup time (to $\overline{UWR}$, $\overline{LWR}$↑)	<52>	t_{SAWR}		$(1.5 + w + w_D + w_{AS})T - 10$		ns
Delay time from $\overline{UWR}$, $\overline{LWR}$↑ to address	<53>	t_{DWRA}		$(0.5 + i)T - 10$		ns
$\overline{UWR}$, $\overline{LWR}$ high-level width	<54>	t_{WWRH}		$(0.5 + i + w_{AS})T - 10$		ns
$\overline{UWR}$, $\overline{LWR}$ low-level width	<55>	t_{WWRL}		$(1 + w + w_D)T - 10$		ns
Delay time from $\overline{UWR}$, $\overline{LWR}$↑ to $\overline{IORD}$↑	<61>	t_{DWRIRD}		$T - 10$		ns
Delay time from $\overline{DMAAKm}$↓ to $\overline{IORD}$↓	<62>	t_{DDARD}		$(0.5 + w_{AS})T - 10$		ns
Delay time from $\overline{IORD}$↑ to $\overline{DMAAKm}$↑	<63>	t_{DRDDA}		$(0.5 + i)T - 10$		ns

Note For first $\overline{WAIT}$ sampling when wait count based on the DWC1 and DWC2 registers is zero.

Remarks 1. $T = t_{CYK}$

2. w: Wait count based on $\overline{WAIT}$

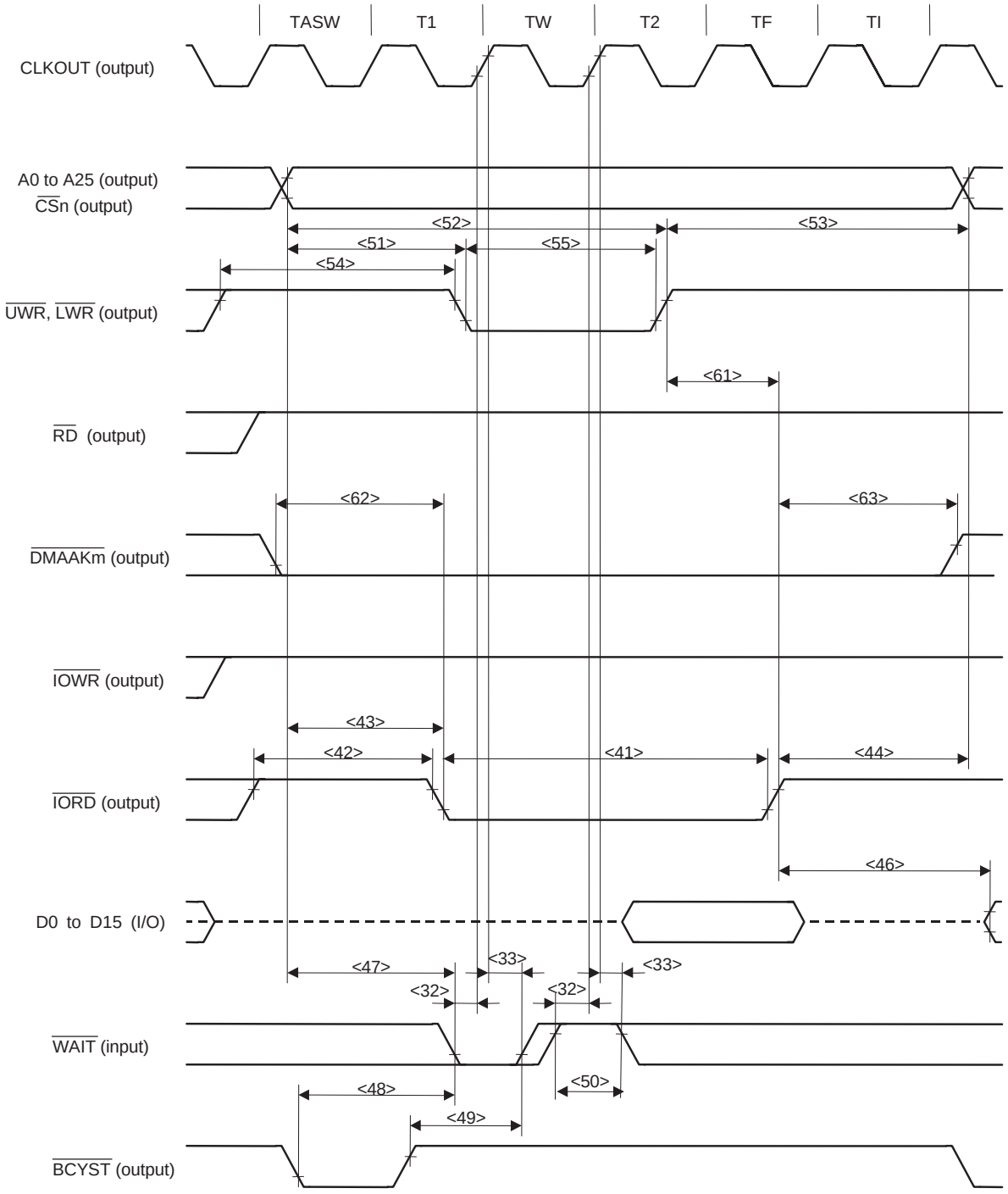
3. w_D: Wait count based on the DWC1 and DWC2 registers

4. n = 0 to 7, m = 0 to 3

5. i: Count of idle states inserted when a write cycle follows a read cycle

6. w_{AS}: Address setup wait count based on the ASC register

(e) DMA flyby transfer timing (external I/O → SRAM transfer) (2/2)



Remarks 1. This is the timing when the wait count based on the DWC1 and DWC2 registers is zero, the idle state count based on the BCC register is 1, and the wait count based on the ASC register is 1.

2. The broken lines indicate high impedance.

3. n = 0 to 7, m = 0 to 3

(5) Page ROM access timing

(a) 8-bit bus width (half-word/word access) and 16-bit bus width (word access) (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to CLKOUT↑)	<32>	t_{SWK}		8		ns
$\overline{WAIT}$ hold time (from CLKOUT↑)	<33>	t_{HKW}		0		ns
Data input setup time (to CLKOUT↑)	<34>	t_{SKID}		8		ns
Data input hold time (from CLKOUT↑)	<35>	t_{HKID}		0		ns
Off-page data input setup time (to address)	<39>	t_{SAID}			$(2 + w + w_D + w_{AS})T - 21$	ns
Off-page data input setup time (from $\overline{RD}$)	<40>	t_{SRDID}			$(1.5 + w + w_D)T - 21$	ns
Data input hold time (from $\overline{RD}$↑)	<45>	t_{HRDID}		0		ns
Delay time from $\overline{RD}$↑ to data output	<46>	t_{DRDOD}		$(0.5 + i)T - 10$		ns
★ On-page data input setup time (from address)	<64>	t_{SOAID}			$(2 + w + w_{PR} + w_{AS})T - 21$	ns

Remarks 1. $T = t_{CYK}$

2. w: Wait count based on $\overline{WAIT}$

3. w_D: Wait count based on the DWC1 and DWC2 registers

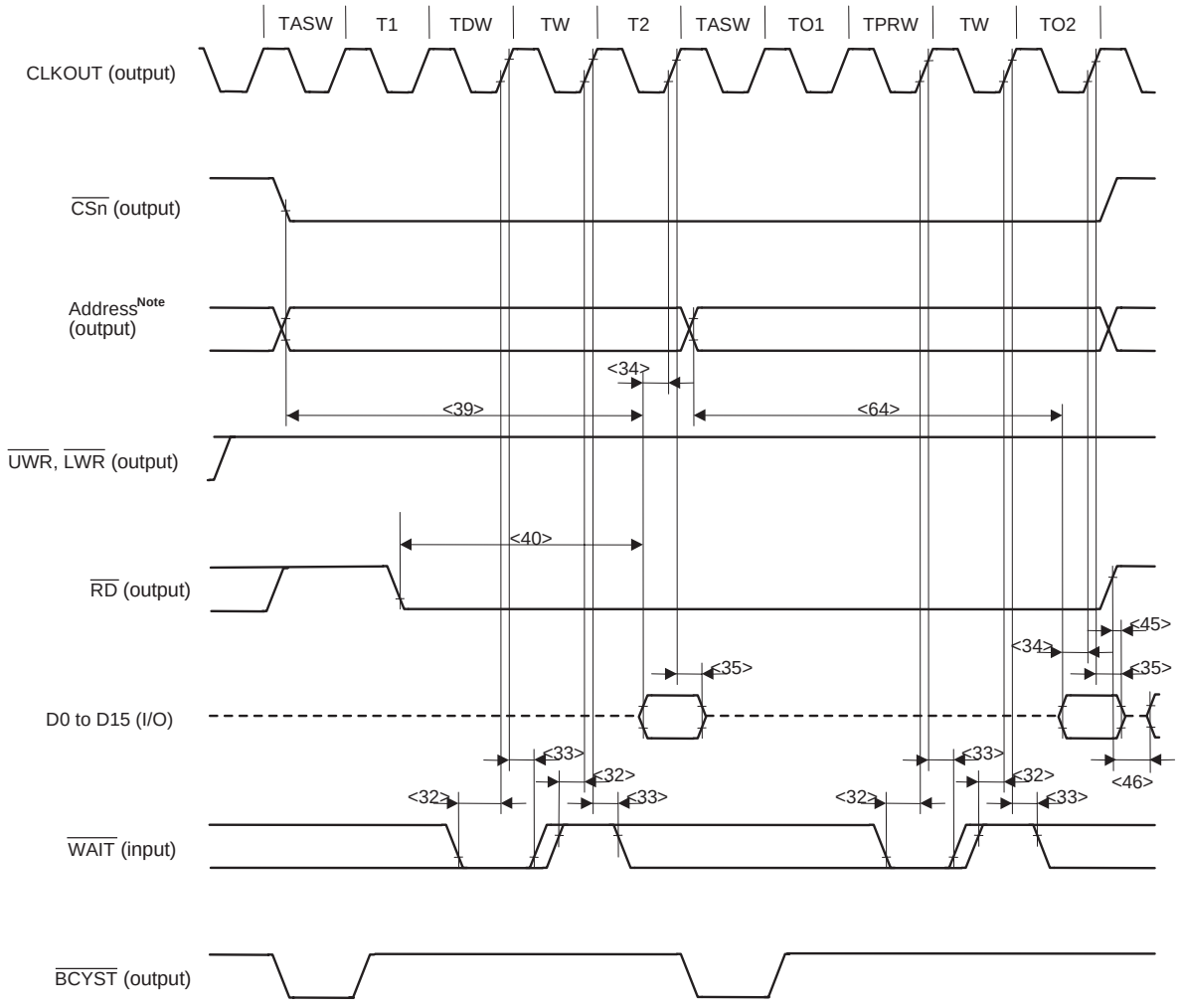
4. w_{PR}: Wait count based on the PRC register

5. i: Count of idle states inserted when a write cycle follows a read cycle

6. w_{AS}: Address setup wait count based on the ASC register

7. Maintain at least one of the data input hold times t_{HKID} or t_{HRDID}

(a) 8-bit bus width (half-word/word access) and 16-bit bus width (word access) (2/2)



Note On-page and off-page addresses are as follows.

PRC Register				On-Page Address	Off-Page Address
MA6	MA5	MA4	MA3		
0	0	0	0	A0 to A2	A3 to A25
0	0	0	1	A0 to A3	A4 to A25
0	0	1	1	A0 to A4	A5 to A25
0	1	1	1	A0 to A5	A6 to A25
1	1	1	1	A0 to A6	A7 to A25

Remarks 1. This is the timing for the following case.
Wait count based on the DWC1 and DWC2 registers (TDW): 1
Wait count based on the PRC register (TPRW): 1
Wait count based on the ASC register (TASW): 1

2. The broken lines indicate high impedance.

3. n = 0 to 7

★ **(b) 8-bit bus width (byte access) and 16-bit bus width (byte/half-word access) (1/2)**

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to CLKOUT↑)	<32>	t_{SWK}		8		ns
$\overline{WAIT}$ hold time (from CLKOUT↑)	<33>	t_{HKW}		0		ns
Data input setup time (to CLKOUT↑)	<34>	t_{SKID}		8		ns
Data input hold time (from CLKOUT↑)	<35>	t_{HKID}		0		ns
Off-page data input setup time (to address)	<39>	t_{SAID}			$(2 + w + w_D + w_{AS})T - 21$	ns
Off-page data input setup time (from $\overline{RD}$)	<40>	t_{SRDID}			$(1.5 + w + w_D)T - 21$	ns
Off-page $\overline{RD}$ low-level width	<180>	t_{WRDL}		$(1.5 + w + w_D)T - 10$		ns
$\overline{RD}$ high-level width	<181>	t_{WRDH}		$(0.5 + w_{AS})T - 10$		ns
Data input hold time (from $\overline{RD}$↑)	<45>	t_{HRDID}		0		ns
Delay time from $\overline{RD}$↑ to data output	<46>	t_{DRDOD}		$(0.5 + i)T - 10$		ns
On-page $\overline{RD}$ low-level width	<182>	t_{WORDL}		$(1.5 + w + w_{PR})T - 10$		ns
On-page data input setup time (from address)	<64>	t_{SOAID}			$(2 + w + w_{PR} + w_{AS})T - 21$	ns
On-page data input setup time (from $\overline{RD}$)	<183>	t_{SORDID}			$(1.5 + w + w_{PR})T - 21$	ns

Remarks 1. $T = t_{CYK}$

2. w: Wait count based on $\overline{WAIT}$

3. w_D: Wait count based on the DWC1 and DWC2 registers

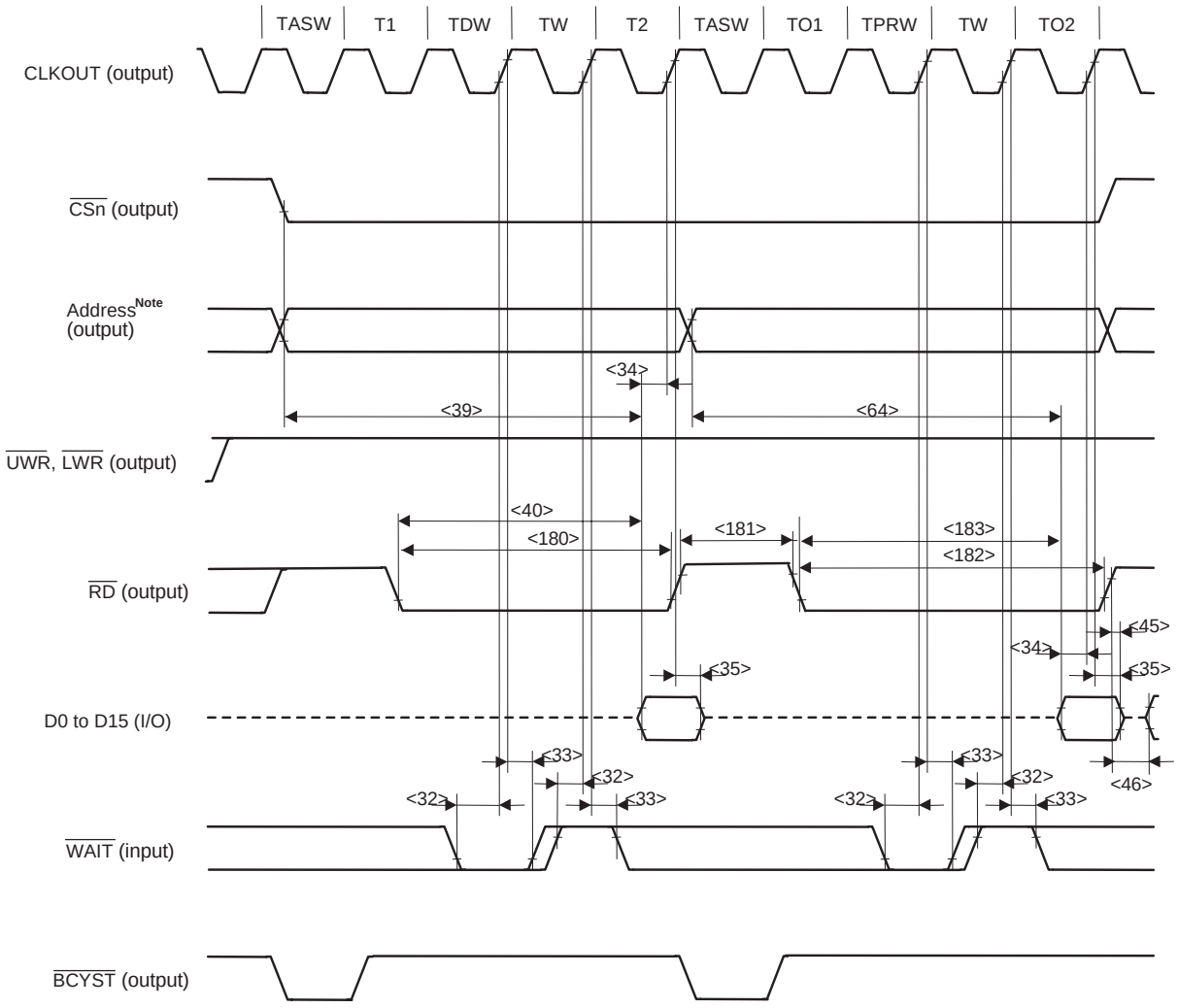
4. w_{PR}: Wait count based on the PRC register

5. i: Count of idle states inserted when a write cycle follows a read cycle

6. w_{AS}: Address setup wait count based on the ASC register

7. Maintain at least one of the data input hold times t_{HKID} or t_{HRDID}

★ **(b) 8-bit bus width (byte access) and 16-bit bus width (byte/half-word access) (2/2)**



Note On-page and off-page addresses are as follows.

PRC Register				On-Page Address	Off-Page Address
MA6	MA5	MA4	MA3		
0	0	0	0	A0 to A2	A3 to A25
0	0	0	1	A0 to A3	A4 to A25
0	0	1	1	A0 to A4	A5 to A25
0	1	1	1	A0 to A5	A6 to A25
1	1	1	1	A0 to A6	A7 to A25

Remarks 1. This is the timing for the following case.
Wait count based on the DWC1 and DWC2 registers (TDW): 1
Wait count based on the PRC register (TPRW): 1
Wait count based on the ASC register (TASW): 1

2. The broken lines indicate high impedance.

3. n = 0 to 7

(6) DRAM access timing

(a) Read timing (EDO DRAM) (1/3)

Parameter		Symbol		Conditions	MIN.	MAX.	Unit
Data input setup time (to CLKOUT↓)		<34>	t_{SKID}		8		ns
Data input hold time (from CLKOUT↓)		<35>	t_{HKID}		0		ns
Delay time from $\overline{OE}$↑ to data output		<46>	t_{DRDOD}		(1 + i)T – 10		ns
Read/write cycle time		<65>	t_{HPC}		(1 + w_{DA} + w_{CP})T – 10		ns
Row address setup time		<66>	t_{ASR}		0.5T – 10		ns
Row address hold time		<67>	t_{RAH}		(0.5 + w_{RH})T – 10		ns
Column address setup time		<68>	t_{ASC}		0.5T – 10		ns
Column address hold time		<69>	t_{CAH}		(0.5 + w_{DA})T – 10		ns
$\overline{RAS}$ precharge time		<70>	t_{RP}	w_{RP} = 0	T – 10		ns
				w_{RP} ≥ 1	w_{RP}T – 10		ns
Column address read time (to $\overline{RAS}$↑)		<71>	t_{RAL}		(1.5 + w_{CP} + w_{DA})T – 10		ns
$\overline{CAS}$ hold time		<72>	t_{CSH}		(1.5 + w_{RH} + w_{DA})T – 10		ns
Delay time from $\overline{RAS}$ to column address		<73>	t_{RAD}		(0.5 + w_{RH})T – 10		ns
Delay time from $\overline{RAS}$ to $\overline{CAS}$		<74>	t_{RCD}		(1 + w_{RH})T – 10		ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time		<75>	t_{CRP}	w_{RP} = 0	1.5T – 10		ns
				w_{RP} ≥ 1	(0.5 + w_{RP})T – 10		ns
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge		<76>	t_{RHCP}		(1.5 + w_{CP} + w_{DA})T – 10		ns
$\overline{WE}$ setup time (to $\overline{CAS}$↓)		<77>	t_{RCS}	w_{RP} = 0	(3 + w_{RH})T – 10		ns
				w_{RP} ≥ 1	(2 + w_{RP} + w_{RH})T – 10		ns
$\overline{WE}$ hold time (from $\overline{RAS}$↑)		<78>	t_{RRH}		(1 + i)T – 10		ns
$\overline{WE}$ hold time (from $\overline{CAS}$↑)		<79>	t_{RCH}		(1.5 + i)T – 10		ns
$\overline{RAS}$ pulse width	Off-page	<80>	t_{RASP}		(2 + w_{RH} + w_{DA})T – 10		ns
$\overline{CAS}$ pulse width		<81>	t_{HCAS}		(0.5 + w_{DA})T – 10		ns
$\overline{CAS}$ precharge time		<82>	t_{CP}		(0.5 + w_{CP})T – 10		ns
$\overline{CAS}$ hold time from $\overline{OE}$	Off-page	<83>	t_{OCH1}	w_{RP} = 0	(2.5 + w_{RH} + w_{DA})T – 10		ns
				w_{RP} ≥ 1	(1.5 + w_{RP} + w_{RH} + w_{DA})T – 10		ns
	On-page	<84>	t_{OCH2}		(0.5 + w_{CP} + w_{DA})T – 10		ns
Access time to $\overline{CAS}$ precharge		<85>	t_{ACP}			(1.5 + w_{CP} + w_{DA})T – 21	ns
Data input hold time (from $\overline{CAS}$↓)		<86>	t_{DHC}		0		ns
$\overline{CAS}$ access time		<87>	t_{CAC}			(1 + w_{DA})T – 21	ns
Access time from column address		<88>	t_{AA}			(1.5 + w_{DA})T – 21	ns

(a) Read Timing (EDO DRAM) (2/3)

Parameter		Symbol		Conditions	MIN.	MAX.	Unit
Output enable access time	Off-page	<89>	t_{OEA1}	$w_{RP} = 0$		$(3 + w_{RP} + w_{RH} + w_{DA})T - 21$	ns
				$w_{RP} \geq 1$		$(2 + w_{RP} + w_{RH} + w_{DA})T - 21$	ns
	On-page	<90>	t_{OEA2}			$(1 + w_{CP} + w_{DA})T - 21$	ns
$\overline{RAS}$ access time		<91>	t_{RAC}			$(2 + w_{RH} + w_{DA})\ T - 21$	ns
Output buffer turn-off delay time (from $\overline{OE}$)		<92>	t_{OEZ}		0		ns

Cautions 1. At least one clock is inserted in w_{RP} by default regardless of the setting of the RPC1n and RPC0n bits in the DRCn register (n = 1, 3, 4, or 6)

2. The $\overline{WAIT}$ signal cannot be controlled using the $\overline{BCYST}$ signal when using EDO DRAM.

Remarks 1. $T = t_{CYK}$

2. w_{DA}: Wait count based on the DAC1n and DAC0n bits of the DRCn register (n = 1, 3, 4, 6)

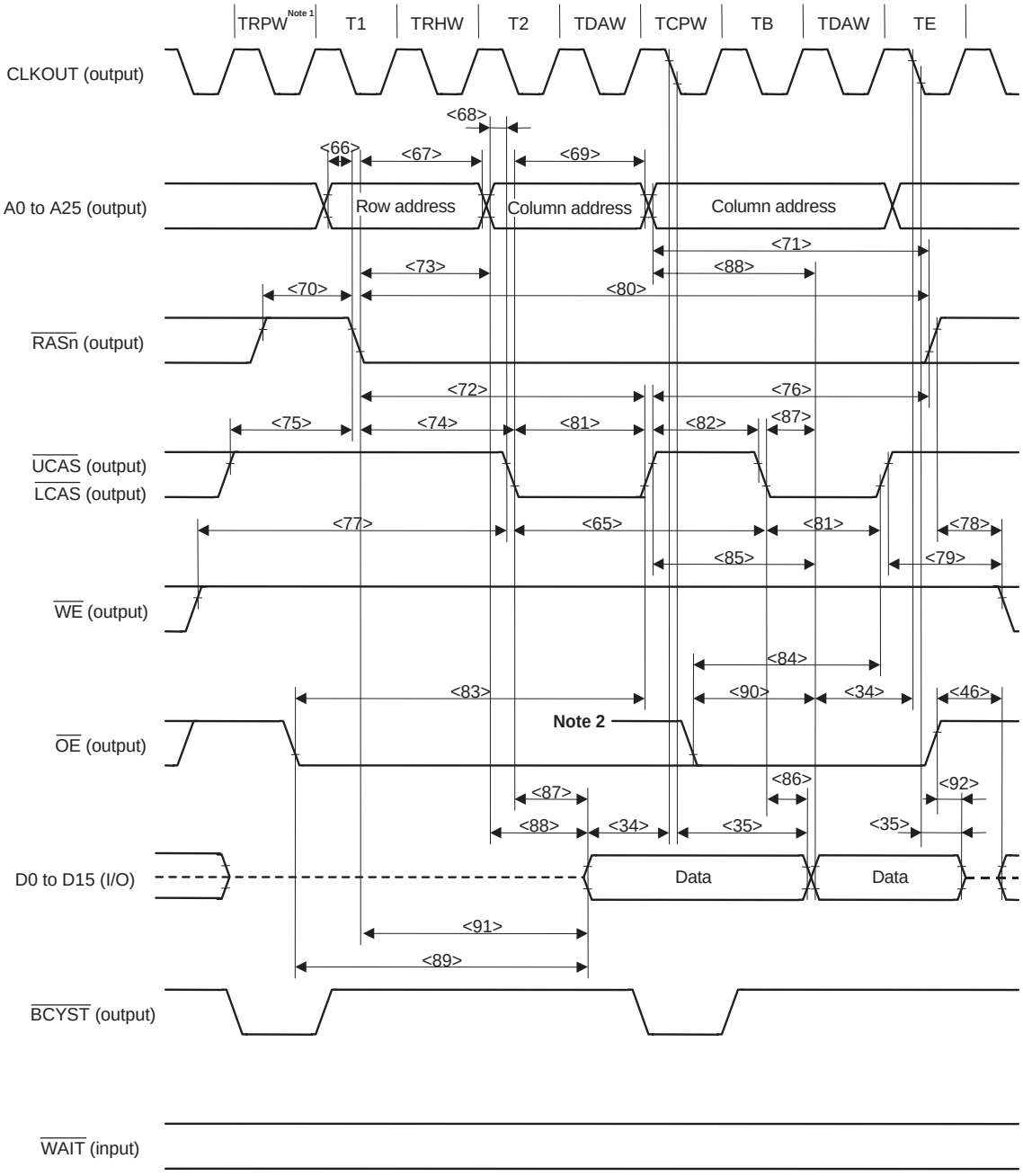
3. w_{CP}: Wait count based on the CPC1n and CPC0n bits of the DRCn register (n = 1, 3, 4, 6)

4. w_{RP}: Wait count based on the RPC1n and RPC0n bits of the DRCn register (n = 1, 3, 4, 6)

5. w_{RH}: Wait count based on the RHC1n and RHC0n bits of the DRCn register (n = 1, 3, 4, 6)

6. i: Idle state count

(a) Read timing (EDO DRAM) (3/3)



Notes 1. At least one clock is always inserted in TRPW.

2. During on-page access from other cycles while $\overline{RAS}$ is low level.

Remarks 1. This is the timing for the following case.

Wait count based on the RPC1n and RPC0n bits of the DRCn register (TRPW): 1

Wait count based on the RHC1n and RHC0n bits of the DRCn register (TRHW): 1

Wait count based on the DAC1n and DAC0n bits of the DRCn register (TDAW): 1

Wait count based on the CPC1n and CPC0n bits of the DRCn register (TCPW): 1

2. The broken lines indicate high impedance.

3. n = 1, 3, 4, 6

(b) Write timing (EDO DRAM) (1/2)

Parameter		Symbol		Conditions	MIN.	MAX.	Unit
Read/write cycle time		<65>	t_{HPC}	$w_{CP} = 0$	$(2 + w_{DA})T - 10$		ns
				$w_{CP} \geq 1$	$(1 + w_{DA} + w_{CP})T - 10$		ns
Row address setup time		<66>	t_{ASR}		$0.5T - 10$		ns
Row address hold time		<67>	t_{RAH}		$(0.5 + w_{RH})T - 10$		ns
Column address setup time		<68>	t_{ASC}		$0.5T - 10$		ns
Column address hold time		<69>	t_{CAH}		$(0.5 + w_{DA})T - 10$		ns
$\overline{RAS}$ precharge time		<70>	t_{RP}	$w_{RP} = 0$	$T - 10$		ns
				$w_{RP} \geq 1$	$w_{RP}T - 10$		ns
Column address read time (to $\overline{RAS}\downarrow$)		<71>	t_{RAL}	$w_{CP} = 0$	$(2.5 + w_{DA})T - 10$		ns
				$w_{CP} \geq 1$	$(1.5 + w_{CP} + w_{DA})T - 10$		ns
$\overline{CAS}$ hold time		<72>	t_{CSH}		$(1.5 + w_{RH} + w_{DA})T - 10$		ns
Delay time from $\overline{RAS}$ to column address		<73>	t_{RAD}		$(0.5 + w_{RH})T - 10$		ns
Delay time from $\overline{RAS}$ to $\overline{CAS}$		<74>	t_{RCD}		$(1 + w_{RH})T - 10$		ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time		<75>	t_{CRP}	$w_{RP} = 0$	$1.5T - 10$		ns
				$w_{RP} \geq 1$	$(0.5 + w_{RP})T - 10$		ns
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge		<76>	t_{RHCP}	$w_{CP} = 0$	$(2.5 + w_{DA})T - 10$		ns
				$w_{CP} \geq 1$	$(1.5 + w_{CP} + w_{DA})T - 10$		ns
$\overline{RAS}$ pulse width	Off-page	<80>	t_{RASP}		$(2 + w_{RH} + w_{DA})T - 10$		ns
$\overline{CAS}$ pulse width		<81>	t_{HCAS}		$(0.5 + w_{DA})T - 10$		ns
$\overline{CAS}$ precharge time		<82>	t_{CP}	$w_{CP} = 0$	$1.5T - 10$		ns
				$w_{CP} \geq 1$	$(0.5 + w_{CP})T - 10$		ns
$\overline{RAS}$ hold time		<93>	t_{RSH}		$(1 + w_{DA})T - 10$		ns
$\overline{WE}$ setup time (to $\overline{CAS}\downarrow$)	Off-page	<94>	t_{WCS1}	$w_{RP} = 0$	$(2 + w_{RH})T - 10$		ns
				$w_{RP} \geq 1$	$(1 + w_{RP} + w_{RH})T - 10$		ns
	On-page	<95>	t_{WCS2}	$w_{CP} = 0$	$T - 10$		ns
				$w_{CP} \geq 1$	$w_{CP}T - 10$		ns
$\overline{WE}$ hold time (from $\overline{CAS}\downarrow$)		<96>	t_{WCH}		$(1 + w_{DA})T - 10$		ns
Data setup time (to $\overline{CAS}\downarrow$)	Off-page	<97>	t_{DS1}		$(1.5 + w_{RH})T - 10$		ns
	On-page	<98>	t_{DS2}	$w_{CP} = 0$	$1.5T - 10$		ns
				$w_{CP} \geq 1$	$(0.5 + w_{CP})T - 10$		ns
Data hold time (from $\overline{CAS}\downarrow$)		<99>	t_{DH}		$(0.5 + w_{DA})T - 10$		ns
$\overline{WE}$ pulse width	On-page	<100>	t_{WP}	$w_{CP} = 0$	$(2 + w_{DA})T - 10$		ns
				$w_{CP} \geq 1$	$(1 + w_{DA} + w_{CP})T - 10$		ns
$\overline{WE}$ read time (to $\overline{RAS}\uparrow$)	On-page	<101>	t_{RWL}	$w_{CP} = 0$	$(2 + w_{DA})T - 10$		ns
				$w_{CP} \geq 1$	$(1 + w_{DA} + w_{CP})T - 10$		ns
$\overline{WE}$ read time (to $\overline{CAS}\uparrow$)	On-page	<102>	t_{CWL}	$w_{CP} = 0$	$(1.5 + w_{DA})T - 10$		ns
				$w_{CP} \geq 1$	$(0.5 + w_{DA} + w_{CP})T - 10$		ns

Cautions 1. At least one clock is inserted in w_{RP} by default regardless of the setting of the RPC1n and RPC0n bits in the DRCn register (n = 1, 3, 4, 6).

2. At least one clock is inserted in w_{CP} by default regardless of the setting of the CPC1n and CPC0n bits in the DRCn register (n = 1, 3, 4, 6).

3. The $\overline{\text{WAIT}}$ signal cannot be controlled using the $\overline{\text{BCYST}}$ signal when using EDO DRAM.

Remarks 1. T = t_{CYK}

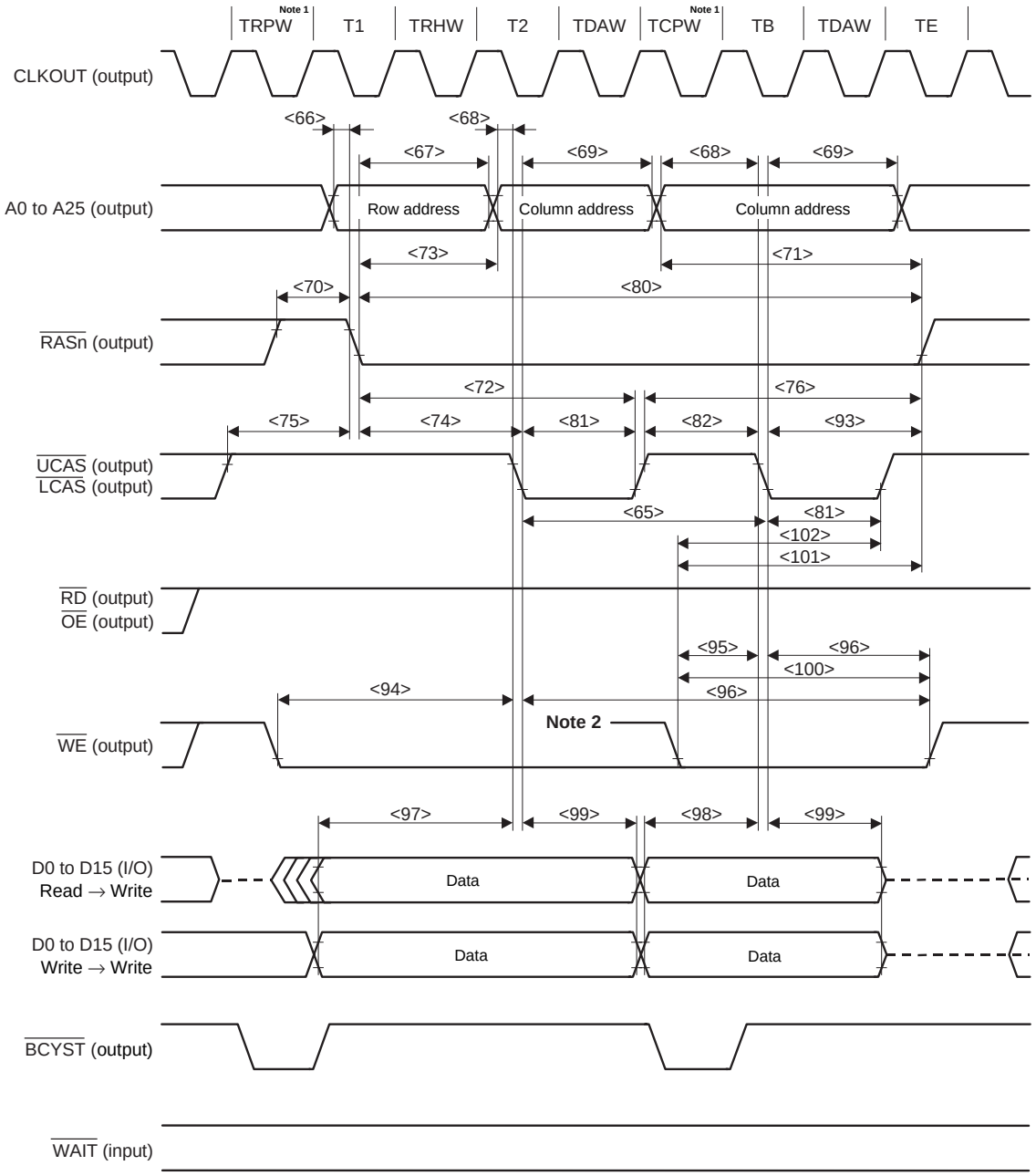
2. w_{DA}: Wait count based on the DAC1n and DAC0n bits of the DRCn register (n = 1, 3, 4, 6)

3. w_{CP}: Wait count based on the CPC1n and CPC0n bits of the DRCn register (n = 1, 3, 4, 6)

4. w_{RP}: Wait count based on the RPC1n and RPC0n bits of the DRCn register (n = 1, 3, 4, 6)

5. w_{RH}: Wait count based on the RHC1n and RHC0n bits of the DRCn register (n = 1, 3, 4, 6)

(b) Write timing (EDO DRAM) (2/2)



Notes 1. At least one clock is always inserted in TRPW and TCPW.

2. During on-page access from other cycles while $\overline{RAS}$ is low level.

Remarks 1. This is the timing for the following case.

Wait count based on the RPC1n and RPC0n bits of the DRCn register (TRPW): 1

Wait count based on the RHC1n and RHC0n bits of the DRCn register (TRHW): 1

Wait count based on the DAC1n and DAC0n bits of the DRCn register (TDAW): 1

Wait count based on the CPC1n and CPC0n bits of the DRCn register (TCPW): 1

2. The broken lines indicate high impedance.

3. n = 1, 3, 4, 6

(c) DMA flyby transfer timing (EDO DRAM → external I/O transfer) (1/3)

Parameter		Symbol		Conditions	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to CLKOUT↑)		<32>	t_{SWK}		8		ns
$\overline{WAIT}$ hold time (from CLKOUT↑)		<33>	t_{HKW}		0		ns
Delay time from $\overline{OE}$↑ to data output		<46>	t_{DRDOD}		(1 + i)T – 10		ns
Delay time from $\overline{IOWR}$↑ to address		<53>	t_{DWRA}		1.5T – 10		ns
$\overline{IOWR}$ low-level width		<55>	t_{WWRL}	w_{RP} = 0	(3 + w_{RH} + w_{DA} + w)T – 10		ns
				w_{RP} ≥ 1	(2 + w_{RP} + w_{DA} + w_{RH} + w)T – 10		ns
Delay time from $\overline{IOWR}$↑ to $\overline{OE}$↑		<58>	t_{DWRRD}		T – 10		ns
Row address setup time		<66>	t_{ASR}		0.5T – 10		ns
Row address hold time		<67>	t_{RAH}		(0.5 + w_{RH})T – 10		ns
Column address setup time		<68>	t_{ASC}		0.5T – 10		ns
Column address hold time		<69>	t_{CAH}		(2.5 + w_{DA} + w)T – 10		ns
$\overline{RAS}$ precharge time		<70>	t_{RP}	w_{RP} = 0	T – 10		ns
				w_{RP} ≥ 1	w_{RP}T – 10		ns
Column address read time (to $\overline{RAS}$)		<71>	t_{RAL}		(3.5 + w_{CP} + w_{DA} + w)T – 10		ns
$\overline{CAS}$ hold time		<72>	t_{CSH}		(3 + w_{RH} + w_{DA} + w)T – 10		ns
Delay time from $\overline{RAS}$ to column address		<73>	t_{RAD}		(0.5 + w_{RH})T – 10		ns
Delay time from $\overline{RAS}$ to $\overline{CAS}$		<74>	t_{RCD}		(1 + w_{RH})T – 10		ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time		<75>	t_{CRP}	w_{RP} = 0	2T – 10		ns
				w_{RP} ≥ 1	(1 + w_{RP})T – 10		ns
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge		<76>	t_{RHCP}		(4 + w_{CP} + w_{DA} + w)T – 10		ns
$\overline{WE}$ setup time (to $\overline{CAS}$↓)		<77>	t_{RCS}	w_{RP} = 0	(3 + w_{RH})T – 10		ns
				w_{RP} ≥ 1	(2 + w_{RP} + w_{RH})T – 10		ns
$\overline{WE}$ hold time (from $\overline{RAS}$↑)		<78>	t_{RRH}		0		ns
$\overline{WE}$ hold time (from $\overline{CAS}$↑)		<79>	t_{RCH}		T – 10		ns
$\overline{RAS}$ pulse width	Off-page	<80>	t_{RASP}		(4 + w_{RH} + w_{DA} + w) T – 10		ns
$\overline{CAS}$ precharge time		<82>	t_{CP}		(1 + w_{CP})T – 10		ns
$\overline{OE}$ to $\overline{CAS}$ hold time	Off-page	<83>	t_{OCH1}	w_{RP} = 0	(4 + w_{RH} + w_{DA} + w)T – 10		ns
				w_{RP} ≥ 1	(3 + w_{RP} + w_{RH} + w_{DA} + w)T – 10		ns
	On-page	<84>	t_{OCH2}		(2 + w_{CP} + w_{DA} + w)T – 10		ns
Output buffer turn-off delay time (from $\overline{OE}$↑)		<92>	t_{OEZ}		0		ns
$\overline{RAS}$ hold time		<93>	t_{RSH}		(3 + w_{DA} + w) T – 10		ns
Read/write cycle time		<103>	t_{RC}	w_{RP} = 0	(5.5 + w_{RH} + w_{DA} + w)T – 10		ns
				w_{RP} ≥ 1	(4.5 + w_{RP} + w_{RH} + w_{DA} + w)T – 10		ns
$\overline{CAS}$ pulse width		<104>	t_{CAS}		(2 + w_{DA} + w)T – 10		ns
$\overline{CAS}$ precharge time		<105>	t_{CPN}	W_{RP} = 0	(3 + w_{RH})T – 10		ns
				W_{RP} ≥ 1	(2 + w_{RP} + w_{RH})T – 10		ns
High-speed page mode cycle time		<106>	t_{PC}		(3 + w_{CP} + w_{DA} + w)T – 10		ns

(c) DMA flyby transfer timing (EDO DRAM → external I/O transfer) (2/3)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from $\overline{\text{DMAAK}}$m↓ to $\overline{\text{CAS}}$↓	<107>	t_{DDACS}	w_{RP} = 0	(2.5 + w_{RH})T − 10		ns
			w_{RP} ≥ 1	(1.5 + w_{RP} + w_{RH})T − 10		ns
Delay time from $\overline{\text{IOWR}}$↓ to $\overline{\text{CAS}}$↓	<108>	t_{DRDCS}	w_{RP} = 0	(2 + w_{RH})T − 10		ns
			w_{RP} ≥ 1	(1 + w_{RP} + w_{RH})T − 10		ns
Output buffer turn-off delay time (from $\overline{\text{CAS}}$↑)	<109>	t_{OFF}		0		ns

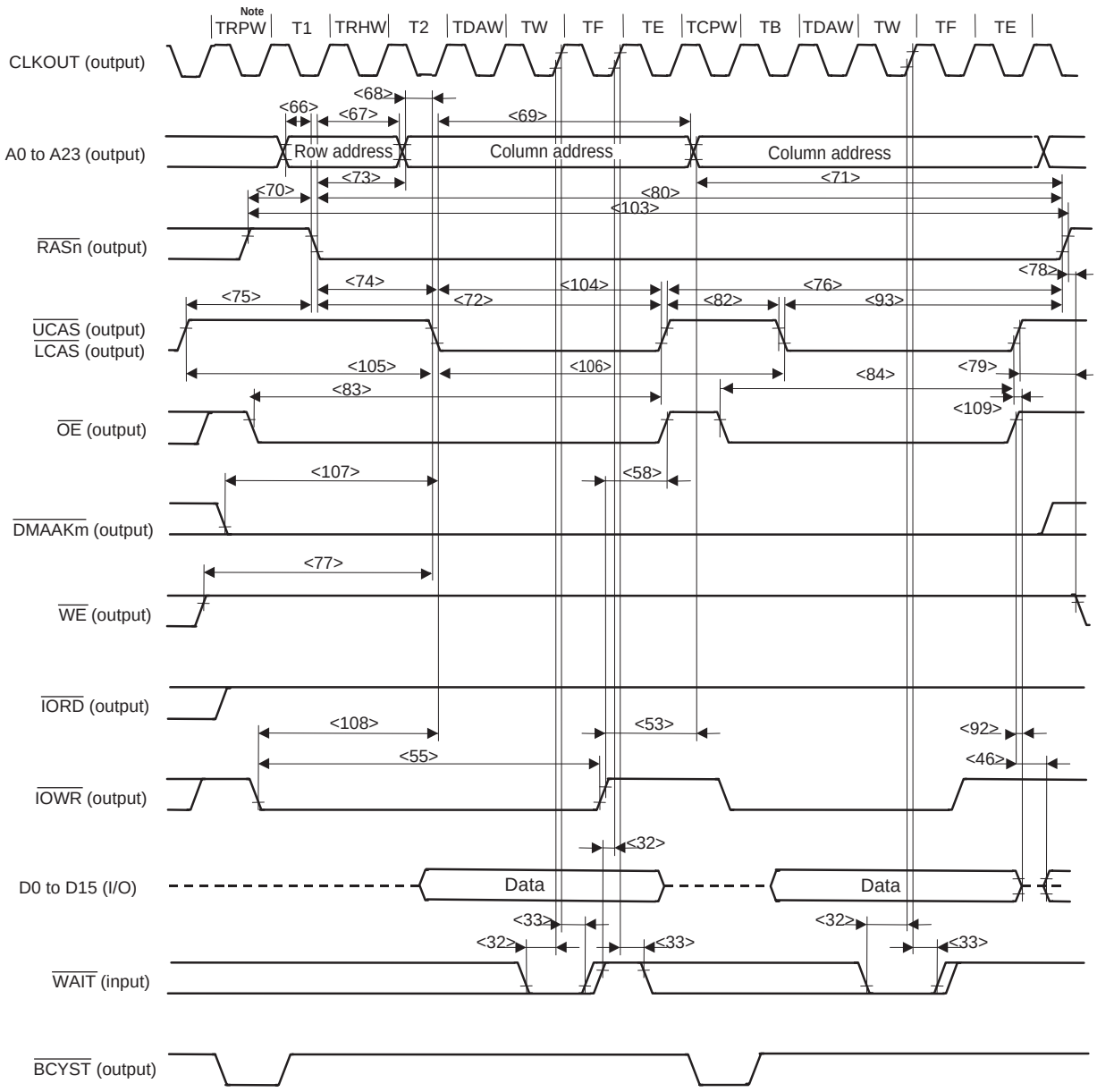
Cautions

1. **At least one clock is inserted in w_{RP} by default regardless of the setting of the RPC1n and RPC0n bits in the DRCn register (n = 1, 3, 4, 6).**
2. **The $\overline{\text{WAIT}}$ signal cannot be controlled using the $\overline{\text{BCYST}}$ signal when using EDO DRAM.**

Remarks

1. T = t_{CYK}
2. w: Wait count based on $\overline{\text{WAIT}}$
3. w_{DA}: Wait count based on the DAC1n and DAC0n bits of the DRCn register (n = 1, 3, 4, 6)
4. w_{CP}: Wait count based on the CPC1n and CPC0n bits of the DRCn register (n = 1, 3, 4, 6)
5. w_{RP}: Wait count based on the RPC1n and RPC0n bits of the DRCn register (n = 1, 3, 4, 6)
6. w_{RH}: Wait count based on the RHC1n and RHC0n bits of the DRCn register (n = 1, 3, 4, 6)
7. i: Idle state count
8. m = 0 to 3

(c) DMA flyby transfer timing (EDO DRAM → external I/O transfer) (3/3)



Note At least one clock is always inserted in TRPW.

Remarks 1. This is the timing for the following case.
Wait count based on the RPC1n and RPC0n bits of the DRCn register (TRPW): 1
Wait count based on the RHC1n and RHC0n bits of the DRCn register (TRHW): 1
Wait count based on the DAC1n and DAC0n bits of the DRCn register (TDAW): 1
Wait count based on the CPC1n and CPC0n bits of the DRCn register (TCPW): 1

2. The broken lines indicate high impedance.

3. n = 1, 3, 4, 6, m = 0 to 3

(d) DMA flyby transfer timing (external I/O → EDO DRAM transfer) (1/3)

Parameter		Symbol		Conditions	MIN.	MAX.	Unit
$\overline{WAIT}$ setup time (to CLKOUT↑)		<32>	t_{SWK}		8		ns
$\overline{WAIT}$ hold time (from CLKOUT↑)		<33>	t_{HKW}		0		ns
$\overline{IORD}$ low-level width		<41>	t_{WRDL}		$(2 + w_{RH} + w_{DA} + w)$ T – 10		ns
$\overline{IORD}$ high-level width		<42>	t_{WRDH}		T – 10		ns
Delay time from $\overline{IORD}$↑ to address		<44>	t_{DRDA}		(0.5 + i) T – 10		ns
Row address setup time		<66>	t_{ASR}		0.5T – 10		ns
Row address hold time		<67>	t_{RAH}		$(0.5 + w_{RH})$T – 10		ns
Column address setup time		<68>	t_{ASC}		0.5T – 10		ns
Column address hold time		<69>	t_{CAH}		$(1.5 + w_{DA})$T – 10		ns
$\overline{RAS}$ precharge time		<70>	t_{RP}	$w_{RP} = 0$	T – 10		ns
				$w_{RP} \geq 1$	w_{RP}T – 10		ns
Column address read time (to $\overline{RAS}$)		<71>	t_{RAL}		$(2.5 + w_{CP} + w_{DA} + w)$T – 10		ns
$\overline{CAS}$ hold time		<72>	t_{CSH}		$(2 + w_{RH} + w_{DA} + w)$T – 10		ns
Delay time from $\overline{RAS}$ to column address		<73>	t_{RAD}		$(0.5 + w_{RH})$ T–10		ns
Delay time from $\overline{RAS}$ to $\overline{CAS}$		<74>	t_{RCD}		$(1 + w_{RH} + w)$T – 10		ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time		<75>	t_{CRP}	$w_{RP} = 0$	2T – 10		ns
				$w_{RP} \geq 1$	$(1 + w_{RP})$T – 10		ns
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge		<76>	t_{RHCP}		$(4 + w_{CP} + w_{DA} + w)$T – 10		ns
$\overline{RAS}$ pulse width	Off-page	<80>	t_{RASP}		$(3 + w_{RH} + w_{DA} + w)$T – 10		ns
$\overline{CAS}$ precharge time		<82>	t_{CP}		$(1 + w_{CP} + w)$T – 10		ns
$\overline{RAS}$ hold time		<93>	t_{RSH}		$(2 + w_{DA})$T – 10		ns
Read/write cycle time		<103>	t_{RC}	$w_{RP} = 0$	$(4.5 + w_{RH} + w_{DA} + w)$T – 10		ns
				$w_{RP} \geq 1$	$(3.5 + w_{RP} + w_{RH} + w_{DA} + w)$T – 10		ns
$\overline{CAS}$ pulse width		<104>	t_{CAS}		$(1 + w_{DA})$T – 10		ns
$\overline{CAS}$ precharge time		<105>	t_{CPN}	$w_{RP} = 0$	$(3 + w_{RH} + w)$T – 10		ns
				$w_{RP} \geq 1$	$(2 + w_{RP} + w_{RH} + w)$T – 10		ns
High-speed page mode cycle		<106>	t_{PC}		$(2 + w_{CP} + w_{DA} + w)$T – 10		ns
Delay time from $\overline{DMAAKm}$↓ to $\overline{CAS}$ ↓		<107>	t_{DDACS}	$w_{RP} = 0$	$(2.5 + w_{RH} + w)$T – 10		ns
				$w_{RP} \geq 1$	$(1.5 + w_{RP} + w_{RH} + w)$T – 10		ns
Delay time from $\overline{IORD}$↓ to $\overline{CAS}$ ↓		<108>	t_{DRDCS}	$w_{RP} = 0$	$(2 + w_{RH} + w)$T – 10		ns
				$w_{RP} \geq 1$	$(1 + w_{RP} + w_{RH} + w)$T – 10		ns
$\overline{WE}$ read time (to $\overline{RAS}$ ↑)		<110>	t_{RWL}		$(3 + w_{DA} + w)$T – 10		ns
$\overline{WE}$ read time (to $\overline{CAS}$ ↑)		<111>	t_{CWL}		$(2 + w_{DA} + w)$T – 10		ns
$\overline{WE}$ pulse width		<112>	t_{WP}		$(2 + w_{DA} + w)$T – 10		ns
$\overline{WE}$ setup time (to $\overline{CAS}$ ↓)	Off-page	<113>	t_{WCS1}		$(2 + w_{RH} + w)$T – 10		ns
	On-page	<114>	t_{WCS2}		T – 10		ns

(d) DMA flyby transfer timing (external I/O → EDO DRAM transfer) (2/3)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{WE}$ hold time (from $\overline{CAS}$ ↓)	<115>	t_{WCH}		$(1 + w_{DA})T - 10$		ns
Delay time from $\overline{WE}$↑ to $\overline{IORD}$↑	<116>	t_{DWERD}		0		ns

Cautions 1. At least one clock is inserted in w_{RP} by default regardless of the setting of the RPC1n and RPC0n bits in the DRCn register (n = 1, 3, 4, 6).

2. At least one clock is inserted in w_{CP} by default regardless of the setting of the CPC1n and CPC0n bits in the DRCn register (n = 1, 3, 4, 6).

3. The $\overline{WAIT}$ signal cannot be controlled using the $\overline{BCYST}$ signal when using EDO DRAM.

Remarks 1. $T = t_{CYK}$

2. w: Wait counts based on $\overline{WAIT}$

3. w_{DA}: Wait count based on the DAC1n and DAC0n bits of the DRCn register (n = 1, 3, 4, 6)

4. w_{CP}: Wait count based on the CPC1n and CPC0n bits of the DRCn register (n = 1, 3, 4, 6)

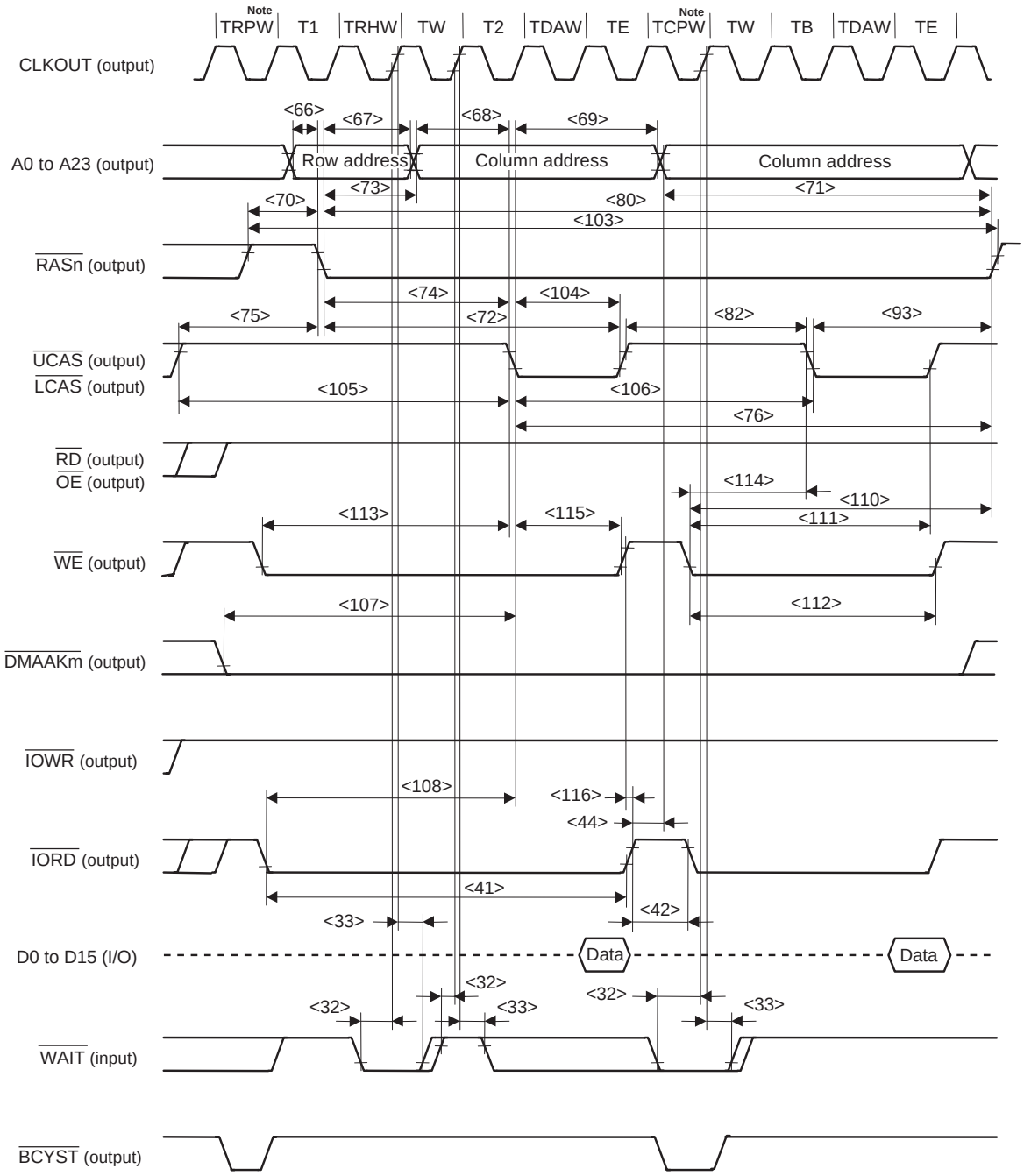
5. w_{RP}: Wait count based on the RPC1n and RPC0n bits of the DRCn register (n = 1, 3, 4, 6)

6. w_{RH}: Wait count based on the RHC1n and RHC0n bits of the DRCn register (n = 1, 3, 4, 6)

7. i: Idle state count

8. m = 0 to 3

(d) DMA flyby transfer timing (external I/O → EDO DRAM transfer) (3/3)



Note At least one clock is always inserted in TRPW and TCPW.

Remarks 1. This is the timing for the following case.
Wait count based on the RPC1n and RPC0n bits of the DRCn register (TRPW): 1
Wait count based on the RHC1n and RHC0n bits of the DRCn register (TRHW): 1
Wait count based on the DAC1n and DAC0n bits of the DRCn register (TDAW): 1
Wait count based on the CPC1n and CPC0n bits of the DRCn register (TCPW): 1

2. The broken lines indicate high impedance.

3. n = 1, 3, 4, 6, m = 0 to 3

(e) CBR refresh timing

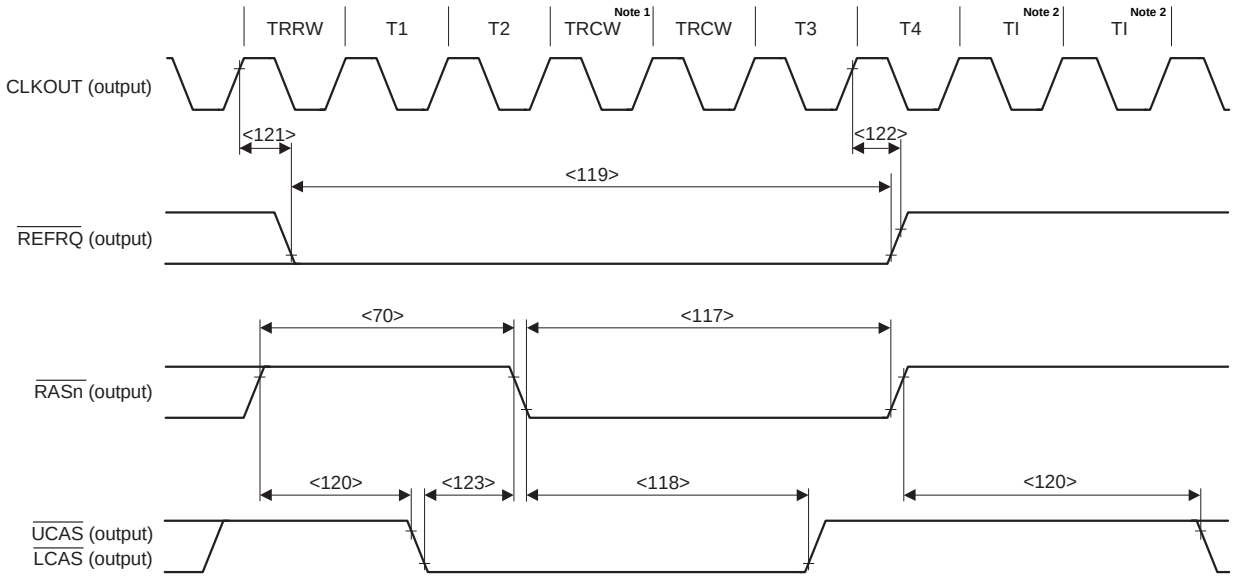
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{RAS}$ precharge time	<70>	t_{RP}		$(1.5 + w_{RRW})T - 10$		ns
$\overline{RAS}$ pulse width	<117>	t_{RAS}		$(1.5 + w_{RCW}^{Note})T - 10$		ns
$\overline{CAS}$ hold time	<118>	t_{CHR}		$(0.5 + w_{RCW}^{Note})T - 10$		ns
$\overline{REFRQ}$ pulse width	<119>	t_{WRFL}		$(3 + w_{RRW} + w_{RCW}^{Note})T - 10$		ns
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	<120>	t_{RPC}		$(2.5 + w_{RRW})T - 10$		ns
$\overline{REFRQ}$ active delay time (from CLKOUT↑)	<121>	t_{DKRF}		2	13	ns
$\overline{REFRQ}$ inactive delay time (from CLKOUT↑)	<122>	t_{HKRF}		2	13	ns
$\overline{CAS}$ setup time	<123>	t_{CSR}		T – 10		ns

Note At least one clock is always inserted in w_{RCW} by default, regardless of the settings of the RCW0 to RCW2 bits of the RWC register.

Remarks 1. $T = t_{CYK}$

2. w_{RRW}: Wait count based on the RRW0 and RRW1 bits of the RWC register

3. w_{RCW}: Wait count based on the RCW0 to RCW2 bits of the RWC register



Notes 1. At least one clock is always inserted in TRCW, regardless of the settings of the RCW0 to RCW2 bits of the RWC register.

2. Idle state (TI) independent of the setting of the BCC register

Remarks 1. This is the timing for the following case.
Wait count based on the RRW0 and RRW1 bits of the RWC register (TRRW): 1
Wait count based on the RCW0 to RCW2 bits of the RWC register (TRCW): 2

2. n = 0 to 7

(f) CBR self-refresh timing

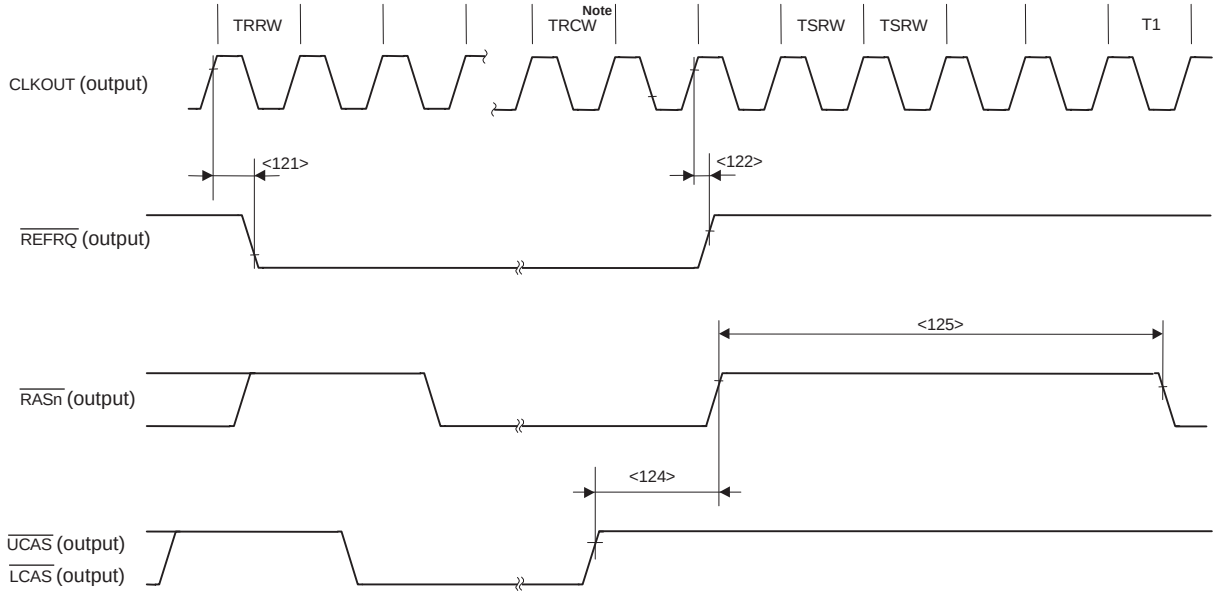
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{REFRQ}}$ active delay time (from CLKOUT↑)	<121>	t_{DKRF}		2	13	ns
$\overline{\text{REFRQ}}$ inactive delay time (from CLKOUT↑)	<122>	t_{HKRF}		2	13	ns
$\overline{\text{CAS}}$ hold time	<124>	t_{CHS}		$-(w_{RCW}T - 10)$		ns
$\overline{\text{RAS}}$ precharge time	<125>	t_{RPS}	$w_{RP} = 0$	$(3 + 2w_{SRW})T - 10$		ns
			$w_{RP} \geq 1$	$(2 + 2w_{SRW} + w_{RPW})T - 10$		ns

Remarks 1. $T = t_{CYK}$

2. w_{SRW}: Wait count based on the SRW0 to SRW2 bits of the RWC register

3. w_{RCW}: Wait count based on the RCW0 to RCW2 bits of the RWC register

4. w_{RPW}: Wait count based on the RRW0 and RRW1 bits of the RWC register



Note At least one clock is always inserted in TRCW, regardless of the settings of the RCW0 to RCW2 bits of the RWC register.

Remarks 1. This is the timing for the following case.
Wait count based on the RRW0 and RRW1 bits of the RWC register (TRRW): 1
Wait count based on the RCW0 to RCW2 bits of the RWC register (TRCW): 1
Wait count based on the SRW0 to SRW2 bits of the RWC register (TSRW): 1 (twice the number of waits as the set value are inserted)

2. The broken lines indicate high impedance.

3. n = 0 to 7

(7) SDRAM access timing

(a) Read timing (SDRAM access) (1/2)

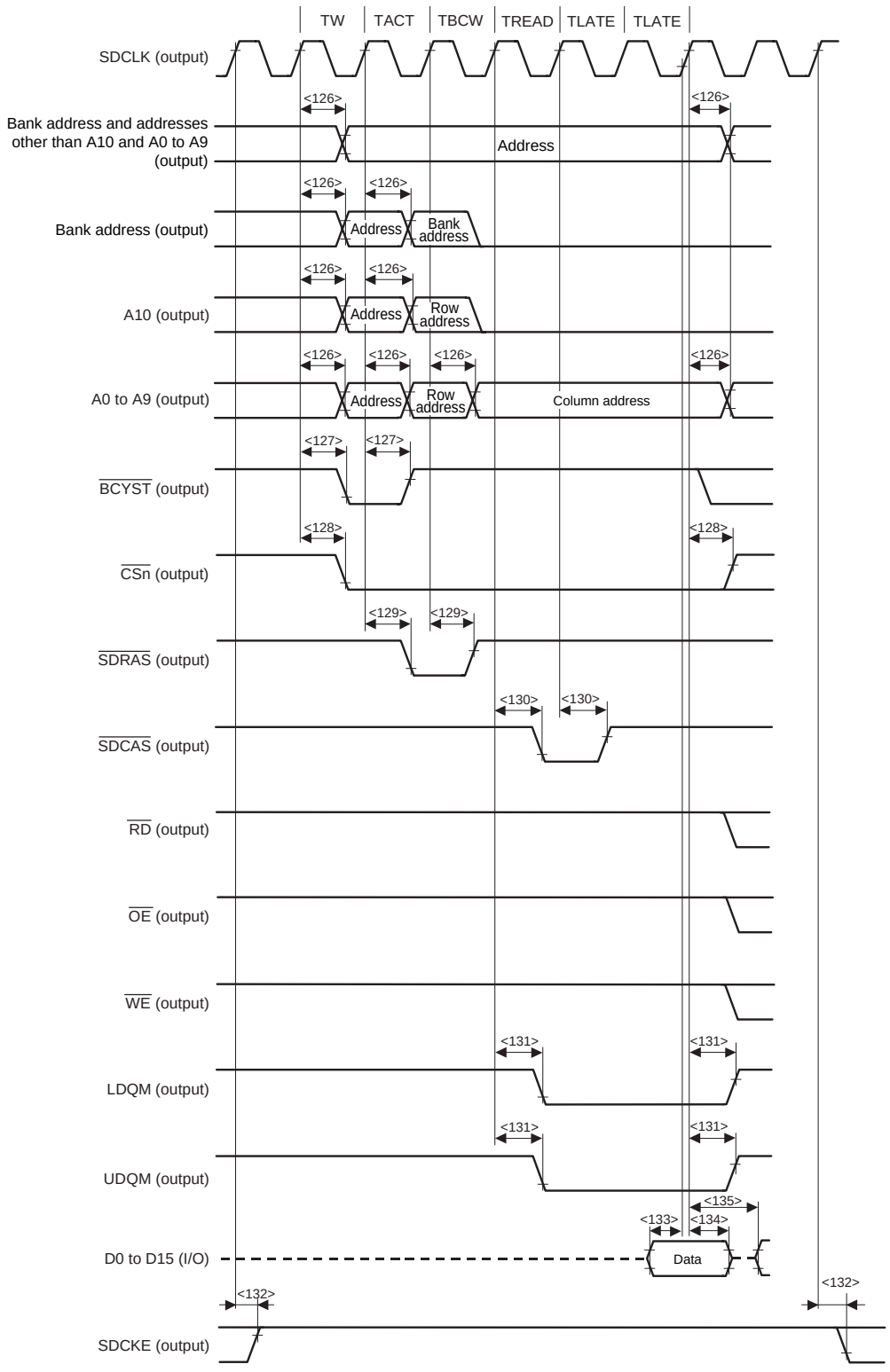
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address delay time (from SDCLK↑)	<126>	t_{DKA}		2	13	ns
$\overline{BCYST}$ delay time (from SDCLK↑)	<127>	t_{DKBC}		2	13	ns
$\overline{CSn}$ delay time (from SDCLK↑)	<128>	t_{DKCS}		2	13	ns
$\overline{SDRAS}$ delay time (from SDCLK↑)	<129>	t_{DKRAS}		2	13	ns
$\overline{SDCAS}$ delay time (from SDCLK↑)	<130>	t_{DKCAS}		2	13	ns
UDQM, LDQM delay time (from SDCLK↑)	<131>	t_{DKDQM}		2	13	ns
SDCKE delay time (from SDCLK↑)	<132>	t_{DKCKE}		2	13	ns
Data input setup time (at SDRAM read, to SDCLK↑)	<133>	t_{SDRMK}		8		ns
Data input hold time (at SDRAM read, from SDCLK↑)	<134>	t_{HKDRM}		0		ns
Delay time from SDCLK↑ to data output	<135>	t_{DSDOD}			(1 + i) T – 5	ns

Remarks 1. T = t_{CYK2}

2. i = Idle state count

3. n = 1, 3, 4, 6

(a) Read timing (SDRAM access) (2/2)



Remarks 1. Wait count based on the BCW1n and BCW0n bits of the SCRn register (TBCW): 2

2. The broken lines indicate high impedance.

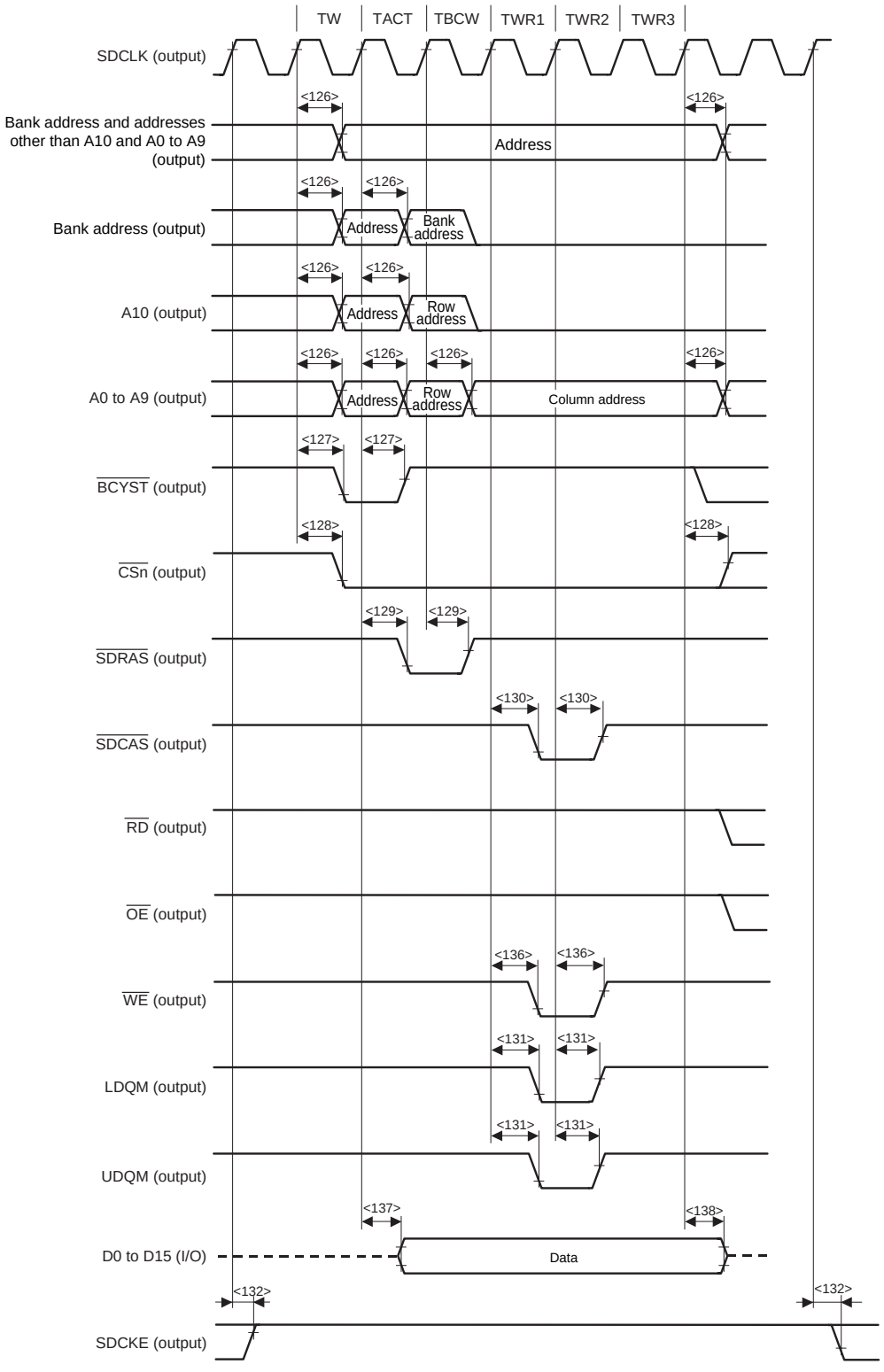
3. n = 1, 3, 4, 6

(b) Write timing (SDRAM access) (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address delay time (from SDCLK↑)	<126>	t_{DKA}		2	13	ns
$\overline{\text{BCYST}}$ delay time (from SDCLK↑)	<127>	t_{DKBC}		2	13	ns
$\overline{\text{CSn}}$ delay time (from SDCLK↑)	<128>	t_{DKCS}		2	13	ns
$\overline{\text{SDRAS}}$ delay time (from SDCLK↑)	<129>	t_{DKRAS}		2	13	ns
$\overline{\text{SDCAS}}$ delay time (from SDCLK↑)	<130>	t_{DKCAS}		2	13	ns
UDQM, LDQM delay time (from SDCLK↑)	<131>	t_{DKDQM}		2	13	ns
SDCKE delay time (from SDCLK↑)	<132>	t_{DKCKE}		2	13	ns
$\overline{\text{WE}}$ delay time (from SDCLK↑)	<136>	t_{DKWE}		2	13	ns
Data output delay time (from SDCLK↑)	<137>	t_{DKDT}		2	13	ns
Data float delay time (from SDCLK↑)	<138>	t_{HZKDT}		2	13	ns

Remark n = 1, 3, 4, 6

(b) Write timing (SDRAM access) (2/2)



Remarks 1. Wait count based on the BCW1n and BCW0n bits of the SCRn register (TBCW): 2

2. The broken lines indicate high impedance.

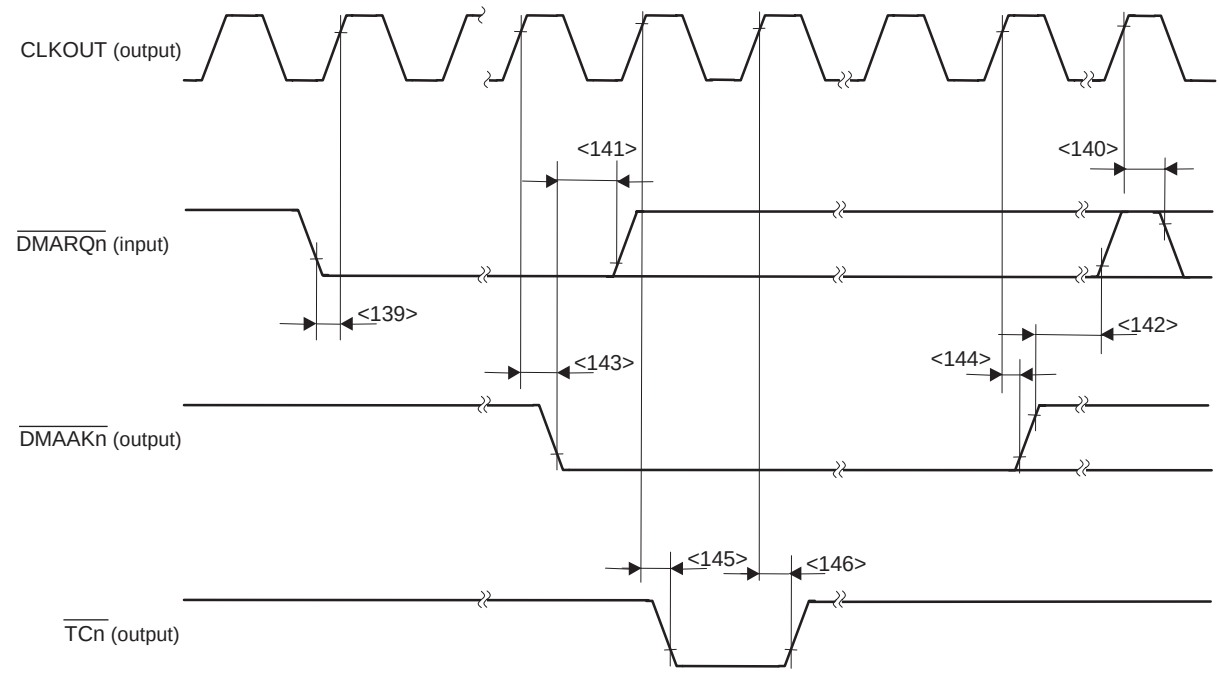
3. n = 1, 3, 4, 6

(8) DMAC timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{DMARQn}}$ setup time (to CLKOUT↑)	<139>	t_{SDRK}		8		ns
$\overline{\text{DMARQn}}$ hold time	<140>	t_{HKDR1}	After inactive (from CLKOUT↑)	3		ns
	<141>	t_{HKDR2}		Until $\overline{\text{DMAAKn}}$↓		ns
Second DMA request disable timing in single transfer	<142>	t_{AKDR}			3T	ns
$\overline{\text{DMAAKn}}$ output delay time (from CLKOUT↑)	<143>	t_{DKDA}		2	13	ns
$\overline{\text{DMAAKn}}$ output hold time (from CLKOUT↑)	<144>	t_{HKDA}		2	13	ns
$\overline{\text{TCn}}$ output delay time (from CLKOUT↑)	<145>	t_{HKTC}		2	13	ns
$\overline{\text{TCn}}$ output hold time (from CLKOUT↑)	<146>	t_{HKTC}		2	13	ns

Remarks 1. T = t_{CYK}

2. n = 0 to 3



Remarks 1. In 2-cycle transfer, the $\overline{\text{TCn}}$ signal is output in the write cycle.

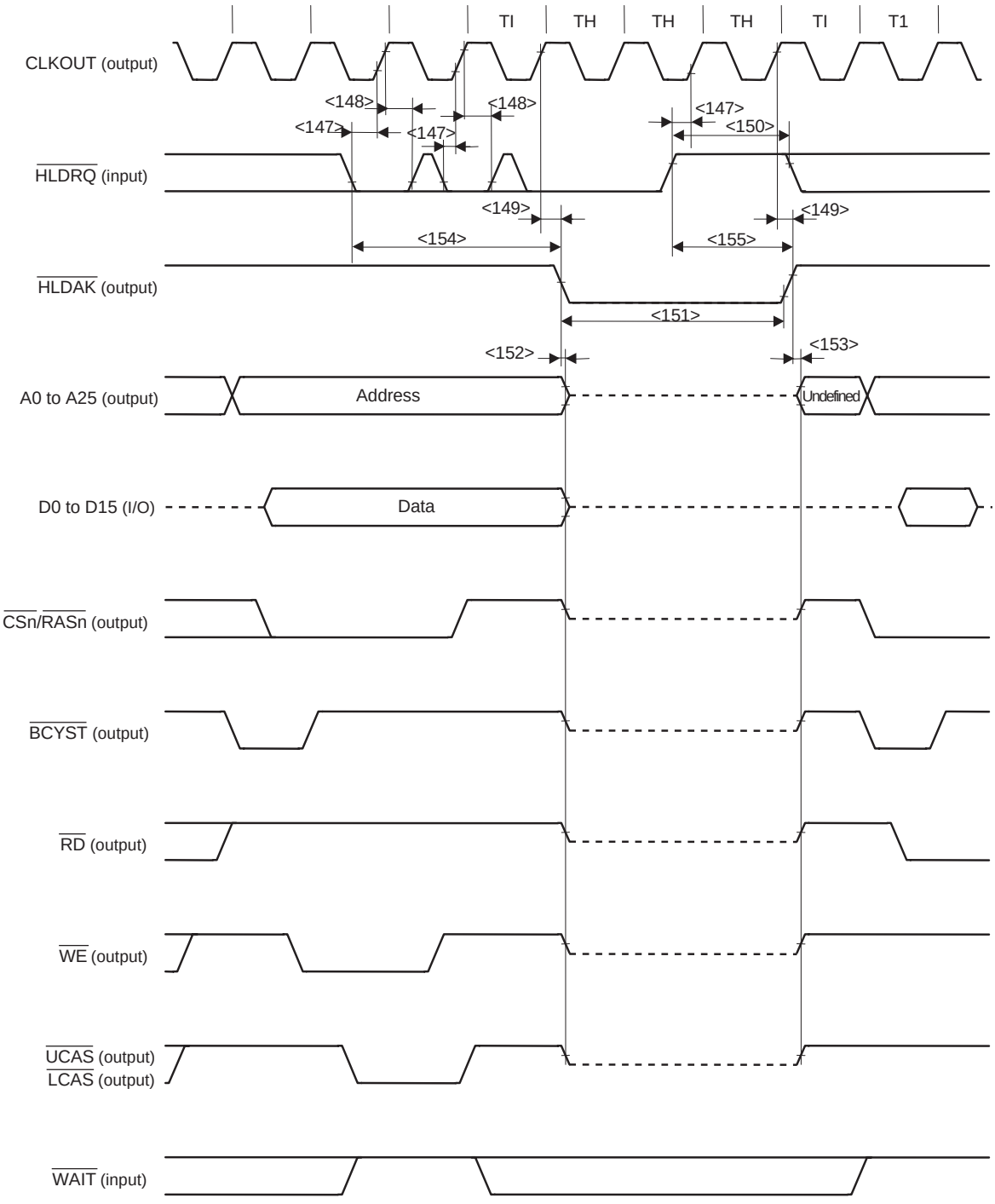
2. n = 0 to 3

(9) Bus hold timing (1/2)

	Parameter	Symbol		Conditions	MIN.	MAX.	Unit
	$\overline{\text{HLDRQ}}$ setup time (to CLKOUT↑)	<147>	t_{SHRK}		8		ns
	$\overline{\text{HLDRQ}}$ hold time (from CLKOUT↑)	<148>	t_{HKHR}		3		ns
	Delay time from CLKOUT↑ to $\overline{\text{HLDAK}}$	<149>	t_{DKHA}		2	13	ns
	$\overline{\text{HLDRQ}}$ high-level width	<150>	t_{WHQH}		T + 3		ns
	$\overline{\text{HLDAK}}$ low-level width	<151>	t_{WHAL}		T − 11		ns
	Delay time from $\overline{\text{HLDAK}}$↓ to bus float	<152>	t_{DKCF}		0		ns
	Delay time from $\overline{\text{HLDAK}}$↑ to bus output	<153>	t_{DHAC}		2	13	ns
	Delay time from $\overline{\text{HLDRQ}}$↓ to $\overline{\text{HLDAK}}$↓	<154>	t_{DHQHA1}		2T		ns
★	Delay time from $\overline{\text{HLDRQ}}$↑ to $\overline{\text{HLDAK}}$↑	<155>	t_{DHQHA2}		T	2T + 10	ns

Remark T = t_{CYK}

(9) Bus hold timing (2/2)



Remarks 1. The broken lines indicate high impedance.

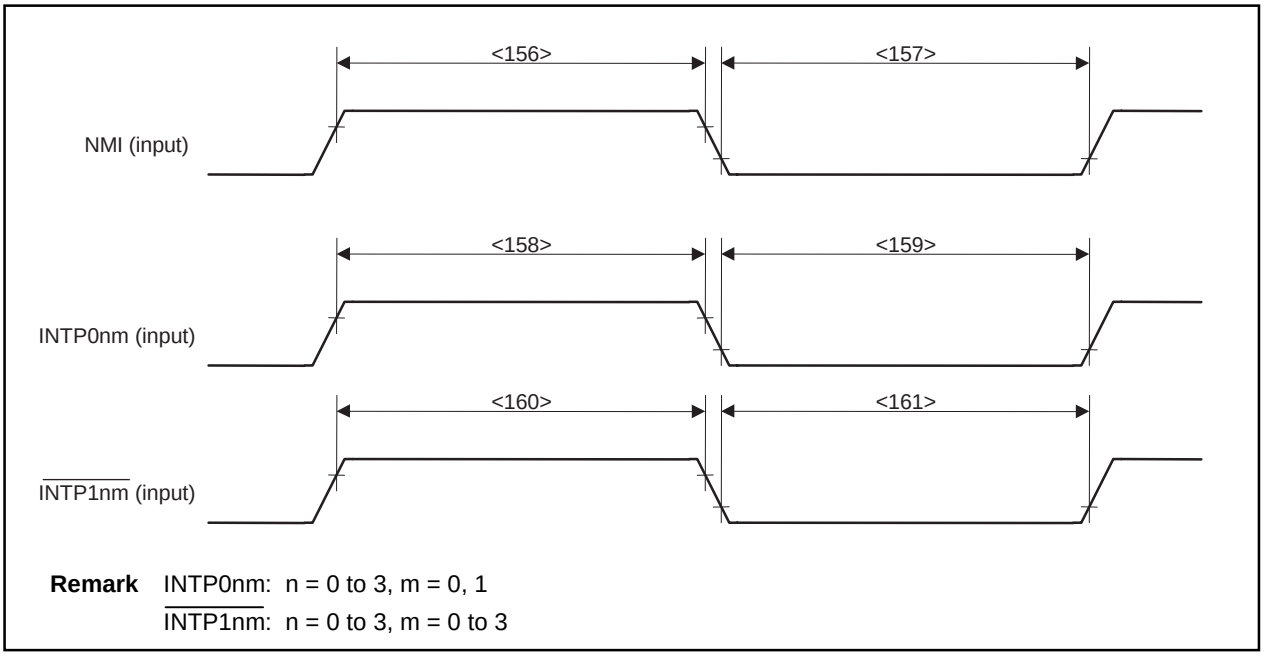
2. n = 0 to 7

(10) Interrupt timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
NMI high-level width	<156>	t_{WNIH}		500		ns
NMI low-level width	<157>	t_{WNIL}		500		ns
INTP0nm high-level width	<158>	t_{WIT0H}		3T + 500		ns
INTP0nm low-level width	<159>	t_{WIT0L}		3T + 500		ns
$\overline{\text{INTP1nm}}$ high-level width	<160>	t_{WIT1H}		500		ns
$\overline{\text{INTP1nm}}$ low-level width	<161>	t_{WIT1L}		500		ns

Remarks 1. INTP0nm: n = 0 to 3, m = 0, 1
$\overline{\text{INTP1nm}}$: n = 0 to 3, m = 0 to 3

2. T = t_{CYK}



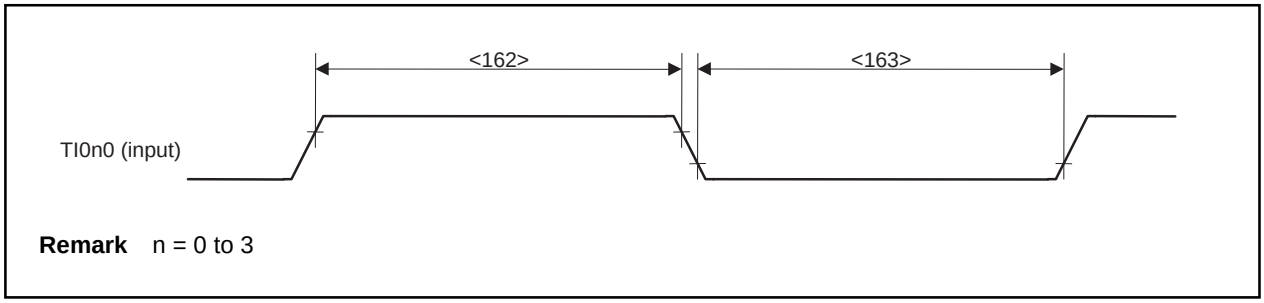
Remark INTP0nm: n = 0 to 3, m = 0, 1
$\overline{\text{INTP1nm}}$: n = 0 to 3, m = 0 to 3

(11) RPU timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
TI0n0 high-level width	<162>	t_{WTIH}		3T + 500		ns
TI0n0 low-level width	<163>	t_{WTIL}		3T + 500		ns

Remarks 1. n = 0 to 3

2. T = t_{CYK}



Remark n = 0 to 3

(12) CSI0 to CSI2 timing

(a) Master mode

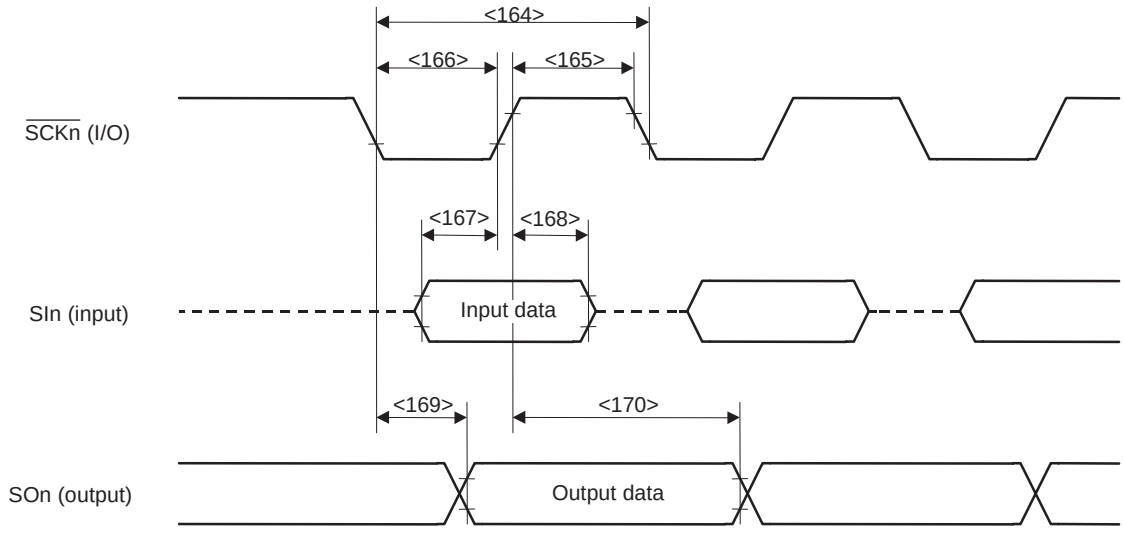
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<164>	t_{CYSK1}	Output	320		ns
$\overline{SCKn}$ high-level width	<165>	t_{WSK1H}	Output	$0.5t_{CYSK1} - 20$		ns
$\overline{SCKn}$ low-level width	<166>	t_{WSK1L}	Output	$0.5t_{CYSK1} - 20$		ns
SIn setup time (to $\overline{SCKn}$↑)	<167>	t_{SSISK}		30		ns
SIn hold time (from $\overline{SCKn}$↑)	<168>	t_{HSKSI}		30		ns
SOn output delay time (from $\overline{SCKn}$↓)	<169>	t_{DSKSO}			30	ns
SOn output hold time (from $\overline{SCKn}$↑)	<170>	t_{HSKSO}		$0.5t_{CYSK1} - 5$		ns

Remark n = 0 to 2

(b) Slave mode

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<164>	t_{CYSK1}	Input	200		ns
$\overline{SCKn}$ high-level width	<165>	t_{WSK1H}	Input	90		ns
$\overline{SCKn}$ low-level width	<166>	t_{WSK1L}	Input	90		ns
SIn setup time (to $\overline{SCKn}$↑)	<167>	t_{SSISK}		50		ns
SIn hold time (from $\overline{SCKn}$↑)	<168>	t_{HSKSI}		50		ns
SOn output delay time (from $\overline{SCKn}$↓)	<169>	t_{DSKSO}			50	ns
SOn output hold time (from $\overline{SCKn}$↑)	<170>	t_{HSKSO}		t_{WSK1H}		ns

Remark n = 0 to 2



Remarks 1. The broken lines indicate high impedance.

2. n = 0 to 2

A/D Converter Characteristics

(T_A = –40 to +85°C, V_{DD} = AV_{DD} = 3.0 to 3.6 V, V_{SS} = AV_{SS} = 0 V, load capacitance of output pins: C_L = 50 pF)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
	Resolution	–		10			bit
★	Total error	–				±5	LSB
	Quantization error	–				±1/2	LSB
	Conversion time	t_{CONV}		5		10	μs
★	Sampling time	t_{SAMP}		Conversion clock[Note]/6			ns
★	Zero scale error	–				±5	LSB
★	Scale error	–				±5	LSB
★	Linearity error	–				±4	LSB
	Analog input voltage	V_{WASN}		–0.3		AV_{REF} + 0.3	V
	AV_{REF} input voltage	AV_{REF}	AV_{REF} = AV_{DD}	3.0		3.6	V
	AV_{DD} power supply current	AI_{DD}				10	mA

Note The conversion clock is a clock count set by the ADM1 register.

4.2 Flash Memory Programming Mode

★ **Basic Characteristics (T_A = 10 to 40°C (during rewrite), T_A = –40 to +85°C (except during rewrite), V_{DD} = AV_{DD} = 3.0 to 3.6 V, V_{SS} = AV_{SS} = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_X		4		50	MHz
V_{PP} supply voltage	V_{PP1}	During flash memory programming	7.5	7.8	8.1	V
	V_{PPL}	V_{PP} low-level detection	$0.8V_{DD}$	V_{DD}	$1.2V_{DD}$	V
	V_{PPM}	V_{PP}, V_{DD} level detection	$0.65V_{DD}$		V_{DD} + 0.3	V
	V_{PPH}	V_{PP} high-voltage level detection	7.5	7.8	8.1	V
V_{DD} supply current	I_{DD}	V_{PP} = V_{PP1}			4.6fx	mA
V_{PP} supply current	I_{PP}	V_{PP} = 7.8 V			100	mA
Step erase time	t_{ER}	**Note 1**	0.398	0.4	0.402	s
Overall erase time per area	t_{ERA}	When the step erase time = 0.4 s **Note 2**			40	s/area
Write-back time	t_{WB}	**Note 3**	0.99	1	1.01	ms
Number of write-backs per write-back command	C_{WB}	When the write-back time = 1 ms **Note 4**			300	Count/write-back command
Number of erase/write-backs	C_{ERWB}				16	Count
Step writing time	t_{WT}	**Note 5**	18	20	22	μs
Overall writing time per word	t_{WTW}	When the step writing time = 20 μs (1 word = 4 bytes) **Note 6**	20		200	μs/word
Number of rewrites per area	C_{ERWR}	1 erase + 1 write after erase = 1 rewrite **Note 7**	20			Count/area

Notes 1. The recommended setting value of the step erase time is 0.4 s.

2. The prewrite time prior to erasure and the erase verify time (write-back time) are not included.

3. The recommended setting value of the write-back time is 1 ms.

4. Write-back is executed once by the issuance of the write-back command. Therefore, the retry count must be the maximum value minus the number of commands issued.

5. The recommended setting value of the step writing time is 20 μs.

6. 100 μs is added to the actual writing time per word. The internal verify time during and after the writing is not included.

7. When writing initially to shipped products, it is counted as one rewrite for both “erase to write” and “write only”.

Example (P: Write, E: Erase)

Shipped product ⟶ P → E → P → E → P: 3 rewrites

Shipped product → E → P → E → P → E → P: 3 rewrites

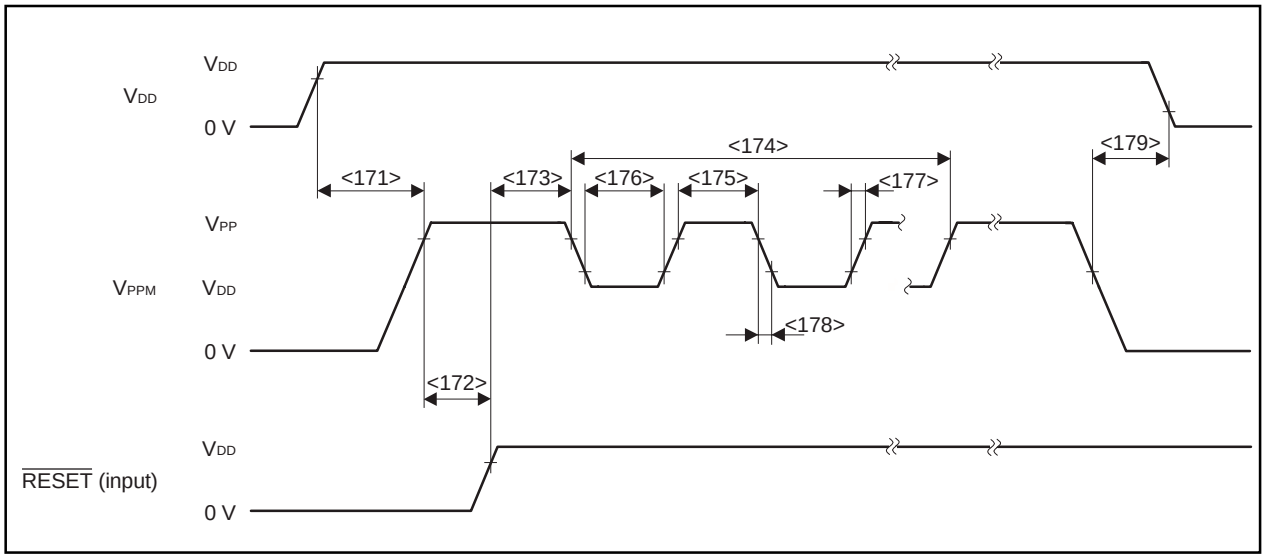
Remarks 1. When the PG-FP3 is used, a time parameter required for writing/erasing by downloading parameter files is automatically set. Do not change the settings otherwise specified.

2. Area 0 = 00000H to 1FFFFH, area 1 = 20000H to 3FFFFH

Serial Write Operation Characteristics

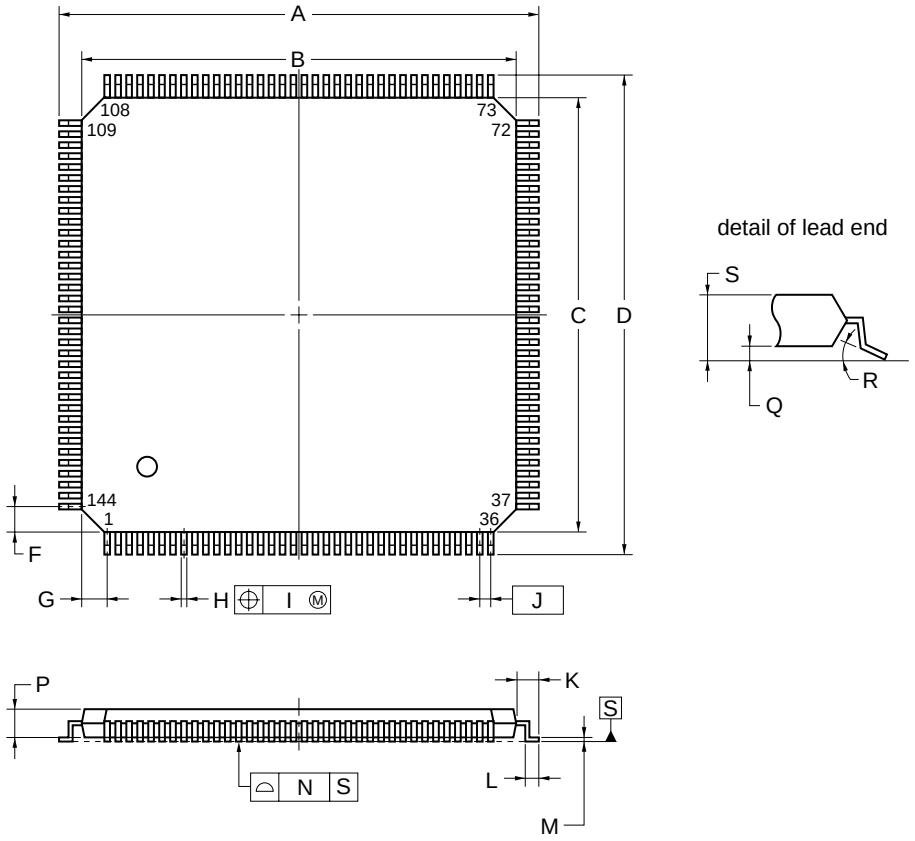
Parameter	Symbol		Conditions	MIN.	TYP.	MAX.	Unit
V_{DD}↑ to V_{PP}↑ set time	<171>	t_{DRPSR}		10			μs
V_{PP}↑ to $\overline{RESET}$↑ set time	<172>	t_{PSRRF}		1			μs
$\overline{RESET}$↑ to V_{PP} count start time	<173>	t_{RFOF}	V_{PP} = 7.8 V	10T + 1500			ns
Count execution time	<174>	t_{COUNT}				15	ms
V_{PP} counter high-level width	<175>	t_{CH}		1			μs
V_{PP} counter low-level width	<176>	t_{CL}		1			μs
V_{PP} counter rise time	<177>	t_R				1	μs
V_{PP} counter fall time	<178>	t_F				1	μs
V_{PP}↓ to V_{DD}↓ reset time	<179>	t_{PFDR}		10			μs

Remark T = t_{CYK}



5. PACKAGE DRAWING

144-PIN PLASTIC LQFP (FINE PITCH) (20x20)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	22.0±0.2
B	20.0±0.2
C	20.0±0.2
D	22.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.4
Q	0.10±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.5±0.1

S144GJ-50-UEN

6. RECOMMENDED SOLDERING CONDITIONS

Undetermined

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Related document: μPD703106, 703107 Data Sheet (U14792E)

Reference document: Electrical Characteristics for Microcomputer (IEI-601)[Note]

Note This document number is that of the Japanese version.

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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