NEC

MOS INTEGRATED CIRCUITS

# μPD70F3102A-33

## V850E/MS1™
## 32-BIT SINGLE-CHIP MICROCONTROLLER

### DESCRIPTION

The μPD70F3102A-33 is a product that substitutes the internal mask ROM of the μPD703102A-33 with flash memory. This enables users to perform on-board program writing and erasure, enabling effective evaluation during system development, small-lot production of multiple devices, and rapid production start, and quick development and time-to-market.

A version using a 5.0 V power supply for external pins, the μPD70F3102-33, is also available.

**Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.**

**V850E/MS1 User's Manual Hardware: U12688E**
**V850E/MS1, V850E/MS2™ User's Manual Architecture: U12197E**

### FEATURES

- μPD703102A-33 compatible
  Can be replaced by the μPD703102A-33 with internal mask ROM for mass production
- Internal flash memory: 128 KB

### ORDERING INFORMATION

| Part Number | Package |
|---|---|
| μPD70F3102AF1-33-FA1 | 157-pin plastic FBGA (14 × 14) |
| μPD70F3102AGJ-33-8EU | 144-pin plastic LQFP (fine pitch) (20 × 20) |
| μPD70F3102AGJ-33-UEN[Note] | 144-pin plastic LQFP (fine pitch) (20 × 20) |

**Note** Under development

**The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.**
**Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.**

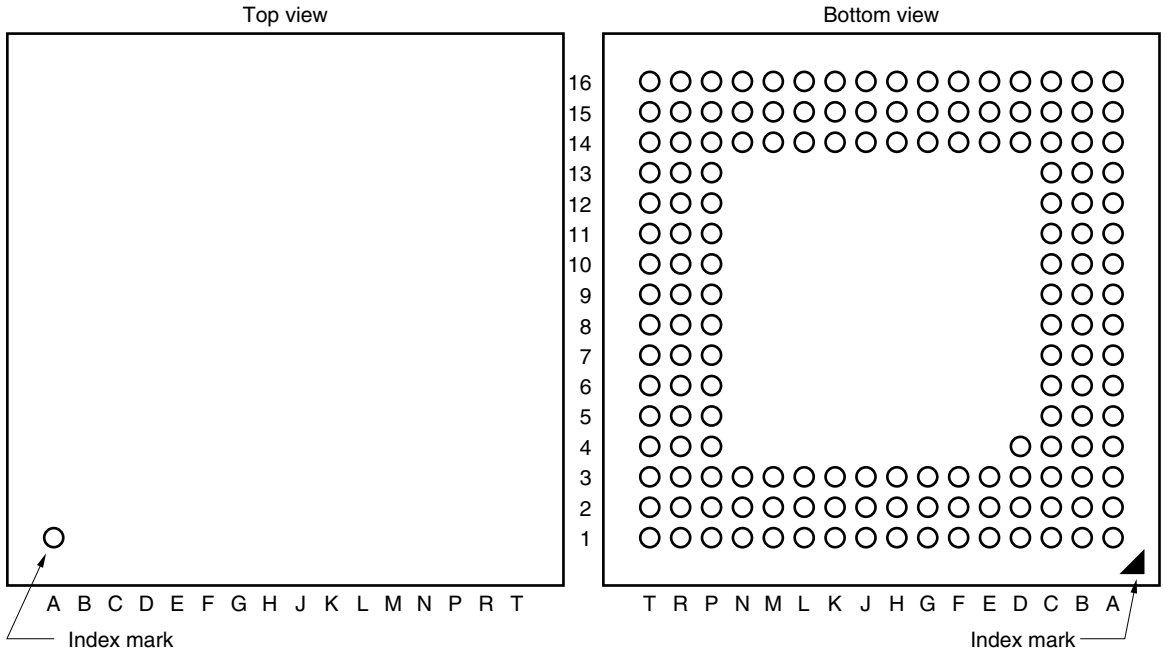
Document No. U13845EJ5V0DS00 (5th edition)
Date Published June 2002 N CP(K)
Printed in Japan

**The mark ⋆ shows major revised points.**

## PIN CONFIGURATION (TOP VIEW)

**157-pin plastic FBGA (14 × 14)**

- **μPD70F3102AF1-33-FA1**

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| Pin No. | Name | Pin No. | Name | Pin No. | Name |
|---|---|---|---|---|---|
| A1 | — | B1 | INTP103/$\overline{\text{DMARQ3}}$/P07 | C1 | INTP101/$\overline{\text{DMARQ1}}$/P05 |
| A2 | D0/P40 | B2 | D1/P41 | C2 | INTP102/$\overline{\text{DMARQ2}}$/P06 |
| A3 | D2/P42 | B3 | D3/P43 | C3 | $V_{SS}$ |
| A4 | D4/P44 | B4 | D5/P45 | C4 | $V_{SS}$ |
| A5 | D6/P46 | B5 | D7/P47 | C5 | $HV_{DD}$ |
| A6 | D8/P50 | B6 | D9/P51 | C6 | $V_{SS}$ |
| A7 | D10/P52 | B7 | D11/P53 | C7 | D12/P54 |
| A8 | D13/P55 | B8 | D14/P56 | C8 | D15/P57 |
| A9 | A0/PA0 | B9 | A1/PA1 | C9 | $HV_{DD}$ |
| A10 | A2/PA2 | B10 | A3/PA3 | C10 | A4/PA4 |
| A11 | A5/PA5 | B11 | A6/PA6 | C11 | A7/PA7 |
| A12 | A8/PB0 | B12 | A9/PB1 | C12 | $V_{SS}$ |
| A13 | A10/PB2 | B13 | A11/PB3 | C13 | A12/PB4 |
| A14 | A13/PB5 | B14 | A14/PB6 | C14 | A18/P62 |
| A15 | A15/PB7 | B15 | A17/P61 | C15 | A19/P63 |
| A16 | — | B16 | A16/P60 | C16 | — |

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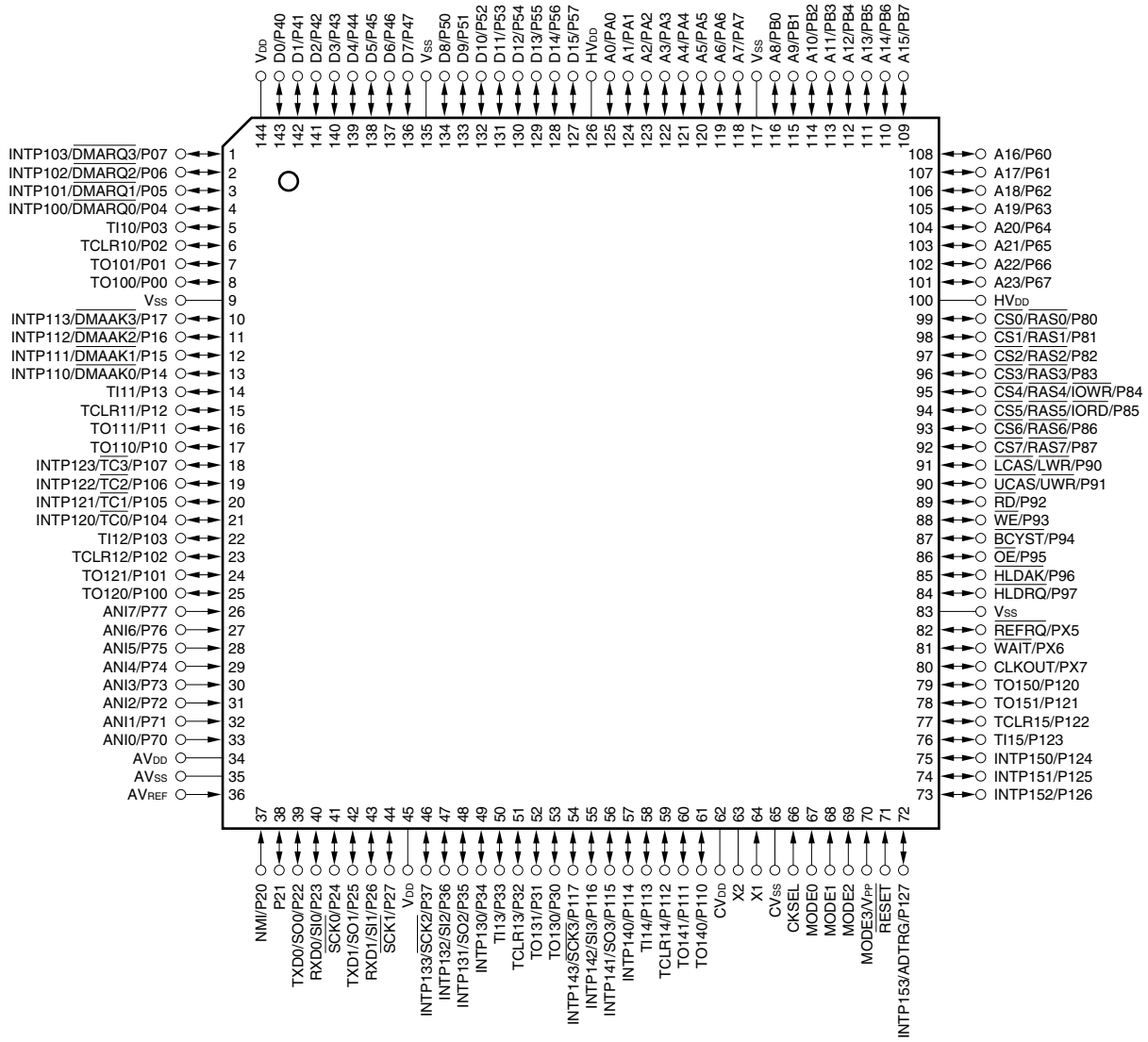
| Pin No. | Name | Pin No. | Name | Pin No. | Name |
|---|---|---|---|---|---|
| D1 | TI10/P03 | K1 | TI12/P103 | P14 | $\overline{\text{RESET}}$ |
| D2 | INTP100/$\overline{\text{DMARQ0}}$/P04 | K2 | INTP120/$\overline{\text{TC0}}$/P104 | P15 | INTP151/P125 |
| D3 | $HV_{DD}$ | K3 | INTP121/$\overline{\text{TC1}}$/P105 | P16 | INTP150/P124 |
| D4 | — | K14 | $\overline{\text{HLDAK}}$/P96 | R1 | $AV_{SS}$ |
| D14 | $V_{SS}$ | K15 | $\overline{\text{OE}}$/P95 | R2 | ANI0/P70 |
| D15 | A21/P65 | K16 | $\overline{\text{BCYST}}$/P94 | R3 | P21 |
| D16 | A20/P64 | L1 | TO120/P100 | R4 | $\overline{\text{SCK0}}$/P24 |
| E1 | TO101/P01 | L2 | TO121/P101 | R5 | $\overline{\text{SCK1}}$/P27 |
| E2 | TCLR10/P02 | L3 | TCLR12/P102 | R6 | INTP132/SI2/P36 |
| E3 | $V_{SS}$ | L14 | $V_{SS}$ | R7 | TI13/P33 |
| E14 | $HV_{DD}$ | L15 | $\overline{\text{REFRQ}}$/PX5 | R8 | TO130/P30 |
| E15 | A23/P67 | L16 | $\overline{\text{HLDRQ}}$/P97 | R9 | INTP141/SO3/P115 |
| E16 | A22/P66 | M1 | ANI5/P75 | R10 | TCLR14/P112 |
| F1 | INTP113/$\overline{\text{DMAAK3}}$/P17 | M2 | ANI6/P76 | R11 | TO140/P110 |
| F2 | TO100/P00 | M3 | ANI7/P77 | R12 | MODE0 |
| F3 | $V_{DD}$ | M14 | TO150/P120 | R13 | MODE1 |
| F14 | $\overline{\text{CS2}}$/$\overline{\text{RAS2}}$/P82 | M15 | $\overline{\text{WAIT}}$/PX6 | R14 | MODE2 |
| F15 | $\overline{\text{CS1}}$/$\overline{\text{RAS1}}$/P81 | M16 | CLKOUT/PX7 | R15 | INTP153/ADTRG/P127 |
| F16 | $\overline{\text{CS0}}$/$\overline{\text{RAS0}}$/P80 | N1 | ANI2/P72 | R16 | INTP152/P126 |
| G1 | INTP110/$\overline{\text{DMAAK0}}$/P14 | N2 | ANI3/P73 | T1 | — |
| G2 | INTP111/$\overline{\text{DMAAK1}}$/P15 | N3 | ANI4/P74 | T2 | $AV_{REF}$ |
| G3 | INTP112/$\overline{\text{DMAAK2}}$/P16 | N14 | TI15/P123 | T3 | NMI/P20 |
| G14 | $\overline{\text{CS5}}$/$\overline{\text{RAS5}}$/$\overline{\text{IORD}}$/P85 | N15 | TCLR15/P122 | T4 | RXD0/SI0/P23 |
| G15 | $\overline{\text{CS4}}$/$\overline{\text{RAS4}}$/$\overline{\text{IOWR}}$/P84 | N16 | TO151/P121 | T5 | RXD1/SI1/P26 |
| G16 | $\overline{\text{CS3}}$/$\overline{\text{RAS3}}$/P83 | P1 | $AV_{DD}$ | T6 | INTP131/SO2/P35 |
| H1 | TO111/P11 | P2 | ANI1/P71 | T7 | TCLR13/P32 |
| H2 | TCLR11/P12 | P3 | TXD0/SO0/P22 | T8 | INTP143/$\overline{\text{SCK3}}$/P117 |
| H3 | TI11/P13 | P4 | TXD1/SO1/P25 | T9 | INTP140/P114 |
| H14 | $\overline{\text{LCAS}}$/$\overline{\text{LWR}}$/P90 | P5 | $V_{DD}$ | T10 | $CV_{DD}$ |
| H15 | $\overline{\text{CS7}}$/$\overline{\text{RAS7}}$/P87 | P6 | INTP133/$\overline{\text{SCK2}}$/P37 | T11 | X2 |
| H16 | $\overline{\text{CS6}}$/$\overline{\text{RAS6}}$/P86 | P7 | INTP130/P34 | T12 | X1 |
| J1 | INTP122/$\overline{\text{TC2}}$/P106 | P8 | TO131/P31 | T13 | $CV_{SS}$ |
| J2 | INTP123/$\overline{\text{TC3}}$/P107 | P9 | INTP142/SI3/P116 | T14 | MODE3/$V_{PP}$ |
| J3 | TO110/P10 | P10 | TI14/P113 | T15 | — |
| J14 | $\overline{\text{WE}}$/P93 | P11 | TO141/P111 | T16 | — |
| J15 | $\overline{\text{RD}}$/P92 | P12 | CKSEL | — | — |
| J16 | $\overline{\text{UCAS}}$/$\overline{\text{UWR}}$/P91 | P13 | $HV_{DD}$ | — | — |

**Remark** Leave pins A1, A16, C16, D4, T1, T15, and T16 open.

**144-pin plastic LQFP (fine pitch) (20 × 20)**

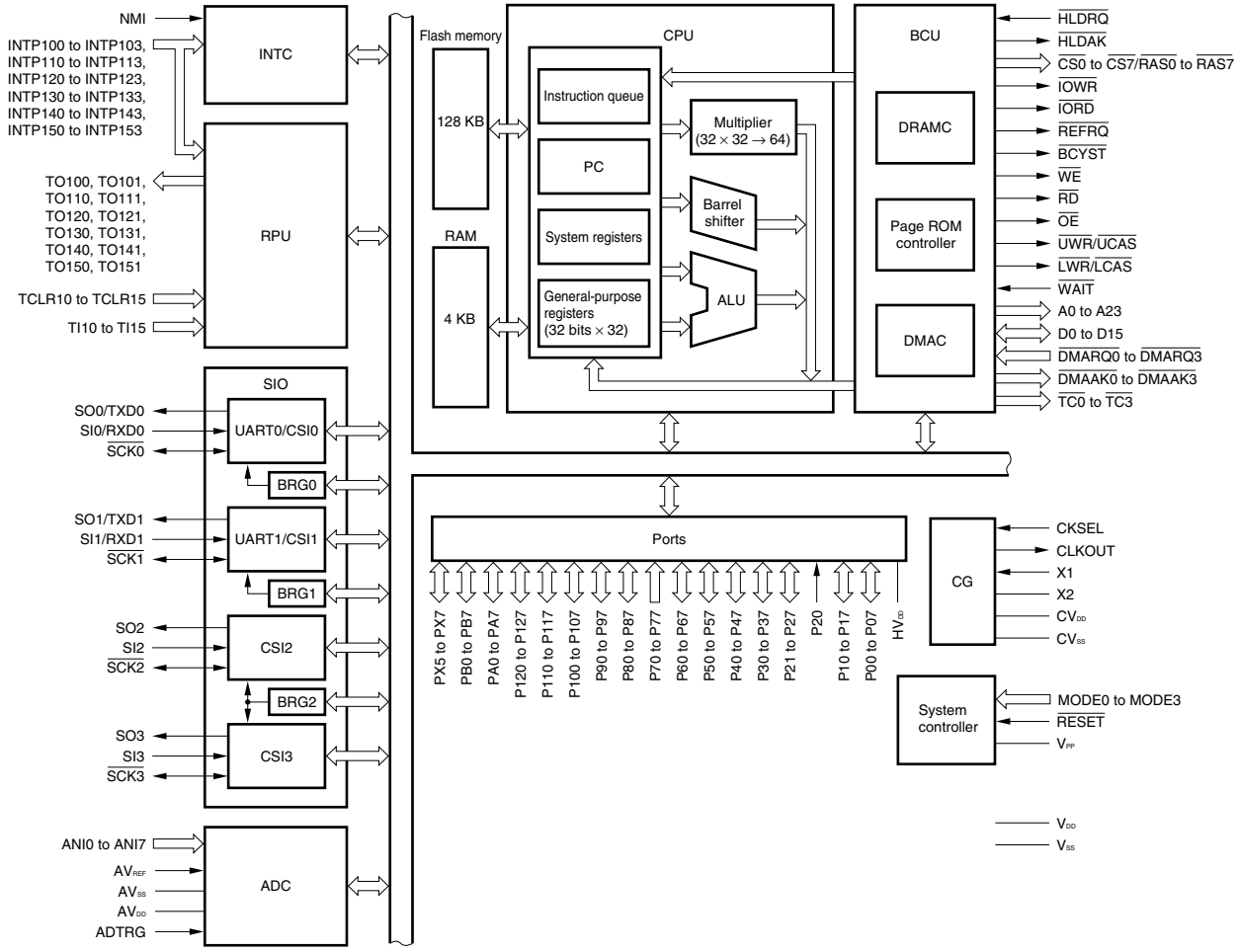
- **μPD70F3102AGJ-33-8EU**
- **μPD70F3102AGJ-33-UEN**



## PIN IDENTIFICATION

| | | | |
|---|---|---|---|
| A0 to A23: | Address bus | P50 to P57: | Port 5 |
| ADTRG: | A/D trigger input | P60 to P67: | Port 6 |
| ANI0 to ANI7: | Analog input | P70 to P77: | Port 7 |
| $AV_{DD}$: | Analog power supply | P80 to P87: | Port 8 |
| $AV_{REF}$: | Analog reference voltage | P90 to P97: | Port 9 |
| $AV_{SS}$: | Analog ground | P100 to P107: | Port 10 |
| $\overline{BCYST}$: | Bus cycle start timing | P110 to P117: | Port 11 |
| CKSEL: | Clock generator operating mode | P120 to P127: | Port 12 |
| | Select | PA0 to PA7: | Port A |
| CLKOUT: | Clock output | PB0 to PB7: | Port B |
| $\overline{CS0}$ to $\overline{CS7}$: | Chip select | PX5 to PX7: | Port X |
| $CV_{DD}$: | Clock generator power supply | $\overline{RAS0}$ to $\overline{RAS7}$: | Row address strobe |
| $CV_{SS}$: | Clock generator | $\overline{RD}$: | Read strobe |
| D0 to D15: | Data bus | $\overline{REFRQ}$: | Refresh request |
| $\overline{DMAAK0}$ to $\overline{DMAAK3}$: | DMA acknowledge | $\overline{RESET}$: | Reset |
| $\overline{DMARQ0}$ to $\overline{DMARQ3}$: | DMA request | RXD0, RXD1: | Receive data |
| $\overline{HLDAK}$: | Hold acknowledge | $\overline{SCK0}$ to $\overline{SCK3}$: | Serial clock |
| $\overline{HLDRQ}$: | Hold request | SI0 to SI3: | Serial input |
| $HV_{DD}$: | Power supply for external pins | SO0 to SO3: | Serial output |
| INTP100 to INTP103, | | $\overline{TC0}$ to $\overline{TC3}$: | Terminal count signal |
| INTP110 to INTP113, | | TCLR10 to TCLR15: | Timer clear |
| INTP120 to INTP123, | | TI10 to TI15: | Timer input |
| INTP130 to INTP133, | | TO100, TO101, | |
| INTP140 to INTP143, | | TO110, TO111, | |
| INTP150 to INTP153: | Interrupt request from peripherals | TO120, TO121, | |
| $\overline{IORD}$: | I/O read strobe | TO130, TO131, | |
| $\overline{IOWR}$: | I/O write strobe | TO140, TO141, | |
| $\overline{LCAS}$: | Lower column address strobe | TO150, TO151: | Timer output |
| $\overline{LWR}$: | Lower write strobe | TXD0, TXD1: | Transmit data |
| MODE0 to MODE3: | Mode | $\overline{UCAS}$: | Upper column address strobe |
| NMI: | Non-maskable interrupt request | $\overline{UWR}$: | Upper write strobe |
| $\overline{OE}$: | Output enable | $V_{DD}$: | Power supply for internal unit |
| P00 to P07: | Port 0 | $V_{PP}$: | Programming power supply |
| P10 to P17: | Port 1 | $V_{SS}$: | Ground |
| P20 to P27: | Port 2 | $\overline{WAIT}$: | Wait |
| P30 to P37: | Port 3 | $\overline{WE}$: | Write enable |
| P40 to P47: | Port 4 | X1, X2: | Crystal |

## INTERNAL BLOCK DIAGRAM



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# 1. DIFFERENCES AMONG PRODUCTS

## 1.1 Differences Between μPD70F3102A-33 and μPD703102A-33

| Item \ Product | μPD70F3102A-33 | μPD703102A-33 |
|---|---|---|
| Internal ROM | Flash memory | Mask ROM |
| Flash memory programming pin | Provided ($V_{PP}$) | None |
| Flash memory programming mode | Provided (MODE0 = L, MODE1 = H, MODE2 = L, MODE3/$V_{PP}$ = 7.8 V) | None |
| Electrical specifications | Consumption current etc. differs (see individual data sheets). | |
| Others | Circuit scale and mask layout differ, thus noise immunity, noise radiation, etc. differ. | |

**Cautions 1. There are differences in noise immunity and noise radiation between the flash memory version and mask ROM version. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluation for commercial samples (not engineering samples) of the mask ROM version.**

**2. When switching from the flash memory version to the mask ROM version, write the same code to the free area of the internal ROM.**

## 1.2 Differences Between μPD70F3102A-33 and μPD70F3102-33

| Item \ Product | μPD70F3102A-33 | μPD70F3102-33 |
|---|---|---|
| $HV_{DD}$ | 3.0 to 3.6 V | 4.5 to 5.5 V |
| Electrical specifications | See individual data sheets. | |
| Package | • 157-pin plastic FBGA (14 × 14)<br>• 144-pin plastic LQFP (fine pitch) (20 × 20) | • 144-pin plastic LQFP (fine pitch) (20 × 20) |

## 2. PIN FUNCTIONS

### 2.1 Port Pins

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| Pin Name | I/O | Function | Alternate Function |
|---|---|---|---|
| P00 | I/O | Port 0<br>8-bit I/O port<br>Input/output can be specified in 1-bit units. | TO100 |
| P01 | | | TO101 |
| P02 | | | TCLR10 |
| P03 | | | TI10 |
| P04 | | | INTP100/$\overline{\text{DMARQ0}}$ |
| P05 | | | INTP101/$\overline{\text{DMARQ1}}$ |
| P06 | | | INTP102/$\overline{\text{DMARQ2}}$ |
| P07 | | | INTP103/$\overline{\text{DMARQ3}}$ |
| P10 | I/O | Port 1<br>8-bit I/O port<br>Input/output can be specified in 1-bit units. | TO110 |
| P11 | | | TO111 |
| P12 | | | TCLR11 |
| P13 | | | TI11 |
| P14 | | | INTP110/$\overline{\text{DMAAK0}}$ |
| P15 | | | INTP111/$\overline{\text{DMAAK1}}$ |
| P16 | | | INTP112/$\overline{\text{DMAAK2}}$ |
| P17 | | | INTP113/$\overline{\text{DMAAK3}}$ |
| P20 | Input | Port 2<br>P20 is an input-only port.<br>When a valid edge is input, it operates as an NMI input. The status of the NMI input is shown by bit 0 of register P2.<br>P21 to P27 is a 7-bit I/O port.<br>Input/output can be specified in 1-bit units. | NMI |
| P21 | I/O | | — |
| P22 | | | TXD0/SO0 |
| P23 | | | RXD0/SI0 |
| P24 | | | $\overline{\text{SCK0}}$ |
| P25 | | | TXD1/SO1 |
| P26 | | | RXD1/SI1 |
| P27 | | | $\overline{\text{SCK1}}$ |
| P30 | I/O | Port 3<br>8-bit I/O port<br>Input/output can be specified in 1-bit units. | TO130 |
| P31 | | | TO131 |
| P32 | | | TCLR13 |
| P33 | | | TI13 |
| P34 | | | INTP130 |
| P35 | | | INTP131/SO2 |
| P36 | | | INTP132/SI2 |
| P37 | | | INTP133/$\overline{\text{SCK2}}$ |
| P40 to P47 | I/O | Port 4<br>8-bit I/O port<br>Input/output can be specified in 1-bit units. | D0 to D7 |

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| Pin Name | I/O | Function | Alternate Function |
|---|---|---|---|
| P50 to P57 | I/O | Port 5<br>8-bit I/O port<br>Input/output can be specified in 1-bit units. | D8 to D15 |
| P60 to P67 | I/O | Port 6<br>8-bit I/O port<br>Input/output can be specified in 1-bit units. | A16 to A23 |
| P70 to P77 | Input | Port 7<br>8-bit input-only port | ANI0 to ANI7 |
| P80 | I/O | Port 8<br>8-bit I/O port<br>Input/output can be specified in 1-bit units. | $\overline{CS0}$/$\overline{RAS0}$ |
| P81 | | | $\overline{CS1}$/$\overline{RAS1}$ |
| P82 | | | $\overline{CS2}$/$\overline{RAS2}$ |
| P83 | | | $\overline{CS3}$/$\overline{RAS3}$ |
| P84 | | | $\overline{CS4}$/$\overline{RAS4}$/$\overline{IOWR}$ |
| P85 | | | $\overline{CS5}$/$\overline{RAS5}$/$\overline{IORD}$ |
| P86 | | | $\overline{CS6}$/$\overline{RAS6}$ |
| P87 | | | $\overline{CS7}$/$\overline{RAS7}$ |
| P90 | I/O | Port 9<br>8-bit I/O port<br>Input/output can be specified in 1-bit units | $\overline{LCAS}$/$\overline{LWR}$ |
| P91 | | | $\overline{UCAS}$/$\overline{UWR}$ |
| P92 | | | $\overline{RD}$ |
| P93 | | | $\overline{WE}$ |
| P94 | | | $\overline{BCYST}$ |
| P95 | | | $\overline{OE}$ |
| P96 | | | $\overline{HLDAK}$ |
| P97 | | | $\overline{HLDRQ}$ |
| P100 | I/O | Port 10<br>8-bit I/O port<br>Input/output can be specified in 1-bit units. | TO120 |
| P101 | | | TO121 |
| P102 | | | TCLR12 |
| P103 | | | TI12 |
| P104 | | | INTP120/$\overline{TC0}$ |
| P105 | | | INTP121/$\overline{TC1}$ |
| P106 | | | INTP122/$\overline{TC2}$ |
| P107 | | | INTP123/$\overline{TC3}$ |
| P110 | I/O | Port 11<br>8-bit I/O port<br>Input/output can be specified in 1-bit units. | TO140 |
| P111 | | | TO141 |
| P112 | | | TCLR14 |
| P113 | | | TI14 |
| P114 | | | INTP140 |
| P115 | | | INTP141/SO3 |
| P116 | | | INTP142/SI3 |
| P117 | | | INTP143/$\overline{SCK3}$ |

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| Pin Name | I/O | Function | Alternate Function |
|---|---|---|---|
| P120 | I/O | Port 12<br>8-bit I/O port<br>Input/output can be specified in 1-bit units. | TO150 |
| P121 | | | TO151 |
| P122 | | | TCLR15 |
| P123 | | | TI15 |
| P124 | | | INTP150 |
| P125 | | | INTP151 |
| P126 | | | INTP152 |
| P127 | | | INTP153/ADTRG |
| PA0 | I/O | Port A<br>8-bit I/O port<br>Input/output can be specified in 1-bit units. | A0 |
| PA1 | | | A1 |
| PA2 | | | A2 |
| PA3 | | | A3 |
| PA4 | | | A4 |
| PA5 | | | A5 |
| PA6 | | | A6 |
| PA7 | | | A7 |
| PB0 | I/O | Port B<br>8-bit I/O port<br>Input/output can be specified in 1-bit units. | A8 |
| PB1 | | | A9 |
| PB2 | | | A10 |
| PB3 | | | A11 |
| PB4 | | | A12 |
| PB5 | | | A13 |
| PB6 | | | A14 |
| PB7 | | | A15 |
| PX5 | I/O | Port X<br>3-bit I/O port<br>Input/output can be specified in 1-bit units. | $\overline{\text{REFRQ}}$ |
| PX6 | | | $\overline{\text{WAIT}}$ |
| PX7 | | | CLKOUT |

## 2.2 Non-Port Pins

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| Pin Name | I/O | Function | Alternate Function |
|---|---|---|---|
| TO100 | Output | Pulse signal output of timers 10 to 15 | P00 |
| TO101 | | | P01 |
| TO110 | | | P10 |
| TO111 | | | P11 |
| TO120 | | | P100 |
| TO121 | | | P101 |
| TO130 | | | P30 |
| TO131 | | | P31 |
| TO140 | | | P110 |
| TO141 | | | P111 |
| TO150 | | | P120 |
| TO151 | | | P121 |
| TCLR10 | Input | External clear signal input of timers 10 to 15 | P02 |
| TCLR11 | | | P12 |
| TCLR12 | | | P102 |
| TCLR13 | | | P32 |
| TCLR14 | | | P112 |
| TCLR15 | | | P122 |
| TI10 | Input | External count clock input of timers 10 to 15 | P03 |
| TI11 | | | P13 |
| TI12 | | | P103 |
| TI13 | | | P33 |
| TI14 | | | P113 |
| TI15 | | | P123 |
| INTP100 | Input | External maskable interrupt request input, or timer 10 external capture trigger input | P04/$\overline{\text{DMARQ0}}$ |
| INTP101 | | | P05/$\overline{\text{DMARQ1}}$ |
| INTP102 | | | P06/$\overline{\text{DMARQ2}}$ |
| INTP103 | | | P07/$\overline{\text{DMARQ3}}$ |
| INTP110 | Input | External maskable interrupt request input, or timer 11 external capture trigger input | P14/$\overline{\text{DMAAK0}}$ |
| INTP111 | | | P15/$\overline{\text{DMAAK1}}$ |
| INTP112 | | | P16/$\overline{\text{DMAAK2}}$ |
| INTP113 | | | P17/$\overline{\text{DMAAK3}}$ |
| INTP120 | Input | External maskable interrupt request input, or timer 12 external capture trigger input | P104/$\overline{\text{TC0}}$ |
| INTP121 | | | P105/$\overline{\text{TC1}}$ |
| INTP122 | | | P106/$\overline{\text{TC2}}$ |
| INTP123 | | | P107/$\overline{\text{TC3}}$ |

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| Pin Name | I/O | Function | Alternate Function |
|---|---|---|---|
| INTP130 | Input | External maskable interrupt request input, or timer 13 external capture trigger input | P34 |
| INTP131 | | | P35/SO2 |
| INTP132 | | | P36/SI2 |
| INTP133 | | | P37/$\overline{\text{SCK2}}$ |
| INTP140 | Input | External maskable interrupt request input, or timer 14 external capture trigger input | P114 |
| INTP141 | | | P115/SO3 |
| INTP142 | | | P116/SI3 |
| INTP143 | | | P117/$\overline{\text{SCK3}}$ |
| INTP150 | Input | External maskable interrupt request input, or timer 15 external capture trigger input | P124 |
| INTP151 | | | P125 |
| INTP152 | | | P126 |
| INTP153 | | | P127/ADTRG |
| SO0 | Output | CSI0 to CSI3 serial transmission data output (3-wire) | P22/TXD0 |
| SO1 | | | P25/TXD1 |
| SO2 | | | P35/INTP131 |
| SO3 | | | P115/INTP141 |
| SI0 | Input | CSI0 to CSI3 serial reception data input (3-wire) | P23/RXD0 |
| SI1 | | | P26/RXD1 |
| SI2 | | | P36/INTP132 |
| SI3 | | | P116/INTP142 |
| $\overline{\text{SCK0}}$ | I/O | CSI0 to CSI3 serial clock input/output (3-wire) | P24 |
| $\overline{\text{SCK1}}$ | | | P27 |
| $\overline{\text{SCK2}}$ | | | P37/INTP133 |
| $\overline{\text{SCK3}}$ | | | P117/INTP143 |
| TXD0 | Output | UART0 and UART1 serial transmission data output | P22/SO0 |
| TXD1 | | | P25/SO1 |
| RXD0 | Input | UART0 and UART1 serial reception data input | P23/SI0 |
| RXD1 | | | P26/SI1 |
| D0 to D7 | I/O | 16-bit data bus for external memory | P40 to P47 |
| D8 to D15 | | | P50 to P57 |
| A0 to A7 | Output | 24-bit address bus for external memory | PA0 to PA7 |
| A8 to A15 | | | PB0 to PB7 |
| A16 to A23 | | | P60 to P67 |
| $\overline{\text{LWR}}$ | Output | External data bus lower byte write enable signal output | P90/$\overline{\text{LCAS}}$ |
| $\overline{\text{UWR}}$ | Output | External data bus upper byte write enable signal output | P91/$\overline{\text{UCAS}}$ |
| $\overline{\text{RD}}$ | Output | External data bus read strobe signal output | P92 |
| $\overline{\text{WE}}$ | Output | Write enable signal output for DRAM | P93 |
| $\overline{\text{OE}}$ | Output | Output enable signal output for DRAM | P95 |

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| Pin Name | I/O | Function | Alternate Function |
|---|---|---|---|
| $\overline{\text{LCAS}}$ | Output | Column address strobe signal output for lower data of DRAM | P90/$\overline{\text{LWR}}$ |
| $\overline{\text{UCAS}}$ | Output | Column address strobe signal output for higher data of DRAM | P91/$\overline{\text{UWR}}$ |
| $\overline{\text{RAS0}}$ to $\overline{\text{RAS3}}$ | Output | Row address strobe signal output for DRAM | P80/$\overline{\text{CS0}}$ to P83/$\overline{\text{CS3}}$ |
| $\overline{\text{RAS4}}$ | | | P84/$\overline{\text{CS4}}$/$\overline{\text{IOWR}}$ |
| $\overline{\text{RAS5}}$ | | | P85/$\overline{\text{CS5}}$/$\overline{\text{IORD}}$ |
| $\overline{\text{RAS6}}$ | | | P86/$\overline{\text{CS6}}$ |
| $\overline{\text{RAS7}}$ | | | P87/$\overline{\text{CS7}}$ |
| $\overline{\text{BCYST}}$ | Output | Strobe signal output indicating start of bus cycle | P94 |
| $\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ | Output | Chip select signal output | P80/$\overline{\text{RAS0}}$ to P83/$\overline{\text{RAS3}}$ |
| $\overline{\text{CS4}}$ | | | P84/$\overline{\text{RAS4}}$/$\overline{\text{IOWR}}$ |
| $\overline{\text{CS5}}$ | | | P85/$\overline{\text{RAS5}}$/$\overline{\text{IORD}}$ |
| $\overline{\text{CS6}}$ | | | P86/$\overline{\text{RAS6}}$ |
| $\overline{\text{CS7}}$ | | | P87/$\overline{\text{RAS7}}$ |
| $\overline{\text{WAIT}}$ | Input | Control signal input that inserts a wait in the bus cycle | PX6 |
| $\overline{\text{REFRQ}}$ | Output | Refresh request signal output for DRAM | PX5 |
| $\overline{\text{IOWR}}$ | Output | DMA write strobe signal output | P84/$\overline{\text{RAS4}}$/$\overline{\text{CS4}}$ |
| $\overline{\text{IORD}}$ | Output | DMA read strobe signal output | P85/$\overline{\text{RAS5}}$/$\overline{\text{CS5}}$ |
| $\overline{\text{DMARQ0}}$ to $\overline{\text{DMARQ3}}$ | Input | DMA request signal input | P04/INTP100 to P07/INTP103 |
| $\overline{\text{DMAAK0}}$ to $\overline{\text{DMAAK3}}$ | Output | DMA acknowledge signal output | P14/INTP110 to P17/INTP113 |
| $\overline{\text{TC0}}$ to $\overline{\text{TC3}}$ | Output | DMA termination (terminal count) signal output | P104/INTP120 to P107/INTP123 |
| $\overline{\text{HLDAK}}$ | Output | Bus hold acknowledge output | P96 |
| $\overline{\text{HLDRQ}}$ | Input | Bus hold request input | P97 |
| ANI0 to ANI7 | Input | Analog input to A/D converter | P70 to P77 |
| NMI | Input | Non-maskable interrupt request input | P20 |
| CLKOUT | Output | System clock output | PX7 |
| CKSEL | Input | Input that specifies the clock generator's operation mode | — |
| MODE0 to MODE2 | Input | Operation mode specification | — |
| MODE3 | | | $V_{PP}$ |
| $\overline{\text{RESET}}$ | Input | System reset input | — |
| X1 | Input | Connecting system clock resonator. In the case of an external clock, it is input to X1. | — |
| X2 | — | | — |
| ADTRG | Input | A/D converter external trigger input | P127/INTP153 |
| $AV_{REF}$ | Input | Reference voltage applied to A/D converter | — |
| $AV_{DD}$ | — | Positive power supply for A/D converter | — |

(4/4)

| Pin Name | I/O | Function | Alternate Function |
|---|---|---|---|
| $AV_{SS}$ | — | Ground potential for A/D converter | — |
| $CV_{DD}$ | — | Positive power supply for dedicated clock generator | — |
| $CV_{SS}$ | — | Ground potential for dedicated clock generator | — |
| $V_{DD}$ | — | Positive power supply (internal unit power supply) | — |
| $HV_{DD}$ | — | Positive power supply (external pin power supply) | — |
| $V_{SS}$ | — | Ground potential | — |
| $V_{PP}$ | — | High-voltage application pin during program write/verify | MODE3 |

### 2.3 Pin I/O Circuit Types and Recommended Connection of Unused Pins

Table 2-1 shows the I/O circuit type of each pin and the recommended connection of unused pins, and Figure 2-1 shows the schematic circuit diagram for each I/O circuit type.

In the case of connection to $V_{DD}$ or $V_{SS}$ via a resistor, connection of a resistor of 1 to 10 kΩ is recommended.

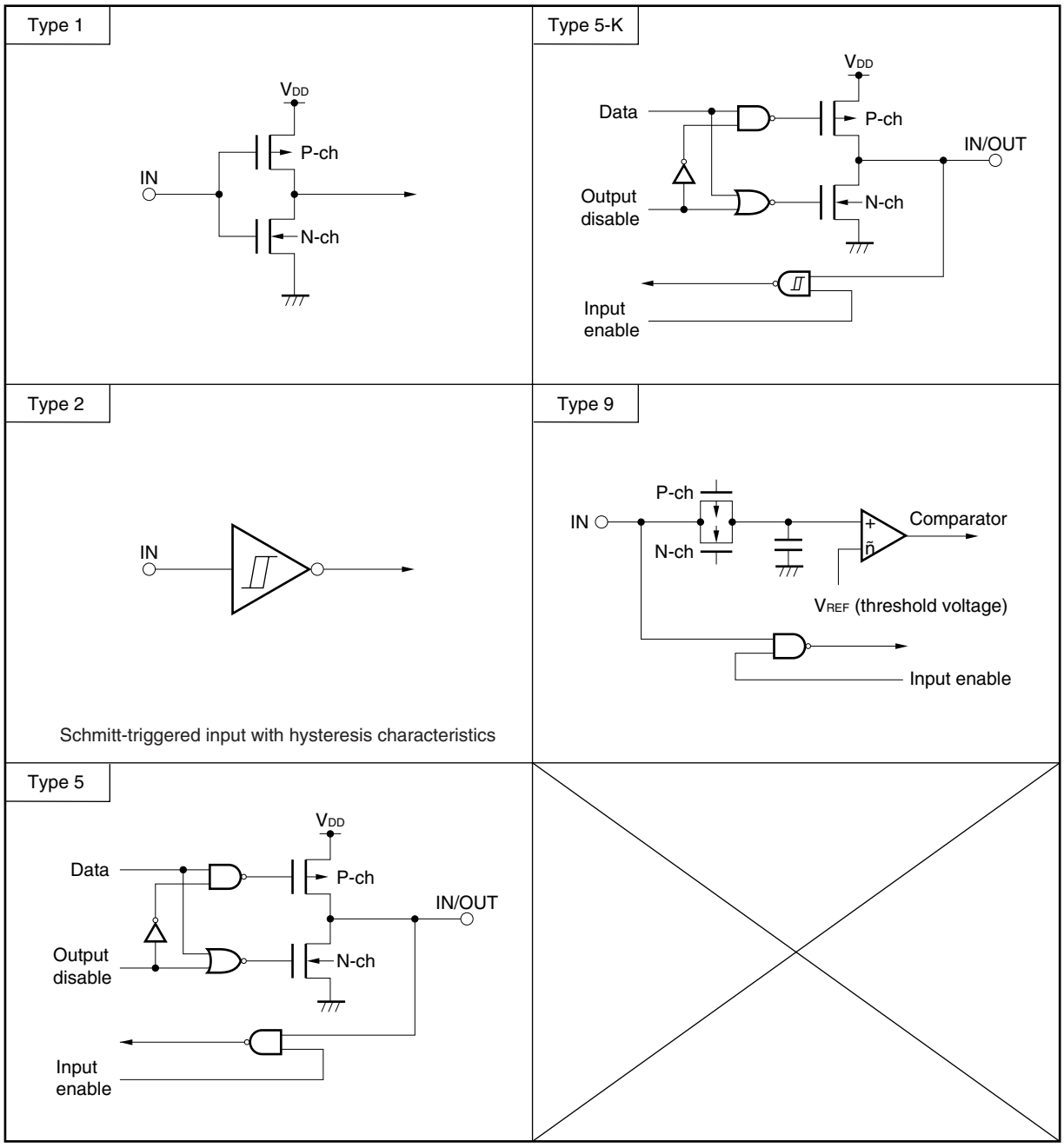
**Table 2-1. Pin I/O Circuit Types and Recommended Connection of Unused Pins (1/2)**

| Pin | I/O Circuit Type | Recommended Connection of Unused Pins |
|---|---|---|
| P00/TO100, P01/TO101 | 5 | Input: Independently connect to $HV_{DD}$ or $V_{SS}$ via a resistor.<br>Output: Leave open. |
| P02/TCLR10, P03/TI10 | 5-K | |
| P04/INTP100/$\overline{\text{DMARQ0}}$ to P07/INTP103/$\overline{\text{DMARQ3}}$ | | |
| P10/TO110, P11/TO111 | 5 | |
| P12/TCLR11, P13/TI11 | 5-K | |
| P14/INTP110/$\overline{\text{DMAAK0}}$ to P17/INTP113/$\overline{\text{DMAAK3}}$ | | |
| P20/NMI | 2 | Connect directly to $V_{SS}$. |
| P21 | 5 | Input: Independently connect to $HV_{DD}$ or $V_{SS}$ via a resistor.<br>Output: Leave open. |
| P22/TXD0/SO0 | | |
| P23/RXD0/SI0 | 5-K | |
| P24/$\overline{\text{SCK0}}$ | | |
| P25/TXD1/SO1 | 5 | |
| P26/RXD1/SI1 | 5-K | |
| P27/$\overline{\text{SCK1}}$ | | |
| P30/TO130, P31/TO131 | 5 | |
| P32/TCLR13, P33/TI13 | 5-K | |
| P34/INTP130 | | |
| P35/INTP131/SO2 | | |
| P36/INTP132/SI2 | | |
| P37/INTP133/$\overline{\text{SCK2}}$ | | |
| P40/D0 to P47/D7 | 5 | |
| P50/D8 to P57/D15 | | |
| P60/A16 to P67/A23 | | |
| P70/ANI0 to P77/ANI7 | 9 | Connect directly to $V_{SS}$. |

**Table 2-1. Pin I/O Circuit Types and Recommended Connection of Unused Pins (2/2)**

| Pin | I/O Circuit Type | Recommended Connection of Unused Pins |
|---|---|---|
| P80/$\overline{CS0}$/$\overline{RAS0}$ to P83/$\overline{CS3}$/$\overline{RAS3}$ | 5 | Input: Independently connect to $HV_{DD}$ or $V_{SS}$ via a resistor.<br>Output: Leave open. |
| P84/$\overline{CS4}$/$\overline{RAS4}$/$\overline{IOWR}$, P85/$\overline{CS5}$/$\overline{RAS5}$/$\overline{IORD}$ | | |
| P86/$\overline{CS6}$/$\overline{RAS6}$, P87/$\overline{CS7}$/$\overline{RAS7}$ | | |
| P90/$\overline{LCAS}$/$\overline{LWR}$ | | |
| P91/$\overline{UCAS}$/$\overline{UWR}$ | | |
| P92/$\overline{RD}$ | | |
| P93/$\overline{WE}$ | | |
| P94/$\overline{BCYST}$ | | |
| P95/$\overline{OE}$ | | |
| P96/$\overline{HLDAK}$ | | |
| P97/$\overline{HLDRQ}$ | | |
| P100/TO120, P101/TO121 | 5 | Input: Independently connect to $HV_{DD}$ or $V_{SS}$ via a resistor.<br>Output: Leave open. |
| P102/TCLR12, P103/TI12 | 5-K | |
| P104/INTP120/$\overline{TC0}$ to P107/INTP123/$\overline{TC3}$ | | |
| P110/TO140, P111/TO141 | 5 | |
| P112/TCLR14, P113/T114 | 5-K | |
| P114/INTP140 | | |
| P115/INTP141/SO3 | | |
| P116/INTP142/SI3 | | |
| P117/INTP143/$\overline{SCK3}$ | | |
| P120/TO150, P121/TO151 | 5 | |
| P122/TCLR15, P123/TI15 | 5-K | |
| P124/INTP150 to P126/INTP152 | | |
| P127/INTP153/ADTRG | | |
| PA0/A0 to PA7/A7 | 5 | |
| PB0/A8 to PB7/A15 | | |
| PX5/$\overline{REFRQ}$ | | |
| PX6/$\overline{WAIT}$ | | |
| PX7/CLKOUT | | |
| CKSEL | 1 | – |
| $\overline{RESET}$ | 2 | |
| MODE0 to MODE2 | | |
| MODE3/$V_{PP}$ | | Connect to $V_{SS}$ via a resistor ($R_{VPP}$). |
| $AV_{REF}$, $AV_{SS}$ | – | Connect directly to $V_{SS}$. |
| $AV_{DD}$ | – | Connect directly to $HV_{DD}$. |

**Figure 2-1. Pin Input/Output Circuits**




**Caution Replace $V_{DD}$ in the circuit diagrams with $HV_{DD}$.**

## 3. FLASH MEMORY PROGRAMMING

The following two flash memory programming methods are available.

**(1) On-board programming**

The program is written to the flash memory using a dedicated flash programmer after the μPD70F3102A-33 is mounted on the target board. Install the connectors, etc., required for communication with the dedicated flash programmer, on the target board.

**(2) Off-board programming**

The program is written to the flash memory using a dedicated adapter before the μPD70F3102A-33 is mounted on the target board.

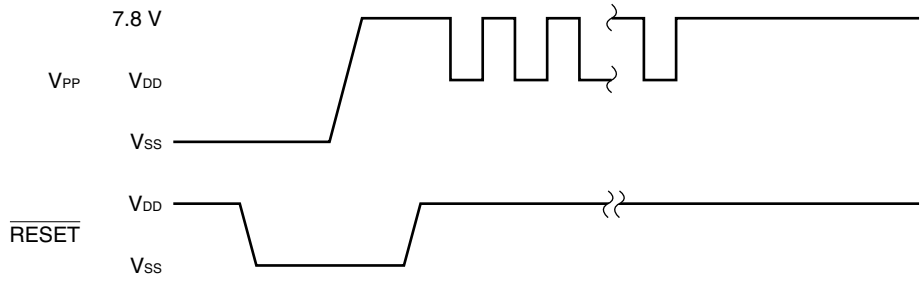
### 3.1 Selection of Communication Mode

Writing to the flash memory is done via serial communication using the dedicated flash programmer. Select one of the communication modes listed in Table 3-1. Base your selection of the communication mode on the selection format shown in Table 3-1. Refer to the number of $V_{PP}$ pulses shown in Table 3-1 when selecting the communication mode.

**Table 3-1. Communication Modes**

| Communication Mode | Pins Used | Number of $V_{PP}$ Pulses |
|---|---|---|
| CSI0 | SO0 (serial data output)<br>SI0 (serial data input)<br>$\overline{SCK0}$ (serial clock input) | 0 |
| UART0 | TXD0 (serial data output)<br>RXD0 (serial data input) | 8 |

**Figure 3-1. Communication Mode Selection Format**



### 3.2 Flash Memory Programming Functions

Flash memory programming is performed by sending and receiving commands and data according to the selected communication mode. Table 3-2 shows the main flash memory programming functions.

**Table 3-2. Main Flash Memory Programming Functions**

| Function | Description |
|---|---|
| Batch erase | Erases the contents of the entire memory. |
| Batch blank check | Checks whether the entire memory has been erased. |
| Data write | Writes data to flash memory based on the write start address and the number of bytes to be written. |
| Batch verify | Compares the contents of the entire memory with the input data. |

### 3.3 Connecting Dedicated Flash Programmer

The connection of the dedicated flash programmer to the μPD70F3102A-33 differs depending on the communication mode. Figures 3-2 and 3-3 show the various connection types.

**Figure 3-2. Connection of Dedicated Flash Programmer for CSI0 Mode**

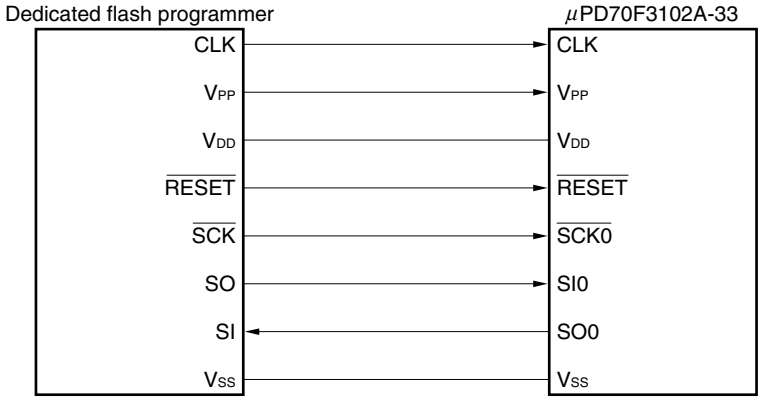
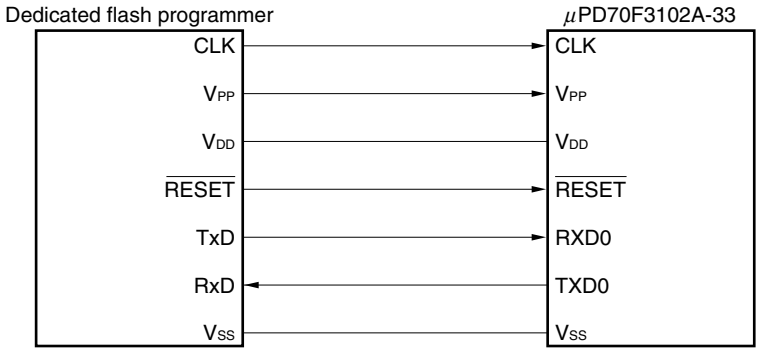



**Figure 3-3. Connection of Dedicated Flash Programmer for UART0 Mode**



# 4. ELECTRICAL SPECIFICATIONS

## 4.1 Normal Operation Mode

**Absolute Maximum Ratings ($T_A$ = 25°C)**

| Parameter | Symbol | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | $V_{DD}$ pin | | –0.5 to +4.6 | V |
| | $HV_{DD}$ | $HV_{DD}$ pin, $HV_{DD} \geq V_{DD}$ | | –0.5 to +4.6 | V |
| | $CV_{DD}$ | $CV_{DD}$ pin | | –0.5 to +4.6 | V |
| | $CV_{SS}$ | $CV_{SS}$ pin | | –0.5 to +0.5 | V |
| | $AV_{DD}$ | $AV_{DD}$ pin | | –0.5 to $HV_{DD}$ + 0.5[Note] | V |
| | $AV_{SS}$ | $AV_{SS}$ pin | | –0.5 to +0.5 | V |
| Input voltage | $V_I$ | Except X1 pin, MODE3/$V_{PP}$ pin | | –0.5 to $HV_{DD}$ + 0.5[Note] | V |
| | | MODE3/$V_{PP}$ pin | | –0.5 to 8.5 | V |
| Clock input voltage | $V_K$ | X1, $V_{DD}$ = 3.0 to 3.6 V | | –0.5 to $V_{DD}$ + 1.0[Note] | V |
| Output current, low | $I_{OL}$ | 1 pin | | 4.0 | mA |
| | | Total of all pins | | 100 | mA |
| Output current, high | $I_{OH}$ | 1 pin | | –4.0 | mA |
| | | Total of all pins | | –100 | mA |
| Output voltage | $V_O$ | $HV_{DD}$ = 3.0 to 3.6 V | | –0.5 to $HV_{DD}$ + 0.5[Note] | V |
| Analog input voltage | $V_{IAN}$ | P70/ANI0 to P77/ANI7 pins | $AV_{DD} > HV_{DD}$ | –0.5 to $HV_{DD}$ + 0.5[Note] | V |
| | | | $HV_{DD} \geq AV_{DD}$ | –0.5 to $AV_{DD}$ + 0.5[Note] | V |
| A/D converter reference input voltage | $AV_{REF}$ | $AV_{DD} > HV_{DD}$ | | –0.5 to $HV_{DD}$ + 0.5[Note] | V |
| | | $HV_{DD} \geq AV_{DD}$ | | –0.5 to $AV_{DD}$ + 0.5[Note] | V |
| Operating ambient temperature | $T_A$ | | | –40 to +85 | °C |
| Storage temperature | $T_{stg}$ | | | –65 to +125 | °C |

**Note** The product must be used under conditions that ensure the absolute maximum ratings (max. values) of each supply voltage are not exceeded.

**Cautions 1. Do not directly connect output pins (or I/O pins) of IC products to each other, and do not connect them directly to $V_{DD}$, $V_{CC}$, or GND. However, open-drain pins and open-collector pins can be directly connected to each other. Moreover, external circuits that implement a timing that avoids conflict with the output of pins that go into high-impedance can be directly connected.**

**2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.**

**Capacitance ($T_A$ = 25°C, $V_{DD}$ = $HV_{DD}$ = $CV_{DD}$ = $AV_{DD}$ = $V_{SS}$ = $CV_{SS}$ = $AV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Input capacitance | $C_I$ | $f_C$ = 1 MHz<br>Unmeasured pins returned to 0 V | | | 15 | pF |
| I/O capacitance | $C_{IO}$ | | | | 15 | pF |
| Output capacitance | $C_O$ | | | | 15 | pF |

**Operating Conditions**

| Operation Mode | Internal Operation Clock Frequency ($f_X$) | Operating Ambient Temperature ($T_A$) | Supply Voltage ($V_{DD}$, $HV_{DD}$) |
|---|---|---|---|
| Direct mode | 2 to 33 MHz | –40 to +85°C | 3.0 to 3.6 V |
| PLL mode[Note 1] | 20 to 33 MHz[Note 2] | –40 to +85°C | 3.0 to 3.6 V |

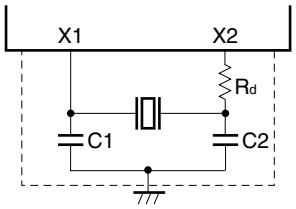
**Notes 1.** The internal operation clock frequency in PLL mode is the value during ×5 operation. Operation at 20 MHz or lower is possible when using ×1 or ×1/2 operation by setting the CKDIVn (n = 0, 1) bit of the CKC register.

**2.** Set the input clock frequency used in PLL mode to 4.0 to 6.6 MHz.

**Recommended Oscillator**

**(a) Connection of ceramic resonator ($T_A$ = –40 to +85°C)**

**(i) Murata Mfg. Co., Ltd. ($T_A$ = –40 to +85°C)**



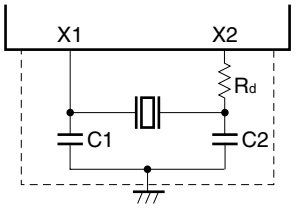

| Type | Product Name | Oscillation Frequency $f_{XX}$ (MHz) | Recommended Circuit Constant | | | Oscillation Voltage Range | | Oscillation Stabilization Time (MAX.) $T_{OST}$ (ms) |
|---|---|---|---|---|---|---|---|---|
| | | | C1 (pF) | C2 (pF) | $R_d$ (kΩ) | MIN. (V) | MAX. (V) | |
| Surface mount | CSAC4.00MGC040 | 4.0 | 100 | 100 | 0 | 3.0 | 3.6 | 0.5 |
| | CSTCC4.00MG0H6 | 4.0 | On-chip | On-chip | 0 | 3.0 | 3.6 | 0.3 |
| | CSAC5.00MGC040 | 5.0 | 100 | 100 | 0 | 3.0 | 3.6 | 0.4 |
| | CSTCC5.00MG0H6 | 5.0 | On-chip | On-chip | 0 | 3.0 | 3.6 | 0.2 |
| | CSAC6.60MT | 6.6 | 30 | 30 | 0 | 3.0 | 3.6 | 0.2 |
| | CSTCC6.60MG0H6 | 6.6 | On-chip | On-chip | 0 | 3.0 | 3.6 | 0.1 |
| Lead | CSA4.00MG040 | 4.0 | 100 | 100 | 0 | 3.0 | 3.6 | 0.5 |
| | CSTC4.00MGW040 | 4.0 | On-chip | On-chip | 0 | 3.0 | 3.6 | 0.5 |
| | CSA5.00MG040 | 5.0 | 100 | 100 | 0 | 3.0 | 3.6 | 0.5 |
| | CSTC5.00MGW040 | 5.0 | On-chip | On-chip | 0 | 3.0 | 3.6 | 0.5 |
| | CSA6.60MTZ | 6.6 | 30 | 30 | 0 | 3.0 | 3.6 | 0.1 |
| | CSA6.60MTW | 6.6 | On-chip | On-chip | 0 | 3.0 | 3.6 | 0.1 |

**Cautions 1. Connect the oscillator as closely to the X1 and X2 pins as possible.**

**2. Do not wire any other signal lines in the area indicated by the broken lines.**

**3. Thoroughly evaluate the matching between the μPD70F3102A-33 and the resonator.**

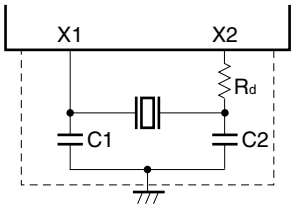
**(ii) TDK Corporation ($T_A$ = –40 to +85°C)**




| Manufacturer | Product Name | Oscillation Frequency $f_{XX}$ (MHz) | Recommended Circuit Constant | | | Oscillation Voltage Range | | Oscillation Stabilization Time (MAX.) $T_{OST}$ (ms) |
|---|---|---|---|---|---|---|---|---|
| | | | C1 (pF) | C2 (pF) | $R_d$ (kΩ) | MIN. (V) | MAX. (V) | |
| TDK | CCR4.0MC3 | 4.0 | On-chip | On-chip | 0 | 3.0 | 3.6 | 0.17 |
| | CCR5.0MC3 | 5.0 | On-chip | On-chip | 0 | 3.0 | 3.6 | 0.15 |

**Cautions 1. Connect the oscillator as closely to the X1 and X2 pins as possible.**
**2. Do not wire any other signal lines in the area indicated by the broken lines.**
**3. Thoroughly evaluate the matching between the μPD70F3102A-33 and the resonator.**

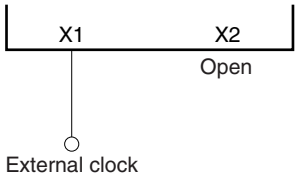
**(iii) Kyocera Corporation ($T_A$ = –20 to +80°C)**




| Manufacturer | Product Name | Oscillation Frequency $f_{XX}$ (MHz) | Recommended Circuit Constant | | | Oscillation Voltage Range | | Oscillation Stabilization Time (MAX.) $T_{OST}$ (ms) |
|---|---|---|---|---|---|---|---|---|
| | | | C1 (pF) | C2 (pF) | $R_d$ (kΩ) | MIN. (V) | MAX. (V) | |
| Kyocera | PBRC5.00BR-A | 5.0 | On-chip | On-chip | 0 | 3.0 | 3.6 | 0.06 |
| | PBRC6.00BR-A | 6.0 | On-chip | On-chip | 0 | 3.0 | 3.6 | 0.06 |
| | PBRC6.60BR-A | 6.6 | On-chip | On-chip | 0 | 3.0 | 3.6 | 0.06 |

**Cautions 1. Connect the oscillator as closely to the X1 and X2 pins as possible.**
**2. Do not wire any other signal lines in the area indicated by the broken lines.**
**3. Thoroughly evaluate the matching between the μPD70F3102A-33 and the resonator.**

**(b) External clock input ($T_A$ = –40 to +85°C)**




**Caution Input a CMOS level voltage to the X1 pin.**

**Cautions when turning on/off the power**

The μPD70F3102A-33 is configured with power supply pins for the internal unit ($V_{DD}$) and for the external pins ($HV_{DD}$).

The operation guaranteed range is $V_{DD}$ = $HV_{DD}$ = 3.0 to 3.6 V. The input and output state of ports may be undefined when the voltage exceeds this range.

**DC Characteristics ($T_A$ = –40 to 85°C, $V_{DD}$ = $HV_{DD}$ = $CV_{DD}$ = $AV_{DD}$ = 3.0 to 3.6 V, $V_{SS}$ = $CV_{SS}$ = $AV_{SS}$ = 0 V)**

| Parameter | | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage, high | | $V_{IH}$ | Except **Note 1** | | 0.65$HV_{DD}$ | | $HV_{DD}$ + 0.3 | V |
| | | | **Note 1** | | 0.8$HV_{DD}$ | | $HV_{DD}$ + 0.3 | V |
| Input voltage, low | | $V_{IL}$ | Except **Notes 1** and **2** | | –0.5 | | 0.2$HV_{DD}$ | V |
| | | | **Note 1** | | –0.5 | | 0.15$HV_{DD}$ | V |
| Clock input voltage, high | | $V_{XH}$ | X1 pin | Direct mode | 0.8$V_{DD}$ | | $V_{DD}$ + 0.3 | V |
| | | | | PLL mode | 0.8$V_{DD}$ | | $V_{DD}$ + 0.3 | V |
| Clock input voltage, low | | $V_{XL}$ | X1 pin | Direct mode | –0.3 | | 0.15$V_{DD}$ | V |
| | | | | PLL mode | –0.3 | | 0.15$V_{DD}$ | V |
| Schmitt trigger input threshold voltage | | $HV_T^+$ | **Note 1**, rising edge | | | 2.0 | | V |
| | | $HV_T^-$ | **Note 1**, falling edge | | | 1.0 | | V |
| Schmitt trigger input hysteresis width | | $HV_T^+ - HV_T^-$ | **Note 1** | | 0.3 | | | V |
| Output voltage, high | | $V_{OH}$ | $I_{OH}$ = –1.0 mA | | 0.8$HV_{DD}$ | | | V |
| Output voltage, low, | | $V_{OL}$ | $I_{OL}$ = 2.5 mA | | | | 0.15$HV_{DD}$ | V |
| Input leakage current, high | | $I_{LIH}$ | $V_I$ = $HV_{DD}$, except **Note 2** | | | | 10 | μA |
| Input leakage current, low | | $I_{LIL}$ | $V_I$ = 0 V, except **Note 2** | | | | –10 | μA |
| Output leakage current, high | | $I_{LOH}$ | $V_O$ = $HV_{DD}$ | | | | 10 | μA |
| Output leakage current, low | | $I_{LOL}$ | $V_O$ = 0 V | | | | –10 | μA |
| Supply current[Note 3] | Normal | $I_{DD1}$ | | | | 2.7 × fx | 4.5 × fx | mA |
| | HALT | $I_{DD2}$ | | | | 1.2 × fx | 3.0 × fx | mA |
| | IDLE | $I_{DD3}$ | | | | 3.0 | 10.0 | mA |
| | STOP | $I_{DD4}$ | –40°C ≤ $T_A$ ≤ +40°C | | | 5.0 | 50 | μA |
| | | | +40°C < $T_A$ ≤ +85°C | | | | 600 | μA |

**Notes 1.** P04/INTP100/$\overline{\text{DMARQ0}}$ to P07/INTP103/$\overline{\text{DMARQ3}}$, P14/INTP110/$\overline{\text{DMAAK0}}$ to P17/INTP113/$\overline{\text{DMAAK3}}$, P34/INTP130, P35/INTP131/SO2, P36/INTP132/SI2, P37/INTP133/$\overline{\text{SCK2}}$, P104/INTP120/$\overline{\text{TC0}}$ to P107/INTP123/$\overline{\text{TC3}}$, P114/INTP140, P115/INTP141/SO3, P116/INTP142/SI3, P117/INTP143/$\overline{\text{SCK3}}$, P124/INTP150 to P126/INTP152, P127/INTP153/ADTRG, P02/TCLR10, P12/TCLR11, P32/TCLR13, P102/TCLR12, P112/TCLR14, P122/TCLR15, P03/TI10, P13/TI11, P33/TI13, P103/TI12, P113/TI14, P123/TI15, P20/NMI, P23/RXD0/SI0, P24/$\overline{\text{SCK0}}$, P26/RXD1/SI1, P27/$\overline{\text{SCK1}}$, MODE0 to MODE2, $\overline{\text{RESET}}$

**2.** When using the P70/AN10 to P77/AN17 pins as analog inputs.

**3.** $V_{DD}$ + $HV_{DD}$ + $CV_{DD}$

**Remarks 1.** TYP. values are reference values for when $T_A$ = 25°C, $V_{DD}$ = $HV_{DD}$ = $CV_{DD}$ = 3.3 V.

**2.** Direct mode: fx (CPU operation frequency) = 2 to 33 MHz
PLL mode: fx (CPU operation frequency) = 20 to 33 MHz

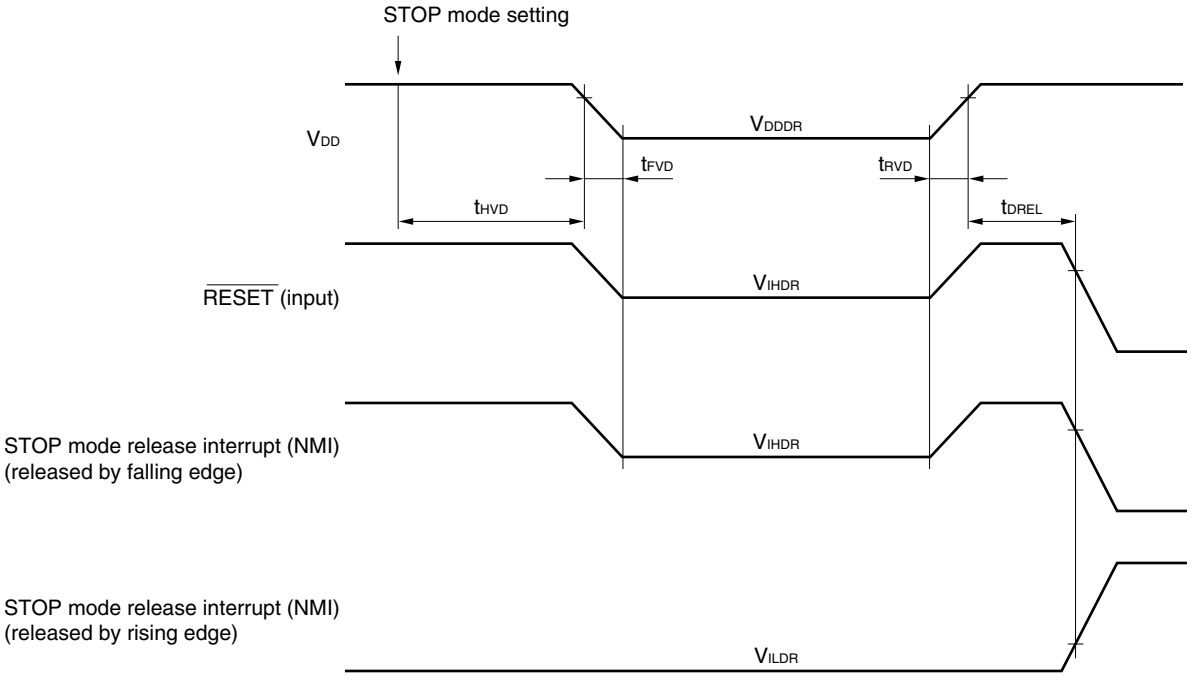
**3.** The fx unit is MHz.

**Data Retention Characteristics ($T_A$ = –40 to +85°C)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Data retention voltage | $V_{DDDR}$ | STOP mode, $V_{DD} = V_{DDDR}$ | | 1.5 | | 3.6 | V |
| Data retention current | $I_{DDDR}$ | $V_{DD} = V_{DDDR}$ | –40°C ≤ $T_A$ ≤ +40°C | | 5.0 | 50 | μA |
| | | | +40°C < $T_A$ ≤ +85°C | | | 600 | μA |
| Supply voltage rise time | $t_{RVD}$ | | | 200 | | | μs |
| Supply voltage fall time | $t_{FVD}$ | | | 200 | | | μs |
| Supply voltage hold time (from STOP mode setting) | $t_{HVD}$ | | | 0 | | | ms |
| STOP release signal input time | $t_{DREL}$ | | | 0 | | | ns |
| Data retention high-level input voltage | $V_{IHDR}$ | **Note** | | 0.8$V_{DDDR}$ | | $V_{DDDR}$ | V |
| Data retention low-level input voltage | $T_{ILDR}$ | **Note** | | 0 | | 0.2$V_{DDDR}$ | V |

**Note** P04/INTP100/$\overline{\text{DMARQ0}}$ to P07/INTP103/$\overline{\text{DMARQ3}}$, P14/INTP110/$\overline{\text{DMAAK0}}$ to P17/INTP113/$\overline{\text{DMAAK3}}$, P34/INTP130, P35/INTP131/SO2, P36/INTP132/SI2, P37/INTP133/$\overline{\text{SCK2}}$, P104/INTP120/$\overline{\text{TC0}}$ to P107/INTP123/$\overline{\text{TC3}}$, P114/INTP140, P115/INTP141/SO3, P116/INTP142/SI3, P117/INTP143/$\overline{\text{SCK3}}$, P124/INTP150 to P126/INTP152, P127/INTP153/ADTRG, P02/TCLR10, P12/TCLR11, P32/TCLR13, P102/TCLR12, P112/TCLR14, P122/TCLR15, P03/TI10, P13/TI11, P33/TI13, P103/TI12, P113/TI14, P123/TI15, P20/NMI, P23/RXD0/SI0, P24/$\overline{\text{SCK0}}$, P26/RXD1/SI1, P27/$\overline{\text{SCK1}}$, MODE0 to MODE2, $\overline{\text{RESET}}$

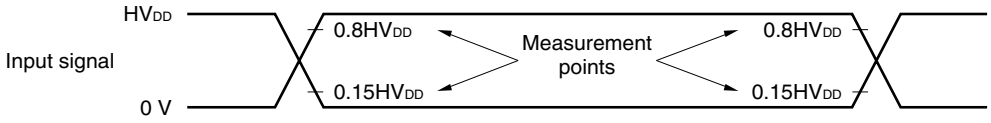
**Remark** TYP. values are reference values for when $T_A$ = 25°C.



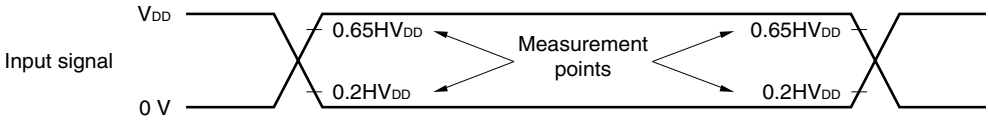
**AC Characteristics ($T_A$ = –40 to +85°C, $V_{DD}$ = $HV_{DD}$ = $CV_{DD}$ = $AV_{DD}$ = 3.0 to 3.6 V, $V_{SS}$ = $CV_{SS}$ = $AV_{SS}$ = 0 V, Output Pin Load Capacitance: $C_L$ = 50 pF)**

**AC Test Input Measurement Points**

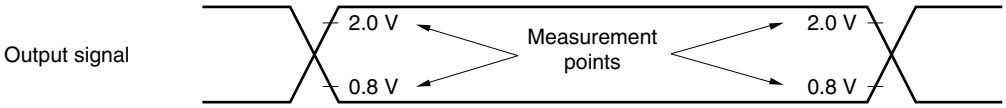
(a) P04/INTP100/$\overline{\text{DMARQ0}}$ to P07/INTP103/$\overline{\text{DMARQ3}}$, P14/INTP110/$\overline{\text{DMAAK0}}$ to P17/INTP113/$\overline{\text{DMAAK3}}$, P34/INTP130, P35/INTP131/SO2, P36/INTP132/SI2, P37/INTP133/$\overline{\text{SCK2}}$, P104/INTP120/$\overline{\text{TC0}}$ to P107/INTP123/$\overline{\text{TC3}}$, P114/INTP140, P115/INTP141/SO3, P116/INTP142/SI3, P117/INTP143/$\overline{\text{SCK3}}$, P124/INTP150 to P126/INTP152, P127/INTP153/ADTRG, P02/TCLR10, P12/TCLR11, P32/TCLR13, P102/TCLR12, P112/TCLR14, P122/TCLR15, P03/TI10, P13/TI11, P33/TI13, P103/TI12, P113/TI14, P123/TI15, P20/NMI, P23/RXD0/SI0, P24/$\overline{\text{SCK0}}$, P26/RXD1/SI1, P27/$\overline{\text{SCK1}}$, MODE0 to MODE2, $\overline{\text{RESET}}$



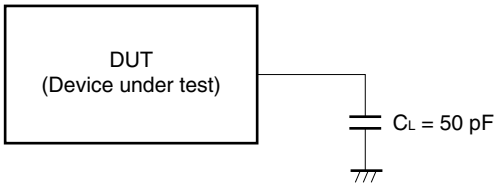

(b) Other than (a)




**AC Test Output Measurement Points**




**Load Conditions**

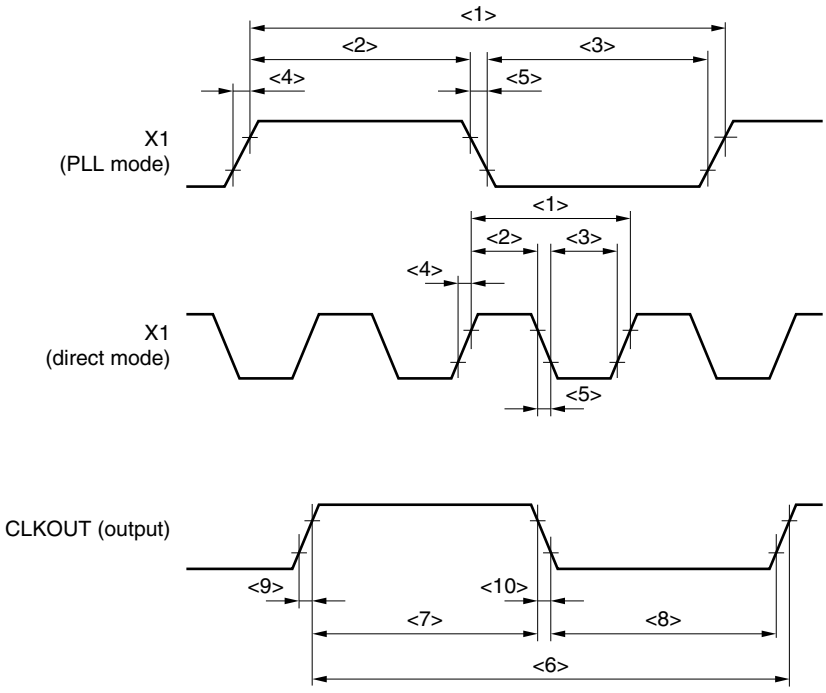



**Caution If the load capacitance exceeds 50 pF due to the circuit configuration, reduce the load capacitance of the device to 50 pF or less by inserting a buffer or by some other means.**

### (1) Clock timing

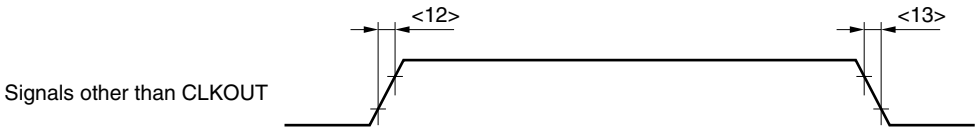
| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| X1 input cycle | <1> | $t_{CYX}$ | In direct mode | 15 | 250 | ns |
| | | | In PLL mode | 150 | 250 | ns |
| X1 input high-level width | <2> | $t_{WXH}$ | In direct mode | 5 | | ns |
| | | | In PLL mode | 50 | | ns |
| X1 input low-level width | <3> | $t_{WXL}$ | In direct mode | 5 | | ns |
| | | | In PLL mode | 50 | | ns |
| X1 input rise time | <4> | $t_{XR}$ | In direct mode | | 4 | ns |
| | | | In PLL mode | | 10 | ns |
| X1 input fall time | <5> | $t_{XF}$ | In direct mode | | 4 | ns |
| | | | In PLL mode | | 10 | ns |
| CLKOUT output cycle | <6> | $t_{CYK}$ | | 30 | 100 | ns |
| CLKOUT high-level width | <7> | $t_{WKH}$ | | 0.5T – 7 | | ns |
| CLKOUT low-level width | <8> | $t_{WKL}$ | | 0.5T – 4 | | ns |
| CLKOUT rise time | <9> | $t_{KR}$ | | | 5 | ns |
| CLKOUT fall time | <10> | $t_{KF}$ | | | 5 | ns |

**Remark** T = $t_{CYK}$



**(2) Output waveform (other than CLKOUT)**

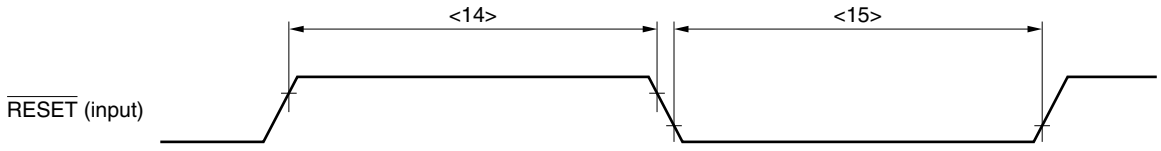
| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Output rise time | <12> | $t_{OR}$ | | | 5 | ns |
| Output fall time | <13> | $t_{OF}$ | | | 5 | ns |



### (3) Reset timing

| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $\overline{\text{RESET}}$ pin high-level width | <14> | $t_{WRSH}$ | | 500 | | ns |
| $\overline{\text{RESET}}$ pin low-level width | <15> | $t_{WRSL}$ | At power ON, STOP mode release | 500 + $T_{OS}$ | | ns |
| | | | Except at power ON, STOP mode release | 500 | | ns |

**Remark** $T_{OS}$: Oscillation stabilization time



### (4) SRAM, external ROM, external I/O access timing

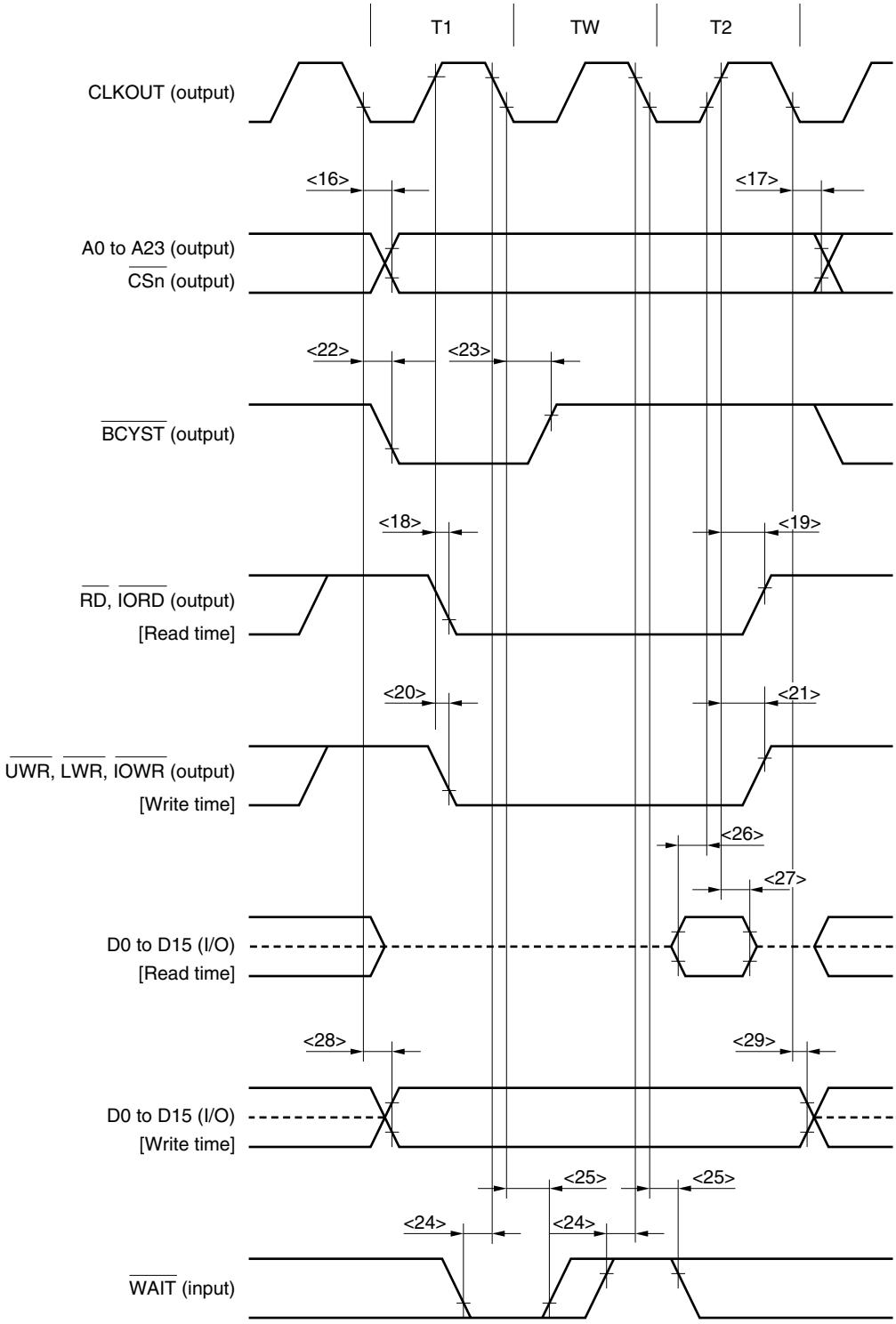
#### (a) Access timing (SRAM, external ROM, external I/O) (1/2)

| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Address, $\overline{CSn}$ output delay time (from CLKOUT↓) | <16> | $t_{DKA}$ | | 2 | 10 | ns |
| Address, $\overline{CSn}$ output hold time (from CLKOUT↓) | <17> | $t_{HKA}$ | | 2 | 10 | ns |
| $\overline{RD}$, $\overline{IORD}$↓ delay time (from CLKOUT↑) | <18> | $t_{DKRDL}$ | | 2 | 14 | ns |
| $\overline{RD}$, $\overline{IORD}$↑ delay time (from CLKOUT↑) | <19> | $t_{HKRDH}$ | | 2 | 14 | ns |
| $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$↓ delay time (from CLKOUT↑) | <20> | $t_{DKWRL}$ | | 2 | 10 | ns |
| $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$↑ delay time (from CLKOUT↑) | <21> | $t_{HKWRH}$ | | 2 | 10 | ns |
| $\overline{BCYST}$↓ delay time (from CLKOUT↓) | <22> | $t_{DKBSL}$ | | 2 | 10 | ns |
| $\overline{BCYST}$↑ delay time (from CLKOUT↓) | <23> | $t_{HKBSH}$ | | 2 | 10 | ns |
| $\overline{WAIT}$ setup time (to CLKOUT↓) | <24> | $t_{SWK}$ | | 10 | | ns |
| $\overline{WAIT}$ hold time (from CLKOUT↓) | <25> | $t_{HKW}$ | | 2 | | ns |
| Data input setup time (to CLKOUT↑) | <26> | $t_{SKID}$ | | 10 | | ns |
| Data input hold time (from CLKOUT↑) | <27> | $t_{HKID}$ | | 2 | | ns |
| Data output delay time (from CLKOUT↓) | <28> | $t_{DKOD}$ | | 2 | 10 | ns |
| Data output hold time (from CLKOUT↓) | <29> | $t_{HKOD}$ | | 2 | 10 | ns |

**Remarks 1.** Observe at least one of the data input hold times, $t_{HKID}$ or $t_{HRDID}$.

**2.** n = 0 to 7

**(a) Access timing (SRAM, external ROM, external I/O) (2/2)**




**Remarks 1.** Timing when number of waits specified by registers DWC1 and DWC2 is 0.

**2.** Broken lines indicate high impedance.

**3.** n = 0 to 7

**(b) Read timing (SRAM, external ROM, external I/O) (1/2)**

| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data input setup time (to address) | <30> | $t_{SAID}$ | | | $(1.5 + w_D + w)T - 20$ | ns |
| Data input setup time (to $\overline{RD}$) | <31> | $t_{SRDID}$ | | | $(1 + w_D + w)T - 24$ | ns |
| $\overline{RD}$, $\overline{IORD}$ low-level width | <32> | $t_{WRDL}$ | | $(1 + w_D + w)T - 10$ | | ns |
| $\overline{RD}$, $\overline{IORD}$ high-level width | <33> | $t_{WRDH}$ | | $T - 10$ | | ns |
| Delay time from address, CSn to $\overline{RD}$, $\overline{IORD}\downarrow$ | <34> | $t_{DARD}$ | | $0.5T - 5$ | | ns |
| Delay time from $\overline{RD}$, $\overline{IORD}\uparrow$ to address | <35> | $t_{DRDA}$ | | $(0.5 + i)T - 5$ | | ns |
| Data input hold time (from $\overline{RD}$, $\overline{IORD}\uparrow$) | <36> | $t_{HRDID}$ | | 0 | | ns |
| Delay time from $\overline{RD}$, $\overline{IORD}\uparrow$ to data output | <37> | $t_{DRDOD}$ | | $(0.5 + i)T - 10$ | | ns |
| $\overline{WAIT}$ setup time (to address) | <38> | $t_{SAW}$ | **Note** | | $T - 20$ | ns |
| $\overline{WAIT}$ setup time (to $\overline{BCYST}\downarrow$) | <39> | $t_{SBSW}$ | **Note** | | $T - 20$ | ns |
| $\overline{WAIT}$ hold time (from $\overline{BCYST}\uparrow$) | <40> | $t_{HBSW}$ | **Note** | 0 | | ns |

**Note** During the first $\overline{WAIT}$ sampling, when the number of waits specified by registers DWC1 and DWC2 is 0.

**Remarks 1.** $T = t_{CYK}$

**2.** w: Number of waits due to $\overline{WAIT}$

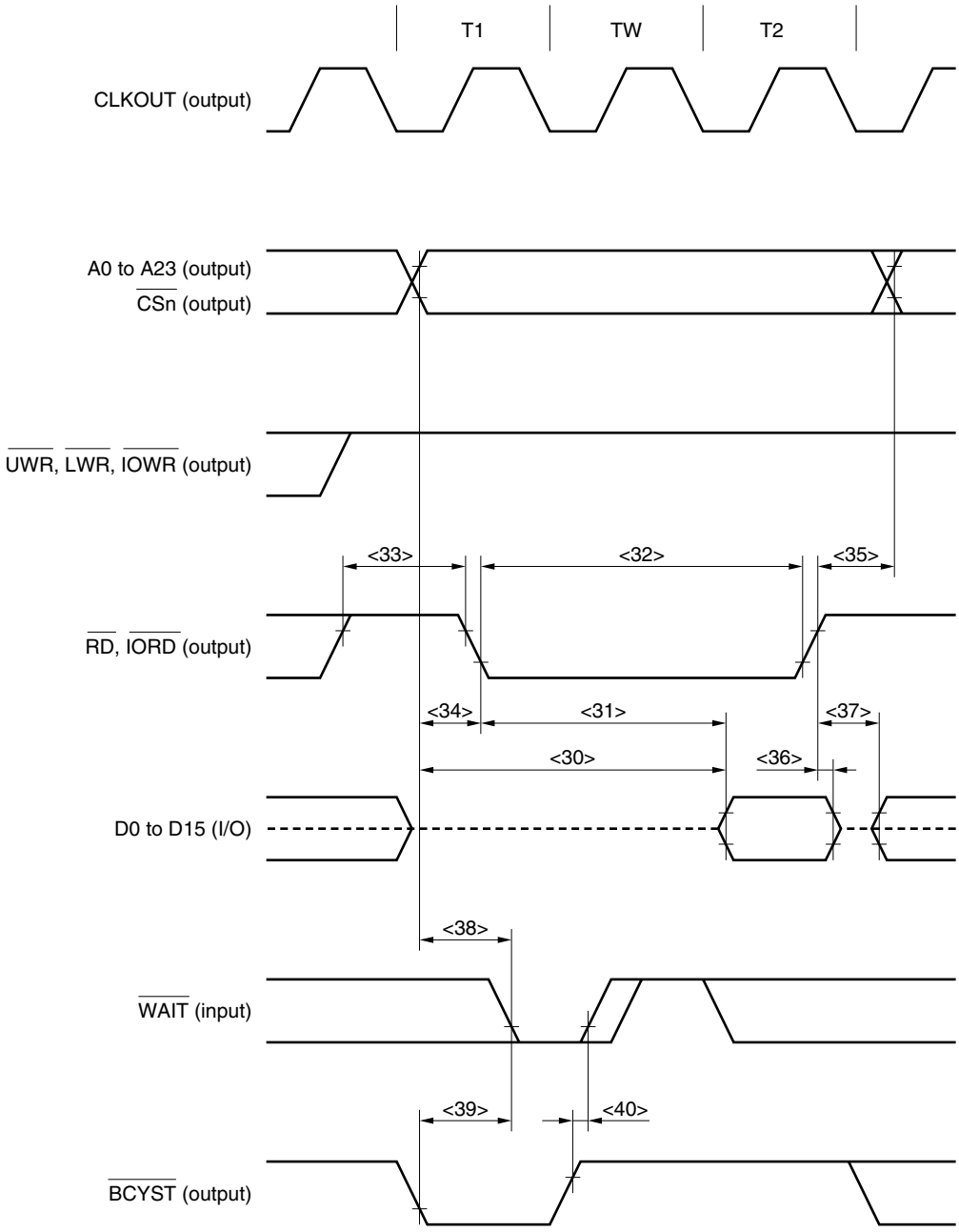
**3.** $w_D$: Number of waits specified by registers DWC1, DWC2

**4.** i: Number of idle states inserted when a write cycle follows the read cycle.

**5.** Observe at least one of the data input hold times, $t_{HKID}$ or $t_{HRDID}$.

**6.** n = 0 to 7

**(b) Read timing (SRAM, external ROM, external I/O) (2/2)**




**Remarks 1.** Timing when the number of waits specified by registers DWC1 and DWC2 is 0.

**2.** Broken lines indicate high impedance.

**3.** n = 0 to 7

**(c) Write timing (SRAM, external ROM, external I/O) (1/2)**

| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $\overline{WAIT}$ setup time (to address) | <38> | $t_{SAW}$ | **Note** | | T – 20 | ns |
| $\overline{WAIT}$ setup time (to $\overline{BCYST}\downarrow$) | <39> | $t_{SBSW}$ | **Note** | | T – 20 | ns |
| $\overline{WAIT}$ hold time (from $\overline{BCYST}\uparrow$) | <40> | $t_{HBSW}$ | **Note** | 0 | | ns |
| Delay time from address, $\overline{CSn}$ to $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}\downarrow$ | <41> | $t_{DAWR}$ | | 0.5T – 5 | | ns |
| Address setup time (to $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}\uparrow$) | <42> | $t_{SAWR}$ | | $(1.5 + w_D + w)T – 10$ | | ns |
| Delay time from $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}\uparrow$ to address | <43> | $t_{DWRA}$ | | 0.5T – 5 | | ns |
| $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ high-level width | <44> | $t_{WWRH}$ | | T – 10 | | ns |
| $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}$ low-level width | <45> | $t_{WWRL}$ | | $(1 + w_D + w)T – 10$ | | ns |
| Data output setup time (to $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}\uparrow$) | <46> | $t_{SODWR}$ | | $(1.5 + w_D + w)T – 10$ | | ns |
| Data output hold time (from $\overline{UWR}$, $\overline{LWR}$, $\overline{IOWR}\uparrow$) | <47> | $t_{HWROD}$ | | 0.5T – 5 | | ns |

**Note** During the first $\overline{WAIT}$ sampling, when the number of waits specified by registers DWC1 and DWC2 is 0.

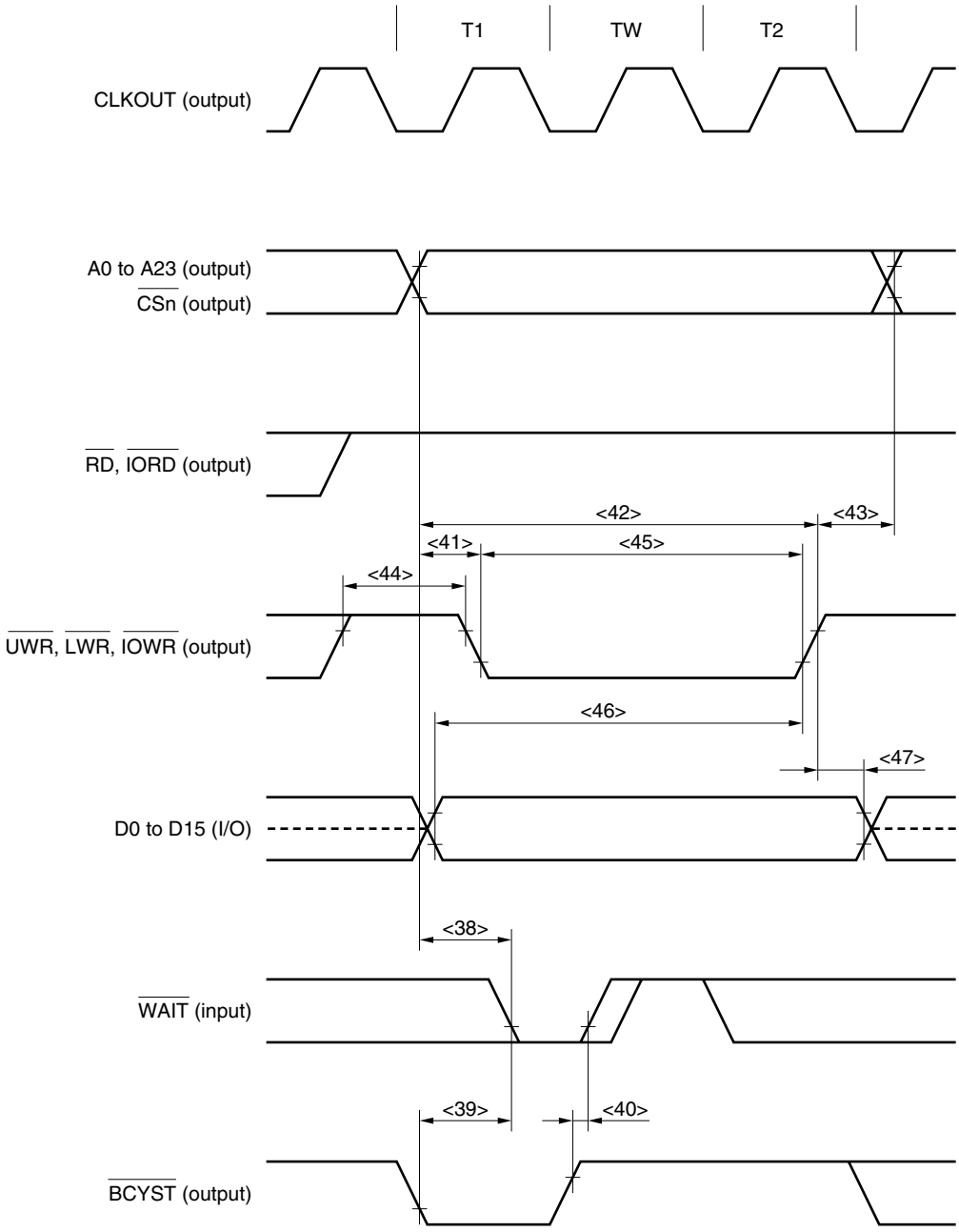
**Remarks 1.** $T = t_{CYK}$

**2.** w: Number of waits due to $\overline{WAIT}$

**3.** $w_D$: Number of waits specified by registers DWC1 and DWC2

**4.** n = 0 to 7

**(c) Write timing (SRAM, external ROM, external I/O) (2/2)**




**Remarks 1.** Timing when the number of waits specified by registers DWC1 and DWC2 is 0.

**2.** Broken lines indicate high impedance.

**3.** n = 0 to 7

**(d) DMA flyby transfer timing (SRAM → external I/O transfer) (1/2)**

| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $\overline{WAIT}$ setup time (to CLKOUT↓) | <24> | $t_{SWK}$ | | 10 | | ns |
| $\overline{WAIT}$ hold time (from CLKOUT↓) | <25> | $t_{HKW}$ | | 2 | | ns |
| $\overline{RD}$ low-level width | <32> | $t_{WRDL}$ | | $(1 + w_D + w_F + w)T - 10$ | | ns |
| $\overline{RD}$ high-level width | <33> | $t_{WRDH}$ | | $T - 10$ | | ns |
| Delay time from address, $\overline{CSn}$ to $\overline{RD}$↓ | <34> | $t_{DARD}$ | | $0.5T - 5$ | | ns |
| Delay time from $\overline{RD}$↑ to address | <35> | $t_{DRDA}$ | | $(0.5 + i)T - 5$ | | ns |
| Delay time from $\overline{RD}$↑ to data output | <37> | $t_{DRDOD}$ | | $(0.5 + i)T - 10$ | | ns |
| $\overline{WAIT}$ setup time (to address) | <38> | $t_{SAW}$ | **Note** | | $T - 20$ | ns |
| $\overline{WAIT}$ setup time (to $\overline{BCYST}$↓) | <39> | $t_{SBSW}$ | **Note** | | $T - 20$ | ns |
| $\overline{WAIT}$ hold time (from $\overline{BCYST}$↑) | <40> | $t_{HBSW}$ | **Note** | 0 | | ns |
| Delay time from address to $\overline{IOWR}$↓ | <41> | $t_{DAWR}$ | | $0.5T - 5$ | | ns |
| Address setup time (to $\overline{IOWR}$↑) | <42> | $t_{SAWR}$ | | $(1.5 + w_D + w)T - 10$ | | ns |
| Delay time from $\overline{IOWR}$↑ to address | <43> | $t_{DWRA}$ | | $0.5T - 5$ | | ns |
| $\overline{IOWR}$ high-level width | <44> | $t_{WWRH}$ | | $T - 10$ | | ns |
| $\overline{IOWR}$ low-level width | <45> | $t_{WWRL}$ | | $(1 + w_D + w)T - 10$ | | ns |
| Delay time from $\overline{IOWR}$↑ to $\overline{RD}$↑ | <48> | $t_{DWRRD}$ | $w_F = 0$ | 0 | | ns |
| | | | $w_F = 1$ | $T - 10$ | | ns |
| Delay time from $\overline{DMAAKm}$↓ to $\overline{IOWR}$↓ | <49> | $t_{DDAWR}$ | | $0.5T - 10$ | | ns |
| Delay time from $\overline{IOWR}$↑ to $\overline{DMAAKm}$↑ | <50> | $t_{DWRDA}$ | | $(0.5 + w_F)T - 10$ | | ns |

**Note** During the first $\overline{WAIT}$ sampling, when the number of waits specified by registers DWC1 and DWC2 is 0.

**Remarks 1.** $T = t_{CYK}$

**2.** w: Number of waits due to $\overline{WAIT}$

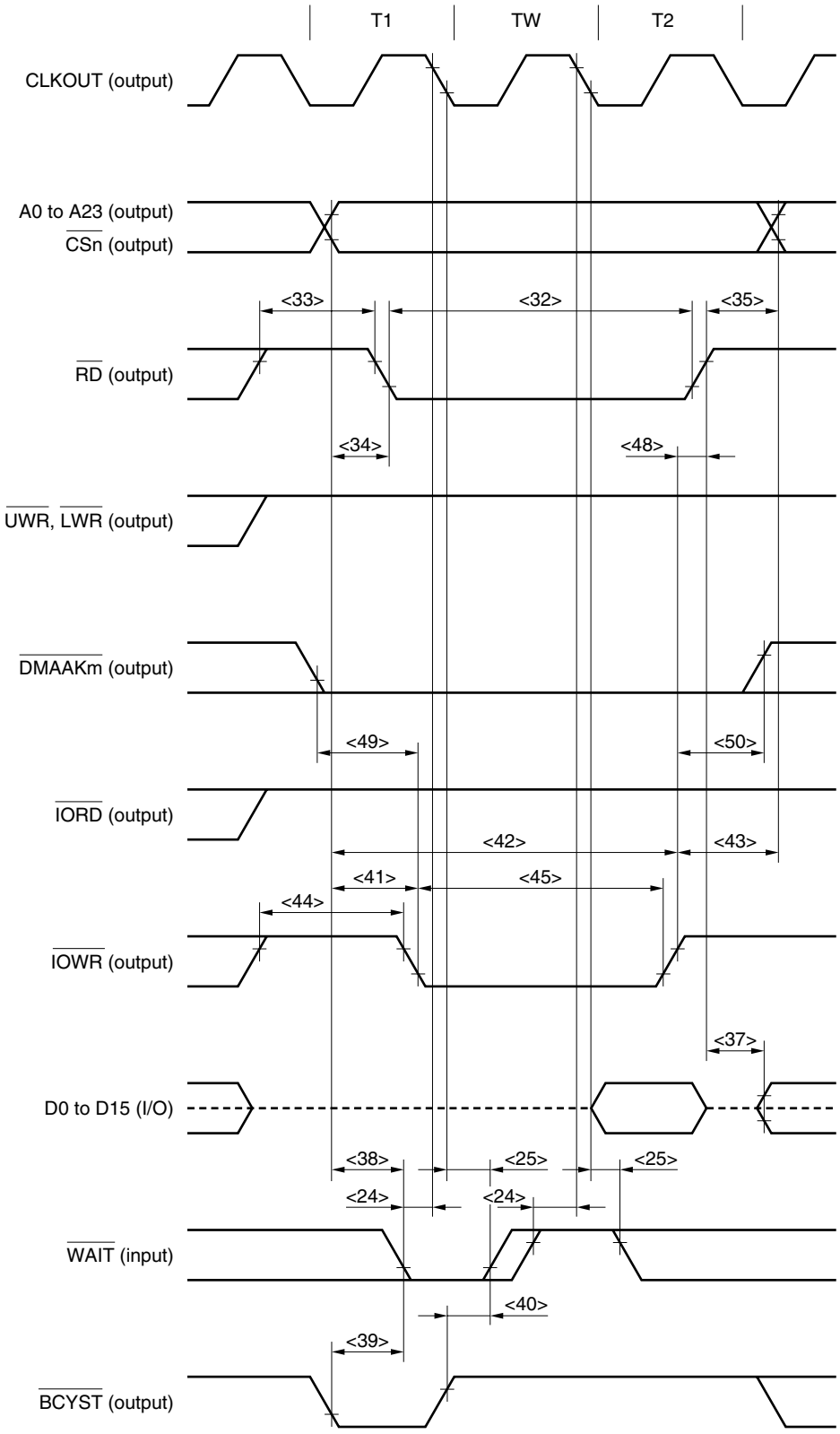
**3.** $w_D$: Number of waits specified by registers DWC1, DWC2

**4.** $w_F$: Number of waits inserted to source-side access during DMA flyby transfer

**5.** i: Number of idle states inserted when a write cycle follows the read cycle

**6.** n = 0 to 7, m = 0 to 3

**(d) DMA flyby transfer timing (SRAM → external I/O transfer) (2/2)**




**Remarks 1.** Timing when the number of waits specified by registers DWC1 and DWC2 is 0 and $w_F = 0$.

**2.** Broken lines indicate high impedance.

**3.** n = 0 to 7, m = 0 to 3

**(e) DMA flyby transfer timing (external I/O → SRAM transfer) (1/2)**

| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $\overline{WAIT}$ setup time (to CLKOUT↓) | <24> | $t_{SWK}$ | | 10 | | ns |
| $\overline{WAIT}$ hold time (from CLKOUT↓) | <25> | $t_{HKW}$ | | 2 | | ns |
| $\overline{IORD}$ low-level width | <32> | $t_{WRDL}$ | | $(1 + w_D + w_F + w)T - 10$ | | ns |
| $\overline{IORD}$ high-level width | <33> | $t_{WRDH}$ | | $T - 10$ | | ns |
| Delay time from address, $\overline{CSn}$ to $\overline{IORD}$↓ | <34> | $t_{DARD}$ | | $0.5T - 5$ | | ns |
| Delay time from $\overline{IORD}$↑ to address | <35> | $t_{DRDA}$ | | $(0.5 + i)T - 5$ | | ns |
| Delay time from $\overline{IORD}$↑ to data output | <37> | $t_{DRDOD}$ | | $(0.5 + i)T - 10$ | | ns |
| $\overline{WAIT}$ setup time (to address) | <38> | $t_{SAW}$ | **Note** | | $T - 20$ | ns |
| $\overline{WAIT}$ setup time (to $\overline{BCYST}$↓) | <39> | $t_{SBSW}$ | **Note** | | $T - 20$ | ns |
| $\overline{WAIT}$ hold time (from $\overline{BCYST}$↑) | <40> | $t_{HBSW}$ | **Note** | 0 | | ns |
| Delay time from address to $\overline{UWR}$, $\overline{LWR}$↓ | <41> | $t_{DAWR}$ | | $0.5T - 5$ | | ns |
| Address setup time (to $\overline{UWR}$, $\overline{LWR}$↑) | <42> | $t_{SAWR}$ | | $(1.5 + w_D + w)T - 10$ | | ns |
| Delay time from $\overline{UWR}$, $\overline{LWR}$↑ to address | <43> | $t_{DWRA}$ | | $0.5T - 5$ | | ns |
| $\overline{UWR}$, $\overline{LWR}$ high-level width | <44> | $t_{WWRH}$ | | $T - 10$ | | ns |
| $\overline{UWR}$, $\overline{LWR}$ low-level width | <45> | $t_{WWRL}$ | | $(1 + w_D + w)T - 10$ | | ns |
| Delay time from $\overline{UWR}$, $\overline{LWR}$↑ to $\overline{IORD}$↑ | <48> | $t_{DWRRD}$ | $w_F = 0$ | 0 | | ns |
| | | | $w_F = 1$ | $T - 10$ | | ns |
| Delay time from $\overline{DMAAKm}$↓ to $\overline{IORD}$↓ | <51> | $t_{DDARD}$ | | $0.5T - 10$ | | ns |
| Delay time from $\overline{IORD}$↑ to $\overline{DMAAKm}$↑ | <52> | $t_{DRDDA}$ | | $0.5T - 10$ | | ns |

**Note** During the first $\overline{WAIT}$ sampling, when the number of waits specified by registers DWC1 and DWC2 is 0.

**Remarks 1.** $T = t_{CYK}$

**2.** w: Number of waits due to $\overline{WAIT}$

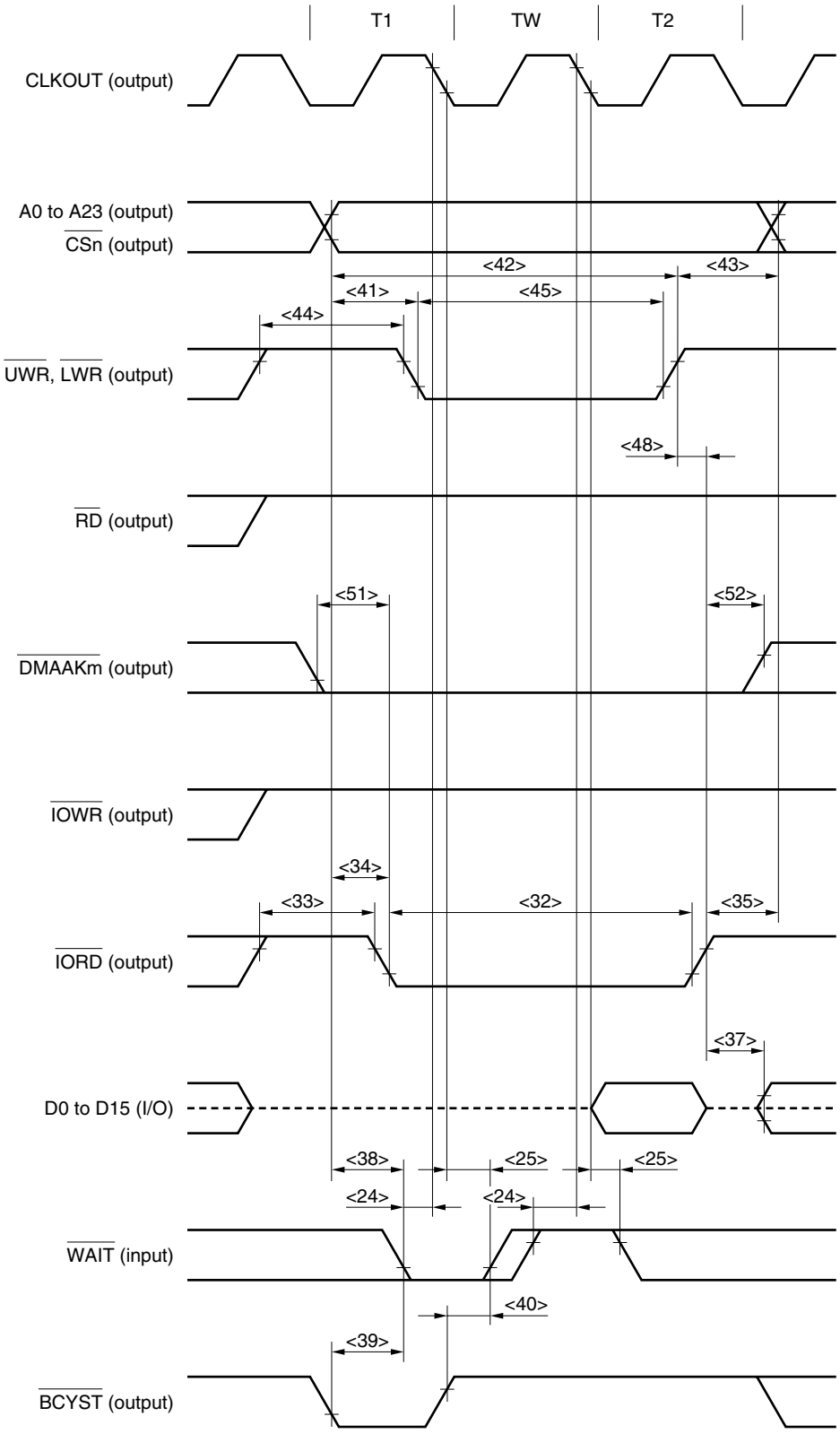
**3.** $w_D$: Number of waits specified by registers DWC1 and DWC2.

**4.** $w_F$: Number of waits inserted to source-side access during DMA flyby transfer.

**5.** i: Number of idle states inserted when a write cycle follows the read cycle.

**6.** n = 0 to 7, m = 0 to 3

**(e) DMA flyby transfer timing (external I/O → SRAM transfer) (2/2)**




**Remarks 1.** Timing when the number of waits specified by registers DWC1 and DWC2 is 0 and $w_F$ = 0.

**2.** Broken lines indicate high impedance.

**3.** n = 0 to 7, m = 0 to 3

### (5) Page ROM access timing (1/2)

| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $\overline{WAIT}$ setup time (to CLKOUT↓) | <24> | $t_{SWK}$ | | 10 | | ns |
| $\overline{WAIT}$ hold time (from CLKOUT↓) | <25> | $t_{HKW}$ | | 2 | | ns |
| Data input setup time (to CLKOUT↑) | <26> | $t_{SKID}$ | | 10 | | ns |
| Data input hold time (from CLKOUT↑) | <27> | $t_{HKID}$ | | 2 | | ns |
| Off-page data input setup time (to address) | <30> | $t_{SAID}$ | | | $(1.5 + w_D + w)T - 20$ | ns |
| Off-page data input setup time (to $\overline{RD}$) | <31> | $t_{SRDID}$ | | | $(1 + w_D + w)T - 24$ | ns |
| Off-page $\overline{RD}$ low-level width | <32> | $t_{WRDL}$ | | $(1 + w_D + w)T - 10$ | | ns |
| $\overline{RD}$ high-level width | <33> | $t_{WRDH}$ | | $0.5T - 10$ | | ns |
| Data input hold time (from $\overline{RD}$) | <36> | $t_{HRDID}$ | | 0 | | ns |
| Delay time from $\overline{RD}$↑ to data output | <37> | $t_{DRDOD}$ | | $(0.5 + i)T - 10$ | | ns |
| On-page $\overline{RD}$ low-level width | <53> | $t_{WORDL}$ | | $(1.5 + w_{PR} + w)T - 10$ | | ns |
| On-page data input setup time (to address) | <54> | $t_{SOAID}$ | | | $(1.5 + w_{PR} + w)T - 20$ | ns |
| On-page data input setup time (to $\overline{RD}$) | <55> | $t_{SORDID}$ | | | $(1.5 + w_{PR} + w)T - 24$ | ns |

**Remarks 1.** $T = t_{CYK}$

**2.** w: Number of waits due to $\overline{WAIT}$

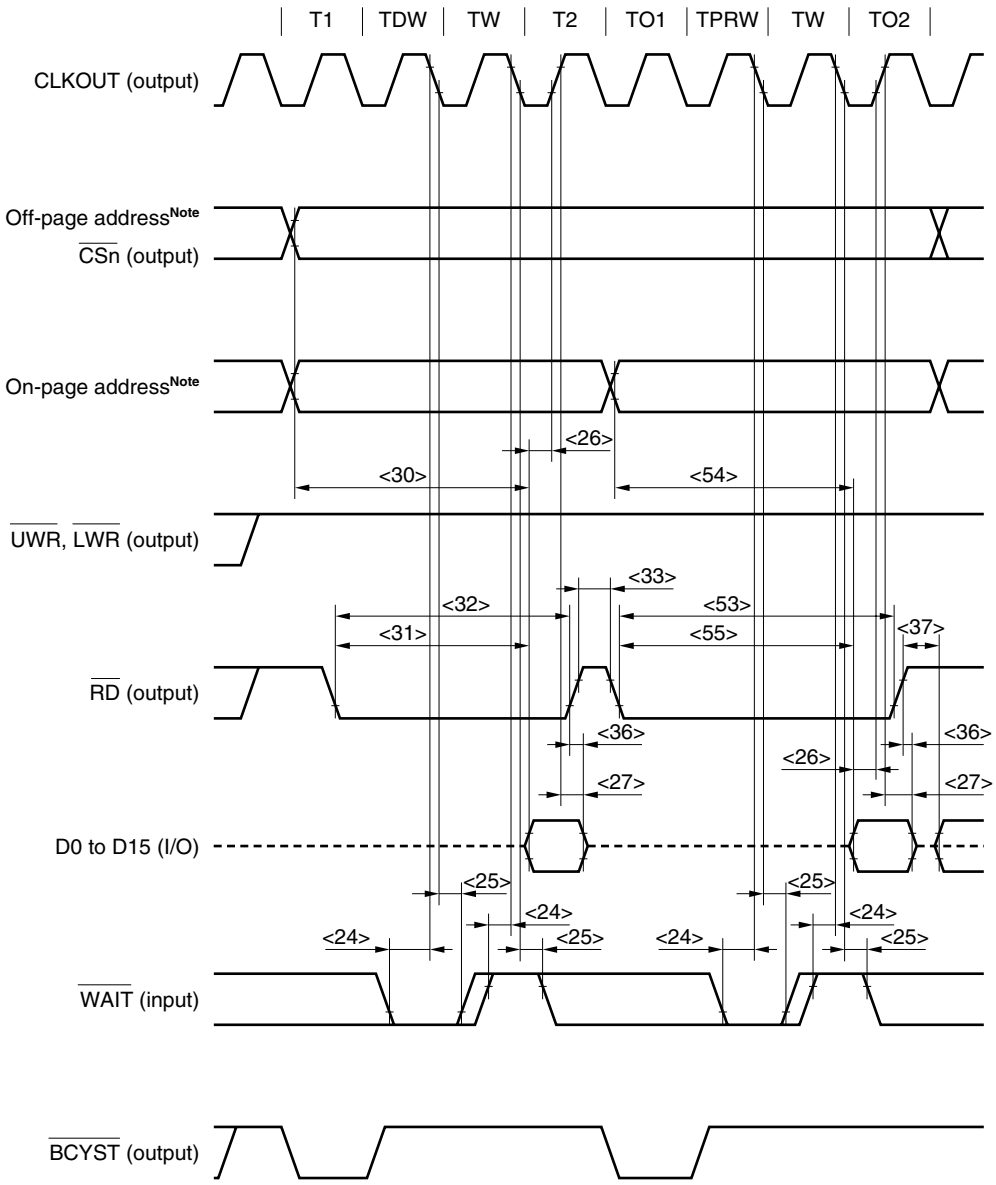
**3.** $w_D$: Number of waits specified by registers DWC1 and DWC2.

**4.** $w_{PR}$: Number of waits specified by register PRC.

**5.** i: Number of idle states inserted when a write cycle follows the read cycle.

**6.** Observe at least one of the data input hold times, $t_{HKID}$ or $t_{HRDID}$.

**(5) Page ROM access timing (2/2)**




**Note** On-page addresses and off-page addresses are as follows.

| PRC Register | | | On-Page Address | Off-Page Address |
|---|---|---|---|---|
| MA5 | MA4 | MA3 | | |
| 0 | 0 | 0 | A0, A1 | A2 to A23 |
| 0 | 0 | 1 | A0 to A2 | A3 to A23 |
| 0 | 1 | 1 | A0 to A3 | A4 to A23 |
| 1 | 1 | 1 | A0 to A4 | A5 to A23 |

**Remarks 1.** These timings are for the following cases:

Number of waits (TDW) specified by registers DWC1 and DWC2: 1

Number of waits (TPRW) specified by register PRC: 1

**2.** Broken lines indicate high impedance.

**3.** n = 0 to 7

### (6) DRAM access timing

#### (a) Read timing (high-speed page DRAM access, normal access: off-page) (1/3)

| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $\overline{WAIT}$ setup time (to CLKOUT↓) | <24> | $t_{SWK}$ | | 10 | | ns |
| $\overline{WAIT}$ hold time (from CLKOUT↓) | <25> | $t_{HKW}$ | | 2 | | ns |
| Data input setup time (to CLKOUT↑) | <26> | $t_{SKID}$ | | 10 | | ns |
| Data input hold time (from CLKOUT↑) | <27> | $t_{HKID}$ | | 2 | | ns |
| Delay time from $\overline{OE}$↑ to data output | <37> | $t_{DRDOD}$ | | (0.5 + i)T – 10 | | ns |
| Row address setup time | <56> | $t_{ASR}$ | | (0.5 + $w_{RP}$)T – 10 | | ns |
| Row address hold time | <57> | $t_{RAH}$ | | (0.5 + $w_{RH}$)T – 10 | | ns |
| Column address setup time | <58> | $t_{ASC}$ | | 0.5T – 10 | | ns |
| Column address hold time | <59> | $t_{CAH}$ | | (1.5 + $w_{DA}$ + w)T – 10 | | ns |
| Read/write cycle time | <60> | $t_{RC}$ | | (3 + $w_{RP}$ + $w_{RH}$ + $w_{DA}$ + w)T – 10 | | ns |
| $\overline{RAS}$ precharge time | <61> | $t_{RP}$ | | (0.5 + $w_{RP}$)T – 5 | | ns |
| $\overline{RAS}$ pulse time | <62> | $t_{RAS}$ | | (2.5 + $w_{RH}$ + $w_{DA}$ + w)T – 10 | | ns |
| $\overline{RAS}$ hold time | <63> | $t_{RSH}$ | | (1.5 + $w_{DA}$ + w)T – 10 | | ns |
| Column address read time for $\overline{RAS}$ | <64> | $t_{RAL}$ | | (2 + $w_{DA}$ + w)T – 10 | | ns |
| $\overline{CAS}$ pulse width | <65> | $t_{CAS}$ | | (1 + $w_{DA}$ + w)T – 10 | | ns |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | <66> | $t_{CRP}$ | | (1 + $w_{RP}$)T – 10 | | ns |
| $\overline{CAS}$ hold time | <67> | $t_{CSH}$ | | (2 + $w_{RH}$ + $w_{DA}$ + w)T – 10 | | ns |
| $\overline{WE}$ setup time | <68> | $t_{RCS}$ | | (2 + $w_{RP}$ + $w_{RH}$)T – 10 | | ns |
| $\overline{WE}$ hold time (from $\overline{RAS}$↑) | <69> | $t_{RRH}$ | | 0.5T – 10 | | ns |
| $\overline{WE}$ hold time (from $\overline{CAS}$↑) | <70> | $t_{RCH}$ | | T – 10 | | ns |
| $\overline{CAS}$ precharge time | <71> | $t_{CPN}$ | | (2 + $w_{RP}$ + $w_{RH}$)T – 5 | | ns |
| Output enable access time | <72> | $t_{OEA}$ | | | (2 + $w_{RP}$ + $w_{RH}$ + $w_{DA}$ + w)T – 20 | ns |
| $\overline{RAS}$ access time | <73> | $t_{RAC}$ | | | (2 + $w_{RH}$ + $w_{DA}$ + w)T – 20 | ns |
| Access time from column address | <74> | $t_{AA}$ | | | (1.5 + $w_{DA}$ + w)T – 20 | ns |
| $\overline{CAS}$ access time | <75> | $t_{CAC}$ | | | (1 + $w_{DA}$ + w)T – 20 | ns |

**Remarks 1.** T = $t_{CYK}$

**2.** w: Number of waits due to $\overline{WAIT}$

**3.** $w_{RP}$: Number of waits specified by RPCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**4.** $w_{RH}$: Number of waits specified by RHCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**5.** $w_{DA}$: Number of waits specified by DACxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**6.** i: Number of idle states inserted when a write cycle follows the read cycle.

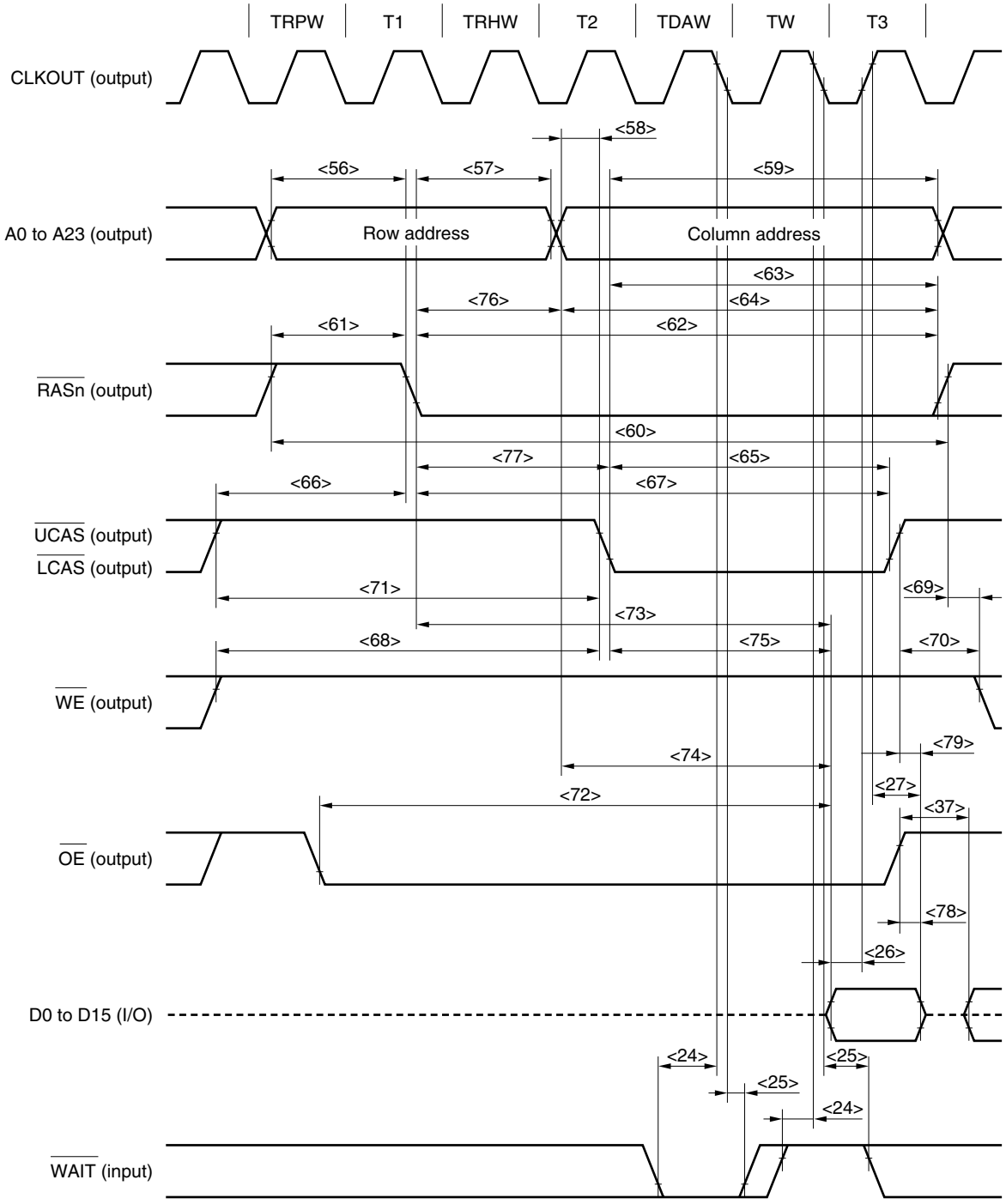
**(a) Read timing (high-speed page DRAM access, normal access: off-page) (2/3)**

| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $\overline{RAS}$ column address delay time | <76> | $t_{RAD}$ | | $(0.5 + w_{RH})T - 10$ | | ns |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | <77> | $t_{RCD}$ | | $(1 + w_{RH})T - 10$ | | ns |
| Output buffer turn off delay time (from $\overline{OE}\uparrow$) | <78> | $t_{OEZ}$ | | 0 | | ns |
| Output buffer turn off delay time (from $\overline{CAS}\uparrow$) | <79> | $t_{OFF}$ | | 0 | | ns |

**Remarks 1.** $T = t_{CYK}$

**2.** $w_{RH}$: Number of waits specified by RHCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**(a) Read timing (high-speed page DRAM access, normal access: off-page) (3/3)**




**Remarks 1.** These timings are for the following cases (n = 0 to 3, xx = 00 to 03, 10 to 13):

Number of waits (TRPW) specified by RPCxx bit of register DRCn: 1

Number of waits (TRHW) specified by RHCxx bit of register DRCn: 1

Number of waits (TDAW) specified by DACxx bit of register DRCn: 1

**2.** Broken lines indicate high impedance.

**3.** n = 0 to 7

**[MEMO]**

**(b) Read timing (high-speed DRAM access: on-page) (1/2)**

| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data input setup time (to CLKOUT↑) | <26> | $t_{SKID}$ | | 10 | | ns |
| Data input hold time (from CLKOUT↑) | <27> | $t_{HKID}$ | | 2 | | ns |
| Delay time from $\overline{OE}$↑ to data output | <37> | $t_{DRDOD}$ | | (0.5 + i)T – 10 | | ns |
| Column address setup time | <58> | $t_{ASC}$ | | (0.5 + $w_{CP}$)T – 10 | | ns |
| Column address hold time | <59> | $t_{CAH}$ | | (1.5 + $w_{DA}$)T – 10 | | ns |
| $\overline{RAS}$ hold time | <63> | $t_{RSH}$ | | (1.5 + $w_{DA}$)T – 10 | | ns |
| Column address read time for $\overline{RAS}$ | <64> | $t_{RAL}$ | | (2 + $w_{CP}$ + $w_{DA}$)T – 10 | | ns |
| $\overline{CAS}$ pulse width | <65> | $t_{CAS}$ | | (1 + $w_{DA}$)T – 10 | | ns |
| $\overline{WE}$ setup time (to $\overline{CAS}$↓) | <68> | $t_{RCS}$ | | (1 + $w_{CP}$)T – 10 | | ns |
| $\overline{WE}$ hold time (from $\overline{RAS}$↑) | <69> | $t_{RRH}$ | | 0.5 T – 10 | | ns |
| $\overline{WE}$ hold time (from $\overline{CAS}$↑) | <70> | $t_{RCH}$ | | T – 10 | | ns |
| Output enable access time | <72> | $t_{OEA}$ | | | (1 + $w_{CP}$ + $w_{DA}$)T – 20 | ns |
| Access time from column address | <74> | $t_{AA}$ | | | (1.5 + $w_{CP}$ + $w_{DA}$)T – 20 | ns |
| $\overline{CAS}$ access time | <75> | $t_{CAC}$ | | | (1 + $w_{DA}$)T – 20 | ns |
| Output buffer turn-off delay time (from $\overline{OE}$↑) | <78> | $t_{OEZ}$ | | 0 | | ns |
| Output buffer turn-off delay time (from $\overline{CAS}$↑) | <79> | $t_{OFF}$ | | 0 | | ns |
| Access time from $\overline{CAS}$ precharge | <80> | $t_{ACP}$ | | | (2 + $w_{CP}$ + $w_{DA}$)T – 20 | ns |
| $\overline{CAS}$ precharge time | <81> | $t_{CP}$ | | (1 + $w_{CP}$)T – 5 | | ns |
| High-speed page mode cycle time | <82> | $t_{PC}$ | | (2 + $w_{CP}$ + $w_{DA}$)T – 10 | | ns |
| $\overline{RAS}$ hold time from $\overline{CAS}$ precharge | <83> | $t_{RHCP}$ | | (2.5 + $w_{CP}$ + $w_{DA}$)T – 10 | | ns |

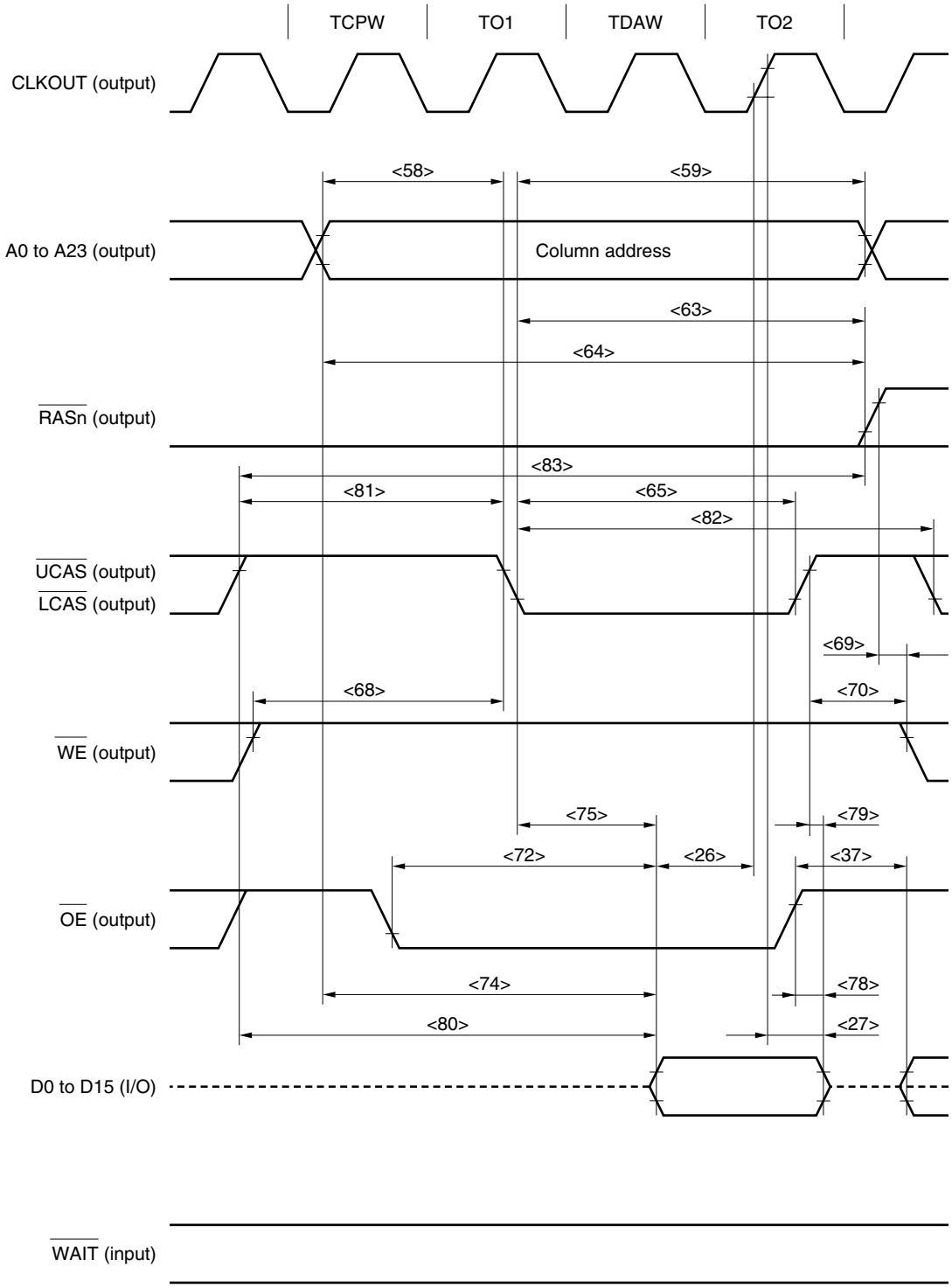
**Remarks 1.** T = $t_{CYK}$

**2.** $w_{CP}$: Number of waits specified by CPCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**3.** $w_{DA}$: Number of waits specified by DACxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**4.** i: Number of idle states inserted when a write cycle follows the read cycle.

**(b) Read timing (high-speed DRAM access: on-page) (2/2)**




**Remarks 1.** These timings are for the following cases (n = 0 to 3, xx = 00 to 03, 10 to 13):

Number of waits (TCPW) specified by CPCxx bit of register DRCn: 1

Number of waits (TDAW) specified by DACxx bit of register DRCn: 1

**2.** Broken lines indicate high impedance.

**3.** n = 0 to 7

**(c) Write timing (high-speed page DRAM access, normal access: off-page) (1/2)**

| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $\overline{WAIT}$ setup time (to CLKOUT↓) | <24> | $t_{SWK}$ | | 10 | | ns |
| $\overline{WAIT}$ hold time (from CLKOUT↓) | <25> | $t_{HKW}$ | | 2 | | ns |
| Row address setup time | <56> | $t_{ASR}$ | | $(0.5 + w_{RP})T - 10$ | | ns |
| Row address hold time | <57> | $t_{RAH}$ | | $(0.5 + w_{RH})T - 10$ | | ns |
| Column address setup time | <58> | $t_{ASC}$ | | $0.5T - 10$ | | ns |
| Column address hold time | <59> | $t_{CAH}$ | | $(1.5 + w_{DA} + w)T - 10$ | | ns |
| Read/write cycle time | <60> | $t_{RC}$ | | $(3 + w_{RP} + w_{RH} + w_{DA} + w)T - 10$ | | ns |
| $\overline{RAS}$ precharge time | <61> | $t_{RP}$ | | $(0.5 + w_{RP})T - 5$ | | ns |
| $\overline{RAS}$ pulse time | <62> | $t_{RAS}$ | | $(2.5 + w_{RH} + w_{DA} + w)T - 10$ | | ns |
| $\overline{RAS}$ hold time | <63> | $t_{RSH}$ | | $(1.5 + w_{DA} + w)T - 10$ | | ns |
| Column address read time (from $\overline{RAS}$↑) | <64> | $t_{RAL}$ | | $(2 + w_{DA} + w)T - 10$ | | ns |
| $\overline{CAS}$ pulse width | <65> | $t_{CAS}$ | | $(1 + w_{DA} + w)T - 10$ | | ns |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | <66> | $t_{CRP}$ | | $(1 + w_{RH})T - 10$ | | ns |
| $\overline{CAS}$ hold time | <67> | $t_{CSH}$ | | $(2 + w_{RH} + w_{DA} + w)T - 10$ | | ns |
| $\overline{CAS}$ precharge time | <71> | $t_{CPN}$ | | $(2 + w_{RP} + w_{RH})T - 5$ | | ns |
| $\overline{RAS}$ column address delay time | <76> | $t_{RAD}$ | | $(0.5 + w_{RH})T - 10$ | | ns |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | <77> | $t_{RCD}$ | | $(1 + w_{RH})T - 10$ | | ns |
| $\overline{WE}$ setup time (to $\overline{CAS}$↓) | <84> | $t_{WCS}$ | | $(1 + w_{RP} + w_{RH})T - 10$ | | ns |
| $\overline{WE}$ hold time (from $\overline{CAS}$↓) | <85> | $t_{WCH}$ | | $(1 + w_{DA} + w)T - 10$ | | ns |
| Data setup time (to $\overline{CAS}$↓) | <86> | $t_{DS}$ | | $(1.5 + w_{RP} + w_{RH})T - 10$ | | ns |
| Data hold time (from $\overline{CAS}$↓) | <87> | $t_{DH}$ | | $(1.5 + w_{DA} + w)T - 10$ | | ns |

**Remarks 1.** $T = t_{CYK}$

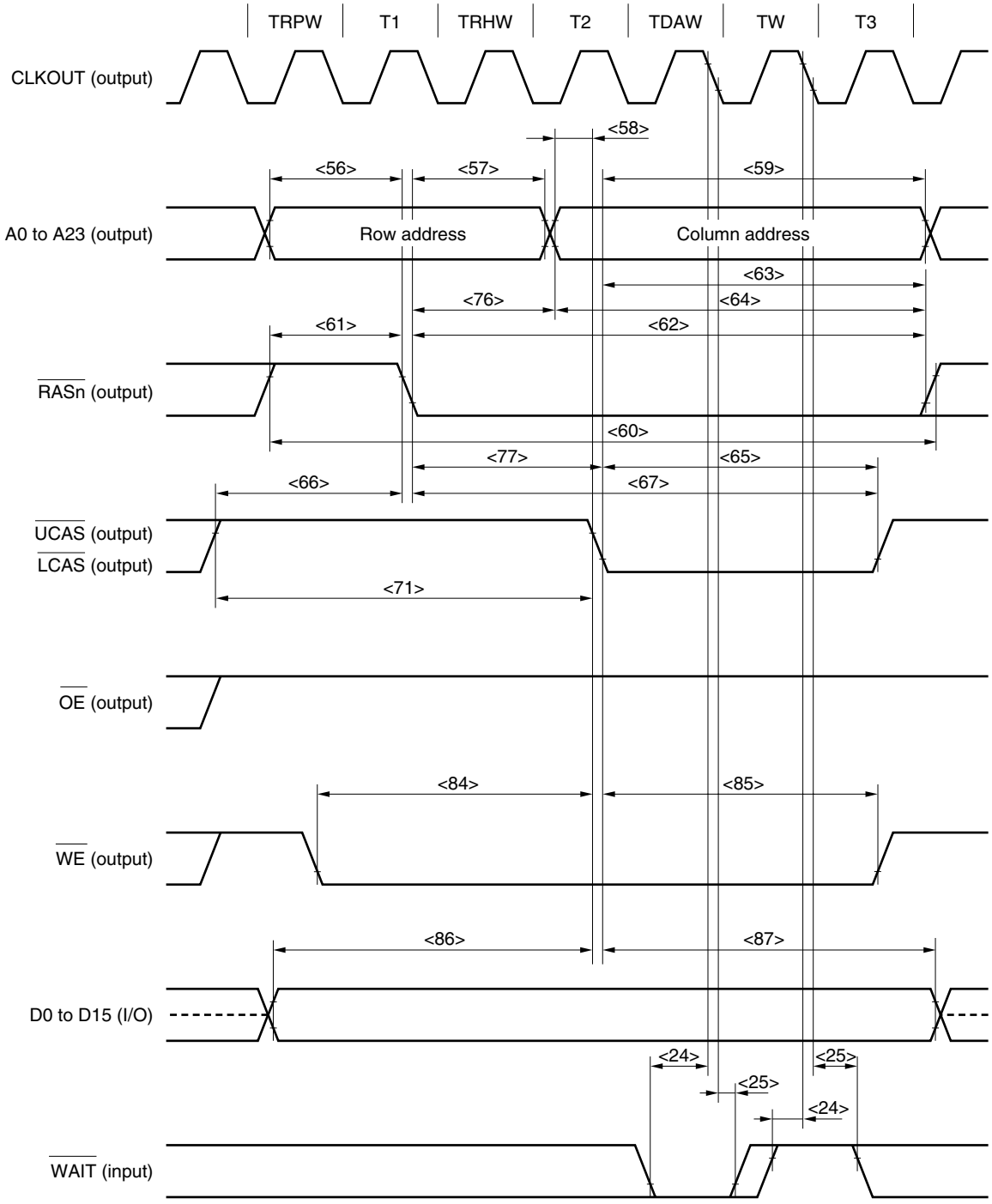
**2.** w: Number of waits due to $\overline{WAIT}$

**3.** $w_{RP}$: Number of waits specified by RPCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**4.** $w_{RH}$: Number of waits specified by RHCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**5.** $w_{DA}$: Number of waits specified by DACxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**(c) Write timing (high-speed page DRAM access, normal access: off-page) (2/2)**




**Remarks 1.** These timings are for the following cases (n = 0 to 3, xx = 00 to 03, 10 to 13):

Number of waits (TRPW) specified by RPCxx bit of register DRCn: 1

Number of waits (TRHW) specified by RHCxx bit of register DRCn: 1

Number of waits (TDAW) specified by DACxx bit of register DRCn: 1

**2.** Broken lines indicate high impedance.

**3.** n = 0 to 7

**(d) Write timing (high-speed page DRAM access: on-page) (1/2)**

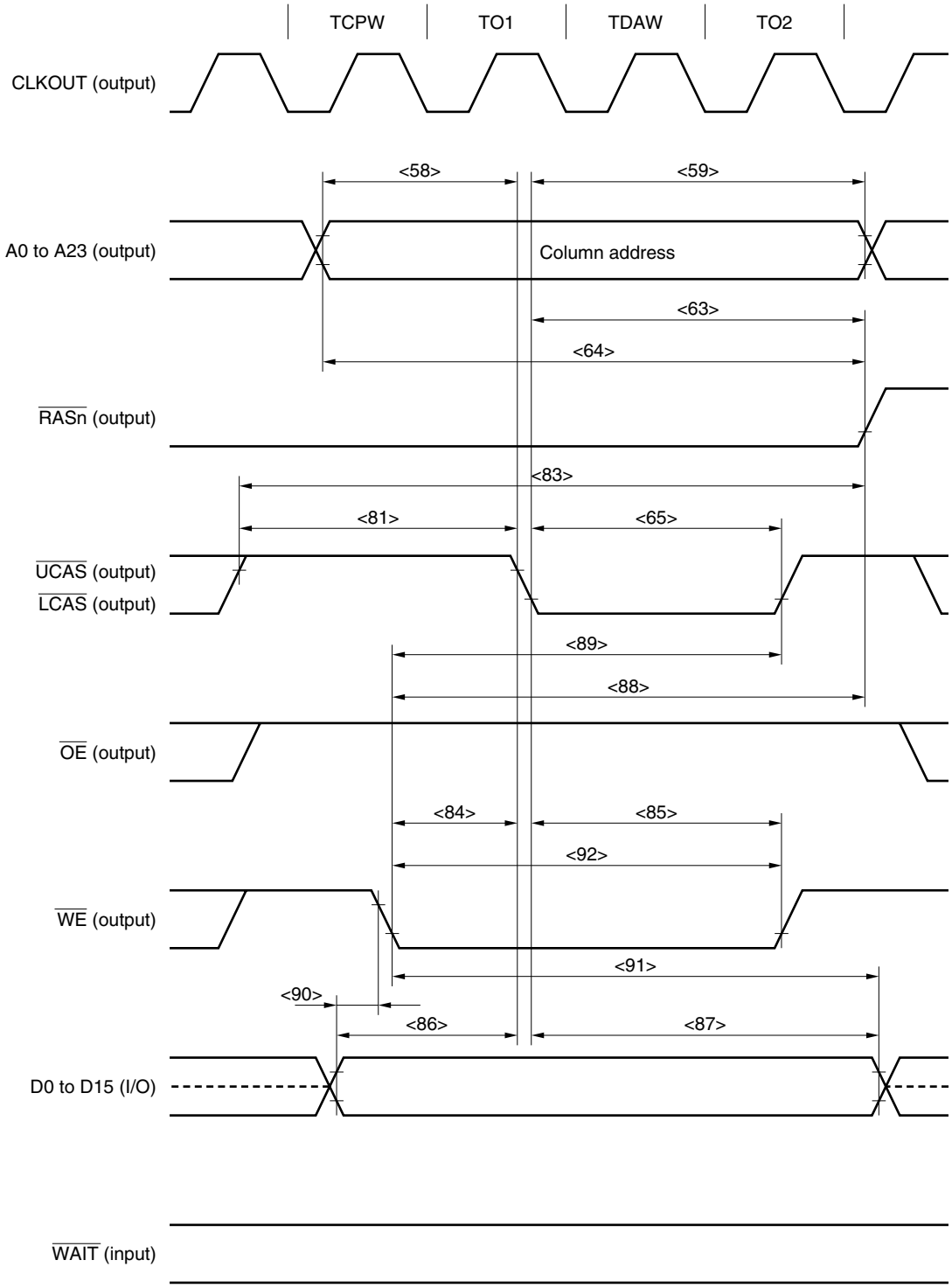
| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Column address setup time | <58> | $t_{ASC}$ | | $(0.5 + w_{CP})T - 10$ | | ns |
| Column address hold time | <59> | $t_{CAH}$ | | $(1.5 + w_{DA})T - 10$ | | ns |
| $\overline{RAS}$ hold time | <63> | $t_{RSH}$ | | $(1.5 + w_{DA})T - 10$ | | ns |
| Column address read time (from $\overline{RAS}\uparrow$) | <64> | $t_{RAL}$ | | $(2 + w_{CP} + w_{DA})T - 10$ | | ns |
| $\overline{CAS}$ pulse width | <65> | $t_{CAS}$ | | $(1 + w_{DA})T - 10$ | | ns |
| $\overline{CAS}$ precharge time | <81> | $t_{CP}$ | | $(1 + w_{CP})T - 5$ | | ns |
| $\overline{RAS}$ hold time for $\overline{CAS}$ precharge | <83> | $t_{RHCP}$ | | $(2.5 + w_{CP} + w_{DA})T - 10$ | | ns |
| $\overline{WE}$ setup time (to $\overline{CAS}\downarrow$) | <84> | $t_{WCS}$ | $w_{CP} \geq 1$ | $w_{CP}T - 10$ | | ns |
| $\overline{WE}$ hold time (from $\overline{CAS}\downarrow$) | <85> | $t_{WCH}$ | | $(1 + w_{DA})T - 10$ | | ns |
| Data setup time (to $\overline{CAS}\downarrow$) | <86> | $t_{DS}$ | | $(0.5 + w_{CP})T - 10$ | | ns |
| Data hold time (from $\overline{CAS}\downarrow$) | <87> | $t_{DH}$ | | $(1.5 + w_{DA})T - 10$ | | ns |
| $\overline{WE}$ read time (from $\overline{RAS}\uparrow$) | <88> | $t_{RWL}$ | $w_{CP} = 0$ | $(1.5 + w_{DA})T - 10$ | | ns |
| $\overline{WE}$ read time (from $\overline{CAS}\uparrow$) | <89> | $t_{CWL}$ | $w_{CP} = 0$ | $(1 + w_{DA})T - 10$ | | ns |
| Data setup time (to $\overline{WE}\downarrow$) | <90> | $t_{DSWE}$ | $w_{CP} = 0$ | $0.5T - 10$ | | ns |
| Data hold time (from $\overline{WE}\downarrow$) | <91> | $t_{DHWE}$ | $w_{CP} = 0$ | $(1.5 + w_{DA})T - 10$ | | ns |
| $\overline{WE}$ pulse width | <92> | $t_{WP}$ | $w_{CP} = 0$ | $(1 + w_{DA})T - 10$ | | ns |

**Remarks 1.** $T = t_{CYK}$

**2.** $w_{CP}$: Number of waits specified by CPCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**3.** $w_{DA}$: Number of waits specified by DACxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**(d) Write timing (high-speed page DRAM access: on-page) (2/2)**




**Remarks 1.** These timings are for the following cases (n = 0 to 3, xx = 00 to 03, 10 to 13):

Number of waits (TCPW) specified by CPCxx bit of register DRCn: 1

Number of waits (TDAW) specified by DACxx bit of register DRCn: 1

**2.** Broken lines indicate high impedance.

**3.** n = 0 to 7

### (e) Read timing (EDO DRAM) (1/3)

| Parameter | | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Data input setup time (to CLKOUT↑) | | <26> | $t_{SKID}$ | | 10 | | ns |
| Data input hold time (from CLKOUT↑) | | <27> | $t_{HKID}$ | | 2 | | ns |
| Data output delay time from $\overline{OE}$↑ | | <37> | $t_{DRDOD}$ | | (0.5 + i)T – 10 | | ns |
| Row address setup time | | <56> | $t_{ASR}$ | | (0.5 + $w_{RP}$)T – 10 | | ns |
| Row address hold time | | <57> | $t_{RAH}$ | | (0.5 + $w_{RH}$)T – 10 | | ns |
| Column address setup time | | <58> | $t_{ASC}$ | | 0.5T – 10 | | ns |
| Column address hold time | | <59> | $t_{CAH}$ | | (0.5 + $w_{DA}$)T – 10 | | ns |
| $\overline{RAS}$ precharge time | | <61> | $t_{RP}$ | | (0.5 + $w_{RP}$)T – 5 | | ns |
| Column address read time (to $\overline{RAS}$↑) | | <64> | $t_{RAL}$ | | (2 + $w_{CP}$ + $w_{DA}$)T – 10 | | ns |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | | <66> | $t_{CRP}$ | | (1 + $w_{RP}$)T – 10 | | ns |
| $\overline{CAS}$ hold time | | <67> | $t_{CSH}$ | | (1.5 + $w_{RH}$ + $w_{DA}$)T – 10 | | ns |
| $\overline{WE}$ setup time (to $\overline{CAS}$↓) | | <68> | $t_{RCS}$ | | (2 + $w_{RP}$ +$w_{RH}$)T – 10 | | ns |
| $\overline{WE}$ hold time (from $\overline{RAS}$↑) | | <69> | $t_{RRH}$ | | 0.5T – 10 | | ns |
| $\overline{WE}$ hold time (from $\overline{CAS}$↑) | | <70> | $t_{RCH}$ | | 1.5T – 10 | | ns |
| $\overline{RAS}$ access time | | <73> | $t_{RAC}$ | | | (2 + $w_{RH}$ + $w_{DA}$)T – 20 | ns |
| Access time from column address | | <74> | $t_{AA}$ | | | (1.5 + $w_{DA}$)T – 20 | ns |
| $\overline{CAS}$ access time | | <75> | $t_{CAC}$ | | | (1 + $w_{DA}$)T – 20 | ns |
| Delay time from $\overline{RAS}$ to column address | | <76> | $t_{RAD}$ | | (0.5 + $w_{RH}$)T – 10 | | ns |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | | <77> | $t_{RCD}$ | | (1 + $w_{RH}$)T – 10 | | ns |
| Output buffer turn-off delay time (from $\overline{OE}$) | | <78> | $t_{OEZ}$ | | 0 | | ns |
| Access time from $\overline{CAS}$ precharge | | <80> | $t_{ACP}$ | | | (1.5 + $w_{CP}$ + $w_{DA}$)T – 20 | ns |
| $\overline{CAS}$ precharge time | | <81> | $t_{CP}$ | | (0.5 + $w_{CP}$)T – 5 | | ns |
| $\overline{RAS}$ hold time for $\overline{CAS}$ precharge | | <83> | $t_{RHCP}$ | | (2 + $w_{CP}$ + $w_{DA}$)T – 10 | | ns |
| Read cycle time | | <93> | $t_{HPC}$ | | (1 + $w_{DA}$ + $w_{CP}$)T – 10 | | ns |
| $\overline{RAS}$ pulse width | | <94> | $t_{RASP}$ | | (2.5 + $w_{RH}$ + $w_{DA}$)T – 10 | | ns |
| $\overline{CAS}$ pulse width | | <95> | $t_{HCAS}$ | | (0.5 + $w_{DA}$)T – 10 | | ns |
| $\overline{CAS}$ hold time from $\overline{OE}$ | Off-page | <96> | $t_{OCH1}$ | | (2 + $w_{RH}$ + $w_{DA}$)T – 10 | | ns |
| | On-page | <97> | $t_{OCH2}$ | | (0.5 + $w_{DA}$)T – 10 | | ns |
| Data input hold time (from $\overline{CAS}$↓) | | <98> | $t_{DHC}$ | | 0 | | ns |

**Remarks 1.** T = $t_{CYK}$

**2.** $w_{RP}$: Number of waits specified by RPCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**3.** $w_{RH}$: Number of waits specified by RHCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**4.** $w_{DA}$: Number of waits specified by DACxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**5.** $w_{CP}$: Number of waits specified by CPCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**6.** i: Number of idle states inserted when a write cycle follows the read cycle.

**(e) Read timing (EDO DRAM) (2/3)**

| Parameter | | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output enable access time | Off-page | <99> | $t_{OEA1}$ | | | $(2 + w_{RP} + w_{RH} + w_{DA})T - 20$ | ns |
| | On-page | <100> | $t_{OEA2}$ | | | $(1 + w_{CP} + w_{DA})T - 20$ | ns |

**Remarks 1.** $T = t_{CYK}$

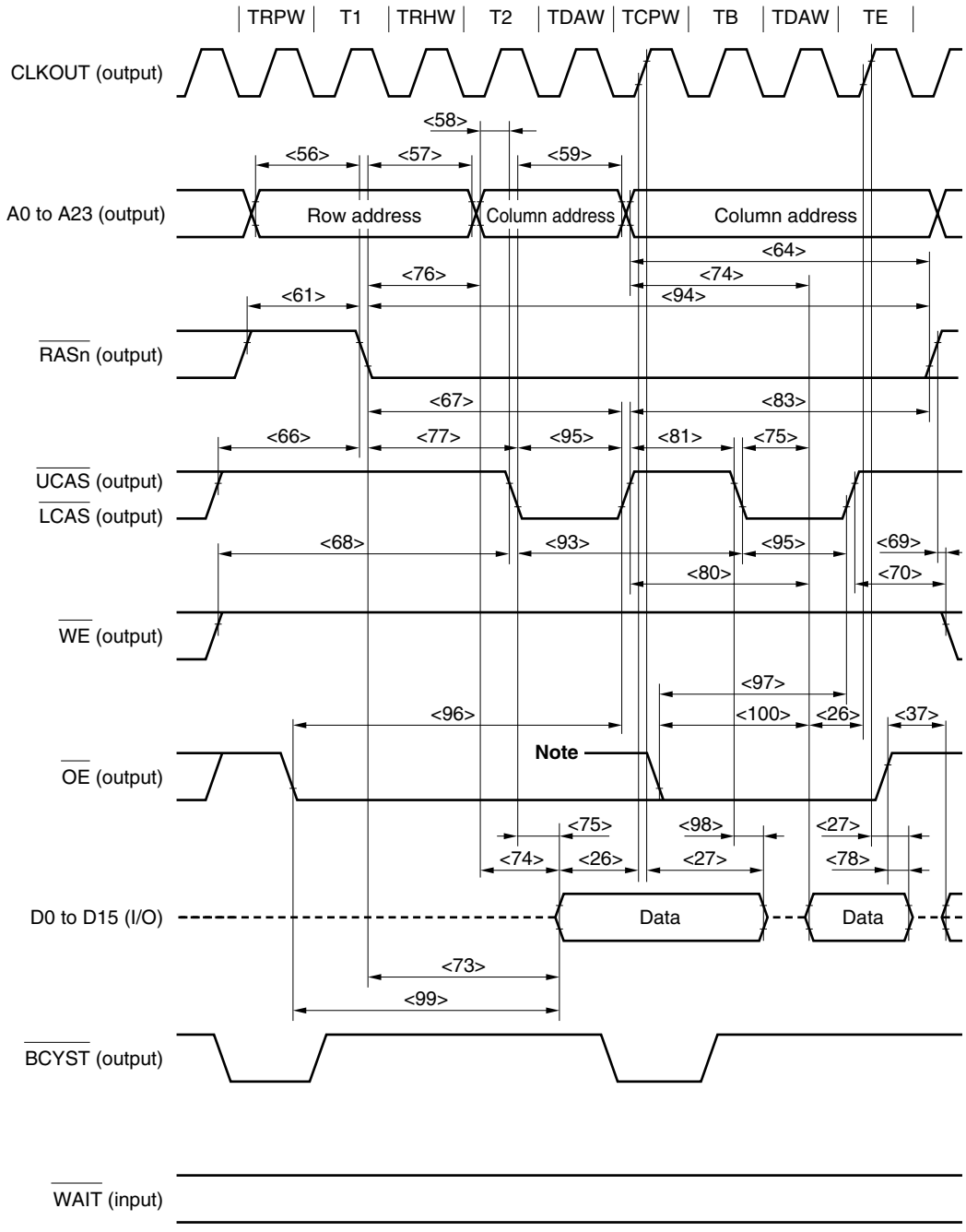
**2.** $w_{RP}$: Number of waits specified by RPCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**3.** $w_{RH}$: Number of waits specified by RHCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**4.** $w_{DA}$: Number of waits specified by DACxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**5.** $w_{CP}$: Number of waits specified by CPCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**(e) Read timing (EDO DRAM) (3/3)**




**Note** In case of on-page access from another cycle, while $\overline{\text{RASn}}$ is low level.

**Remarks 1.** These timings are for the following cases (n = 0 to 3, xx = 00 to 03, 10 to 13):

Number of waits (TRPW) specified by RPCxx bit of register DRCn: 1
Number of waits (TRHW) specified by RHCxx bit of register DRCn: 1
Number of waits (TDAW) specified by DACxx bit of register DRCn: 1
Number of waits (TCPW) specified by CPCxx bit of register DRCn: 1

**2.** Broken lines indicate high impedance.

**3.** n = 0 to 7

**[MEMO]**

**(f) Write timing (EDO DRAM) (1/2)**

| Parameter | | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Row address setup time | | <56> | $t_{ASR}$ | | $(0.5 + w_{RP})T - 10$ | | ns |
| Row address hold time | | <57> | $t_{RAH}$ | | $(0.5 + w_{RH})T - 10$ | | ns |
| Column address setup time | | <58> | $t_{ASC}$ | | $0.5T - 10$ | | ns |
| Column address hold time | | <59> | $t_{CAH}$ | | $(0.5 + w_{DA})T - 10$ | | ns |
| $\overline{RAS}$ precharge time | | <61> | $t_{RP}$ | | $(0.5 + w_{RP})T - 5$ | | ns |
| $\overline{RAS}$ hold time | | <63> | $t_{RSH}$ | | $(1.5 + w_{DA})T - 10$ | | ns |
| Column address read time (to $\overline{RAS}\uparrow$) | | <64> | $t_{RAL}$ | | $(2 + w_{CP} + w_{DA})T - 10$ | | ns |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | | <66> | $t_{CRP}$ | | $(1 + w_{RP})T - 10$ | | ns |
| $\overline{CAS}$ hold time | | <67> | $t_{CSH}$ | | $(1.5 + w_{RH} + w_{DA})T - 10$ | | ns |
| Delay time from $\overline{RAS}$ to column address | | <76> | $t_{RAD}$ | | $(0.5 + w_{RH})T - 10$ | | ns |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | | <77> | $t_{RCD}$ | | $(1 + w_{RH})T - 10$ | | ns |
| $\overline{CAS}$ precharge time | | <81> | $t_{CP}$ | | $(0.5 + w_{CP})T - 5$ | | ns |
| $\overline{RAS}$ hold time for $\overline{CAS}$ precharge | | <83> | $t_{RHCP}$ | | $(2 + w_{CP} + w_{DA})T - 10$ | | ns |
| $\overline{WE}$ hold time (from $\overline{CAS}\downarrow$) | | <85> | $t_{WCH}$ | | $(1 + w_{DA})T - 10$ | | ns |
| Data hold time (from $\overline{CAS}\downarrow$) | | <87> | $t_{DH}$ | | $(0.5 + w_{DA})T - 10$ | | ns |
| $\overline{WE}$ read time (to $\overline{RAS}\uparrow$) | On-page | <88> | $t_{RWL}$ | $w_{CP} = 0$ | $(1.5 + tw_{DA})T - 10$ | | ns |
| $\overline{WE}$ read time (to $\overline{CAS}\uparrow$) | On-page | <89> | $t_{CWL}$ | $w_{CP} = 0$ | $(0.5 + w_{DA})T - 10$ | | ns |
| $\overline{WE}$ pulse width | On-page | <92> | $t_{WP}$ | $w_{CP} = 0$ | $(1 + w_{DA})T - 10$ | | ns |
| Write cycle time | | <93> | $t_{HPC}$ | | $(1 + w_{DA} + w_{CP})T - 10$ | | ns |
| $\overline{RAS}$ pulse width | | <94> | $t_{RASP}$ | | $(2.5 + w_{RH} + w_{DA})T - 10$ | | ns |
| $\overline{CAS}$ pulse width | | <95> | $t_{HCAS}$ | | $(0.5 + w_{DA})T - 10$ | | ns |
| $\overline{WE}$ setup time (to $\overline{CAS}\downarrow$) | Off-page | <101> | $t_{WCS1}$ | | $(1 + w_{RP} + w_{RH})T - 10$ | | ns |
| | On-page | <102> | $t_{WCS2}$ | $w_{CP} \geq 1$ | $w_{CP}T - 10$ | | ns |
| Data setup time (to $\overline{CAS}\downarrow$) | Off-page | <103> | $t_{DS1}$ | | $(1.5 + w_{RP} + w_{RH})T - 10$ | | ns |
| | On-page | <104> | $t_{DS2}$ | | $(0.5 + w_{CP})T - 10$ | | ns |

**Remarks 1.** $T = t_{CYK}$

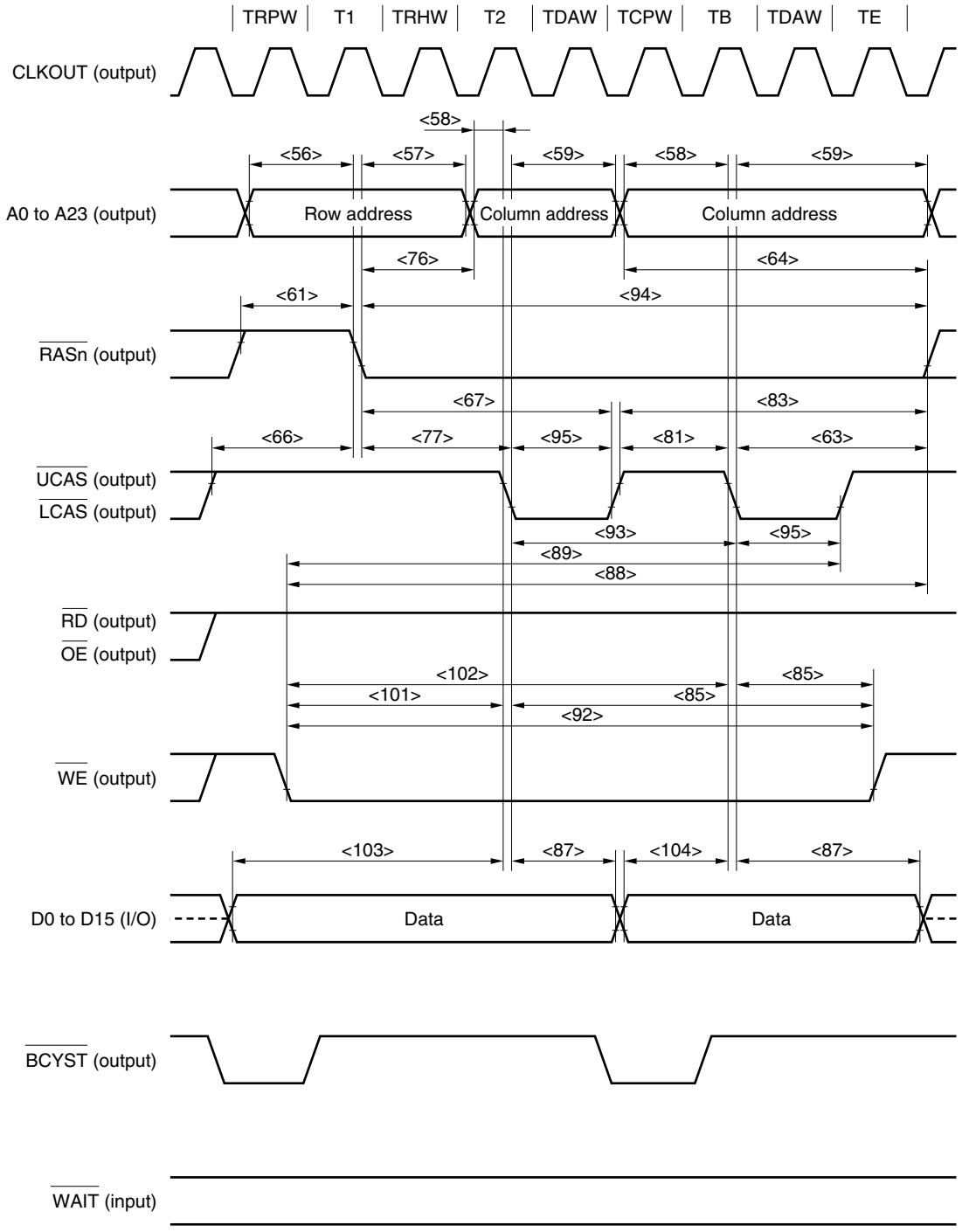
**2.** $w_{RP}$: Number of waits specified by RPCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**3.** $w_{RH}$: Number of waits specified by RHCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**4.** $w_{DA}$: Number of waits specified by DACxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**5.** $w_{CP}$: Number of waits specified by CPCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**(f) Write timing (EDO DRAM) (2/2)**




**Remarks 1.** These timings are for the following cases (n = 0 to 3, xx = 00 to 03, 10 to 13):

Number of waits (TRPW) specified by RPCxx bit of register DRCn: 1
Number of waits (TRHW) specified by RHCxx bit of register DRCn: 1
Number of waits (TDAW) specified by DACxx bit of register DRCn: 1
Number of waits (TCPW) specified by CPCxx bit of register DRCn: 1

**2.** Broken lines indicate high impedance.

**3.** n = 0 to 7

### (g) DMA flyby transfer timing (DRAM (EDO, high-speed page) → external I/O transfer) (1/3)

| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $\overline{WAIT}$ setup time (to CLKOUT↓) | <24> | $t_{SWK}$ | | 10 | | ns |
| $\overline{WAIT}$ hold time (from CLKOUT↓) | <25> | $t_{HKW}$ | | 2 | | ns |
| Delay time from $\overline{OE}$↑ to data output | <37> | $t_{DRDOD}$ | | (0.5 + i)T – 10 | | ns |
| Delay time from address to $\overline{IOWR}$↓ | <41> | $t_{DAWR}$ | | ($0.5 + w_{RP}$)T – 5 | | ns |
| Address setup time (to $\overline{IOWR}$↑) | <42> | $t_{SAWR}$ | | (2 + $w_{RP}$ + $w_{RH}$ + $w_{DA}$ + w)T –10 | | ns |
| Delay time from $\overline{IOWR}$↑ to address | <43> | $t_{DWRA}$ | | 0.5T – 5 | | ns |
| Delay time from $\overline{IOWR}$↑ to $\overline{RD}$↑ | <48> | $t_{DWRRD}$ | $w_F$ = 0 | 0 | | ns |
| | | | $w_F$ = 1 | T – 10 | | ns |
| $\overline{IOWR}$ low-level width | <50> | $t_{WWRL}$ | | (2 + $w_{RH}$ + $w_{DA}$ + w)T – 10 | | ns |
| Row address setup time | <56> | $t_{ASR}$ | | ($0.5 + w_{RP}$)T – 10 | | ns |
| Row address hold time | <57> | $t_{RAH}$ | | ($0.5 + w_{RH}$)T – 10 | | ns |
| Column address setup time | <58> | $t_{ASC}$ | | 0.5T – 10 | | ns |
| Column address hold time | <59> | $t_{CAH}$ | | (1.5 + $w_{DA}$ + $w_F$ + w)T – 10 | | ns |
| Read/write cycle time | <60> | $t_{RC}$ | | (3 + $w_{RP}$ + $w_{RH}$ + $w_{DA}$ + $w_F$ + w)T – 10 | | ns |
| $\overline{RAS}$ precharge time | <61> | $t_{RP}$ | | ($0.5 + w_{RP}$)T – 5 | | ns |
| $\overline{RAS}$ hold time | <63> | $t_{RSH}$ | | (1.5 + $w_{DA}$ + $w_F$ + w)T – 10 | | ns |
| Column address read time for $\overline{RAS}$ | <64> | $t_{RAL}$ | | (2 + $w_{CP}$ + $w_{DA}$ + $w_F$ + w)T – 10 | | ns |
| $\overline{CAS}$ pulse width | <65> | $t_{CAS}$ | | (1 + $w_{DA}$ + $w_F$ + w)T – 10 | | ns |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | <66> | $t_{CRP}$ | | ($1 + w_{RP}$)T –10 | | ns |
| $\overline{CAS}$ hold time | <67> | $t_{CSH}$ | | (2 + $w_{RH}$ + $w_{DA}$ + $w_F$ + w)T – 10 | | ns |
| $\overline{WE}$ setup time (to $\overline{CAS}$↓) | <68> | $t_{RCS}$ | | (2 + $w_{RP}$ + $w_{RH}$)T – 10 | | ns |
| $\overline{WE}$ hold time (from $\overline{RAS}$↑) | <69> | $t_{RRH}$ | | 0.5T – 10 | | ns |
| $\overline{WE}$ hold time (from $\overline{CAS}$↑) | <70> | $t_{RCH}$ | | 1.5T – 10 | | ns |
| $\overline{CAS}$ precharge time | <71> | $t_{CPN}$ | | (2 + $w_{RP}$ + $w_{RH}$)T – 5 | | ns |
| Delay time from $\overline{RAS}$ to column address | <76> | $t_{RAD}$ | | ($0.5 + w_{RH}$)T – 10 | | ns |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | <77> | $t_{RCD}$ | | ($1 + w_{RH}$)T – 10 | | ns |

**Remarks 1.** T = $t_{CYK}$

**2.** w: Number of waits due to $\overline{WAIT}$

**3.** $w_{RP}$: Number of waits specified by RPCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**4.** $w_{RH}$: Number of waits specified by RHCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**5.** $w_{DA}$: Number of waits specified by DACxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**6.** $w_{CP}$: Number of waits specified by CPCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**7.** $w_F$: Number of waits inserted to source-side access during DMA flyby transfer

**8.** i: Number of idle states inserted when a write cycle follows the read cycle.

**(g) DMA flyby transfer timing (DRAM (EDO, high-speed page) → external I/O transfer) (2/3)**

| Parameter | | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output buffer turn-off delay time (from $\overline{OE}$↑) | | <78> | $t_{OEZ}$ | | 0 | | ns |
| Output buffer turn-off delay time (from $\overline{CAS}$↑) | | <79> | $t_{OFF}$ | | 0 | | ns |
| $\overline{CAS}$ precharge time | | <81> | $t_{CP}$ | | $(0.5 + w_{CP})T - 5$ | | ns |
| High-speed mode cycle time | | <82> | $t_{PC}$ | | $(2 + w_{CP} + w_{DA} + w_F + w)T - 10$ | | ns |
| $\overline{RAS}$ hold time for $\overline{CAS}$ precharge | | <83> | $t_{RHCP}$ | | $(2.5 + w_{CP} + w_{DA} + w_F + w)T - 10$ | | ns |
| $\overline{RAS}$ pulse width | | <94> | $t_{RASP}$ | | $(2.5 + w_{RH} + w_{DA} + w_F + w)T - 10$ | | ns |
| $\overline{CAS}$ hold time from $\overline{OE}$ (from $\overline{CAS}$↑) | Off-page | <96> | $t_{OCH1}$ | | $(2.5 + w_{RP} + w_{RH} + w_{DA} + w_F + w)T - 10$ | | ns |
| | On-page | <97> | $t_{OCH2}$ | | $(1.5 + w_{CP} + w_{DA} + w_F + w)T - 10$ | | ns |
| Delay time from $\overline{DMAAKm}$↓ to $\overline{CAS}$↓ | | <105> | $t_{DDACS}$ | | $(1.5 + w_{RH})T - 10$ | | ns |
| Delay time from $\overline{IOWR}$↓ to $\overline{CAS}$↓ | | <106> | $t_{DRDCS}$ | | $(1 + w_{RH})T - 10$ | | ns |

**Remarks 1.** T = $t_{CYK}$

**2.** w: Number of waits due to $\overline{WAIT}$

**3.** $w_{CP}$: Number of waits specified by CPCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**4.** $w_{DA}$: Number of waits specified by DACxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

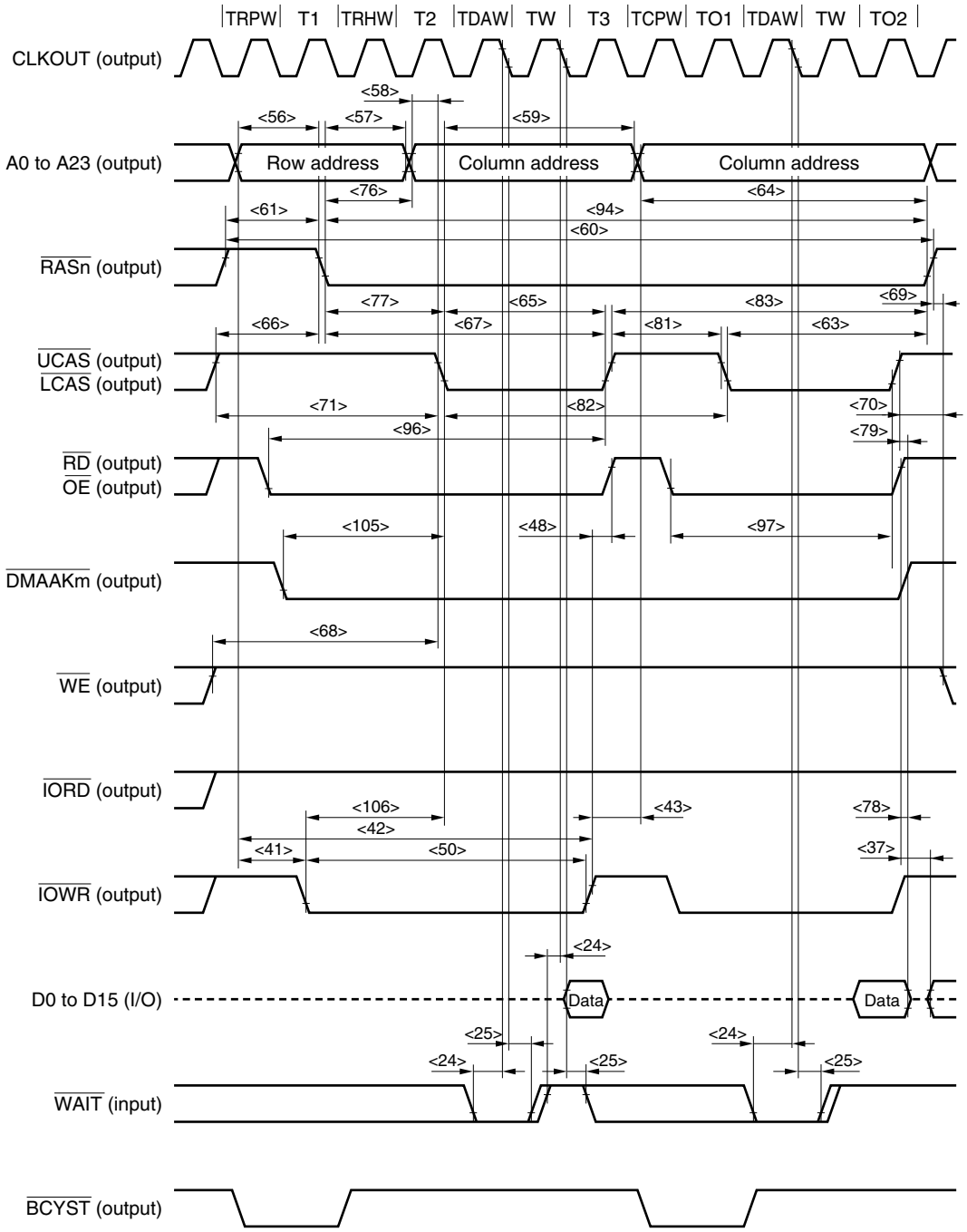
**5.** $w_{RH}$: Number of waits specified by RHCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**6.** $w_{RP}$: Number of waits specified by RPCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**7.** $w_F$: Number of waits inserted to source-side access during DMA flyby transfer

**8.** m = 0 to 3

**(g) DMA flyby transfer timing (DRAM (EDO, high-speed page) → external I/O transfer) (3/3)**




**Remarks 1.** These timings are for the following cases (n = 0 to 3, xx = 00 to 03, 10 to 13):

Number of waits (TRPW) specified by RPCxx bit of register DRCn: 1

Number of waits (TRHW) specified by RHCxx bit of register DRCn: 1

Number of waits (TDAW) specified by DACxx bit of register DRCn: 1

Number of waits (TCPW) specified by CPCxx bit of register DRCn: 1

Number of waits inserted to source-side access during DMA flyby transfer: 0

**2.** Broken lines indicate high impedance.

**3.** n = 0 to 7, m = 0 to 3

**(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (1/3)**

| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $\overline{WAIT}$ setup time (to CLKOUT↓) | <24> | $t_{SWK}$ | | 10 | | ns |
| $\overline{WAIT}$ hold time (from CLKOUT↓) | <25> | $t_{HKW}$ | | 2 | | ns |
| $\overline{IORD}$ low-level width | <32> | $t_{WRDL}$ | | $(2 + w_{RH} + w_{DA} + w_F + w)T - 10$ | | ns |
| $\overline{IORD}$ high-level width | <33> | $t_{WRDH}$ | | $T - 10$ | | ns |
| Delay time from address to $\overline{IORD}$↑ | <34> | $t_{DARD}$ | | $0.5T - 5$ | | ns |
| Delay time from $\overline{IORD}$↑ to address | <35> | $t_{DRDA}$ | | $(0.5 + i)T - 5$ | | ns |
| Row address setup time | <56> | $t_{ASR}$ | | $(0.5 + w_{RP})T - 10$ | | ns |
| Row address hold time | <57> | $t_{RAH}$ | | $(0.5 + w_{RH})T - 10$ | | ns |
| Column address setup time | <58> | $t_{ASC}$ | | $0.5T - 10$ | | ns |
| Column address hold time | <59> | $t_{CAH}$ | | $(1.5 + w_{DA} + w_F)T - 10$ | | ns |
| Read/write cycle time | <60> | $t_{RC}$ | | $(3 + w_{RP} + w_{RH} + w_{DA} + w_F + w)T - 10$ | | ns |
| $\overline{RAS}$ precharge time | <61> | $t_{RP}$ | | $(0.5 + w_{RP})T - 5$ | | ns |
| $\overline{RAS}$ hold time | <63> | $t_{RSH}$ | | $(1.5 + w_{DA} + w_F)T - 10$ | | ns |
| Column address read time for $\overline{RAS}$ | <64> | $t_{RAL}$ | | $(2 + w_{CP} + w_{DA} + w_F + w)T - 10$ | | ns |
| $\overline{CAS}$ pulse width | <65> | $t_{CAS}$ | | $(1 + w_{DA} + w_F)T - 10$ | | ns |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | <66> | $t_{CRP}$ | | $(1 + w_{RP})T - 10$ | | ns |
| $\overline{CAS}$ hold time | <67> | $t_{CSH}$ | | $(2 + w_{RH} + w_{DA} + w_F + w)T - 10$ | | ns |
| $\overline{CAS}$ precharge time | <71> | $t_{CPN}$ | | $(2 + w_{RP} + w_{RH} + w)T - 5$ | | ns |
| Delay time from $\overline{RAS}$ to column address | <76> | $t_{RAD}$ | | $(0.5 + w_{RH})T - 10$ | | ns |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | <77> | $t_{RCD}$ | | $(1 + w_{RH} + w)T - 10$ | | ns |
| $\overline{CAS}$ precharge time | <81> | $t_{CP}$ | | $(0.5 + w_{CP} + w)T - 5$ | | ns |
| High-speed page mode cycle time | <82> | $t_{PC}$ | | $(2 + w_{CP} + w_{DA} + w_F + w)T - 10$ | | ns |
| $\overline{RAS}$ hold time for $\overline{CAS}$ precharge | <83> | $t_{RHCP}$ | | $(2.5 + w_{CP} + w_{DA} + w)T - 10$ | | ns |
| $\overline{WE}$ hold time (from $\overline{CAS}$↓) | <85> | $t_{WCH}$ | | $(1 + w_{DA})T - 10$ | | ns |
| $\overline{WE}$ read time (to $\overline{RAS}$↑) | <88> | $t_{RWL}$ | $w_{CP} = 0$ | $(1.5 + w_{DA} + w)T - 10$ | | ns |
| $\overline{WE}$ read time (to $\overline{CAS}$↑) | <89> | $t_{CWL}$ | $w_{CP} = 0$ | $(1 + w_{DA} + w)T - 10$ | | ns |
| $\overline{WE}$ pulse width | <92> | $t_{WP}$ | $w_{CP} = 0$ | $(1 + w_{DA} + w)T - 10$ | | ns |
| $\overline{RAS}$ pulse width | <94> | $t_{RASP}$ | | $(2.5 + w_{RH} + w_{DA} + w_F + w)T - 10$ | | ns |

**Remarks 1.** $T = t_{CYK}$

**2.** w: Number of waits due to $\overline{WAIT}$

**3.** $w_{RH}$: Number of waits specified by RHCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**4.** $w_{DA}$: Number of waits specified by DACxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**5.** $w_{RP}$: Number of waits specified by RPCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**6.** $w_{CP}$: Number of waits specified by CPCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**7.** $w_F$: Number of waits inserted to source-side access during DMA flyby transfer.

**8.** i: Number of idle states inserted when a write cycle follows the read cycle.

**9.** n = 0 to 7

**(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (2/3)**

| Parameter | | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| $\overline{WE}$ setup time (to $\overline{CAS}\downarrow$) | Off-page | <101> | $t_{WCS1}$ | $w_{CP} = 0$ | $(1 + w_{RH} + w_{RP} + w)T - 10$ | | ns |
| | On-page | <102> | $t_{WCS2}$ | $w_{CP} \geq 1$ | $w_{CP}T - 10$ | | ns |
| Delay time from $\overline{DMAAKm}\downarrow$ to $\overline{CAS}\downarrow$ | | <105> | $t_{DDACS}$ | | $(1.5 + w_{RH} + w)T - 10$ | | ns |
| Delay time from $\overline{IORD}\downarrow$ to $\overline{CAS}\downarrow$ | | <106> | $t_{DRDCS}$ | | $(1 + w_{RH} + w)T - 10$ | | ns |
| Delay time from $\overline{WE}\uparrow$ to $\overline{IORD}\uparrow$ | | <107> | $t_{DWERD}$ | $w_F = 0$ | 0 | | ns |
| | | | | $w_F = 1$ | $T - 10$ | | ns |

**Remarks 1.** $T = t_{CYK}$

**2.** w: Number of waits due to $\overline{WAIT}$

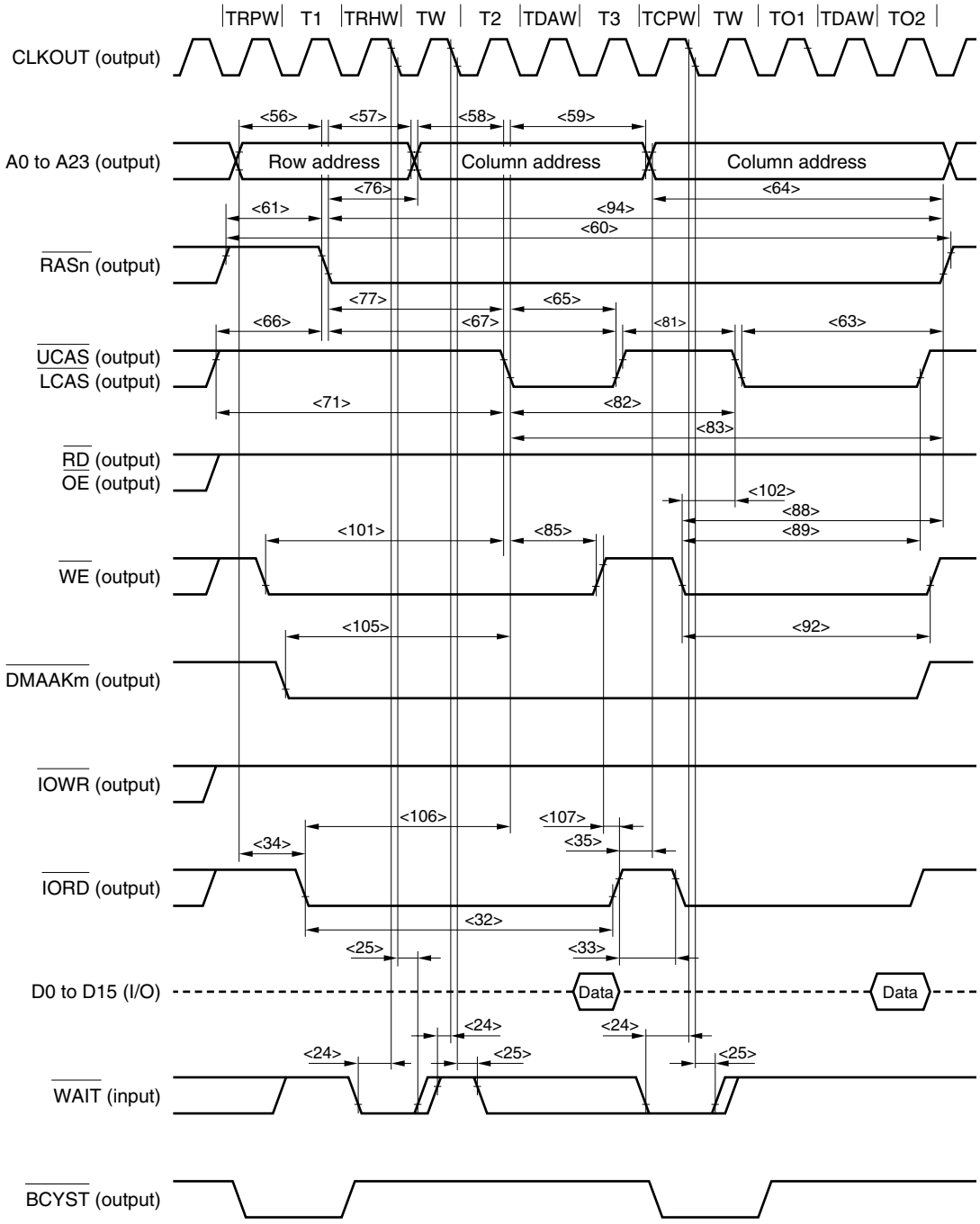
**3.** $w_{RH}$: Number of waits specified by RHCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**4.** $w_{RP}$: Number of waits specified by RPCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**5.** $w_{CP}$: Number of waits specified by CPCxx bit of register DRCn (n = 0 to 3, xx = 00 to 03, 10 to 13)

**6.** m = 0 to 3

**(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (3/3)**




**Remarks 1.** These timings are for the following cases (n = 0 to 3, xx = 00 to 03, 10 to 13):

Number of waits (TRPW) specified by RPCxx bit of register DRCn: 1

Number of waits (TRHW) specified by RHCxx bit of register DRCn: 1

Number of waits (TDAW) specified by DACxx bit of register DRCn: 1

Number of waits (TCPW) specified by CPCxx bit of register DRCn: 1

Number of waits inserted to source-side access during DMA flyby transfer: 0

**2.** Broken lines indicate high impedance.

**3.** n = 0 to 7, m = 0 to 3

### (i) CBR refresh timing

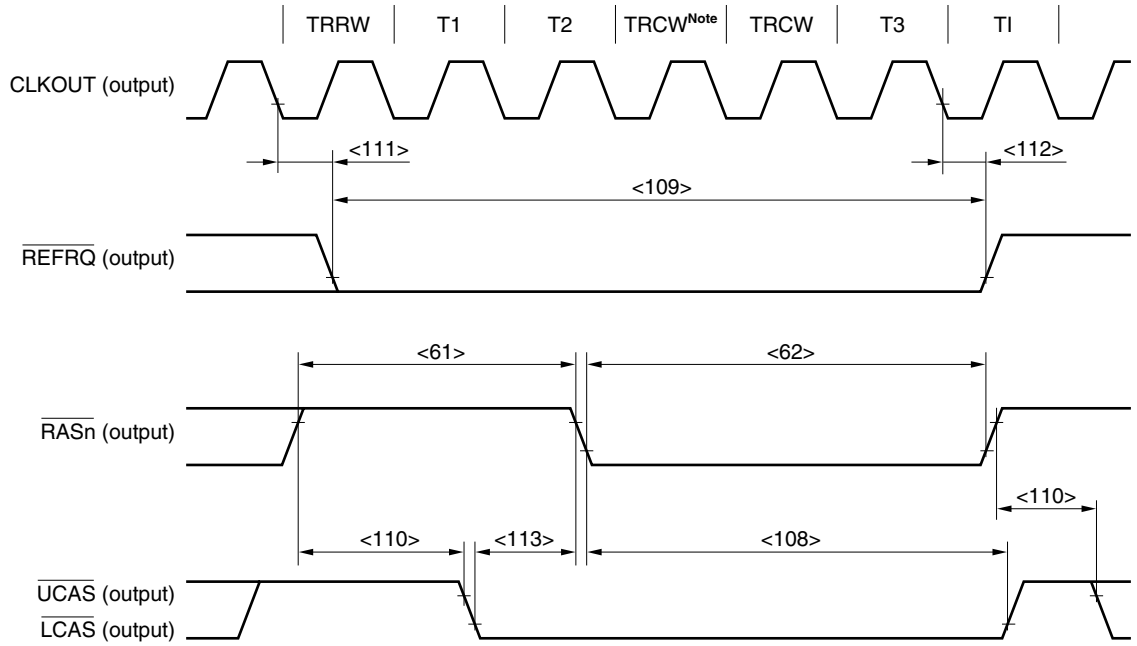
| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $\overline{RAS}$ precharge time | <61> | $t_{RP}$ | | $(1.5 + w_{RRW})T - 5$ | | ns |
| $\overline{RAS}$ pulse width | <62> | $t_{RAS}$ | | $(1.5 + w_{RCW}$ Note$)T - 10$ | | ns |
| $\overline{CAS}$ hold time | <108> | $t_{CHR}$ | | $(1.5 + w_{RCW}$ Note$)T - 10$ | | ns |
| $\overline{REFRQ}$ pulse width | <109> | $t_{WRFL}$ | | $(3 + w_{RRW} + w_{RCW}$ Note$)T - 10$ | | ns |
| $\overline{RAS}$ precharge $\overline{CAS}$ hold time | <110> | $t_{RPC}$ | | $(0.5 + w_{RRW})T - 10$ | | ns |
| $\overline{REFRQ}$ active delay time (from CLKOUT↓) | <111> | $t_{DKRF}$ | | 2 | 10 | ns |
| $\overline{REFRQ}$ inactive delay time (from CLKOUT↓) | <112> | $t_{HKRF}$ | | 2 | 10 | ns |
| $\overline{CAS}$ setup time | <113> | $t_{CSR}$ | | T – 10 | | ns |

**Note** $w_{RCW}$ is inserted for at least 1 clock, regardless of the setting of bits RCW0 to RCW2 of register RWC.

**Remarks 1.** $T = t_{CYK}$

**2.** $w_{RRW}$: Number of waits specified by bits RRW0 and RRW1 of register RWC

**3.** $w_{RCW}$: Number of waits specified by bits RCW0 to RCW2 of register RWC.




**Note** This TRCW is always inserted, regardless of the setting of bits RCW0 to RCW2 of register RWC.

**Remarks 1.** These timings are for the following cases:

Number of waits specified by bits RRW0 and RRW1 of register RWC (TRRW): 1

Number of waits specified by bits RCW0 to RCW2 of register RWC (TRCW): 2

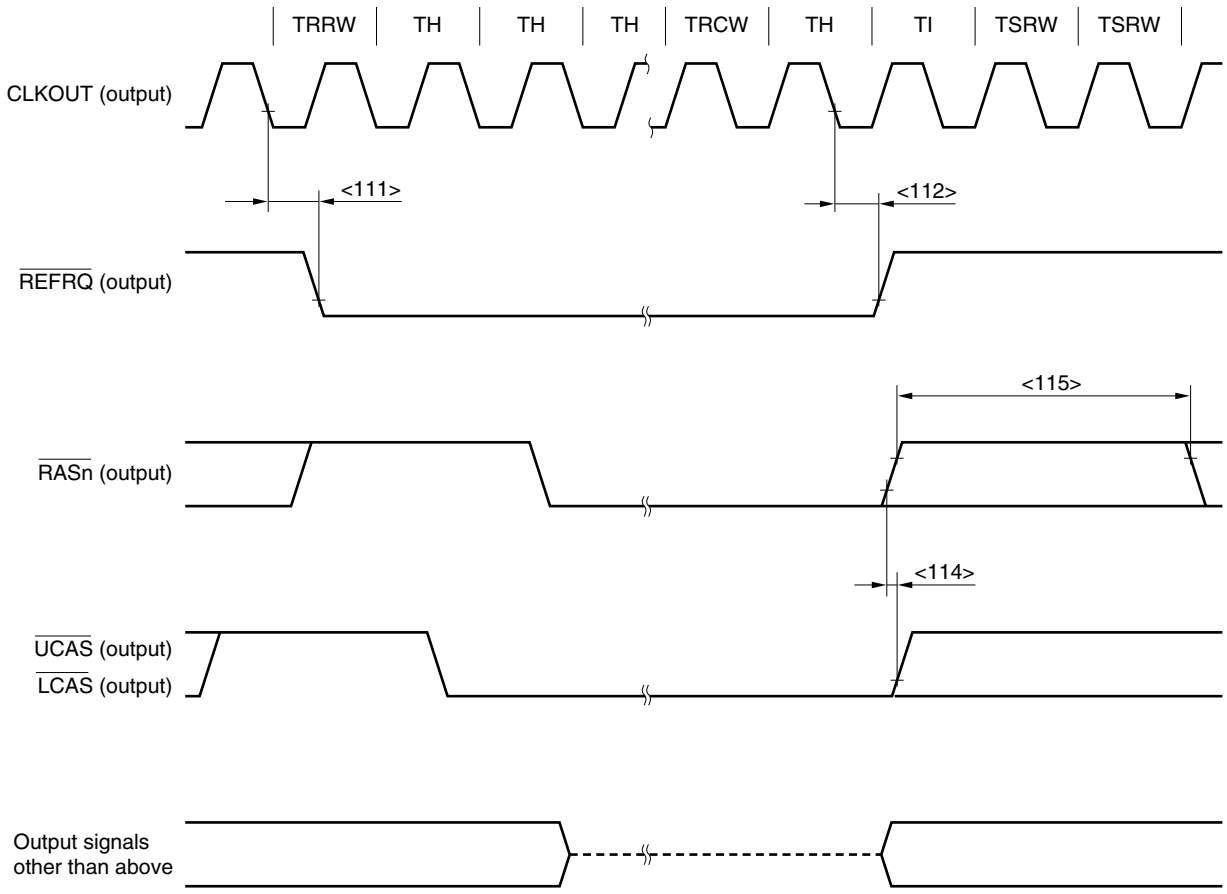
**2.** n = 0 to 7

### (j) CBR self refresh timing

| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $\overline{\text{REFRQ}}$ active delay time (from CLKOUT↓) | <111> | $t_{DKRF}$ | | 2 | 10 | ns |
| $\overline{\text{REFRQ}}$ inactive delay time (from CLKOUT↓) | <112> | $t_{HKRF}$ | | 2 | 10 | ns |
| $\overline{\text{CAS}}$ hold time | <114> | $t_{CHS}$ | | –5 | | ns |
| $\overline{\text{RAS}}$ precharge time | <115> | $t_{RPS}$ | | (1 + 2$w_{SRW}$)T – 10 | | ns |

**Remarks 1.** T = $t_{CYK}$

**2.** $w_{SRW}$: Number of waits specified by bits SRW0 to SRW2 of register RWC.




**Remarks 1.** These timings are for the following cases:

Number of waits (TRRW) specified by bits RRW0 and RRW1 of register RWC: 1

Number of waits (TRCW) specified by bits RCW0 to RCW2 of register RWC: 1

Number of waits (TSRW) specified by bits SRW0 to SRW2 of register RWC: 2

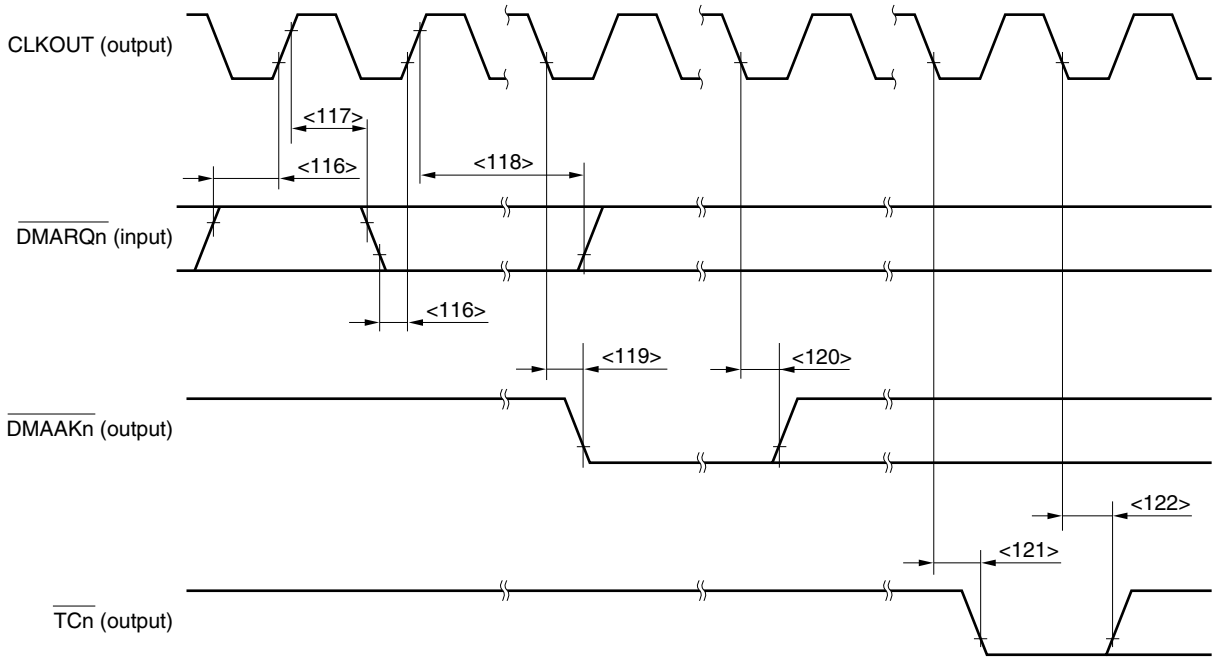
**2.** Broken lines indicate high impedance.

**3.** n = 0 to 7

### (7) DMAC timing

| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $\overline{\text{DMARQn}}$ setup time (to CLKOUT↑) | <116> | $t_{SDRK}$ | | 10 | | ns |
| $\overline{\text{DMARQn}}$ hold time (from CLKOUT↑) | <117> | $t_{HKDR1}$ | | 2 | | ns |
| | <118> | $t_{HKDR2}$ | | Until $\overline{\text{DMAAKn}}$↓ | | ns |
| $\overline{\text{DMAAKn}}$ output delay time (from CLKOUT↓) | <119> | $t_{DKDA}$ | | 2 | 10 | ns |
| $\overline{\text{DMAAKn}}$ output hold time (from CLKOUT↓) | <120> | $t_{HKDA}$ | | 2 | 10 | ns |
| $\overline{\text{TCn}}$ output delay time (from CLKOUT↓) | <121> | $t_{DKTC}$ | | 2 | 10 | ns |
| $\overline{\text{TCn}}$ output hold time (from CLKOUT↓) | <122> | $t_{HKTC}$ | | 2 | 10 | ns |

**Remark** n = 0 to 3




**Remark** n = 0 to 3

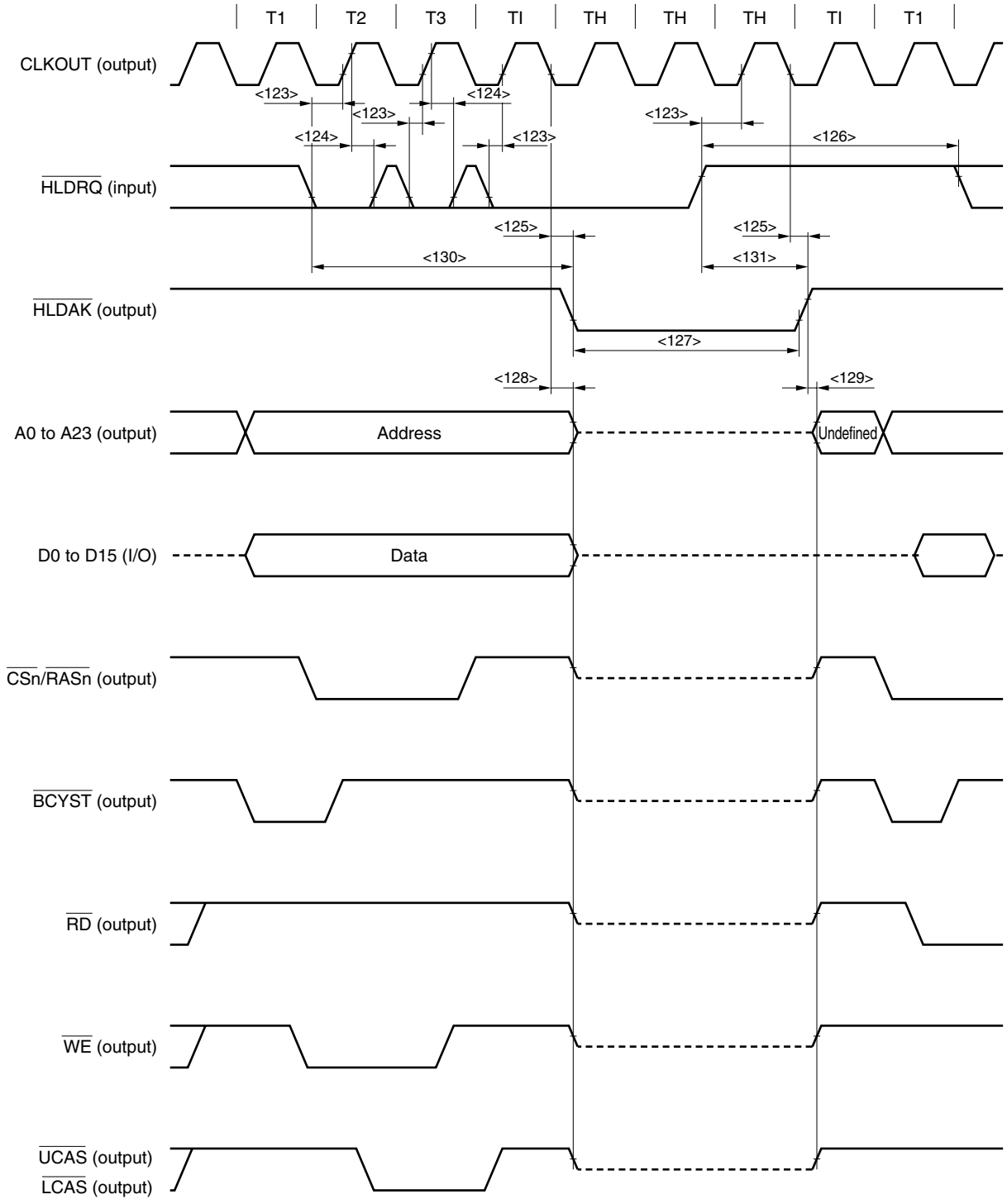
**[MEMO]**

### (8) Bus hold timing (1/2)

| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $\overline{\text{HLDRQ}}$ setup time (to CLKOUT↑) | <123> | $t_{SHRK}$ | | 10 | | ns |
| $\overline{\text{HLDRQ}}$ hold time (from CLKOUT↑) | <124> | $t_{HKHR}$ | | 5 | | ns |
| Delay time from CLKOUT↓ to $\overline{\text{HLDAK}}$ | <125> | $t_{DKHA}$ | | 2 | 10 | ns |
| $\overline{\text{HLDRQ}}$ high-level width | <126> | $t_{WHQH}$ | | T + 17 | | ns |
| $\overline{\text{HLDAK}}$ low-level width | <127> | $t_{WHAL}$ | | T – 8 | | ns |
| Delay time from CLKOUT↓ to bus float | <128> | $t_{DKCF}$ | | | 10 | ns |
| Delay time from $\overline{\text{HLDAK}}$↑ to bus output | <129> | $t_{DHAC}$ | | 0 | | ns |
| Delay time from $\overline{\text{HLDRQ}}$↓ to $\overline{\text{HLDAK}}$↓ | <130> | $t_{DHQHA1}$ | | 2.5T | | ns |
| Delay time from $\overline{\text{HLDRQ}}$↑ to $\overline{\text{HLDAK}}$↑ | <131> | $t_{DHQHA2}$ | | 0.5T | 1.5T | ns |

**Remark** T = $t_{CYK}$

**(8) Bus hold timing (2/2)**




**Remarks 1.** Broken lines indicate high impedance.

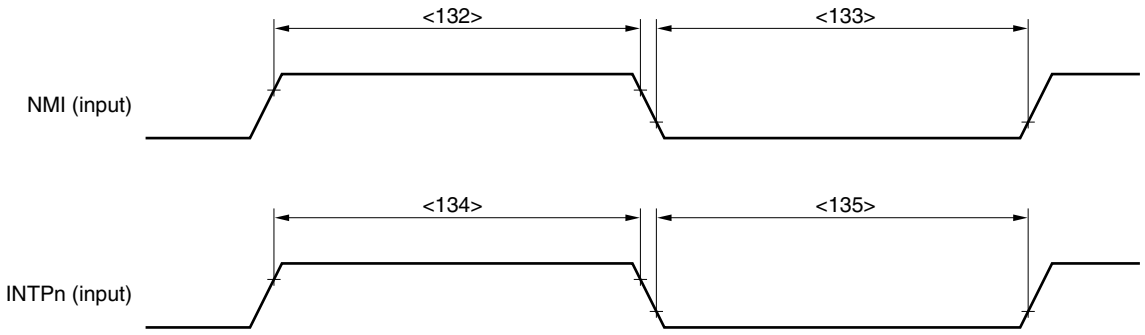
**2.** n = 0 to 7

### (9) Interrupt timing

| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| NMI high-level width | <132> | $t_{WNIH}$ | | 500 | | ns |
| NMI low-level width | <133> | $t_{WNIL}$ | | 500 | | ns |
| INTPn high-level width | <134> | $t_{WITH}$ | | 4T + 10 | | ns |
| INTPn low-level width | <135> | $t_{WITL}$ | | 4T + 10 | | ns |

**Remarks 1.** n = 100 to 103, 110 to 113, 120 to 123, 130 to 133, 140 to 143, and 150 to 153

**2.** T = $t_{CYK}$



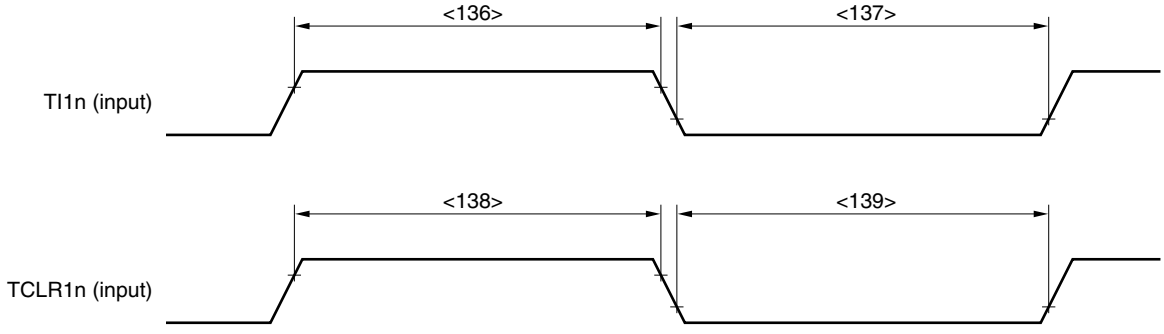

**Remark** n = 100 to 103, 110 to 113, 120 to 123, 130 to 133, 140 to 143, and 150 to 153

### (10) RPU timing

| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| TI1n high-level width | <136> | $t_{WTIH}$ | | 3T + 18 | | ns |
| TI1n low-level width | <137> | $t_{WTIL}$ | | 3T + 18 | | ns |
| TCLR1n high-level width | <138> | $t_{WTCH}$ | | 3T + 18 | | ns |
| TCLR1n low-level width | <139> | $t_{WTCL}$ | | 3T + 18 | | ns |

**Remarks 1.** n = 0 to 5

**2.** T = $t_{CYK}$

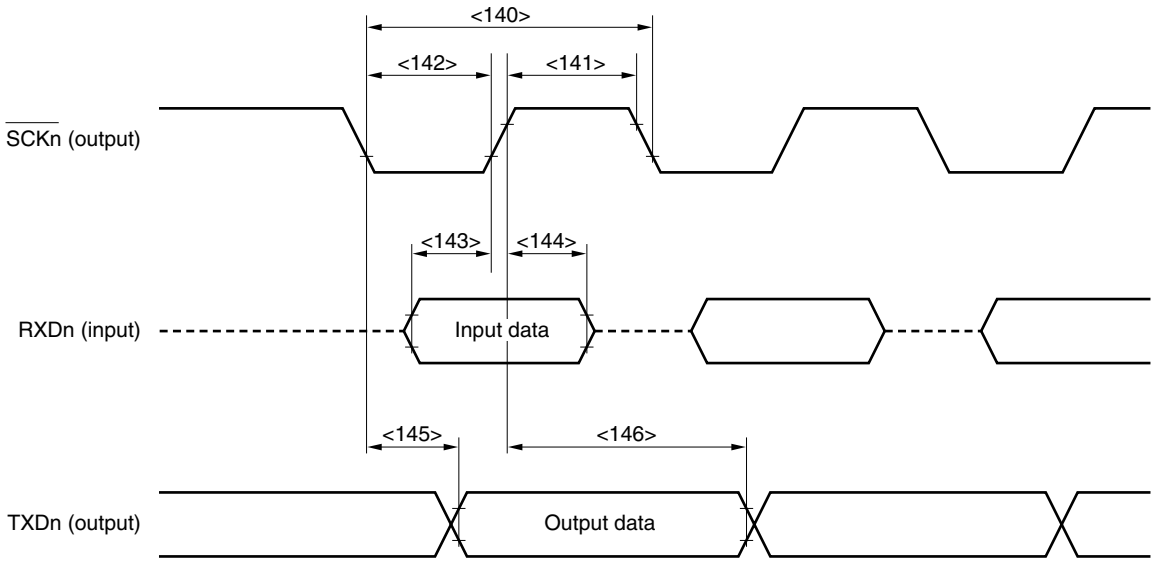



**Remark** n = 0 to 5

### (11) UART0, UART1 timing (synchronized with clock, master mode only)

| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $\overline{SCKn}$ cycle | <140> | $t_{CYSK0}$ | Output | 250 | | ns |
| $\overline{SCKn}$ high-level width | <141> | $t_{WSK0H}$ | Output | $0.5t_{CYSK0} - 20$ | | ns |
| $\overline{SCKn}$ low-level width | <142> | $t_{WSK0L}$ | Output | $0.5t_{CYSK0} - 20$ | | ns |
| RXDn setup time (to $\overline{SCKn}\uparrow$) | <143> | $t_{SRXSK}$ | | 30 | | ns |
| RXDn hold time (from $\overline{SCKn}\uparrow$) | <144> | $t_{HSKRX}$ | | 0 | | ns |
| TXDn output delay time (from $\overline{SCKn}\downarrow$) | <145> | $t_{DSKTX}$ | | | 20 | ns |
| TXDn output hold time (from $\overline{SCKn}\uparrow$) | <146> | $t_{HSKTX}$ | | $0.5t_{CYSK0} - 5$ | | ns |

**Remark** n = 0, 1




**Remarks 1.** Broken lines indicate high impedance.

**2.** n = 0, 1

### (12) CSI0 to CSI3 timing

#### (a) Master mode

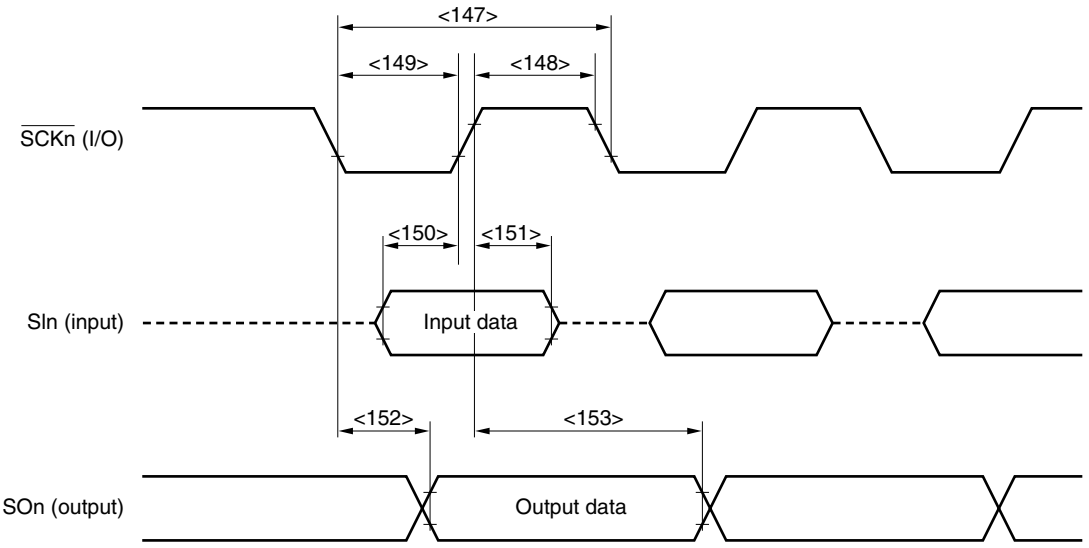
| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $\overline{SCKn}$ cycle | <147> | $t_{CYSK1}$ | Output | 100 | | ns |
| $\overline{SCKn}$ high-level width | <148> | $t_{WSK1H}$ | Output | $0.5t_{CYSK1} - 20$ | | ns |
| $\overline{SCKn}$ low-level width | <149> | $t_{WSK1L}$ | Output | $0.5t_{CYSK1} - 20$ | | ns |
| SIn setup time (to $\overline{SCKn}\uparrow$) | <150> | $t_{SSISK}$ | | 30 | | ns |
| SIn hold time (from $\overline{SCKn}\uparrow$) | <151> | $t_{HSKSI}$ | | 0 | | ns |
| SOn output delay time (from $\overline{SCKn}\downarrow$) | <152> | $t_{DSKSO}$ | | | 20 | ns |
| SOn output hold time (from $\overline{SCKn}\uparrow$) | <153> | $t_{HSKSO}$ | | $0.5t_{CYSK1} - 5$ | | ns |

**Remark** n = 0 to 3

#### (b) Slave mode

| Parameter | Symbol | | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $\overline{SCKn}$ cycle | <147> | $t_{CYSK1}$ | Input | 100 | | ns |
| $\overline{SCKn}$ high-level width | <148> | $t_{WSK1H}$ | Input | 30 | | ns |
| $\overline{SCKn}$ low-level width | <149> | $t_{WSK1L}$ | Input | 30 | | ns |
| SIn setup time (to $\overline{SCKn}\uparrow$) | <150> | $t_{SSISK}$ | | 10 | | ns |
| SIn hold time (from $\overline{SCKn}\uparrow$) | <151> | $t_{HSKSI}$ | | 10 | | ns |
| SOn output delay time (from $\overline{SCKn}\downarrow$) | <152> | $t_{DSKSO}$ | | | 30 | ns |
| SOn output hold time (from $\overline{SCKn}\uparrow$) | <153> | $t_{HSKSO}$ | | $t_{WSK1H}$ | | ns |

**Remark** n = 0 to 3




**Remarks 1.** Broken lines indicate high impedance.

**2.** n = 0 to 3

**A/D Converter Characteristics**

**($T_A$ = –40 to +85°C, $V_{DD}$ = $HV_{DD}$ = $CV_{DD}$ = $AV_{DD}$ = $AV_{REF}$ = 3.0 to 3.6 V, $V_{SS}$ = $CV_{SS}$ = $AV_{SS}$ = 0 V, output pin load capacitance: $C_L$ = 50 pF)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Resolution | – | | 10 | | | bit |
| Overall error | – | | | | ±5 | LSB |
| Quantization error | – | | | | ±1/2 | LSB |
| Conversion time | $t_{CONV}$ | | 5 | | 10 | μs |
| Sampling time | $t_{SAMP}$ | | Conversion clock[Note 1]/6 | | | ns |
| Zero scale error | – | | | | ±5 | LSB |
| Scale error | – | | | | ±5 | LSB |
| Linearity error | – | | | | ±3 | LSB |
| Analog input voltage | $V_{IAN}$ | | –0.3 | | $AV_{REF}$ + 0.3 | V |
| Analog input resistance | $R_{AN}$ | | | 1.0 | | MΩ |
| $AV_{REF}$ input voltage | $AV_{REF}$ | **Note 2** | 3.0 | | 3.6 | V |
| $AV_{REF}$ input current | $AI_{REF}$ | **Note 3** | | | 2.0 | mA |
| $AV_{DD}$ current | $AI_{DD}$ | | | | 5.0 | mA |

**Notes 1.** The conversion clock is the number of clocks converted via the ADM1 register.

★ **2.** Except in IDLE/software STOP mode

★ **3.** The current always flows regardless of the A/D converter operating status or standby mode. To further reduce the power consumption in IDLE/software STOP mode, make the voltage of the $AV_{REF}$ pin the same potential as $V_{SS}$.

## 4.2 Flash Memory Programming Mode

**Basic Characteristics**

**($T_A$ = –40 to +85°C (Other Than When Rewriting), $V_{DD}$ = $AV_{DD}$ = 3.0 to 3.6 V, $V_{SS}$ = $AV_{SS}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Operating frequency | $f_X$ | | 20 | | 33 | MHz |
| $V_{PP}$ power supply voltage | $V_{PP1}$ | During flash memory programming | 7.5 | 7.8 | 8.1 | V |
| | $V_{PPL}$ | $V_{PP}$ low-level detection | 0.8 $V_{DD}$ | | 1.2 $V_{DD}$ | V |
| | $V_{PPM}$ | $V_{PP}$, $V_{DD}$ level detection | 0.65 $V_{DD}$ | $V_{DD}$ | $V_{DD}$ +0.3 | V |
| | $V_{PPH}$ | $V_{PP}$ high-voltage level detection | 7.5 | 7.8 | 8.1 | V |
| Power supply current | $I_{DD}$ | $V_{PP}$ = $V_{PP1}$ | | 2.7 × $f_X$ | 4.5 × $f_X$ | mA |
| $V_{PP}$ supply current | $I_{PP}$ | $V_{PP}$ = 8.1 V | | | 150 | mA |
| Step erase time | $t_{ER}$ | K, P rank[Note 1] (Recommendation: Step erase = 5 s) | | 5 | | s |
| | | M rank[Note 1] (Recommendation: Step erase = 0.2 s) | | 0.2 | | s |
| Total erase time | $t_{ERA}$ | K, P rank[Note 1] When step erase time = 5 s, **Note 2** | | | 60 | s |
| | | M rank[Note 1] When step erase time = 0.2 s, **Note 2** | | | 20 | s |
| Writeback time | $t_{WB}$ | **Note 3**, K, P rank[Note 1] | 19.99 | 20 | 20.01 | ms |
| | | M rank[Note 1] | 0.99 | 1 | 1.01 | ms |
| Number of writebacks per writeback command | $C_{WB}$ | K, P rank[Note 1] When writeback time = 20 ms, **Note 4** | | | 10 | Times/ write-back command |
| | | M rank[Note 1] When writeback time = 1 ms, **Note 4** | | | 60 | |
| Number of erases – writebacks | $C_{ERWB}$ | | | | 16 | Times |

**Notes 1.** The rank is indicated by the fifth letter from the left of the lot number.

**2.** The prewrite time prior to erase and the erase verify time (writeback time) are not included.

**3.** The recommended set value for the writeback time is 1 ms (M rank) or 20 ms (K, P rank).

**4.** When the writeback command is issued, writeback is performed once. Therefore, set the retry count setting value to a value that is this value minus the number of command issuances.

**Caution The I rank applies to engineering samples only. The number of rewrites is not guaranteed for I rank products.**

**Remark** When the PG-FP3 or PG-FP4 is used, the time parameters required for write/erase are automatically set by downloading the parameter file. Do not change the set values unless otherwise specified.

**Basic Characteristics**

**($T_A$ = –40 to +85°C (Other Than When Rewriting), $V_{DD}$ = $AV_{DD}$ = 3.0 to 3.6 V, $V_{SS}$ = $AV_{SS}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Step write time | $t_{WT}$ | **Note 1** | | 18 | 20 | 22 | μs |
| Total write time per word | $t_{WTW}$ | Step write time is set to 20 μs (1 word = 4 bytes), **Note 2** | | 20 | | 200 | μs /word |
| ★ Number of rewrites | $C_{ERWR}$ | One erase + one write after erase are taken as one rewrite, **Note 3** | K rank[Note 4] | 5 | | | Times |
| | | | P rank[Note 4] | 10 | | | Times |
| | | | M rank[Notes 4, 5] | 20 | | | Times |
| | | | M rank[Notes 4, 6] | 100 | | | Times |
| Temperature during write | $T_{PRG}$ | K, P rank[Note 4] | | 10 | | 40 | °C |
| | | M rank[Note 4] | | 10 | | 85 | °C |

**Notes 1.** The recommended set value for the step write time is 20 μs.

**2.** The actual write time per word is longer than this value by 100 μs. This value does not include the internal verify time during and after writing.

**3.** When a shipped product is written for the first time, both “write after erase” and “write only” are taken as one write.

**Example** (P: write, E: erase)

Product ——→ P → E → P → E → P Three rewrites

Product → E → P → E → P → E → P Three rewrites

**4.** The rank is indicated by the fifth letter from the left of the lot number.

★ **5.** Lot number 0120Mxxxx or earlier

★ **6.** Lot number 0121Mxxxx or later

**Caution The I rank applies to engineering samples only. The number of rewrites is not guaranteed for I rank products.**

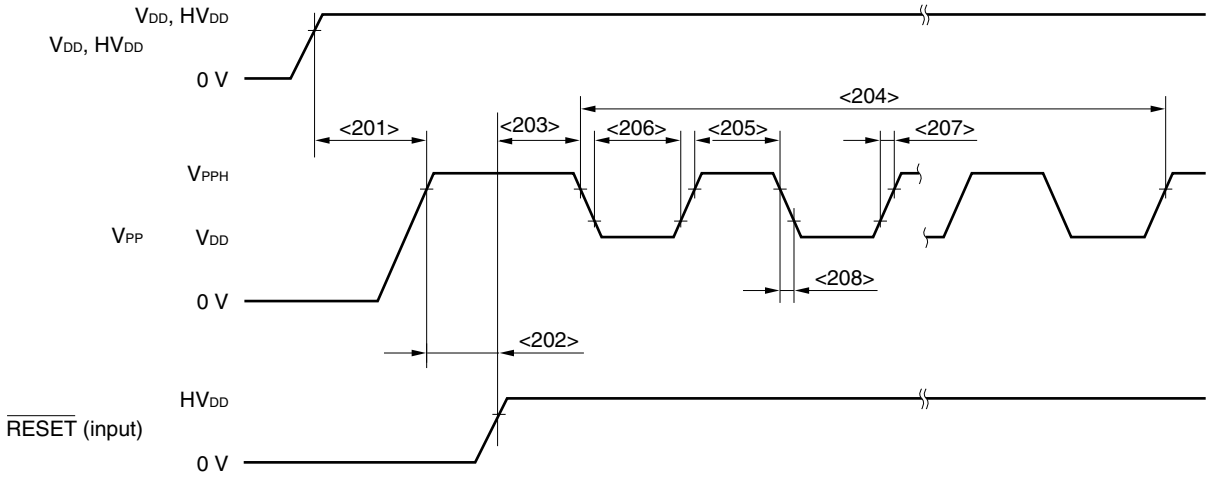
**Remarks 1.** When the PG-FP3 or PG-FP4 is used, the time parameters required for write/erase are automatically set by downloading the parameter file. Do not change the set values unless specified.

★ **2.** In the lot number, the two digits from the left (“01” in Notes 5, 6) indicate the lower 2 digits of the manufacture year and the 3rd and 4th digits from the left (“20” in Note 5 and “21” in Note 6) indicate the week of manufacture.

For example, Note 6 corresponds to products manufactured in 21th week or later (21, 22, 23…) in 2001.

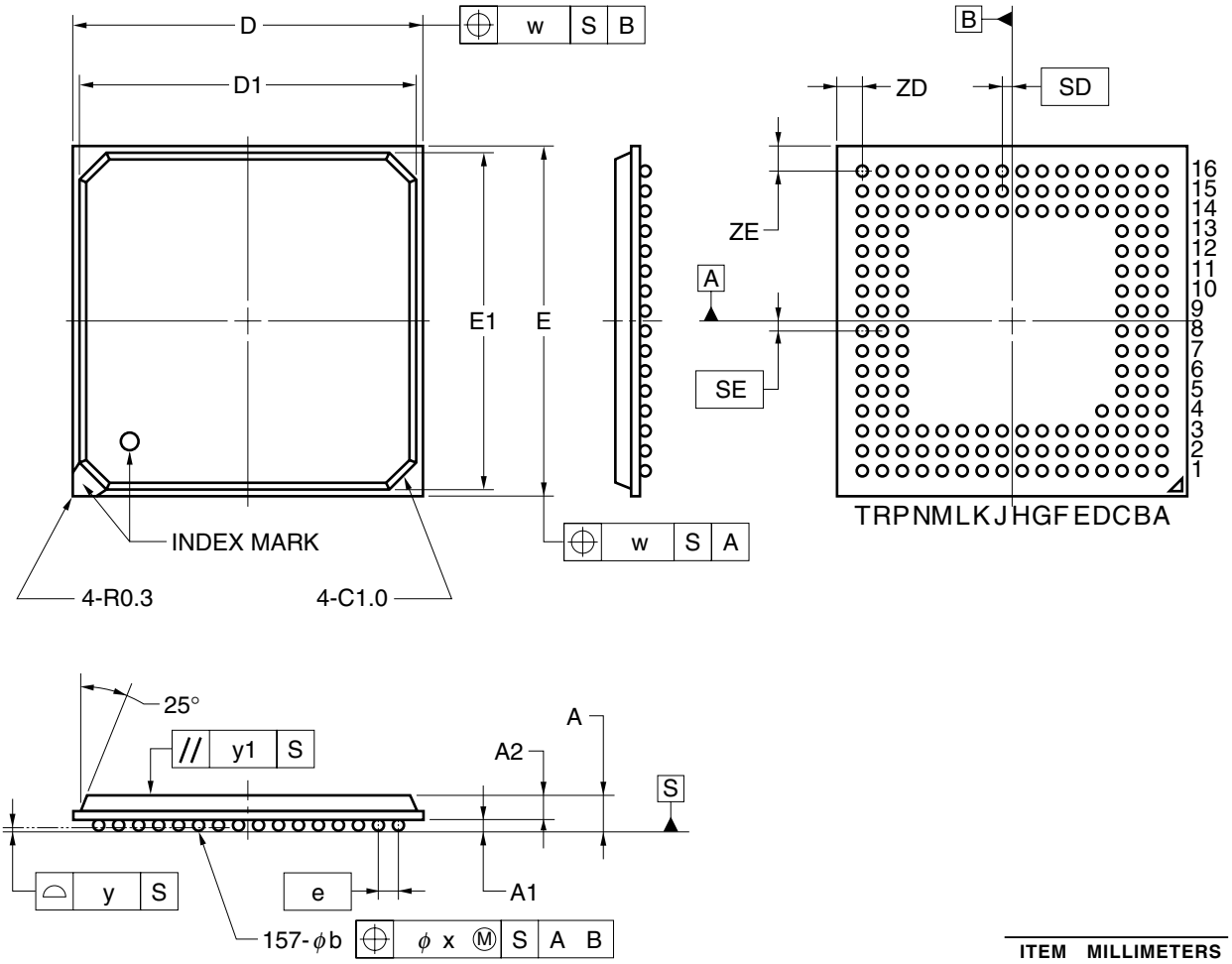
**Serial Write Operation Characteristics**

| Parameter | Symbol | | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Set time from $V_{DD}$↑ to $V_{PP}$↑ | <201> | $t_{DRPSR}$ | | 200 | | | ns |
| Set time from $V_{PP}$↑ to $\overline{RESET}$↑ | <202> | $t_{PSRRF}$ | | 1 | | | μs |
| $\overline{RESET}$↑ to $V_{PP}$ count start time | <203> | $t_{RFOF}$ | $V_{PP}$ = 7.8 V | 5T + 500 | | | μs |
| Count execution time | <204> | $t_{COUNT}$ | | | | 10 | ms |
| $V_{PP}$ counter high-level width | <205> | $t_{CH}$ | | 1 | | | μs |
| $V_{PP}$ counter low-level width | <206> | $t_{CL}$ | | 1 | | | μs |
| $V_{PP}$ counter rise time | <207> | $t_R$ | | | | 3 | μs |
| $V_{PP}$ counter fall time | <208> | $t_F$ | | | | 3 | μs |



## 5. PACKAGE DRAWINGS

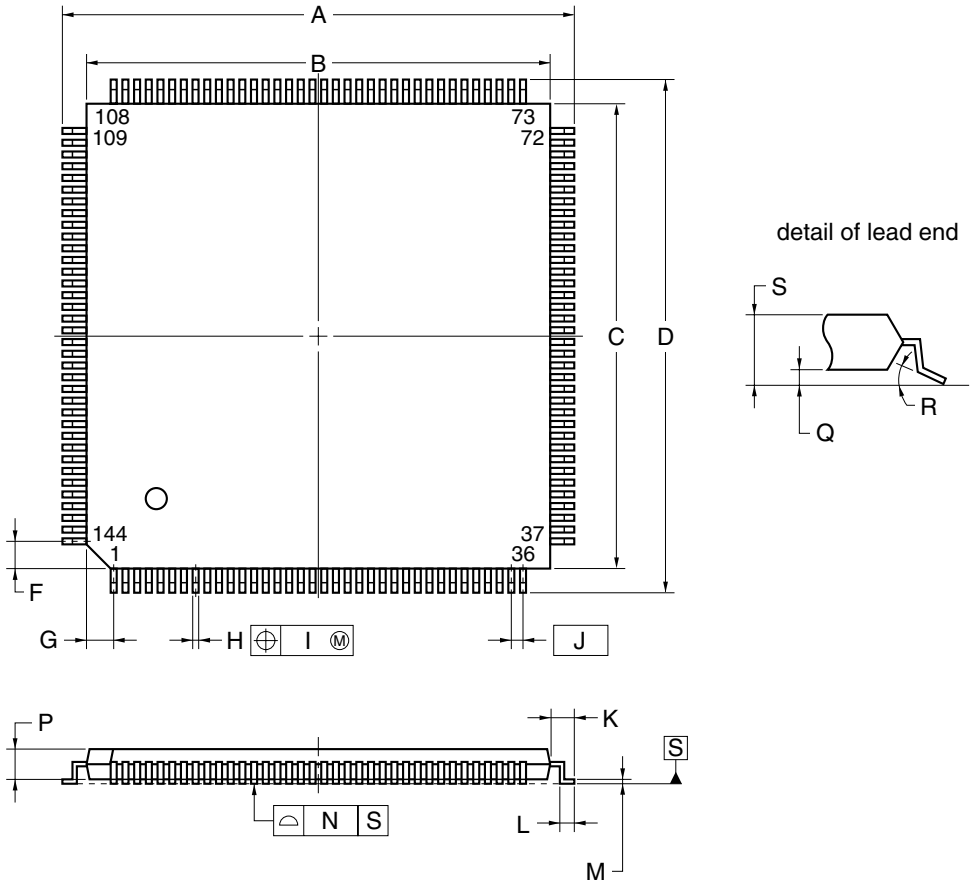
### 157-PIN PLASTIC FBGA (14x14)




| ITEM | MILLIMETERS |
|---|---|
| D | 14.0±0.1 |
| D1 | 13.4 |
| E | 14.0±0.1 |
| E1 | 13.4 |
| w | 0.20 |
| e | 0.8 |
| A | 1.31±0.15 |
| A1 | 0.35±0.10 |
| A2 | 0.96 |
| b | $0.5^{+0.05}_{-0.10}$ |
| x | 0.08 |
| y | 0.10 |
| y1 | 0.2 |
| SD | 0.4 |
| SE | 0.4 |
| ZD | 1.0 |
| ZE | 1.0 |

S157F1-80-FA1

## 144-PIN PLASTIC LQFP (FINE PITCH) (20x20)



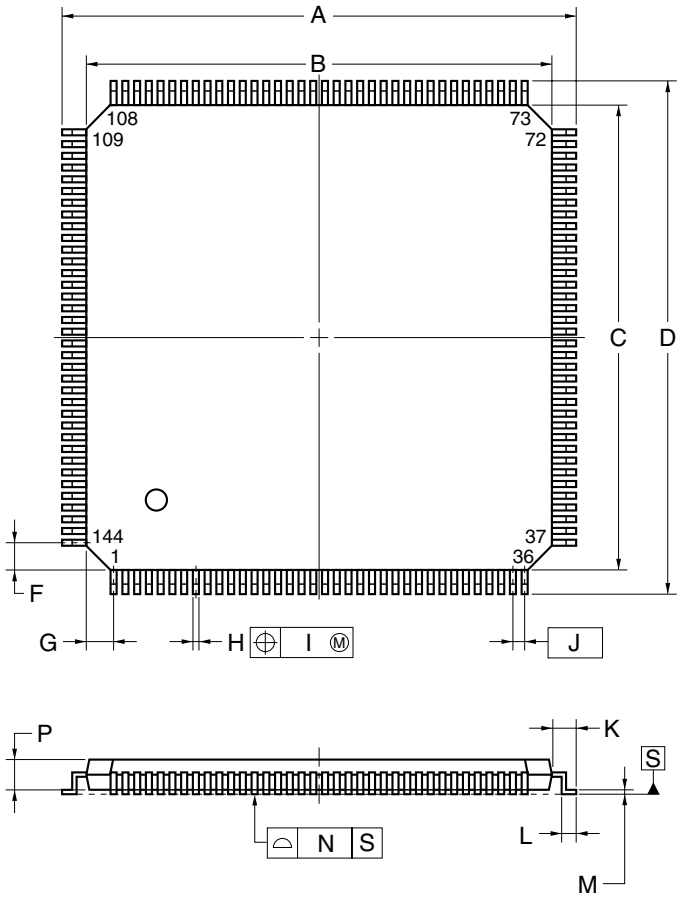

**NOTE**

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

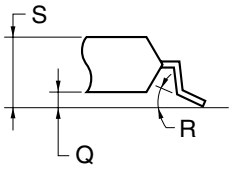
| ITEM | MILLIMETERS |
|---|---|
| A | 22.0±0.2 |
| B | 20.0±0.2 |
| C | 20.0±0.2 |
| D | 22.0±0.2 |
| F | 1.25 |
| G | 1.25 |
| H | $0.22^{+0.05}_{-0.04}$ |
| I | 0.10 |
| J | 0.5 (T.P.) |
| K | 1.0±0.2 |
| L | 0.5±0.2 |
| M | $0.145^{+0.055}_{-0.045}$ |
| N | 0.10 |
| P | 1.4±0.1 |
| Q | 0.125±0.075 |
| R | $3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$ |
| S | 1.7 MAX. |

**S144GJ-50-8EU-3**

## 144-PIN PLASTIC LQFP (FINE PITCH) (20x20)




detail of lead end




**NOTE**

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 22.0±0.2 |
| B | 20.0±0.2 |
| C | 20.0±0.2 |
| D | 22.0±0.2 |
| F | 1.25 |
| G | 1.25 |
| H | 0.22±0.05 |
| I | 0.08 |
| J | 0.5 (T.P.) |
| K | 1.0±0.2 |
| L | 0.5±0.2 |
| M | $0.17^{+0.03}_{-0.07}$ |
| N | 0.08 |
| P | 1.4 |
| Q | 0.10±0.05 |
| R | $3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$ |
| S | 1.5±0.1 |

**S144GJ-50-UEN**

## 6. RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual** (**C10535E**).

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

**Caution The soldering conditions of the μPD70F3102AGJ-33-UEN are yet to be determined.**

**Table 6-1. Surface Mounting Type Soldering Conditions**

**(1) μPD70F3102AF1-33-FA1: 157-pin plastic FBGA (14 × 14)**

| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 230°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours) | IR30-103-2 |

**Note** After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

**(2) μPD70F3102AGJ-33-8EU: 144-pin plastic LQFP (Fine Pitch) (20 × 20)**

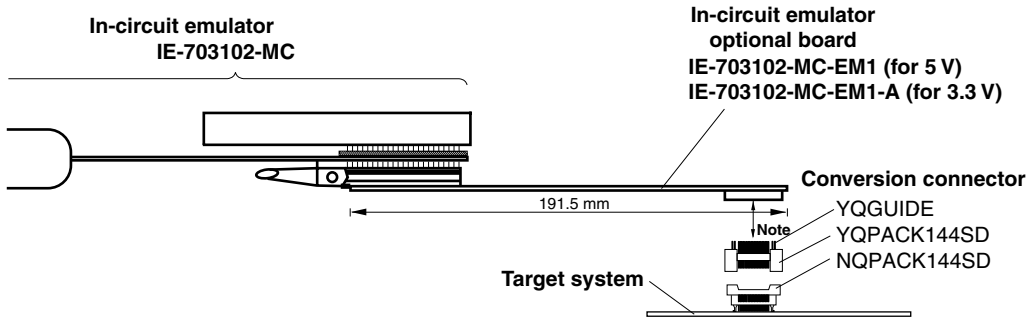
| Soldering Method | Soldering Conditions | Recommended Condition Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Twice or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours) | IR35-103-2 |
| VPS | Package peak temperature: 215°C, Time: Within 25 to 40 seconds (at 200°C or higher), Count: Twice or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours) | VP15-103-2 |
| Partial heating | Pin temperature: 350°C max., Time: 3 seconds max. (per pin row) | – |

**Note** After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

## APPENDIX NOTES ON DESIGNING TARGET SYSTEM

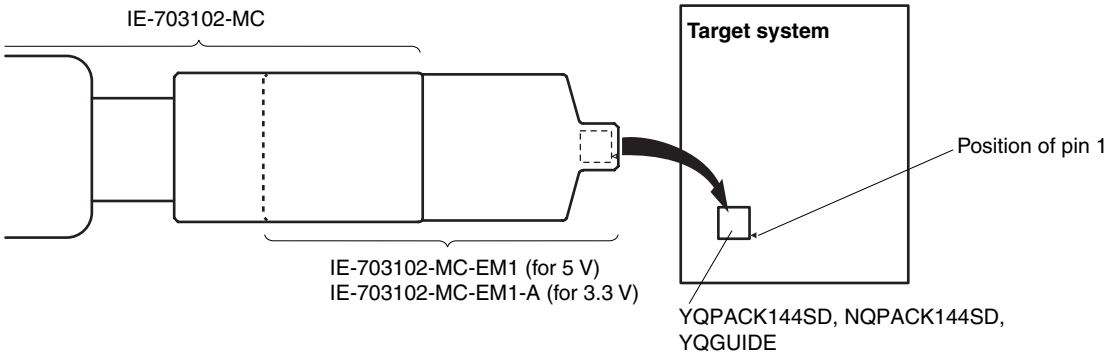
The following shows the connection condition diagrams between in-circuit emulator optional board and conversion connector.

Side View

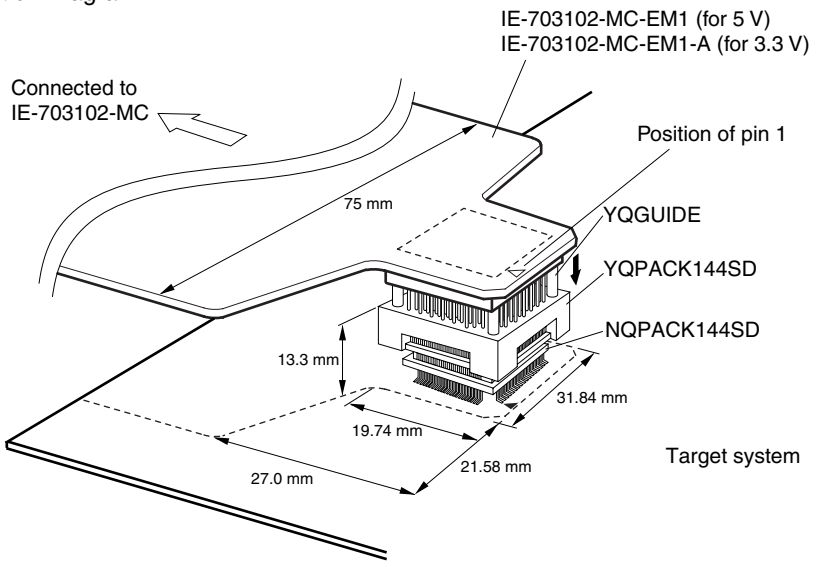



**Note** YQSOCKET144SDN (separately available) can be inserted here to adjust the height (height: 3.2 mm).

Top View

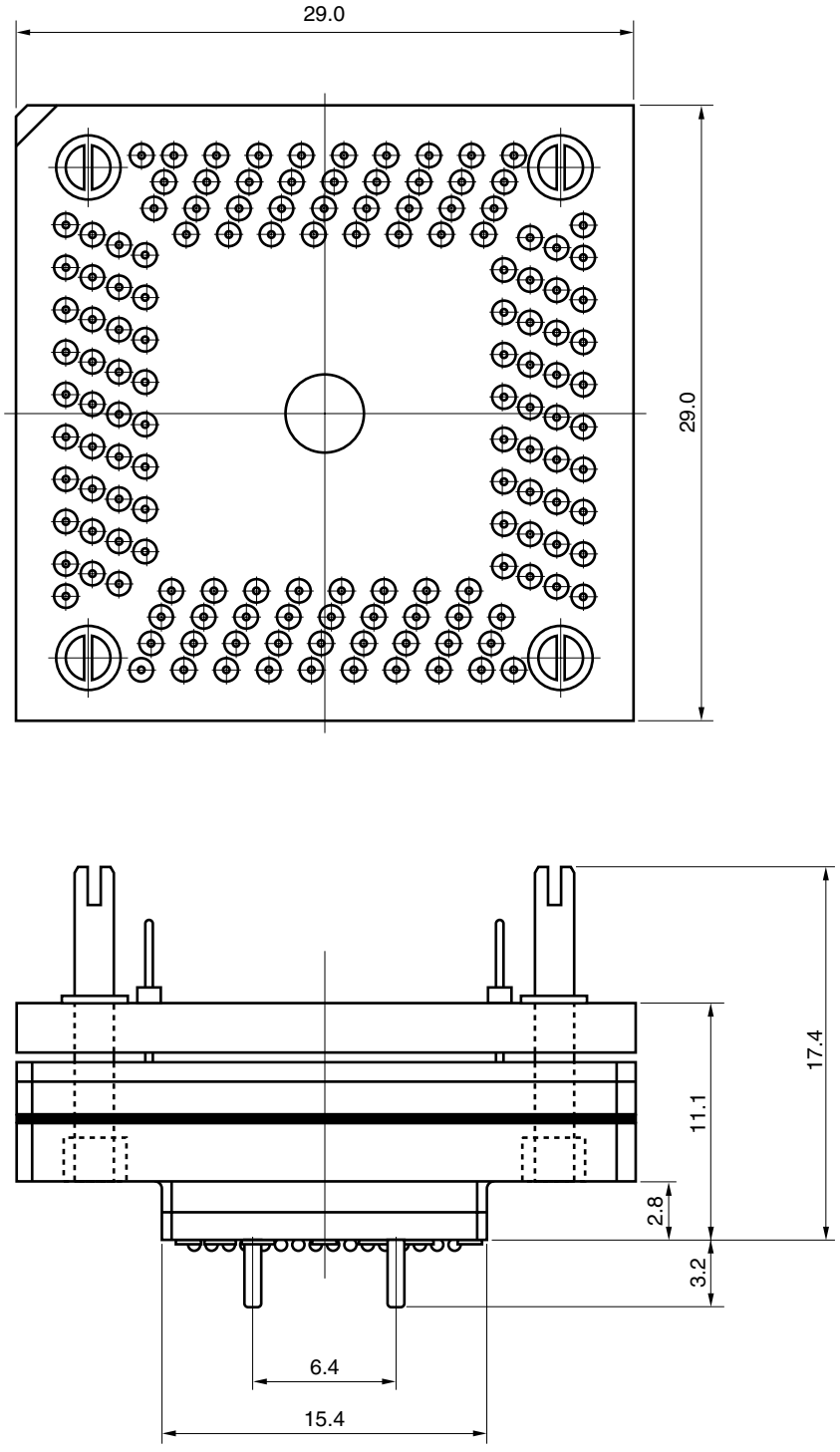



Connection Condition Diagram




The following shows the conversion connector for the 157-pin FBGA package.

157-pin conversion connector for FBGA package
(CSPACK157A1614N01 + CSICE157A1614N01)




**Remarks 1.** The target device of the 157-pin conversion connector for FBGA package is V850E/MS1 only.

**2.** Unit: mm

[MEMO]

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

**Related Documents** μPD70F3102-33 Data Sheet (U13844E)
μPD703100-33, 703100-40, 703101-33, 703102-33 Data Sheet (U13995E)
μPD703100A-33, 703100A-40, 703101A-33, 703102A-33 Data Sheet (U14168E)

**The related documents in this publication may include preliminary versions. However, preliminary versions are not marked as such.**

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- Availability of related technical literature
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- Network requirements

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